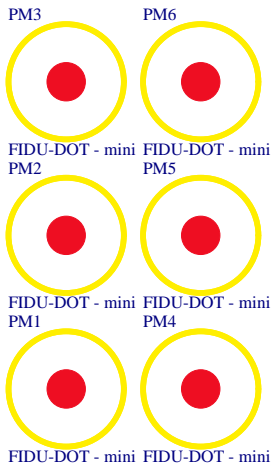
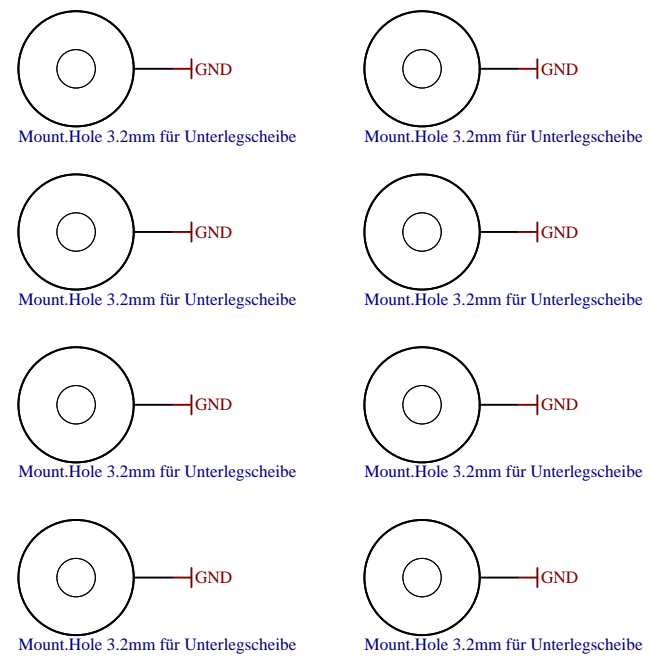


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U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	U_POWER_3 POWER_3.SchDoc
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_4.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	U_RC Revision_Changes.SchDoc
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	
U_B_GT_2 B_GT_2.SchDoc	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	

Special notes:



Serial  
Serialnummer 6,3 x 6.3mm

MECHI  
TE Address Overlay

LOGO ADDRESS

LOGO1  
TE Logo PRINT Layer

LOGO PRINT

Design drawn by:	VY
Checked by:	MR
Assembly variant:	BBE81-A
Created by:	ED
Modified by:	ED
Modified at:	2022-07-25



Title: TE0808		
A4	Number: TE0808 BBE81-A	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 1 of 28
Filename: TE0808.SchDoc		

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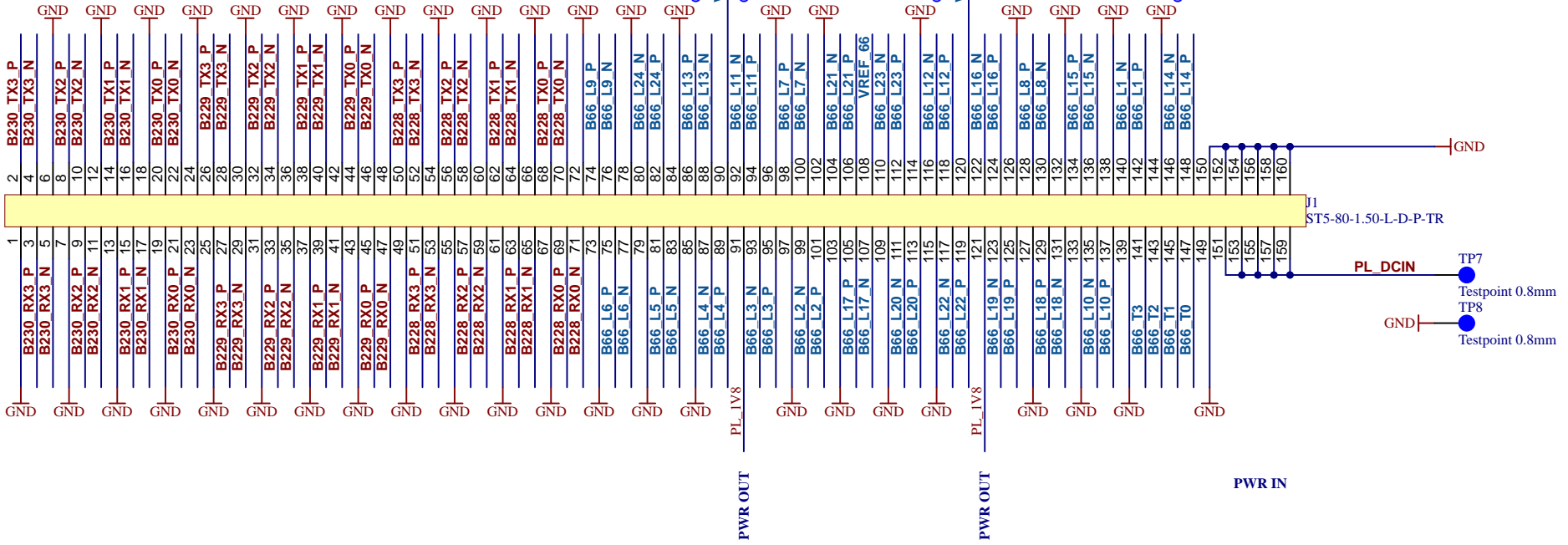
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Title: TE0808 - Connector J1		
A4	Number: TE0808 BBE81-A	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 2 of 28
Filename: J1.SchDoc		

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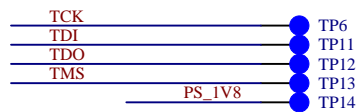
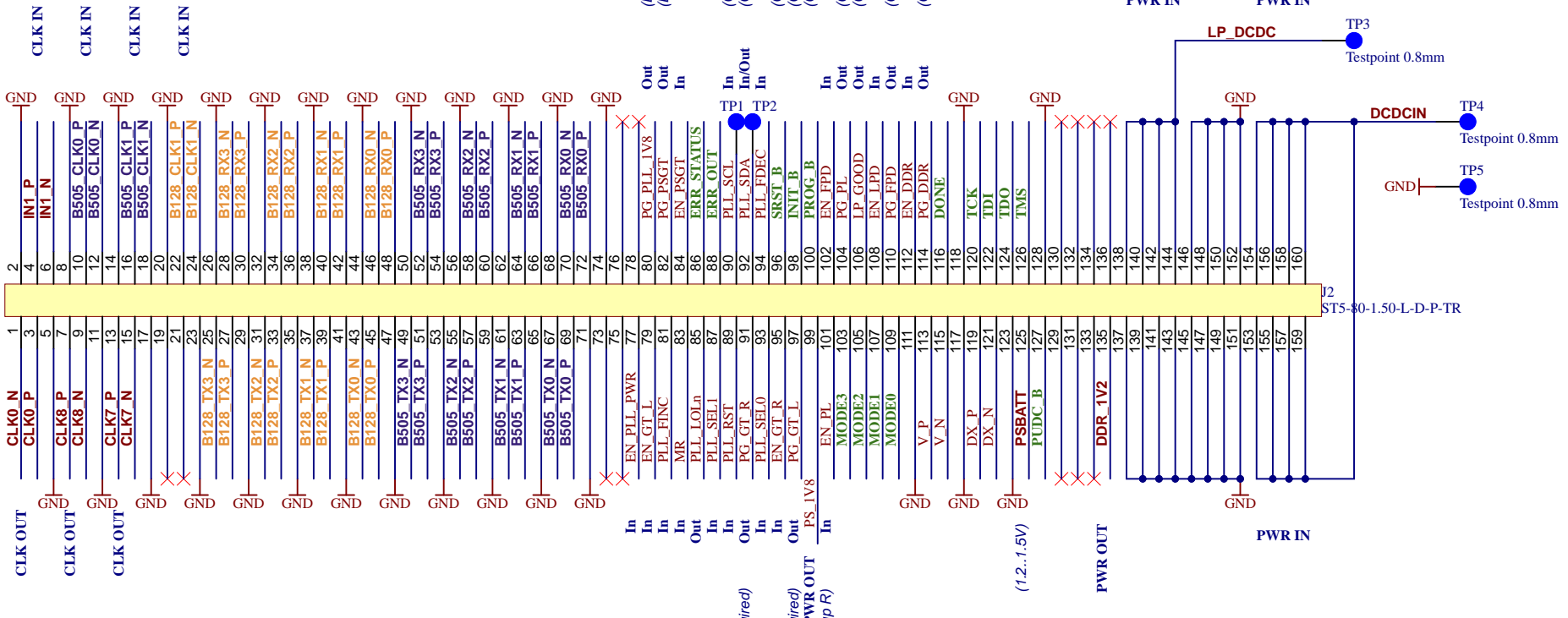
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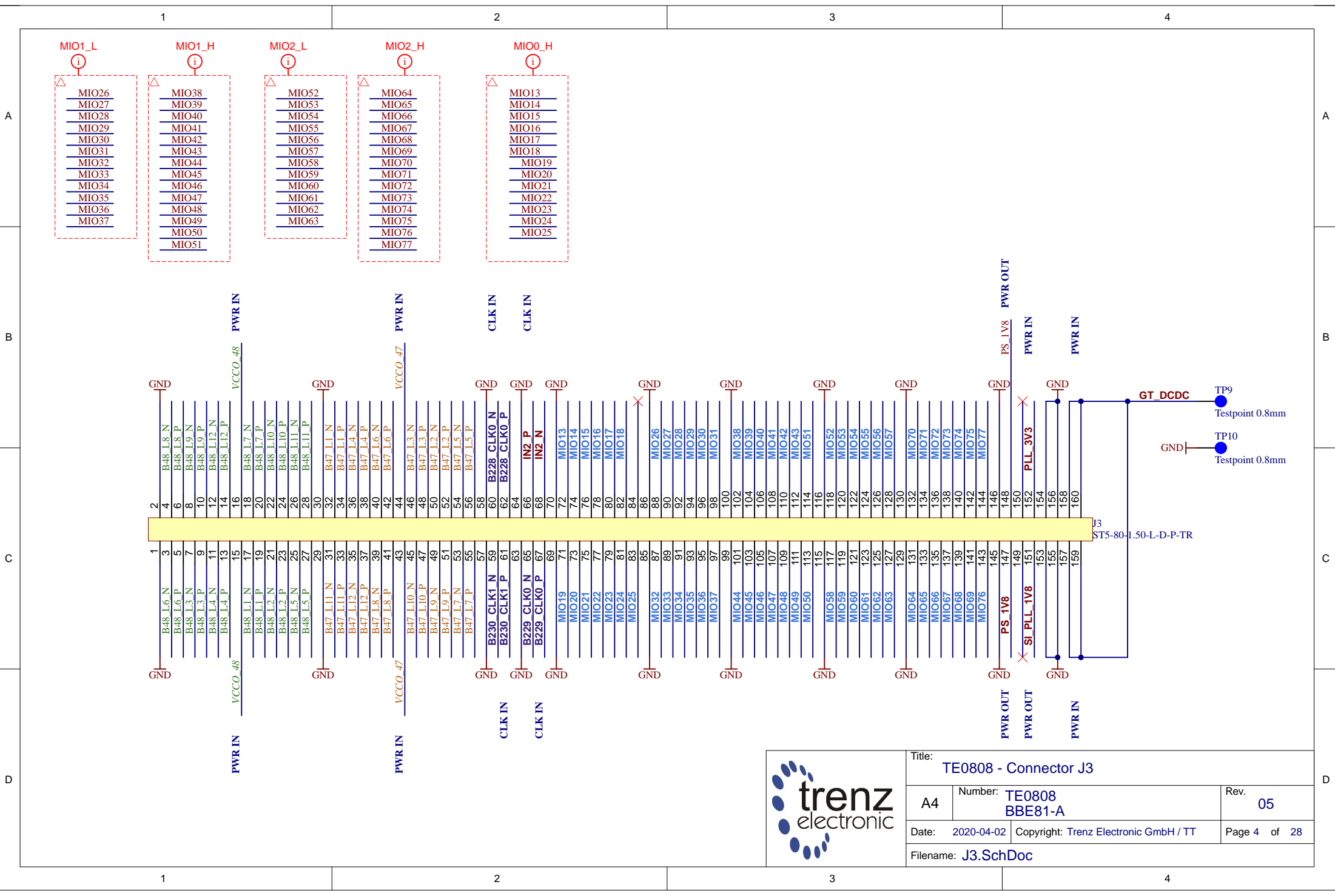
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A4	Number: TE0808 BBE81-A	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 3 of 28
Filename: J2.SchDoc		

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Title: TE0808 - Connector J3		
A4	Number: TE0808 BBE81-A	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 4 of 28
Filename: J3.SchDoc		

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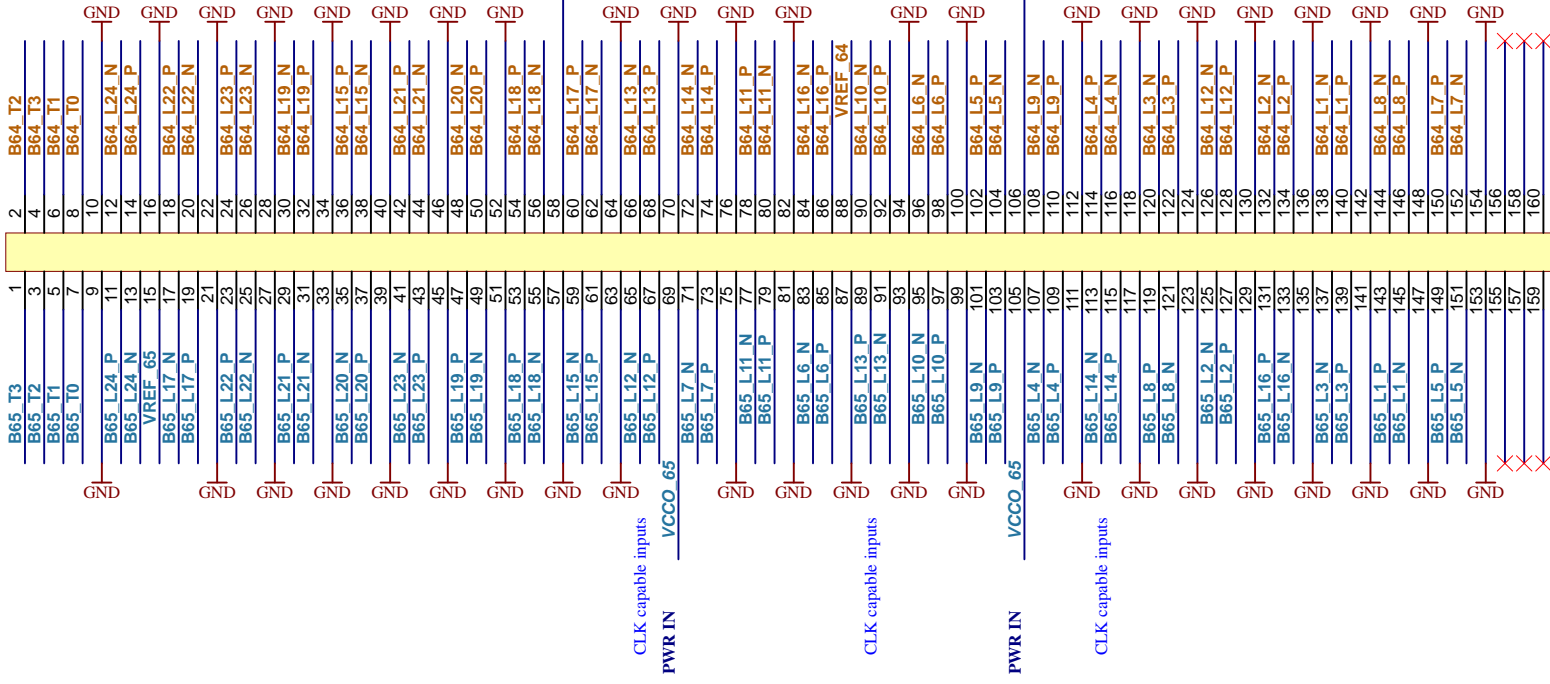
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J4  
ST5-80-1.50-L-D-P-TR



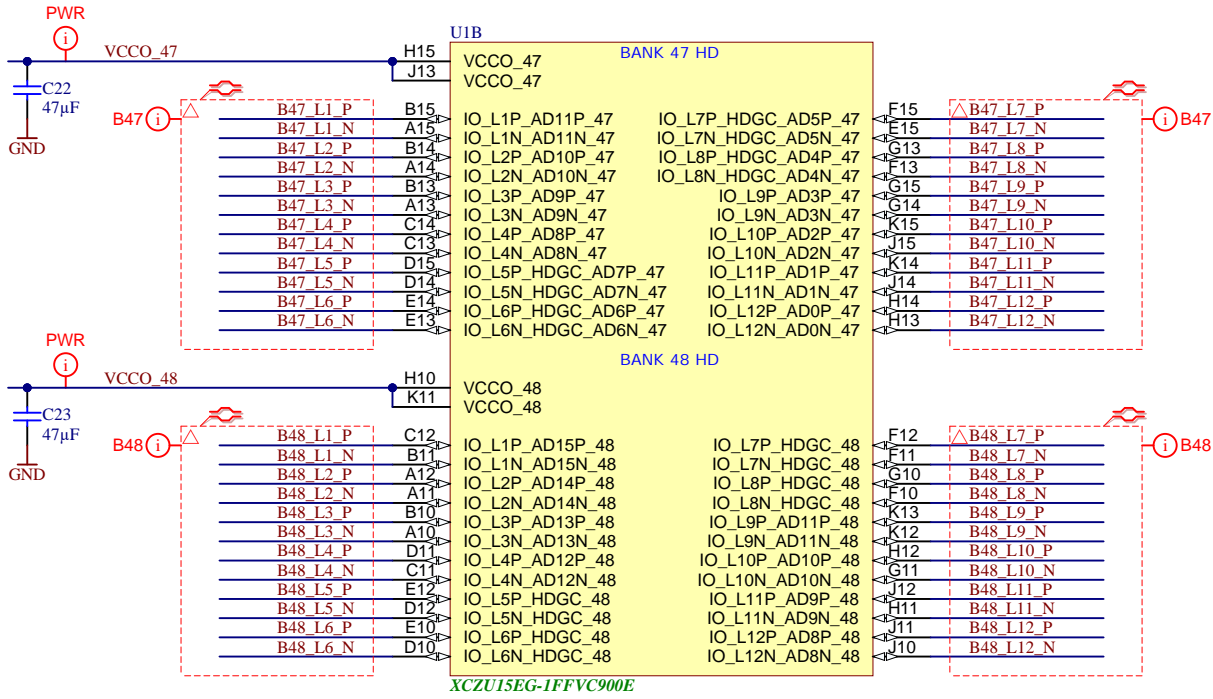
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Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 5 of 28
Filename: J4.SchDoc		

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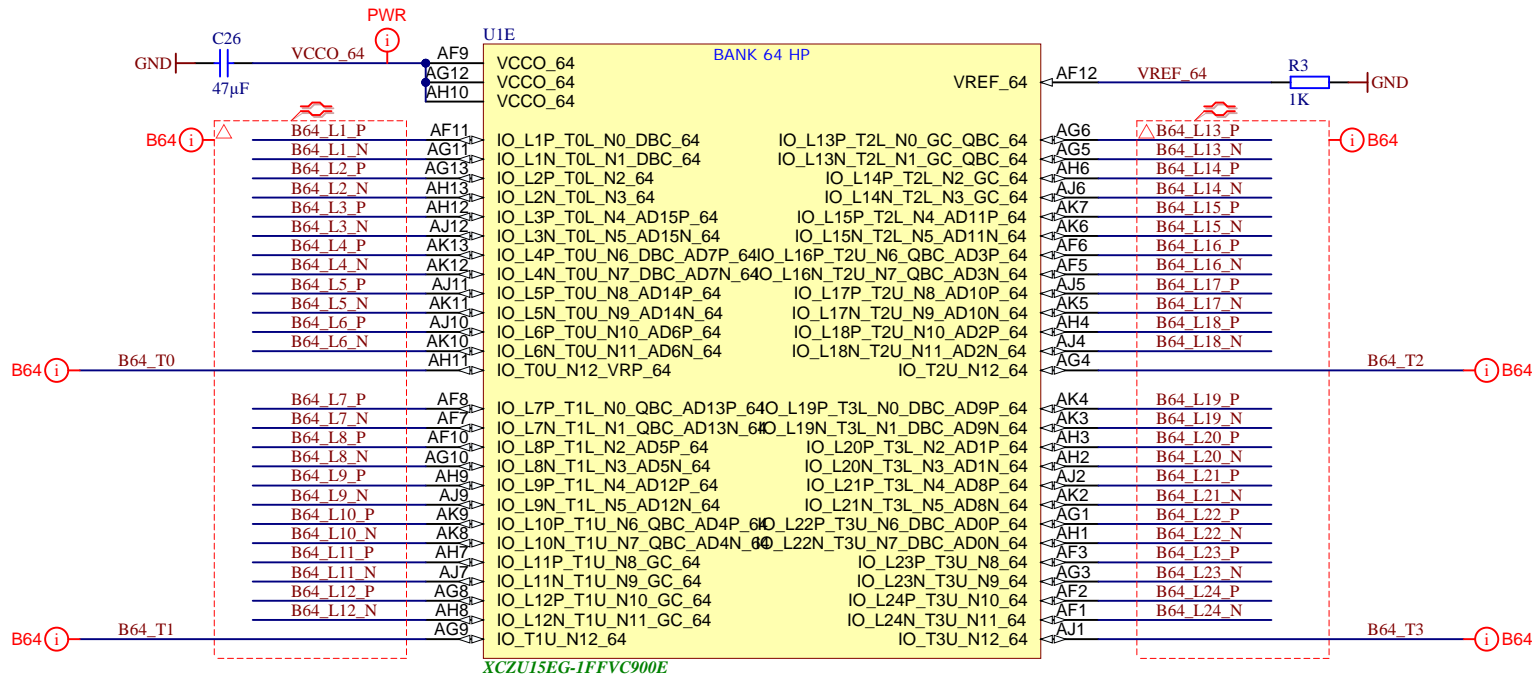
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Title: TE0808 - B47HD and B48HD		
A4	Number: TE0808 BBE81-A	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 6 of 28
Filename: B_HD.SchDoc		

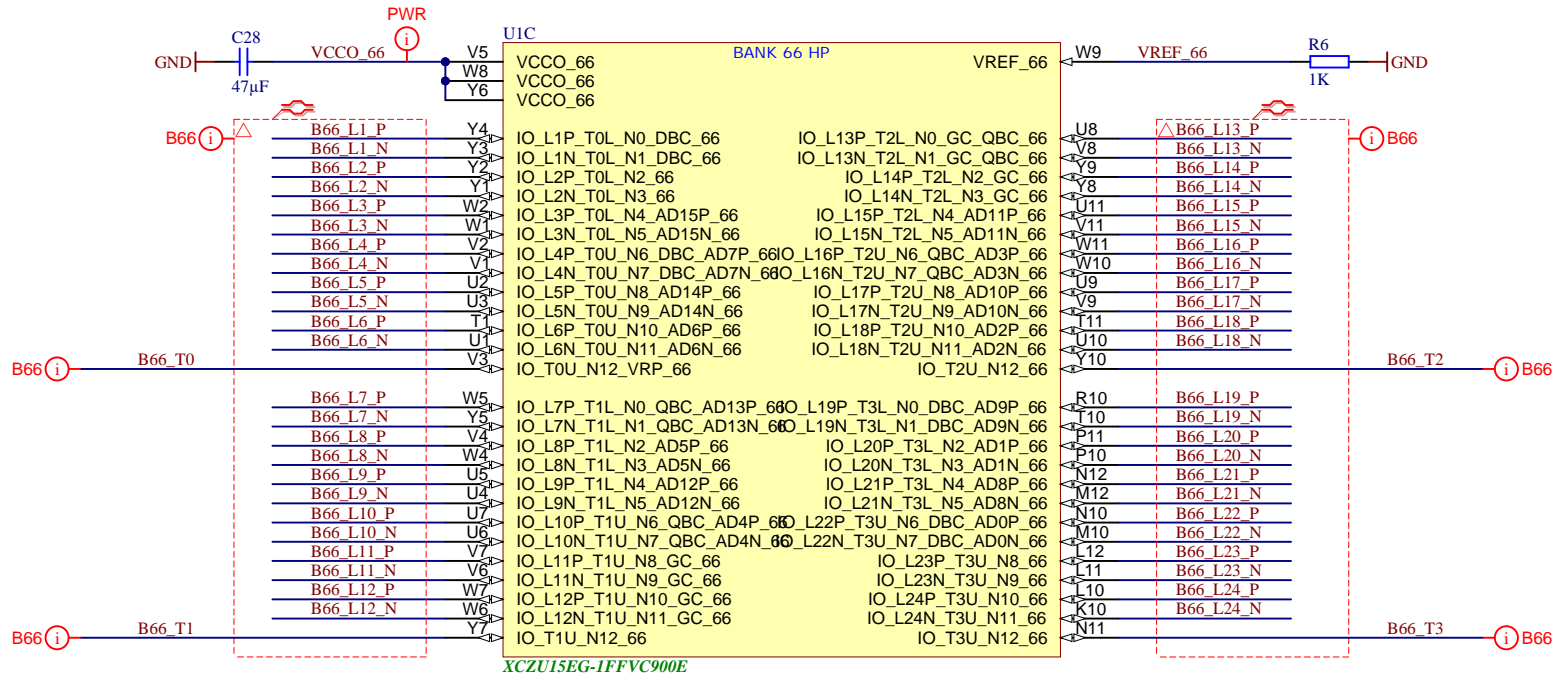





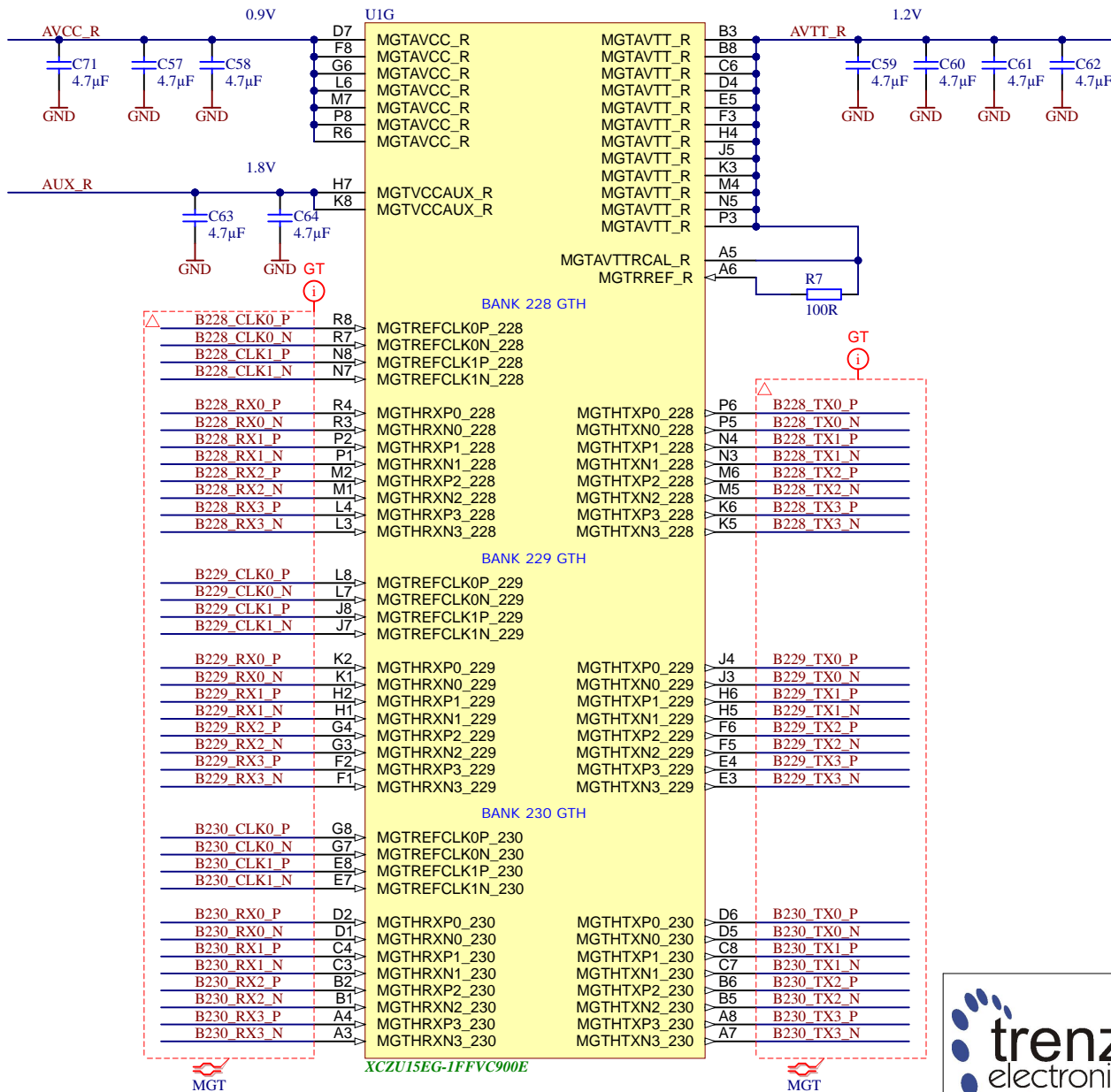
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	Rev. <b>05</b>	Page <b>8</b> of <b>28</b>
Filename: <b>B64.SchDoc</b>		



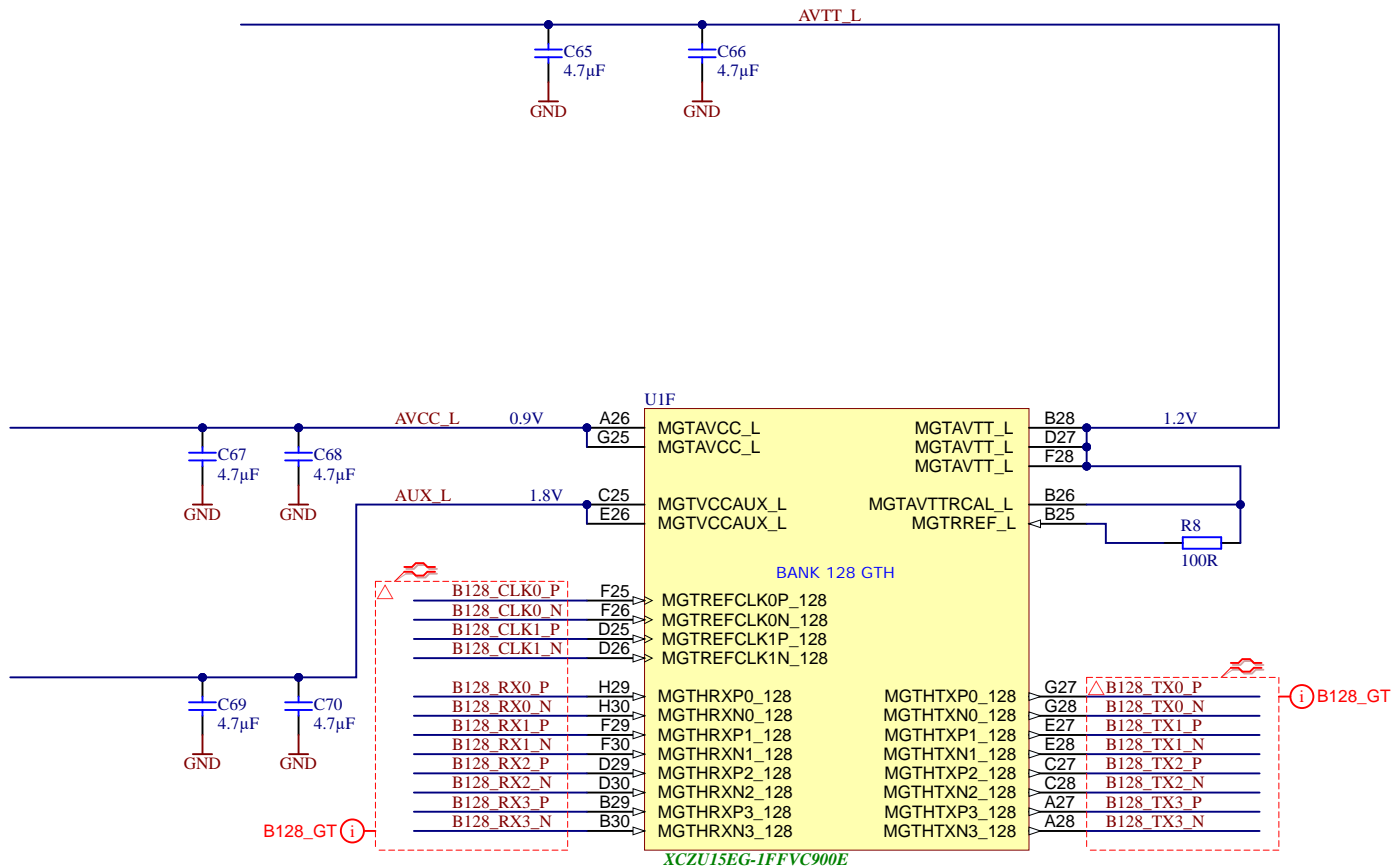




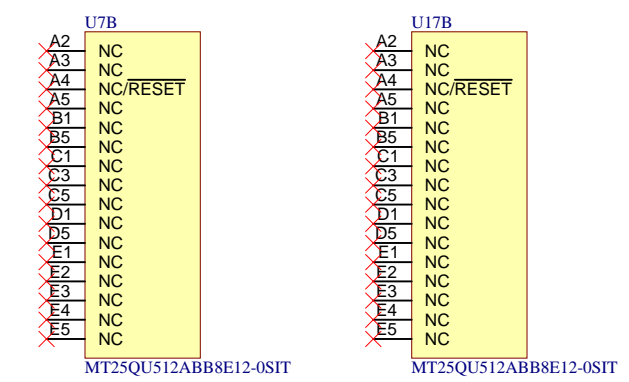
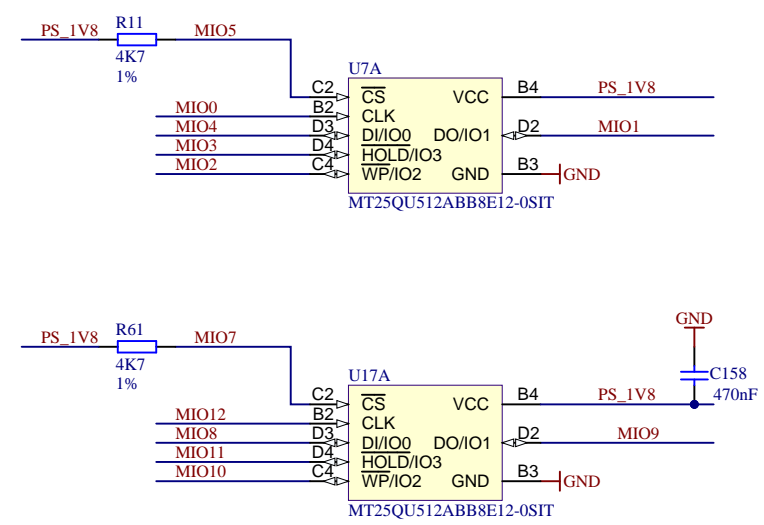
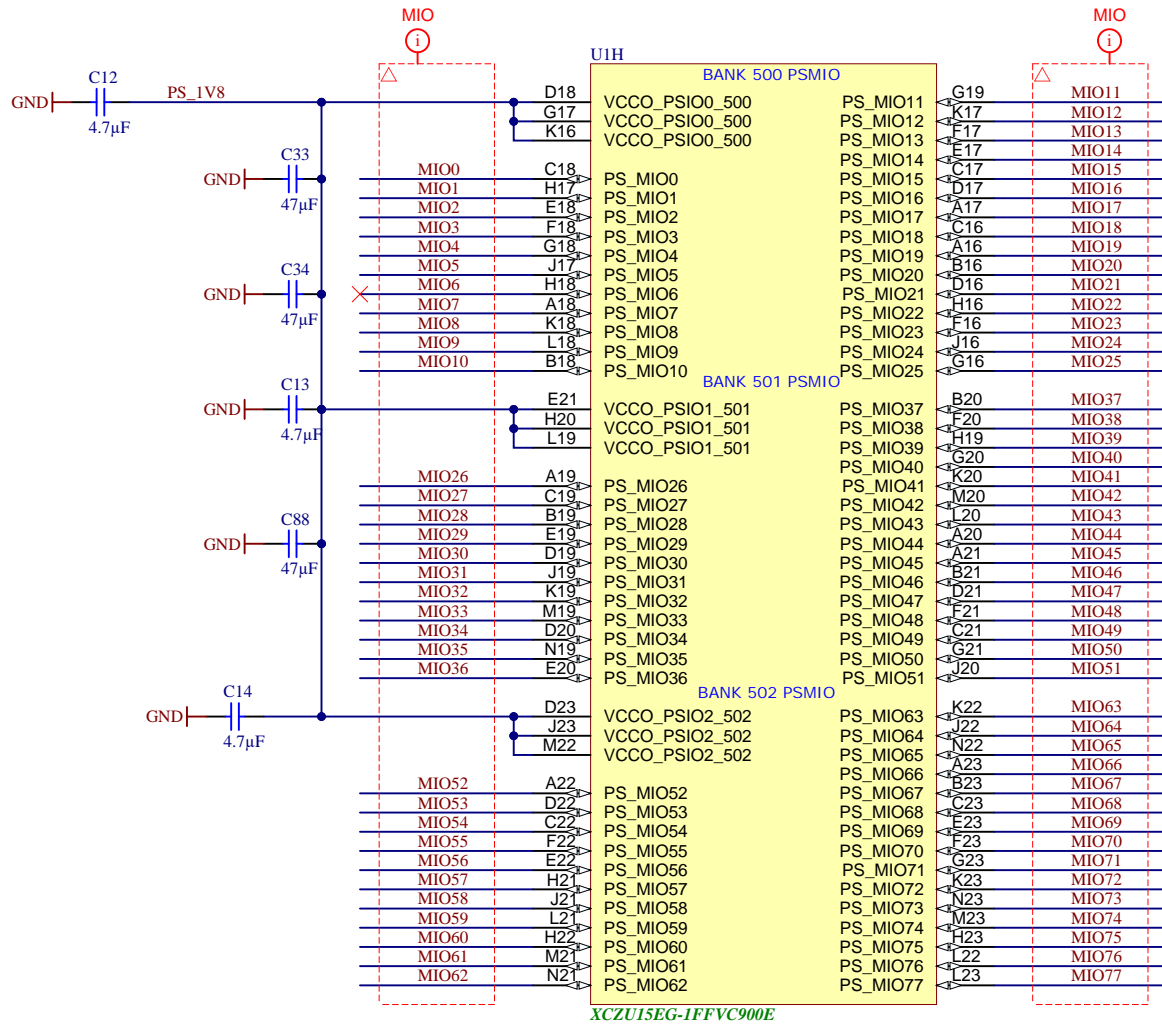
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Date: 2020-04-02		Copyright: Trenz Electronic GmbH / TT	
Filename: B66.SchDoc		Page 10 of 28	



Title: <b>TE0808 - B228GTH_B229GTH_B230GTH</b>		
A4	Number: <b>TE0808 BBE81-A</b>	Rev. <b>05</b>
Date: <b>2020-04-02</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>11</b> of <b>28</b>
Filename: <b>B_GT.SchDoc</b>		



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	Filename: B_GT_2.SchDoc	
	Rev. 05	Page 12 of 28



Title: TE0808 - MIO Banks		
A4	Number: TE0808 BBE81-A	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 13 of 28
Filename: B_MIO.SchDoc		

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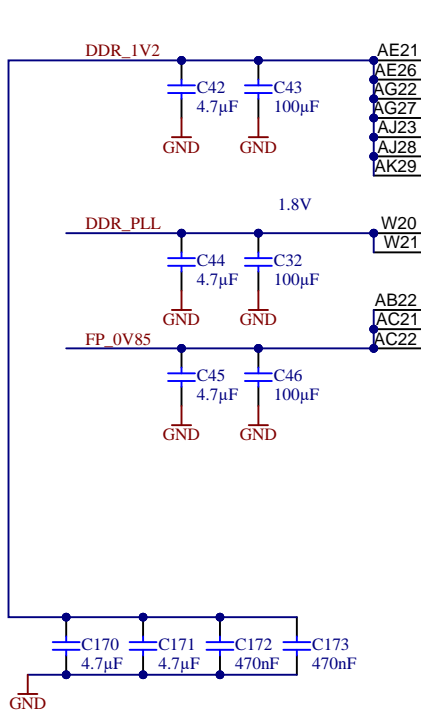
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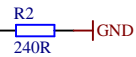
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VCCO_PSDDR_504	PS_DDR_CKE0	AJ25	DDR4-CKE0
VCCO_PSDDR_504		AG23	
VCCO_PSDDR_504	PS_DDR_CK1	AG24	
VCCO_PSDDR_504	PS_DDR_CK_N1	AH27	
VCCO_PSDDR_504	PS_DDR_CKE1	AH27	
VCC_PSDDR_PLL	PS_DDR_A0	AK25	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1	AK28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2	AK27	DDR4-A2
	PS_DDR_A3	AH24	DDR4-A3
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XCZU15EG-1FFVC900E



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		PS_DDR_DQ444	PS_DDR_DQ445
		PS_DDR_DQ446	PS_DDR_DQ447
		PS_DDR_DQ448	PS_DDR_DQ449
		PS_DDR_DQ450	PS_DDR_DQ451
		PS_DDR_DQ452	PS_DDR_DQ453
		PS_DDR_DQ454	PS_DDR_DQ455
		PS_DDR_DQ456	PS_DDR_DQ457
		PS_DDR_DQ458	PS_DDR_DQ459
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		PS_DDR_DQ462	PS_DDR_DQ463
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		PS_DDR_DQ468	PS_DDR_DQ469
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		PS_DDR_DQ472	PS_DDR_DQ473
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		PS_DDR_DQ482	PS_DDR_DQ483
		PS_DDR_DQ484	PS_DDR_DQ485
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		PS_DDR_DQ488	PS_DDR_DQ489
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		PS_DDR_DQ492	PS_DDR_DQ493
		PS_DDR_DQ494	PS_DDR_DQ495
		PS_DDR_DQ496	PS_DDR_DQ497
		PS_DDR_DQ498	PS_DDR_DQ499
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		PS_DDR_DQ502	PS_DDR_DQ503
		PS_DDR_DQ504	PS_DDR_DQ505
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		PS_DDR_DQ522	PS_DDR_DQ523
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		PS_DDR_DQ526	PS_DDR_DQ527
		PS_DDR_DQ528	PS_DDR_DQ529
		PS_DDR_DQ530	PS_DDR_DQ531
		PS_DDR_DQ532	PS_DDR_DQ533
		PS_DDR_DQ534	PS_DDR_DQ535
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A

A

B

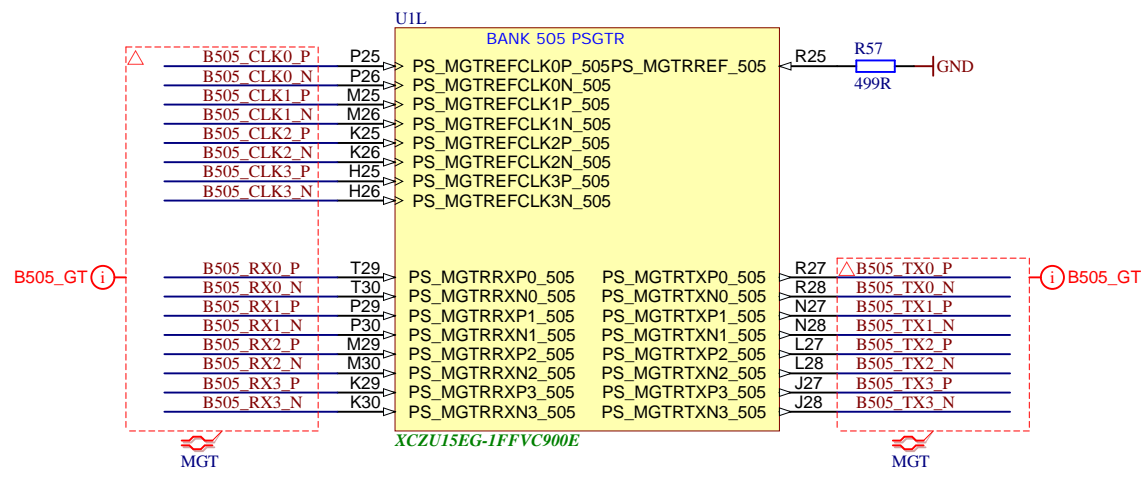
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C

C

D

D



Title: TE0808 - PS_GT		
A4	Number: TE0808 BBE81-A	Rev. 05
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Filename: B_PS_GT.SchDoc		

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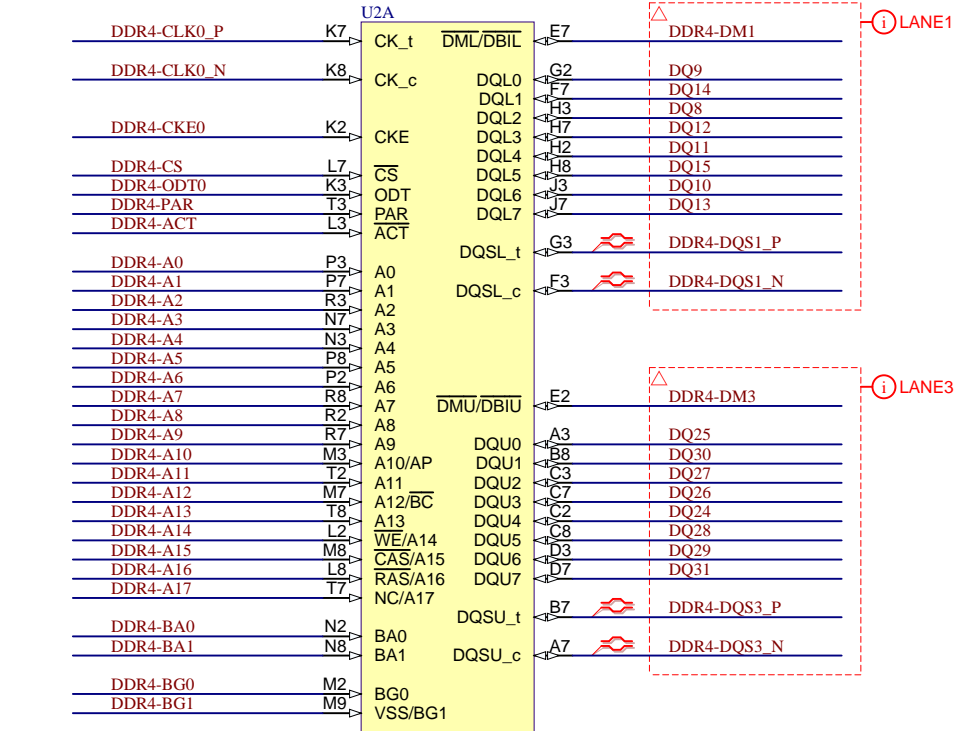
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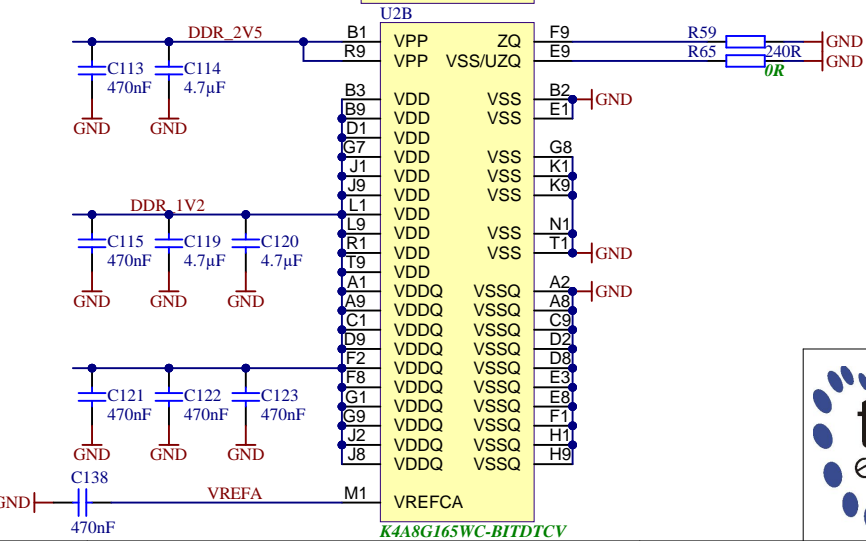




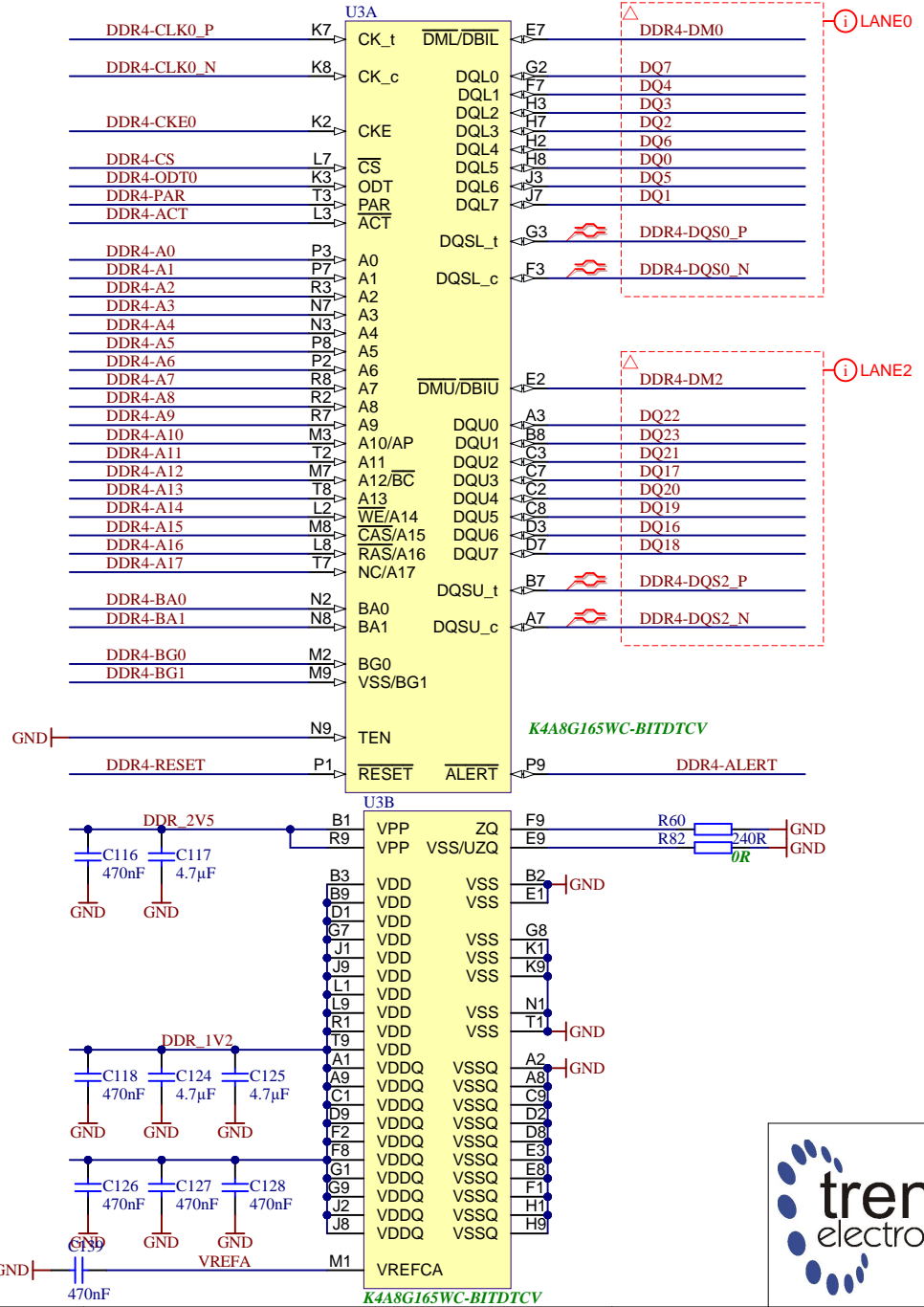




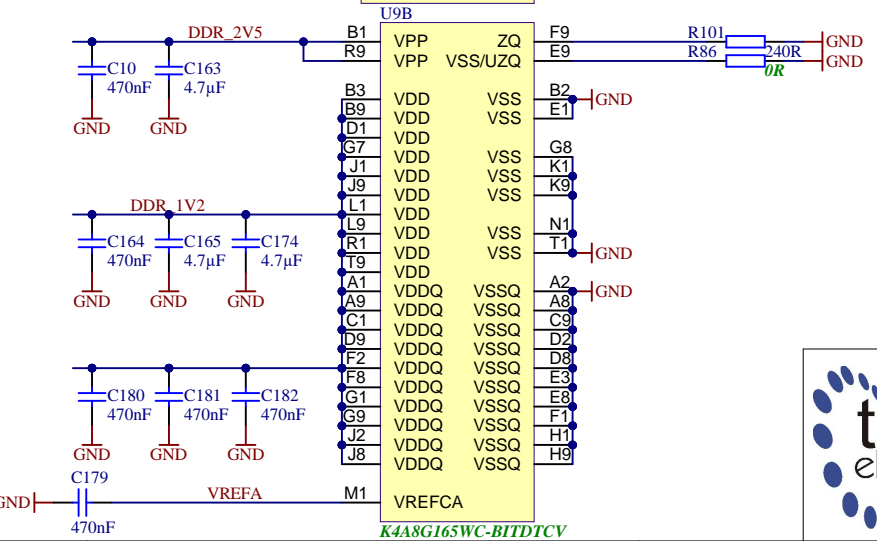
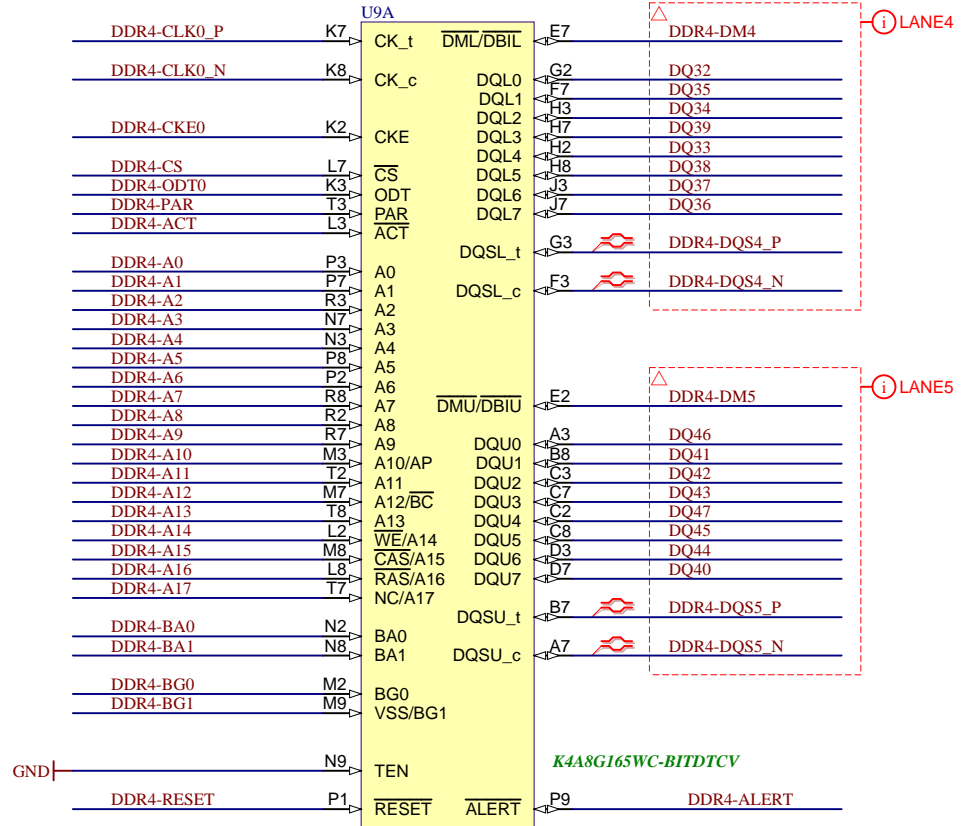
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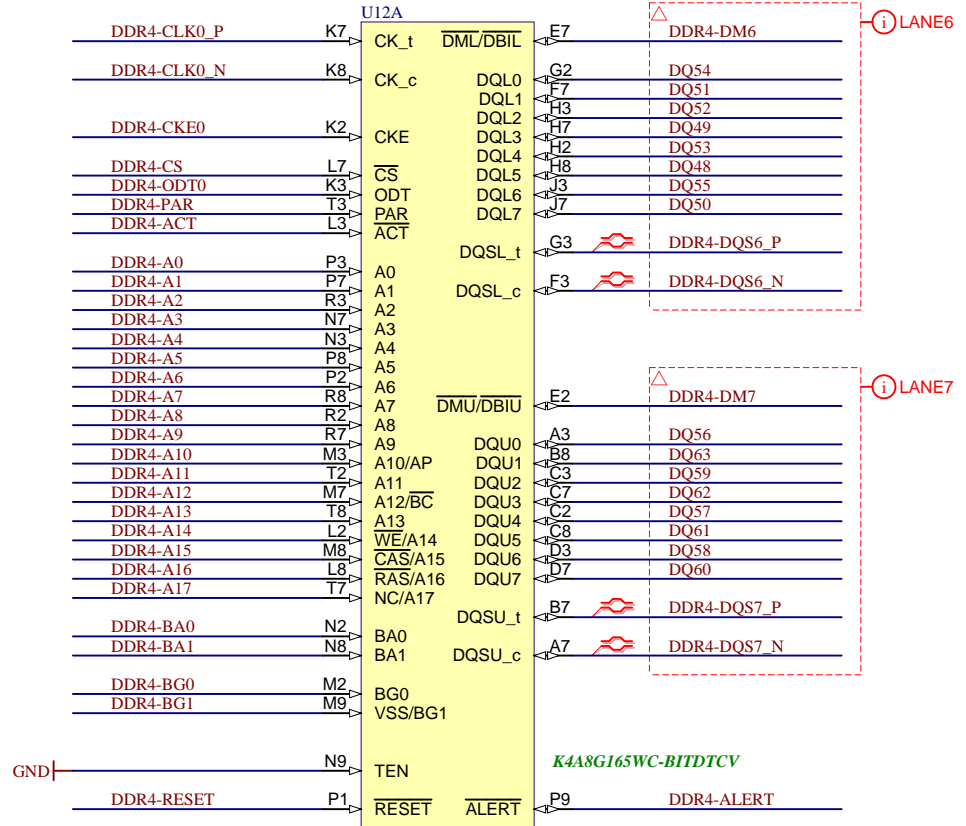
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Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 18 of 28
Filename: DDR4-RAM.SchDoc		



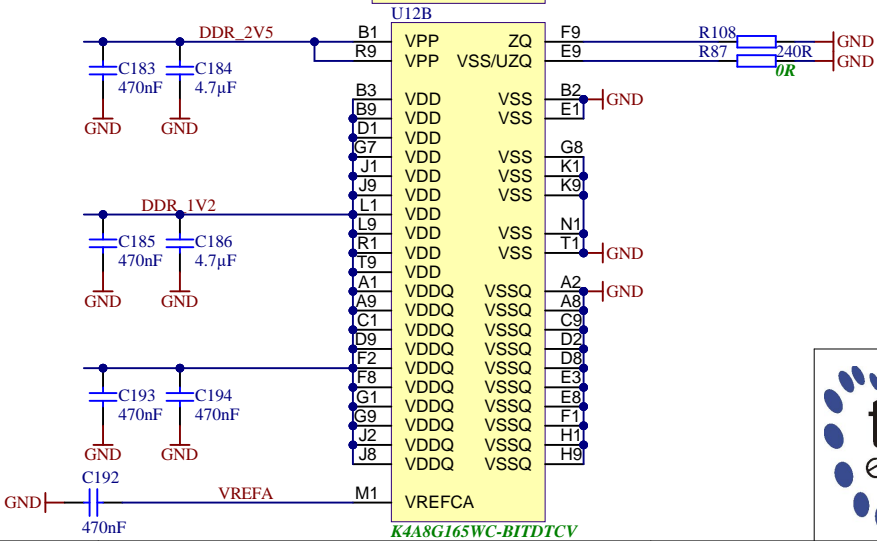
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A4	Number: TE0808 BBE81-A	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 19 of 28
Filename: DDR4-RAM_2.SchDoc		



Title: TE0808 - DDR4_3_RAM		
A4	Number: TE0808 BBE81-A	Rev. 05
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Filename: DDR4-RAM_3.SchDoc		



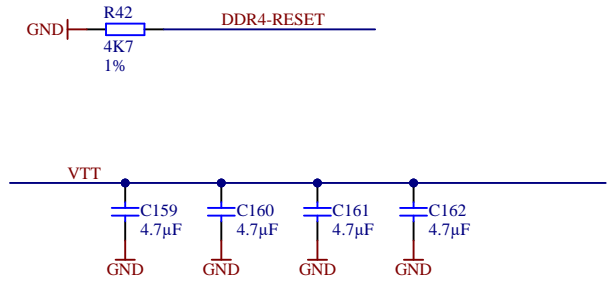
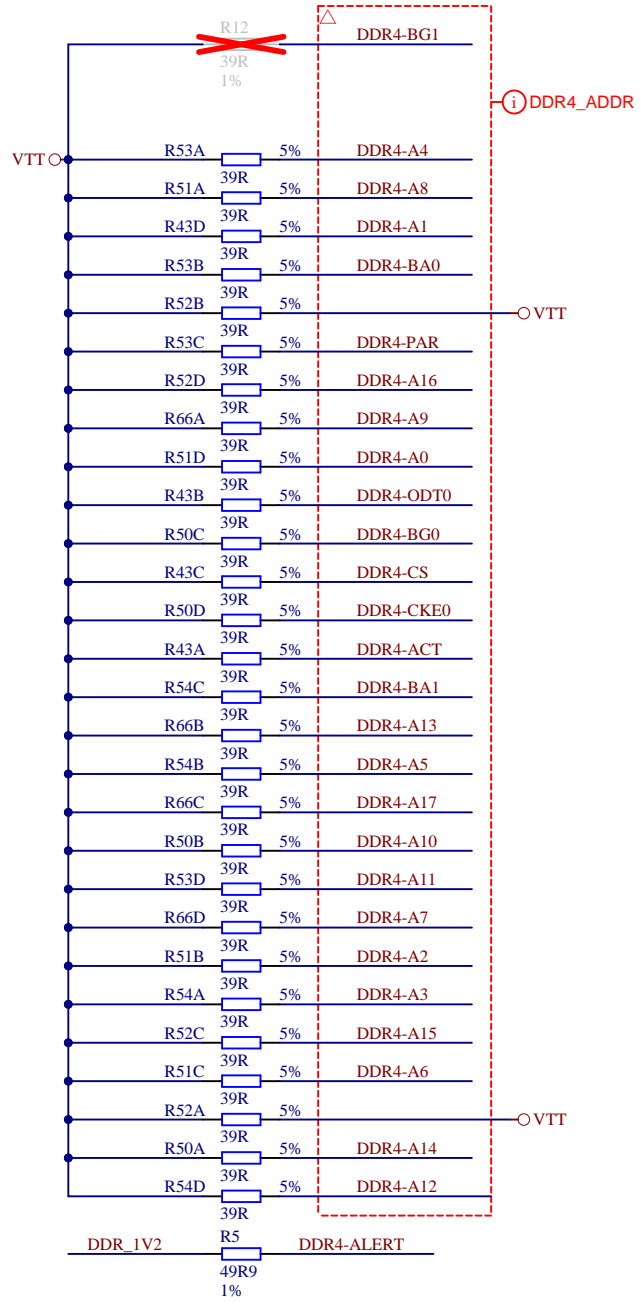
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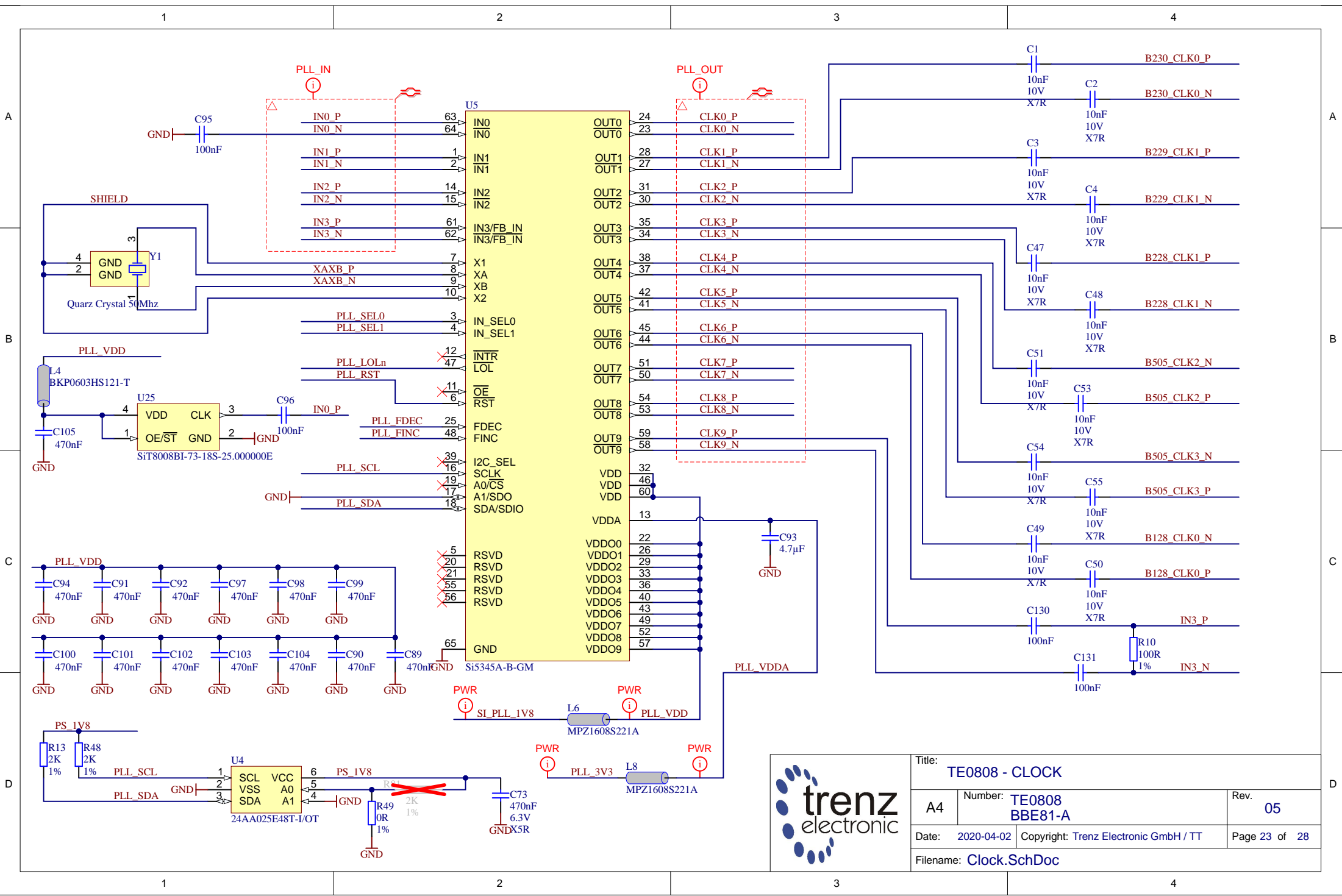
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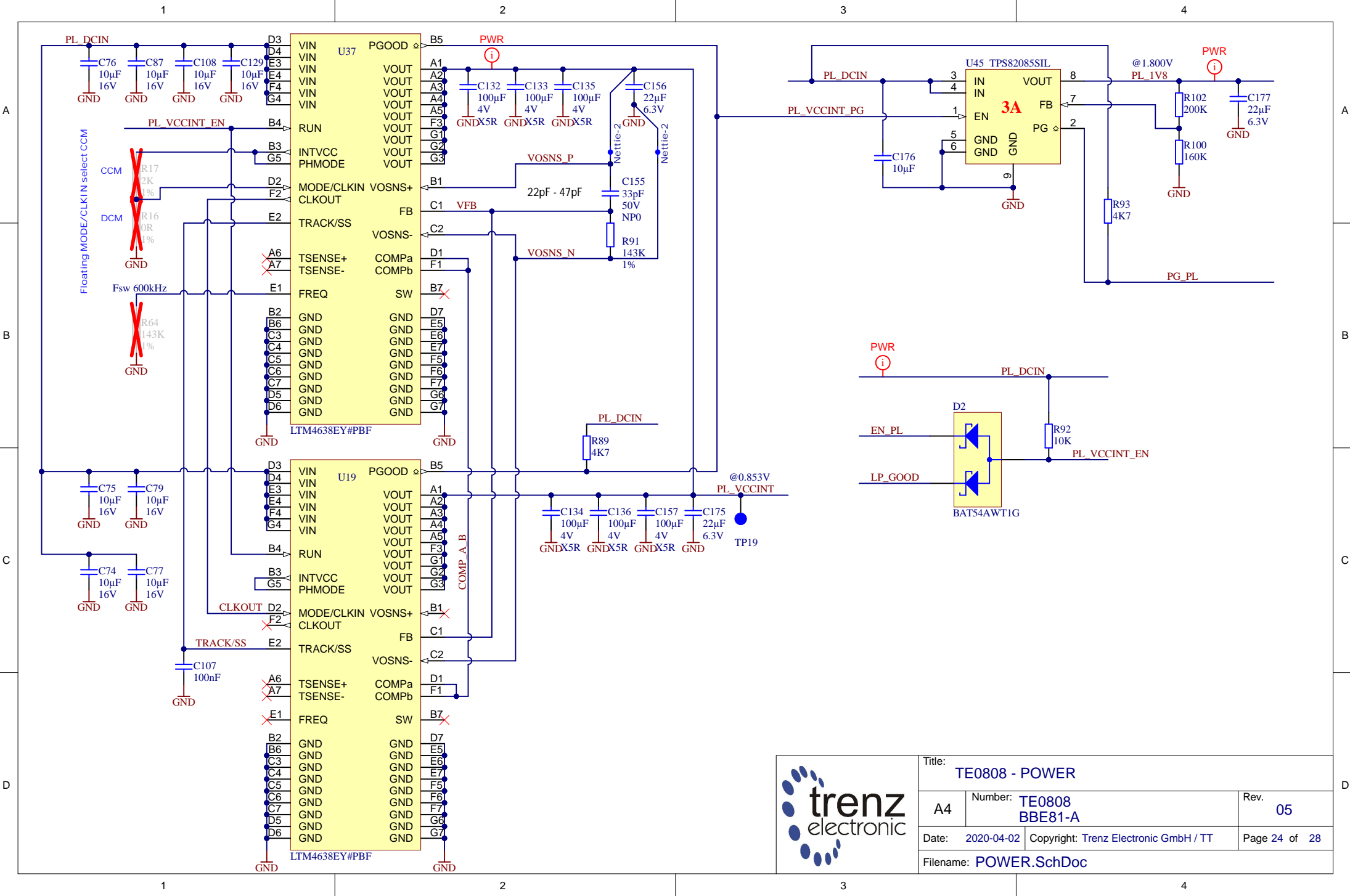
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Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 21 of 28
Filename: DDR4-RAM_4.SchDoc		



Title: TE0808 - DDR4_TERM		
A4	Number: TE0808 BBE81-A	Rev. 05
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Filename: DDR4-TERM.SchDoc		

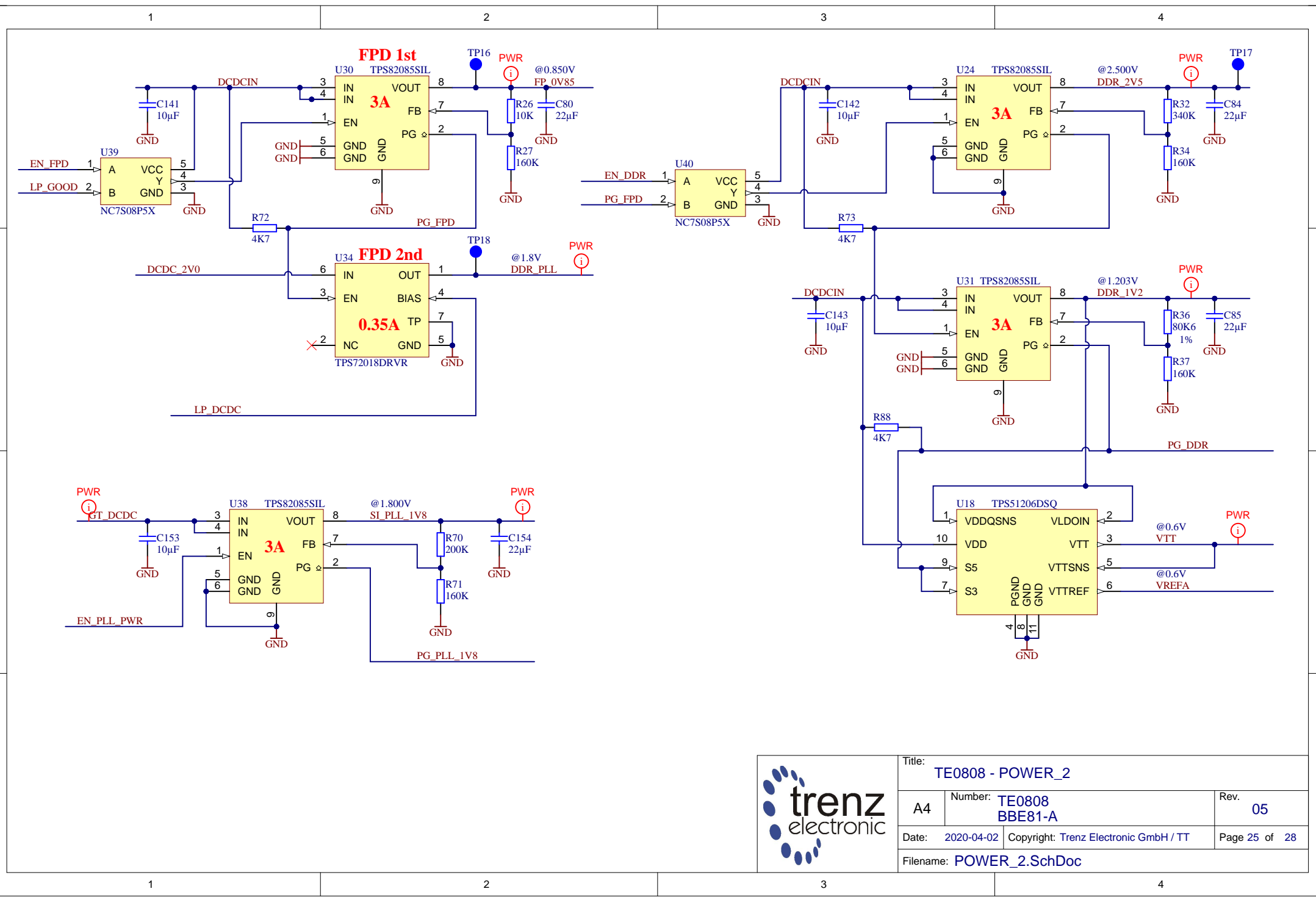



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A4	Number: TE0808 BBE81-A	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 23 of 28
Filename: Clock.SchDoc		

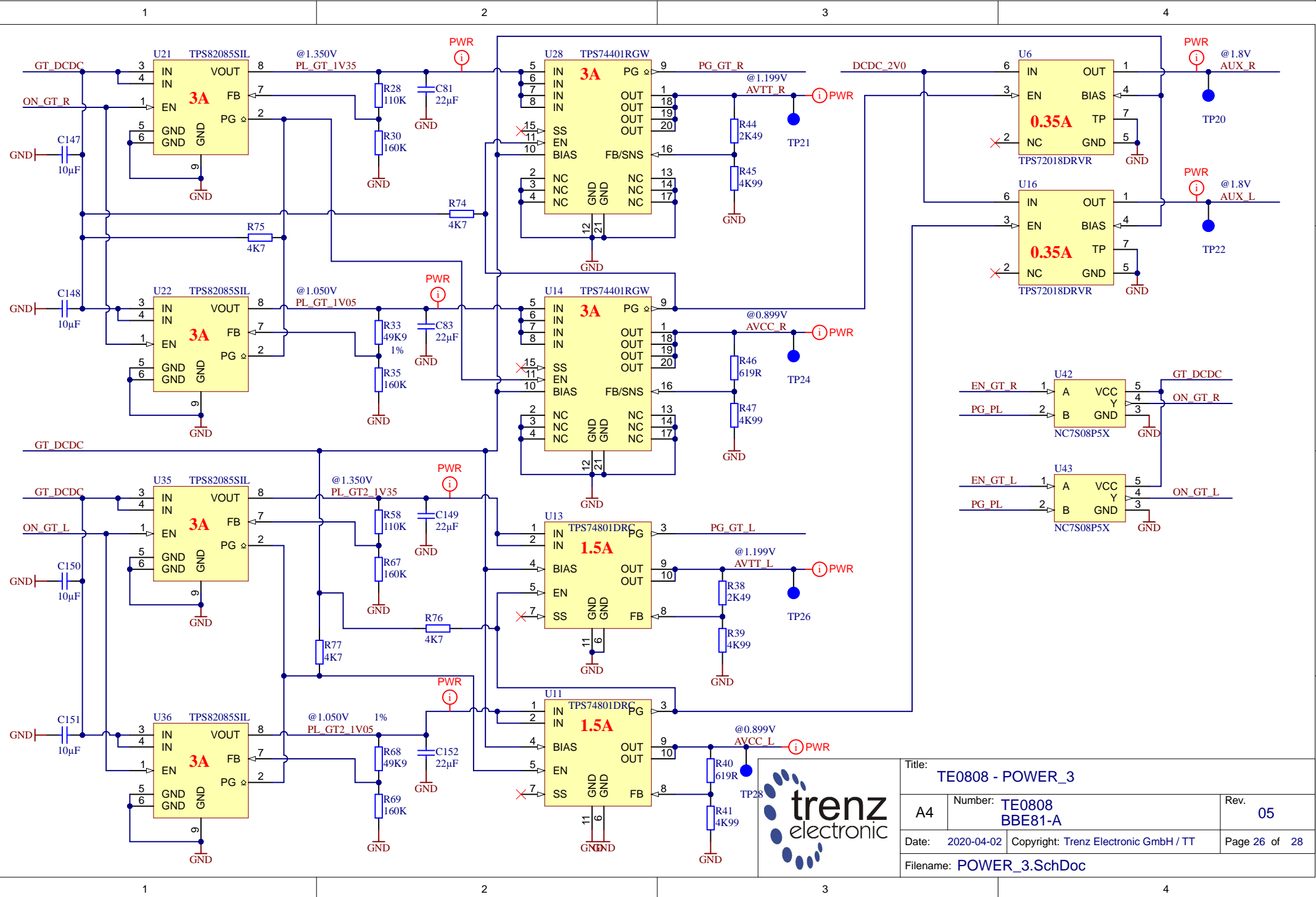


Title: TE0808 - POWER		
A4	Number: TE0808 BBE81-A	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 24 of 28
Filename: POWER.SchDoc		

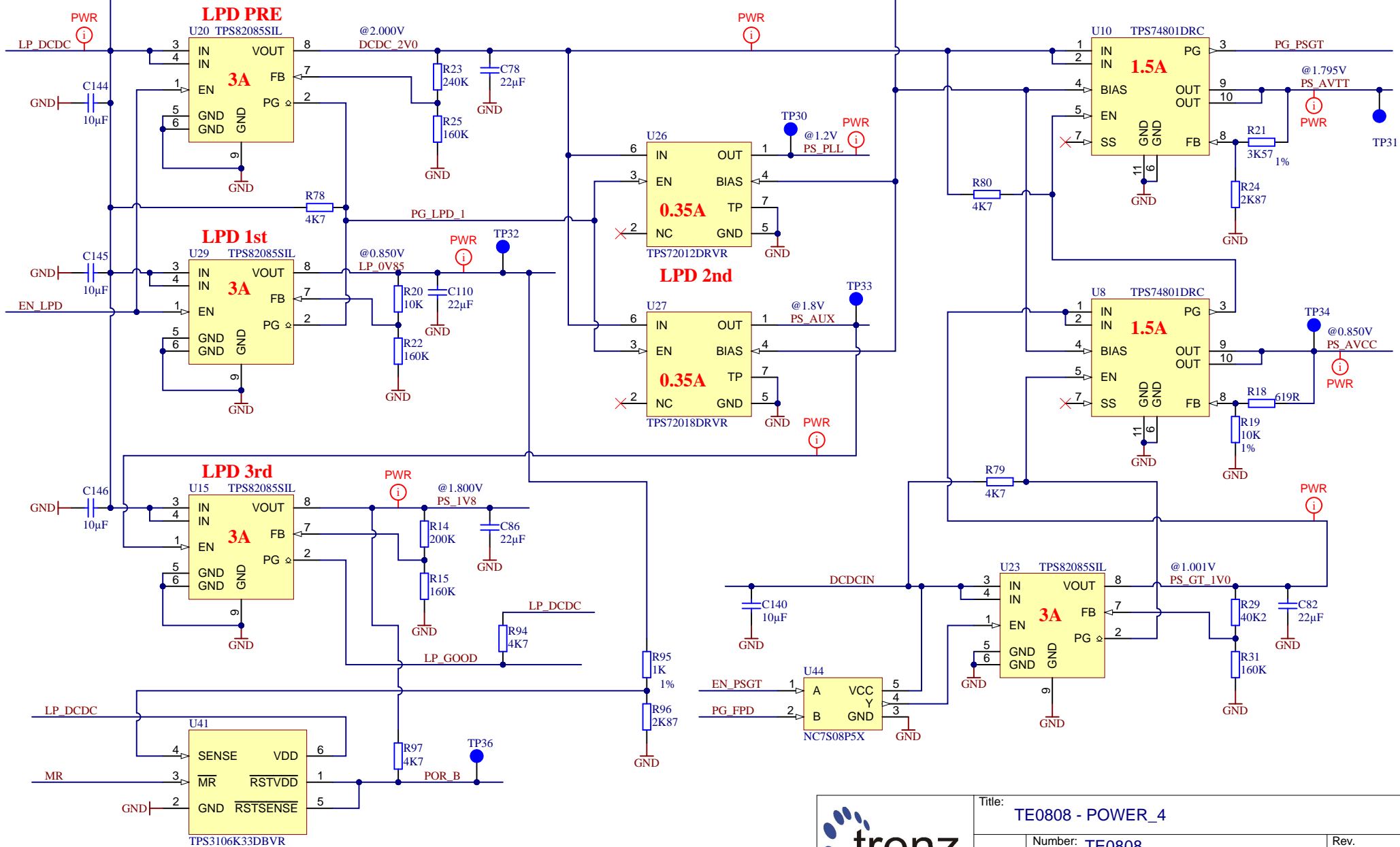




		Title: TE0808 - POWER_2	
		A4	Number: TE0808 BBE81-A
Date: 2020-04-02		Copyright: Trenz Electronic GmbH / TT	
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Title: TE0808 - POWER_3		
A4	Number: TE0808 BBE81-A	Rev. 05
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POR\_B is "0" when LP\_OV85 lower 0.74V



Title: TE0808 - POWER_4		
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Revision 04:

- 1. Added resistors R65,R82,R86,R87 (240R) for each DDR4-chip for supporting DDP DDR4 chips
- 2. Full library update

Revision 04a (09.06.2020):


- 1. VY: R19 value was changed to 10K (was: 4K99) to set PS\_MGTRAVCC 0.85V

Revision 05:

- 1. VY: revised PL\_VCCINT power supply. PCB: revised routing and components placement;
- 2. VY: added signal BG1 for DDP DDR4 IC. Added support of new packages. PCB: revised routing and components placement;
- 3. VY: R5 pulled up to 1.2V. R5 value changed to 49.9R;
- 4. VY: added test points;
- 5. VY: added MAC EEPROM U48. I2C bus PLL\_SCL/SDA. Added pull up resistor to I2C bus;
- 6. VY: PCB - revised FPGA location. Package placed 1.5mm closer to connector J3;
- 7. VY: PCB - updated silkscreen. Added company address, CE and WEEE symbols;
- 8. VY: PCB - updated signal trace lengths.

29.11.2022

- 9. Chnaged note near J2.97 and net PG\_GT\_L from "On board pull-up R" to "External pull-up R Required"

		Title: <b>TE0808 - Changes list</b>		
		A4	Number: <b>TE0808 BBE81-A</b>	Rev. <b>05</b>
		Date: <b>2020-04-02</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>28</b> of <b>28</b>
		Filename: <b>Revision_Changes.SchDoc</b>		

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