



TE0808 Test Board

Revision v.31

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Online version of this document:

<https://wiki.trenz-electronic.de/display/PD/TE0808+Test+Board>

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4 Overview

Design Example with minimum PS Setup (DDR, QSPI, UART0) only for custom boards or easier debug via SDK.

Refer to <http://trenz.org/te0808-info> for the current online version of this manual and other available documentation.

4.1 Key Features

- Vitis/Vivado 2019.2
- QSPI
- Custom Carrier (minimum PS Design with available module components only)
- Modified FSBL (some additional outputs only)
- Special FSBL for QSPI Programming

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2020-09-29	2019.2	TE0808-test_board_noprebuilt-vivado_2019.2-build_15_20200929070740.zip TE0808-test_board-vivado_2019.2-build_15_20200929070725	John Hartfiel	<ul style="list-style-type: none"> • bugfix 8GB board parts
2020-09-22	2019.2	TE0808-test_board_noprebuilt-vivado_2019.2-build_14_20200922073159.zip TE0808-test_board-vivado_2019.2-build_14_20200922073144.zip	John Hartfiel	<ul style="list-style-type: none"> • new assembly variants
2020-03-25	2019.2	TE0808-test_board_noprebuilt-vivado_2019.2-build_8_20200325083246.zip TE0808-test_board-vivado_2019.2-build_8_20200325083204.zip	John Hartfiel	<ul style="list-style-type: none"> • script update
2020-01-22	2019.2	TE0808-test_board_noprebuilt-vivado_2019.2-build_3_20200122142231.zip TE0808-test_board-vivado_2019.2-build_3_20200122142208.zip	John Hartfiel	<ul style="list-style-type: none"> • 2019.2 update • Vitis support

Date	Vivado	Project Built	Authors	Description
2019-08-09	2018.3	TE0808-test_board_noprebuilt-vivado_2018.3-build_07_20190809131546.zip TE0808-test_board-vivado_2018.3-build_07_20190809131522.zip	John Hartfiel	<ul style="list-style-type: none"> new assembly variants
2019-05-06	2018.3	TE0808-test_board_noprebuilt-vivado_2018.3-build_05_20190507124141.zip TE0808-test_board-vivado_2018.3-build_05_20190507124130.zip	John Hartfiel	<ul style="list-style-type: none"> custom FSBL
2018-07-11	2018.2	TE0808-test_board_noprebuilt-vivado_2018.2-build_02_201807111143743.zip TE0808-test_board-vivado_2018.2-build_02_201807111143702.zip	John Hartfiel	<ul style="list-style-type: none"> additional notes for FSBL generated with Win SDK changed *.bif
2018-03-29	2017.4	TE0808-test_board-vivado_2017.4-build_07_20180329151341.zip TE0808-test_board_noprebuilt-vivado_2017.4-build_07_20180329151355.zip	John Hartfiel	<ul style="list-style-type: none"> new assembly variant
2018-01-16	2017.4	TE0808-test_board-vivado_2017.4-build_04_20180116144644.zip TE0808-test_board_noprebuilt-vivado_2017.4-build_04_20180116144657.zip	John Hartfiel	<ul style="list-style-type: none"> Update Board Part for TEBF0808 <ul style="list-style-type: none"> no changes for test board design and minimal board parts
2018-01-15	2017.4	TE0808-test_board-vivado_2017.4-build_03_20180115084954.zip TE0808-test_board_noprebuilt-vivado_2017.4-build_03_20180115085020.zip	John Hartfiel	<ul style="list-style-type: none"> rework Board Part Files
2017-12-20	2017.2	TE0808-test_board-vivado_2017.2-build_07_20171220192501.zip TE0808-test_board_noprebuilt-vivado_2017.2-build_07_20171220192448.zip	John Hartfiel	<ul style="list-style-type: none"> Update Board Part Files

Date	Vivado	Project Built	Authors	Description
2017-11-22	2017.2	TE0808-test_board-vivado_2017.2-build_05_20171122080211.zip TE0808-test_board_noprebuilt-vivado_2017.2-build_05_20171122080228.zip	John Hartfiel	<ul style="list-style-type: none"> Update Board Part CSV File Regenerate design
2017-11-16	2017.2	TE0808-test_board-vivado_2017.2-build_05_20171116151545.zip TE0808-test_board_noprebuilt-vivado_2017.2-build_05_20171116151600.zip	John Hartfiel	<ul style="list-style-type: none"> Update Board Part CSV File with new Flash assembly variants
2017-11-13	2017.2	TE0808-test_board-vivado_2017.2-build_05_20171113140954.zip TE0808-test_board_noprebuilt-vivado_2017.2-build_05_20171113141908.zip	John Hartfiel	<ul style="list-style-type: none"> initial release

Table 1: Design Revision History

4.3 Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2019.2	needed, Vivado is included into Vitis installation

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).¹

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EM MC	Others	Notes
TE0808-ES1	es1_2gb	REV03 REV02	2G B	64MB	NA	NA	Not longer supported by vivado
TE0808-ES2	es2_2gb	REV04 REV03	2G B	64MB	NA	NA	Not longer supported by vivado
TE0808-2ES2	2es2_2gb	REV04 REV03	2G B	64MB	NA	NA	Not longer supported by vivado
TE0808-04-09EG-1EA	9eg_1e_2gb	REV04	2G B	64MB	NA	NA	
TE0808-04-09EG-1EB	9eg_1e_4gb	REV04	4G B	64MB	NA	NA	
TE0808-04-09EG-1ED	9eg_1e_4gb	REV04	4G B	64MB	NA	1 mm connectors	
TE0808-04-09EG-2IB	9eg_2i_4gb	REV04	4G B	64MB	NA	NA	
TE0808-04-15EG-1EB	15eg_1e_4gb	REV04	4G B	64MB	NA	NA	

¹ <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EM MC	Others	Notes
TE0808-04-09EG-1EE	9eg_1e_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-09EG-1EL	9eg_1e_4gb	REV04	4GB	128MB	NA	1 mm connectors	
TE0808-04-09EG-2IE	9eg_2i_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-15EG-1EE	15eg_1e_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-06EG-1EE	6eg_1e_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-06EG-1E3	6eg_1e_4gb	REV04	4GB	128MB	NA	1 mm connectors	
TE0808-04-6GI21-L	6eg_2i_4gb	REV04	4GB	128MB	NA	1 mm connectors	
TE0808-04-6GI21-A	6eg_2i_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-6BI21-A	6eg_1i_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-9GI21-A	9eg_2i_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-9BE21-A	9eg_1e_4gb	REV04	4GB	128MB	NA	NA	

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EM MC	Others	Notes
TE0808-04-6BE21-L	6eg_1e_4gb	REV04	4GB	128MB	NA	1 mm connectors	
TE0808-04-6BE21-A	6eg_1e_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-9BE21-L	9eg_1e_4gb	REV04	4GB	128MB	NA	1 mm connectors	
TE0808-04-BBE21-A	15eg_1e_4gb	REV04	4GB	128MB	NA	NA	
TE0808-04-6BI21-X	6eg_1i_4gb	REV04	4GB	128MB	NA	NA	U41 replaced with schottky diodes
TE0808-05-6BE21-L	6eg_1e_4gb	REV05	4GB	128MB	NA	1 mm connectors	NA
TE0808-05-6BE21-A	6eg_1e_4gb	REV05	4GB	128MB	NA	NA	NA
TE0808-05-6BI21-D	6eg_1i_4gb	REV05	4GB	128MB	NA	1 mm connectors	SoC without encryption
TE0808-05-6BI21-X	6eg_1i_4gb	REV05	4GB	128MB	NA	NA	U41 replaced with schottky diodes
TE0808-05-6BI41-X	6eg_1i_8gb	REV05	8GB	128MB	NA	NA	U41 replaced with schottky diodes
TE0808-05-9BE21-A	9eg_1e_4gb	REV05	4GB	128MB	NA	NA	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EM MC	Others	Notes
TE0808-05-9BE21-L	9eg_1e_4gb	REV05	4GB	128MB	NA	1 mm connectors	NA
TE0808-05-9BI41-X	9eg_1i_8gb	REV05	8GB	128MB	NA	NA	U41 replaced with schottky diodes
TE0808-05-9GI21-A	9eg_2i_4gb	REV05	4GB	128MB	NA	NA	NA
TE0808-05-9GI21-C	9eg_2i_4gb	REV05	4GB	128MB	NA	NA	SoC without encryption
TE0808-05-BBE21-A	15eg_1e_4gb	REV05	4GB	128MB	NA	NA	NA
TE0808-05-BBE21-L	15eg_1e_4gb	REV05	4GB	128MB	NA	1 mm connectors	NA

Table 4: Hardware Modules

Note: Design contains also Board Part Files for TE0803+TEBF0808 configuration, this board part files are not used for this reference design.

Design supports following carriers:

Carrier Model	Notes
Custom PCB	use simple Board Part files, if MIO connected is different to TEBF0808
TEBF0808	Used as reference carrier.
TEBT0808-01	Change UART0 to UART1 (MIO68...69) and regenerate design

Table 5: Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
---	---

Table 6: Additional Hardware

4.5 Content

For general structure and of the reference design, see [Project Delivery - Xilinx devices](#)²

4.5.1 Design Sources

Type	Location	Notes
Vivado	<design name>/ block_design <design name>/ constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
Vitis	<design name>/sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

Table 7: Design sources

4.5.2 Additional Sources

Type	Location	Notes
---	---	---

Table 8: Additional design sources

4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)

² <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices>

File	File-Extension	Description
BIT-File	*.bit	FPGA (PL Part) Configuration File
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebuilt content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0808 "Test Board" Reference Design³](https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0808/Reference_Design/2019.2/test_board)

³ https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0808/Reference_Design/2019.2/test_board

5 Design Flow

⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- [Xilinx Development Tools](#)⁴
- [Vivado Projects - TE Reference Design](#)⁵
- [Project Delivery](#).⁶

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also be executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)⁷

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

```

C:\WINDOWS\system32\cmd.exe
B:\Design\cores\2017.2\design\TE0808\test_board>setlocal
--Set design paths-----
-- Run Design with: _create_win_setup
-- Use Design Path: B:\Design\cores\2017.2\design\TE0808\test_board\
-----TE Reference Design-----
-- (c) Go to CMD-File Generation (Manual setup)
-- (d) Go to Documentation (Web Documentation)
-- (x) Exit Batch (nothing is done!)
-- (0) Create minimum setup of CMD-Files and exit Batch
-- (1) Create maximum setup of CMD-Files and exit Batch
Select (ex.: '0' for min setup):
  
```

2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x: \<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process
 - a. (optional for manual changes) select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guiemode.cmd"

Note: Select correct one, see [TE Board Part Files](#)

⁸ **Important:** Use Board Part Files, which **did not** ends with *_tebf0808
5. Create XSA and export to prebuilt folder

⁴ <https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftware-BasicUserGuides>

⁵ <https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design>

⁶ <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices>

⁷ <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality>


⁸ <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

- a. Run on Vivado TCL: `TE::hw_build_design -export_prebuilt`
Note: Script generate design and export files into `\prebuilt\hardware\<short dir>`. Use GUI is the same, except file export to prebuilt folder
6. Generate Programming Files with Vitis
 - a. Run on Vivado TCL: `TE::sw_run_vitis -all`
Note: Scripts generate applications and bootable files, which are defined in `"sw_lib\apps_list.csv"`
 - b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: `TE::sw_run_vitis`
Note: TCL scripts generate also platform project, this must be done manually in case GUI is used. See [Vitis⁹](#)

⁹ <https://wiki.trenz-electronic.de/display/PD/Vitis>

6 Launch

6.1 Programming

 Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging](#)¹⁰

6.1.1 Get prebuilt boot binaries

1. `_create_win_setup.cmd/_create_linux_setup.sh` and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
 - a. Select assembly version
 - b. Validate selection
 - c. Select Create and open delivery binary folder
Note: Folder (`<project folder>/_binaries_<Artikel Name>`) with subfolder (`boot_<app name>`) for different applications will be generated

6.1.2 QSPI

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "`vivado_open_existing_project_gui mode.cmd`" or if not created, create with "`vivado_create_project_gui mode.cmd`"
3. Type on Vivado TCL Console: `TE::pr_program_flash_binfile -swapp hello_te0808`
Note: To program with SDK/Vivado GUI, use special FSBL (`zynqmp_fsb_flash`) on setup

6.1.3 SD

This does not work, because SD controller is not selected on PS.

6.1.4 JTAG

Load configuration and Application with Vitis Debugger into device,

6.2 Usage

QSPI Boot:

1. Prepare HW like described on section [Programming](#)(see page 17)
2. Connect UART USB (most cases same as JTAG)
3. Select QSPI Card as Boot Mode
Note: See TRM of the Carrier, which is used.

¹⁰<https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftwareProgrammingandDebugging>

4. Power On PCB

Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from QSPI into OCM, 2. FSBL loads Application into DDR

7 System Design - Vivado

7.1 Block Design

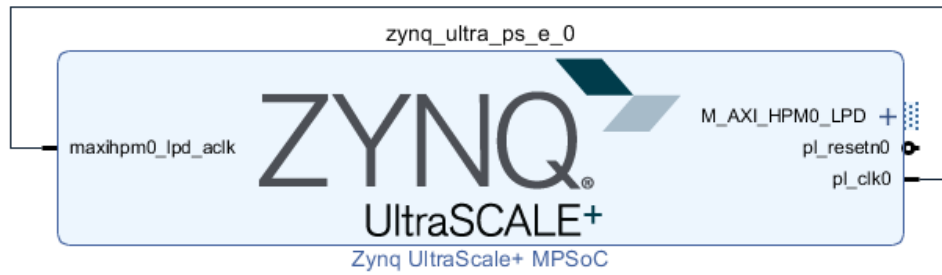


Figure 1: Block Design

7.1.1 PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
UART0	MIO, please select other one, if you have connected uart to second controller or other MIO
SWDT0..1	
TTC0..3	

Table 10: PS Interfaces

7.2 Constrains

7.2.1 Basic module constrains

_i_bitgen.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

7.2.2 Design specific constrain

Not needed.

8 Software Design - Vitis

For SDK project creation, follow instructions from:

[Vitis](#)¹¹

8.1 Application

Template location: `./sw_lib/sw_apps/`

8.1.1 zynqmp_fsbl

TE modified 2019.2 FSBL

General:

- Modified Files: `xfsbl_main.c`, `xfsbl_hooks.h/.c`, `xfsbl_board.h/.c` (search for 'TE Mod' on source code)
- Add Files: `te_xfsbl_hooks.h/.c` (for hooks and board)\n\
- General Changes:
 - Display FSBL Banner and Device Name

8.1.2 zynqmp_fsbl_flash

TE modified 2019.2 FSBL

General:

- Modified Files: `xfsbl_initialisation.c`, `xfsbl_hw.h`, `xfsbl_handoff.c`, `xfsbl_main.c`
- General Changes:
 - Display FSBL Banner
 - Set FSBL Boot Mode to JTAG
 - Disable Memory initialisation

8.1.3 hello_te0808

Hello TE0808 is a Xilinx Hello World example as endless loop instead of one console output.

¹¹ <https://wiki.trenz-electronic.de/display/PD/Vitis>


9 Additional Software

No additional software is needed.

10 Appx. A: Change History and Legal Notices

10.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
 2020-09-29	v.31(see page 6)	John Hartfiel ¹²	<ul style="list-style-type: none"> new assembly variants
2020-03-25	v.28	John Hartfiel	<ul style="list-style-type: none"> script update
2020-01-27	v.27	John Hartfiel	<ul style="list-style-type: none"> documentation update
2020-01-22	v.26	John Hartfiel	<ul style="list-style-type: none"> new assembly variants Release 2019.2
2019-08-09	v.24	John Hartfiel	<ul style="list-style-type: none"> new assembly variants small document style update
2019-05-07	v.22	John Hartfiel	<ul style="list-style-type: none"> Release 2018.3
2018-07-11	v.21	John Hartfiel	<ul style="list-style-type: none"> Release 2018.2
2018-03-29	v.20	John Hartfiel	<ul style="list-style-type: none"> new assembly variant
2018-02-08	v.19	John Hartfiel	<ul style="list-style-type: none"> Release 2017.4
2017-12-20	v.14	John Hartfiel	<ul style="list-style-type: none"> Design Update typo correction on documentation
2017-11-22	v.10	John Hartfiel	<ul style="list-style-type: none"> Update assembly versions with new Flash size Update HW Table Name Update Design

¹² <https://wiki.trenz-electronic.de/display/~j.hartfiel>

Date	Document Revision	Authors	Description
2017-11-14	v.6	John Hartfiel	<ul style="list-style-type: none"> Release 2017.2
--	all	John Hartfiel ¹³	--

Table 11: Document change history.

10.2 Legal Notices

10.3 Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

10.4 Document Warranty

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¹³ <https://wiki.trenz-electronic.de/display/~j.hartfiel>

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WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

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¹⁴ <http://guidance.echa.europa.eu/>

¹⁵ <https://echa.europa.eu/candidate-list-table>

¹⁶ <http://www.echa.europa.eu/>