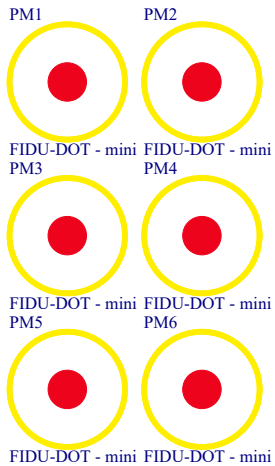
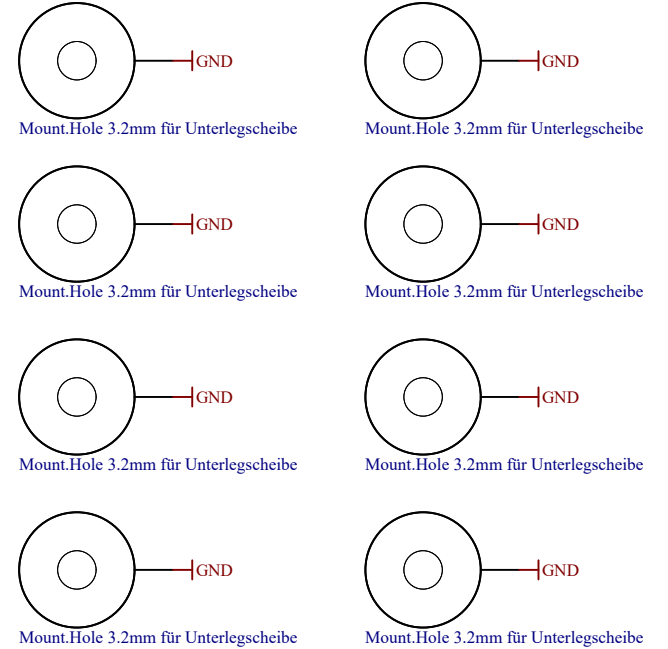


U_J1 J1.SchDoc	U_B_PS_GT B_PS_GT.SchDoc	U_LN Legal Notices Modules.SchDoc
U_J2 J2.SchDoc	U_PS_DDR PS_DDR.SchDoc	U_ZU_POWER ZU_POWER.SchDoc
U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_1 POWER_1.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_3.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	U_REV_CH Revision Changes.SchDoc
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	U_OVERVIEW TE0813-Overview.SchDoc
U_PD Power Diagram.SchDoc	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	

Special notes:



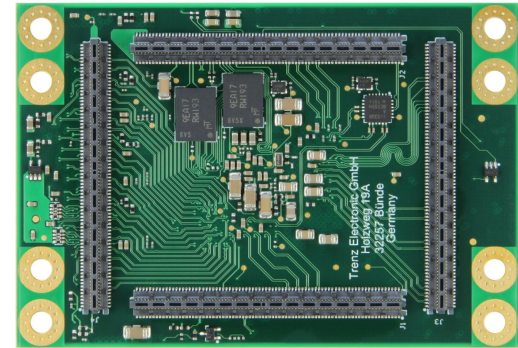
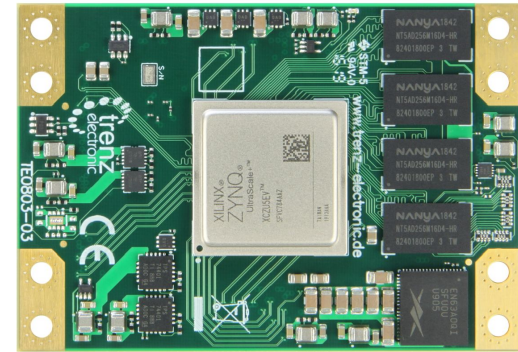
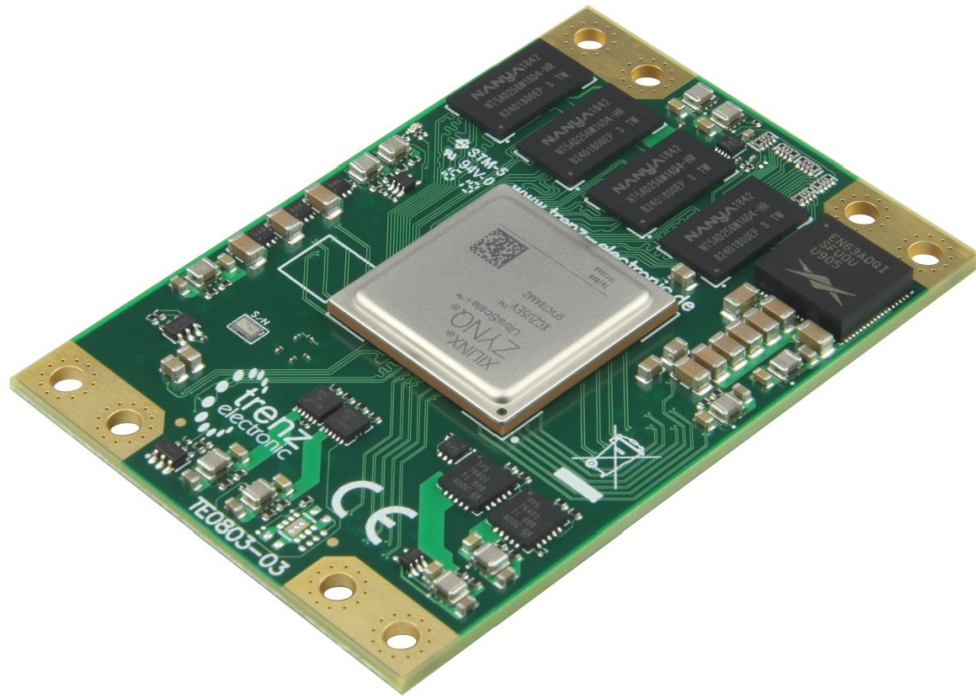
MECH1  
TE Address Overlay  
LOGO ADDRESS

LOGO1  
TE Logo PRINT Layer  
LOGO PRINT

Serial  
Serial  
Serialnumber 6,3 x 6.3mm

Assembly variant	2FE71-A
Created by	VT
Modified by	VT
Modified at	2021-05-18
SVN Revision	11945


	Title: TE0813	
	A4	Number: TE0813 2FE71-A
	Date: 07.07.2021	Copyright: Trenz Electronic GmbH / TT
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Filename: TE0813.SchDoc		



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Schematics and other handouts serve for informational purposes only!

	Title: <b>TE0813</b>		Rev. <b>01</b>
	A4	Number: <b>TE0813 2FE71-A</b>	
	Date: <b>2021-01-19</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>2</b> of <b>30</b>
	Filename: <b>Legal Notices Modules.SchDoc</b>		

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	Title: <b>Module TE0813 - System Overview</b>		
	A4	Number: <b>TE0813 2FE71-A</b>	Rev. <b>01</b>
	Date: <b>2021-01-19</b>	Copyright: <b>2015 Trenz Electronic GmbH</b>	Page <b>3</b> of <b>30</b>
	Filename: <b>TE0813-Overview.SchDoc</b>		

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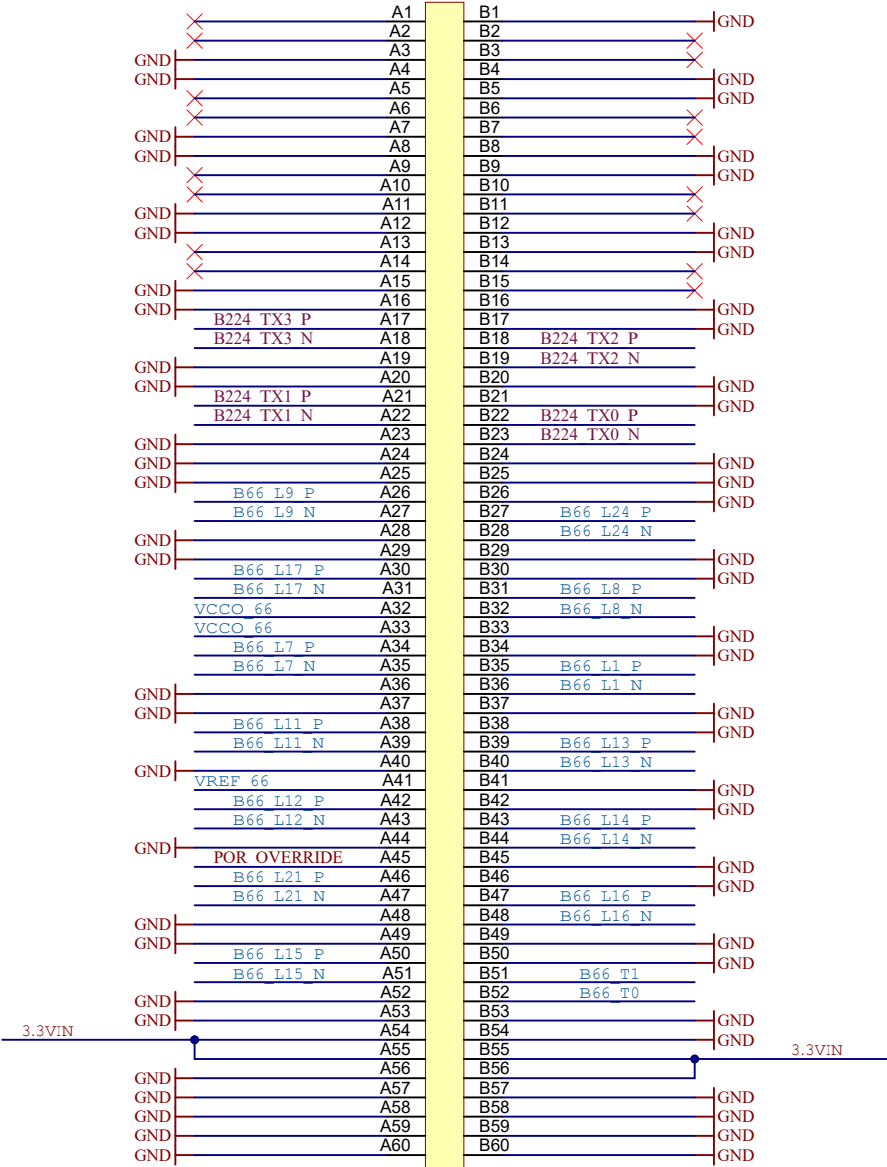
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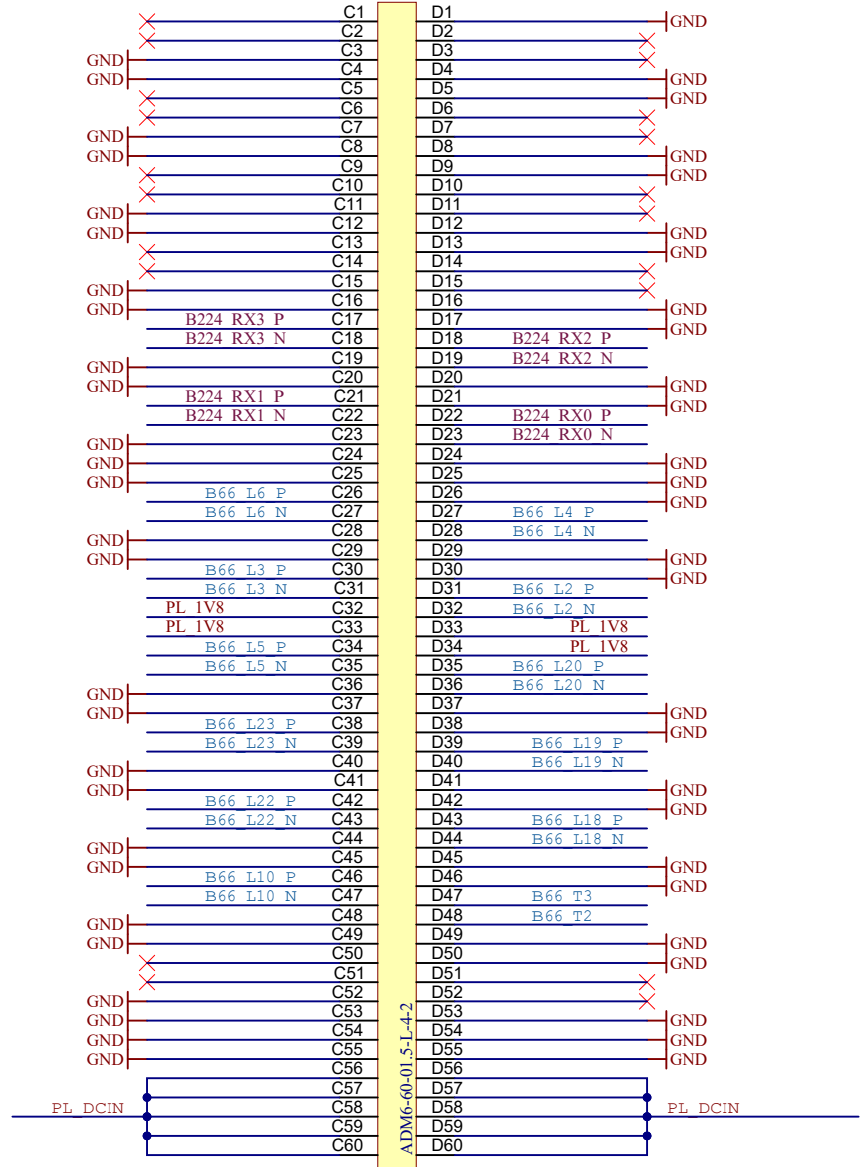
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JM1A

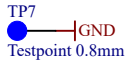
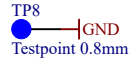
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ADM6-60-01.5-L-4-2



ADM6-60-01.5-L-4-2



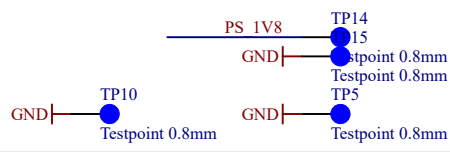
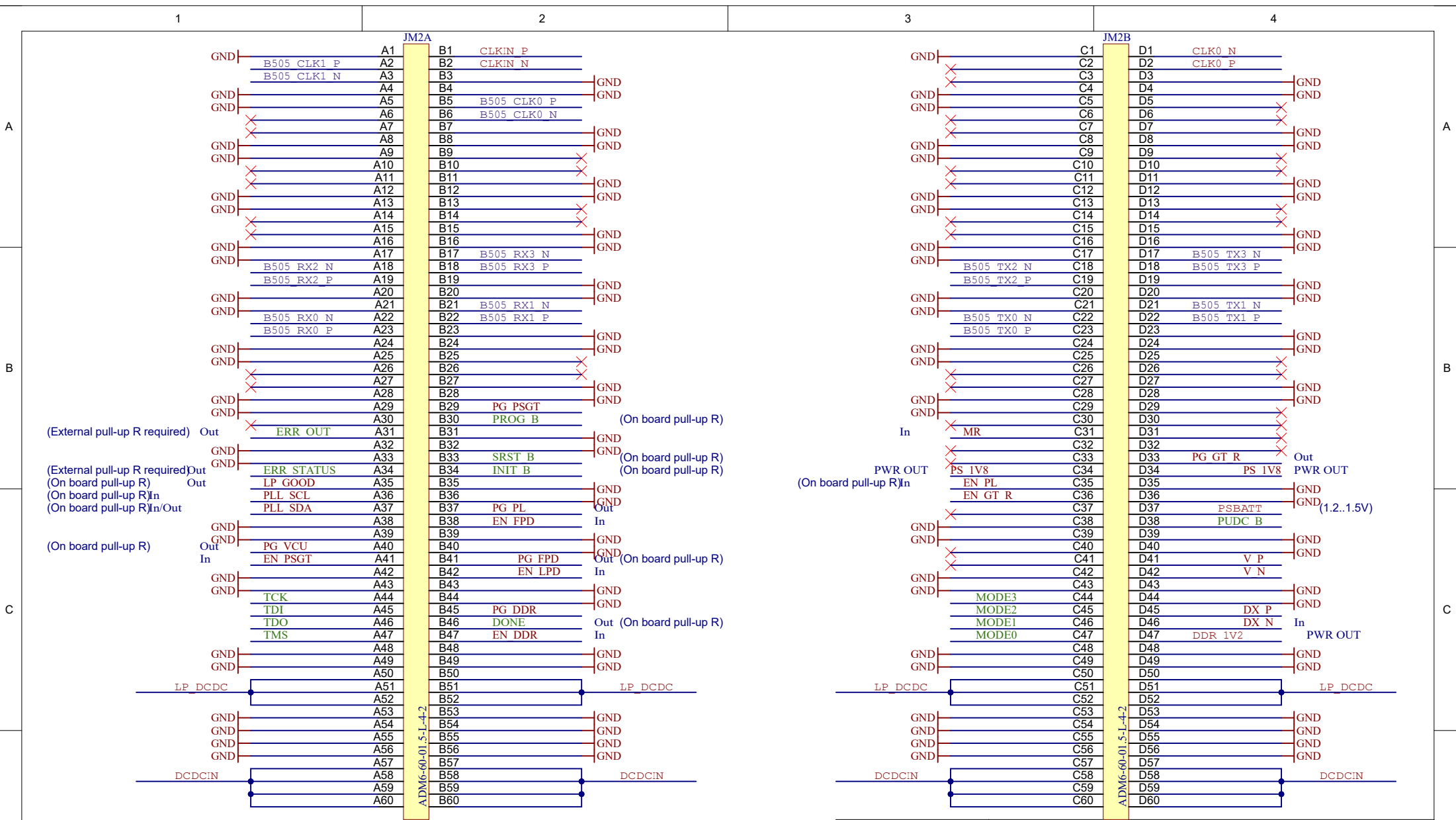
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Date: 07.07.2021	Copyright: Trenz Electronic GmbH / TT	Page4 of 30
Filename: J1.SchDoc		

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Title: TE0813 - Connector J2		
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JM3A  
ADM6-60-01.5-L-4-2

JM3B  
ADM6-60-01.5-L-4-2

\*Bank 25 for XCZU2/3  
\*Bank 45 for XCZU4/6  
\*\*Bank 26 for XCZU2/3  
\*\*Bank 46 for XCZU4/5

CLK IN

PWR IN  
PWR IN

PWR IN  
PWR IN

CLK IN

PWR IN  
PWR IN

PWR IN  
PWR IN

PS 1V8

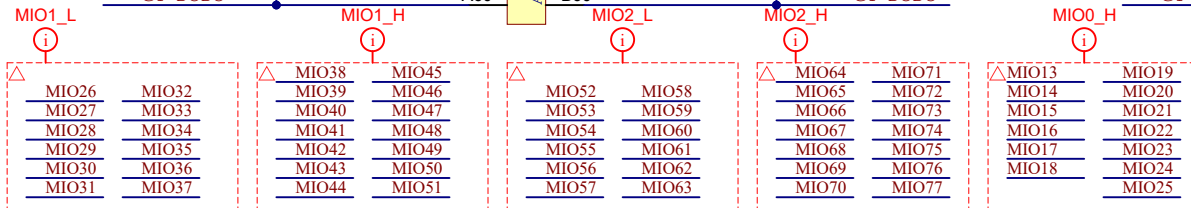
PS 1V8

PS 1V8

PS 1V8

GT DCDC

GT DCDC



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Filename: J3.SchDoc		

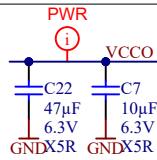
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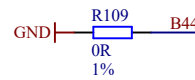


UIC XCZU2CG-1SFVC784E  
BANK 26 HD (ZU4/5 BANK 46 HD)

F14	VCCO_26	B15	IO_L1P_AD11P_26	IO_L7P_HDGC_AD5P_26	G13	B26_L7_P
C15	VCCO_26	A15	IO_L1N_AD11N_26	IO_L7N_HDGC_AD5N_26	F13	B26_L7_N
		B14	IO_L2P_AD10P_26	IO_L8P_HDGC_AD4P_26	F15	B26_L8_P
		A14	IO_L2N_AD10N_26	IO_L8N_HDGC_AD4N_26	E15	B26_L8_N
		B13	IO_L3P_AD9P_26	IO_L9P_AD3P_26	G15	B26_L9_P
		A13	IO_L3N_AD9N_26	IO_L9N_AD3N_26	G14	B26_L9_N
		C14	IO_L4P_AD8P_26	IO_L10P_AD2P_26	H14	B26_L10_P
		C13	IO_L4N_AD8N_26	IO_L10N_AD2N_26	H13	B26_L10_N
		D15	IO_L5P_HDGC_AD7P_26	IO_L11P_AD1P_26	K14	B26_L11_P
		D14	IO_L5N_HDGC_AD7N_26	IO_L11N_AD1N_26	J14	B26_L11_N
		E14	IO_L6P_HDGC_AD6P_26	IO_L12P_AD0P_26	L14	B26_L12_P
		E13	IO_L6N_HDGC_AD6N_26	IO_L12N_AD0N_26	L13	B26_L12_N

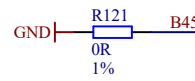

B26

B26



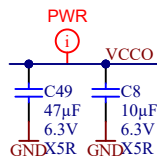
BANK 44 HD (ZU4/5 BANK 43 HD)

AC10	VCCO_44	AD11	IO_L1P_AD11P_44	IO_L7P_HDGC_AD5P_44	AD11	B44_HD
AG12	VCCO_44	AD10	IO_L1N_AD11N_44	IO_L7N_HDGC_AD5N_44	AD10	
		AH10	IO_L2P_AD10P_44	IO_L8P_HDGC_AD4P_44	AB11	
		AF11	IO_L2N_AD10N_44	IO_L8N_HDGC_AD4N_44	AC11	
		AG11	IO_L3P_AD9P_44	IO_L9P_AD3P_44	AA11	
		AH12	IO_L3N_AD9N_44	IO_L9N_AD3N_44	AA10	
		AH11	IO_L4P_AD8P_44	IO_L10P_AD2P_44	W10	
		AE10	IO_L4N_AD8N_44	IO_L10N_AD2N_44	Y10	
		AF10	IO_L5P_HDGC_AD7P_44	IO_L11P_AD1P_44	Y9	
		AE12	IO_L5N_HDGC_AD7N_44	IO_L11N_AD1N_44	AA8	
		AF12	IO_L6P_HDGC_AD6P_44	IO_L12P_AD0P_44	AB10	
		AC12	IO_L6N_HDGC_AD6N_44	IO_L12N_AD0N_44	AB9	
		AD12				

UIB XCZU2CG-1SFVC784E  
BANK 24 HD (ZU4/5 BANK 44 HD)

AA14	VCCO_24	AA13	IO_L1P_AD15P_24	IO_L7P_HDGC_24	AA13	B45_HD
AD13	VCCO_24	AB13	IO_L1N_AD15N_24	IO_L7N_HDGC_24	AB13	
		AB15	IO_L2P_AD14P_24	IO_L8P_HDGC_24	AB15	
		AB14	IO_L2N_AD14N_24	IO_L8N_HDGC_24	AB14	
		W14	IO_L3P_AD13P_24	IO_L9P_AD11P_24	W14	
		W13	IO_L3N_AD13N_24	IO_L9N_AD11N_24	W13	
		Y14	IO_L4P_AD12P_24	IO_L10P_AD10P_24	Y14	
		Y13	IO_L4N_AD12N_24	IO_L10N_AD10N_24	Y13	
		W12	IO_L5P_HDGC_24	IO_L11P_AD9P_24	W12	
		W11	IO_L5N_HDGC_24	IO_L11N_AD9N_24	W11	
		Y12	IO_L6P_HDGC_24	IO_L12P_AD8P_24	Y12	
		AA12	IO_L6N_HDGC_24	IO_L12N_AD8N_24	AA12	

XCZU2CG-1SFVC784E  
BANK 25 HD (ZU4/5 BANK 45 HD)

B12	VCCO_25	J11	IO_L1P_AD15P_25	IO_L7P_HDGC_25	E10	B25_L7_P
E11	VCCO_25	J10	IO_L1N_AD15N_25	IO_L7N_HDGC_25	D10	B25_L7_N
		K13	IO_L2P_AD14P_25	IO_L8P_HDGC_25	E12	B25_L8_P
		K12	IO_L2N_AD14N_25	IO_L8N_HDGC_25	D11	B25_L8_N
		H11	IO_L3P_AD13P_25	IO_L9P_AD11P_25	C11	B25_L9_P
		G10	IO_L3N_AD13N_25	IO_L9N_AD11N_25	B10	B25_L9_N
		J12	IO_L4P_AD12P_25	IO_L10P_AD10P_25	B11	B25_L10_P
		H12	IO_L4N_AD12N_25	IO_L10N_AD10N_25	A10	B25_L10_N
		G11	IO_L5P_HDGC_25	IO_L11P_AD9P_25	A12	B25_L11_P
		F10	IO_L5N_HDGC_25	IO_L11N_AD9N_25	A11	B25_L11_N
		F12	IO_L6P_HDGC_25	IO_L12P_AD8P_25	D12	B25_L12_P
		F11	IO_L6N_HDGC_25	IO_L12N_AD8N_25	C12	B25_L12_N

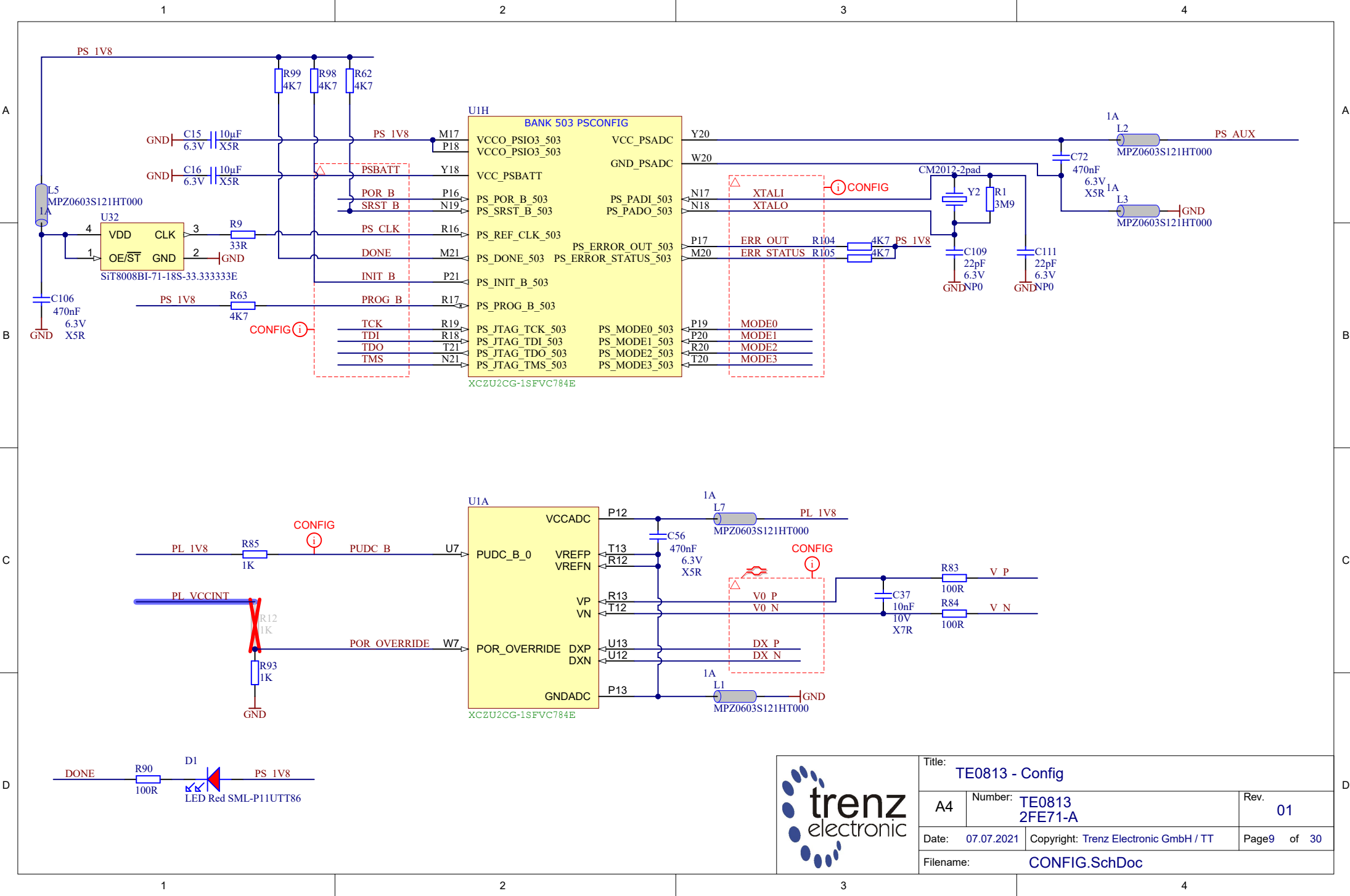

B25

B25



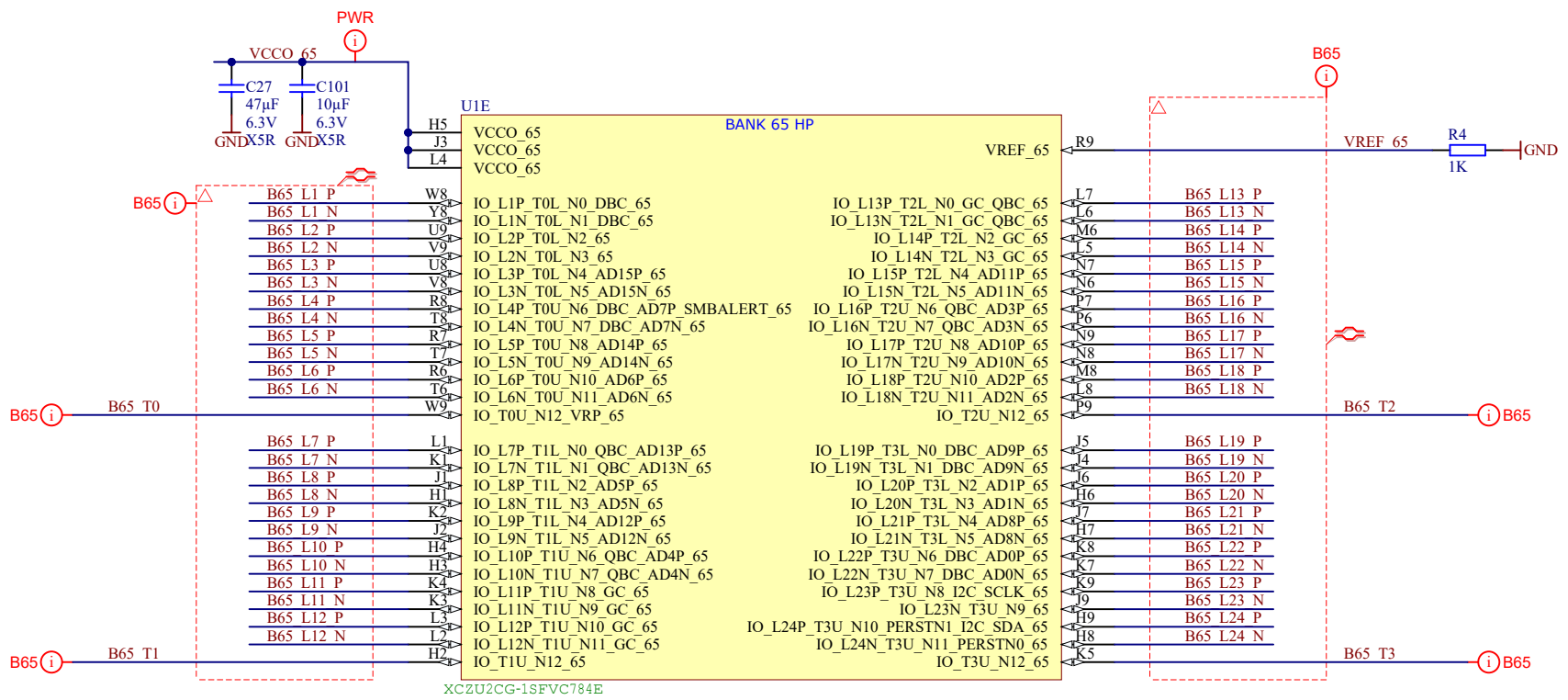
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Date: 07.07.2021	Copyright: Trenz Electronic GmbH / TT	Page8 of 30
Filename: B_HD.SchDoc		



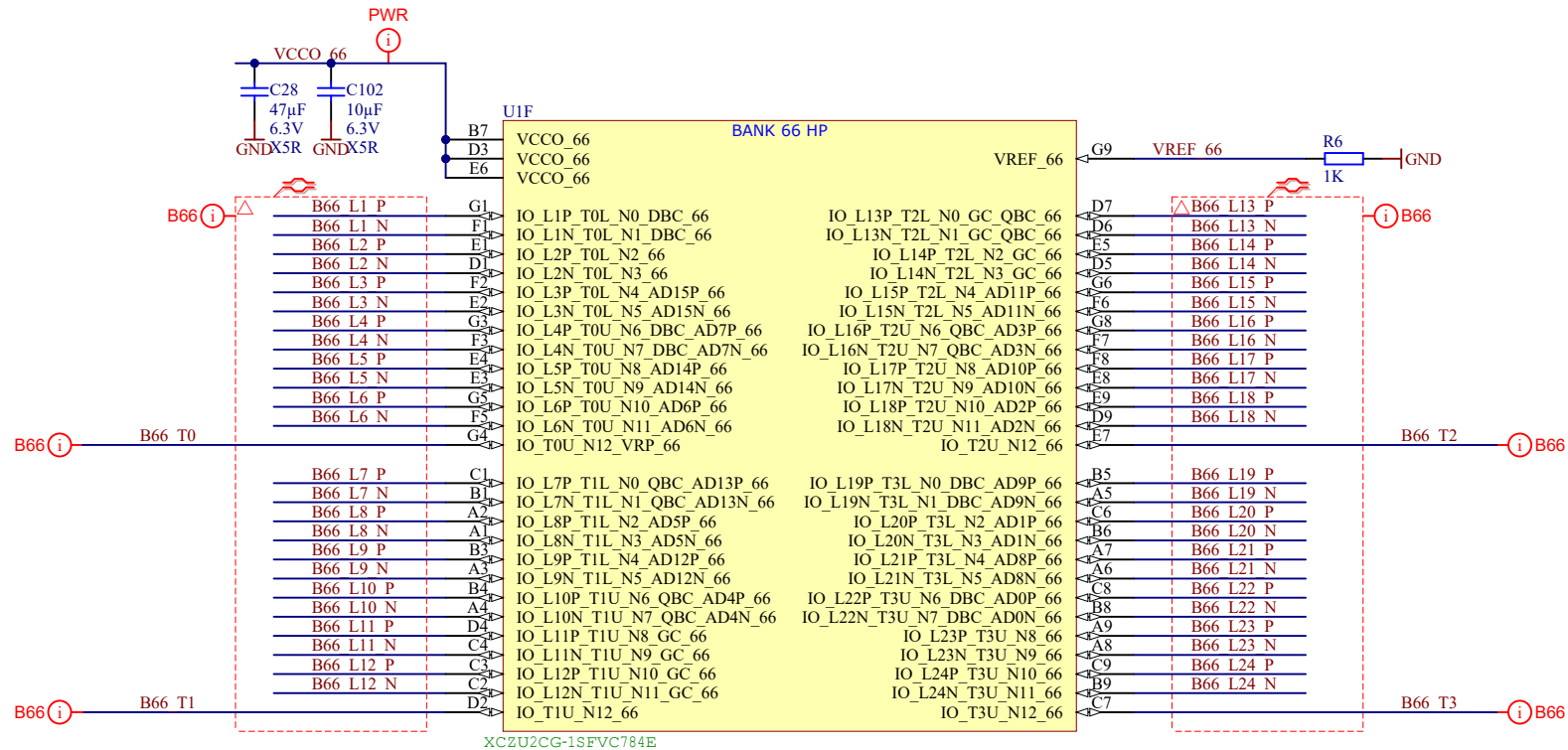


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Date: 07.07.2021	Copyright: Trenz Electronic GmbH / TT	Page9 of 30
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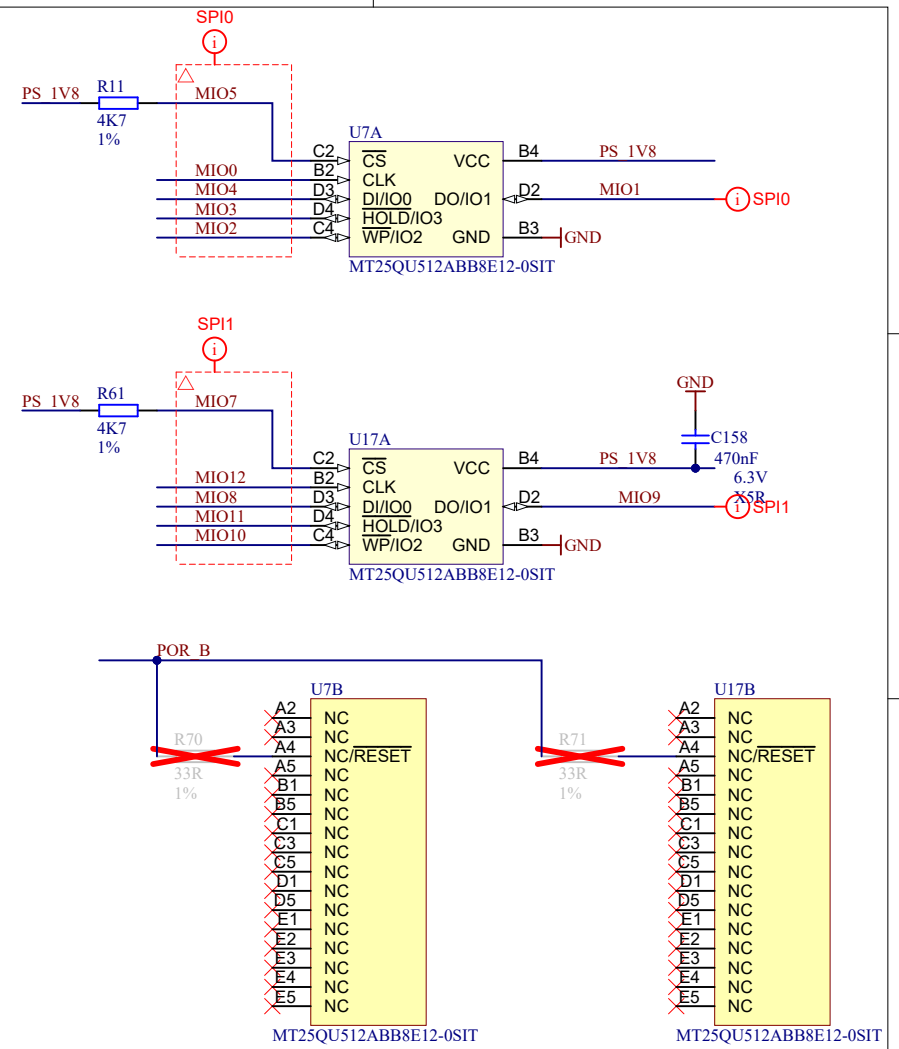
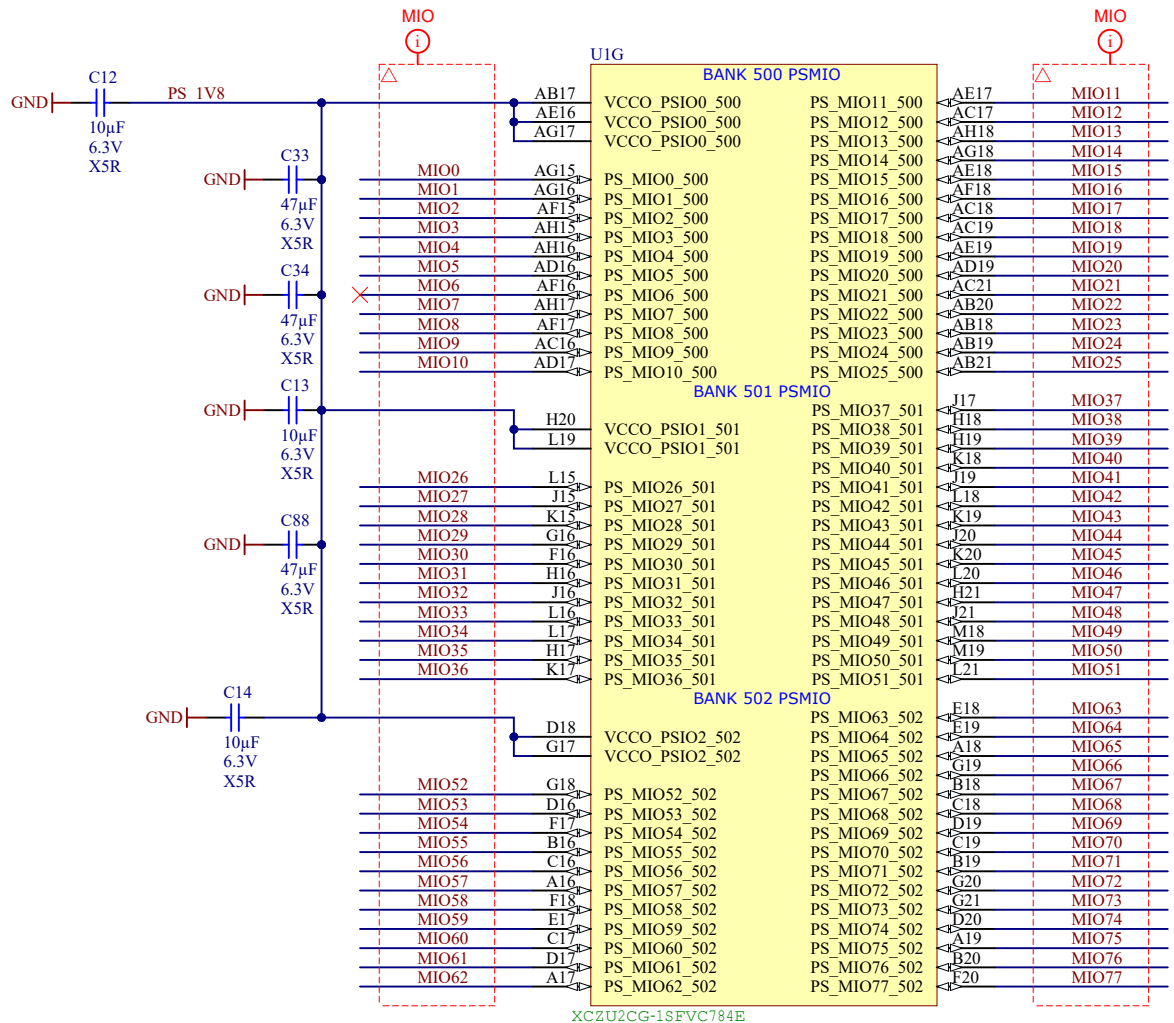




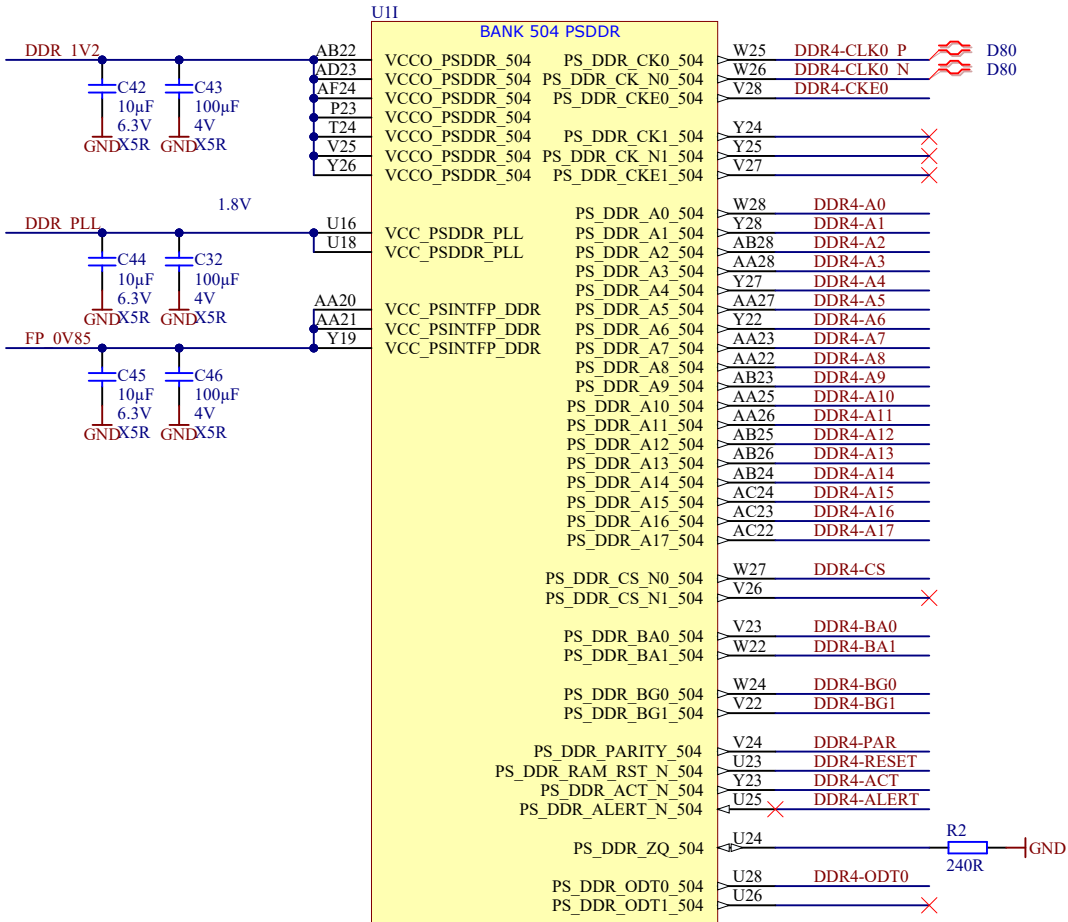
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Date: <b>07.07.2021</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>11</b> of <b>30</b>
Filename: <b>B65.SchDoc</b>		



Title: TE0813 - B66		
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Date: 07.07.2021	Copyright: Trenz Electronic GmbH / TT	Page 12 of 30
Filename: B66.SchDoc		

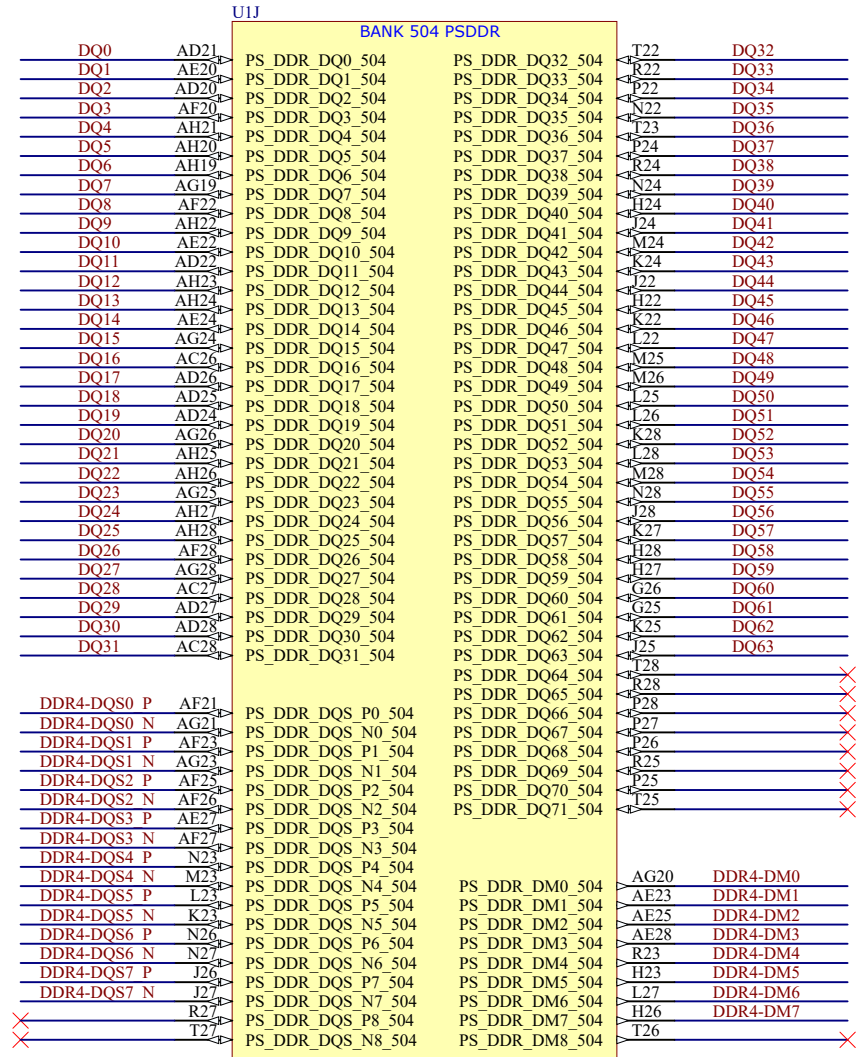


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Date: <b>07.07.2021</b>		Copyright: <b>Trenz Electronic GmbH / TT</b>	
Filename: <b>B_MIO.SchDoc</b>		Rev. <b>01</b>	Page <b>13</b> of <b>30</b>



UII		BANK 504 PSDDR	
VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0 P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0 N
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24	
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25	
VCCO_PSDDR_504	PS_DDR_CKE1_504	V27	
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2
VCC_PSDDR_PLL	PS_DDR_A3_504	AA28	DDR4-A3
VCC_PSDDR_PLL	PS_DDR_A4_504	Y27	DDR4-A4
VCC_PSDDR_PLL	PS_DDR_A5_504	AA27	DDR4-A5
VCC_PSDDR_PLL	PS_DDR_A6_504	Y22	DDR4-A6
VCC_PSDDR_PLL	PS_DDR_A7_504	AA23	DDR4-A7
VCC_PSDDR_PLL	PS_DDR_A8_504	AA22	DDR4-A8
VCC_PSDDR_PLL	PS_DDR_A9_504	AB23	DDR4-A9
VCC_PSDDR_PLL	PS_DDR_A10_504	AA25	DDR4-A10
VCC_PSDDR_PLL	PS_DDR_A11_504	AA26	DDR4-A11
VCC_PSDDR_PLL	PS_DDR_A12_504	AB25	DDR4-A12
VCC_PSDDR_PLL	PS_DDR_A13_504	AB26	DDR4-A13
VCC_PSDDR_PLL	PS_DDR_A14_504	AB24	DDR4-A14
VCC_PSDDR_PLL	PS_DDR_A15_504	AC24	DDR4-A15
VCC_PSDDR_PLL	PS_DDR_A16_504	AC23	DDR4-A16
VCC_PSDDR_PLL	PS_DDR_A17_504	AC22	DDR4-A17
PS_DDR_CS_N0_504		W27	DDR4-CS
PS_DDR_CS_N1_504		V26	
PS_DDR_BA0_504		V23	DDR4-BA0
PS_DDR_BA1_504		W22	DDR4-BA1
PS_DDR_BG0_504		W24	DDR4-BG0
PS_DDR_BG1_504		V22	DDR4-BG1
PS_DDR_PARITY_504		V24	DDR4-PAR
PS_DDR_RAM_RST_N_504		U23	DDR4-RESET
PS_DDR_ACT_N_504		Y23	DDR4-ACT
PS_DDR_ALERT_N_504		U25	DDR4-ALERT
PS_DDR_ZQ_504		U24	
PS_DDR_ODT0_504		U28	DDR4-ODT0
PS_DDR_ODT1_504		U26	

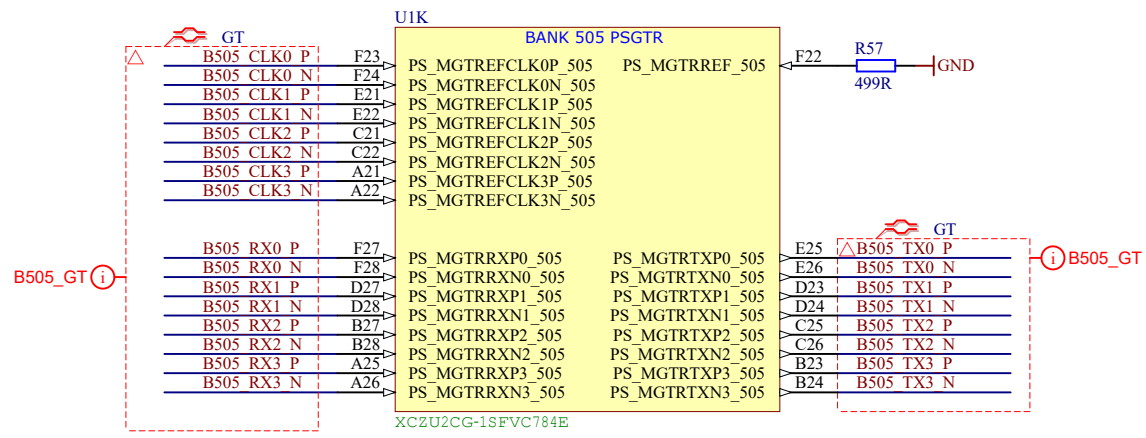
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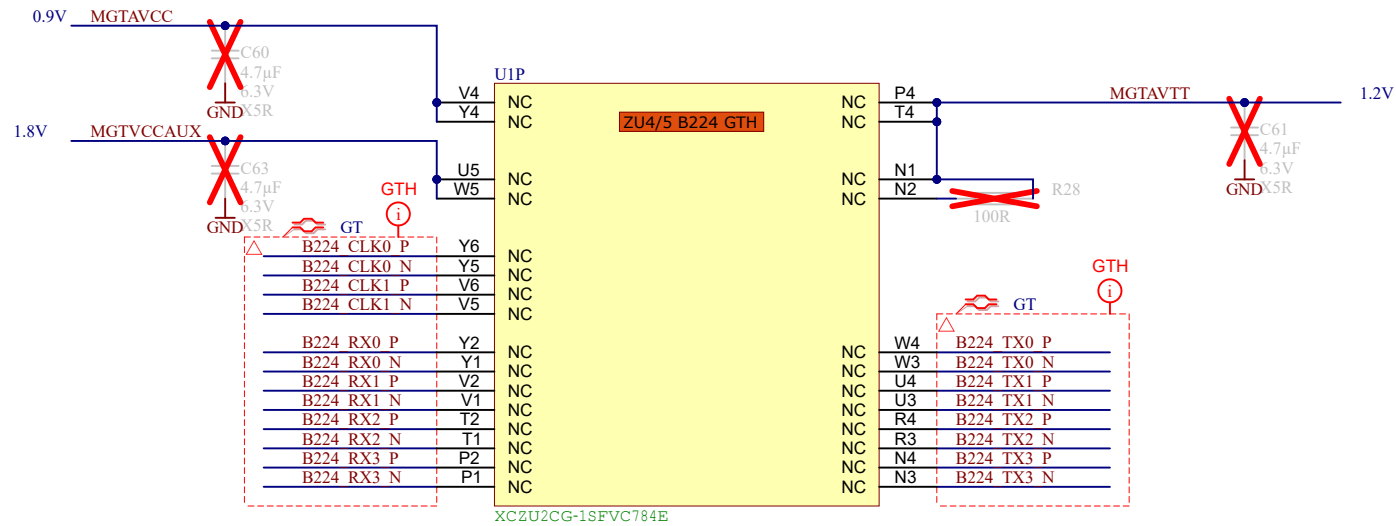
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Title: TE0813 - PS_DDR		
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Date: 07.07.2021	Copyright: Trenz Electronic GmbH / TT	Page 14 of 30
Filename: PS_DDR.SchDoc		

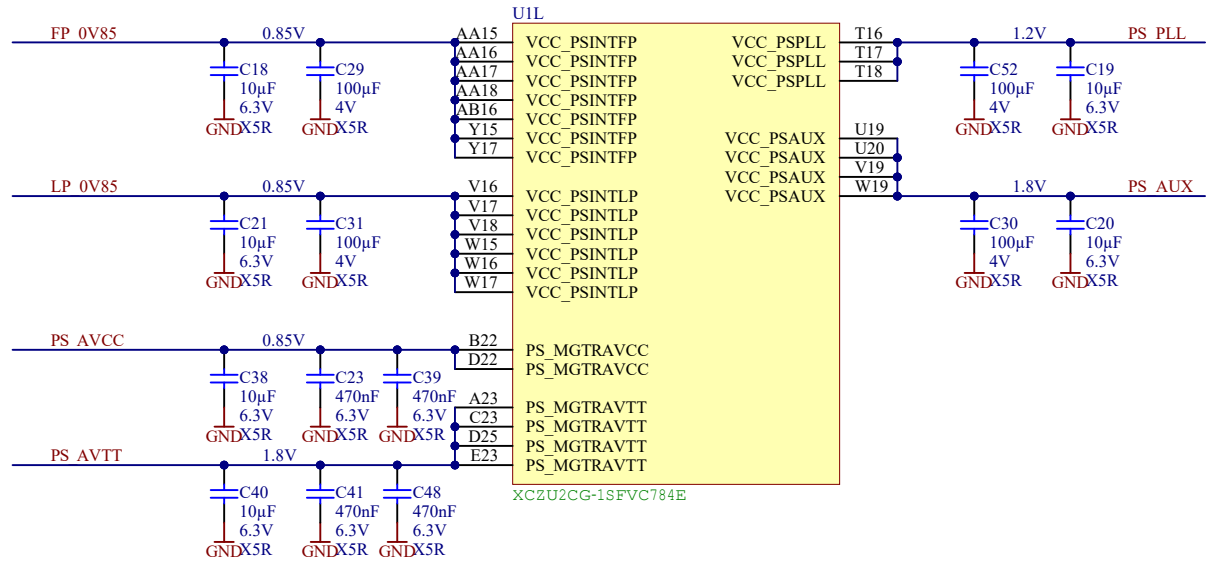



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Date: 07.07.2021	Copyright: Trenz Electronic GmbH / TT	Page 15 of 30
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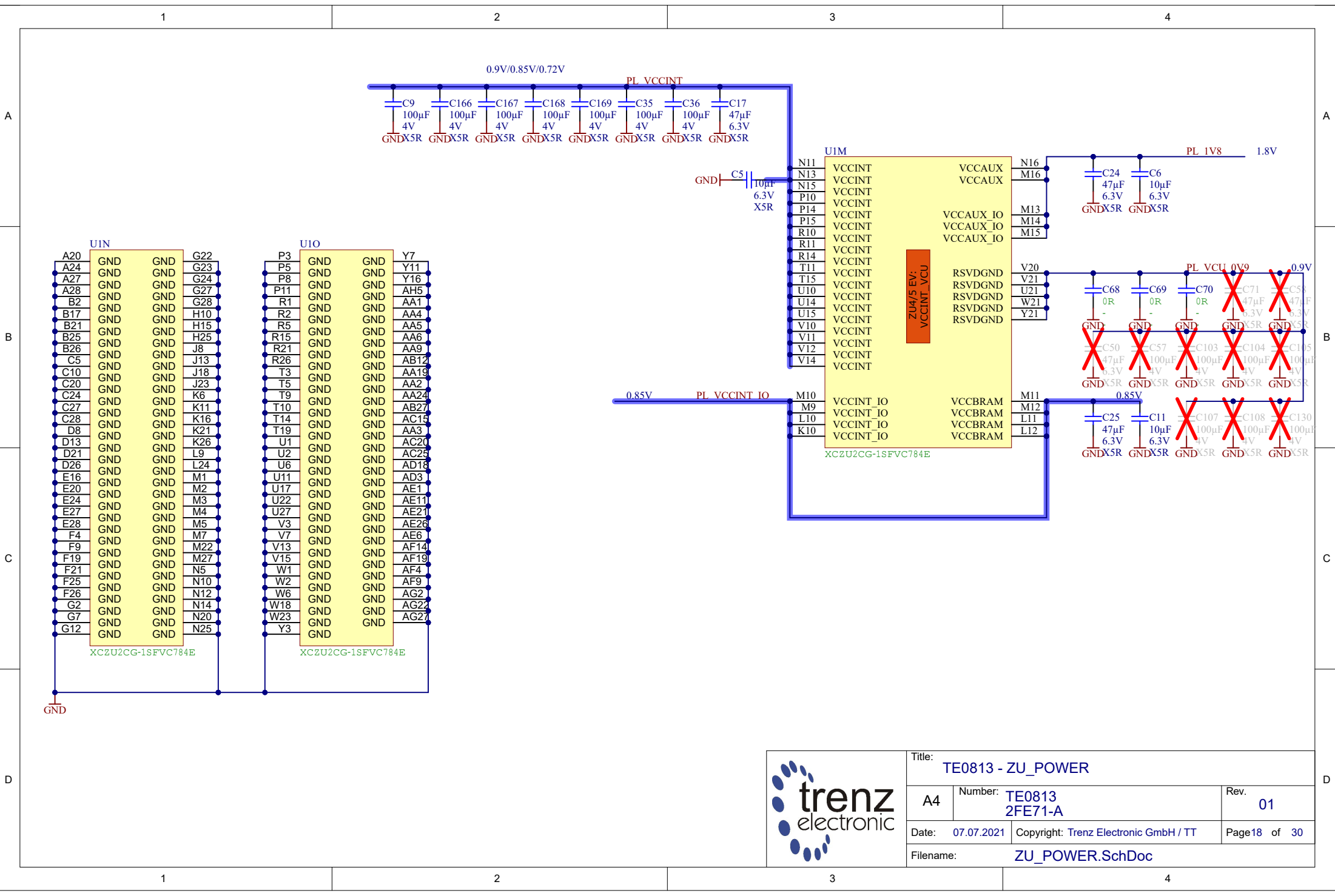


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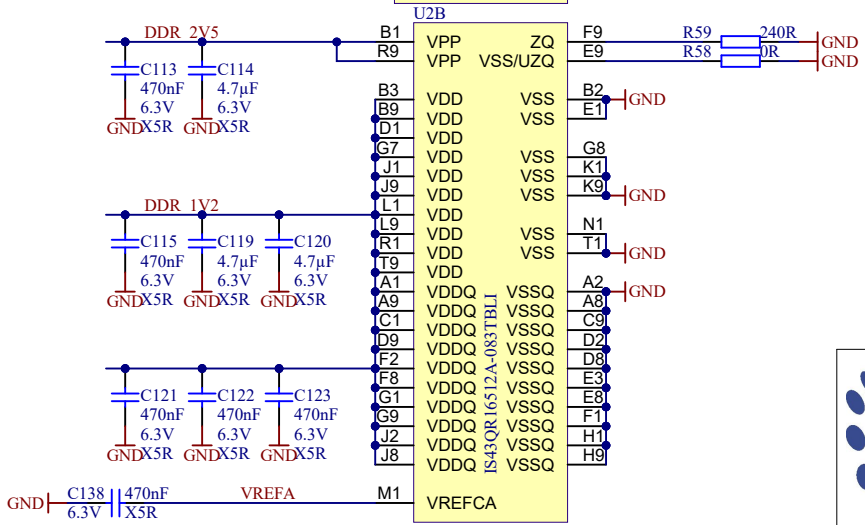
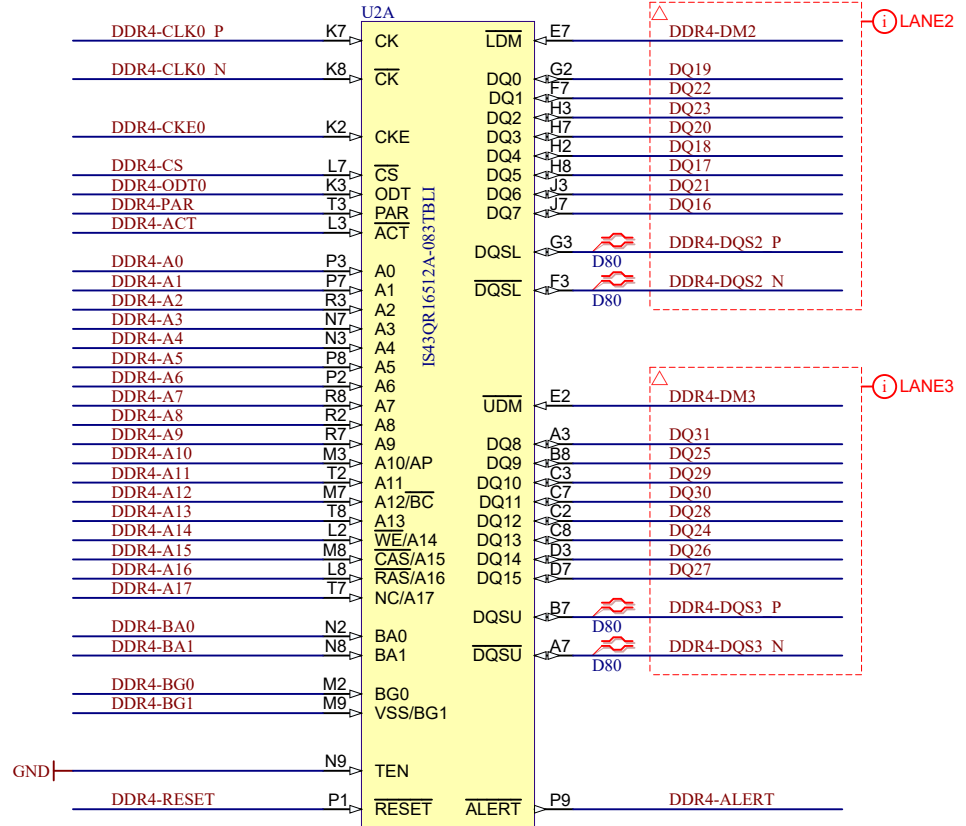




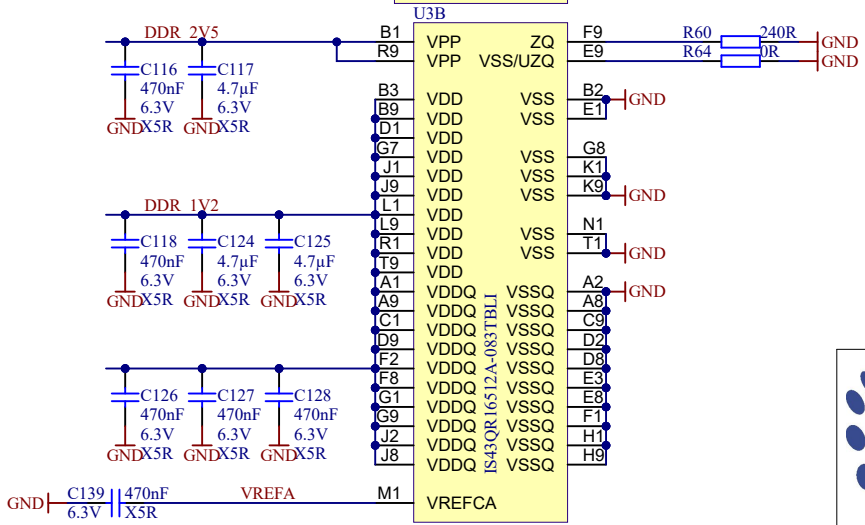
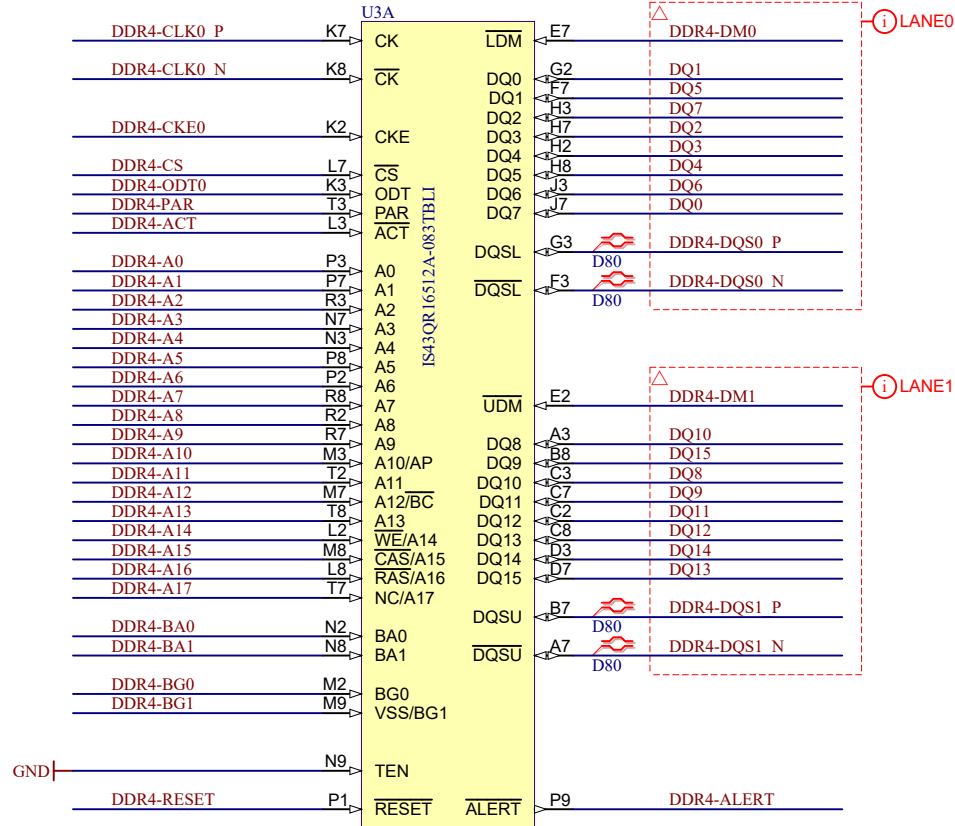
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	Date: 07.07.2021	Copyright: Trenz Electronic GmbH / TT
	Rev. 01	Page 17 of 30
Filename: ZU_PS_POWER.SchDoc		



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Date: 07.07.2021	Copyright: Trenz Electronic GmbH / TT	Page 18 of 30
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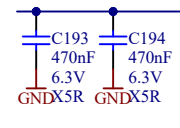
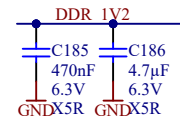
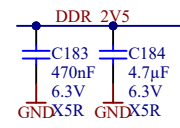
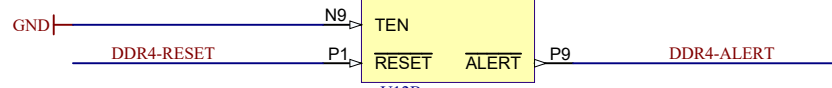
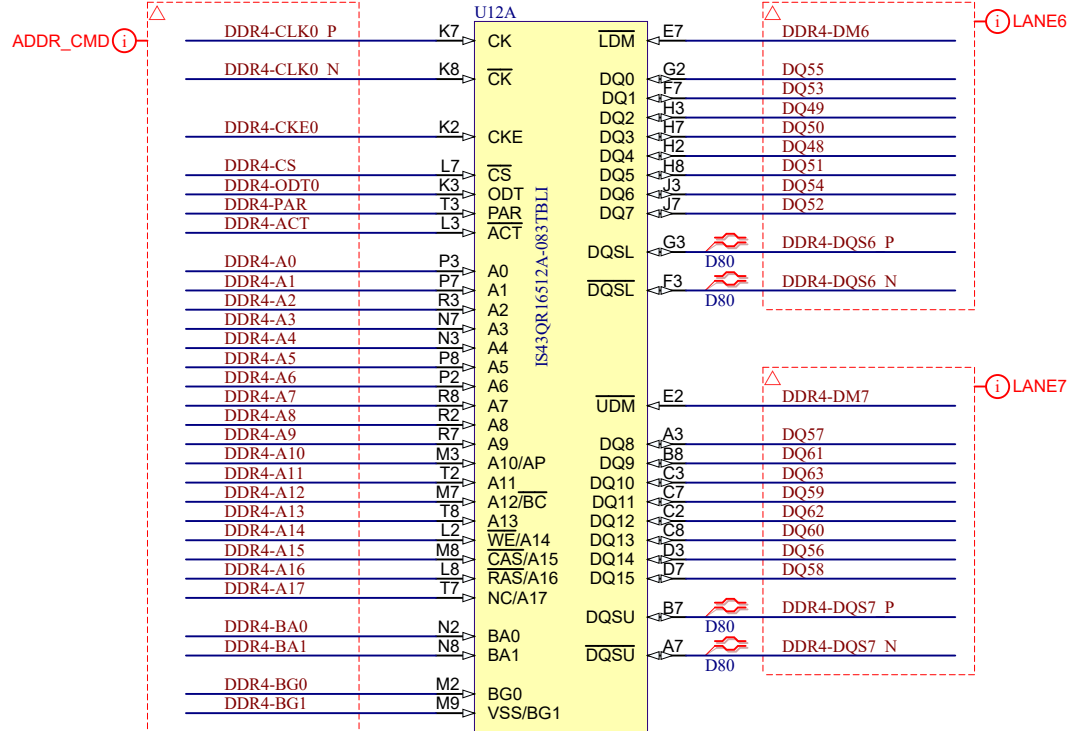



Title: <b>TE0813 - DDR4_1_RAM</b>		
A4	Number: <b>TE0813 2FE71-A</b>	Rev. <b>01</b>
Date: <b>07.07.2021</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>19</b> of <b>30</b>
Filename: <b>DDR4-RAM.SchDoc</b>		



Title: TE0813 - DDR4_2_RAM		
A4	Number: TE0813 2FE71-A	Rev. 01
Date: 07.07.2021	Copyright: Trenz Electronic GmbH / TT	Page 20 of 30
Filename: DDR4-RAM_2.SchDoc		



Title: TE0813 - DDR4_4_RAM		
A4	Number: TE0813 2FE71-A	Rev. 01
Date: 07.07.2021	Copyright: Trenz Electronic GmbH / TT	Page 22 of 30
Filename: DDR4-RAM_4.SchDoc		

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A

A

B

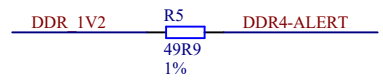
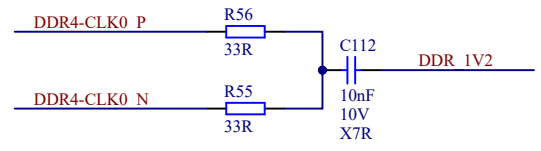
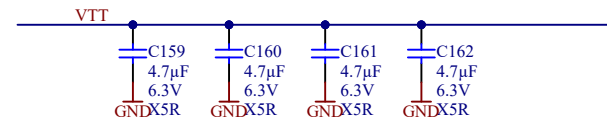
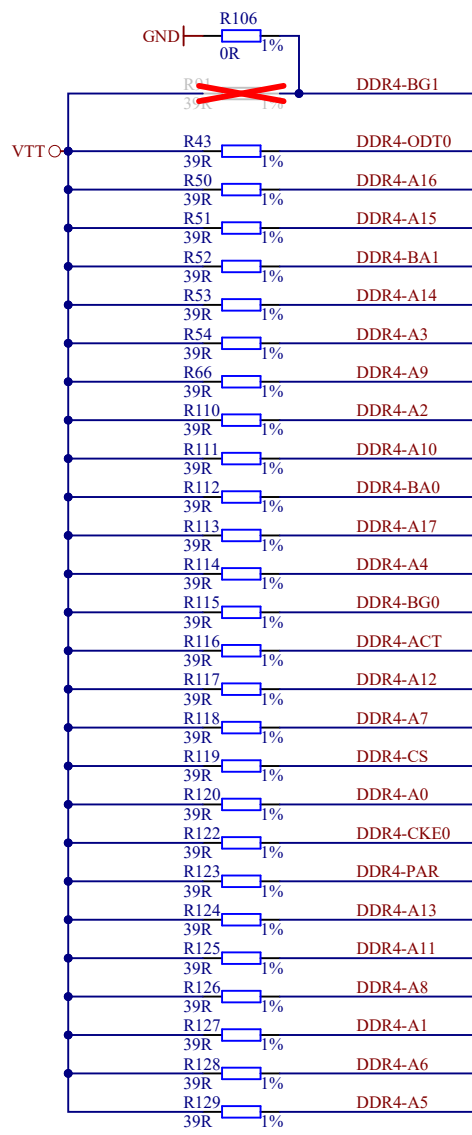
B

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C

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D



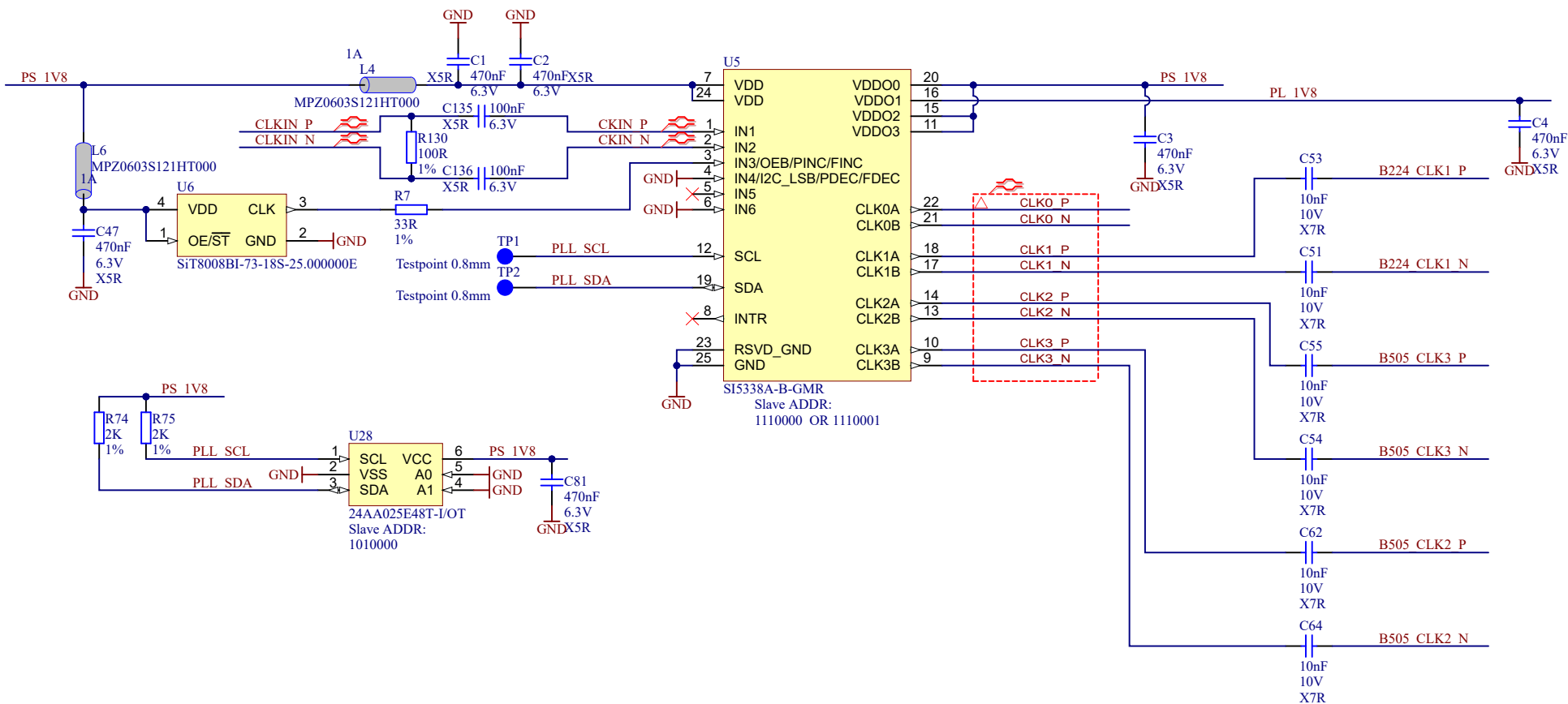
Title: TE0813 - DDR4_TERM		
A4	Number: TE0813 2FE71-A	Rev. 01
Date: 07.07.2021	Copyright: Trenz Electronic GmbH / TT	Page23 of 30
Filename: DDR4-TERM.SchDoc		


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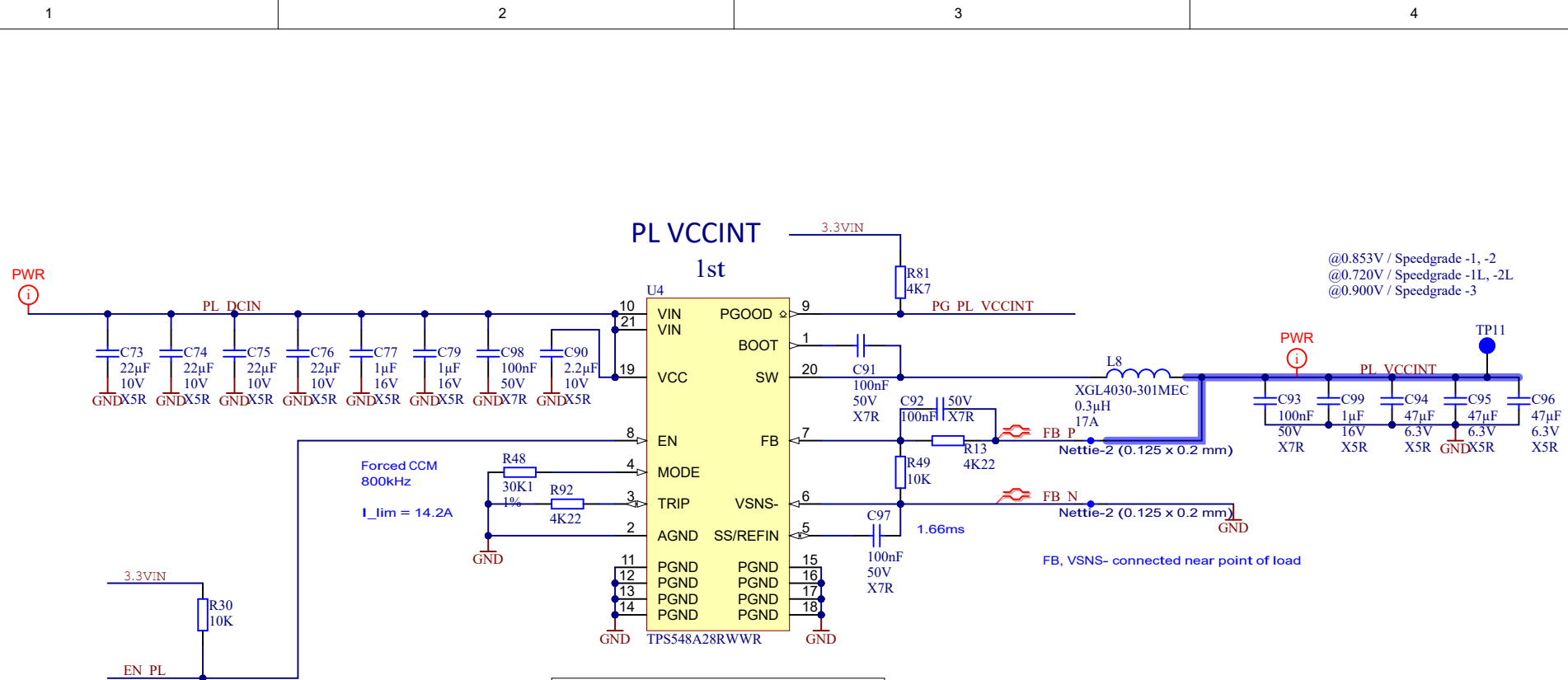
3

4



			Title: TE0813 - CLOCK	
			A4	Number: TE0813 2FE71-A
Date: 07.07.2021		Copyright: Trenz Electronic GmbH / TT		Page24 of 30
Filename: Clock.SchDoc				






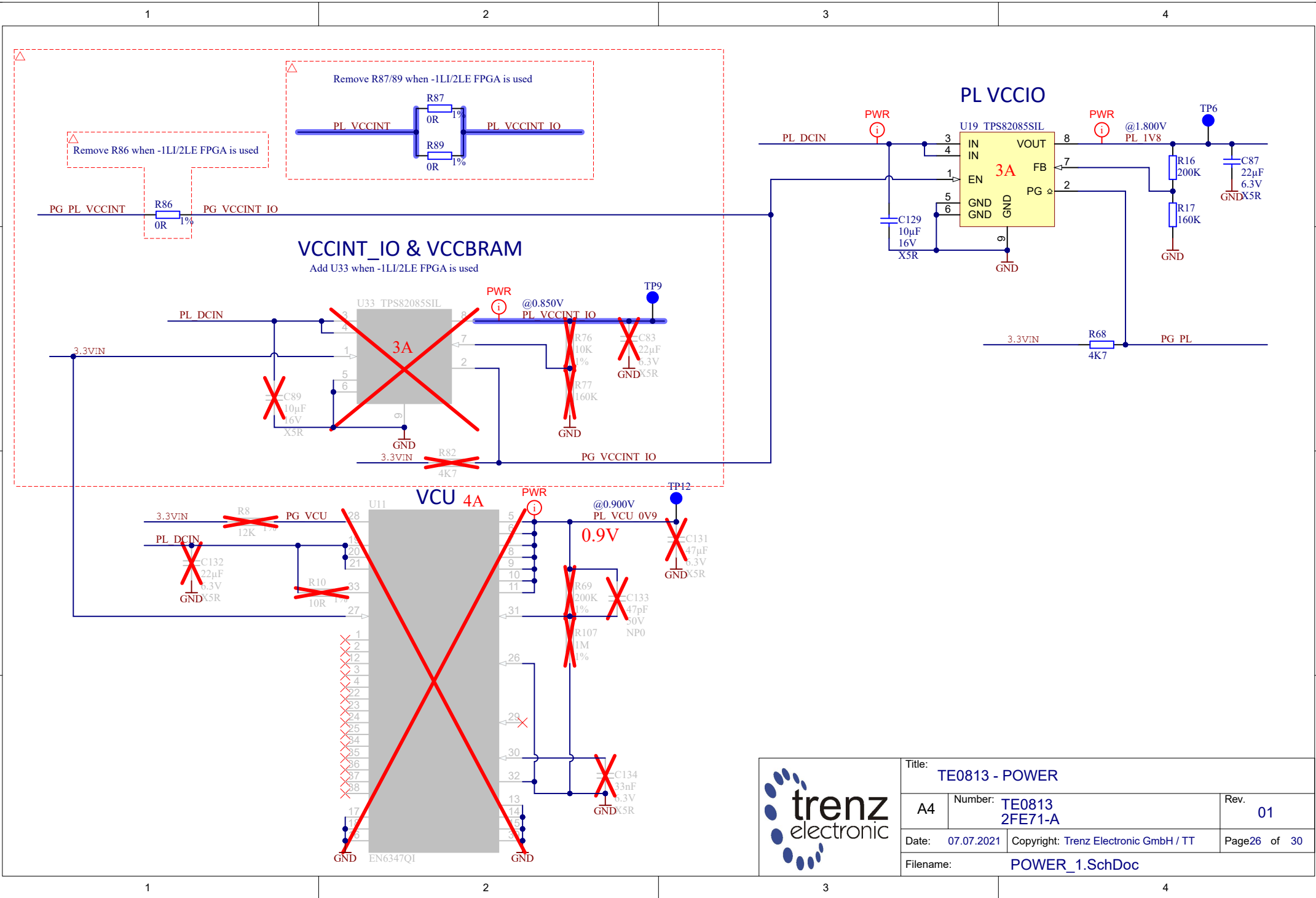
FPGA Speed grade:

-1L / -2LE	R13 - 2K, R49 - 10K	PL_VCCINT = 0.720V
-1 / -2	R13 - 4K22, R49 - 10K	PL_VCCINT = 0.853V
-3E	R13 - 10K, R49 - 20K	PL_VCCINT = 0.900V

U4 pin compatible with  
 -- TPS548B28 (20A)  
 -- TPS54JA20 (12A)



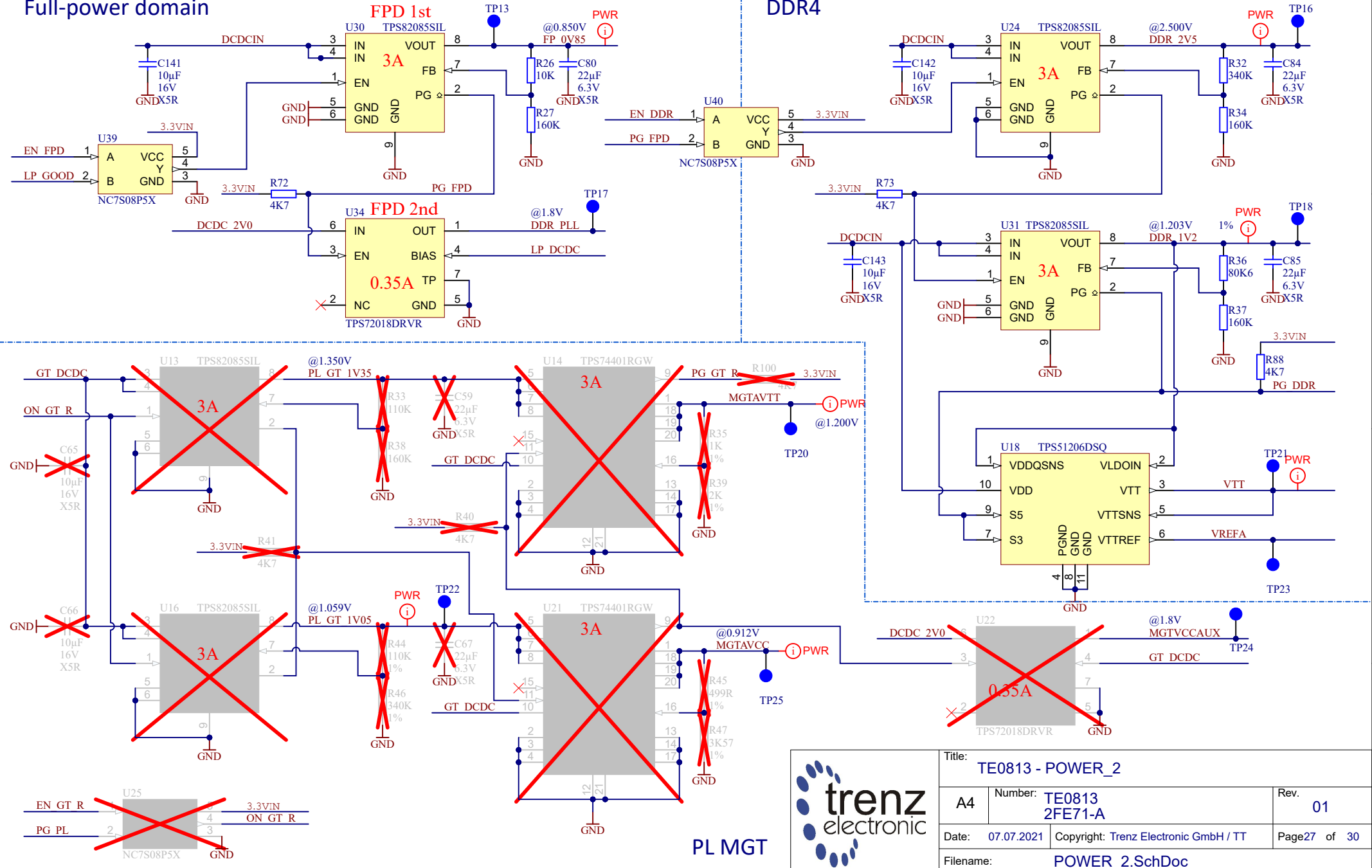
Title: <b>TE0813 - POWER</b>		
A4	Number: <b>TE0813 2FE71-A</b>	Rev. <b>01</b>
Date: <b>07.07.2021</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>25</b> of <b>30</b>
Filename: <b>POWER.SchDoc</b>		



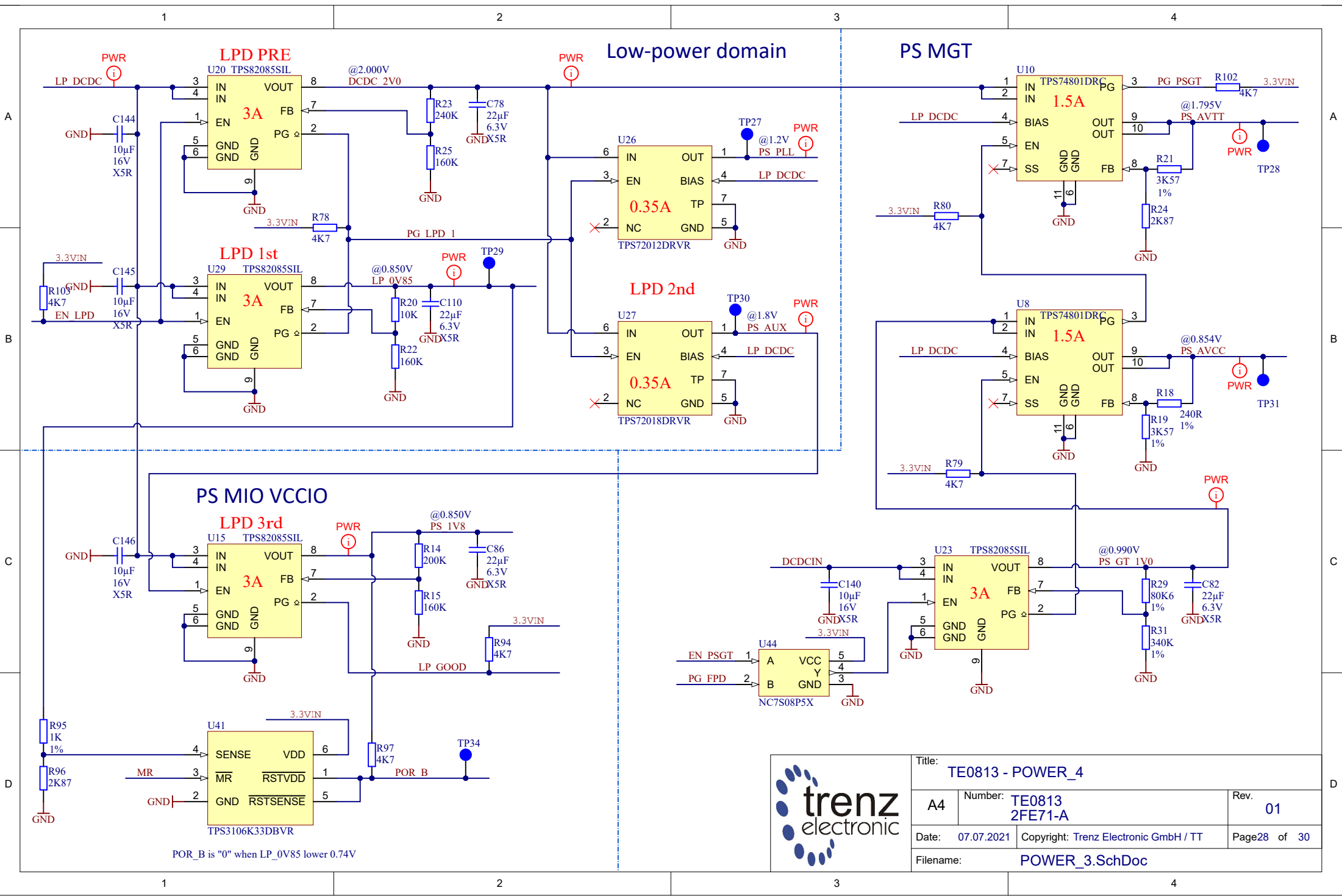
Title: TE0813 - POWER		
A4	Number: TE0813 2FE71-A	Rev. 01
Date: 07.07.2021	Copyright: Trenz Electronic GmbH / TT	Page 26 of 30
Filename: POWER_1.SchDoc		

# Full-power domain

# DDR4



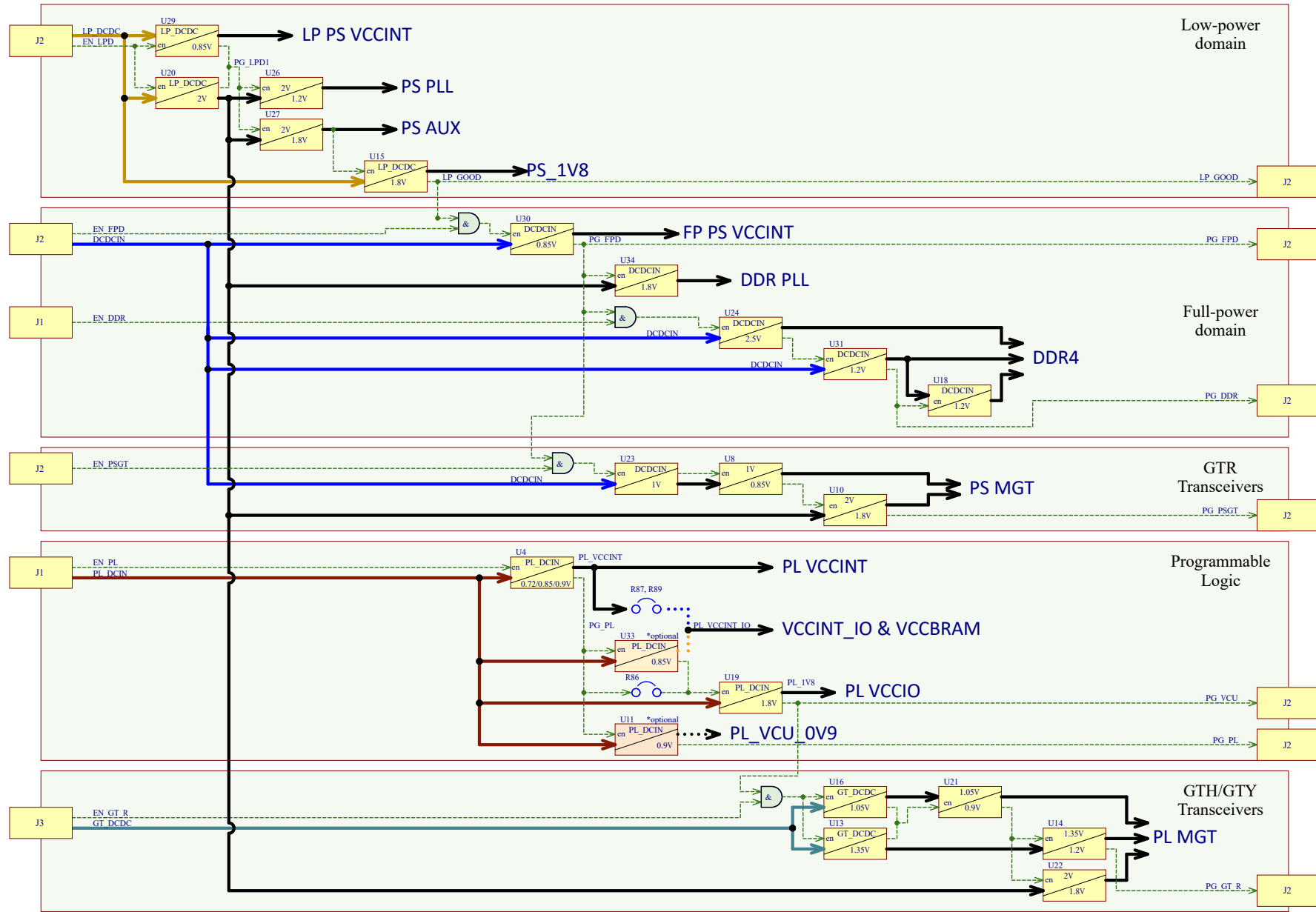
Title: <b>TE0813 - POWER_2</b>		
A4	Number: <b>TE0813 2FE71-A</b>	Rev. <b>01</b>
Date: <b>07.07.2021</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>27</b> of <b>30</b>
Filename: <b>POWER_2.SchDoc</b>		



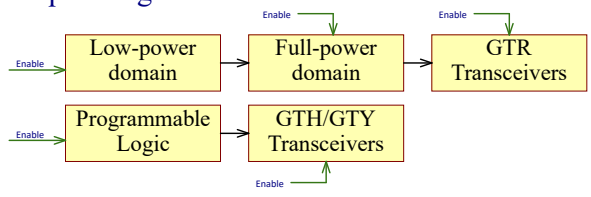
POR\_B is "0" when LP\_0V85 lower 0.74V



Title: TE0813 - POWER_4		
A4	Number: TE0813 2FE71-A	Rev. 01
Date: 07.07.2021	Copyright: Trenz Electronic GmbH / TT	Page28 of 30
Filename: POWER_3.SchDoc		



**Power-on sequencing:**



- EN\_GT\_R Net name
- Power bus
- Control signal
- Power bus in FPGA speedgrade -1/-2/-3 assembly variants
- Power bus in FPGA speedgrade -1L/-2L assembly variants (low power)
- PL\_DCIN 0.9V Optional power converter
- & Logic AND gate



Title: TE0813 - Power Diagram		
A3	Number: TE0813 2FE71-A	Rev. 01
Datum: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 29 of 30
Filename: Power_Diagram.SchDoc		

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A

A

B

B


C

C

D

D

REV	DATE	Description	
-01	2021-05	Initial revision	VT

				Title: <b>TE0813 - Revision History</b>		
				A4	Number: <b>TE0813 2FE71-A</b>	Rev. <b>01</b>
Date: <b>2021-01-19</b>		Copyright: <b>Trenz Electronic GmbH</b>		Page <b>30</b> of <b>30</b>		
Drawn by: <b>VT</b>			Filename: <b>Revision Changes.SchDoc</b>			

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4