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Schematics and other handouts serve for informational purposes only!

	Title: TE0813		
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Cannot open file C:\Users\vitalitsiukala\Pictures\BD-TE0813-01.png. File does not exist.

Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
PL_DCIN	IN	3.3 - 5.0V	+/-5%	Micromodule Power	Programmable Logic, supplied by power rail
LP_DCDC	IN	3.3 - 5.0V	+/-5%	Micromodule Power	Low-Power Domain, supplied by power rail
GT_DCDC	IN	3.3 - 5.0V	+/-5%	Micromodule Power	GTH/GTY Transceiver, supplied by power rail
VCCO_64	IN	1.0 - 1.8V	+/-3%	HP IO Bank64	-
VCCO_65	IN	1.0 - 1.8V	+/-3%	HP IO Bank65	-
VCCO_66	IN	1.0 - 1.8V	+/-3%	HP IO Bank66	-
VCCO_25	IN	1.2 - 3.3V	+/-3%	HD IO Bank25	-
VCCO_26	IN	1.2 - 3.3V	+/-3%	HD IO Bank26	-
PSBATT	IN	1.2 - 1.5V	-	RTC / BBRAM	-
PL_1V8	OUT	1.8V	+/-5%	Power for Carrier	Micromodule: Programmable Logic
PS_1V8	OUT	1.8V	+/-5%	Power for Carrier	Micromodule: Processing System
DDR_1V2	OUT	1.2V	+/-5%	Power for Carrier	Micromodule: PS DDR I/O Supply

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REV	DATE	Description	
-01	2021-05	Initial revision	VT
	2022-03	Added Table with Supported Voltage Ranges	
	2022-05	Changed DCDC U4 TPS548A28 to MPQ8633BGLE-Z Changed C92 100nF to 1nF	

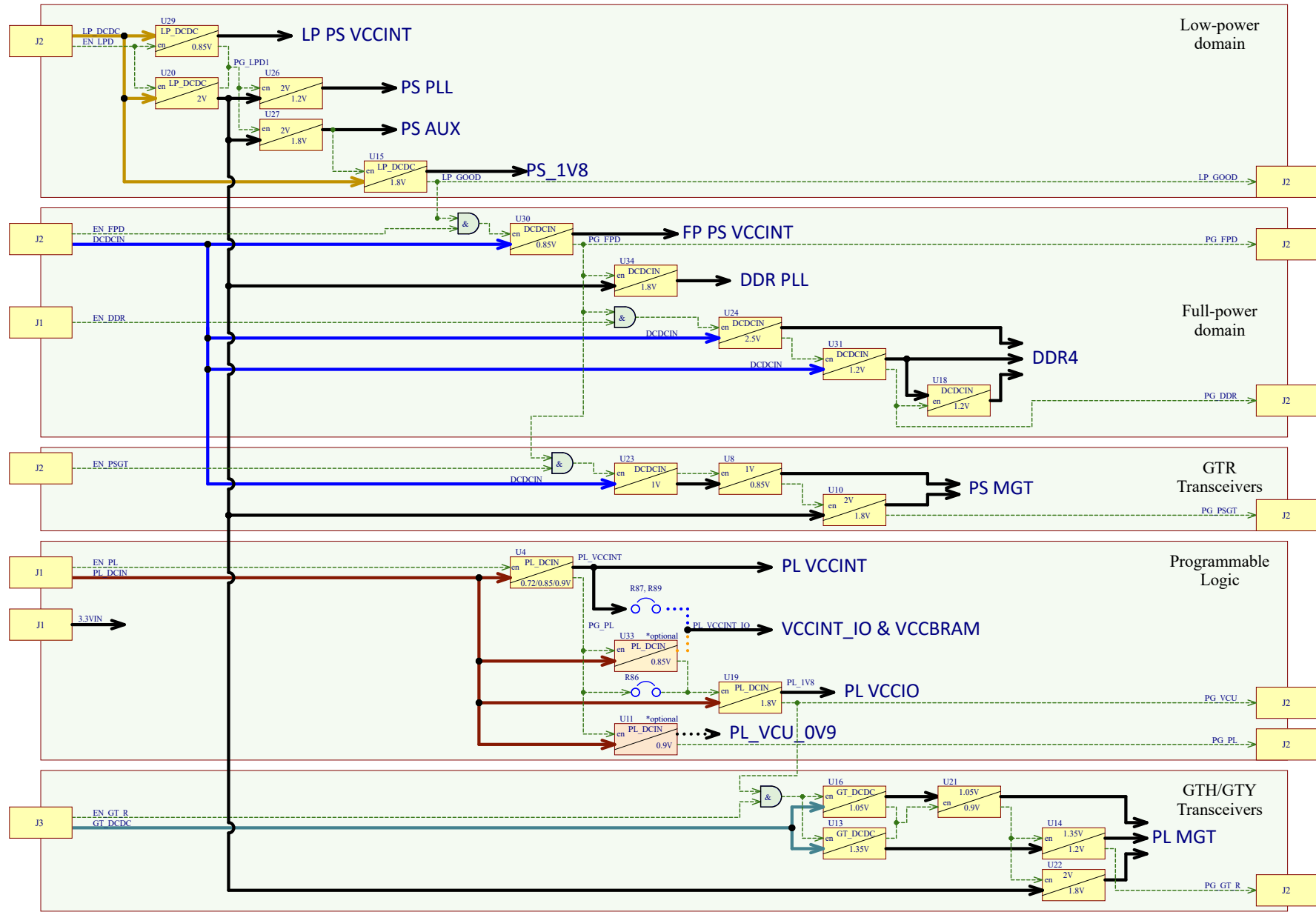
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	Filename: Revision Changes.SchDoc		

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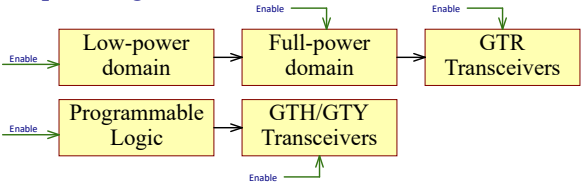
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Power-on sequencing:



- Net name
- Power bus
- Control signal
- Power bus in FPGA speedgrade -1/-2/-3 assembly variants
- Power bus in FPGA speedgrade -1L/-2L assembly variants (low power)
- Optional power converter
- Logic AND gate



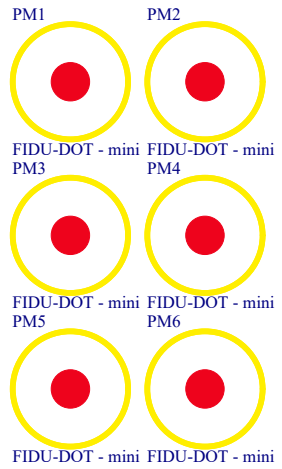
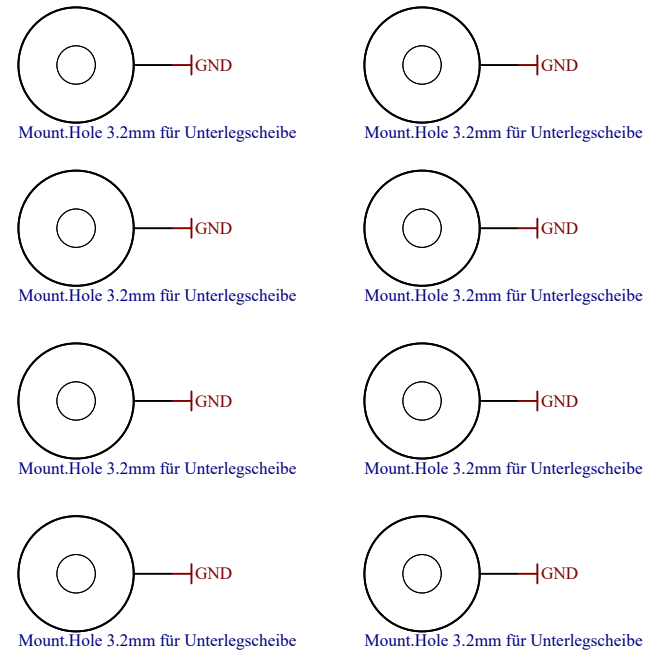
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A3	Number: TE0813 5DI81-A	Rev. 01
Datum: 2021-01-19	Copyright: Trenz Electronic GmbH	Page 4 of 30
Filename: Power_Diagram.SchDoc		

U_J1
J1.SchDoc
U_J2
J2.SchDoc
U_J3
J3.SchDoc
U_J4
J4.SchDoc
U_DDR4-TERM
DDR4-TERM.SchDoc
U_B64
B64.SchDoc
U_B65
B65.SchDoc
U_B66
B66.SchDoc
U_B_GT
B_GT.SchDoc

U_B_PS_GT
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U_ZU_POWER
ZU_POWER.SchDoc
U_ZU_PS_POWER
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U_POWER
POWER.SchDoc
U_POWER_1
POWER_1.SchDoc
U_POWER_2
POWER_2.SchDoc
U_POWER_4
POWER_3.SchDoc

Special notes:




MECH1
TE Address Overlay
LOGO ADDRESS

LOGO1
TE Logo PRINT Layer
LOGO PRINT

Serial
Serial
Serialnumber 6,3 x 6.3mm

Assembly variant	5DI81-A
Created by	ED
Modified by	ED
Modified at	2022-07-19
SVN Revision	

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JM1A

JM1B

ADM6-60-01.5-L-4-2

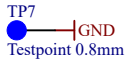
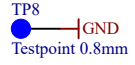
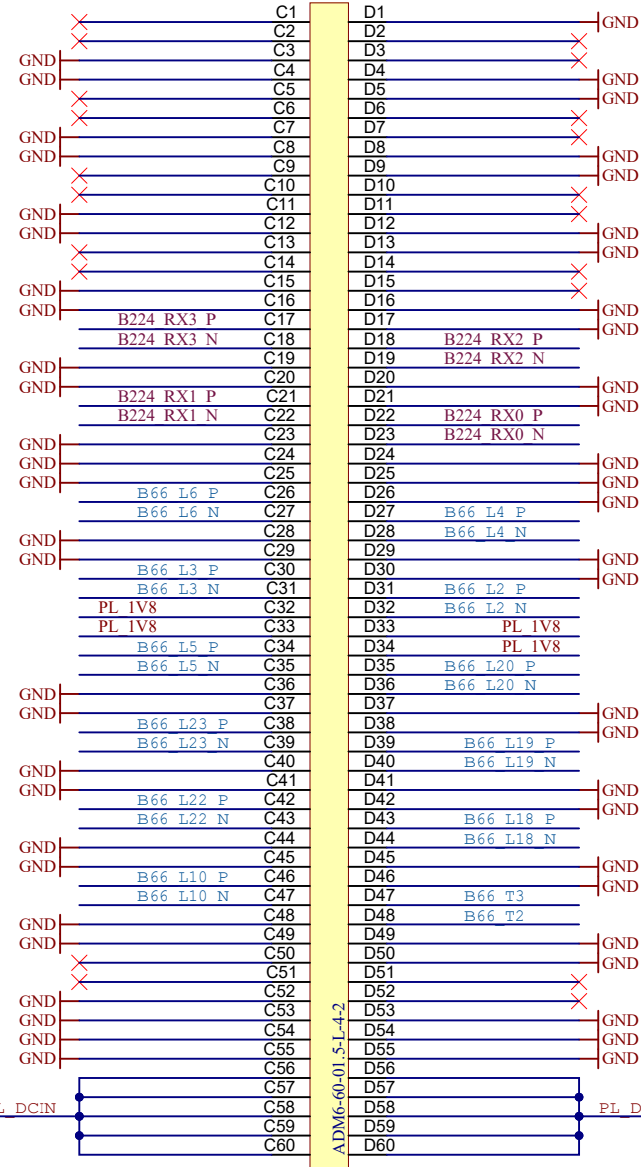
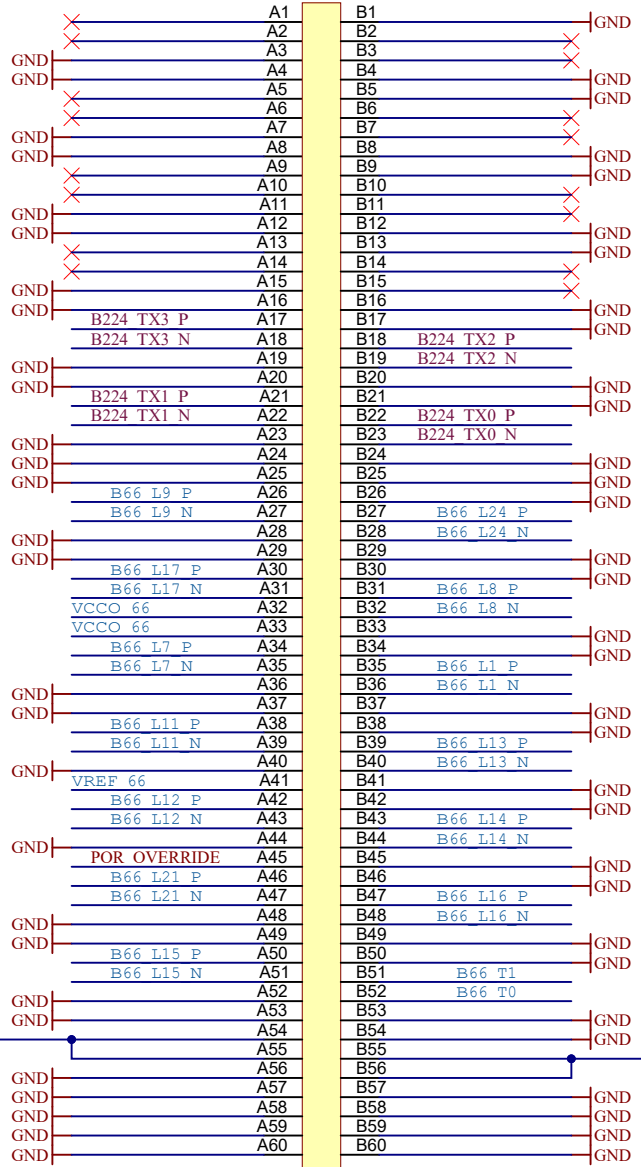
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3.3VIN

3.3VIN

PL_DCIN

PL_DCIN



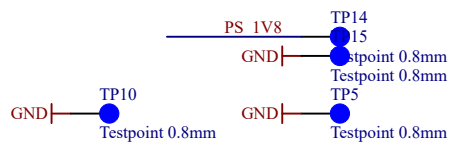
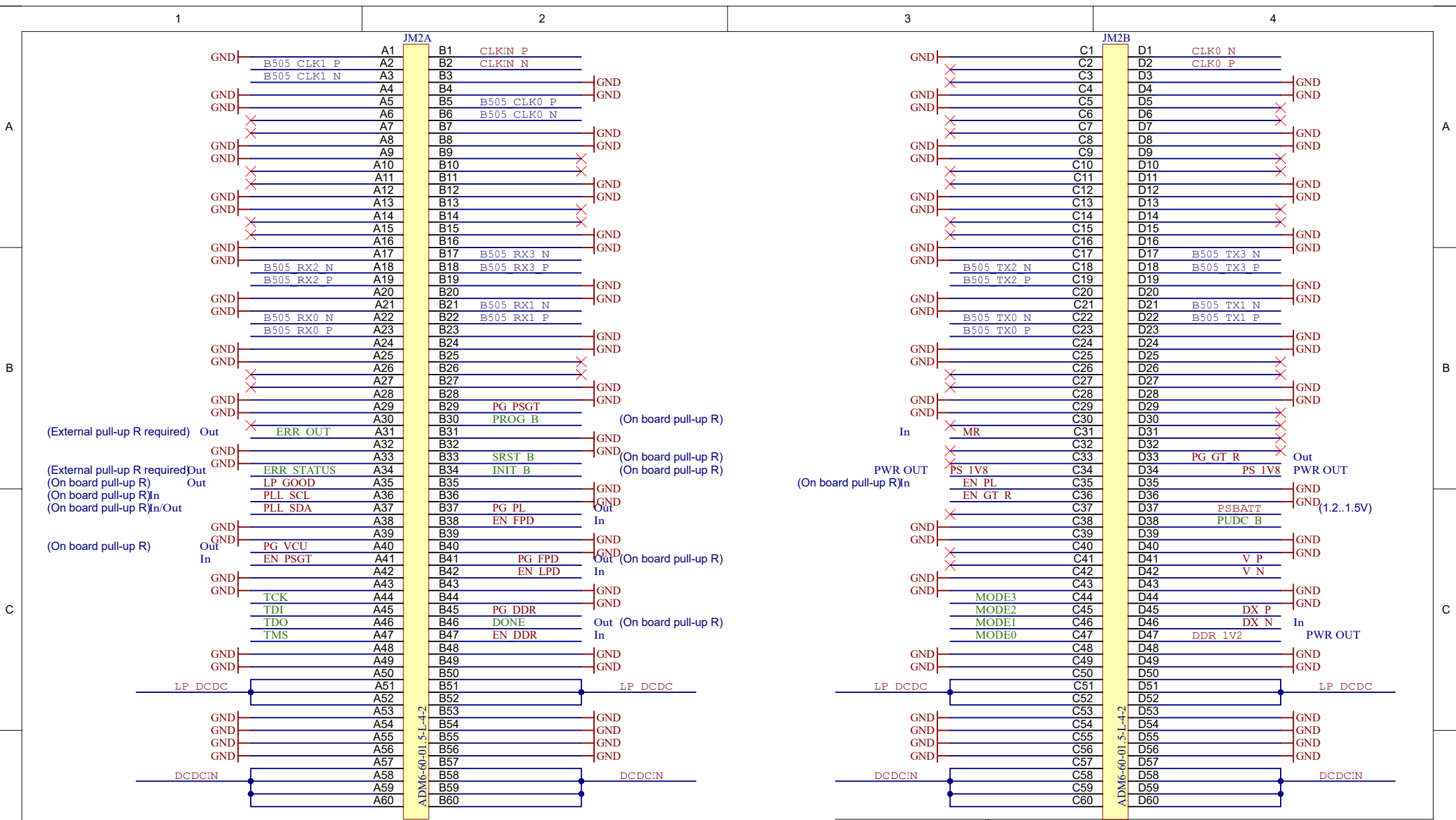
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Filename: J1.SchDoc		

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Title: TE0813 - Connector J2		
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D

JM3A
ADM6-60-01_5-L-4-2

JM3B
ADM6-60-01_5-L-4-2

*Bank 25 for XCZU2/3
*Bank 45 for XCZU4/6
**Bank 26 for XCZU2/3
**Bank 46 for XCZU4/5

CLK IN

PWR IN
PWR IN

PWR IN
PWR IN

CLK IN

PWR IN
PWR IN

PWR IN
PWR IN

PS 1V8

PS 1V8

PS 1V8

PS 1V8

MIO1_L

MIO1_H

MIO2_L

MIO2_H

MIO0_H

MIO26	MIO32	MIO38	MIO45	MIO52	MIO58	MIO64	MIO71	MIO13	MIO19
MIO27	MIO33	MIO39	MIO46	MIO53	MIO59	MIO65	MIO72	MIO14	MIO20
MIO28	MIO34	MIO40	MIO47	MIO54	MIO60	MIO66	MIO73	MIO15	MIO21
MIO29	MIO35	MIO41	MIO48	MIO55	MIO61	MIO67	MIO74	MIO16	MIO22
MIO30	MIO36	MIO42	MIO49	MIO56	MIO62	MIO68	MIO75	MIO17	MIO23
MIO31	MIO37	MIO43	MIO50	MIO57	MIO63	MIO69	MIO76	MIO18	MIO24
		MIO44	MIO51			MIO70	MIO77		MIO25



Title: TE0813 - Connector J3		
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Filename: J3.SchDoc		

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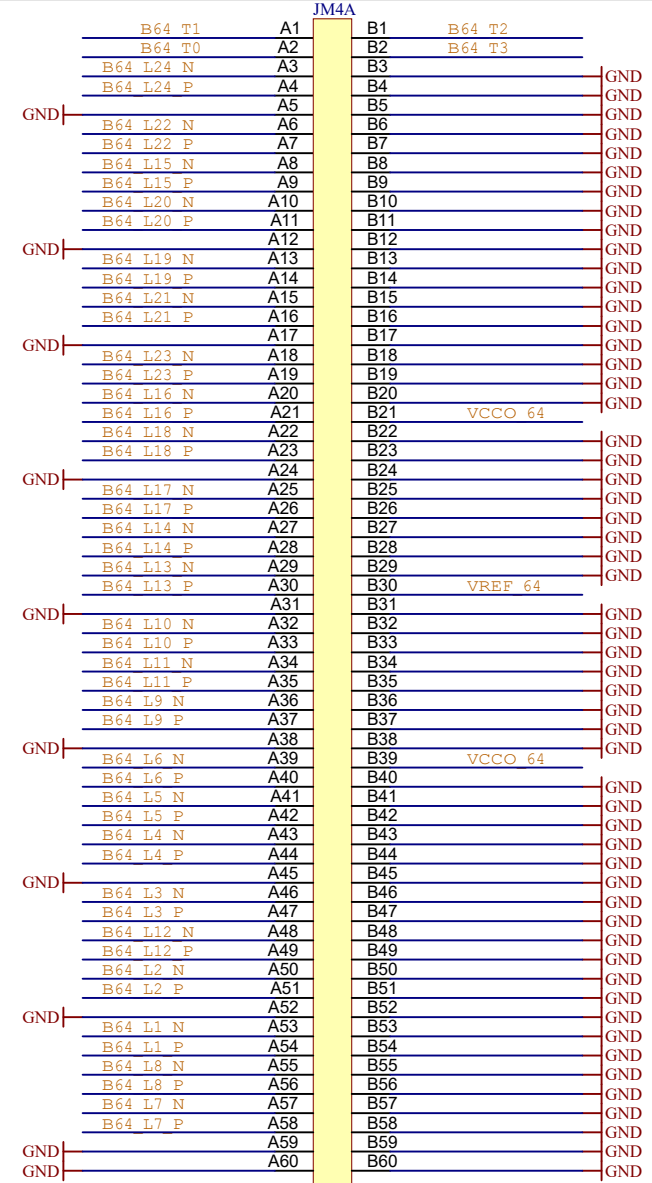
B

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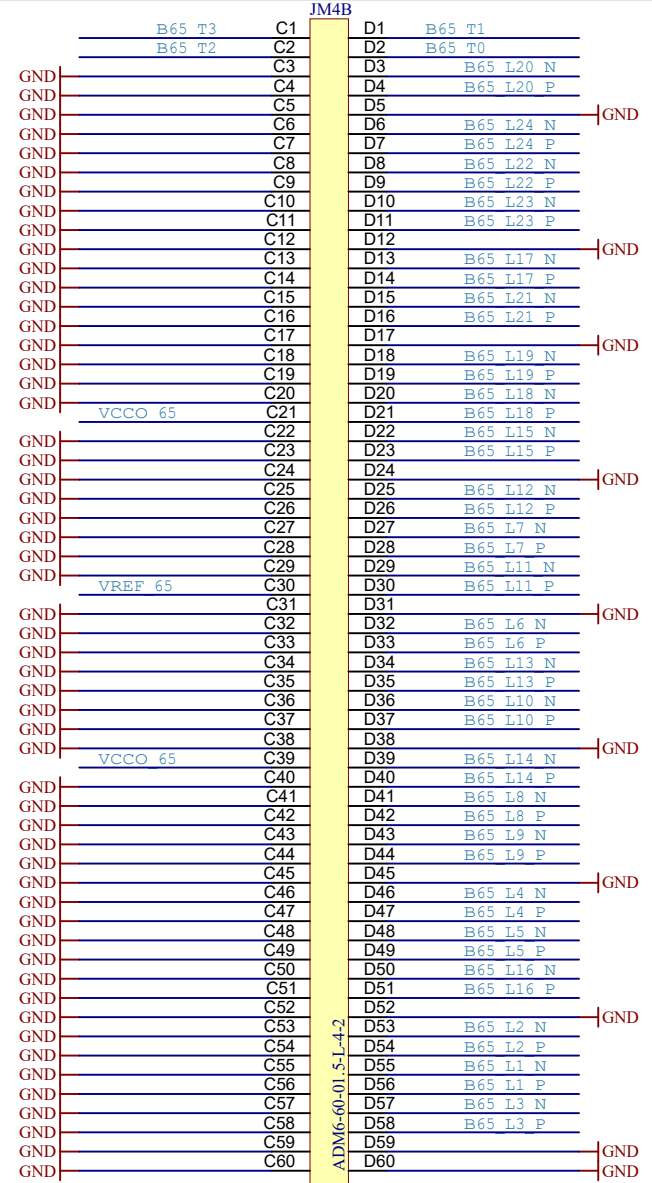
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ADM6-60-01.5-L-4-2



ADM6-60-01.5-L-4-2



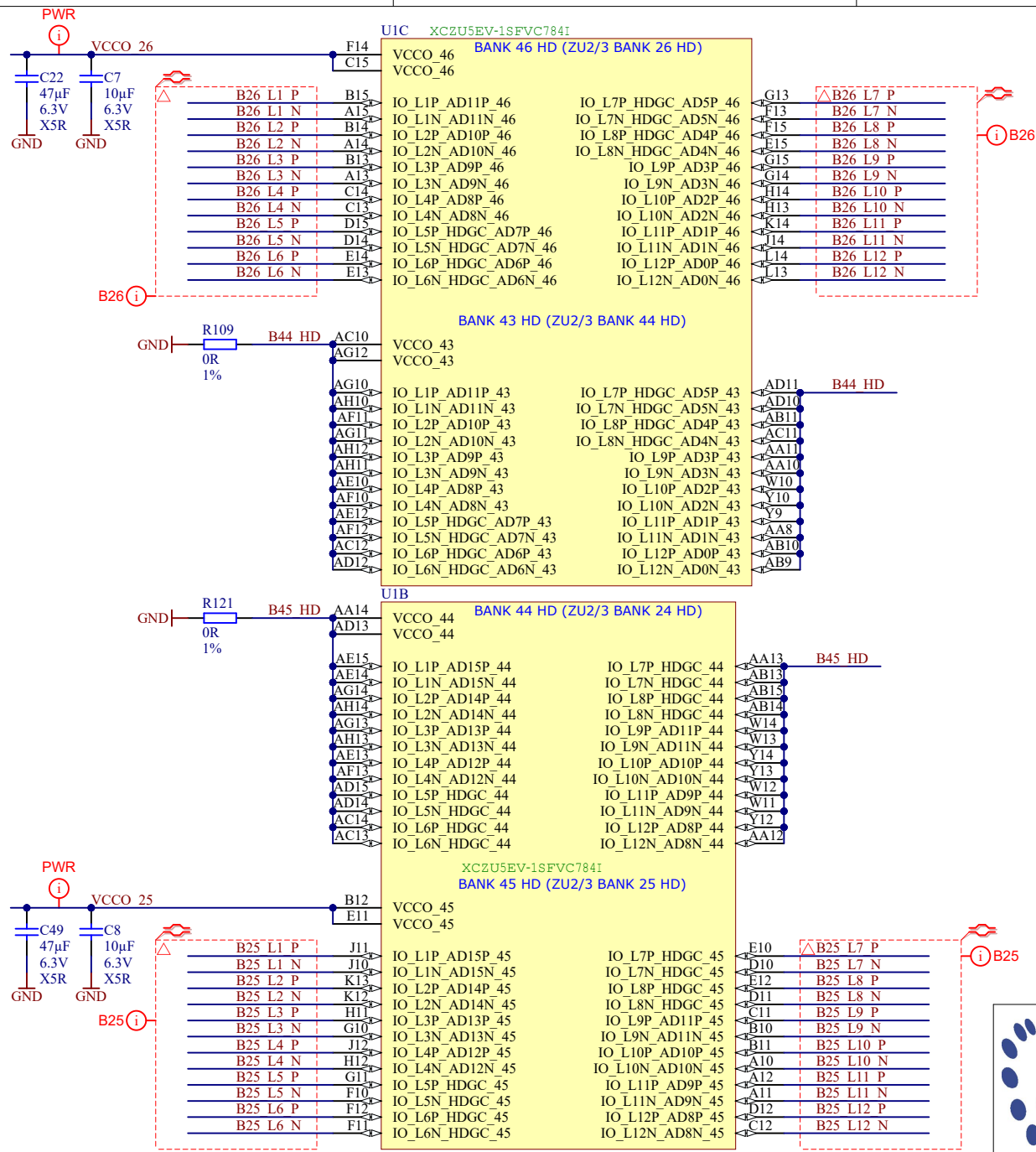
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Date: 08.03.2022	Copyright: Trenz Electronic GmbH	Page 9 of 30
Filename: J4.SchDoc		

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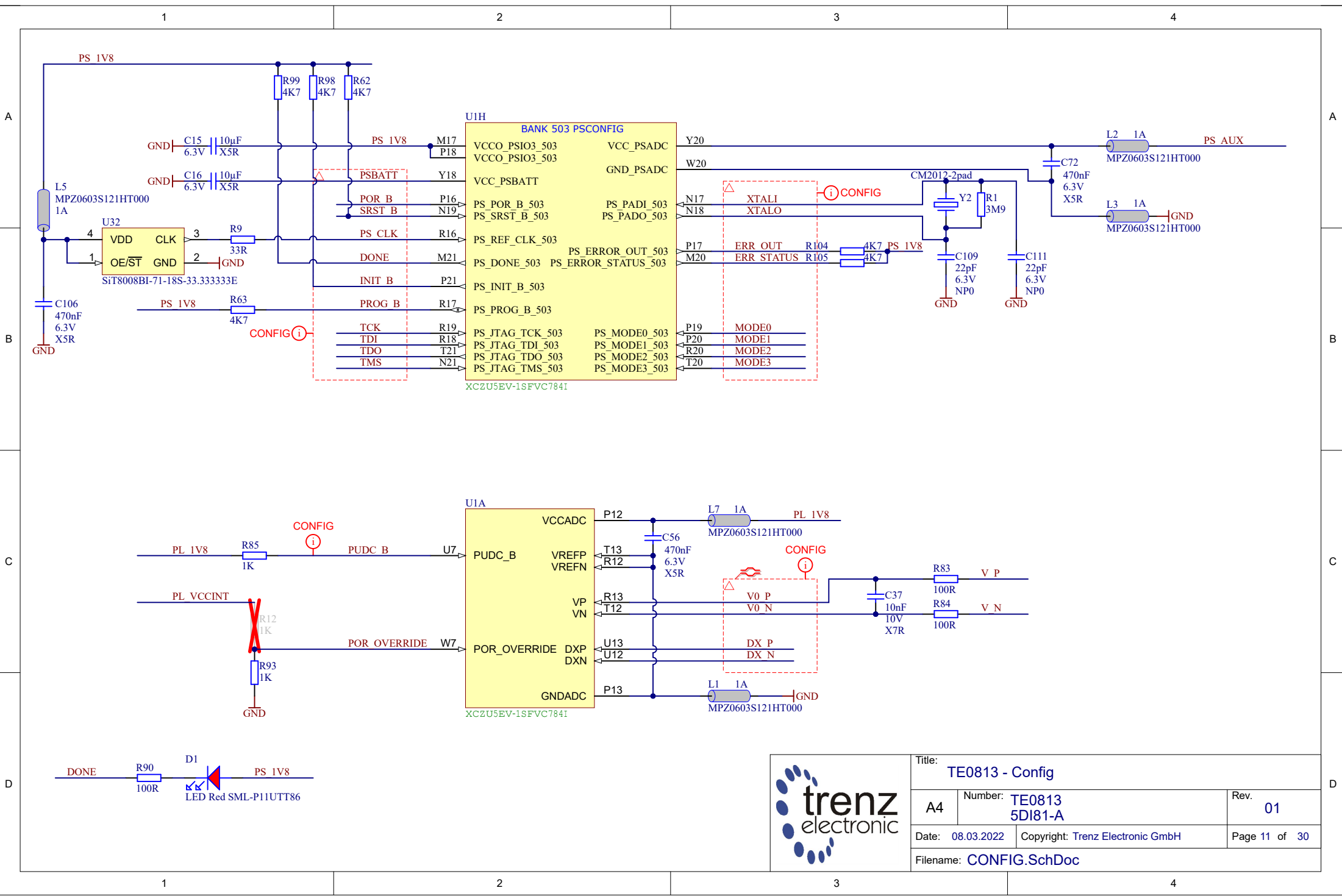
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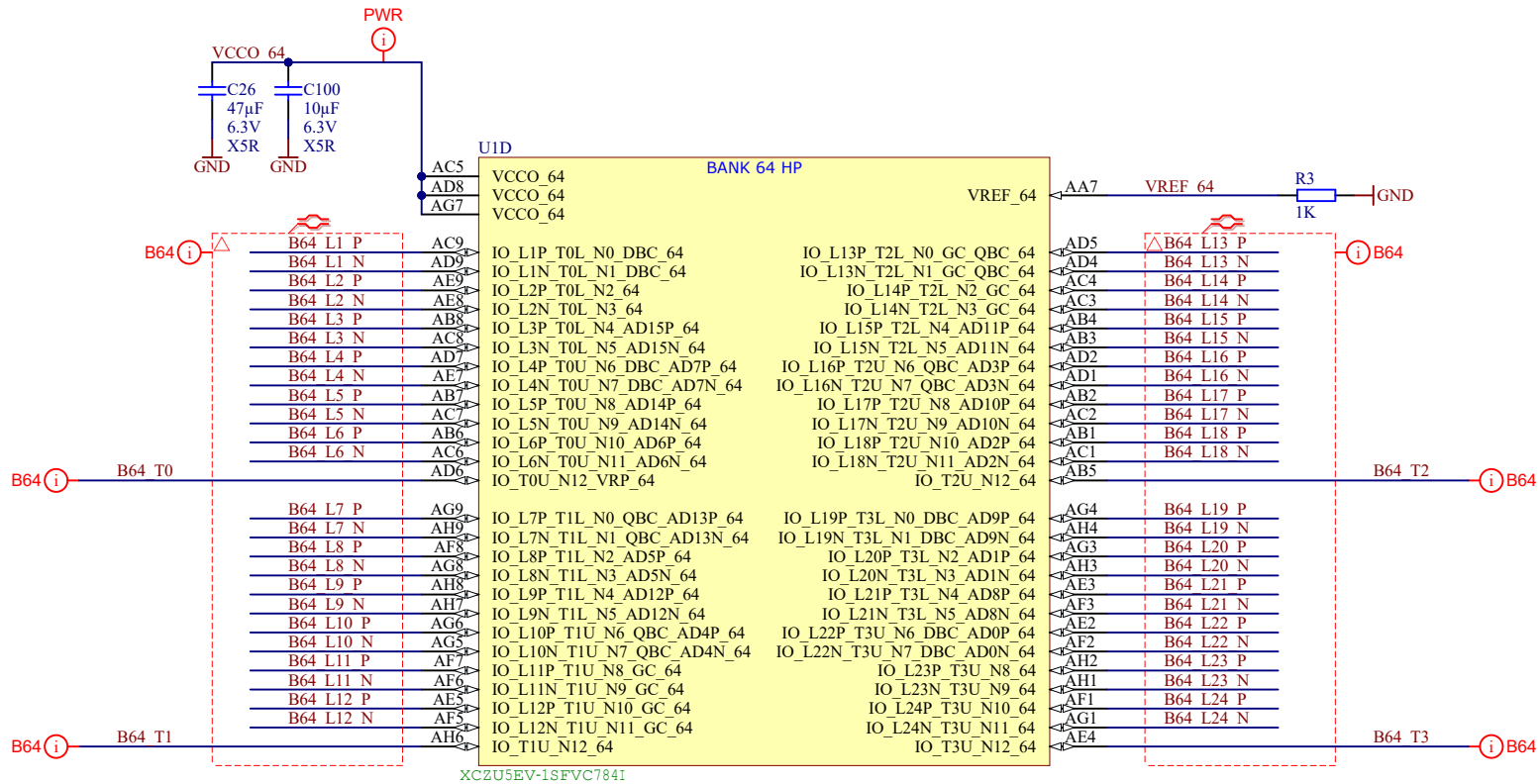
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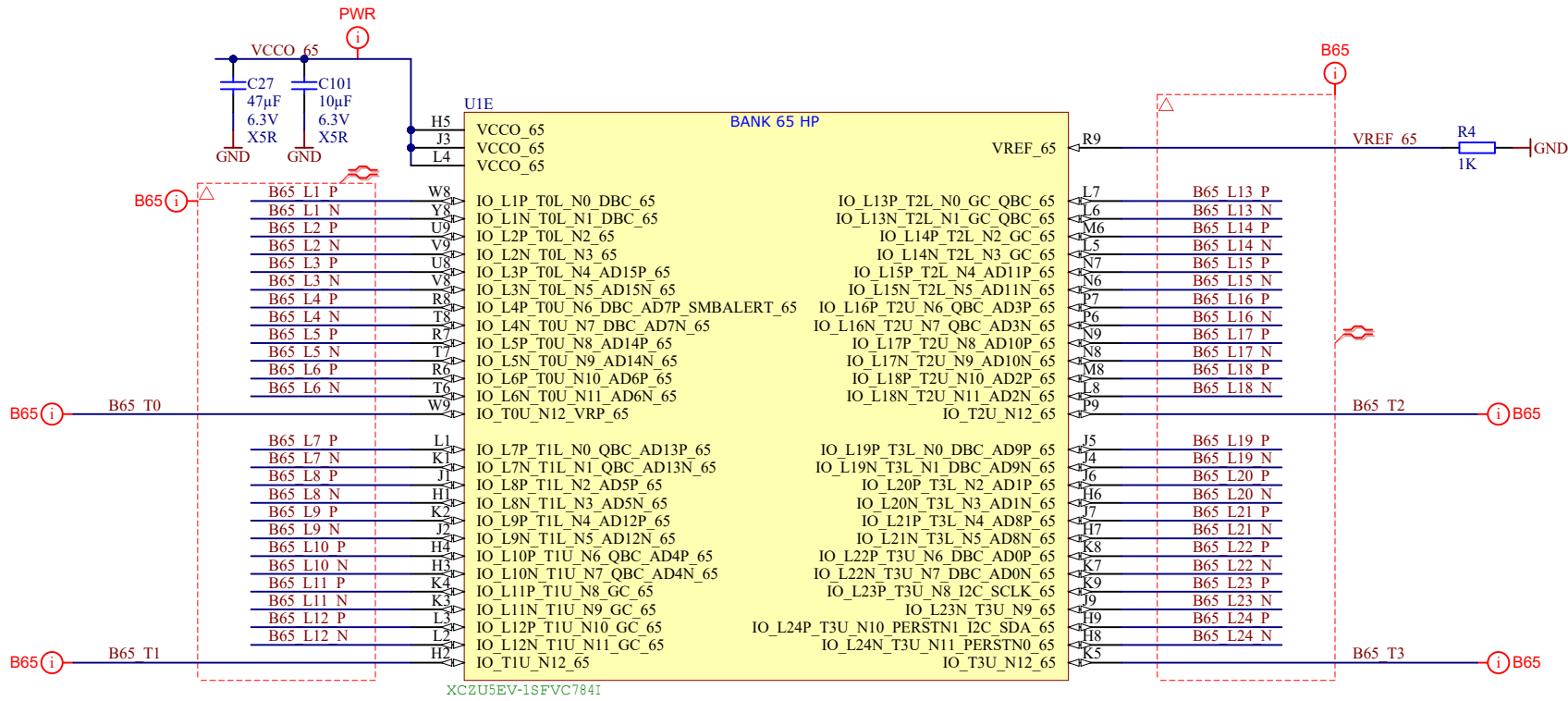
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Date: 08.03.2022	Copyright: Trenz Electronic GmbH	Page 10 of 30
Filename: B_HD.SchDoc		



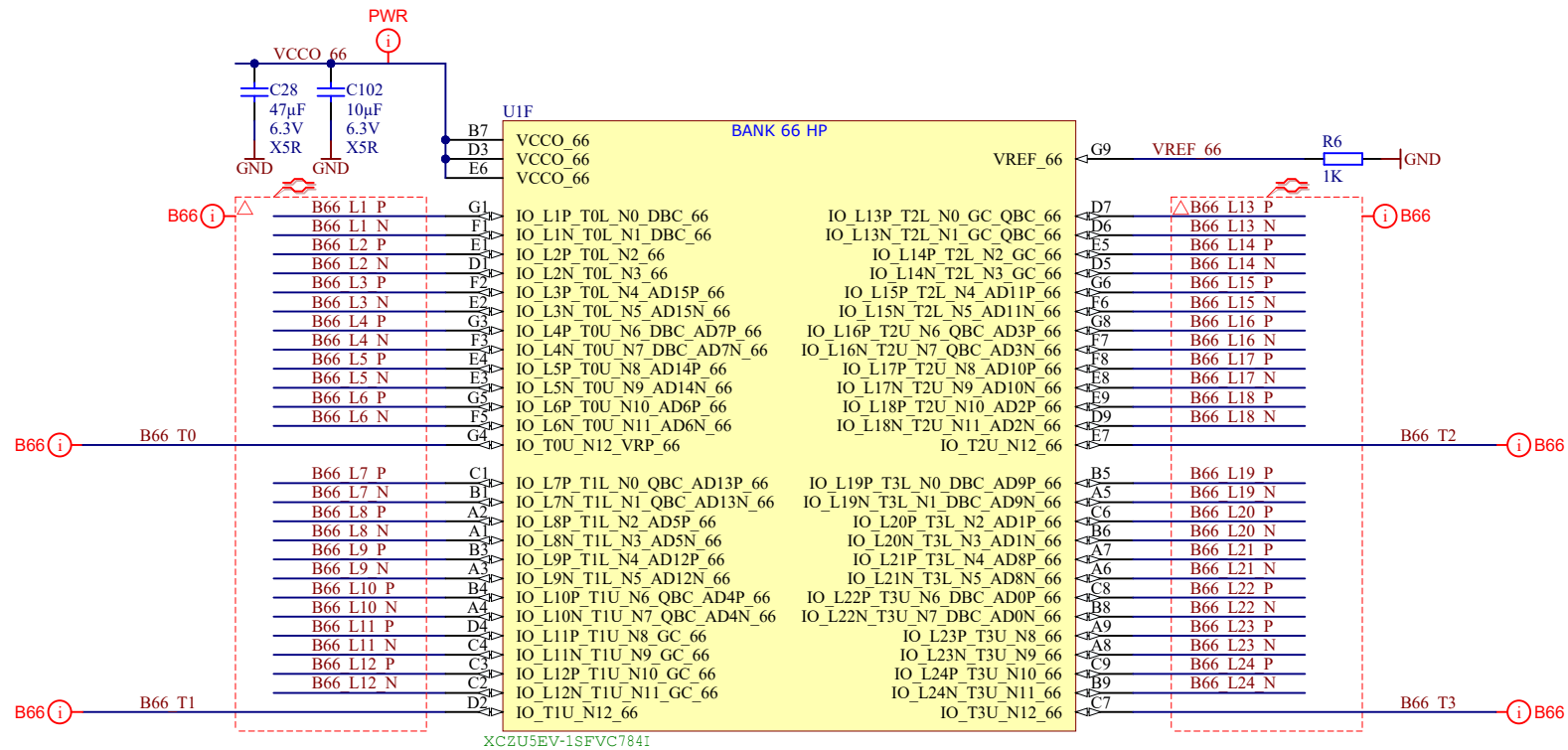
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Date: 08.03.2022	Copyright: Trenz Electronic GmbH	Page 11 of 30
Filename: CONFIG.SchDoc		



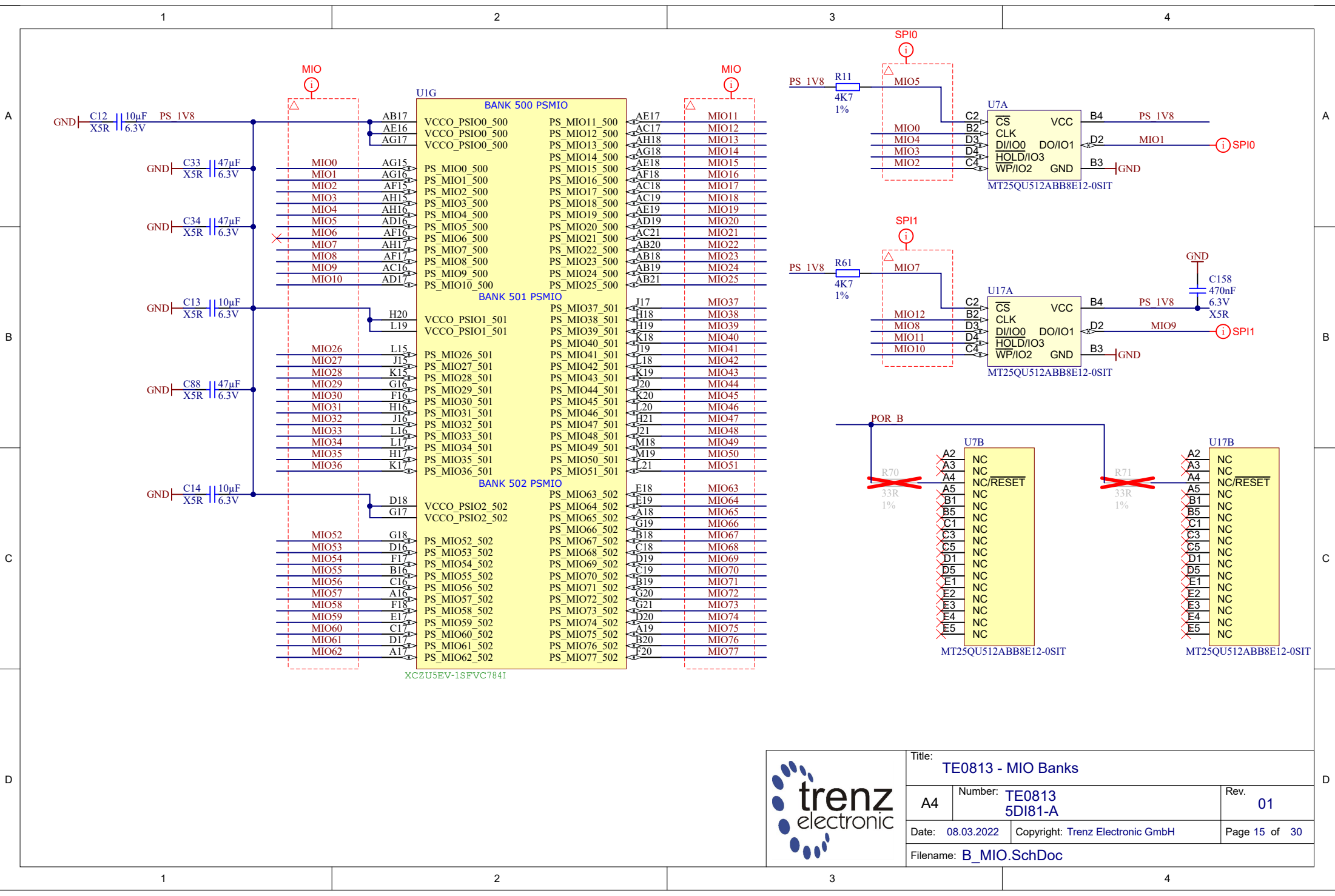
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A4	Number: TE0813 5DI81-A	Rev. 01
Date: 08.03.2022	Copyright: Trenz Electronic GmbH	Page 12 of 30
Filename: B64.SchDoc		



Title: TE0813 - B65		
A4	Number: TE0813 5DI81-A	Rev. 01
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Filename: B65.SchDoc		



Title: TE0813 - B66		
A4	Number: TE0813 5DI81-A	Rev. 01
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Filename: B66.SchDoc		



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Title: **TE0813 - MIO Banks**

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Filename: B_MIO.SchDoc		

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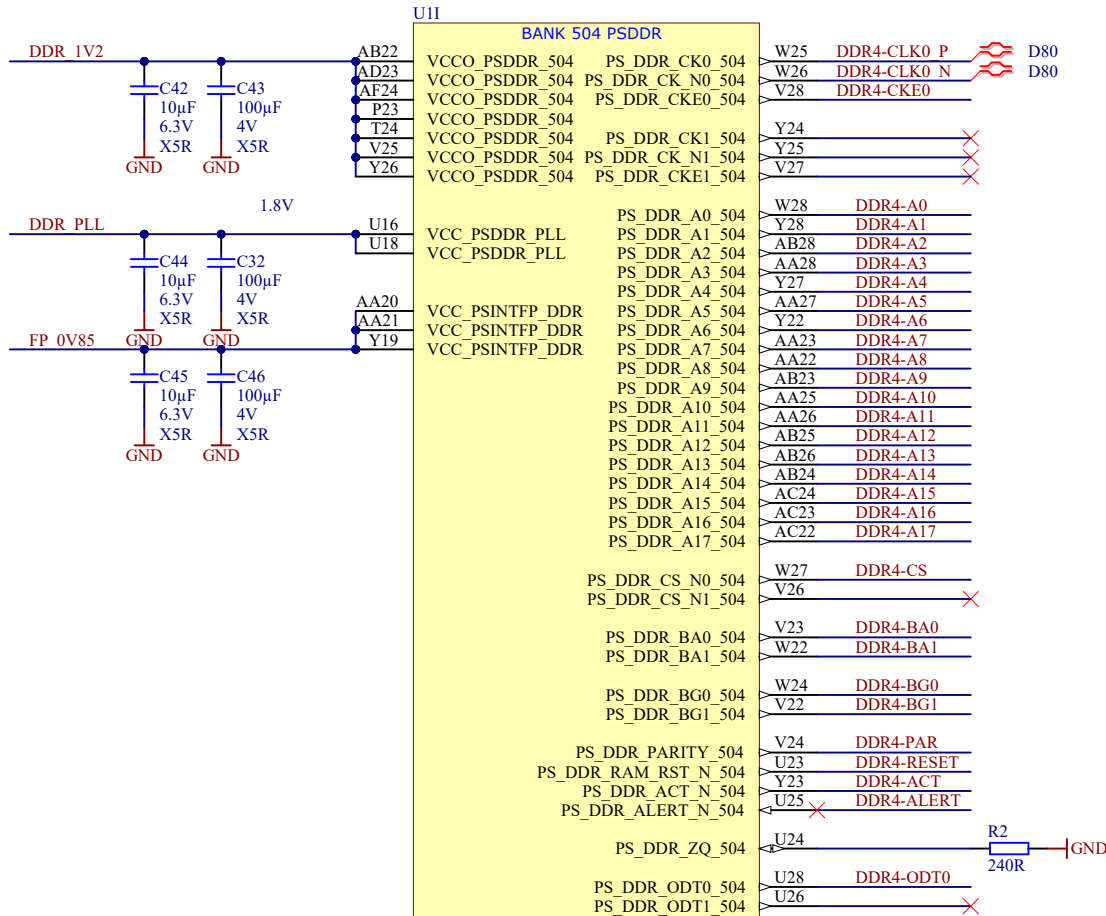
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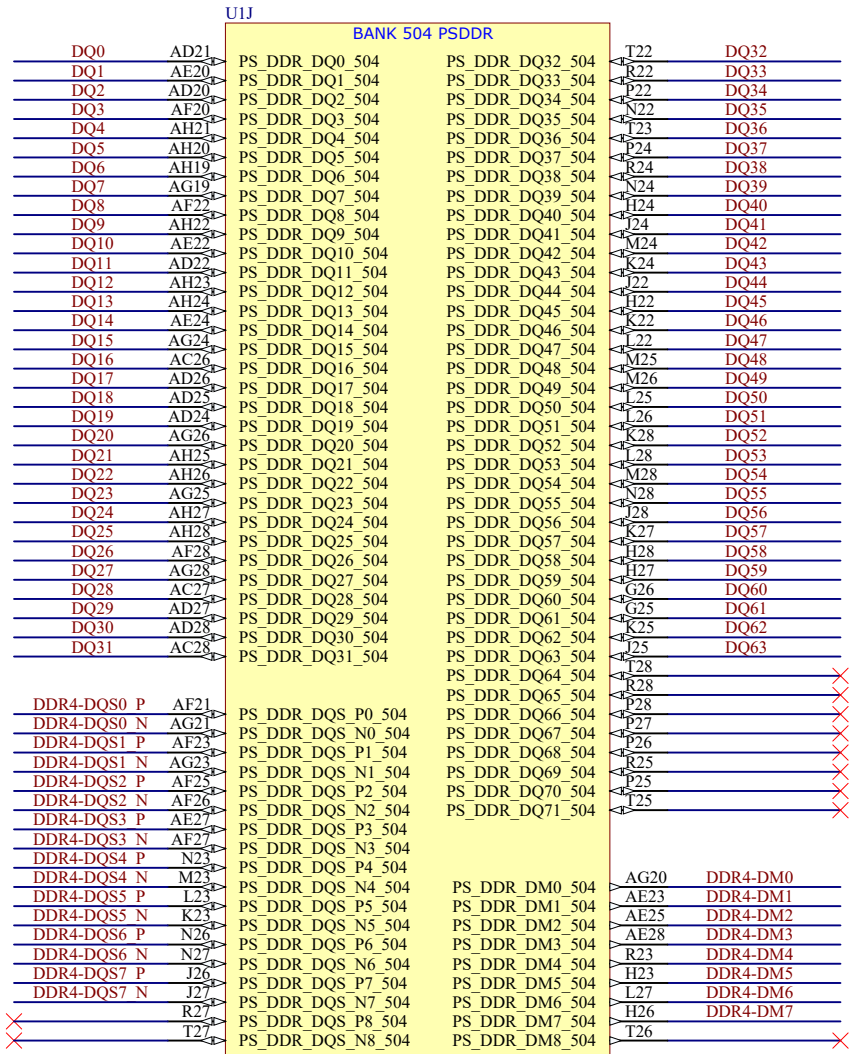
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XC2U5EV-1SFVC784I



XC2U5EV-1SFVC784I



Title: TE0813 - PS_DDR		
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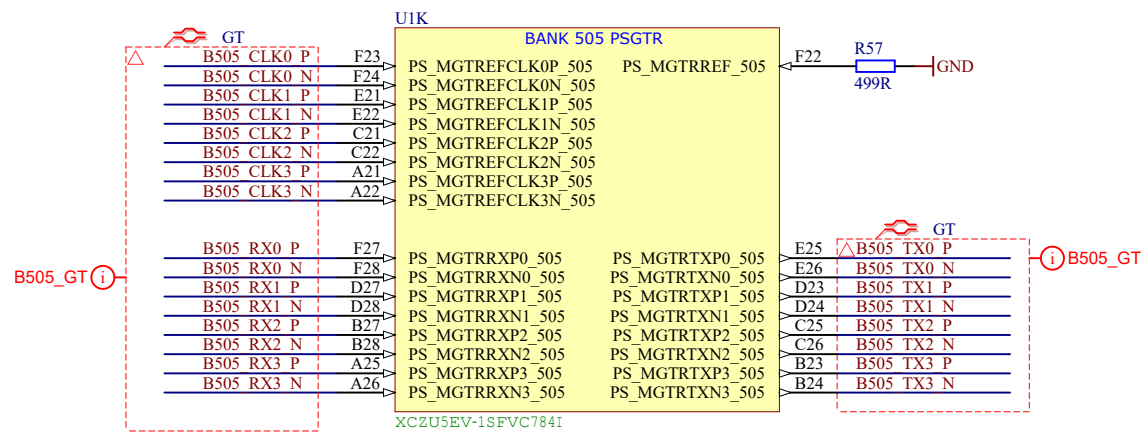
B

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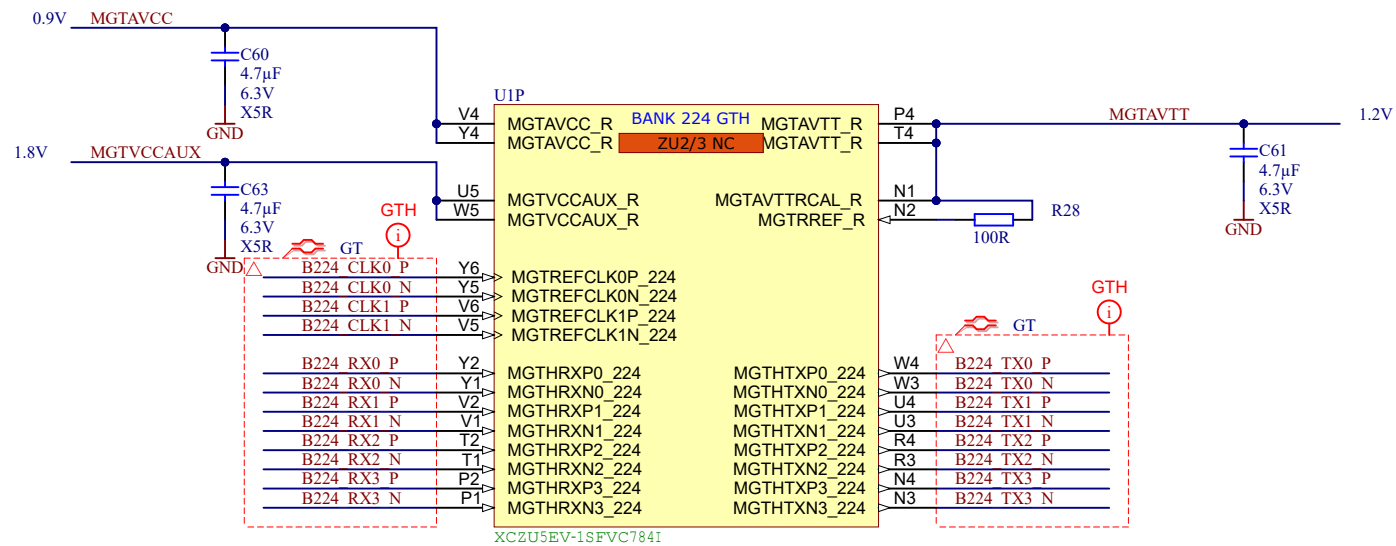
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A4	Number: TE0813 5DI81-A	Rev. 01
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Filename: B_PS_GT.SchDoc		

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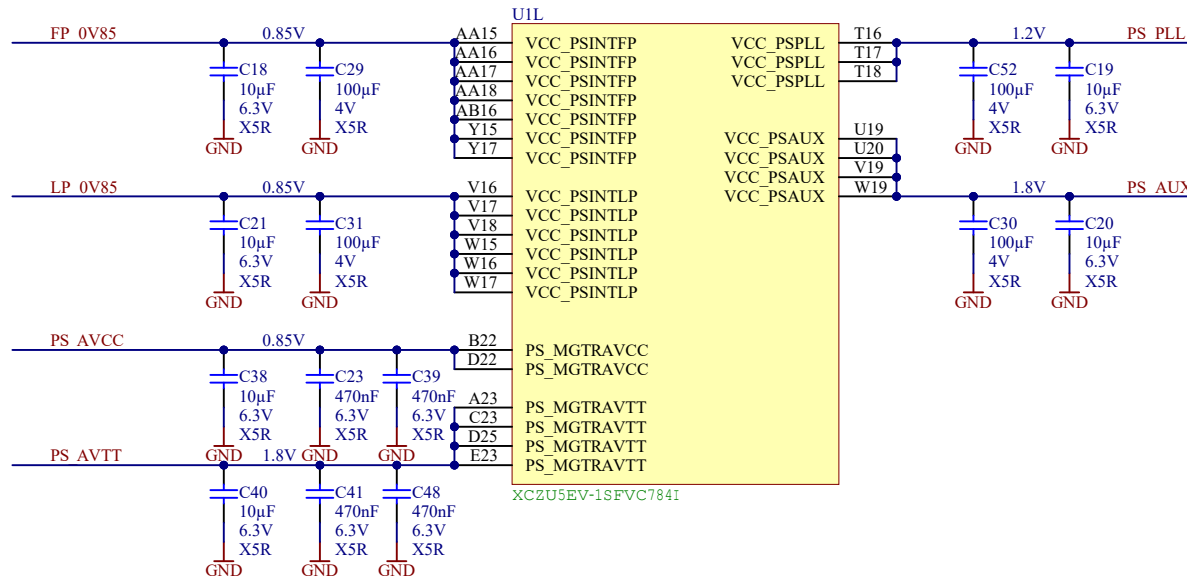
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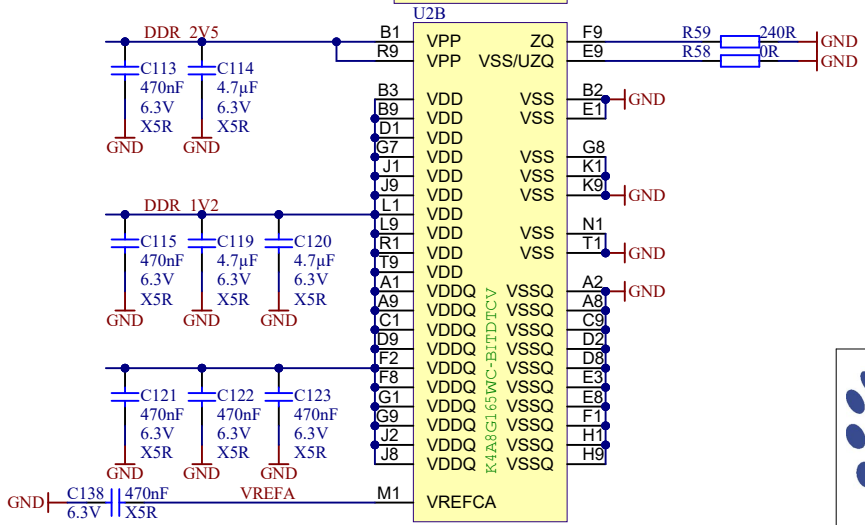
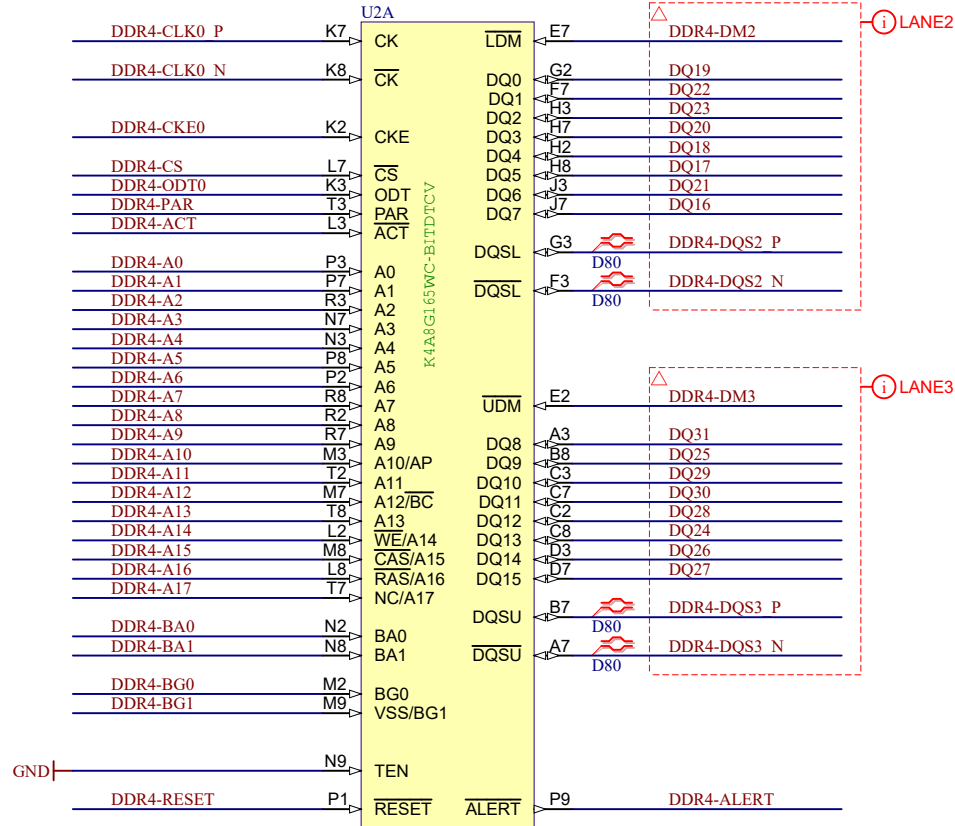
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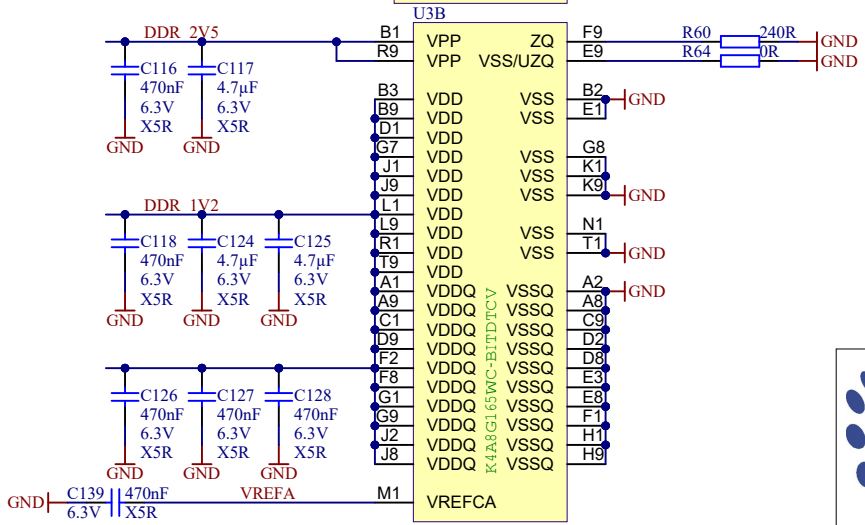
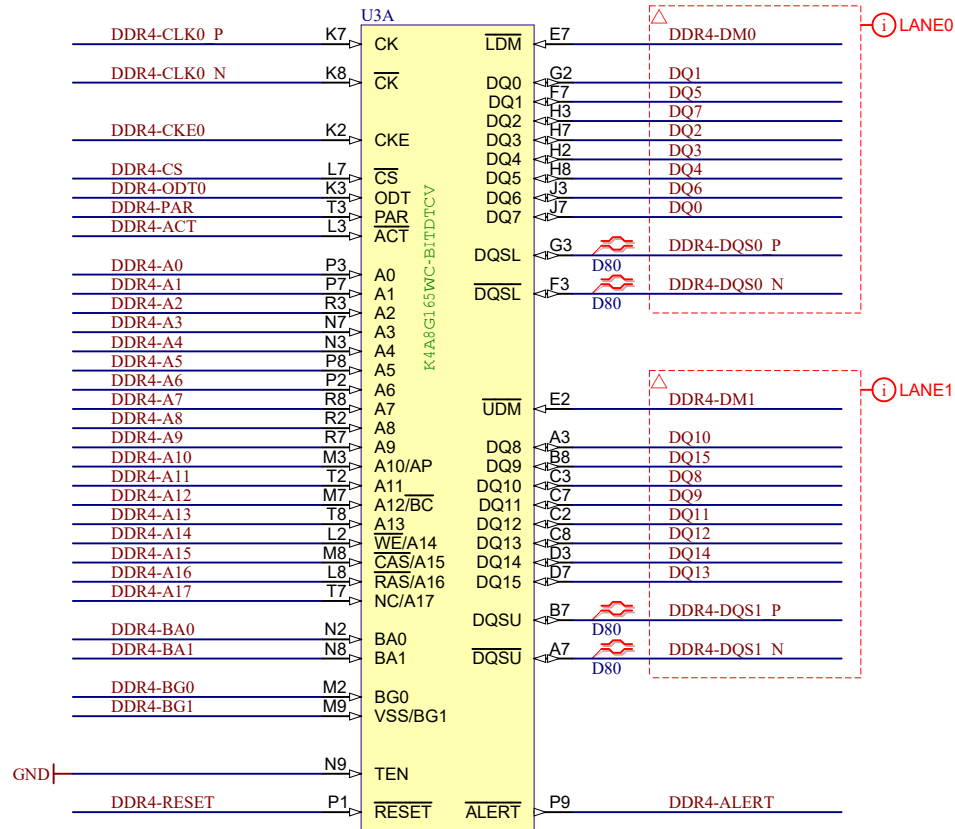

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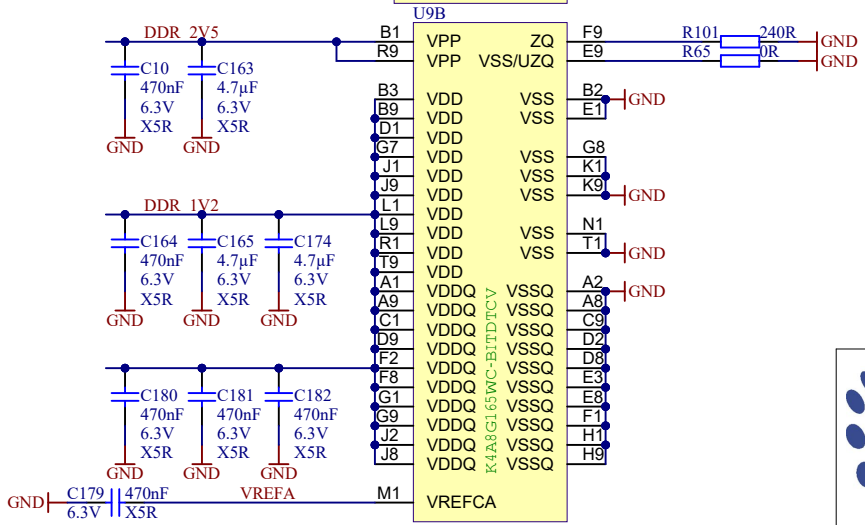
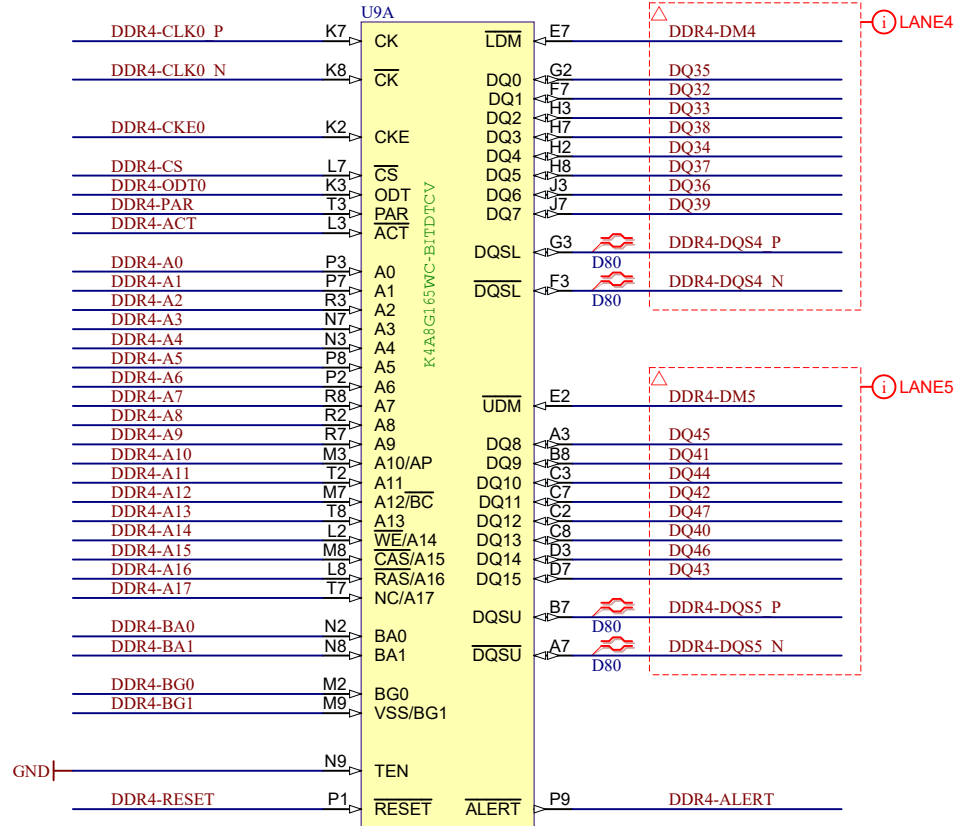
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	Filename: ZU_PS_POWER.SchDoc	
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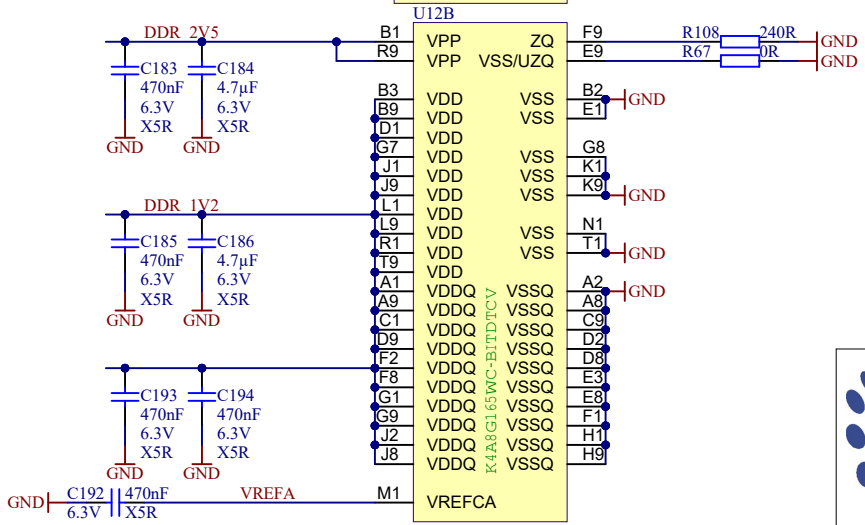
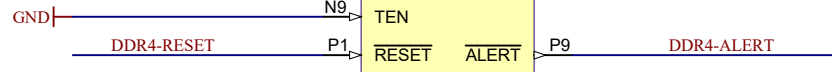
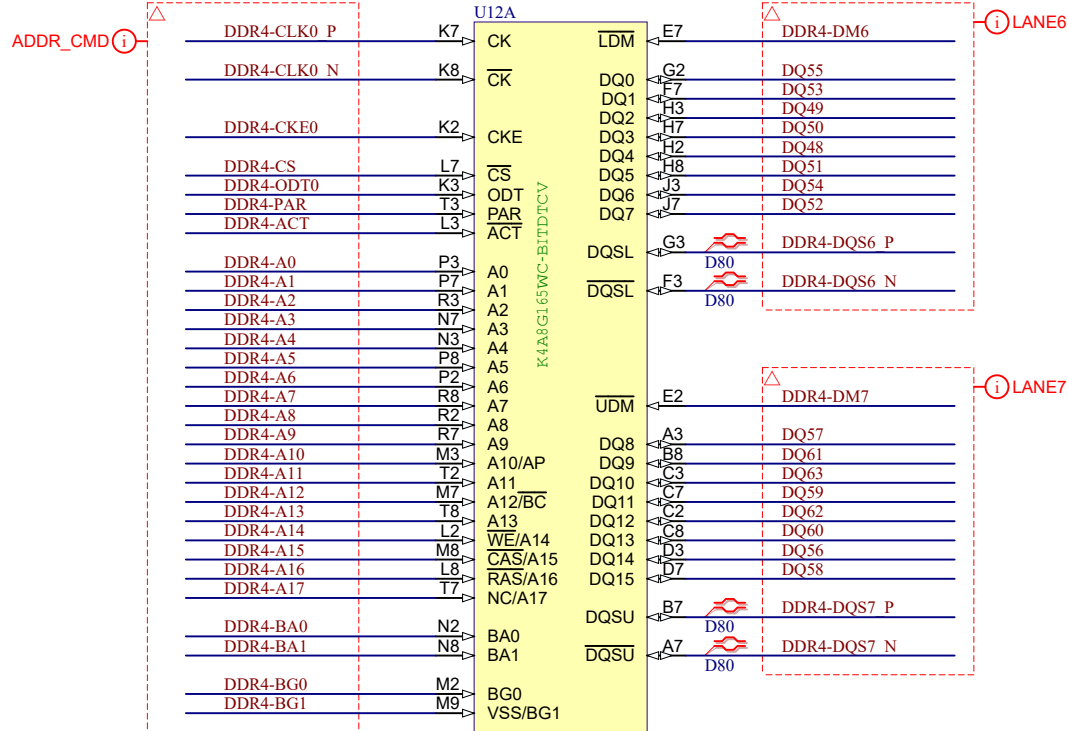

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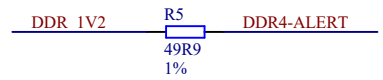
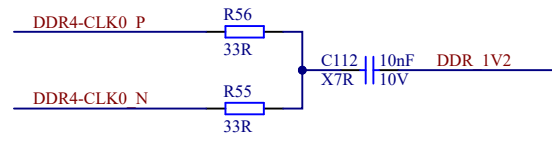
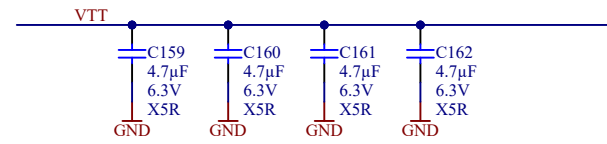
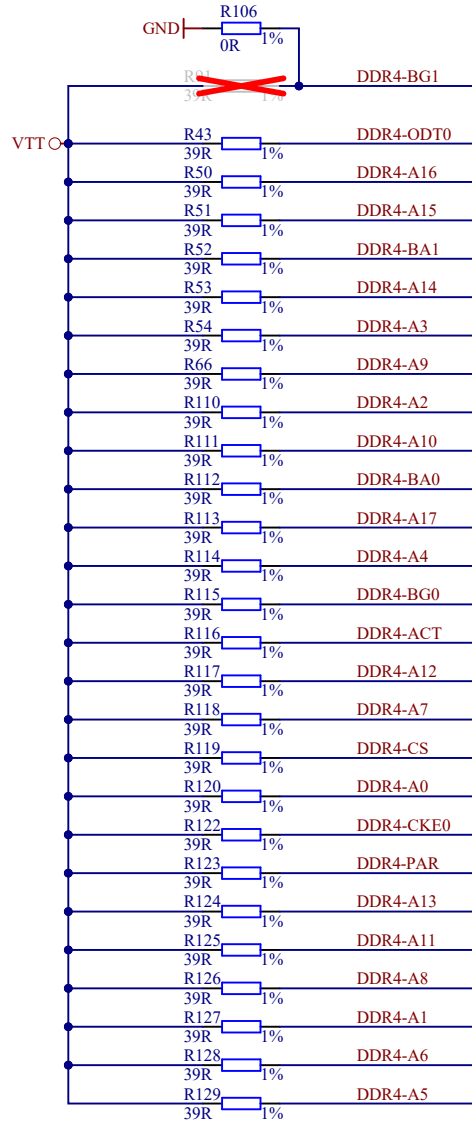
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Filename: DDR4-RAM_2.SchDoc		



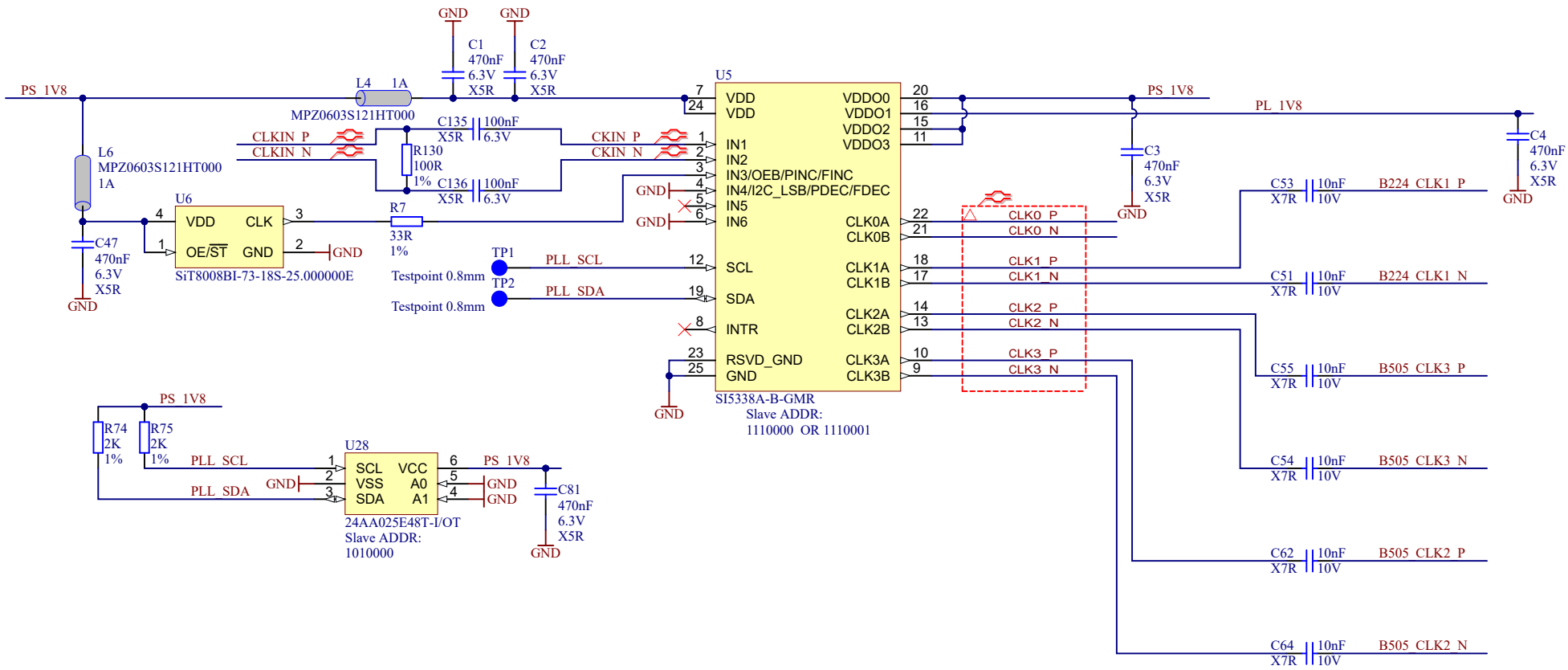
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Filename: DDR4-RAM_3.SchDoc		





Title: TE0813 - DDR4_4_RAM		
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Filename: DDR4-RAM_4.SchDoc		

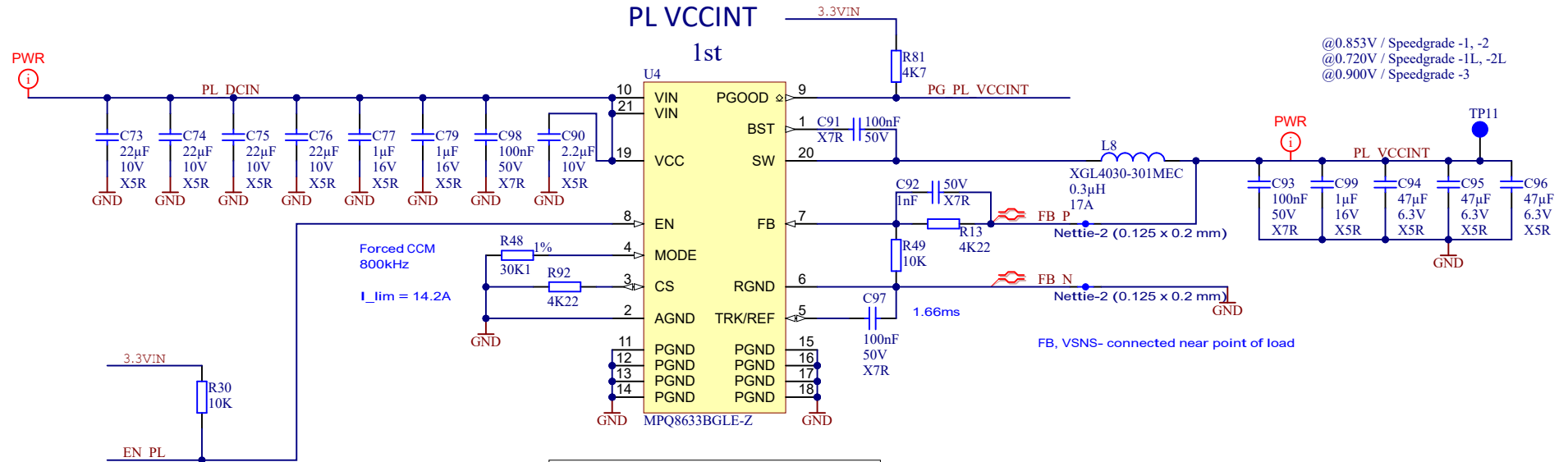


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Filename: Clock.SchDoc				

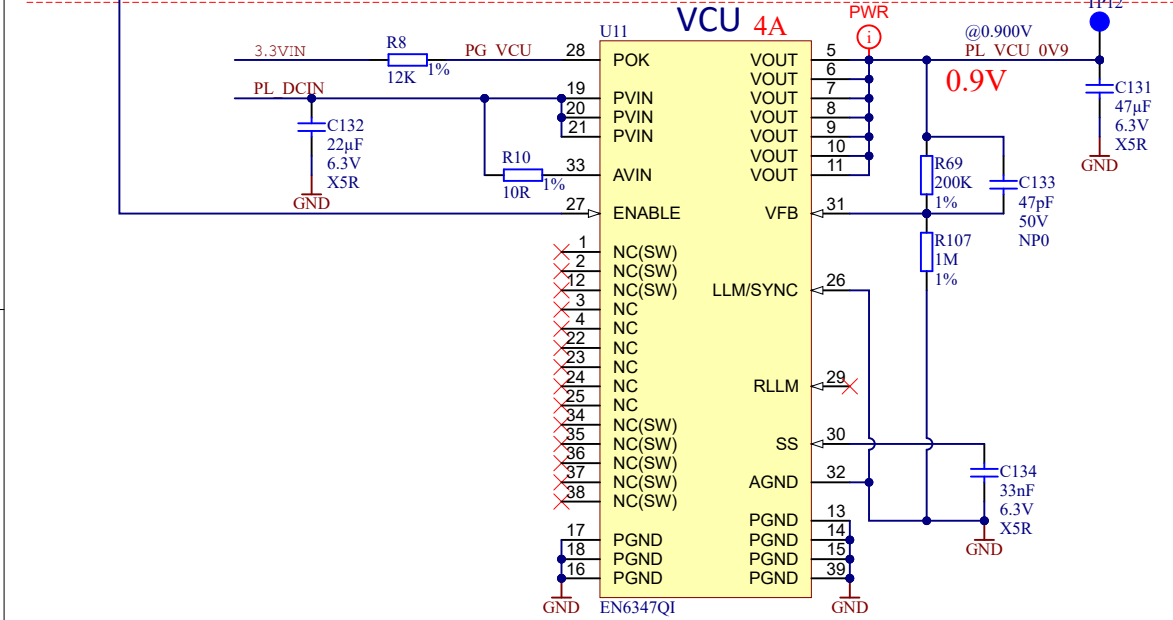
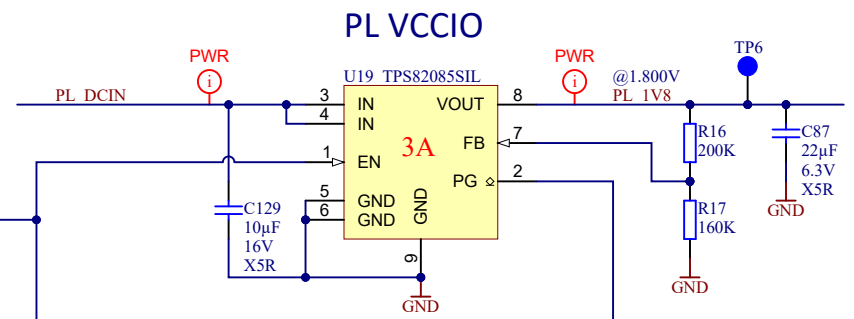
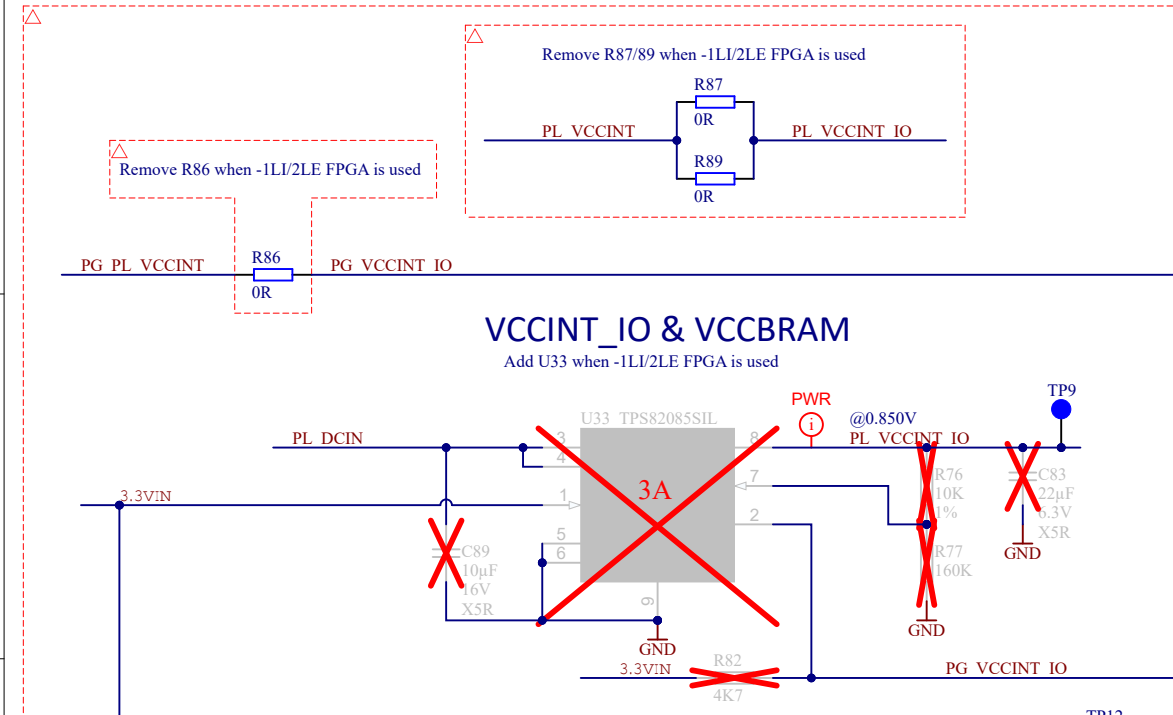
U4 can be TPS548A28RWR or MPQ8633BGLE-Z which is up to Trenz Electronic GmbH.




FPGA Speed grade:		
-1L / -2LE	R13 - 2K, R49 - 10K	PL_VCCINT = 0.720V
-1 / -2	R13 - 4K22, R49 - 10K	PL_VCCINT = 0.853V
-3E	R13 - 10K, R49 - 20K	PL_VCCINT = 0.900V

U4 pin compatible with
 -- TPS548B28 (20A)
 -- TPS548A28 (15A)
 -- TPS54JA20 (12A)

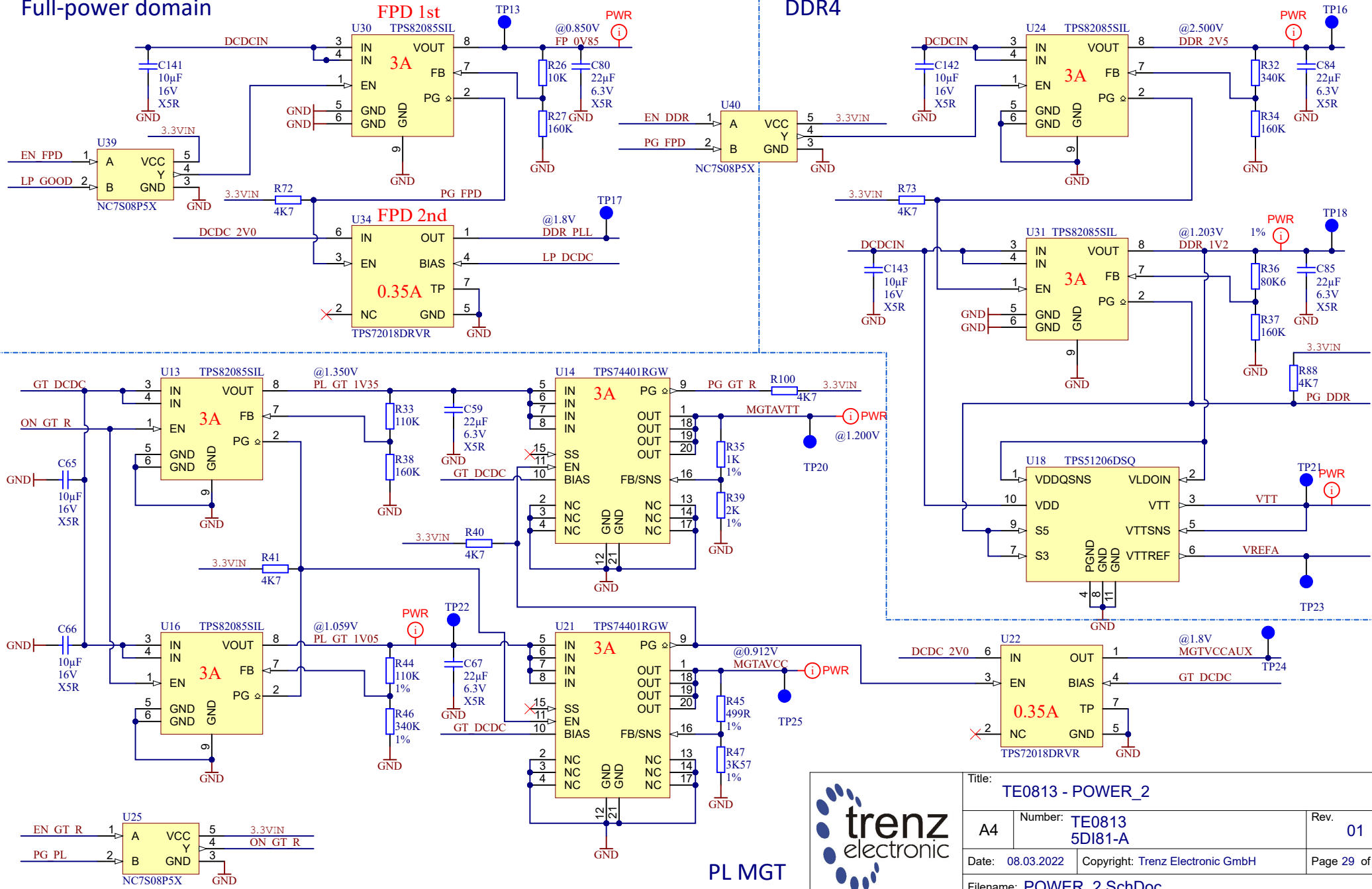
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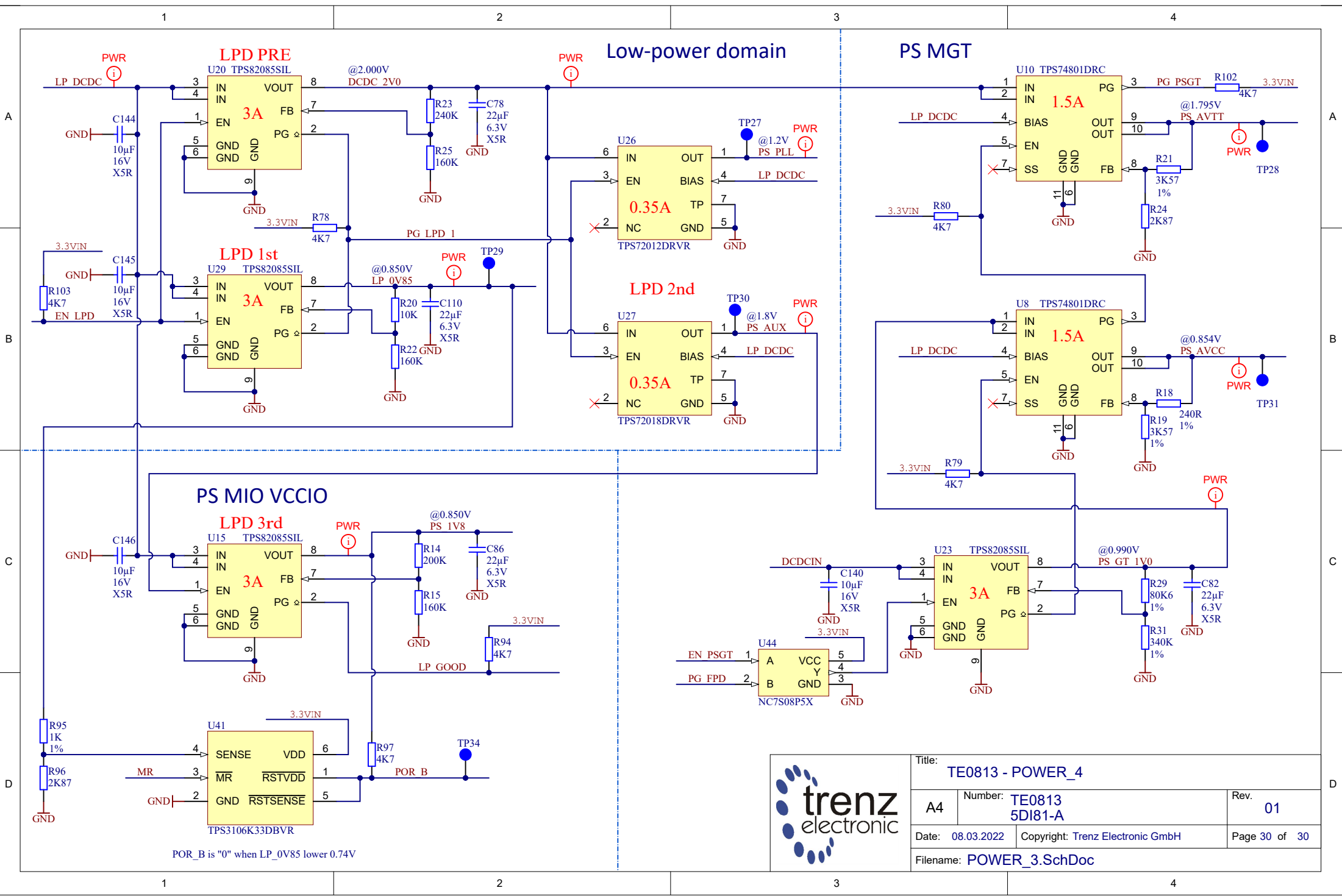
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Full-power domain

DDR4



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