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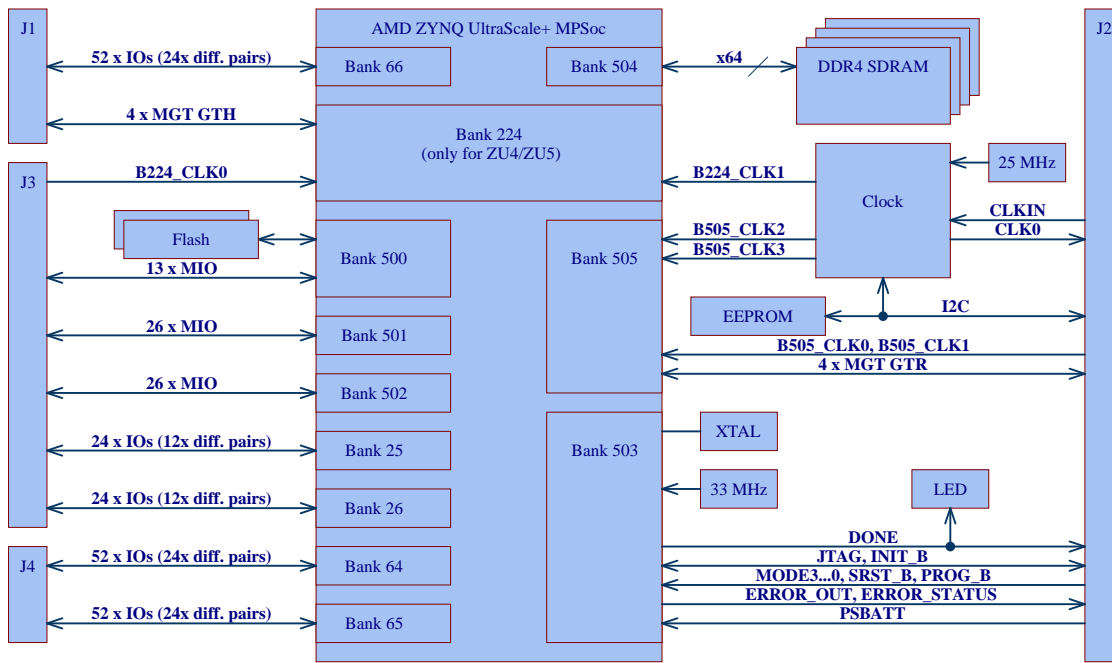
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Schematics and other handouts serve for informational purposes only!

Drawn by	ED
Checked by	MR
Assembly variant	SDE81-A
Created by	ED
Modified by	ED
Modified at	2023-05-17



Title: TE0813 - Legal Notices		
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## Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3VIN	IN	3.3V	+/- 5 %	Micromodule Power	Management voltage rail, supplied by power rail
PL_DCIN	IN	3.3V	+/- 5 %	Micromodule Power	Programmable Logic, supplied by power rail
LP_DCDC	IN	3.3V	+/- 3 %	Micromodule Power	Low-Power Domain, supplied by power rail
GT_DCDC	IN	3.3V	+/- 3 %	Micromodule Power	GTH Transceiver, supplied by power rail
DCDCIN	IN	3.3V	+/- 5 %	Micromodule Power	Full-Power Domain and GTR, supplied by power rail
VCCO_64	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 64	Supplied by external power rail via B2B connector
VCCO_65	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 65	Supplied by external power rail via B2B connector
VCCO_66	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 66	Supplied by external power rail via B2B connector
VCCO_25	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 25	Supplied by external power rail via B2B connector
VCCO_26	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 26	Supplied by external power rail via B2B connector
PSBATT	IN	1.2 V - 1.5 V	-	RTC / BBRAM	Supplied by external power rail via B2B connector
PL_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Micromodule: Programmable Logic
PS_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Micromodule: Processing System
DDR_1V2	OUT	1.2 V	+/- 3 %	Power for Carrier	Micromodule: PS DDR I/O Supply


## I2C Address:

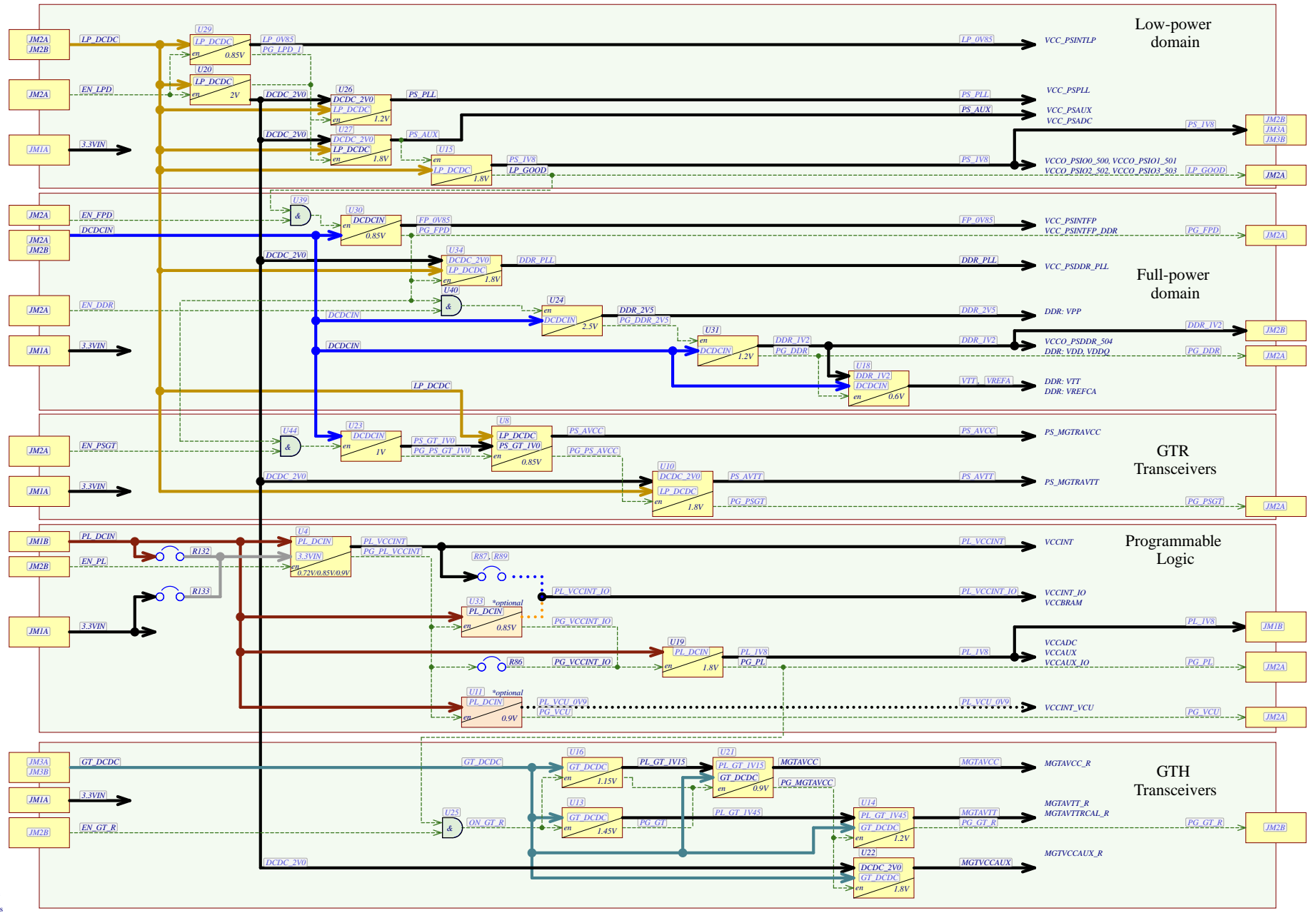
Device	I2C ADDR	Note
PLL <a href="#">U5</a>	0x70	-
EEPROM <a href="#">U28</a>	0x50	-



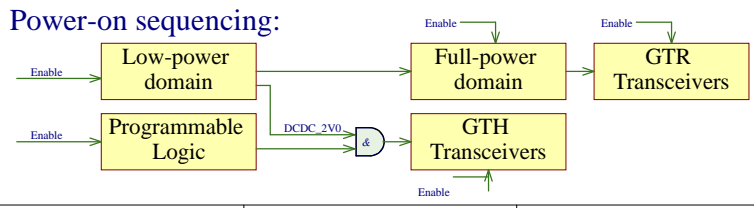
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REV	DATE	Description	
-01	2021-05	Initial revision	VT
	2022-03	Added Table with Supported Voltage Ranges	
	2022-05	Changed DCDC U4 TPS548A28 to MPQ8633BGL-E Changed C92 100nF to 1nF	
	2022-11	Added additional Info about Voltage Range	
-02	2023-07	<p>1. Change DCDC U11 from EN6347QI to MPM3860GQW-Z and adapted according circuits.</p> <p>2. Connected DDR4-TEN signals together for U2, U3, U9, and U12 and pulled them low via 499 Ohm resistor R131. Added a testpoint TP3 for DDR4-TEN.</p> <p>3. Changed voltage rail from 1.35 V to 1.45 V via adapting voltage divider resistors R33 and R38 and changed according voltage rail name PL_GT_1V35 to PL_GT_1V45.</p> <p>4. Changed voltage rail from 1.05 V to 1.15 V via adaption voltage divider resistors R44 and R46 and changed according rail name PL_GT_1V05 to PL_GT_1V15.</p> <p>5. Added diode D2 between U41 pin 3 net MR and voltage rail 3.3VIN.</p> <p>6. Connected enable signal for U11 and U33 from "3.3VIN" to "PG_PL_VCCINT".</p> <p>7. Added capacitors C137, C147, and C148 for VTT voltage rail.</p> <p>8. Added resistors R132 (default: not fitted) and R133 to supply U4 VCC either from "PL_DCCIN" or from "3.3VIN".</p> <p>9. Change resistor R92 from 4.22 kOhm to 9.09 kOhm to set current limit to nearly 14.5 A for U4.</p> <p>10. Added remote sense option:</p> <p>10.1 R134 for U30</p> <p>10.2 R135 for U29</p> <p>10.3 R136 for U31</p> <p>11. Added decoupling capacitors:</p> <p>11.1 C210 and C211 for U5.</p> <p>11.2 C190 for U7.</p> <p>11.3 C198, C199, and C213 for U8.</p> <p>11.4 C153, C170...172 for U9</p> <p>11.5 C196 C197, and C212 for U10.</p> <p>11.6 C156 and C157 for U12</p> <p>11.7 C207 and C208 for U14.</p> <p>11.8 C189 for U17.</p> <p>11.9 C149...152, C205, and C206 for U18</p> <p>11.10 C209 and C217 for U21.</p> <p>11.11 C214...216 for U22.</p> <p>11.12 C154 and C155 for U24</p> <p>11.13 C188 and C191 for U26.</p> <p>11.14 C187 and C195 for U27.</p> <p>11.15 C203 and C204 for U34.</p> <p>11.16 C201 for U39.</p> <p>11.17 C202 for U40.</p> <p>11.18 C178 for U41.</p> <p>11.19 C200 for U44.</p> <p>12. Added testpoints TP4, TP19, TP26.</p> <p>13. Added UKCA logo.</p> <p>14. Change 100 nF capacitors C135 and C136 from 6.3 V to 25 V for BOM optimization.</p>	ED

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- EN\_GT\_R Net name
- Power bus
- Control signal
- Power bus in FPGA speedgrade -1/-2/-3 assembly variants
- Power bus in FPGA speedgrade -1L/-2L assembly variants (low power)
- Optional power converter
- & Logic AND gate



Title: TE0813 - Power Diagram		
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Special notes:

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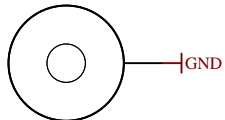
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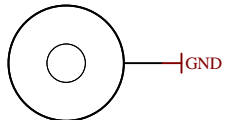
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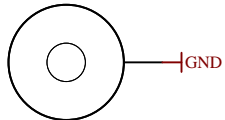
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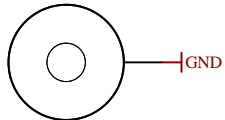
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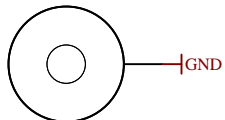
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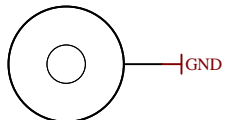
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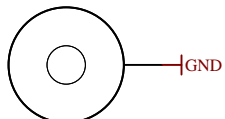
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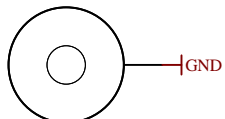
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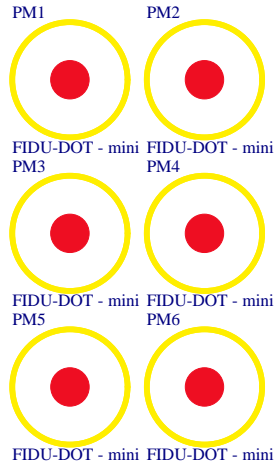
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



UKCA1

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

CE1

CE Logo on Top Overlay

CE-TOPOVERLAY

MECH1

TE Address Overlay

LOGO ADDRESS

LOGO1

TE Logo PRINT Layer

LOGO PRINT

Serial  
Serial  
Serialnumber 6,3 x 6.3mm



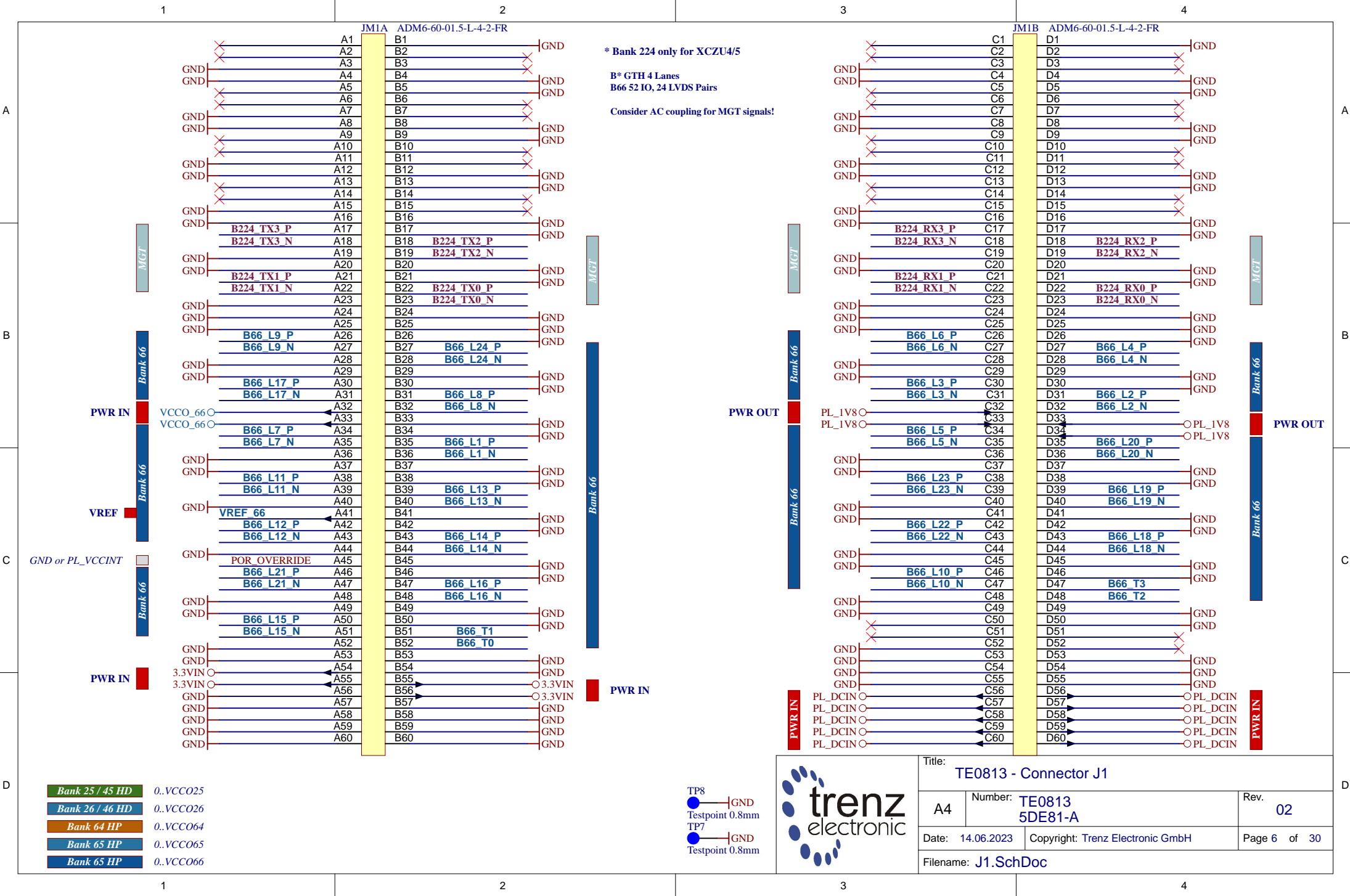
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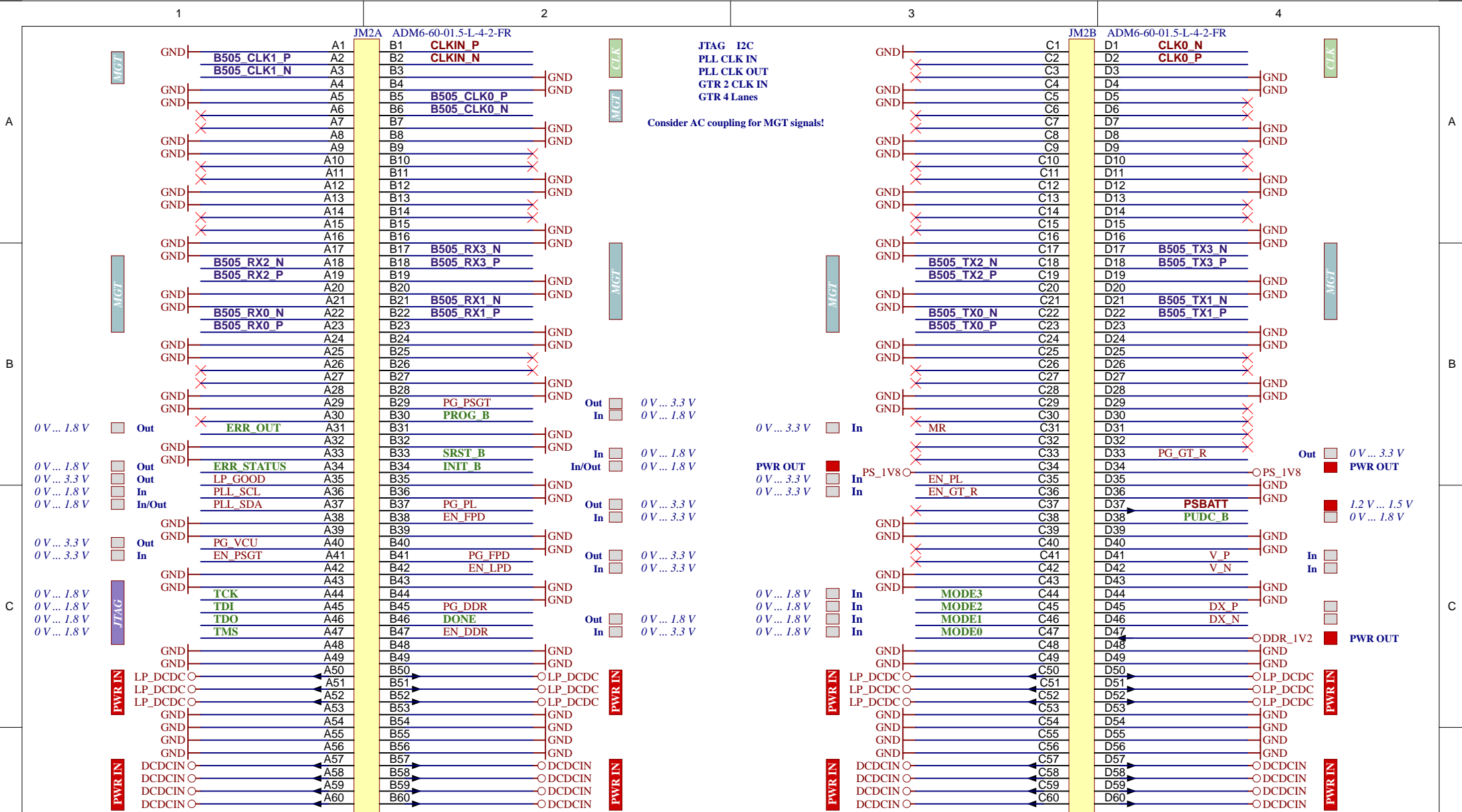
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\* Bank 224 only for XCZU4/5  
 B\* GTH 4 Lanes  
 B66 52 IO, 24 LVDS Pairs  
 Consider AC coupling for MGT signals!



Title: TE0813 - Connector J1		
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JTAG I2C  
PLL CLK IN  
PLL CLK OUT  
GTR 2 CLK IN  
GTR 4 Lanes

Consider AC coupling for MGT signals!

- Bank 25 / 45 HD 0..VCC025
- Bank 26 / 46 HD 0..VCC026
- Bank 64 HP 0..VCC064
- Bank 65 HP 0..VCC065
- Bank 65 HP 0..VCC066



Title: TE0813 - Connector J2		
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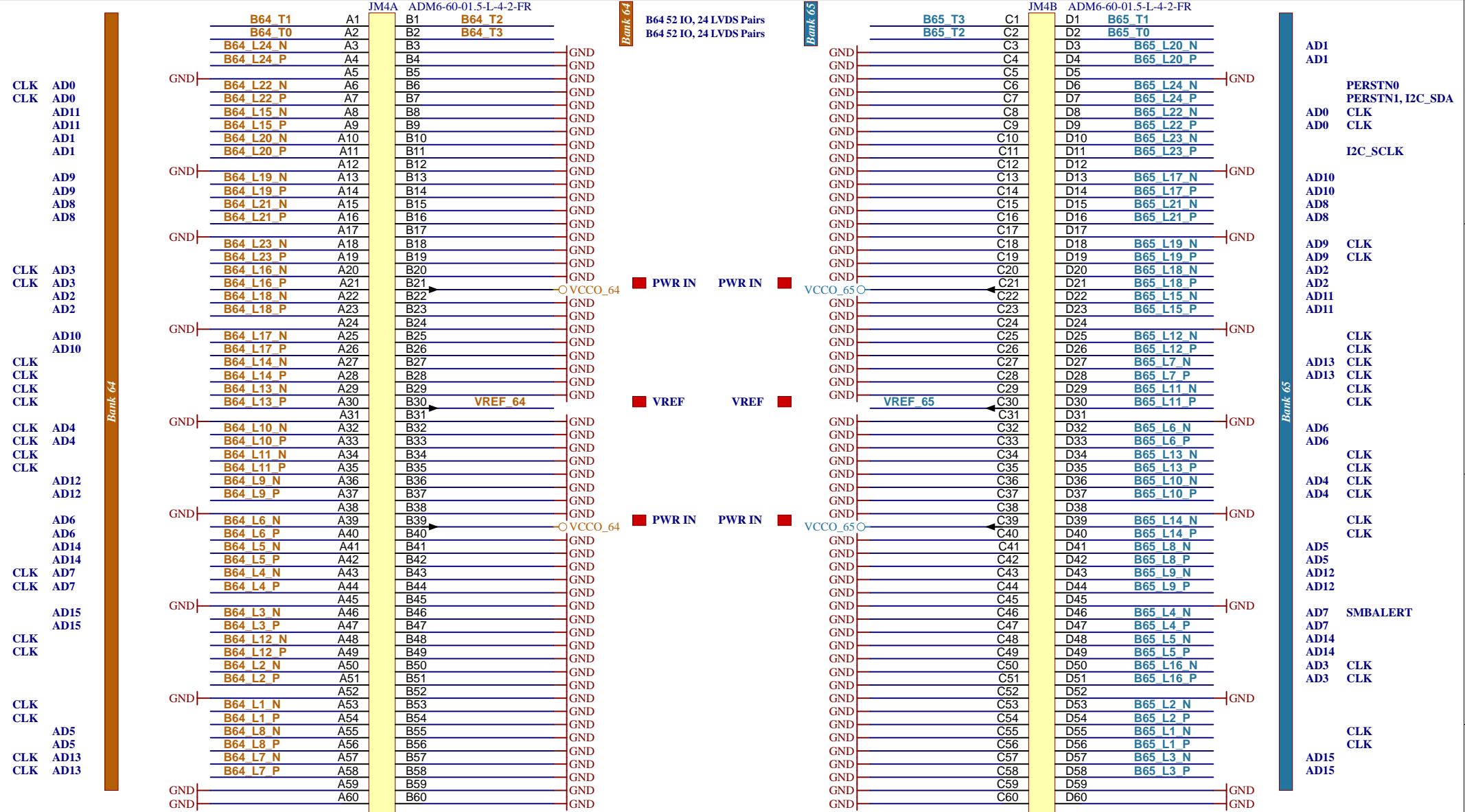
D

A

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- Bank 25 / 45 HD ..VCCO25
- Bank 26 / 46 HD ..VCCO26
- Bank 64 HP ..VCCO64
- Bank 65 HP ..VCCO65
- Bank 65 HP ..VCCO66



Title: TE0813 - Connector J4		
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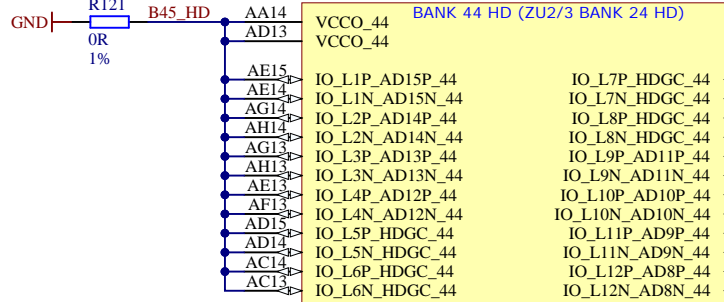
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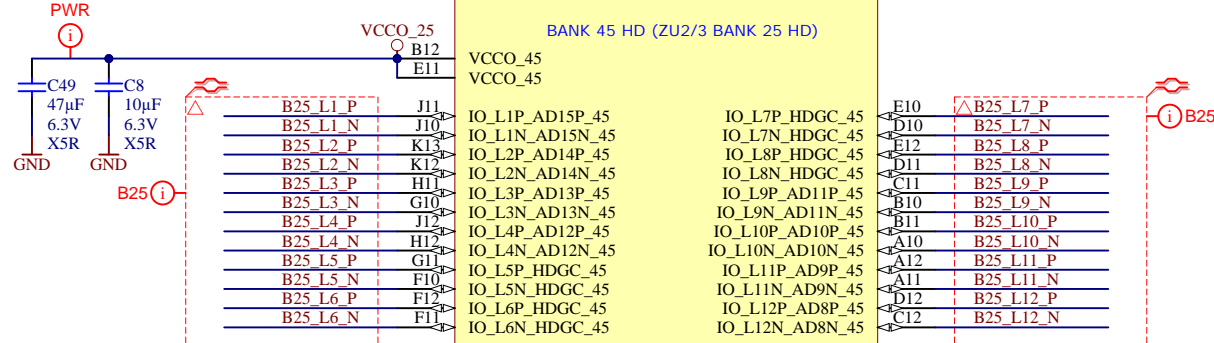
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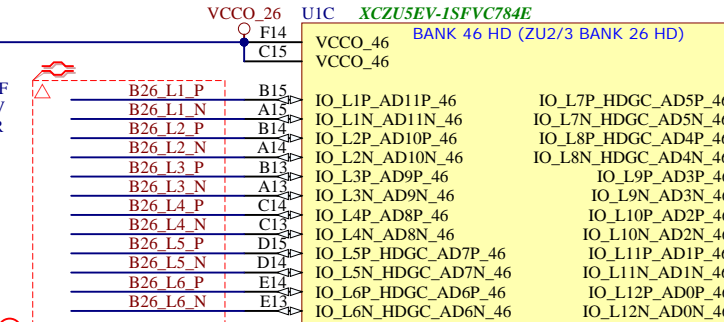
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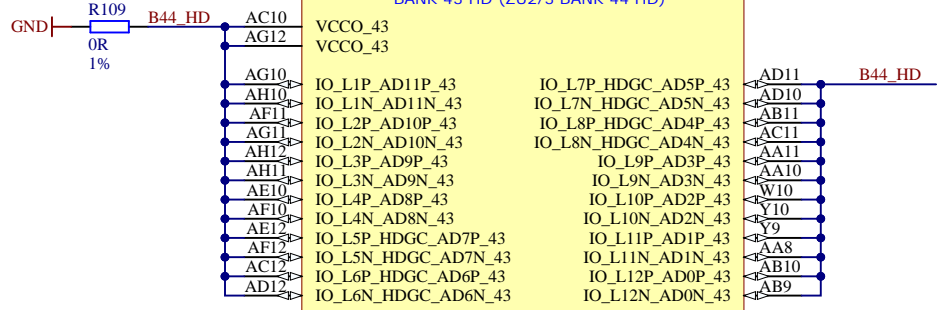
BANK 45 HD (ZU2/3 BANK 25 HD)



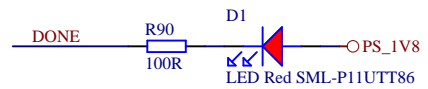
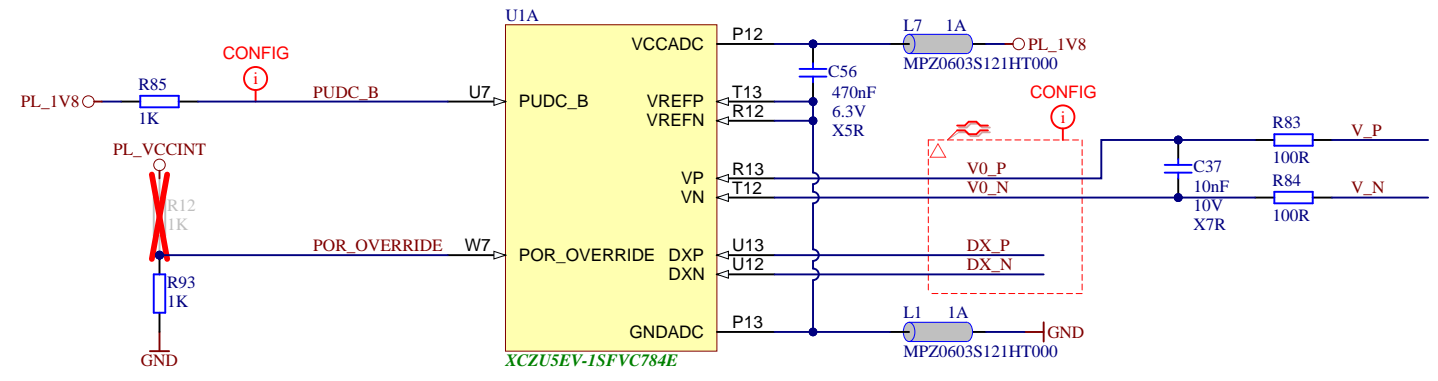
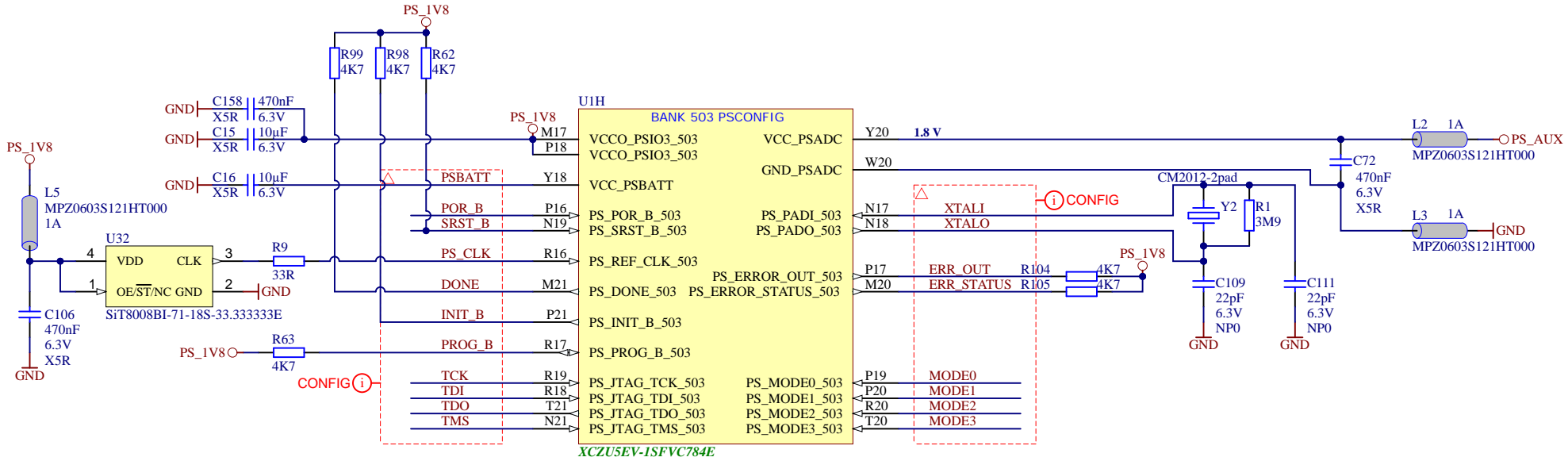
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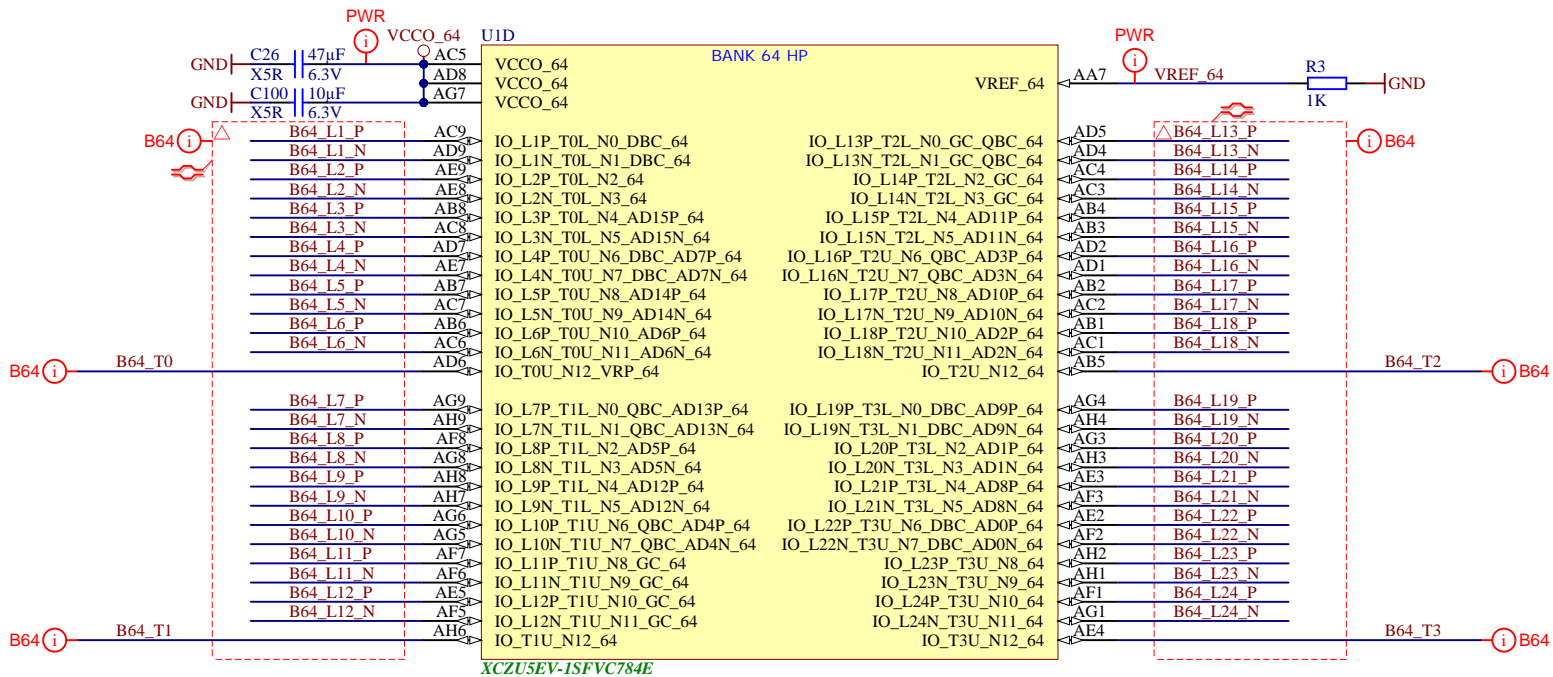
BANK 43 HD (ZU2/3 BANK 44 HD)



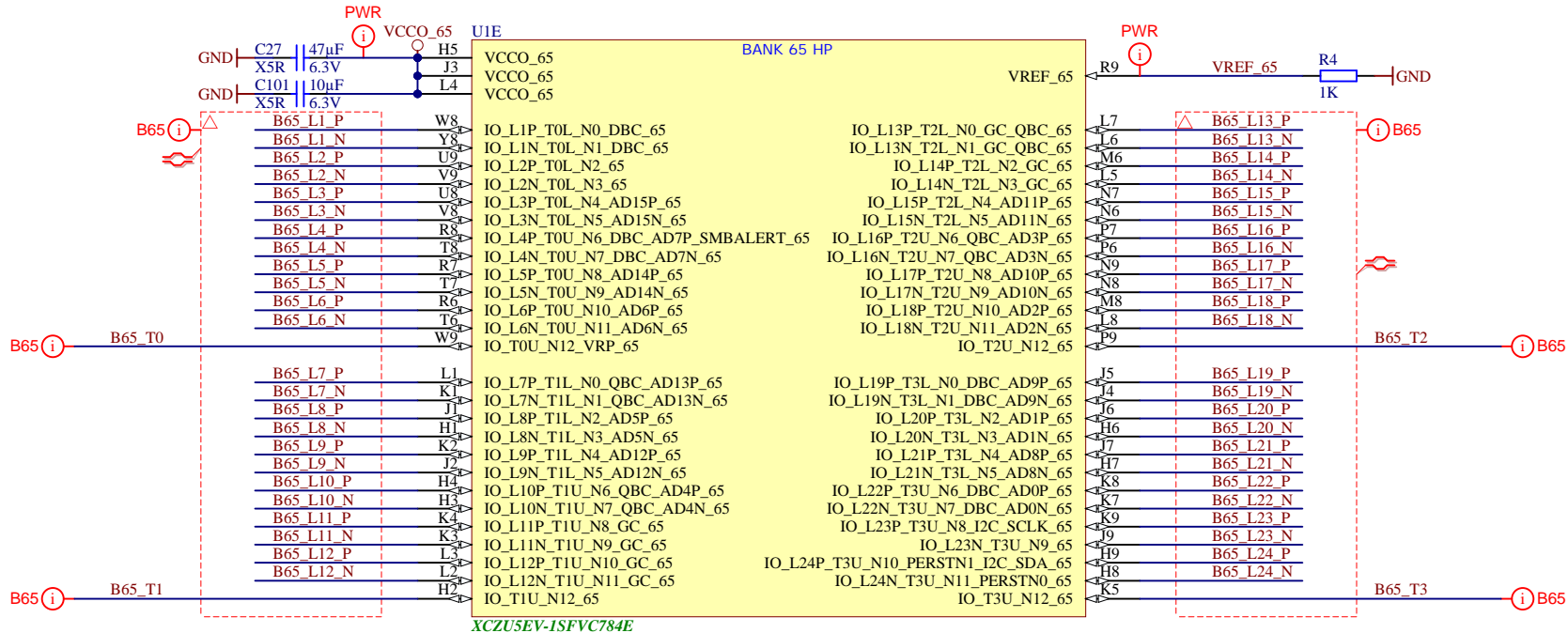
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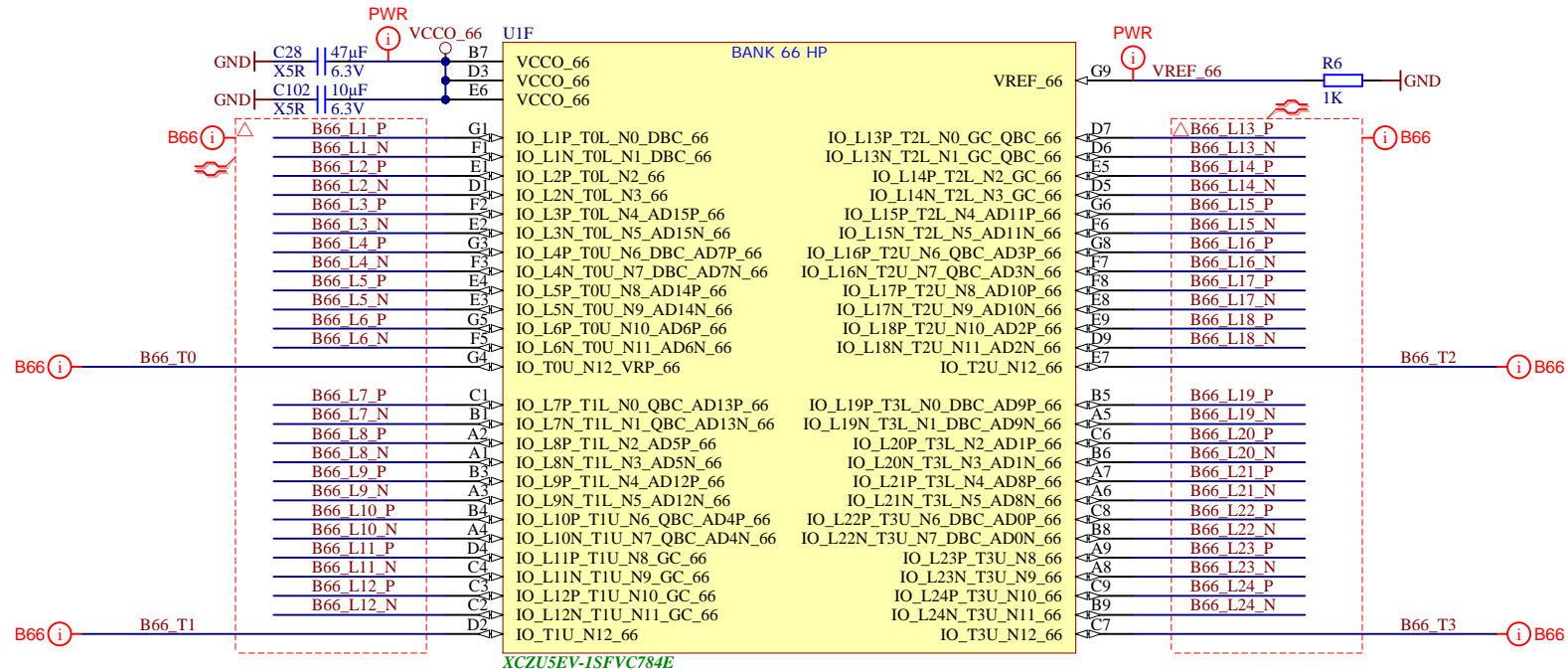
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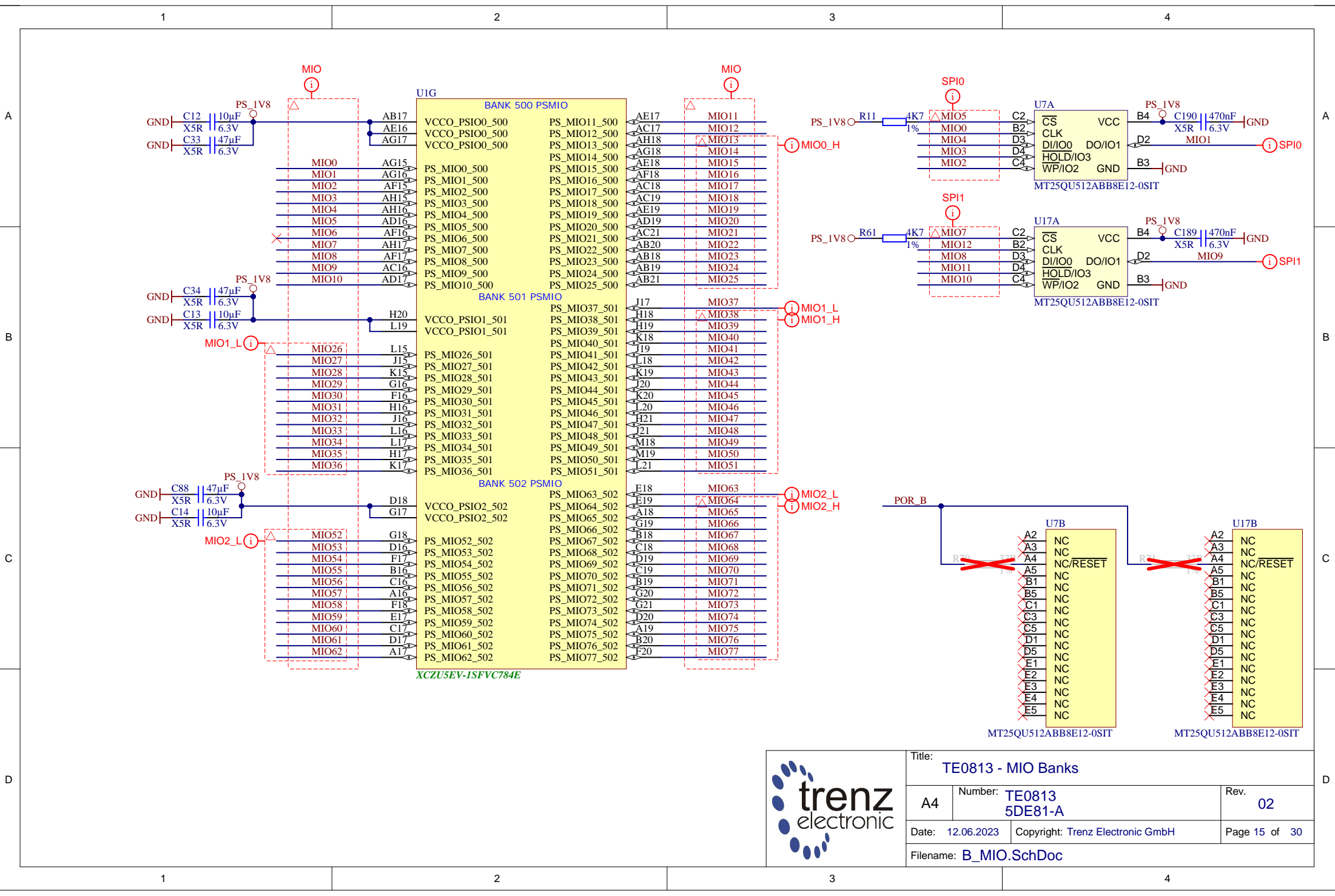
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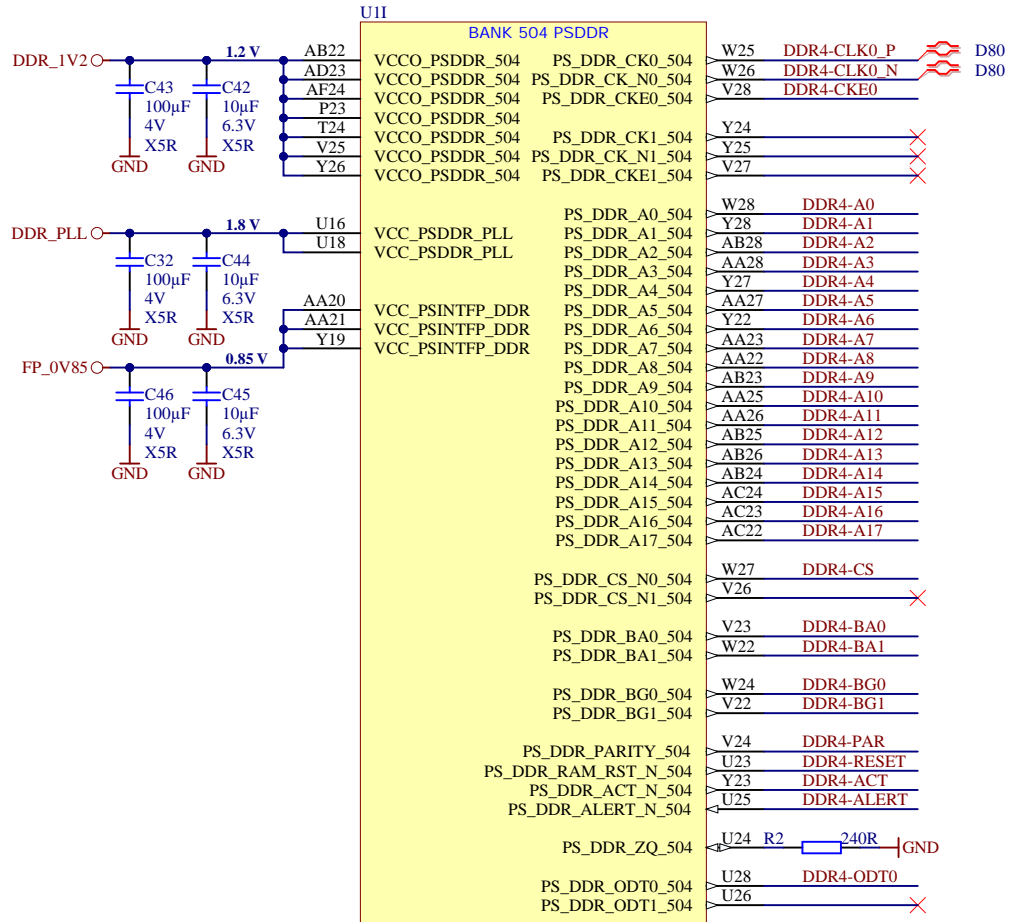
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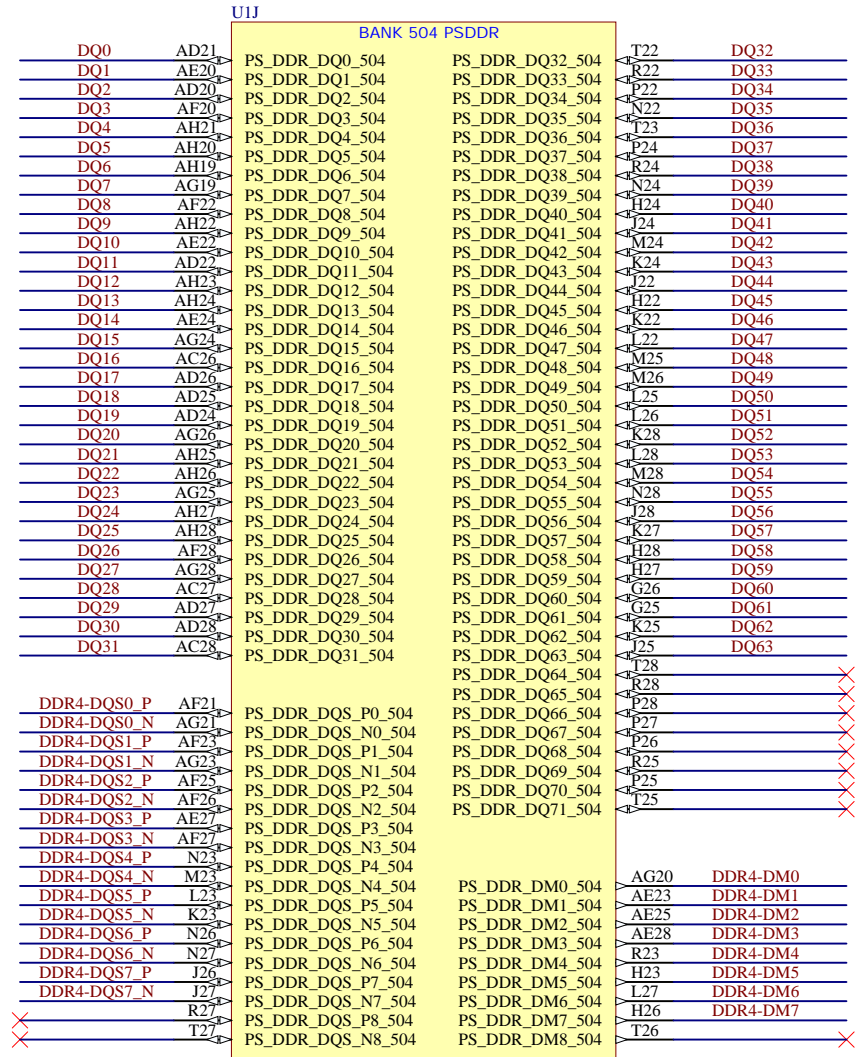
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Title: <b>TE0813 - MIO Banks</b>		
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Filename: <b>B_MIO.SchDoc</b>		



XCZU5EV-1SFVC784E



XCZU5EV-1SFVC784E



Title: <b>TE0813 - PS_DDR</b>		
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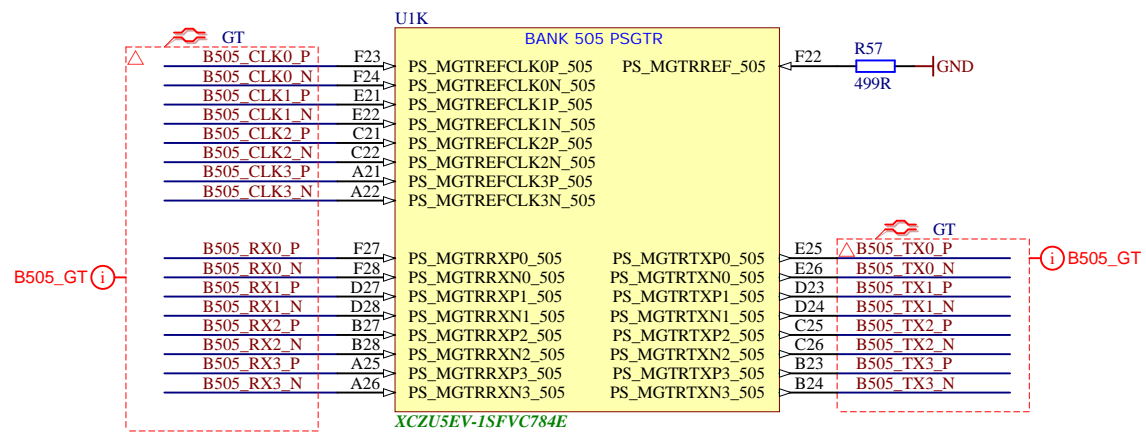
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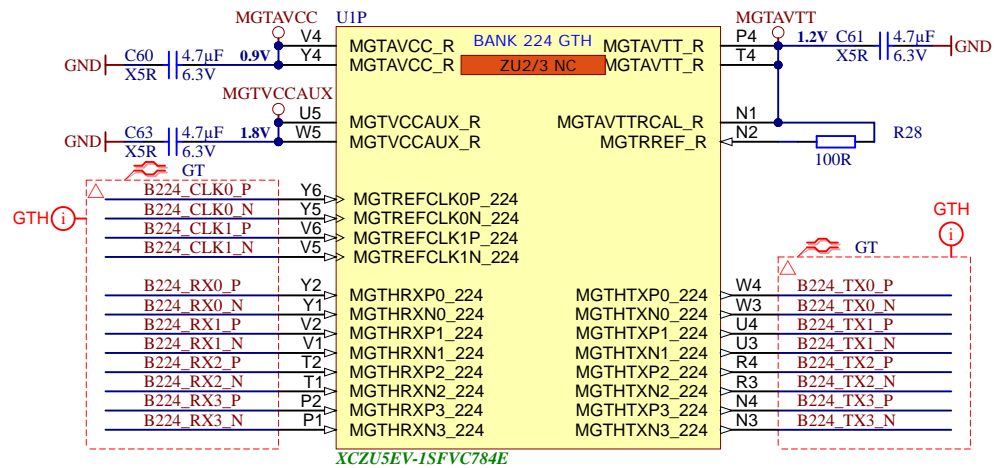
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A4	Number: TE0813 5DE81-A	Rev. 02
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	Title: <b>TE0813 - B224 - GTH</b>		
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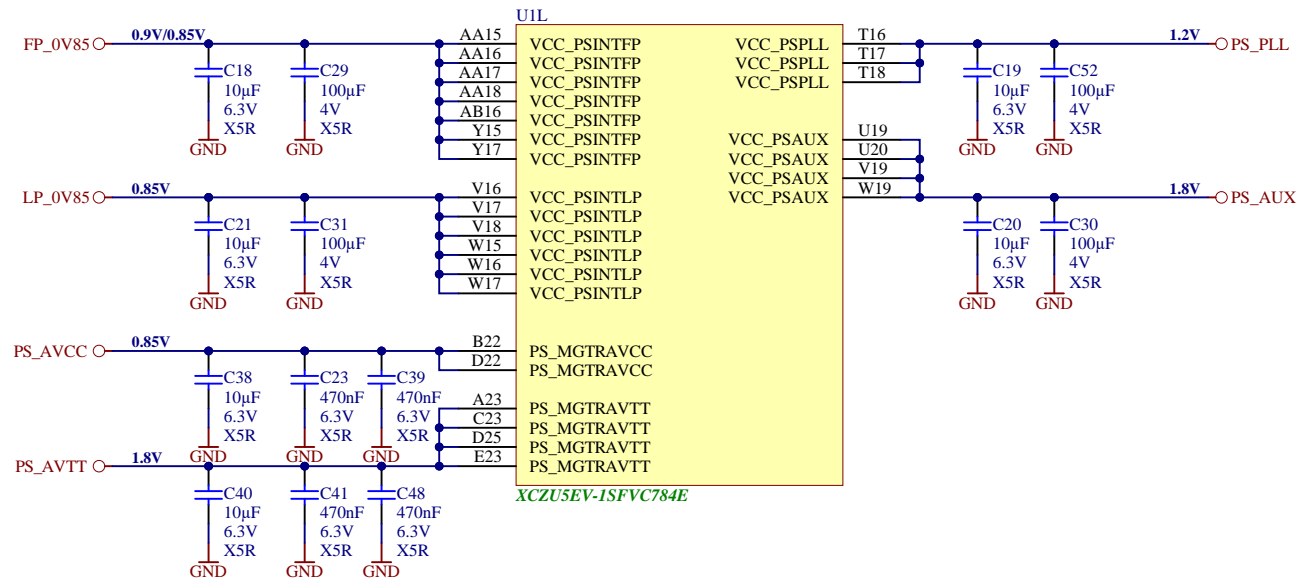
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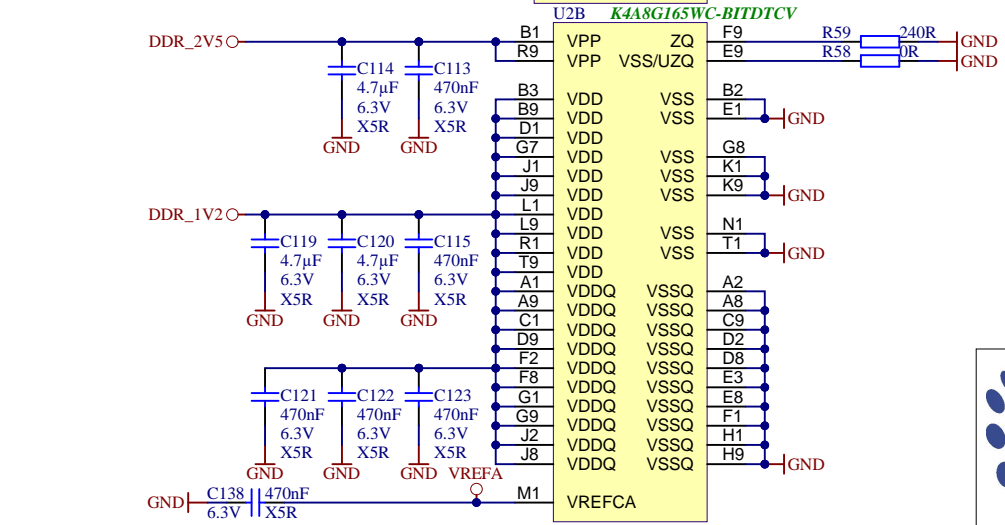
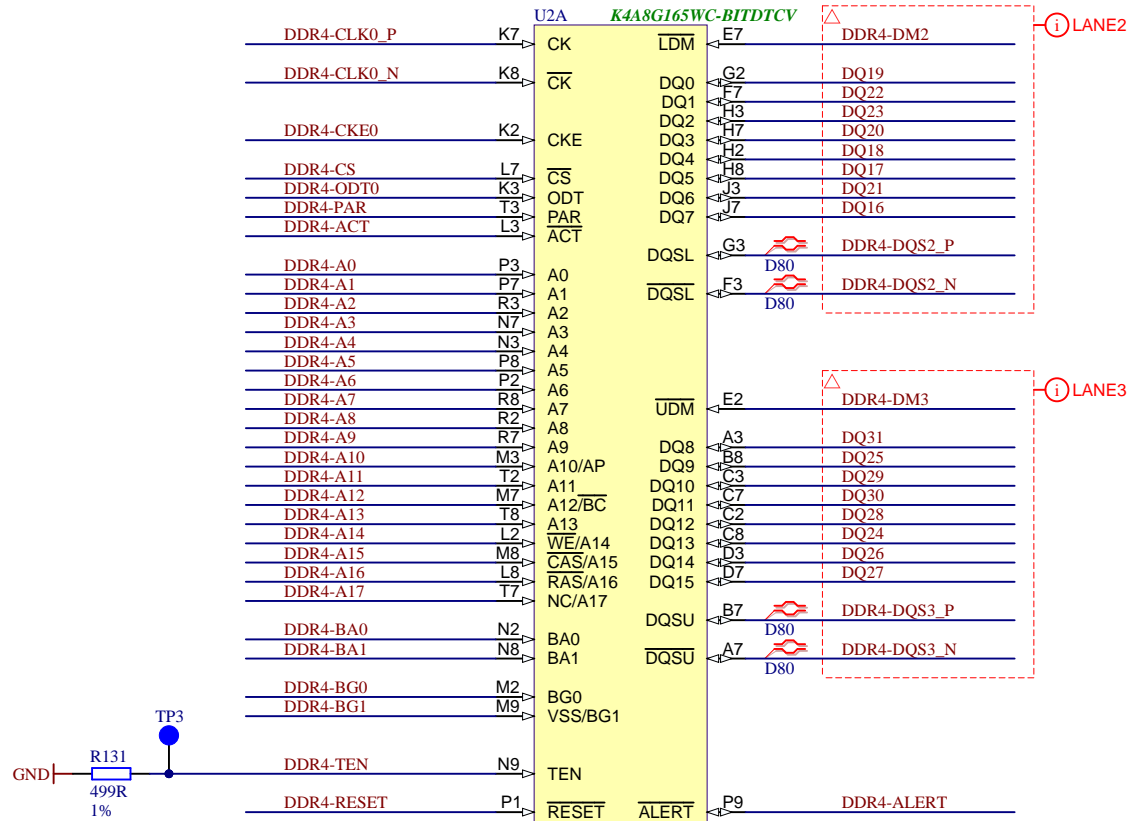
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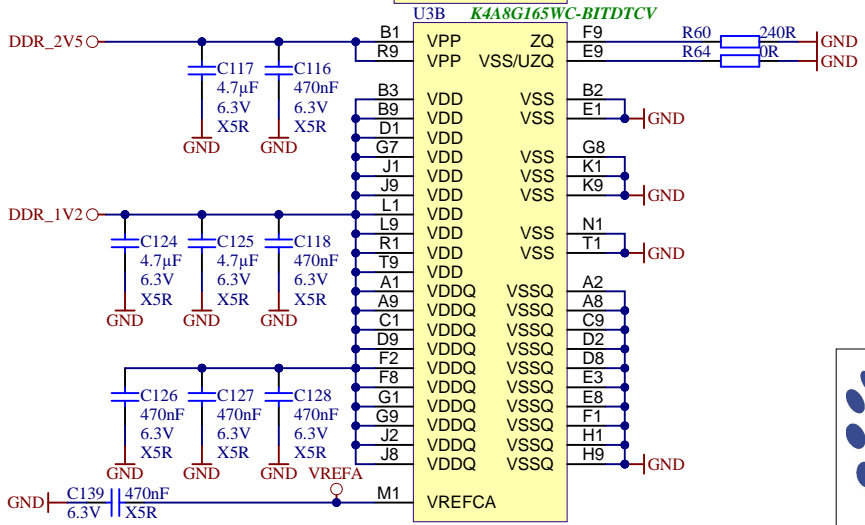
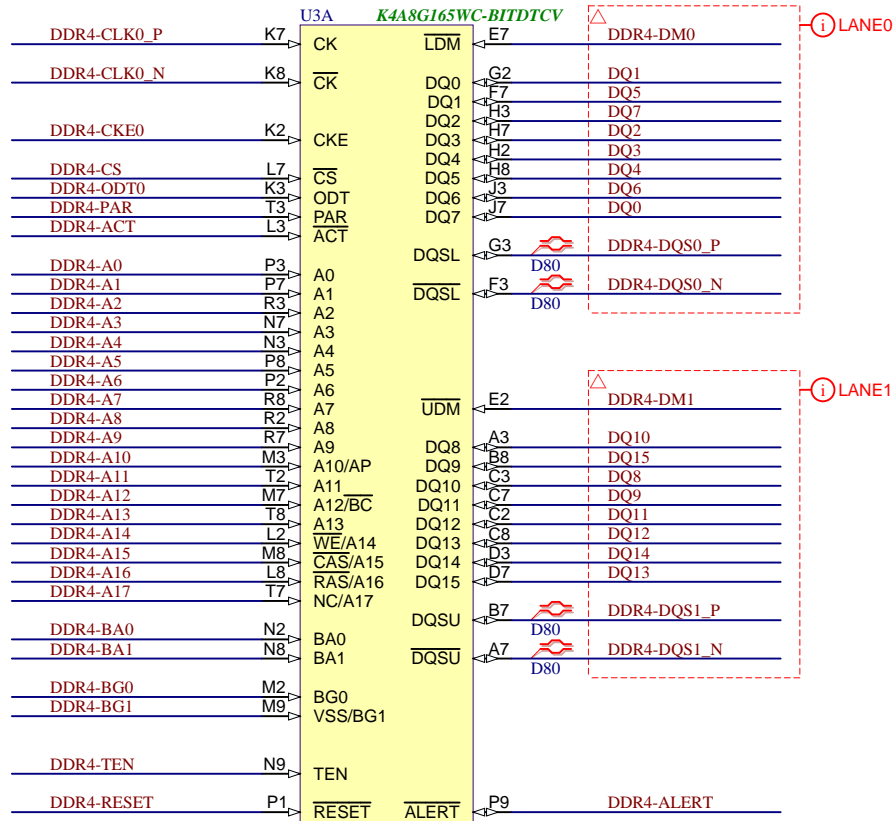


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		A4	Number: TE0813 5DE81-A
Date: 13.06.2023		Copyright: Trenz Electronic GmbH	
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Filename: ZU_PS_POWER.SchDoc			

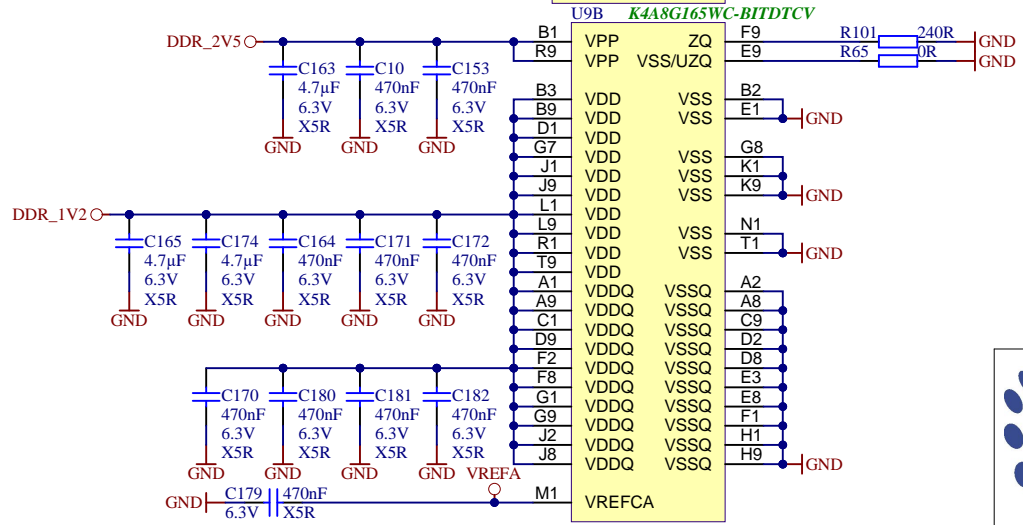
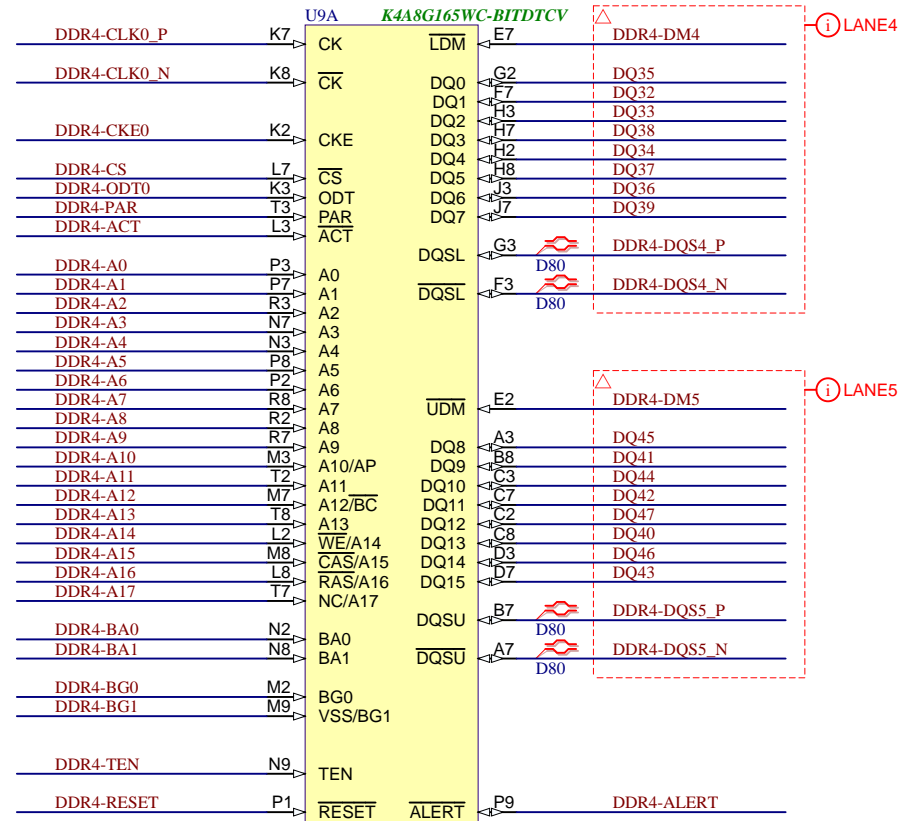




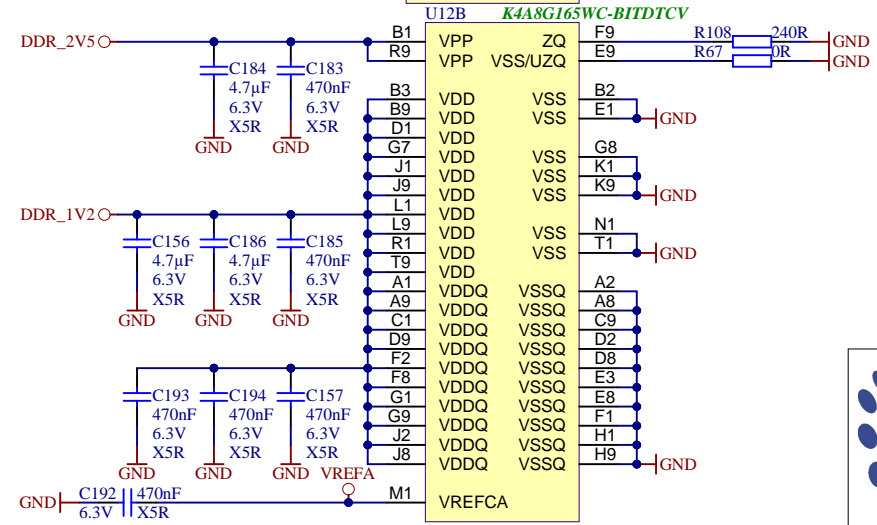
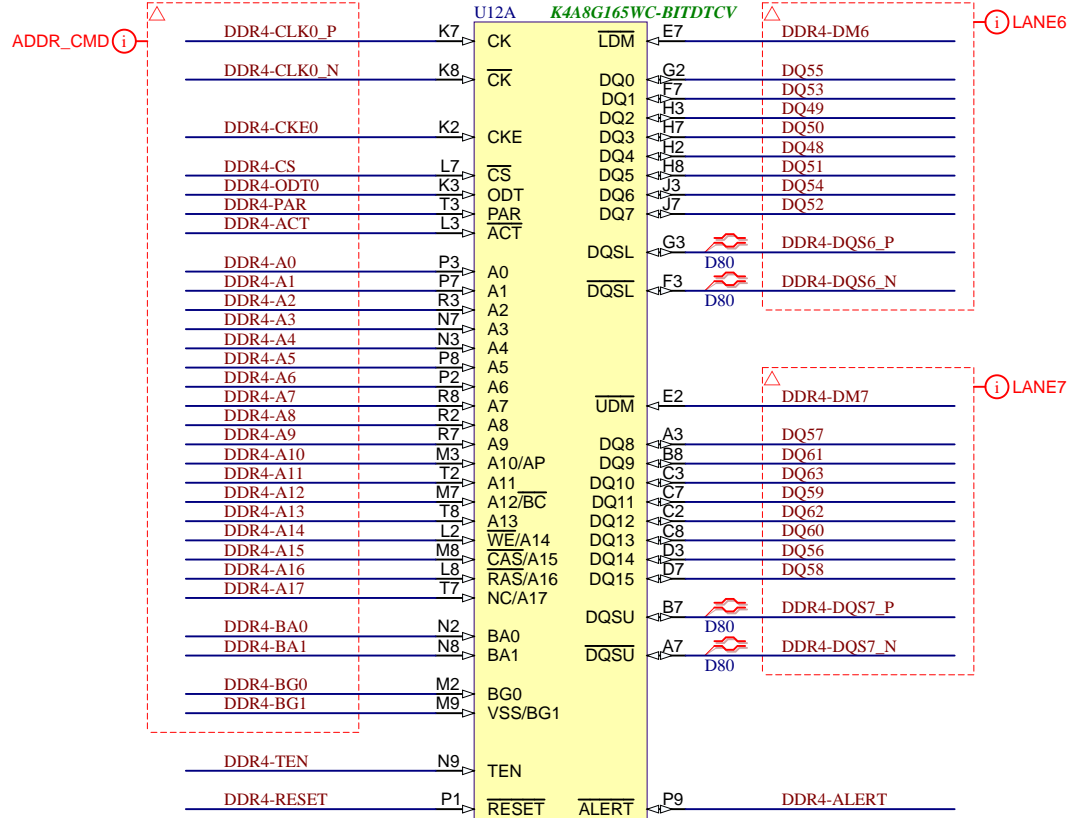
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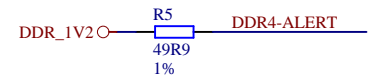
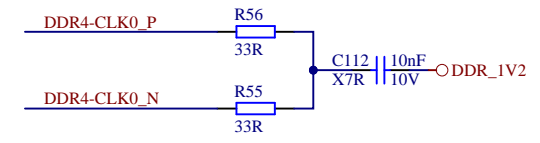
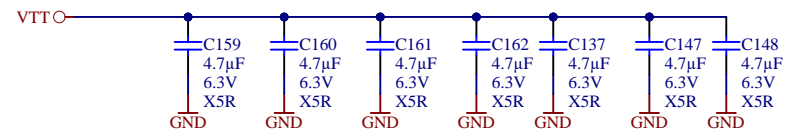
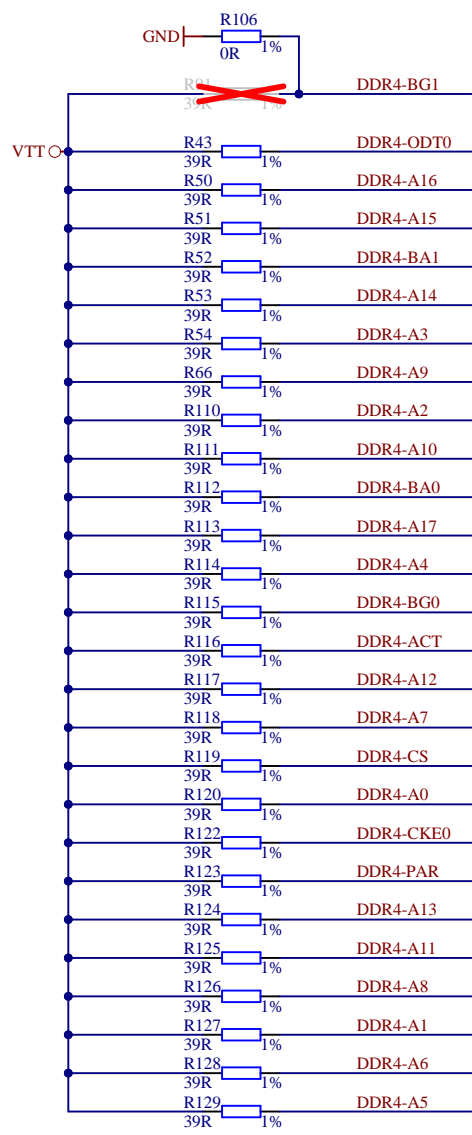


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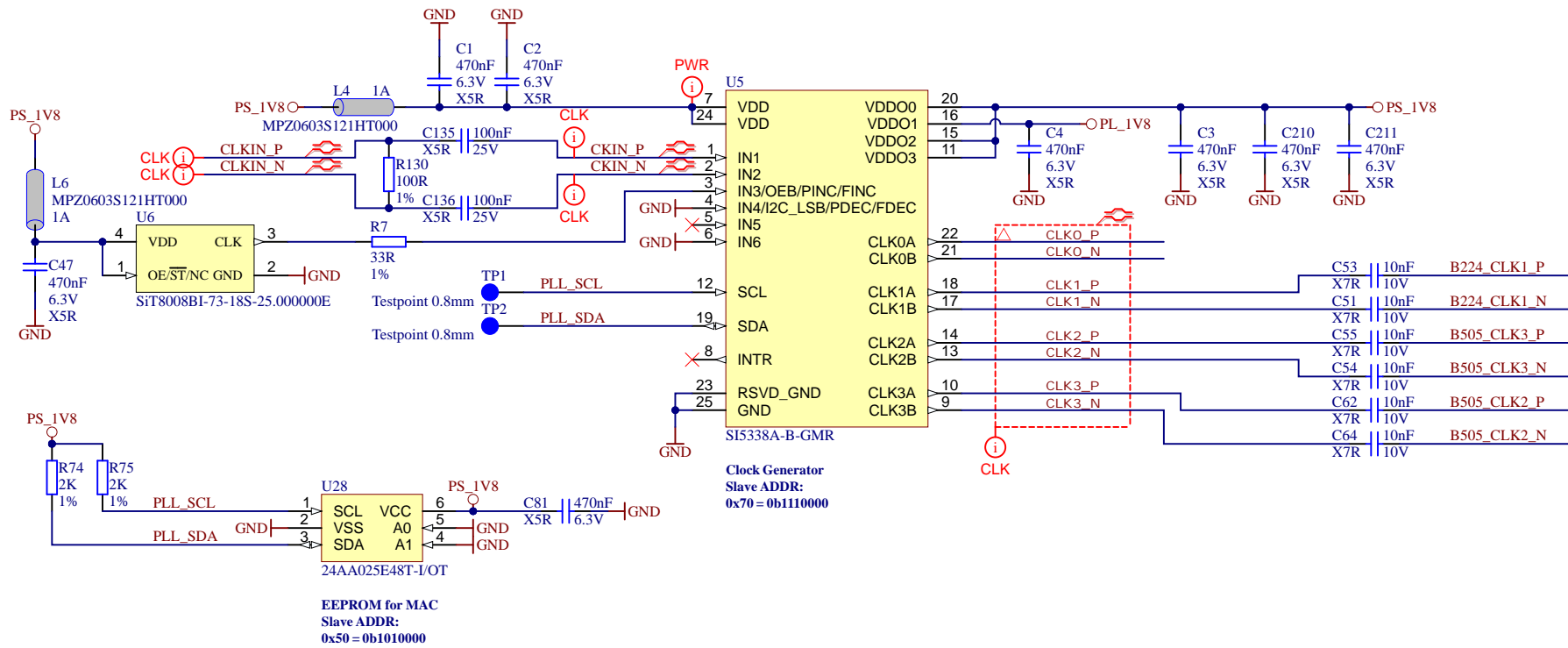



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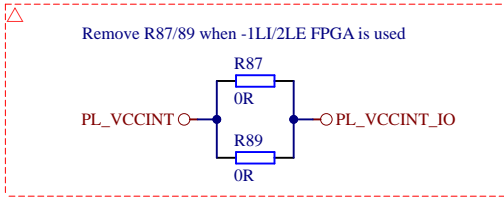


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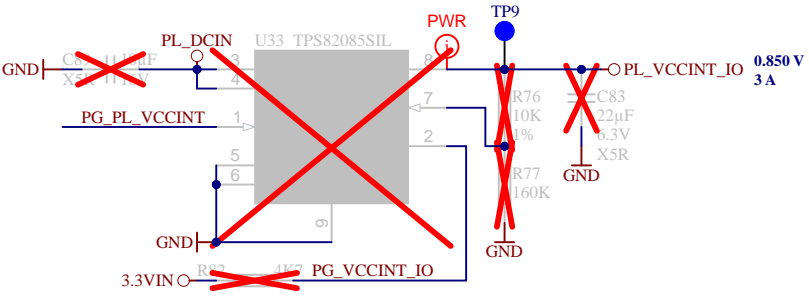
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		A4	Number: TE0813 5DE81-A
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Filename: Clock.SchDoc			



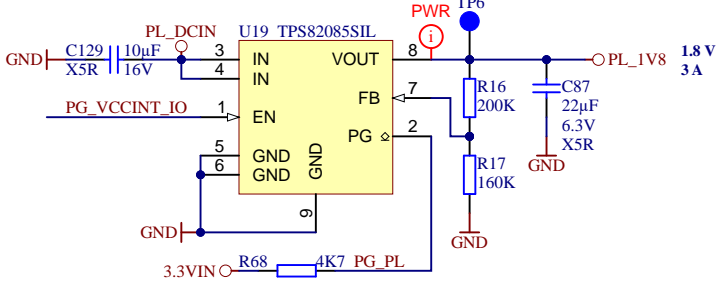


### VCCINT\_IO & VCCBRAM

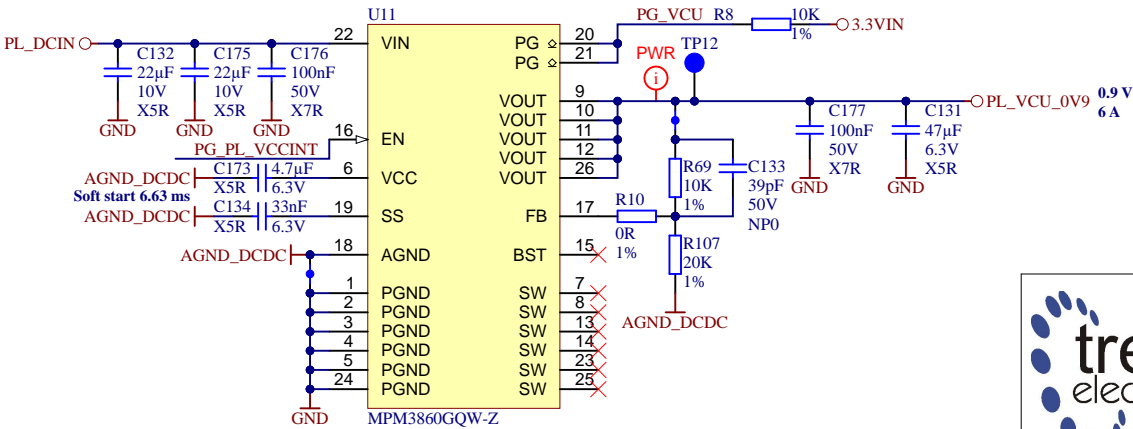
Add U33 when -1L1/2LE FPGA is used



### PL VCCIO

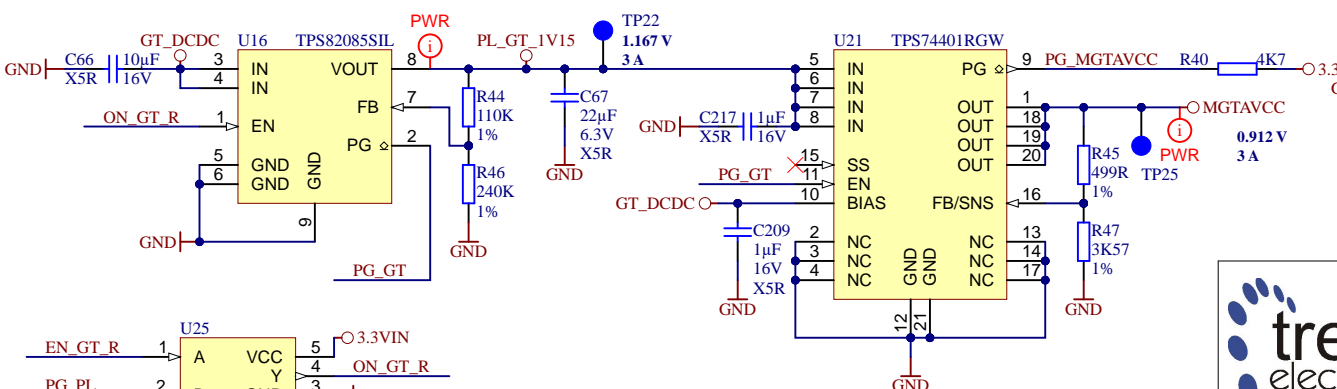
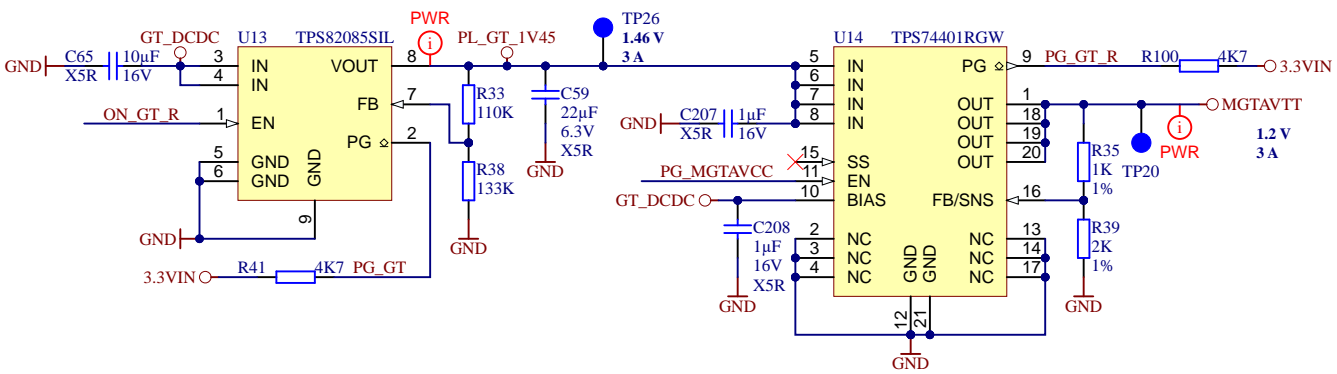
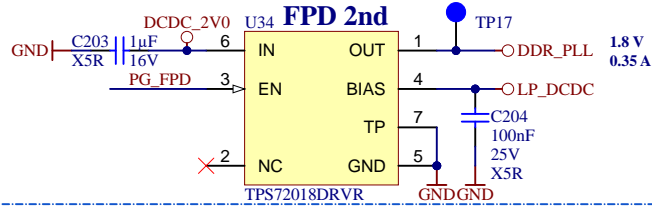
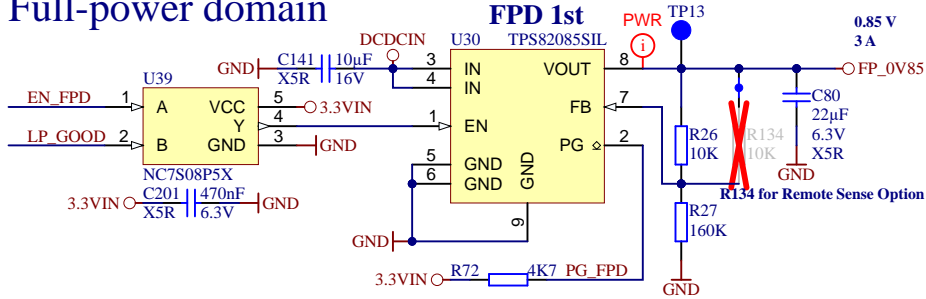


### VCU

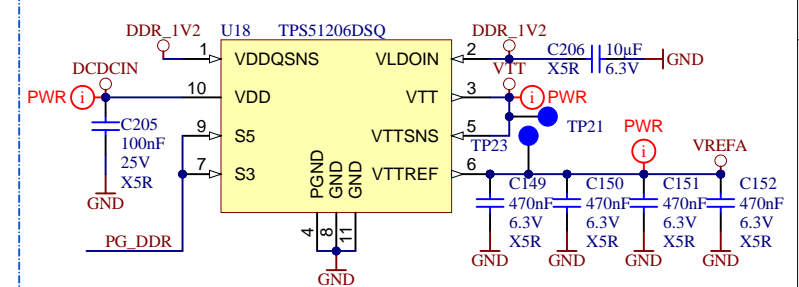
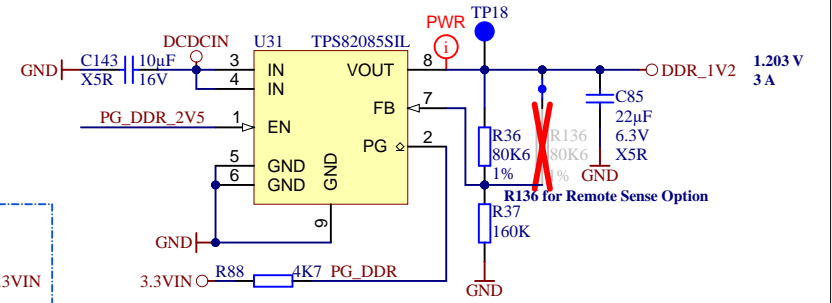
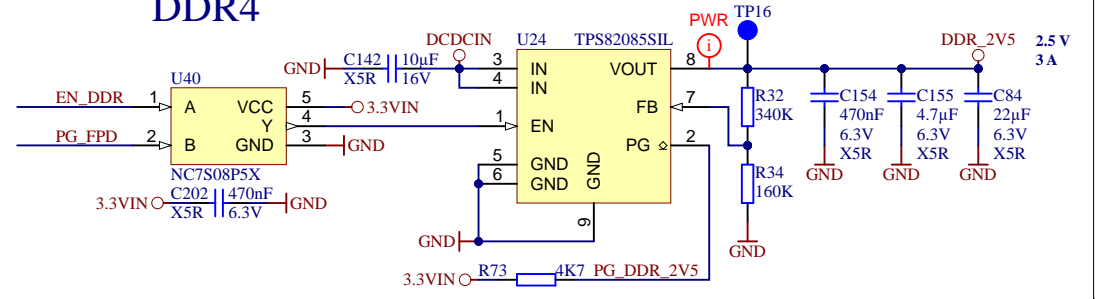


Title: TE0813 - POWER_2		
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# Full-power domain



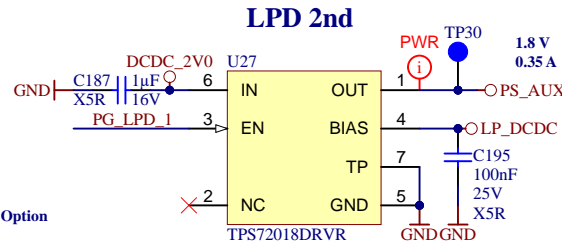
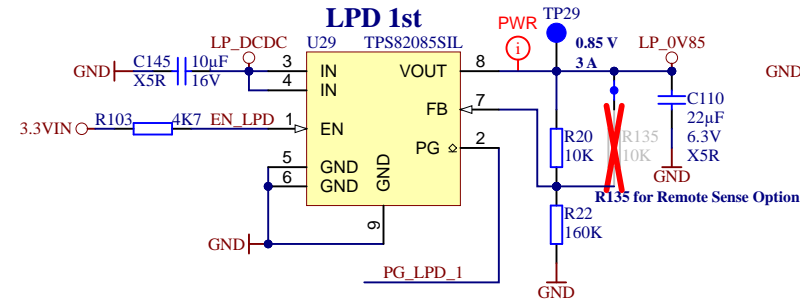
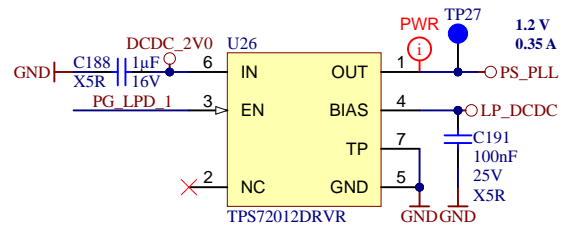
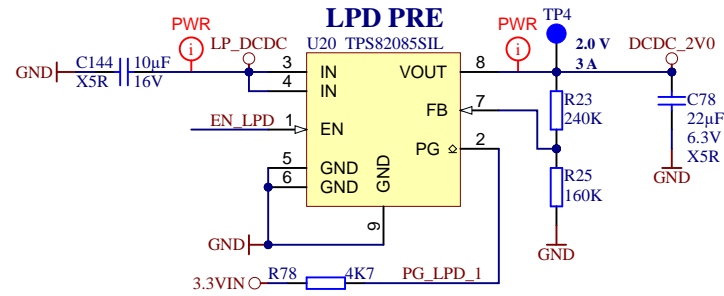
# DDR4



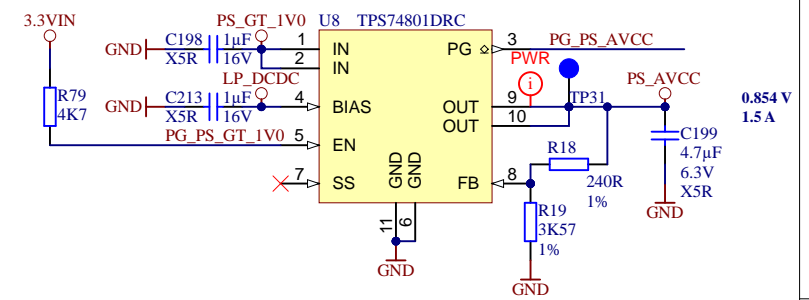
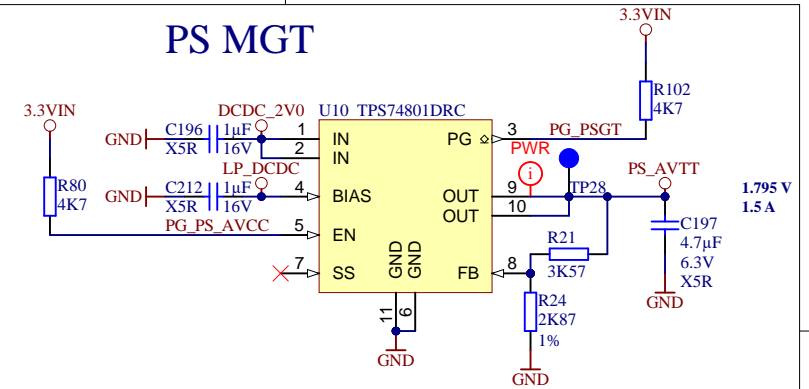
PL MGT

Title: <b>TE0813 - POWER_3</b>		
A4	Number: <b>TE0813 5DE81-A</b>	Rev. <b>02</b>
Date: <b>14.06.2023</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>29</b> of <b>30</b>
Filename: <b>POWER_2.SchDoc</b>		

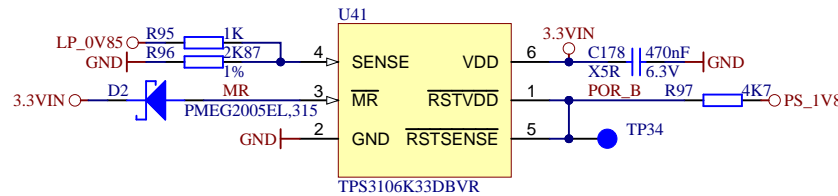
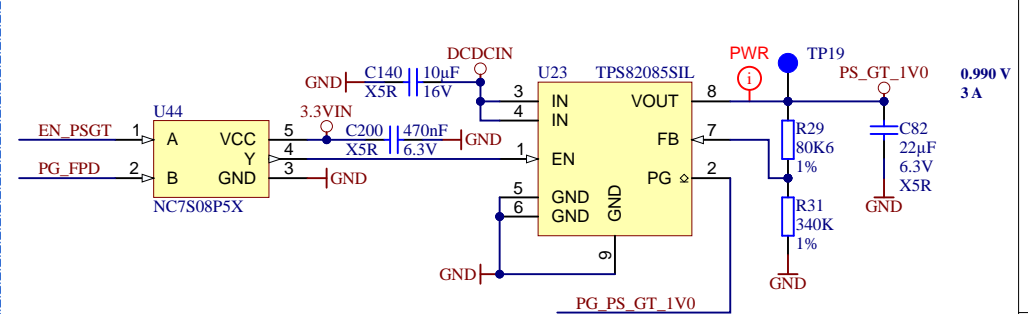
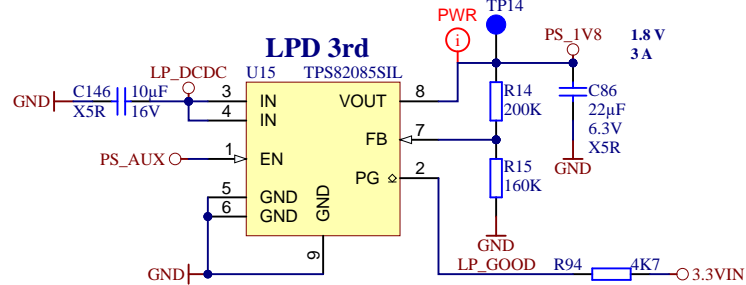
## Low-power domain



## PS MGT



## PS MIO VCCIO



Net Name	Voltage Rail	Low Detect
LP_OV85	0.85 V	0.743 V
3.3V <sub>VIN</sub>	3.3 V	2.941 V



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