



## TE0813 Test Board

Revision v.6

Exported on 2023-06-21

Online version of this document:

<https://wiki.trenz-electronic.de/display/PD/TE0813+Test+Board>

# 1 Table of Contents

---

1	Table of Contents.....	2
2	Table of Figures.....	4
3	Table of Tables.....	5
4	Overview.....	7
4.1	Key Features.....	7
4.2	Revision History.....	7
4.3	Release Notes and Know Issues.....	8
4.4	Requirements.....	8
4.4.1	Software.....	8
4.4.2	Hardware.....	9
4.5	Content.....	10
4.5.1	Design Sources.....	10
4.5.2	Additional Sources.....	11
4.5.3	Prebuilt.....	11
4.5.4	Download.....	12
5	Design Flow.....	13
6	Launch.....	15
6.1	Programming.....	15
6.1.1	Get prebuilt boot binaries.....	15
6.1.2	QSPI-Boot mode.....	15
6.1.3	SD-Boot mode.....	15
6.1.4	JTAG.....	15
6.2	Usage.....	16
7	System Design - Vivado.....	17
7.1	Block Design.....	17
7.1.1	PS Interfaces.....	17
7.2	Constrains.....	18
7.2.1	Basic module constrains.....	18
7.2.2	Design specific constrain.....	18
8	Software Design - Vitis.....	19
8.1	Application.....	19
8.1.1	zynqmp_fsbl.....	19
8.1.2	zynqmp_fsbl_flash.....	19
8.1.3	hello_te0813.....	19
9	Additional Software.....	20
10	Appx. A: Change History and Legal Notices.....	21
10.1	Document Change History.....	21
10.2	Data Privacy.....	21
10.3	Document Warranty.....	21
10.4	Limitation of Liability.....	21

10.5	Copyright Notice .....	22
10.6	Technology Licenses.....	22
10.7	Environmental Protection .....	22
10.8	REACH, RoHS and WEEE .....	22

## 2 Table of Figures

---

Figure 1: Block Design .....	17
------------------------------	----

## 3 Table of Tables

---

Table 1: Design Revision History .....	7
Table 2: Known Issues.....	8
Table 3: Software .....	8
Table 4: Hardware Modules.....	9
Table 5: Hardware Carrier.....	10
Table 6: Additional Hardware.....	10
Table 7: Design sources .....	10
Table 8: Additional design sources .....	11
Table 9: Prebuilt files (only on ZIP with prebuilt content) .....	11
Table 10: PS Interfaces.....	17
Table 11: Document change history. ....	21



## 4 Overview

Design Example with minimum PS Setup (DDR, QSPI, UART0) only for custom boards or easier debug via Vitis.

Refer to <http://trenz.org/te0813-info> for the current online version of this manual and other available documentation.

### 4.1 Key Features

- Vitis/Vivado 2021.2.1
- QSPI
- Custom Carrier (minimum PS Design with available module components only)
- Modified FSBL (some additional outputs only)
- Special FSBL for QSPI Programming

### 4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2022-10-18	2021.2.1	TE0813-test_board_noprebuilt-vivado_2021.2-build_18_20221018115000.zip TE0813-test_board-vivado_2021.2-build_18_20221018115000.zip	Manuela Strücker	<ul style="list-style-type: none"> <li>• update Vivado 2021.2.1</li> <li>• new variants</li> <li>• script update</li> </ul>
2021-11-16	2020.2	TE0813-test_board_noprebuilt-vivado_2020.2-build_9_20211116073725.zip TE0813-test_board-vivado_2020.2-build_9_20211116073013.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• new variants</li> </ul>
2021-10-28	2020.2	TE0813-test_board-vivado_2020.2-build_8_20211028144436.zip TE0813-	Manuela Strücker	<ul style="list-style-type: none"> <li>• initial release</li> </ul>

Date	Vivado	Project Built	Authors	Description
		test_board_noprebuilt-vivado_2020.2-build_8_20211028144418.zip		

**Table 1: Design Revision History**

## 4.3 Release Notes and Known Issues

Issues	Description	Workaround	To be fixed version
Xilinx Software	Incompatibility of board files for ZynqMP with eMMC activated between 2021.2 and 2021.2.1 patch, see <a href="#">Xilinx Forum Request<sup>1</sup></a>	use corresponding board files for the Vivado versions	--
QSPI Flash	Programming QSPI flash fails sometimes	use Vivado 2019.2 for programming	

**Table 2: Known Issues**

## 4.4 Requirements

### 4.4.1 Software

Software	Version	Note
Vitis	2021.2.1	needed, Vivado is included into Vitis installation

**Table 3: Software**

<sup>1</sup> [https://support.xilinx.com/s/feed/0D54U00005Wbon6SAB?language=en\\_US](https://support.xilinx.com/s/feed/0D54U00005Wbon6SAB?language=en_US)



## 4.4.2 Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).<sup>2</sup>

Complete List is available on "<project folder>\board\_files\\*\_board\_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0813-01-4 BE11-A*	4eg_1e_2gb	REV01	2GB	128MB	NA	NA	NA
TE0813-01-2 AE11-A	2cg_1e_2gb	REV01	2GB	128MB	NA	NA	NA
TE0813-01-2 BE11-A	2eg_1e_2gb	REV01	2GB	128MB	NA	NA	NA
TE0813-01-3 AE11-A	3cg_1e_2gb	REV01	2GB	128MB	NA	NA	NA
TE0813-01-4 AE11-A	4cg_1e_2gb	REV01	2GB	128MB	NA	NA	NA
TE0813-01-5 DE11-A	5ev_1e_2gb	REV01	2GB	128MB	NA	NA	NA
TE0813-01-3 BE11-A	3eg_1e_2gb	REV01	2GB	128MB	NA	NA	NA
TE0813-01-4 DE11-A	4ev_1e_2gb	REV01	2GB	128MB	NA	NA	NA
TE0813-01-4 DE11-AZ	4ev_1e_2gb	REV01	2GB	128MB	NA	NA	NA
TE0813-01-4 BE71-A	4eg_1e_4gb	REV01	4GB	128MB	NA	NA	NA

<sup>2</sup> <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0813-01-4 BE11-AZ	4eg_1e_2gb	REV01	2GB	128MB	NA	NA	NA

**Table 4: Hardware Modules**

\*used as reference

Note: Design contains also Board Part Files for TE0813+TEBF0818 configuration, this board part files are not used for this reference design.

Design supports following carriers:

Carrier Model	Notes
TEBF0818*	Used as reference carrier.

**Table 5: Hardware Carrier**

\*used as reference

Additional HW Requirements:

Additional Hardware	Notes
---	---

**Table 6: Additional Hardware**

\*used as reference

## 4.5 Content

For general structure and usage of the reference design, see [Project Delivery - Xilinx devices](https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices)<sup>3</sup>

### 4.5.1 Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints	Vivado Project will be generated by TE Scripts

<sup>3</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices>

Type	Location	Notes
	<project folder>\ip_lib <project folder>\board_files	
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

**Table 7: Design sources**

## 4.5.2 Additional Sources

Type	Location	Notes
---	---	---

**Table 8: Additional design sources**

## 4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Diverse Reports	---	Report files in different formats
Hardware-Platform-Description-File	*.xsa	Exported Vivado <a href="#">hardware description file</a> for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File

File	File-Extension	Description
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

**Table 9: Prebuilt files (only on ZIP with prebuilt content)**

#### 4.5.4 Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0813 "Test Board" Reference Design<sup>4</sup>](#)

---

<sup>4</sup> [https://shop.trenz-electronic.de/Download/?path=Trenz\\_Electronic/Modules\\_and\\_Module\\_Carriers/5.2x7.6/TE0813/Reference\\_Design/2021.2/test\\_board](https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0813/Reference_Design/2021.2/test_board)

## 5 Design Flow

**!** Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- [AMD Development Tools](#)<sup>5</sup>
- [Vivado Projects - TE Reference Design](#)<sup>6</sup>
- [Project Delivery](#).<sup>7</sup>

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "\_create\_win\_setup.cmd" on Windows OS and "\_create\_linux\_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also be executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)<sup>8</sup>

**!** **Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run \_create\_win\_setup.cmd/\_create\_linux\_setup.sh and follow instructions on shell:

### \_create\_win\_setup.cmd/\_create\_linux\_setup.sh

```
-----Set design paths-----
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
-----
-----TE Reference Design-----
-----
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
-----
Select (ex.: '0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"


<sup>5</sup> <https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDDevelopmentTools-XilinxSoftware-BasicUserGuides>

<sup>6</sup> <https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design>

<sup>7</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices>

<sup>8</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality>


3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
  - optional for manual changes: Select correct device and Xilinx install path on "design\_basic\_settings.cmd" and create Vivado project with "vivado\_create\_project\_gui\_mode.cmd"

 Note: Select correct one, see also [Vivado Board Part Flow](#)<sup>9</sup>  
**Important:** Use Board Part Files, which **did not** ends with \*\_tebf0818

4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

**run on Vivado TCL (Script generates design and export files into "\prebuilt\hardware\")**


```
\prebuilt\hardware\")">
TE::hw_build_design -export_prebuilt
```

 Using Vivado GUI is the same, except file export to prebuilt folder.

5. Generate Programming Files with Vitis

**run on Vivado TCL (Script generates applications and bootable files, which are defined in "test\_board\sw\_lib\apps\_list.csv")**

```
TE::sw_run_vitis -all
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start with TE
Scripts on Vivado TCL)
```


 TCL scripts generate also platform project, this must be done manually in case GUI is used. See [Vitis](#)<sup>10</sup>

<sup>9</sup> <https://wiki.trenz-electronic.de/display/PD/Vivado+Board+Part+Flow>

<sup>10</sup> <https://wiki.trenz-electronic.de/display/PD/Vitis>

## 6 Launch


### 6.1 Programming

-  Check Module and Carrier TRMs for proper HW configuration before you try any design. Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: [Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging](#)<sup>11</sup>

#### 6.1.1 Get prebuilt boot binaries

1. Run `_create_win_setup.cmd/_create_linux_setup.sh` and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
  - a. Select assembly version
  - b. Validate selection
  - c. Select create and open delivery binary folder


 Note: Folder "<project folder>\\_binaries\_<Article Name>" with subfolder "boot\_<app name>" for different applications will be generated

#### 6.1.2 QSPI-Boot mode

1. Connect **JTAG** and power on carrier with module
2. Open Vivado Project with "vivado\_open\_existing\_project\_guimode.cmd" or if not created, create with "vivado\_create\_project\_guimode.cmd"

**run on Vivado TCL (Script programs BOOT.bin on QSPI flash)**

```
TE::pr_program_flash -swapp hello_te0813
```

 To program with Vitis/Vivado GUI, use special FSBL (fsbl\_flash) on setup

#### 6.1.3 SD-Boot mode

This does not work, because SD controller is not selected on PS.

#### 6.1.4 JTAG

Load configuration and Application with Vitis Debugger into device


<sup>11</sup> <https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDDevelopmentTools-XilinxSoftwareProgrammingandDebugging>

## 6.2 Usage

---

QSPI Boot:

1. Prepare HW like described on section [Programming](#)(see page 15)
2. Connect UART USB (most cases same as JTAG)
3. Select QSPI as Boot Mode

 Note: See TRM of the Carrier, which is used.

4. Power On PCB

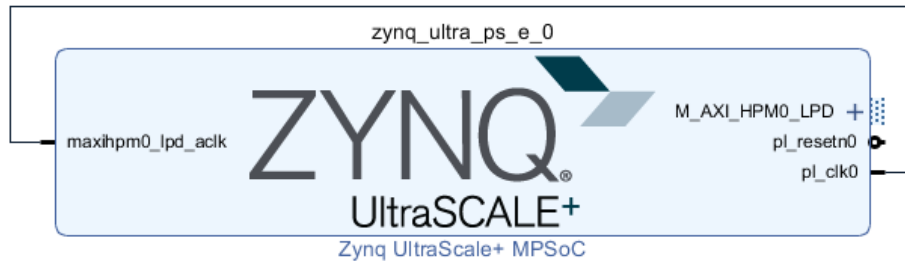
### **boot process**

1. ZynqMP Boot ROM loads FSBL from QSPI into OCM,
2. FSBL init the PS, programs the PL using the bitstream and loads PMU, ATF and U-boot from QSPI into DDR,



## 7 System Design - Vivado

### 7.1 Block Design



**Figure 1: Block Design**

#### 7.1.1 PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
UART0	MIO, please select other one, if you have connected UART to second controller or other MIO
SWDT0..1	
TTC0..3	

**Table 10: PS Interfaces**

## 7.2 Constrains

---

### 7.2.1 Basic module constrains

---

#### **\_i\_bitgen.xdc**

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]  
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

### 7.2.2 Design specific constrain

---

Not needed.

## 8 Software Design - Vitis

---

For Vitis project creation, follow instructions from:

[Vitis<sup>12</sup>](https://wiki.trenz-electronic.de/display/PD/Vitis)

### 8.1 Application

---

Template location: "<project folder>\sw\_lib\sw\_apps\"

#### 8.1.1 zynqmp\_fsbl

---

TE modified 2021.2 FSBL

General:

- Modified Files: xfsbl\_main.c, xfsbl\_hooks.h/.c, xfsbl\_board.h/.c (search for 'TE Mod' on source code)
- Add Files: te\_xfsbl\_hooks.h/.c (for hooks and board)
- General Changes:
  - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te\_\*
  - Si5338 Configuration
  - OTG+PCIe Reset over MIO
  - I2C MUX for EEPROM MAC

#### 8.1.2 zynqmp\_fsbl\_flash

---

TE modified 2021.2 FSBL

General:

- Modified Files: xfsbl\_initialisation.c, xfsbl\_hw.h, xfsbl\_handoff.c, xfsbl\_main.c
- General Changes:
  - Display FSBL Banner
  - Set FSBL Boot Mode to JTAG
  - Disable Memory initialisation

#### 8.1.3 hello\_te0813

---

Hello TE0813 is a Xilinx Hello World example as endless loop instead of one console output.

---

<sup>12</sup> <https://wiki.trenz-electronic.de/display/PD/Vitis>

## 9 Additional Software



---

No additional software is needed.

## 10 Appx. A: Change History and Legal Notices

### 10.1 Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
 2022-10-20	v.6(see page 6)	Manuela Strücker <sup>13</sup>	<ul style="list-style-type: none"> <li>• update Vivado 2021.2.1</li> <li>• new Variants</li> <li>• script update</li> </ul>
2022-09-06	v5	Manuela Strücker	<ul style="list-style-type: none"> <li>• new Variants</li> </ul>
2021-10-28	v.2	Manuela Strücker	<ul style="list-style-type: none"> <li>• initial release 2020.2</li> </ul>
	All		

**Table 11: Document change history.**

Legal Notices

### 10.2 Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

### 10.3 Document Warranty

The material contained in this document is provided “as is” and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

### 10.4 Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked

<sup>13</sup> <https://wiki.trenz-electronic.de/display/~m.struecker>

<sup>14</sup> <https://wiki.trenz-electronic.de/display/~j.hartfiel>

<sup>15</sup> <https://wiki.trenz-electronic.de/display/~m.struecker>

to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

## 10.5 Copyright Notice

---

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Trenz Electronic.

## 10.6 Technology Licenses

---

The hardware / firmware / software described in this document are furnished under a license and may be used / modified / copied only in accordance with the terms of such license.

## 10.7 Environmental Protection

---

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

## 10.8 REACH, RoHS and WEEE

---

### REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH<sup>16</sup>. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List<sup>17</sup> are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA)<sup>18</sup>.

### RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

### WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of

---


<sup>16</sup> <http://guidance.echa.europa.eu/>

<sup>17</sup> <https://echa.europa.eu/candidate-list-table>

<sup>18</sup> <http://www.echa.europa.eu/>

charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

 2019-06-07