


Regarding the usage of our schematics and alike documentation for Trenz module TE0817.

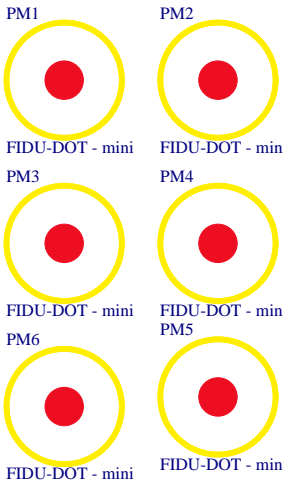
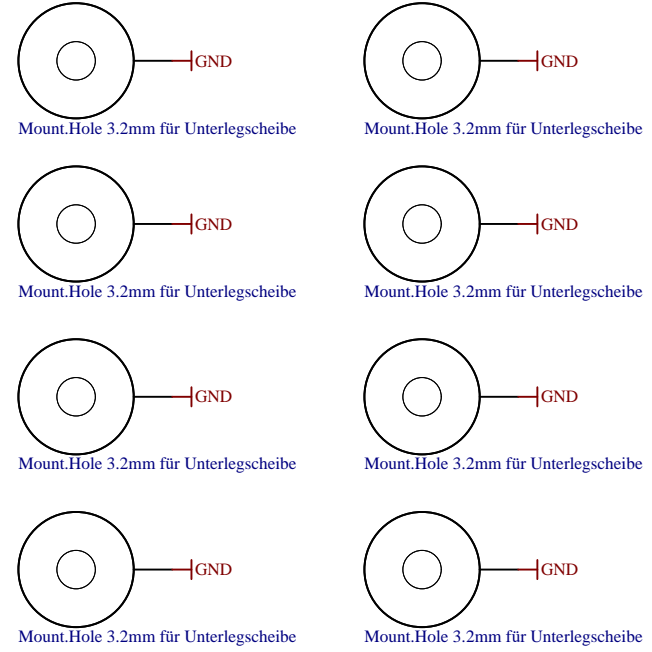
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Schematics and other handouts serve for informational purposes only!

	Title: TE0817		
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	Filename: Legal Notices Modules.SchDoc		

U_J1 J1.SchDoc	U_B_PS_GT B_PS_GT.SchDoc	U_DDR4-TERM DDR4-TERM.SchDoc
U_J2 J2.SchDoc	U_PS_DDR PS_DDR.SchDoc	U_ZU_POWER ZU_POWER.SchDoc
U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	U_POWER_3 POWER_3.SchDoc
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_4.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	U_TE0817-Overview TE0817-Overview.SchDoc
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	U_Power_Diagram Power_Diagram.SchDoc
U_B_GT_2 B_GT_2.SchDoc	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	

Special notes:



LOGO1
TE Logo PRINT Layer
LOGO PRINT

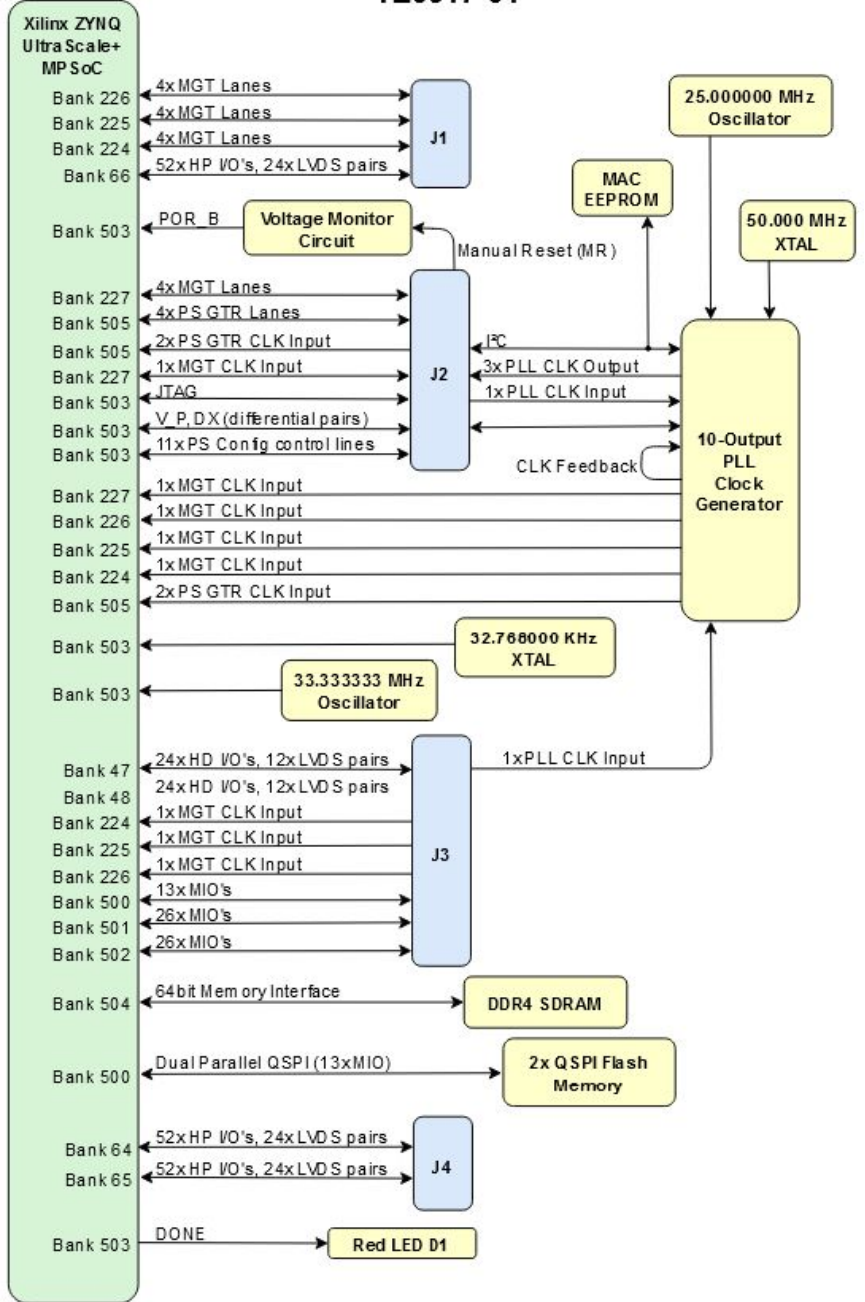
Serial
Serialnumber 6,3 x 6.3mm

MECH1
TE Address Overlay
LOGO ADDRESS

Assembly variant	4AI21-A
Created by	ED
Modified by	VT
Modified at	2022-05-12
SVN Revision	12508

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TE0817-01



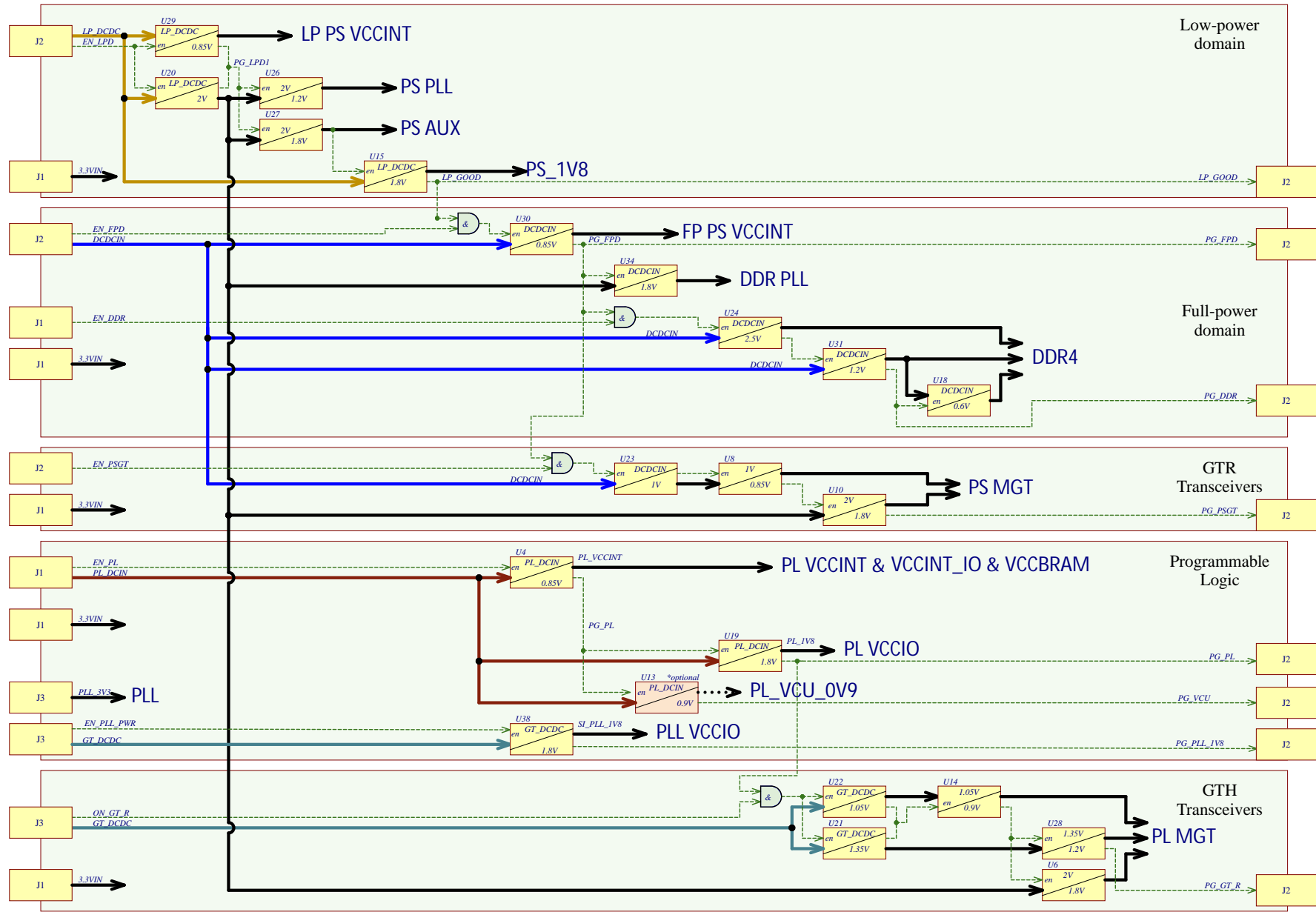
Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
PL_DCIN	IN	3.3 - 5.0V *	+/-5%	Micromodule Power	Programmable Logic, supplied by power rail
LP_DCDC	IN	3.3 - 5.0V	+/-5%	Micromodule Power	Low-Power Domain, supplied by power rail
GT_DCDC	IN	3.3 - 5.0V	+/-5%	Micromodule Power	GTH/GTY Transceiver, supplied by power rail
DCDCIN	IN	3.3 - 5.0V	+/-5%	Micromodule Power	Full-Power Domain and GTR, supplied by power rail
VCCO_64	IN	1.0 - 1.8V	+/-3%	HP IO Bank64	-
VCCO_65	IN	1.0 - 1.8V	+/-3%	HP IO Bank65	-
VCCO_66	IN	1.0 - 1.8V	+/-3%	HP IO Bank66	-
VCCO_47	IN	1.2 - 3.3V	+/-3%	HD IO Bank47	-
VCCO_48	IN	1.2 - 3.3V	+/-3%	HD IO Bank48	-
PSBATT	IN	1.2 - 1.5V	-	RTC / BBRAM	-
PLL_3V3	IN	3.3V	+/-5%	PLL Analog Power	-
PL_1V8	OUT	1.8V	+/-5%	Power for Carrier	Micromodule: Programmable Logic
PS_1V8	OUT	1.8V	+/-5%	Power for Carrier	Micromodule: Processing System
DDR_1V2	OUT	1.2V	+/-5%	Power for Carrier	Micromodule: PS DDR I/O Supply

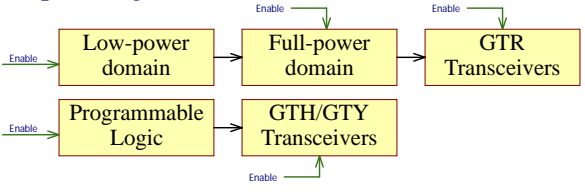
* for Micromodules, where U4 is TPS548A28RWR or MPQ8633BGL-Z maximum Vin range will be 3.3V



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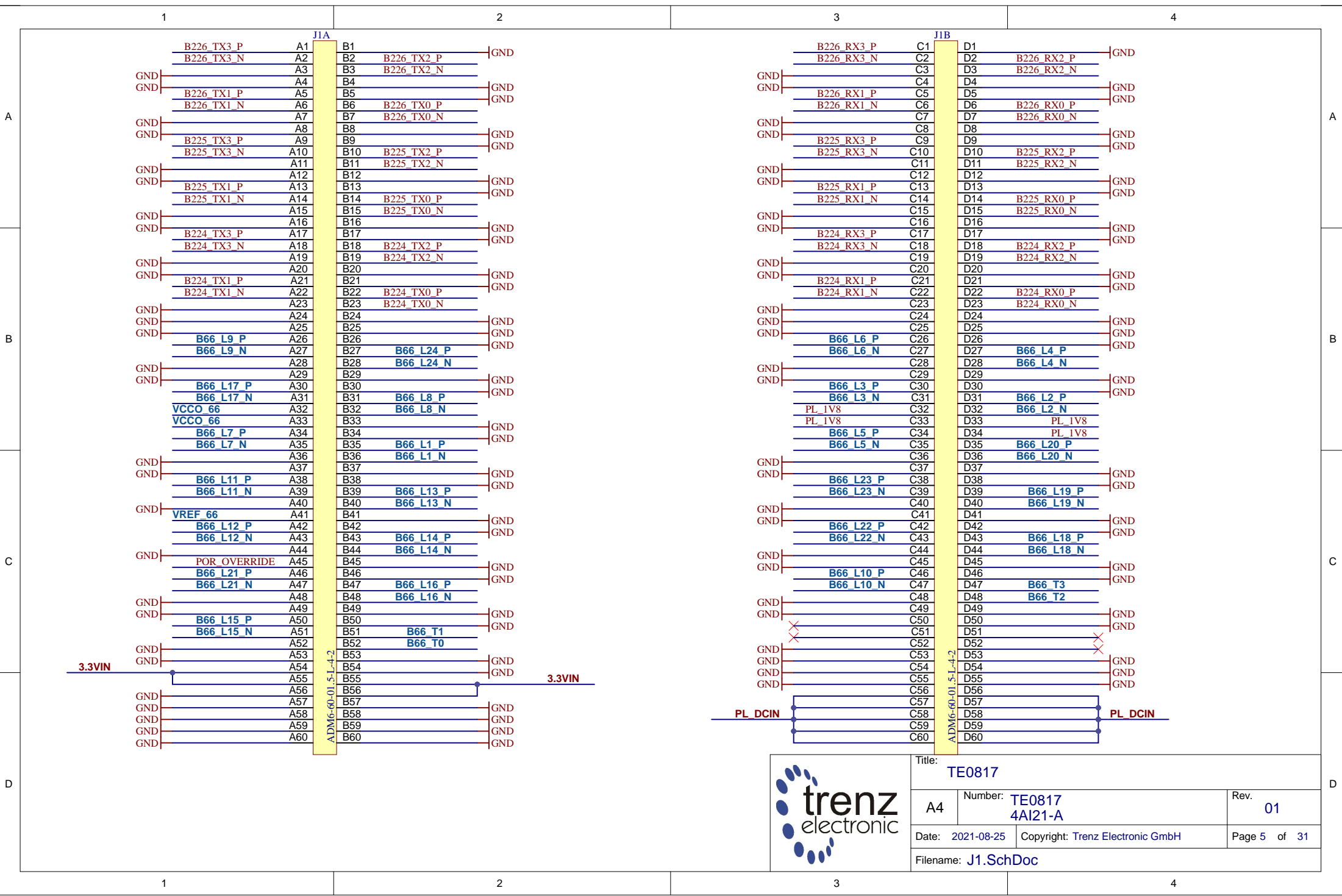
Power-on sequencing:



- EN_GT_R Net name
- Power bus
- Control signal
- Power bus in FPGA speedgrade -1/2/-3 assembly variants
- Power bus in FPGA speedgrade -1L/-2L assembly variants (low power)
- Optional power converter
- Logic AND gate



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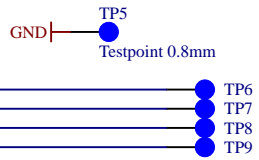
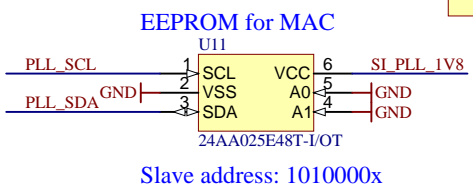
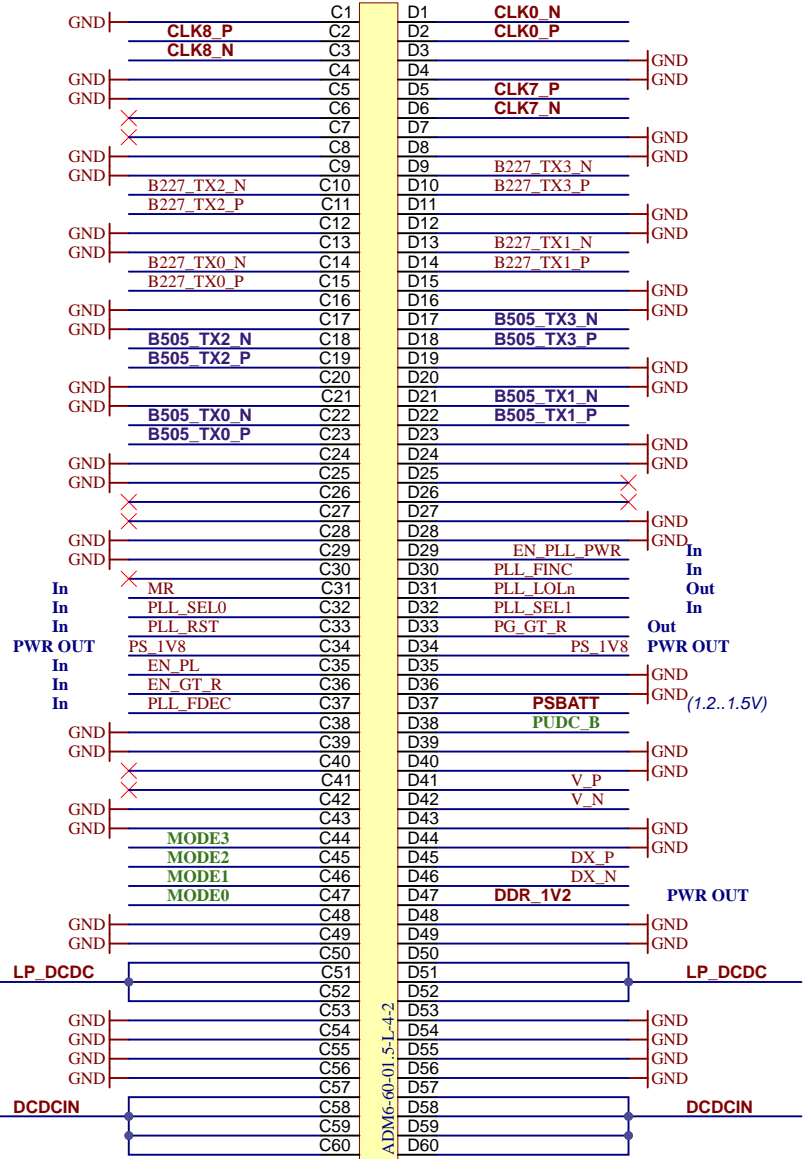
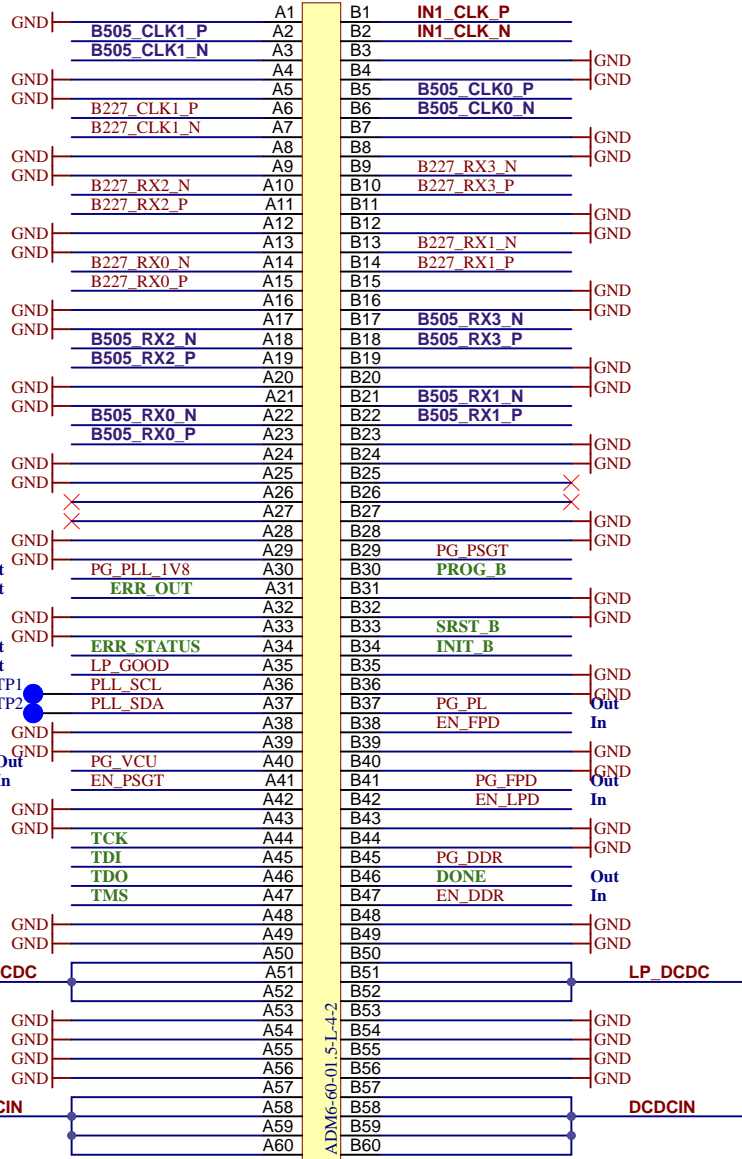
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J2A
ADM6-60-01_5-L-4-2

J2B
ADM6-60-01_5-L-4-2



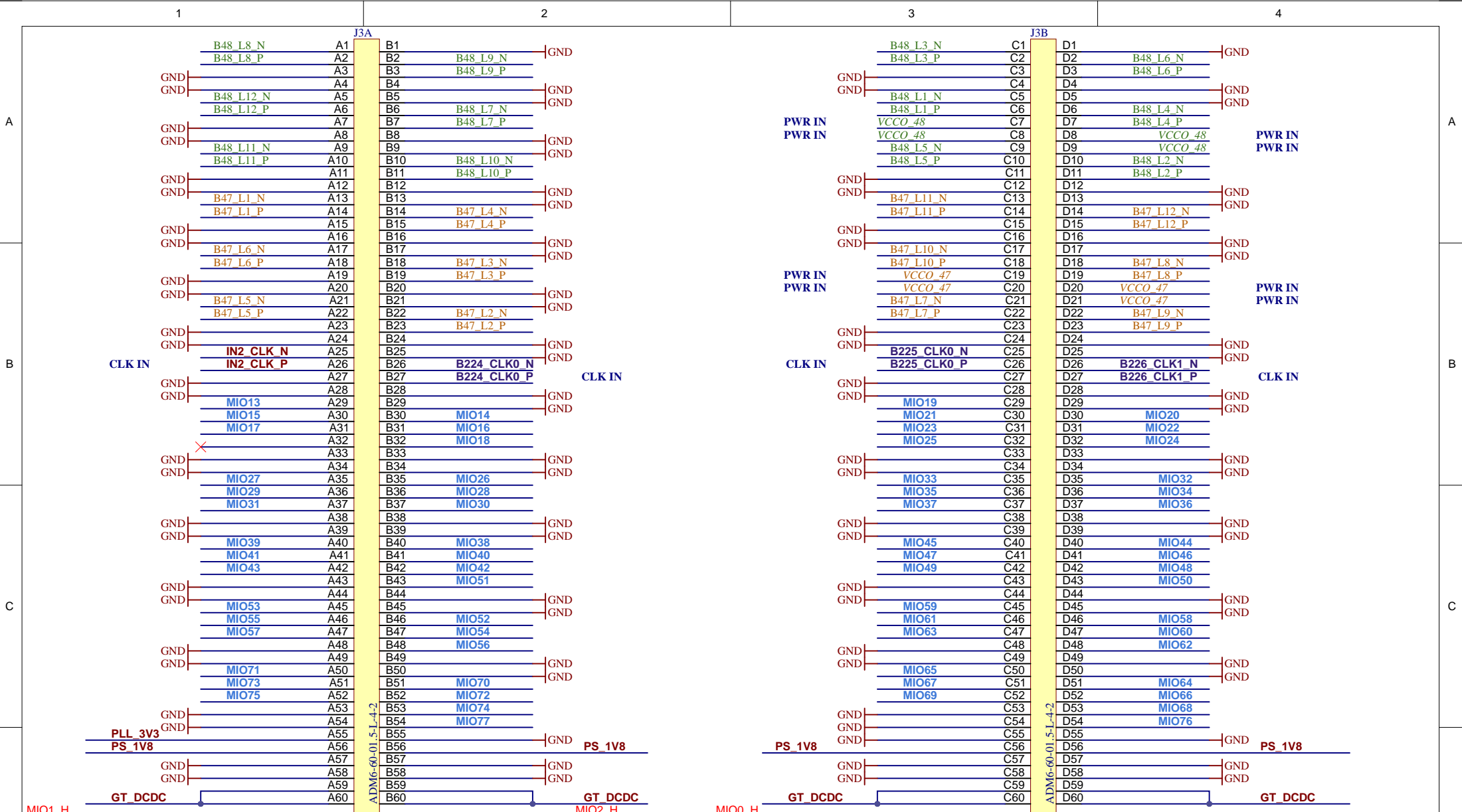
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MIO1_H	MIO1_L	MIO2_L	MIO2_H	MIO0_H
MIO45	MIO38	MIO26	MIO32	MIO64
MIO46	MIO39	MIO27	MIO33	MIO65
MIO47	MIO40	MIO28	MIO34	MIO66
MIO48	MIO41	MIO29	MIO35	MIO67
MIO49	MIO42	MIO30	MIO36	MIO68
MIO50	MIO43	MIO31	MIO37	MIO69
MIO51	MIO44	MIO32	MIO38	MIO70
MIO52	MIO39	MIO52	MIO58	MIO71
MIO53	MIO40	MIO53	MIO59	MIO72
MIO54	MIO41	MIO54	MIO60	MIO73
MIO55	MIO42	MIO55	MIO61	MIO74
MIO56	MIO43	MIO56	MIO62	MIO75
MIO57	MIO44	MIO57	MIO63	MIO76
MIO65	MIO72	MIO65	MIO72	MIO77
MIO66	MIO73	MIO66	MIO73	
MIO67	MIO74	MIO67	MIO74	
MIO68	MIO75	MIO68	MIO75	
MIO69	MIO76	MIO69	MIO76	
MIO70	MIO77	MIO70	MIO77	
MIO13	MIO19	MIO13	MIO19	
MIO14	MIO20	MIO14	MIO20	
MIO15	MIO21	MIO15	MIO21	
MIO16	MIO22	MIO16	MIO22	
MIO17	MIO23	MIO17	MIO23	
MIO18	MIO24	MIO18	MIO24	
MIO19	MIO25	MIO19	MIO25	



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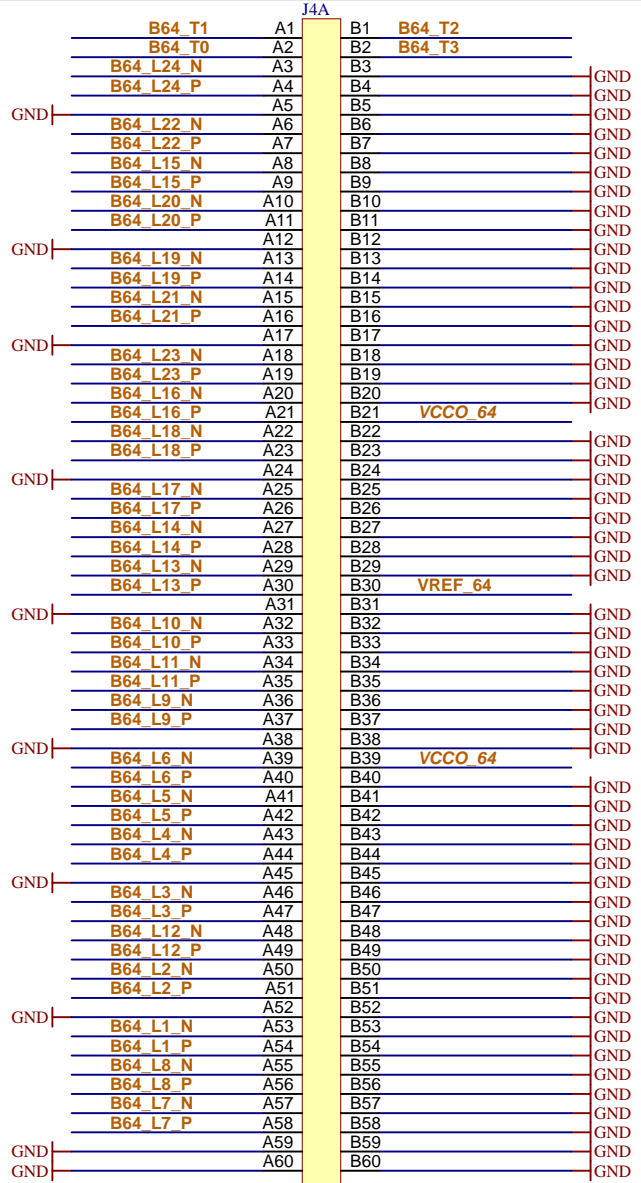
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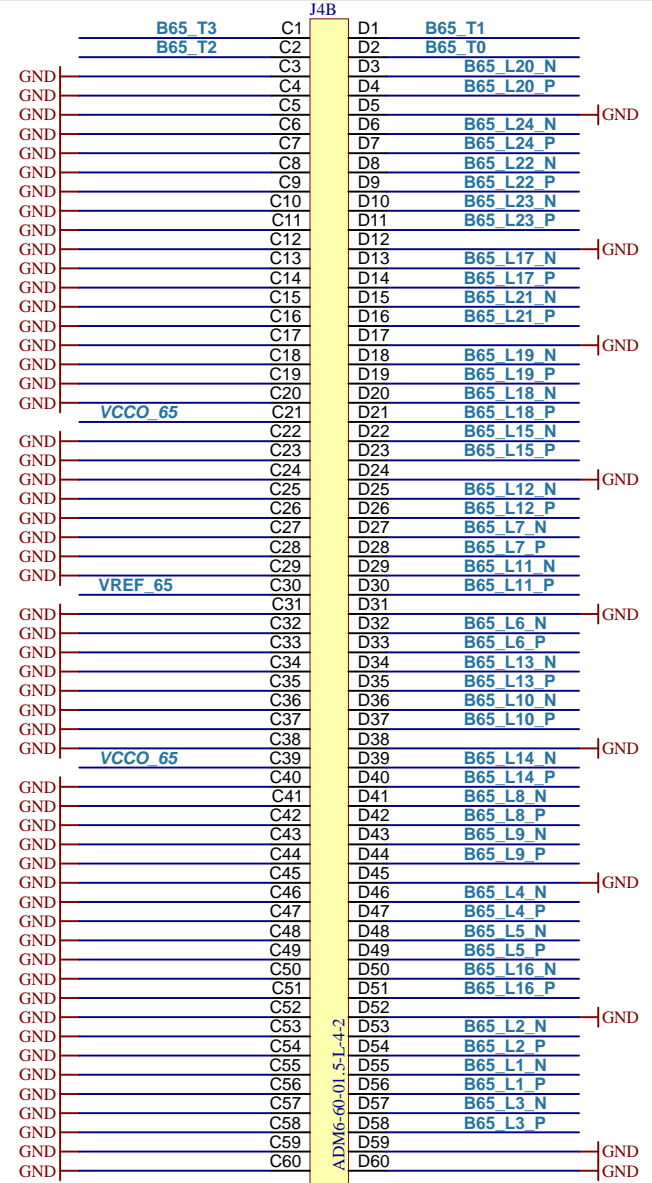
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ADM6-60-01.5-L-4-2



ADM6-60-01.5-L-4-2



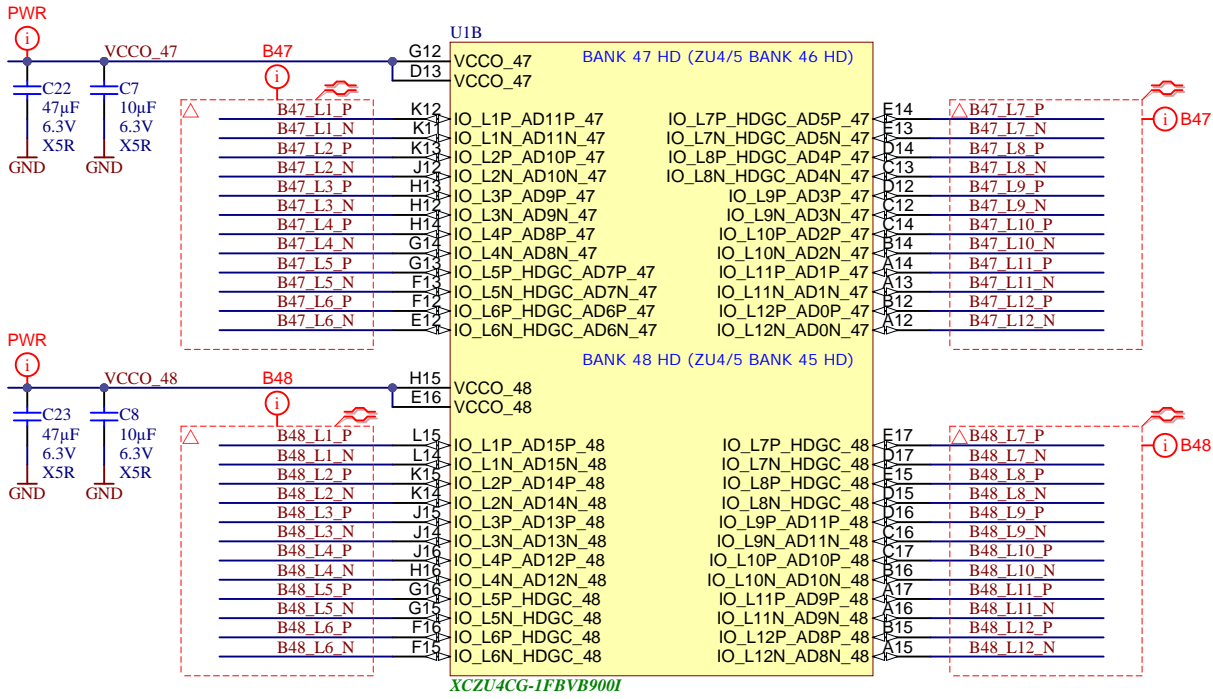
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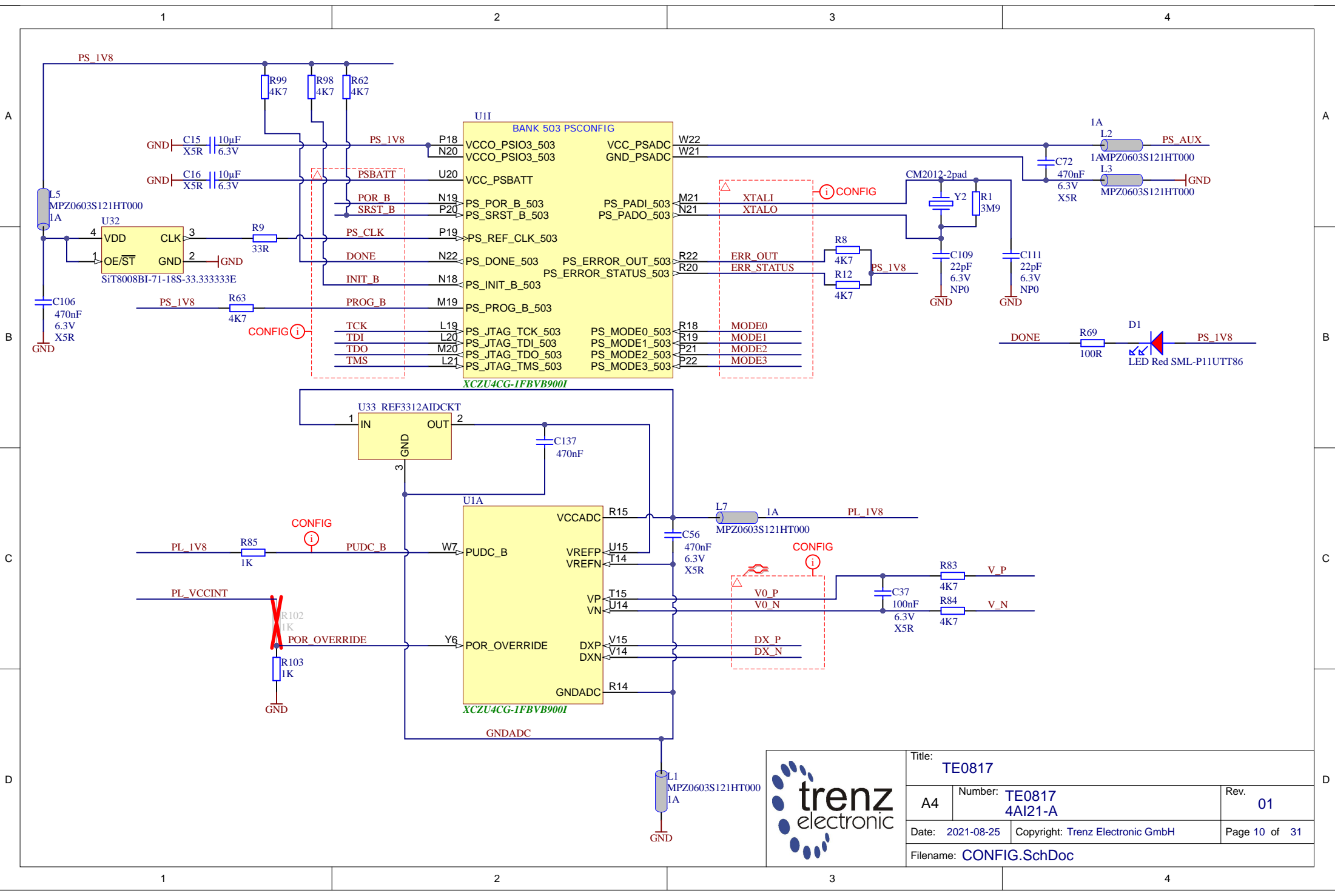
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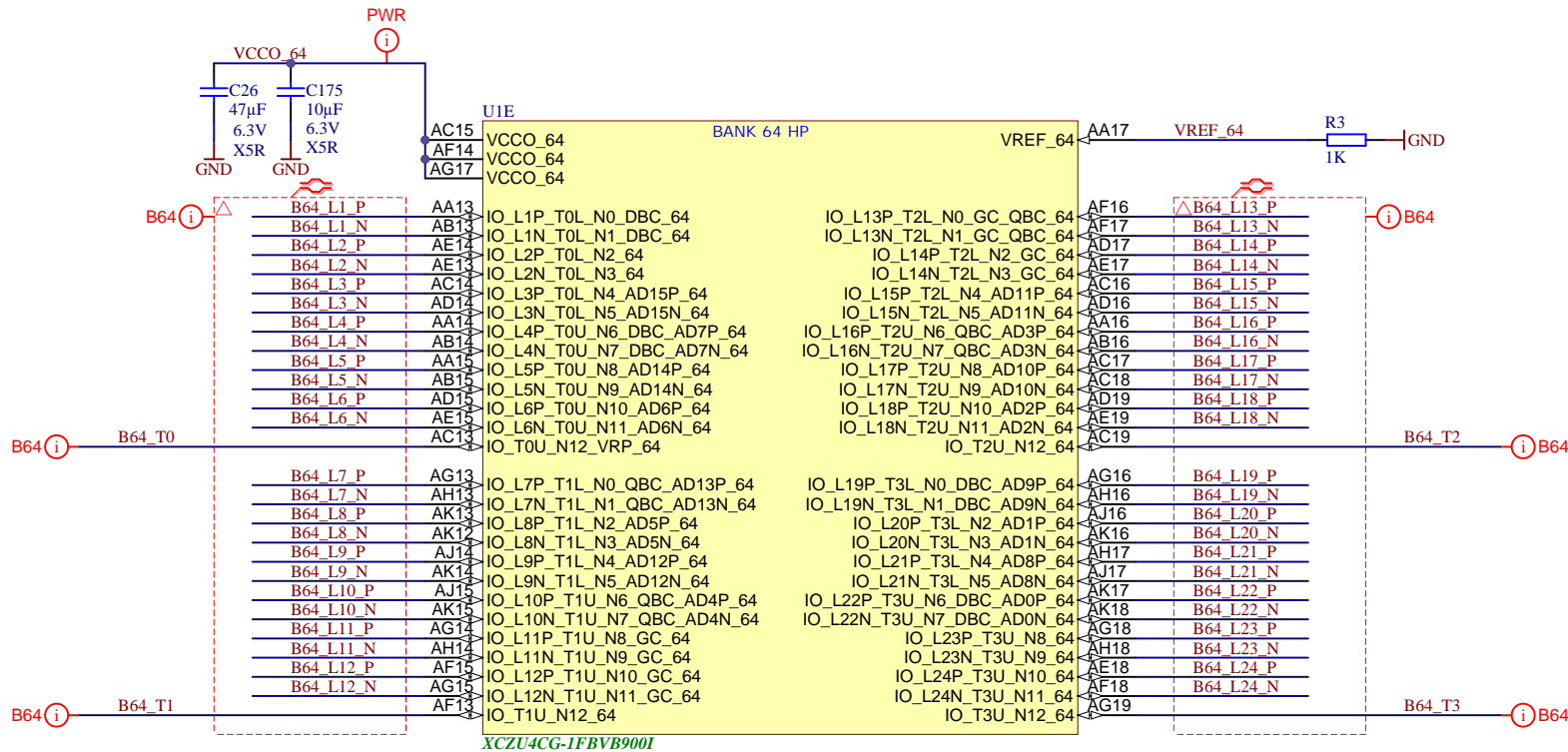
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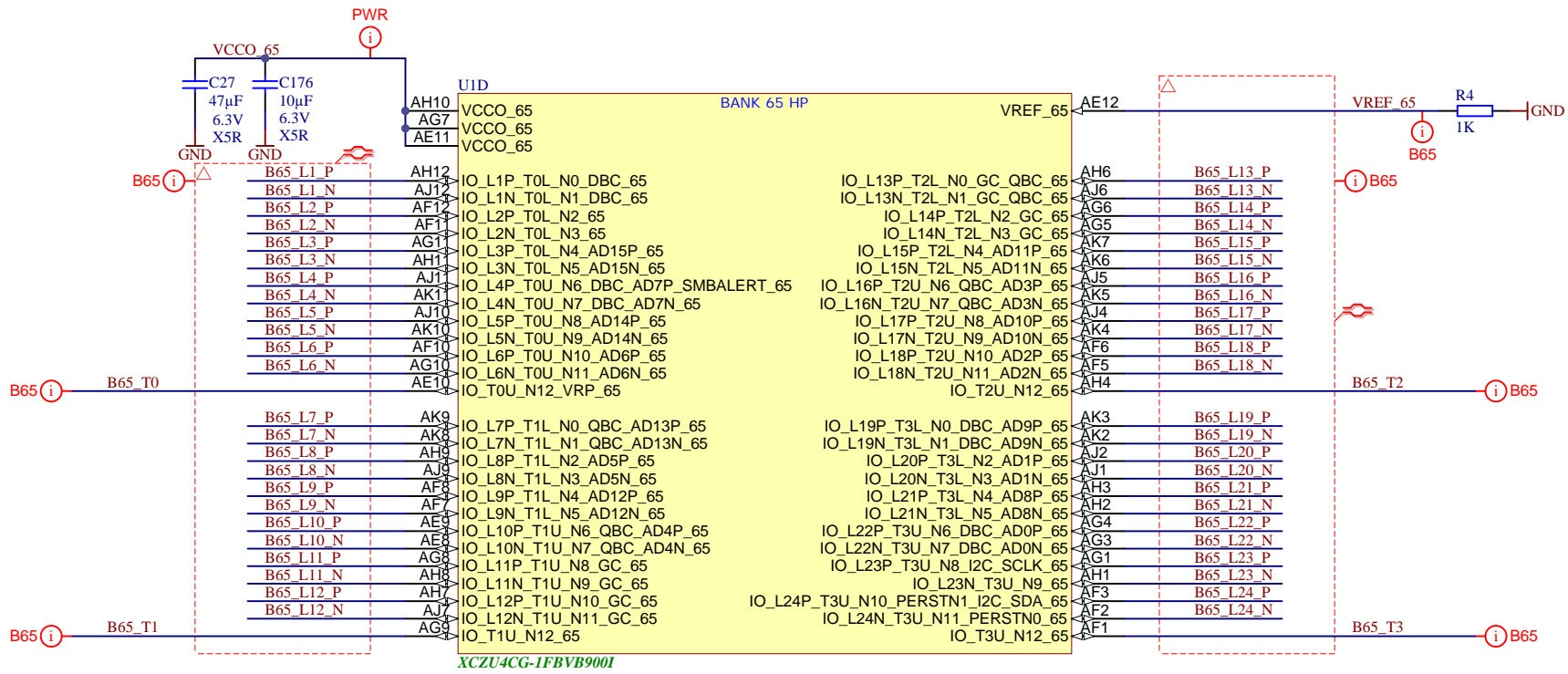
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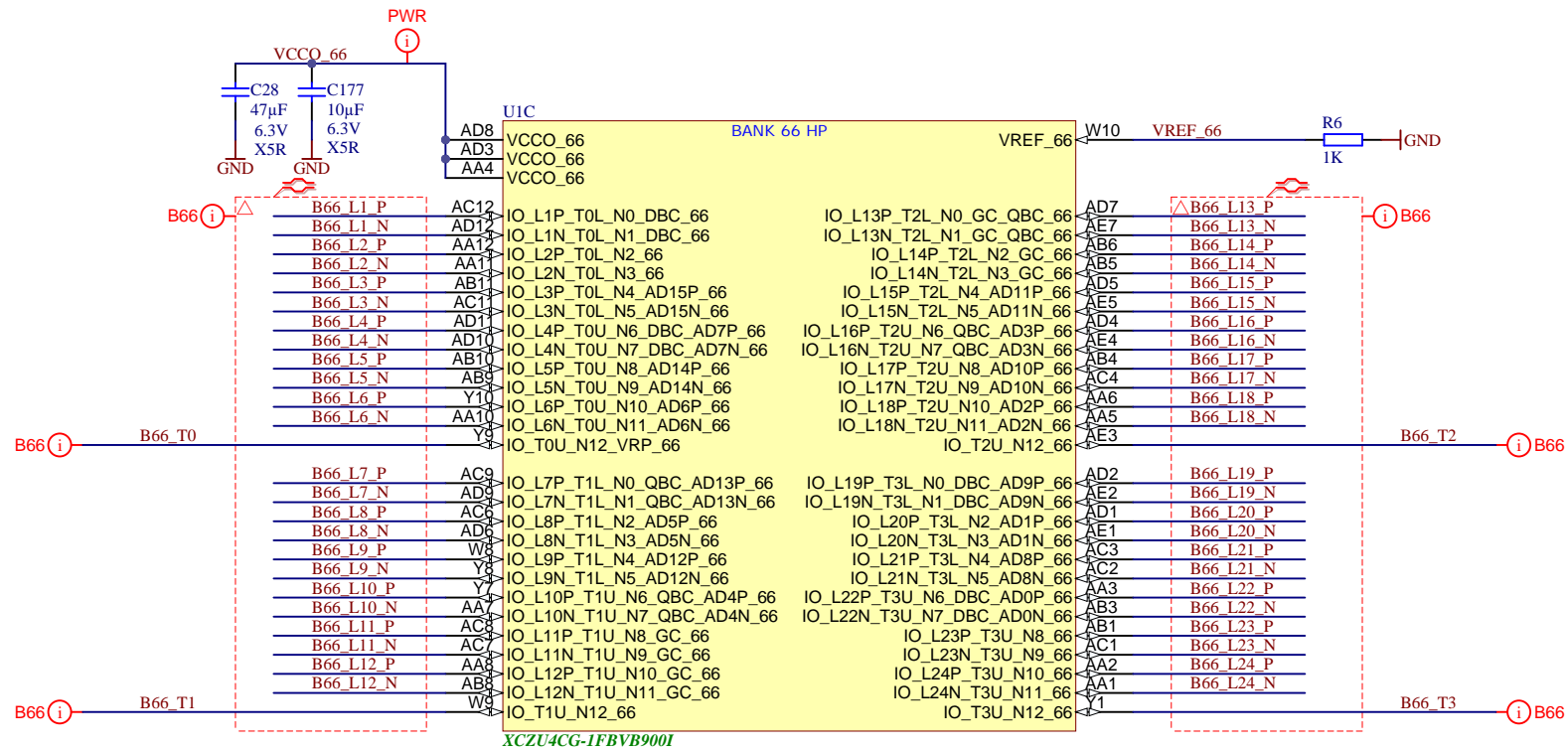
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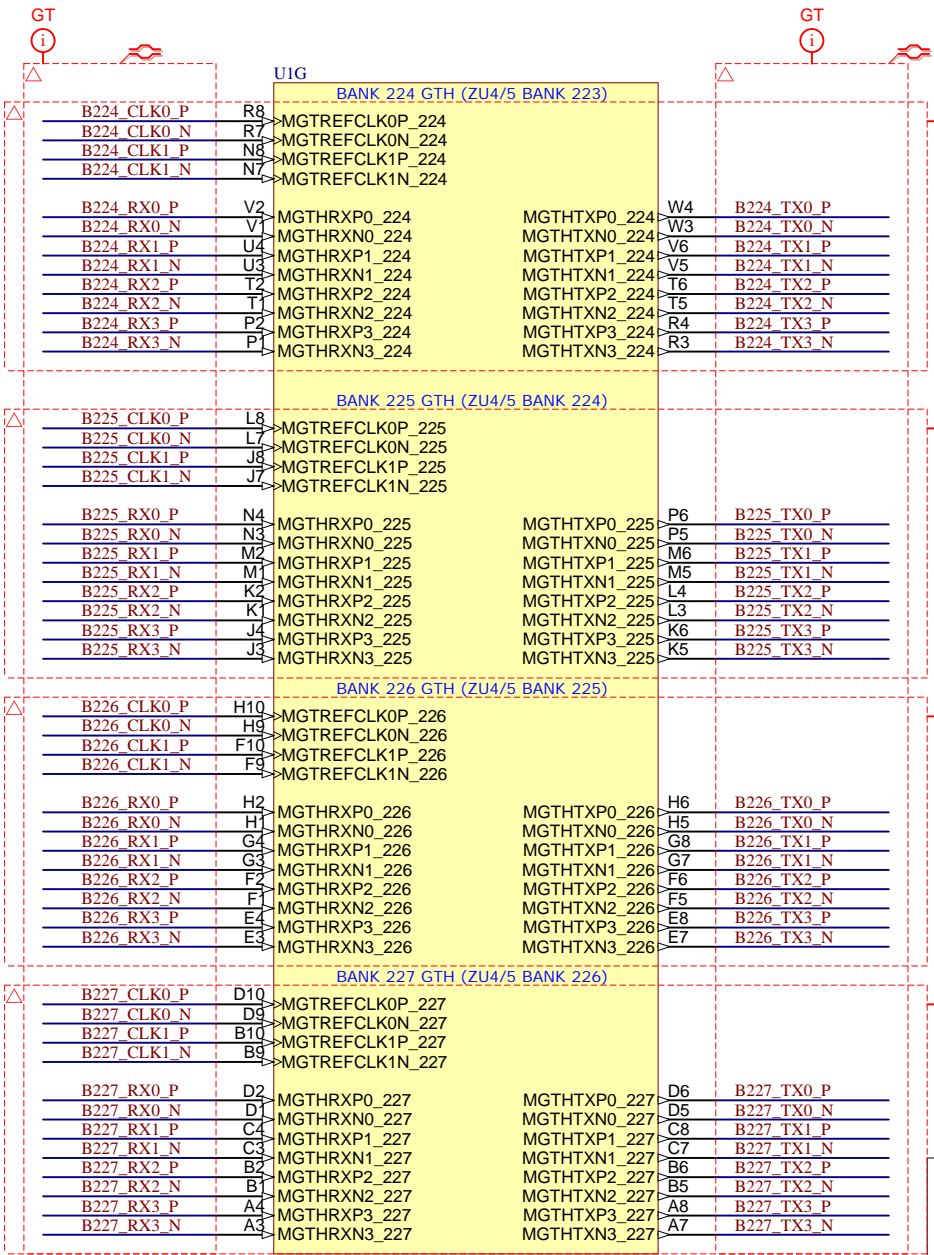
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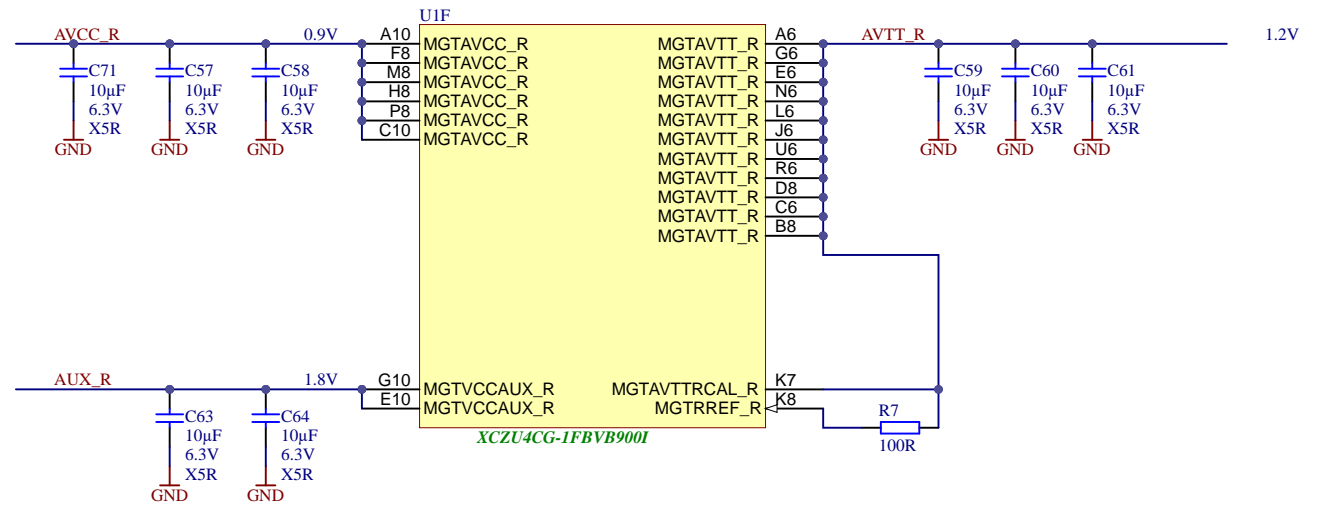
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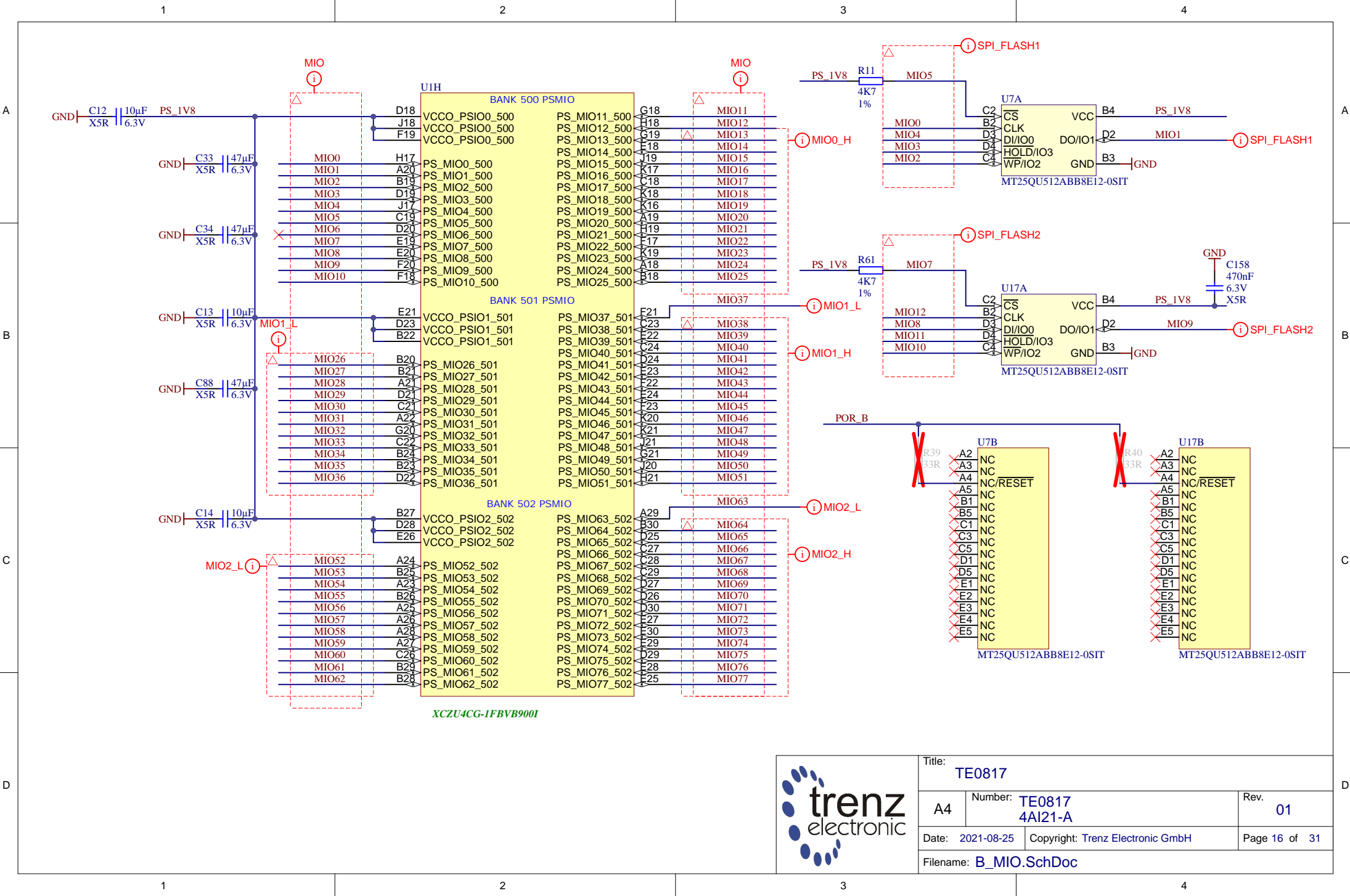
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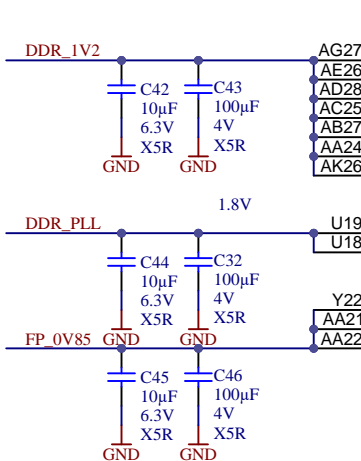
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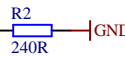
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UIJ
BANK 504 PSDDR

VCCO_PSDDR_504	PS_DDR_CK0_504	AE30	DDR4-CLK0_P
VCCO_PSDDR_504	PS_DDR_CK_NO_504	AF30	DDR4-CLK0_N
VCCO_PSDDR_504	PS_DDR_CKE0_504	AC30	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1_504	AF28	XXXX
VCCO_PSDDR_504	PS_DDR_CK_N1_504	AG28	XXXX
VCCO_PSDDR_504	PS_DDR_CKE1_504	AB28	XXXX
VCC_PSDDR_PLL	PS_DDR_A0_504	AH30	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	AG30	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AK29	DDR4-A2
VCC_PSDDR_PLL	PS_DDR_A3_504	AJ30	DDR4-A3
VCC_PSDDR_PLL	PS_DDR_A4_504	AK28	DDR4-A4
VCC_PSDDR_PLL	PS_DDR_A5_504	AK27	DDR4-A5
VCC_PSDDR_PLL	PS_DDR_A6_504	AF27	DDR4-A6
VCC_PSDDR_PLL	PS_DDR_A7_504	AE27	DDR4-A7
VCC_PSDDR_PLL	PS_DDR_A8_504	AF26	DDR4-A8
VCC_PSDDR_PLL	PS_DDR_A9_504	AG26	DDR4-A9
VCC_PSDDR_PLL	PS_DDR_A10_504	AE29	DDR4-A10
VCC_PSDDR_PLL	PS_DDR_A11_504	AE28	DDR4-A11
VCC_PSDDR_PLL	PS_DDR_A12_504	AH29	DDR4-A12
VCC_PSDDR_PLL	PS_DDR_A13_504	AH28	DDR4-A13
VCC_PSDDR_PLL	PS_DDR_A14_504	AG29	DDR4-A14
VCC_PSDDR_PLL	PS_DDR_A15_504	AJ29	DDR4-A15
VCC_PSDDR_PLL	PS_DDR_A16_504	AH27	DDR4-A16
VCC_PSDDR_PLL	PS_DDR_A17_504	AJ27	DDR4-A17
PS_DDR_CS_NO_504	PS_DDR_CS_N1_504	AD30	DDR4-CS
PS_DDR_CS_NO_504	PS_DDR_CS_N1_504	AD29	XXXX
PS_DDR_BA0_504	PS_DDR_BA1_504	AD27	DDR4-BA0
PS_DDR_BA0_504	PS_DDR_BA1_504	AC26	DDR4-BA1
PS_DDR_BG0_504	PS_DDR_BG1_504	AC28	DDR4-BG0
PS_DDR_BG0_504	PS_DDR_BG1_504	AC27	DDR4-BG1
PS_DDR_PARITY_504	PS_DDR_RAM_RST_N_504	AB26	DDR4-PAR
PS_DDR_ACT_N_504	PS_DDR_ALERT_N_504	AB25	DDR4-RESET
PS_DDR_ACT_N_504	PS_DDR_ALERT_N_504	AD26	DDR4-ACT
PS_DDR_ACT_N_504	PS_DDR_ALERT_N_504	AB24	DDR4-ALERT
PS_DDR_ZQ_504	PS_DDR_ODT0_504	AB23	DDR4-ODT0
PS_DDR_ZQ_504	PS_DDR_ODT1_504	AC29	XXXX

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UIK
BANK 504 PSDDR

DQ0	AH22	PS_DDR_DQ0_504	PS_DDR_DQ32_504
DQ1	AH21	PS_DDR_DQ1_504	PS_DDR_DQ33_504
DQ2	AJ21	PS_DDR_DQ2_504	PS_DDR_DQ34_504
DQ3	AK21	PS_DDR_DQ3_504	PS_DDR_DQ35_504
DQ4	AK20	PS_DDR_DQ4_504	PS_DDR_DQ36_504
DQ5	AJ19	PS_DDR_DQ5_504	PS_DDR_DQ37_504
DQ6	AK19	PS_DDR_DQ6_504	PS_DDR_DQ38_504
DQ7	AH18	PS_DDR_DQ7_504	PS_DDR_DQ39_504
DQ8	AH23	PS_DDR_DQ8_504	PS_DDR_DQ40_504
DQ9	AK23	PS_DDR_DQ9_504	PS_DDR_DQ41_504
DQ10	AG24	PS_DDR_DQ10_504	PS_DDR_DQ42_504
DQ11	AK24	PS_DDR_DQ11_504	PS_DDR_DQ43_504
DQ12	AJ26	PS_DDR_DQ12_504	PS_DDR_DQ44_504
DQ13	AK25	PS_DDR_DQ13_504	PS_DDR_DQ45_504
DQ14	AG25	PS_DDR_DQ14_504	PS_DDR_DQ46_504
DQ15	AH26	PS_DDR_DQ15_504	PS_DDR_DQ47_504
DQ16	AD27	PS_DDR_DQ16_504	PS_DDR_DQ48_504
DQ17	AE27	PS_DDR_DQ17_504	PS_DDR_DQ49_504
DQ18	AF27	PS_DDR_DQ18_504	PS_DDR_DQ50_504
DQ19	AG27	PS_DDR_DQ19_504	PS_DDR_DQ51_504
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DQ23	AG20	PS_DDR_DQ23_504	PS_DDR_DQ55_504
DQ24	AG23	PS_DDR_DQ24_504	PS_DDR_DQ56_504
DQ25	AF23	PS_DDR_DQ25_504	PS_DDR_DQ57_504
DQ26	AF23	PS_DDR_DQ26_504	PS_DDR_DQ58_504
DQ27	AE23	PS_DDR_DQ27_504	PS_DDR_DQ59_504
DQ28	AC23	PS_DDR_DQ28_504	PS_DDR_DQ60_504
DQ29	AC23	PS_DDR_DQ29_504	PS_DDR_DQ61_504
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DDR4-DQS2_P	AC21	PS_DDR_DQS_P2_504	PS_DDR_DQ68_504
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DDR4-DQS3_P	AD21	PS_DDR_DQS_P3_504	PS_DDR_DQ70_504
DDR4-DQS3_N	AE21	PS_DDR_DQS_N3_504	PS_DDR_DQ71_504
DDR4-DQS4_P	W21	PS_DDR_DQS_P4_504	PS_DDR_DM0_504
DDR4-DQS4_N	W25	PS_DDR_DQS_N4_504	PS_DDR_DM1_504
DDR4-DQS5_P	P25	PS_DDR_DQS_P5_504	PS_DDR_DM2_504
DDR4-DQS5_N	R25	PS_DDR_DQS_N5_504	PS_DDR_DM3_504
DDR4-DQS6_P	U29	PS_DDR_DQS_P6_504	PS_DDR_DM4_504
DDR4-DQS6_N	V29	PS_DDR_DQS_N6_504	PS_DDR_DM5_504
DDR4-DQS7_P	R28	PS_DDR_DQS_P7_504	PS_DDR_DM6_504
DDR4-DQS7_N	R29	PS_DDR_DQS_N7_504	PS_DDR_DM7_504
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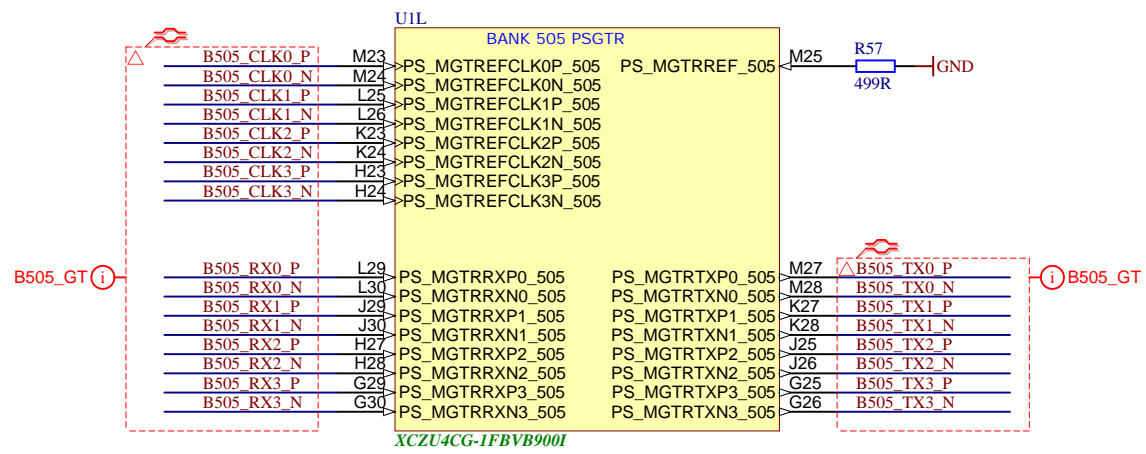
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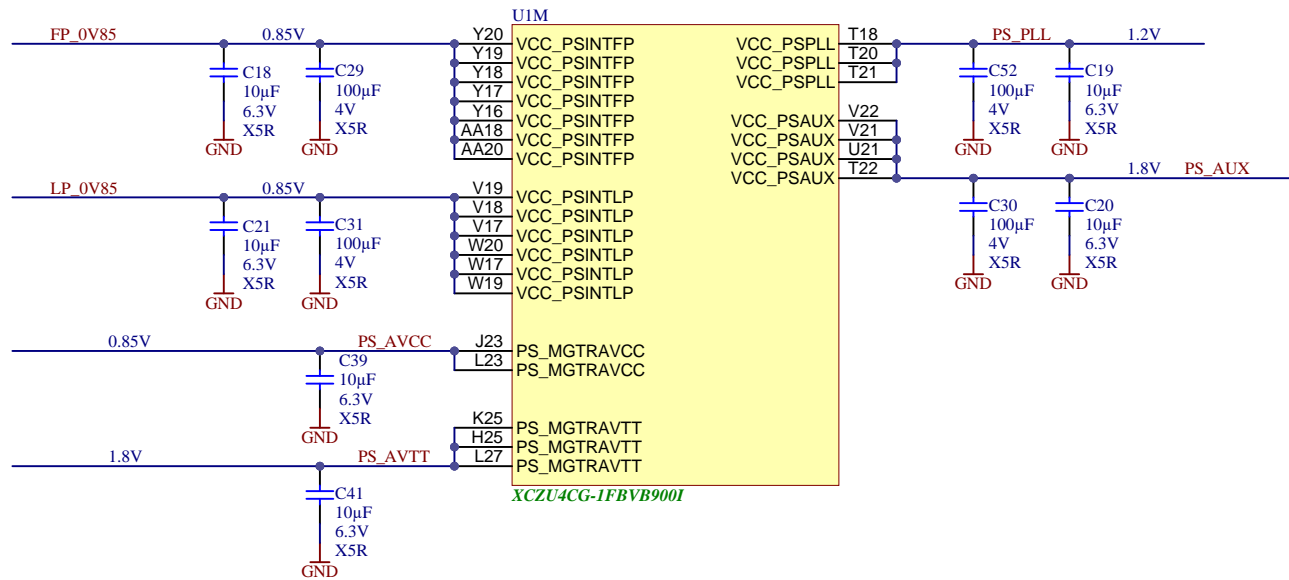
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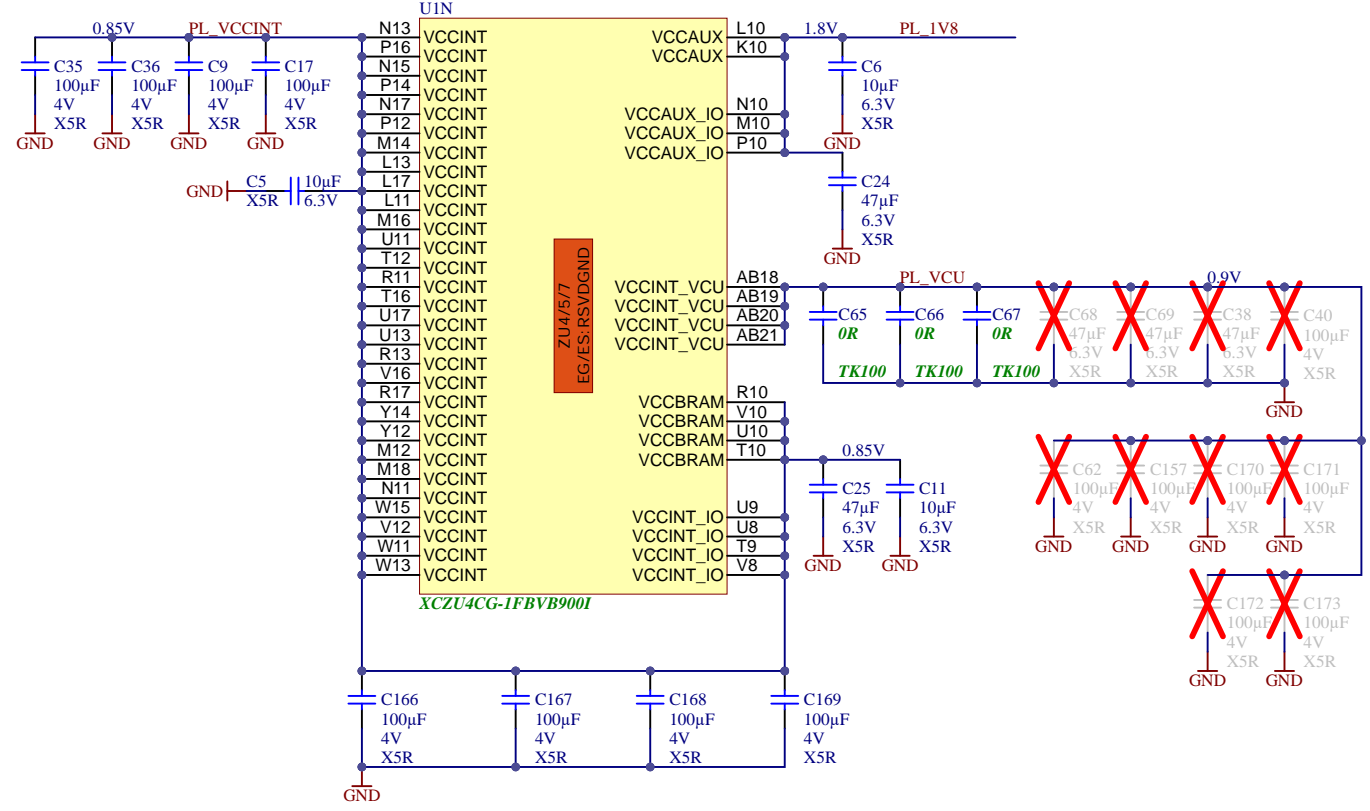
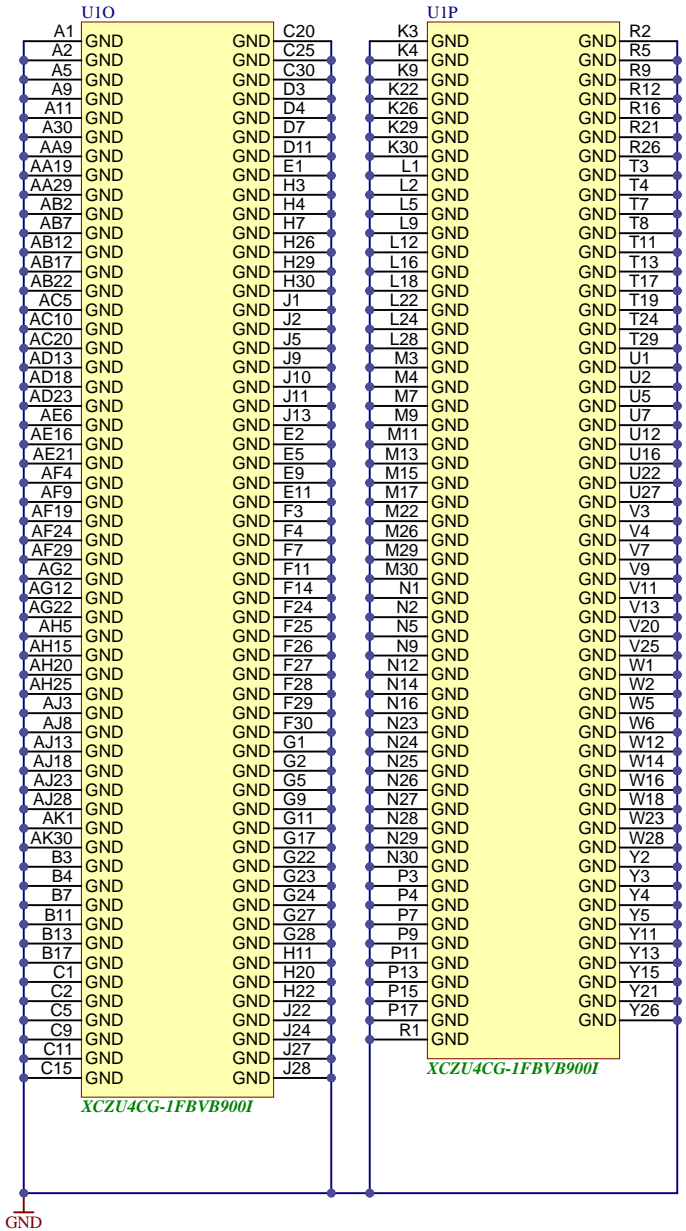
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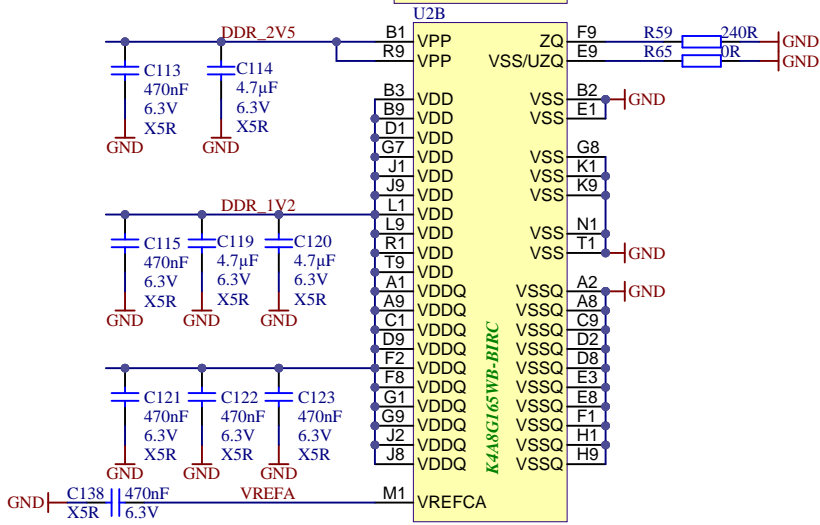
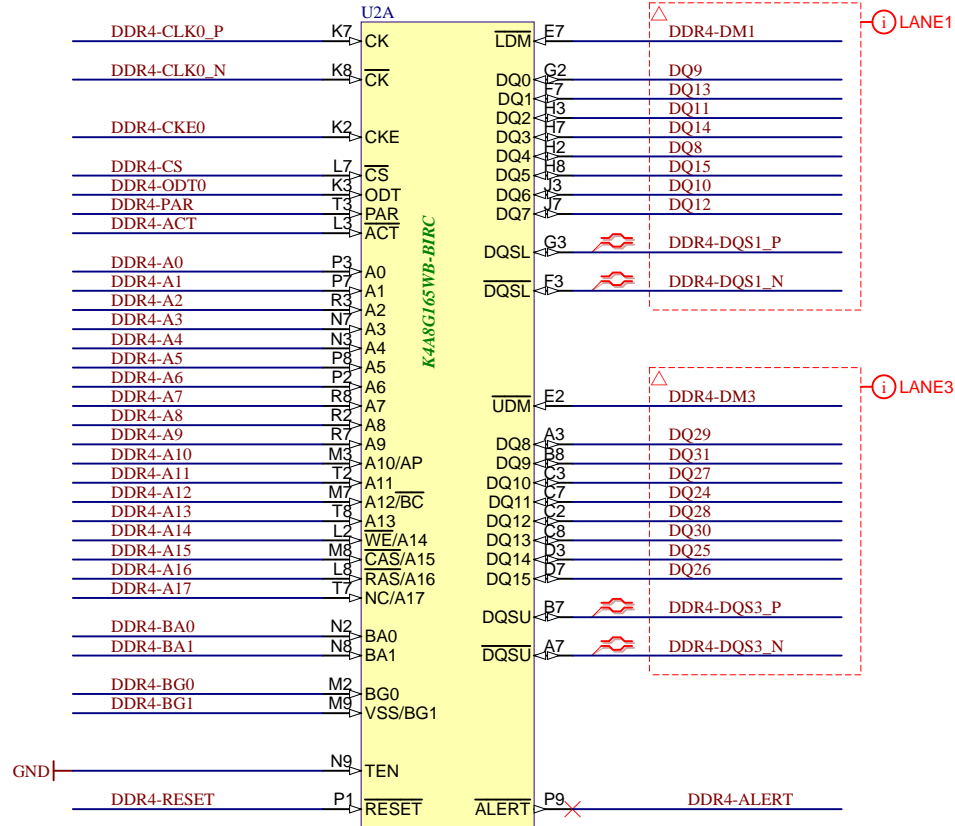
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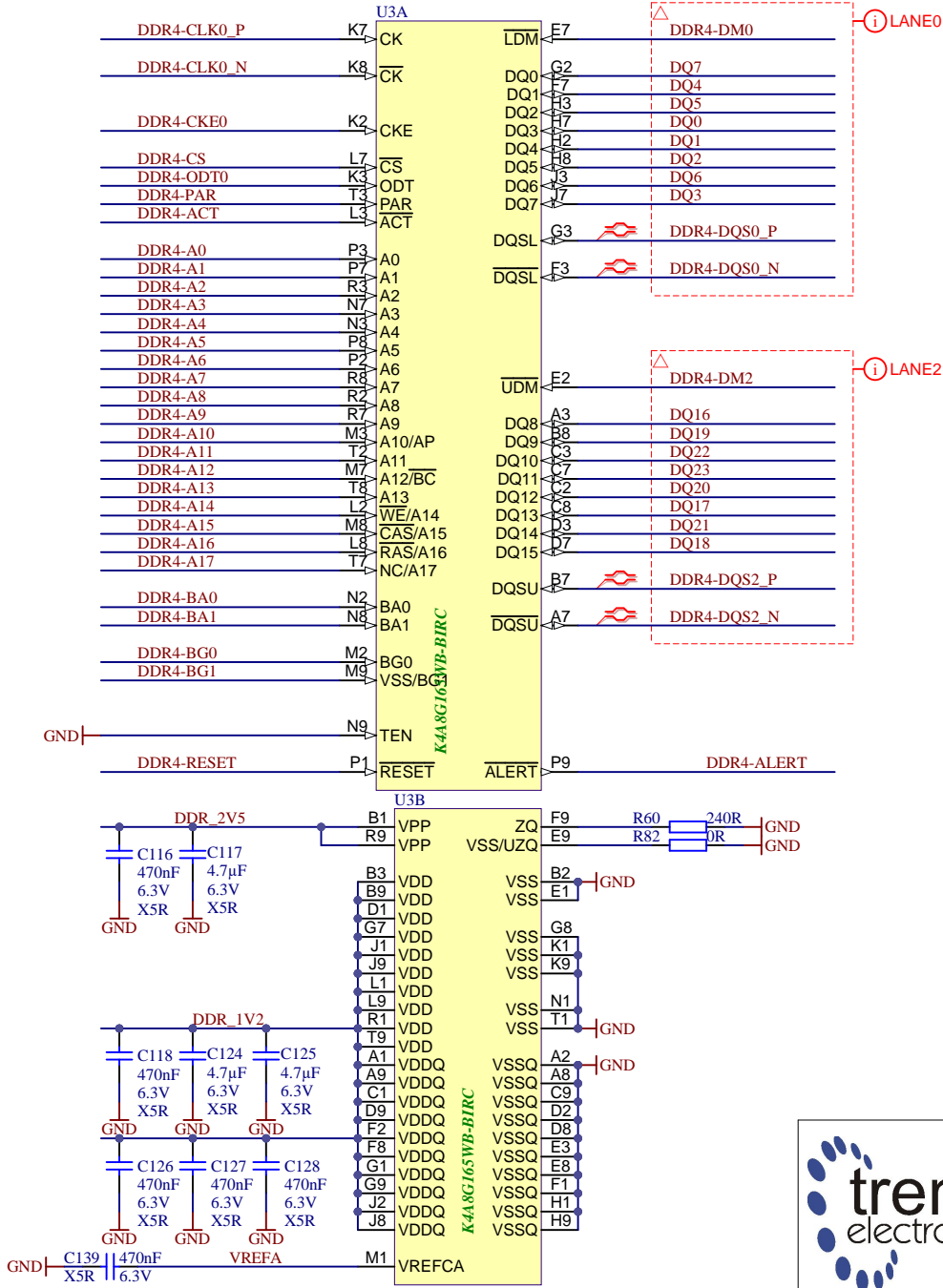
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Filename: ZU_PS_POWER.SchDoc			



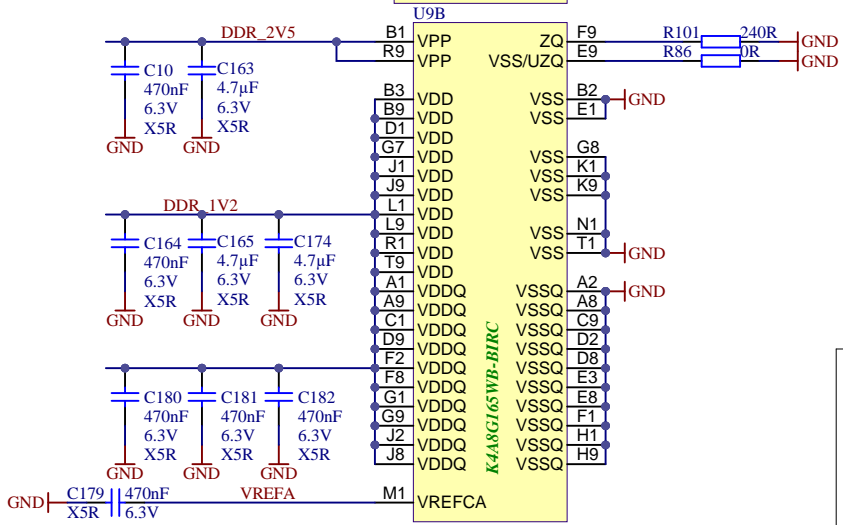
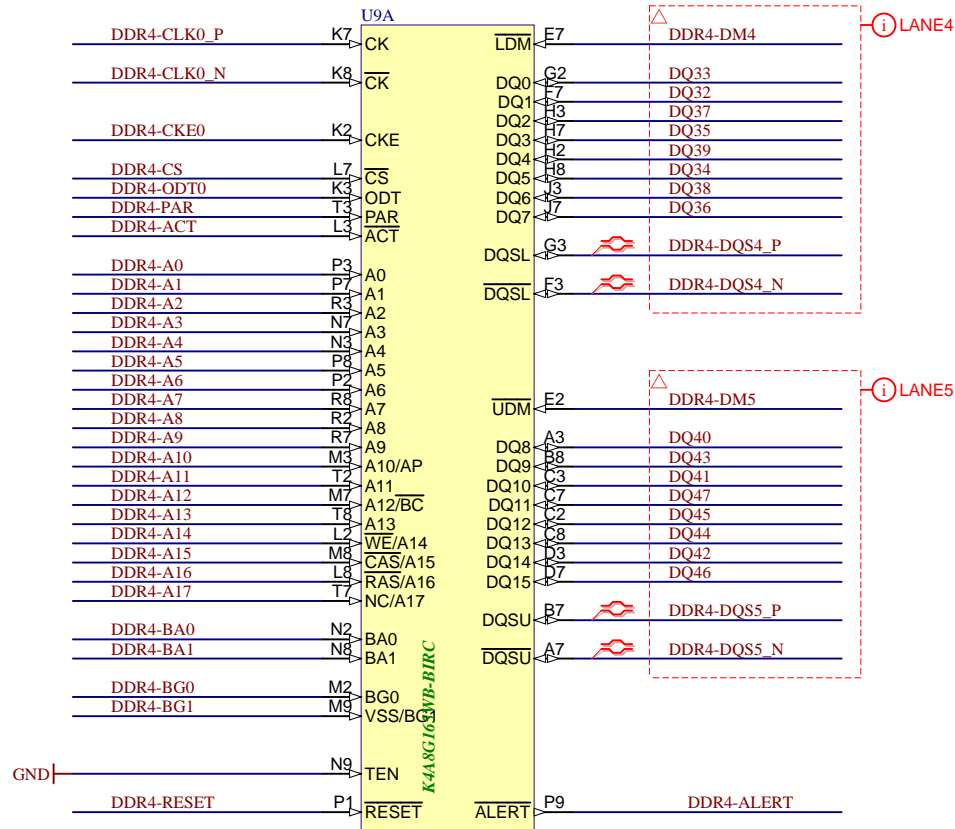
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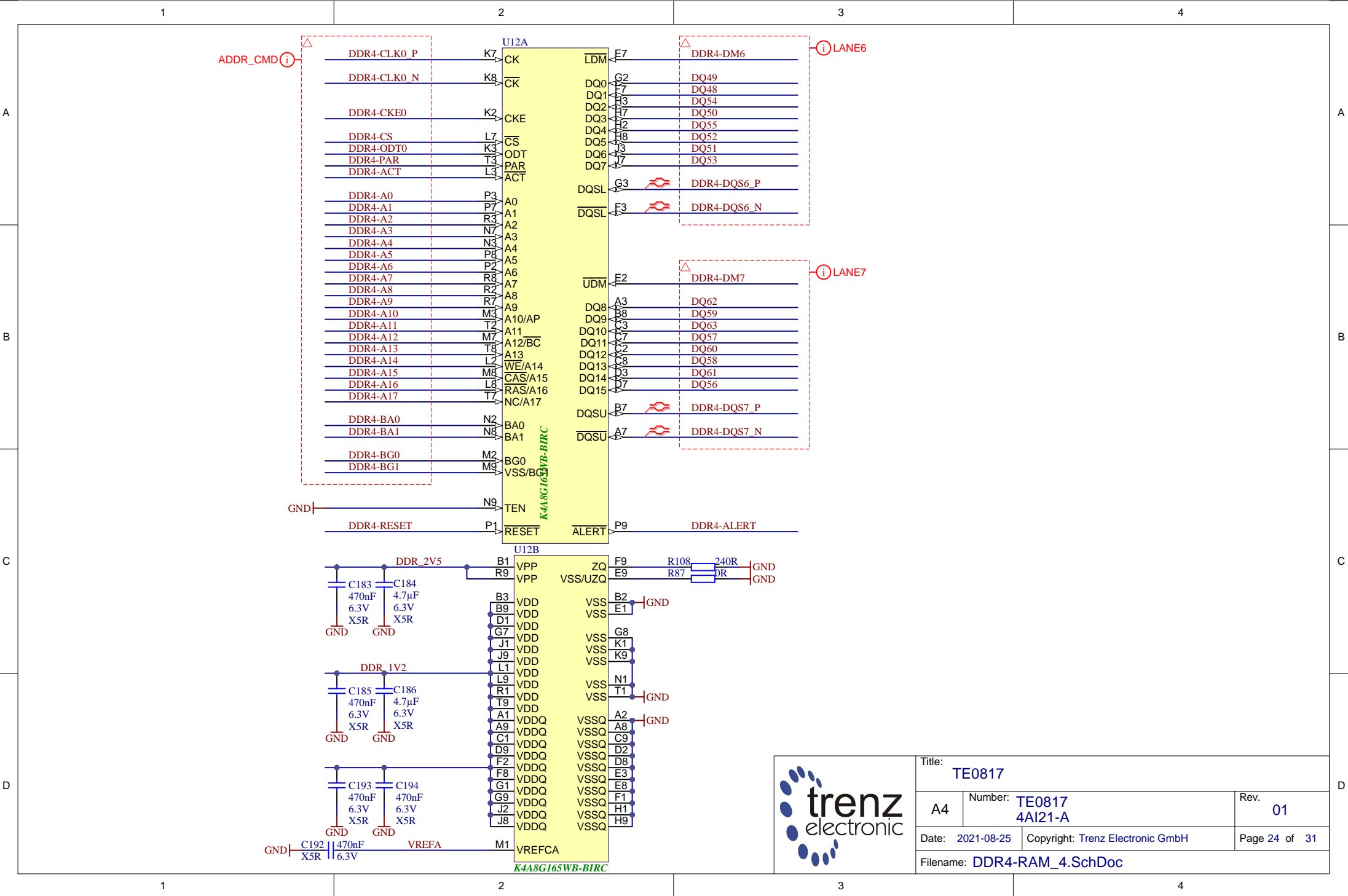
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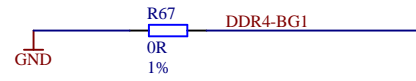
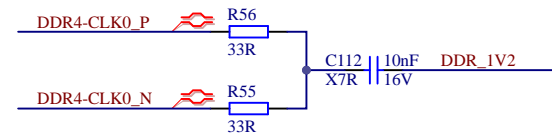
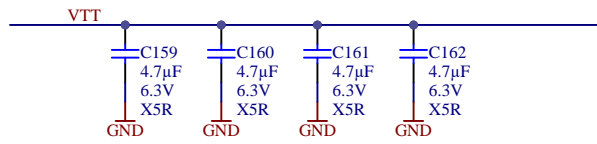
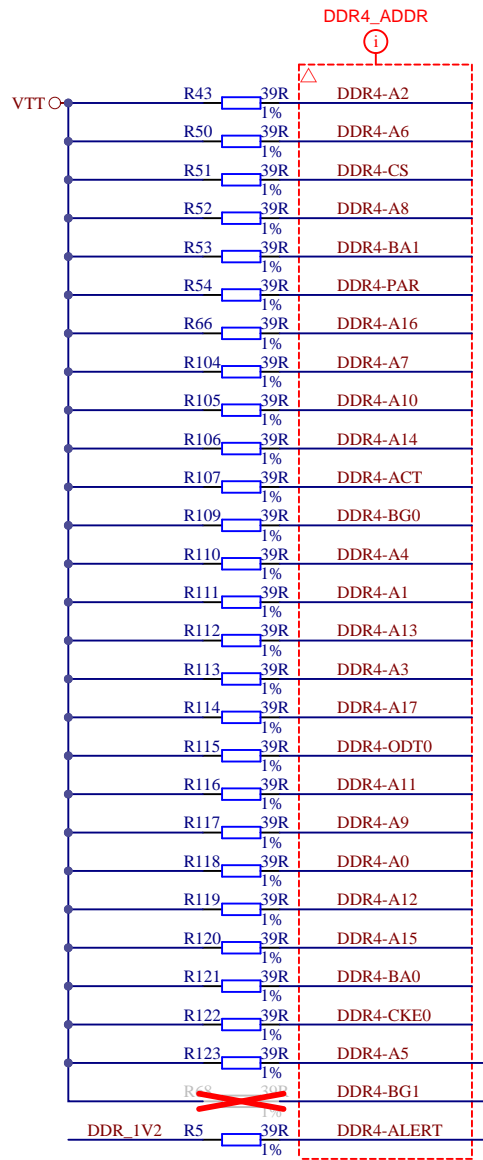
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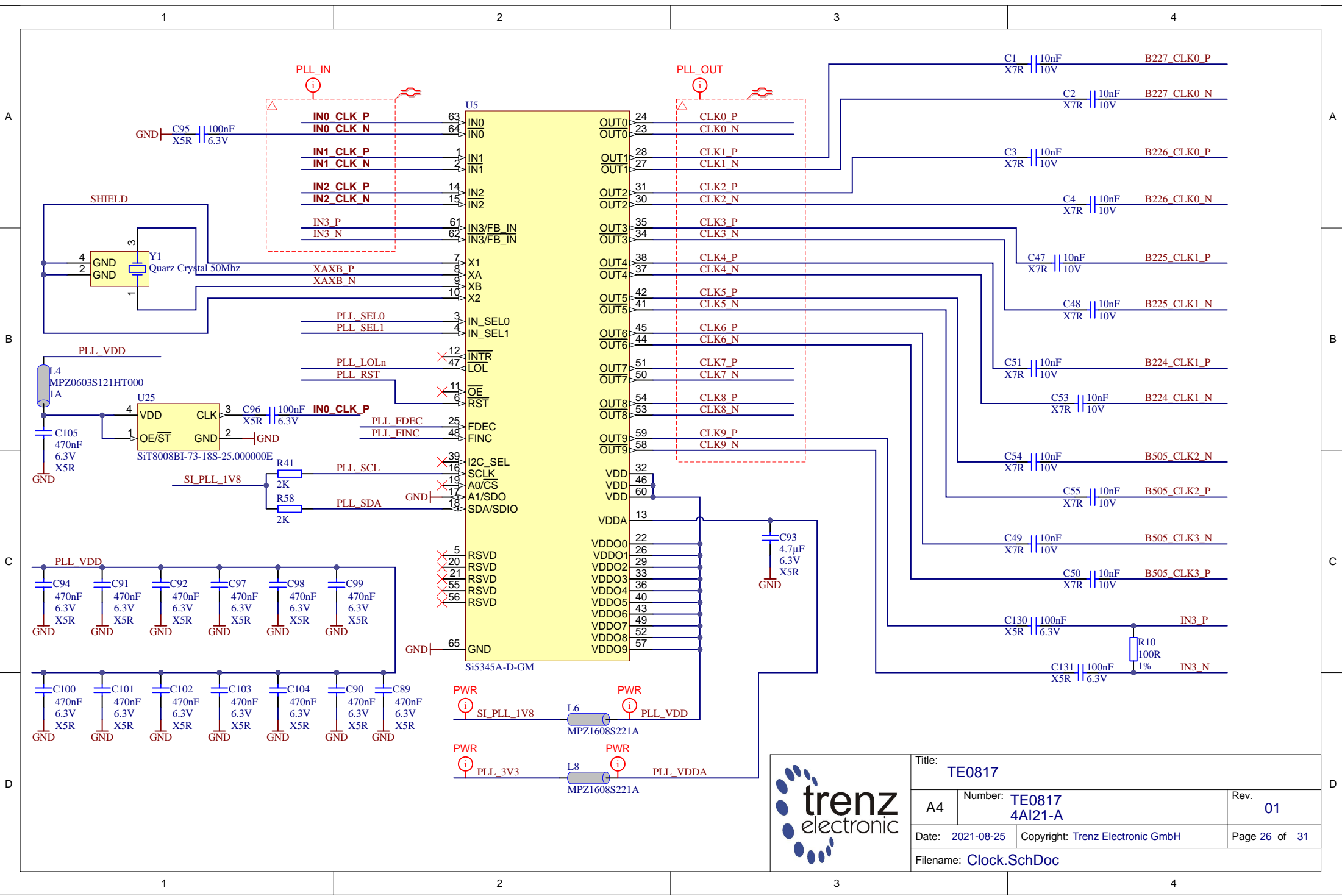
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Filename: DDR4-RAM_3.SchDoc		



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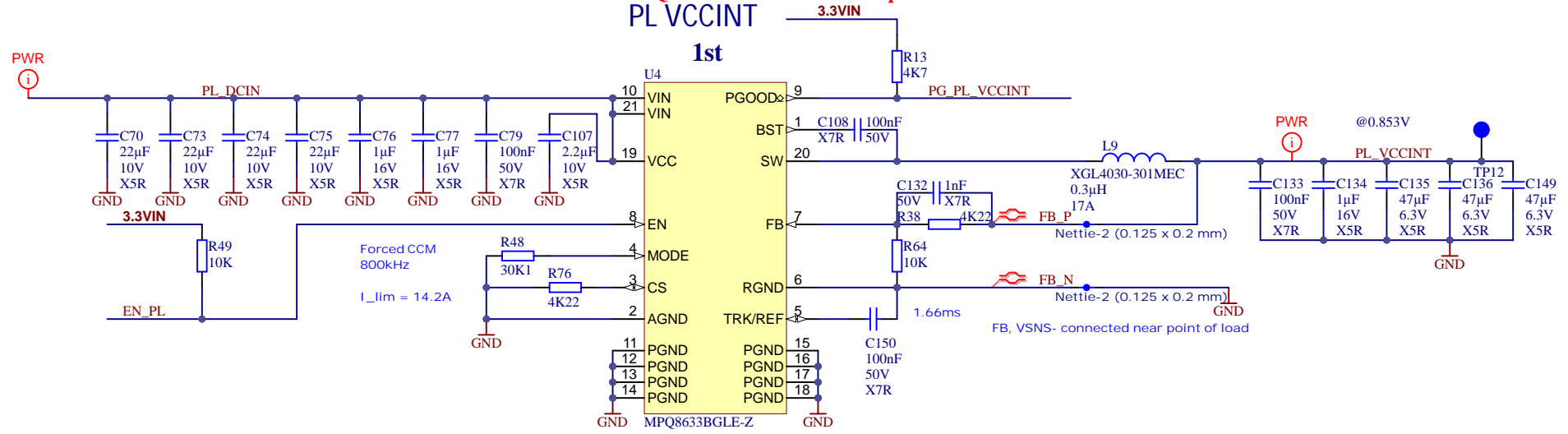


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Filename: DDR4-TERM.SchDoc		

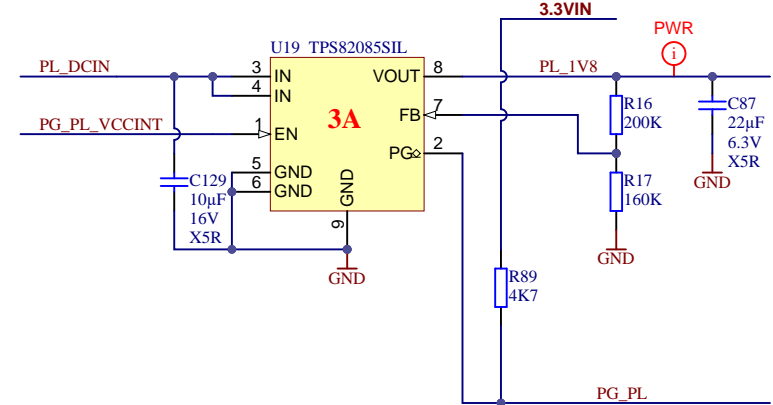
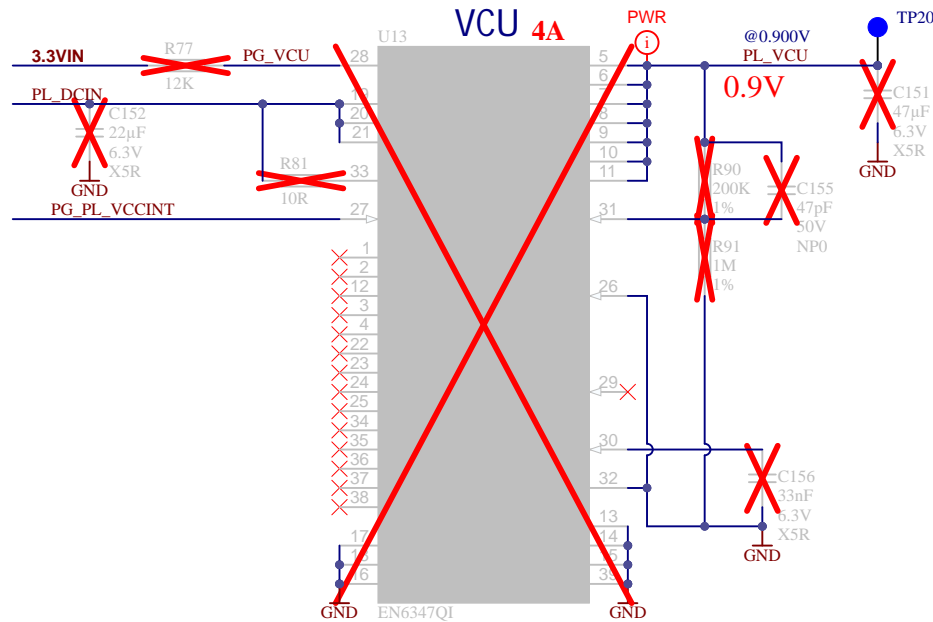



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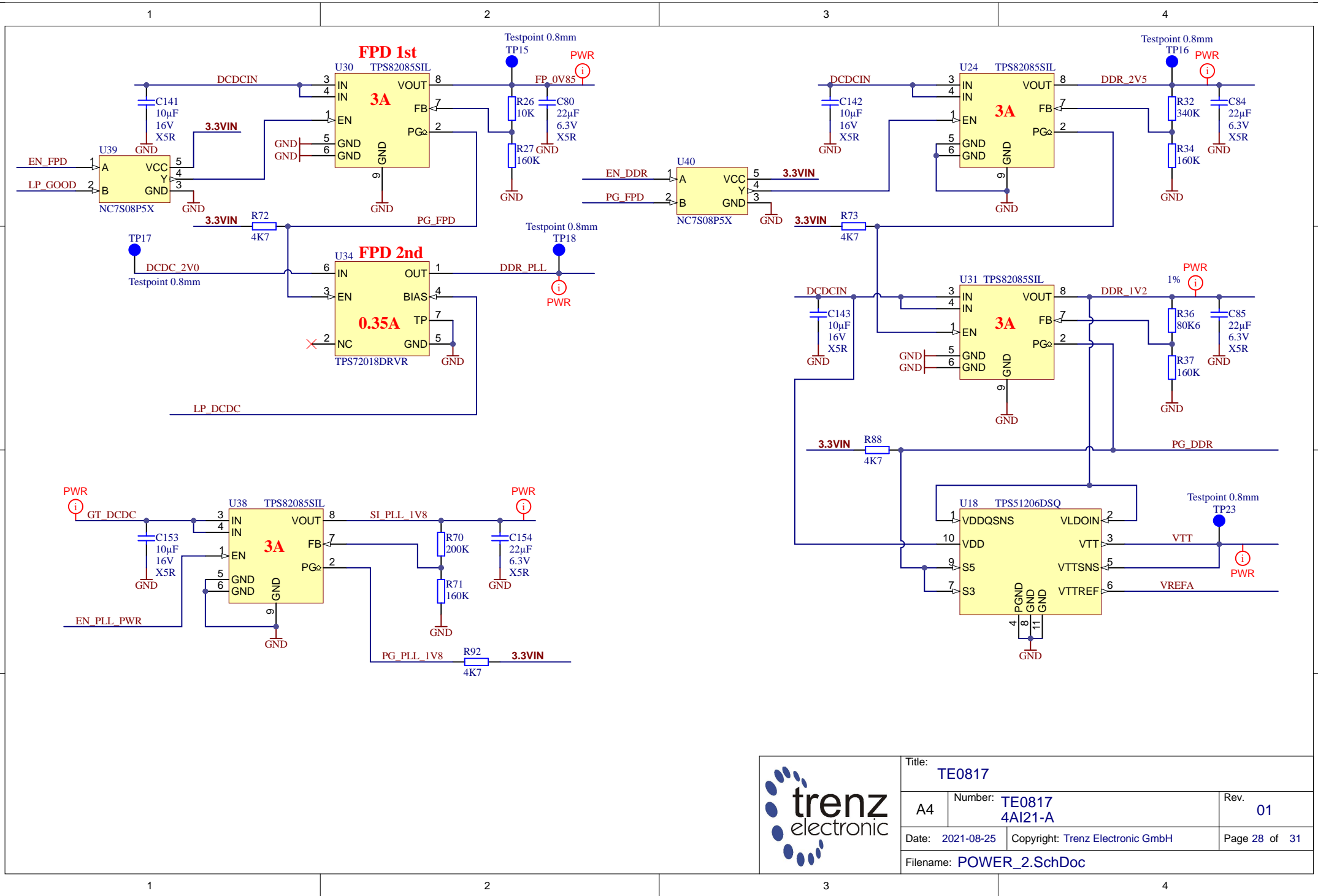
U4 can be TPS548A28RWWR or MPQ8633BGLE-Z which is up to Trenz Electronic GmbH.




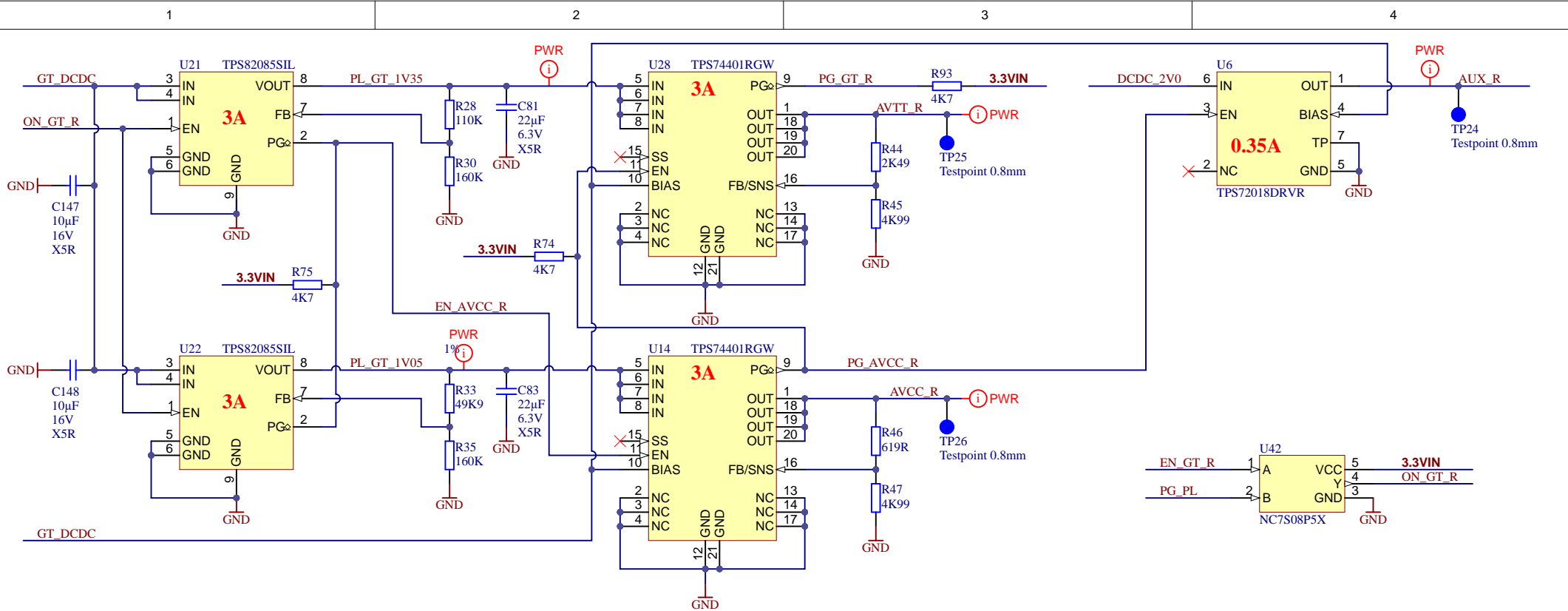
U4 pin compatible with
 -- TPS54JA20 (12A)
 -- TPS548A28 (15A)
 -- TPS548B28 (20A)



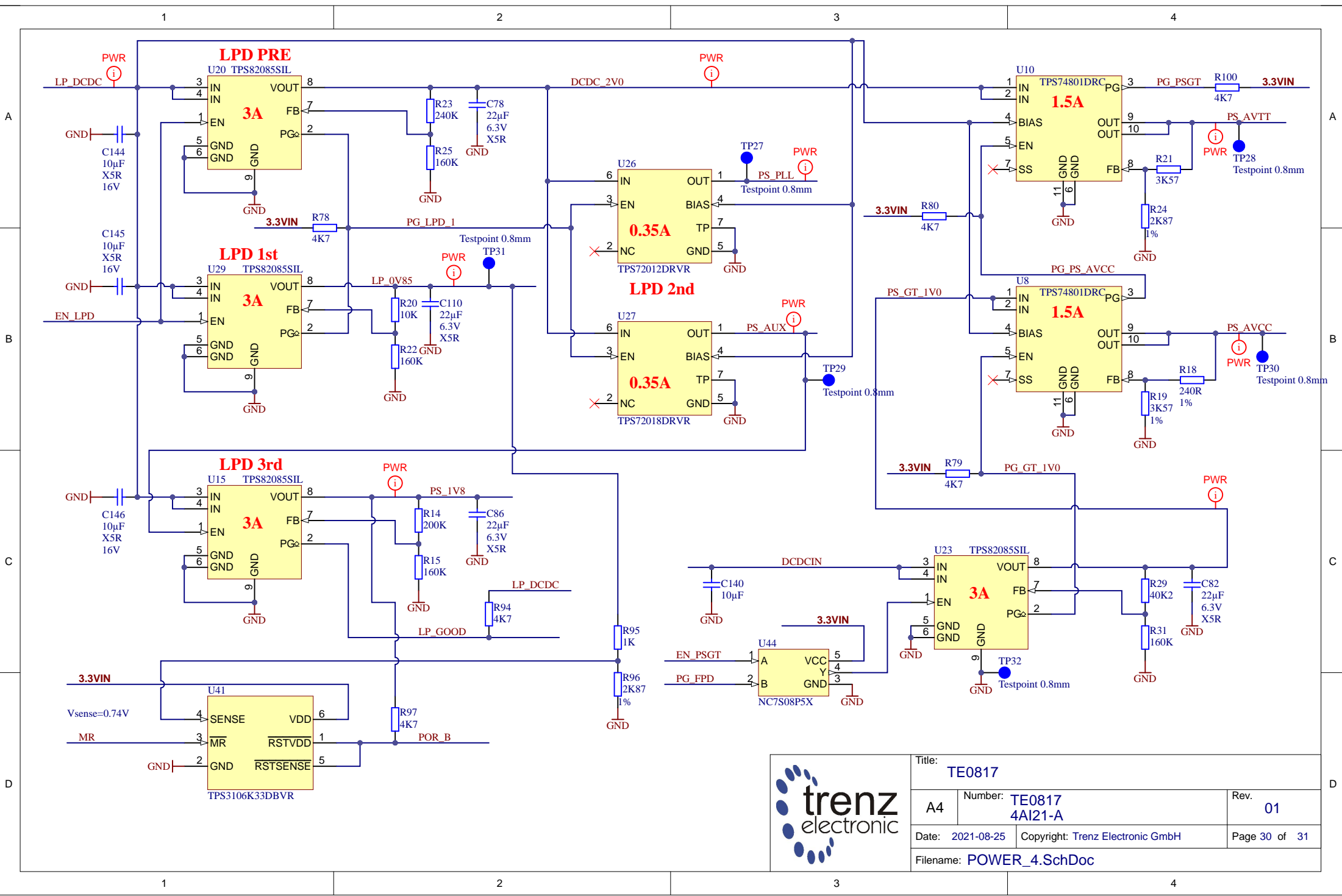
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REV	DATE	Description	
-01	2021-05	Initial revision	VT
	2022-05	Changed DCDC U4 TPS548A28 to MPQ8633BGLE-Z Changed C132 100nF to 1nF	
	2022-11	Added Table with Supported Voltage Ranges	

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