


Regarding the usage of our schematics and alike documentation for Trenz module TE0817.

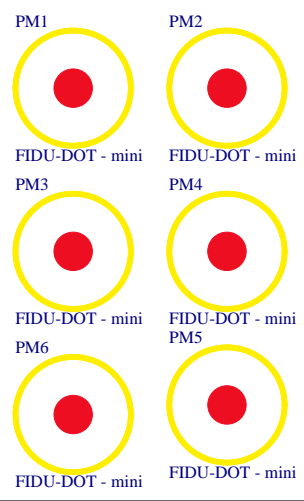
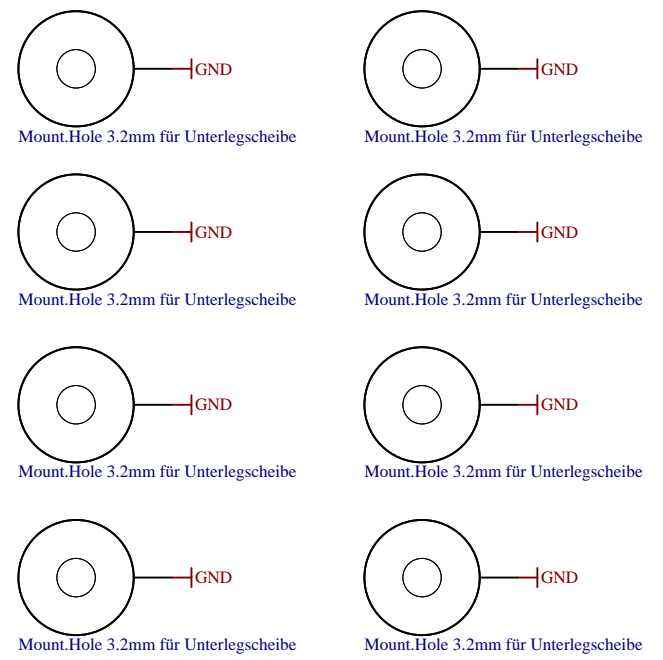
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Schematics and other handouts serve for informational purposes only!

	Title: <b>TE0817</b>		
	A4	Number: <b>TE0817 7DE71-A</b>	Rev. <b>01</b>
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	Filename: <b>Legal Notices Modules.SchDoc</b>		

U_J1 J1.SchDoc	U_B_PS_GT B_PS_GT.SchDoc	U_DDR4-TERM DDR4-TERM.SchDoc
U_J2 J2.SchDoc	U_PS_DDR PS_DDR.SchDoc	U_ZU_POWER ZU_POWER.SchDoc
U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	U_POWER_3 POWER_3.SchDoc
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_4.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	U_TE0817-Overview TE0817-Overview.SchDoc
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	U_Power_Diagram Power_Diagram.SchDoc
U_B_GT_2 B_GT_2.SchDoc	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	

Special notes:




LOGO1  
TE Logo PRINT Layer  
LOGO PRINT

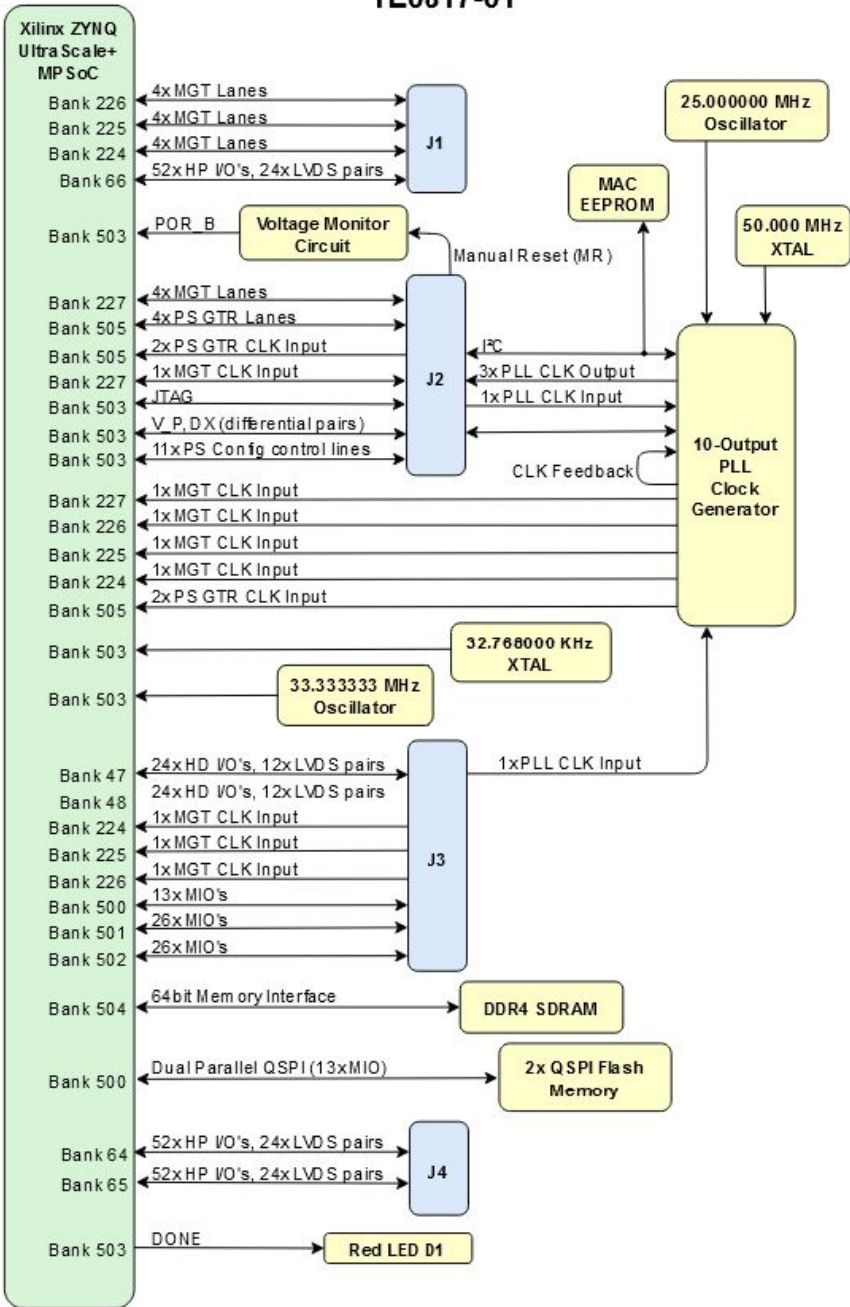
Serial  
Serialnumber 6,3 x 6.3mm

MECH1  
TE Address Overlay  
LOGO ADDRESS

Assembly variant	7DE71-A
Created by	VT
Modified by	VT
Modified at	2022-05-12
SVN Revision	12508

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TE0817-01



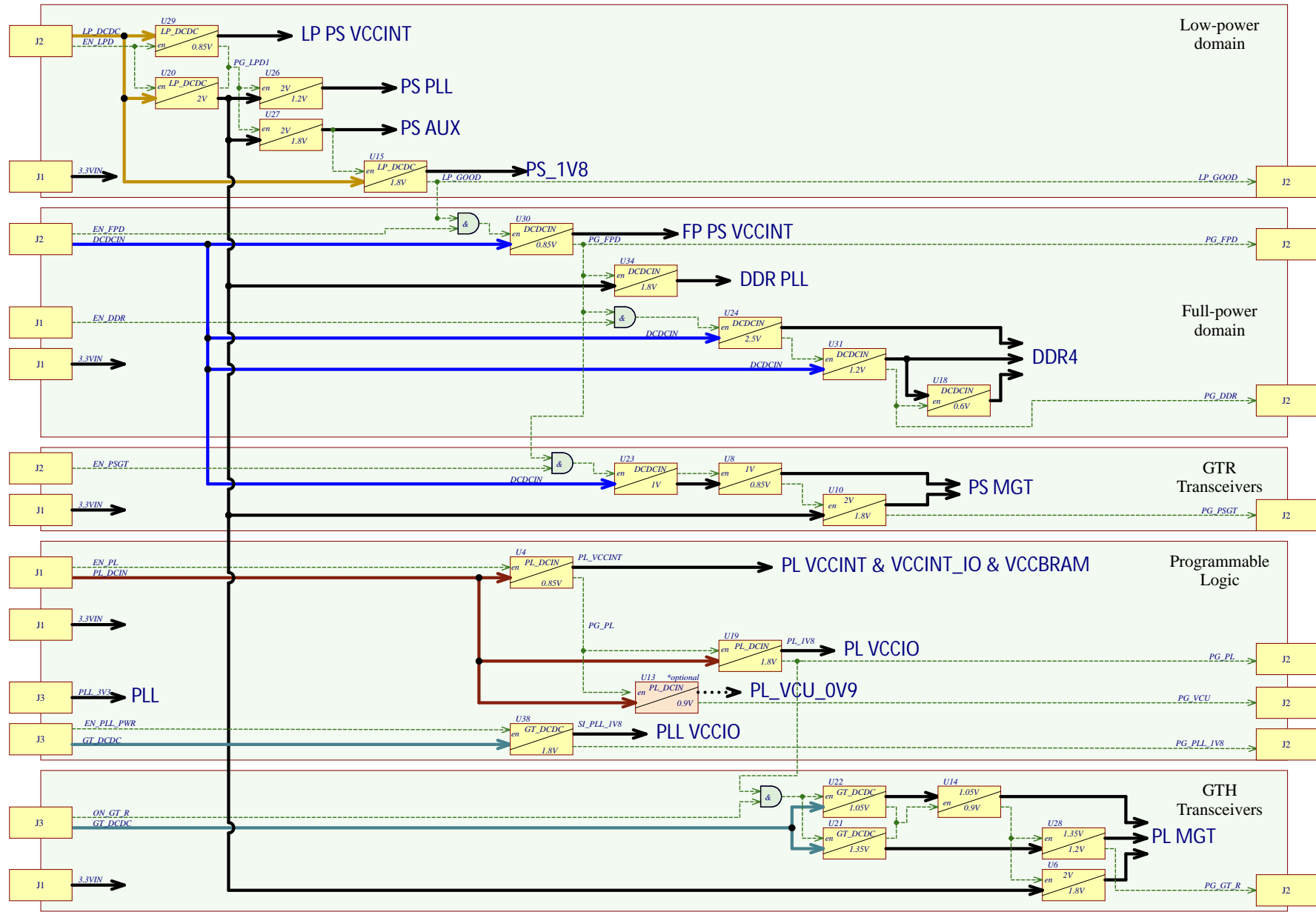
Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
PL_DCIN	IN	3.3 - 5.0V *	+/-5%	Micromodule Power	Programmable Logic, supplied by power rail
LP_DCDC	IN	3.3 - 5.0V	+/-5%	Micromodule Power	Low-Power Domain, supplied by power rail
GT_DCDC	IN	3.3 - 5.0V	+/-5%	Micromodule Power	GTH/GTY Transceiver, supplied by power rail
DCDCIN	IN	3.3 - 5.0V	+/-5%	Micromodule Power	Full-Power Domain and GTR, supplied by power rail
VCCO_64	IN	1.0 - 1.8V	+/-3%	HP IO Bank64	-
VCCO_65	IN	1.0 - 1.8V	+/-3%	HP IO Bank65	-
VCCO_66	IN	1.0 - 1.8V	+/-3%	HP IO Bank66	-
VCCO_47	IN	1.2 - 3.3V	+/-3%	HD IO Bank47	-
VCCO_48	IN	1.2 - 3.3V	+/-3%	HD IO Bank48	-
PSBATT	IN	1.2 - 1.5V	-	RTC / BBRAM	-
PLL_3V3	IN	3.3V	+/-5%	PLL Analog Power	-
PL_1V8	OUT	1.8V	+/-5%	Power for Carrier	Micromodule: Programmable Logic
PS_1V8	OUT	1.8V	+/-5%	Power for Carrier	Micromodule: Processing System
DDR_1V2	OUT	1.2V	+/-5%	Power for Carrier	Micromodule: PS DDR I/O Supply

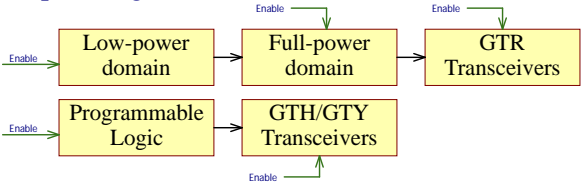
\* for Micromodules, where U4 is TPS548A28RWR or MPQ8633BGL-Z maximum Vin range will be 3.3V



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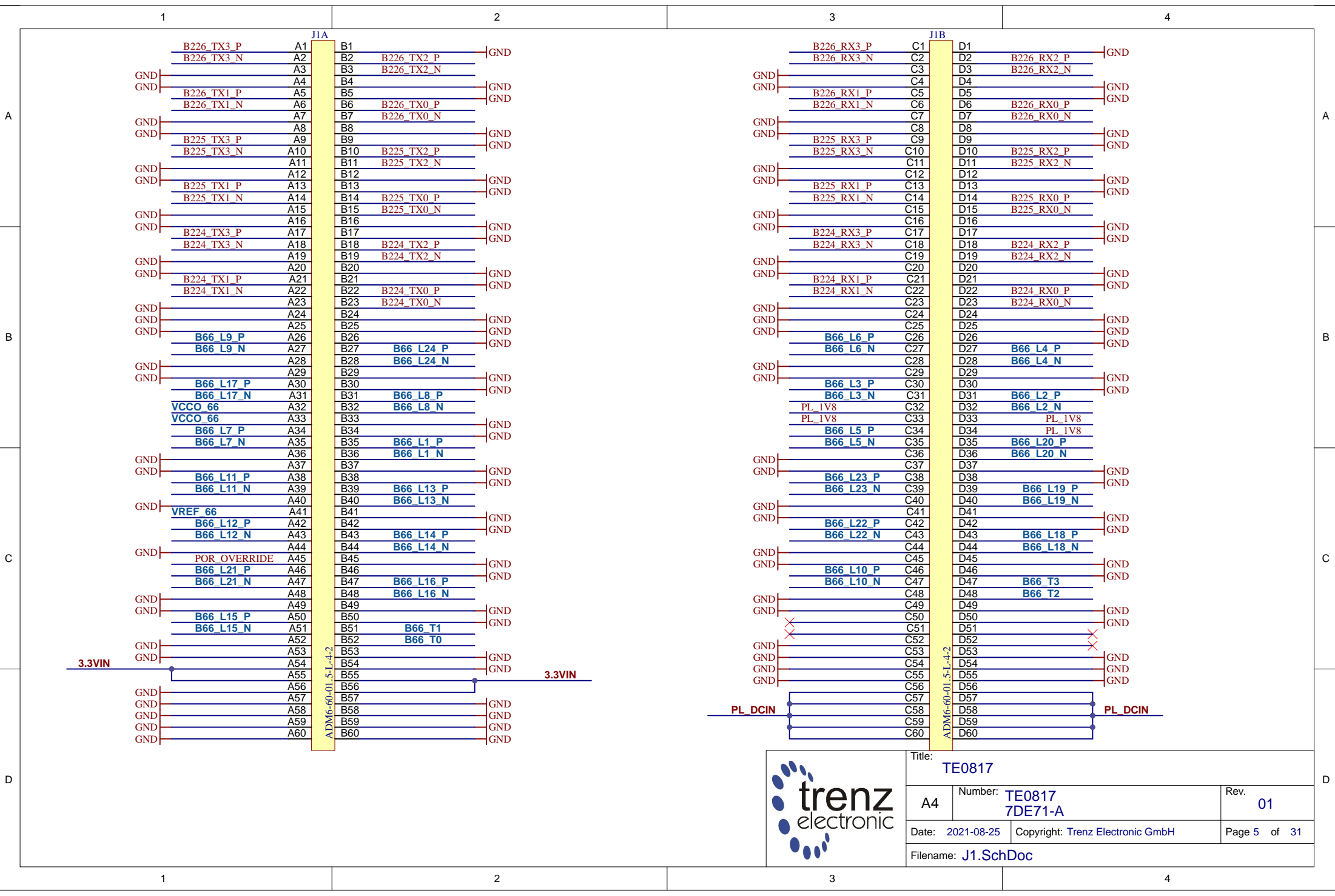
**Power-on sequencing:**



- EN\_GT\_R: Net name
- Power bus: Solid black arrow
- Control signal: Dashed green arrow
- Power bus in FPGA speedgrade -1/-2/-3 assembly variants: Dotted blue arrow
- Power bus in FPGA speedgrade -1L/-2L assembly variants (low power): Dotted orange arrow
- Optional power converter: Box with diagonal line and 0.9V
- Logic AND gate: Circle with '&' symbol



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Filename: J1.SchDoc		

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A

A

B

B

C

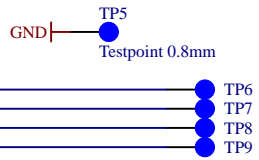
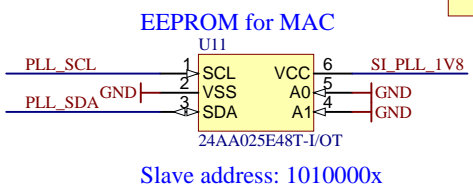
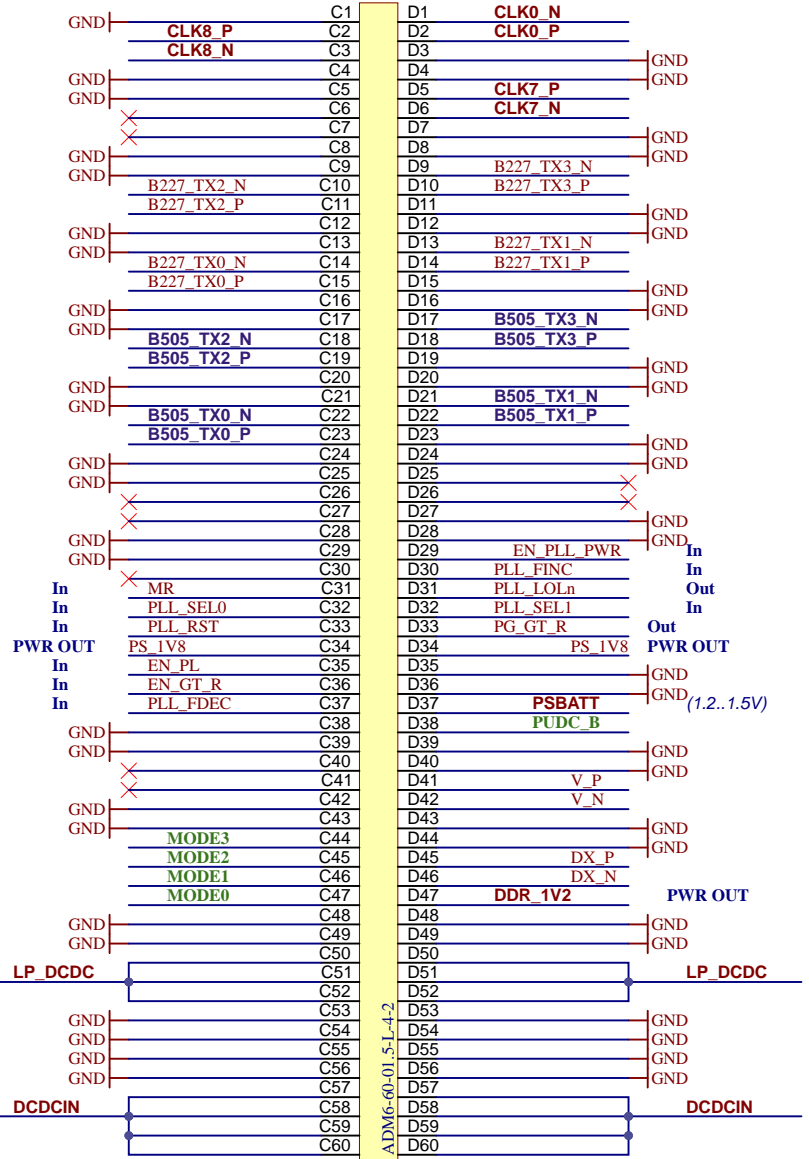
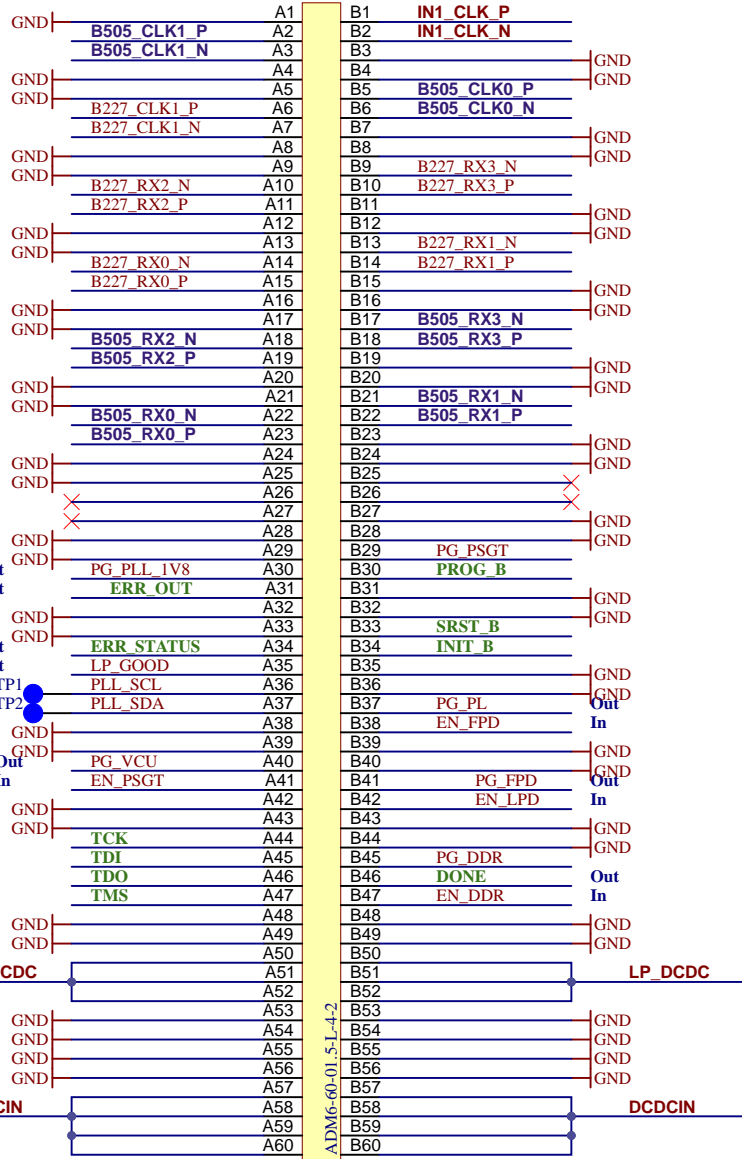
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D

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J2A  
ADM6-60-01\_5-L-4-2

J2B  
ADM6-60-01\_5-L-4-2



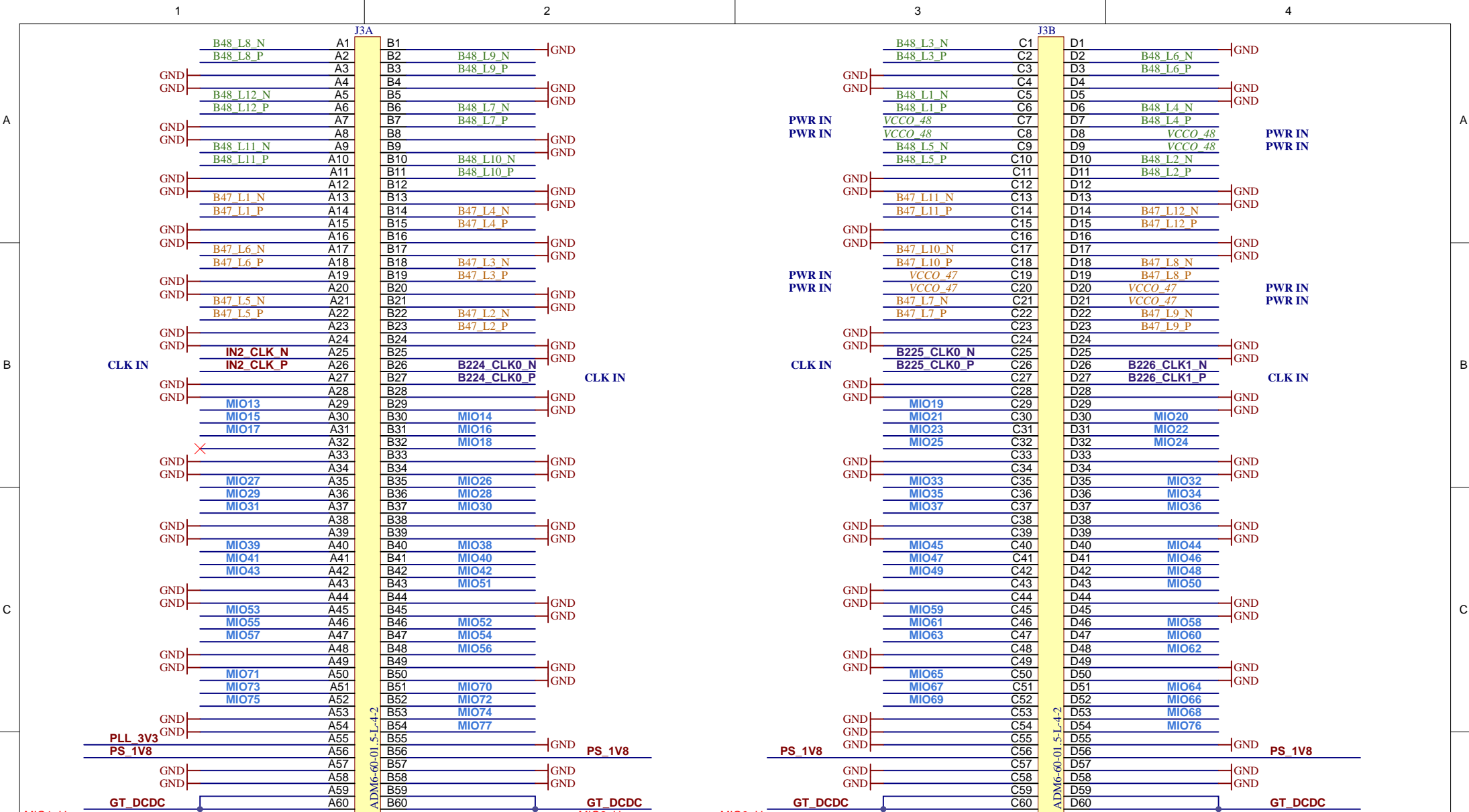
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Filename: J2.SchDoc	

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MIO45	MIO38	MIO26	MIO32	MIO52	MIO58	MIO64	MIO71	MIO13	MIO19
MIO46	MIO39	MIO27	MIO33	MIO53	MIO59	MIO65	MIO72	MIO14	MIO20
MIO47	MIO40	MIO28	MIO34	MIO54	MIO60	MIO66	MIO73	MIO15	MIO21
MIO48	MIO41	MIO29	MIO35	MIO55	MIO61	MIO67	MIO74	MIO16	MIO22
MIO49	MIO42	MIO30	MIO36	MIO56	MIO62	MIO68	MIO75	MIO17	MIO23
MIO50	MIO43	MIO31	MIO37	MIO57	MIO63	MIO69	MIO76	MIO18	MIO24
MIO51	MIO44					MIO70	MIO77		MIO25



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1

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3

4

A

A

B

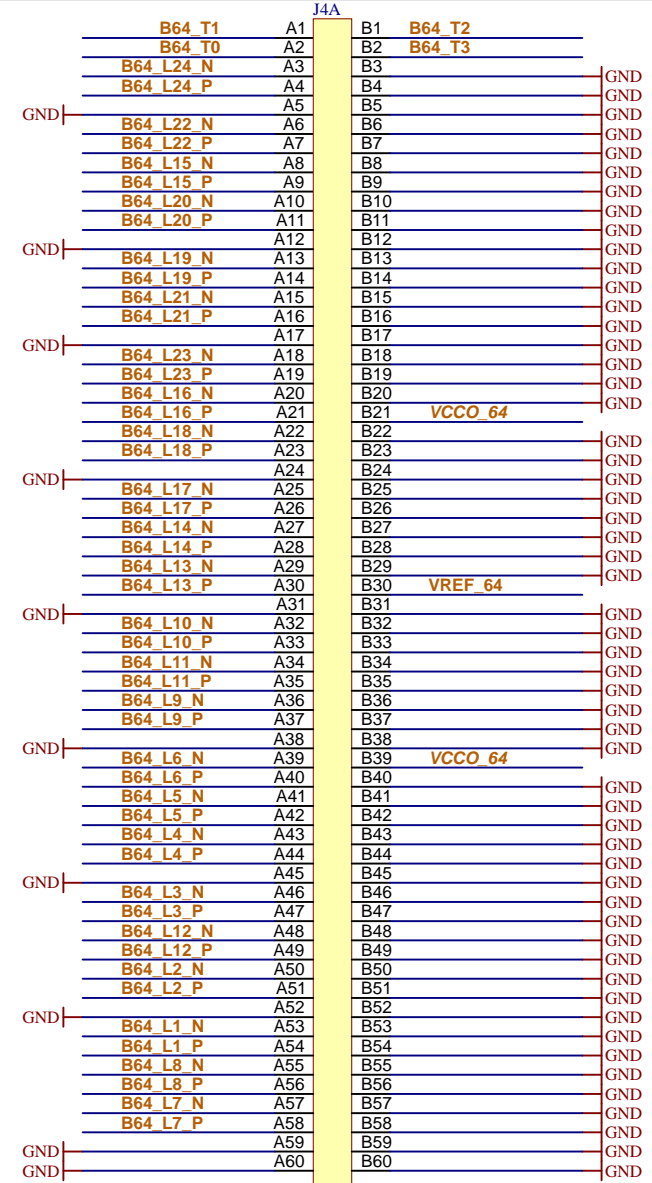
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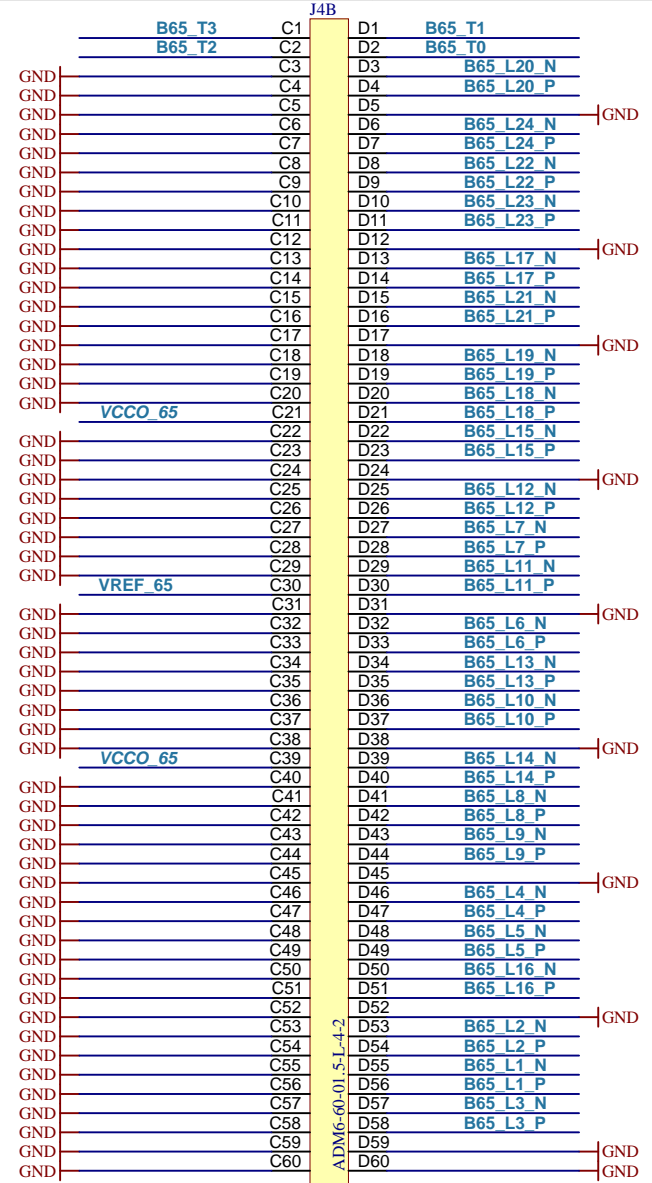
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D

D



ADM6-60-01.5-L-4-2



ADM6-60-01.5-L-4-2



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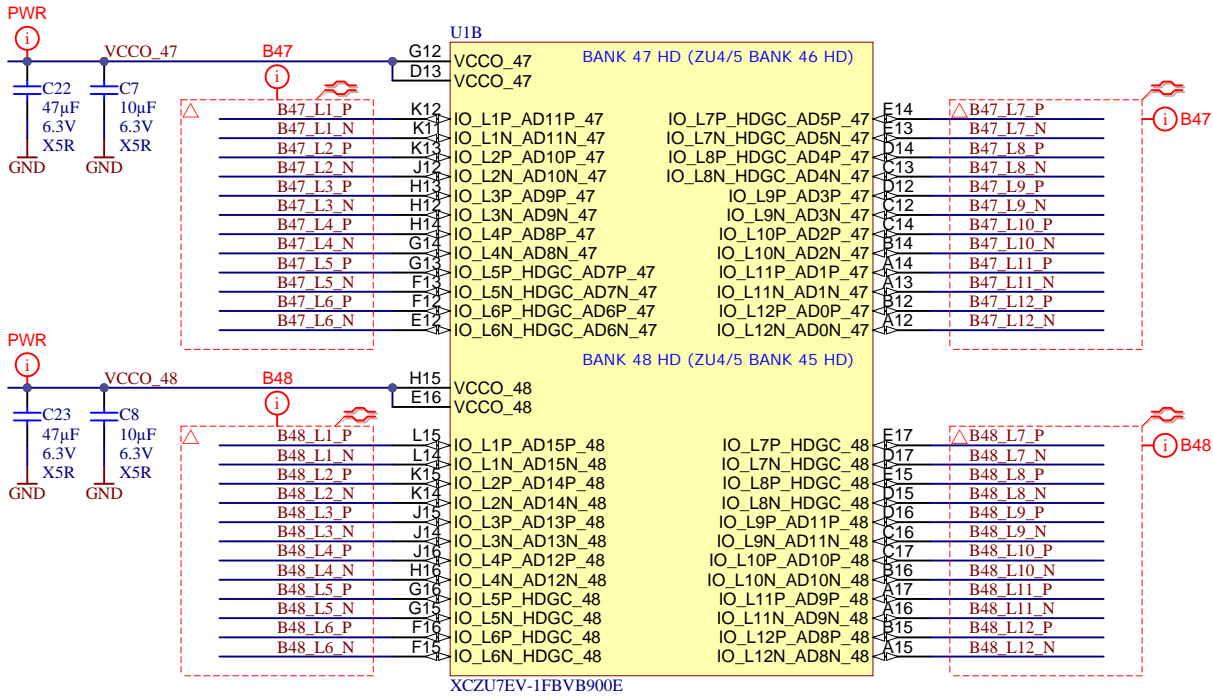

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2

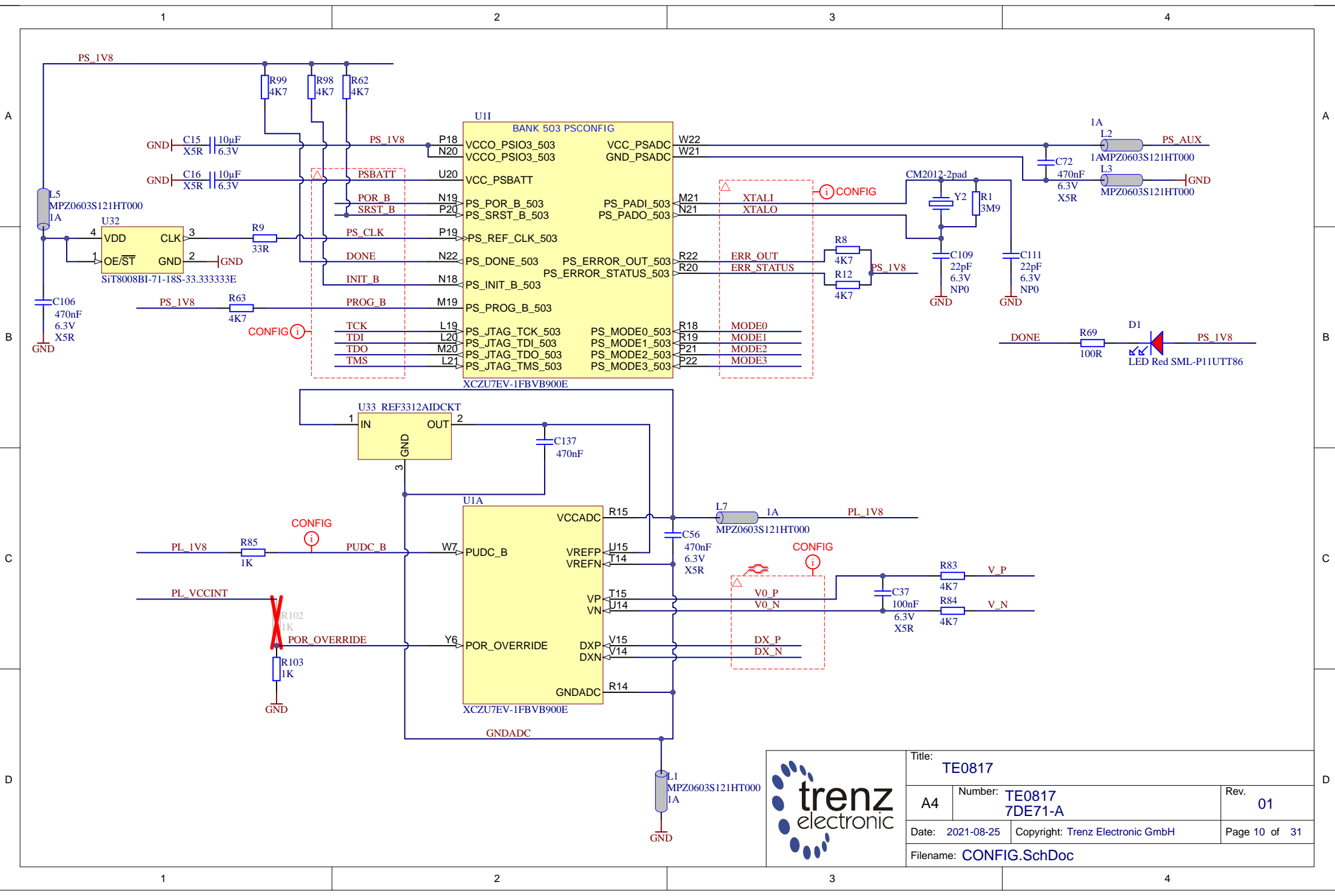
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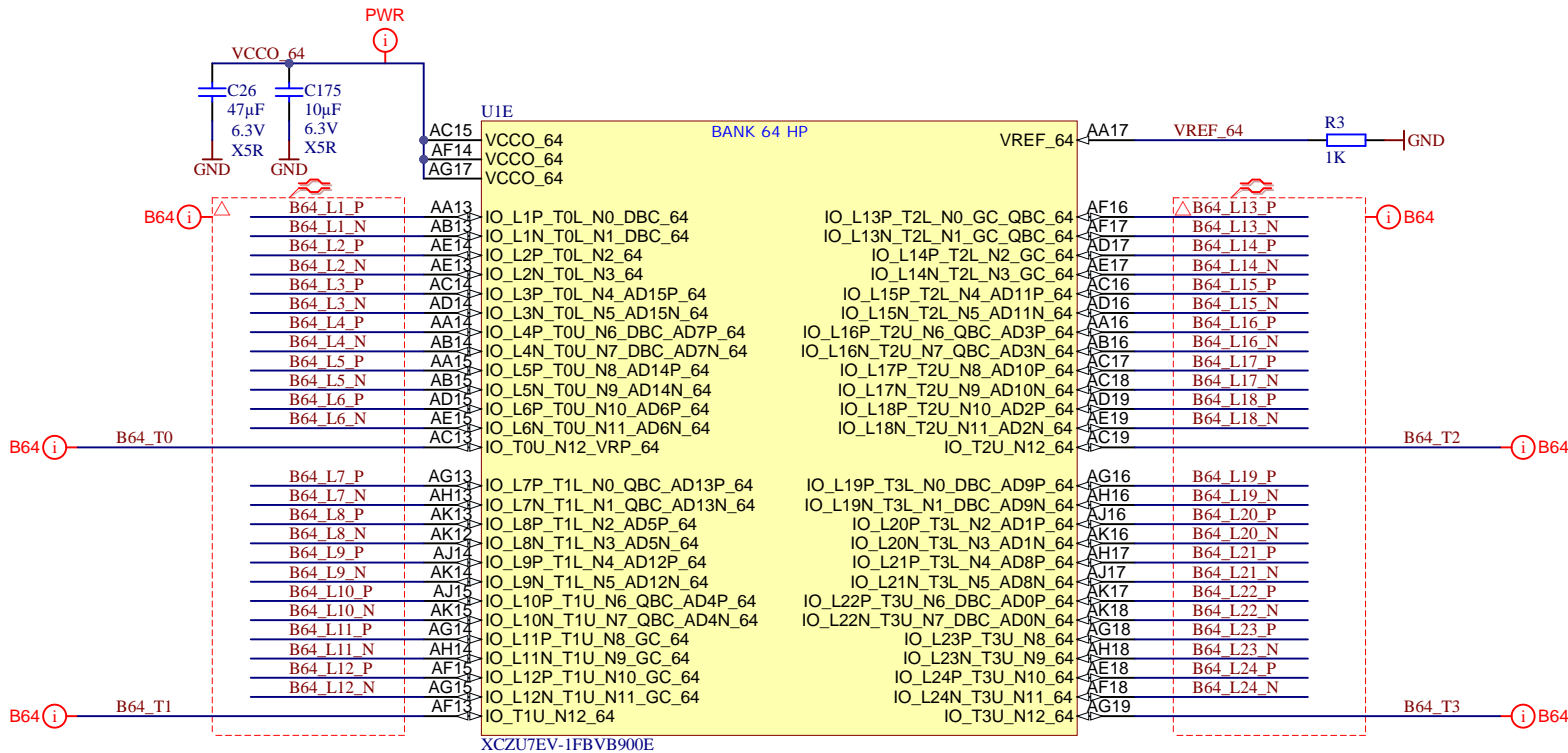


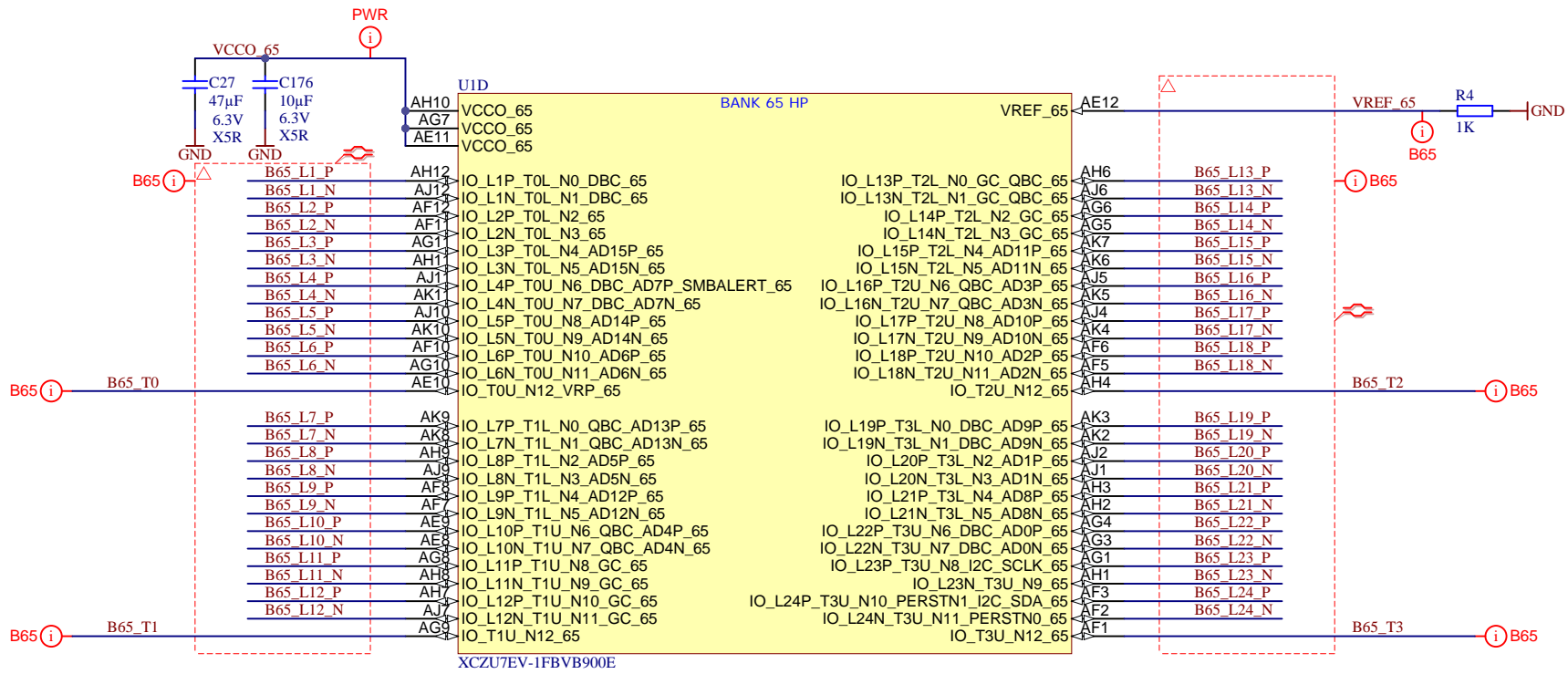
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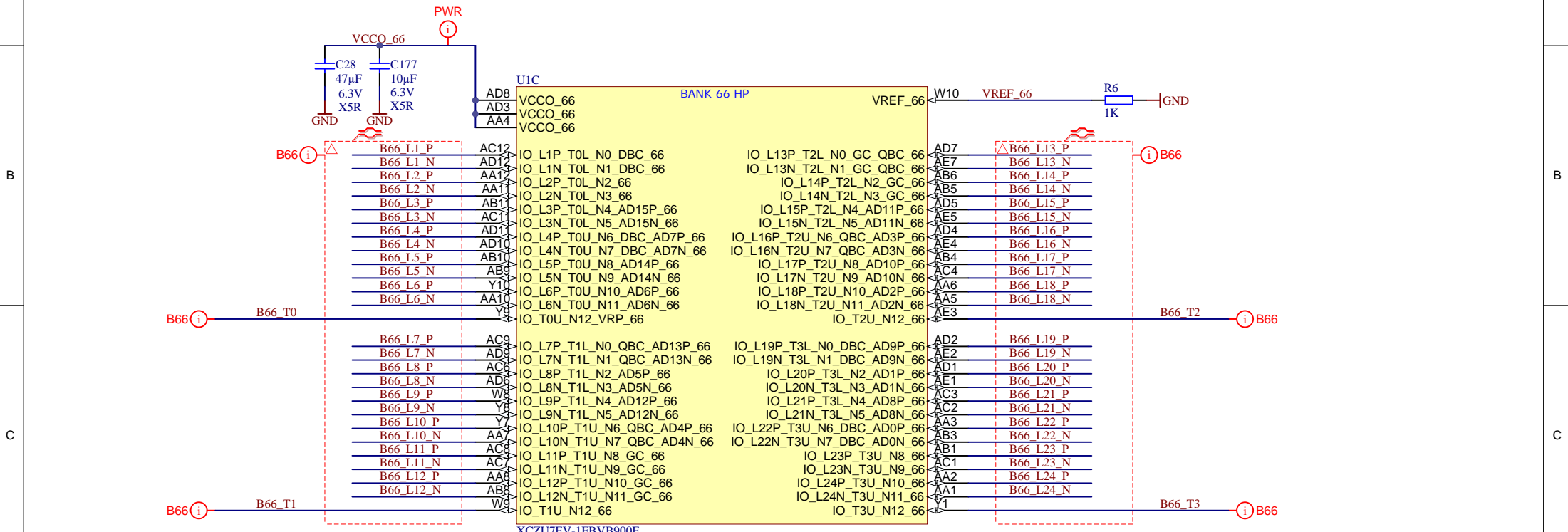

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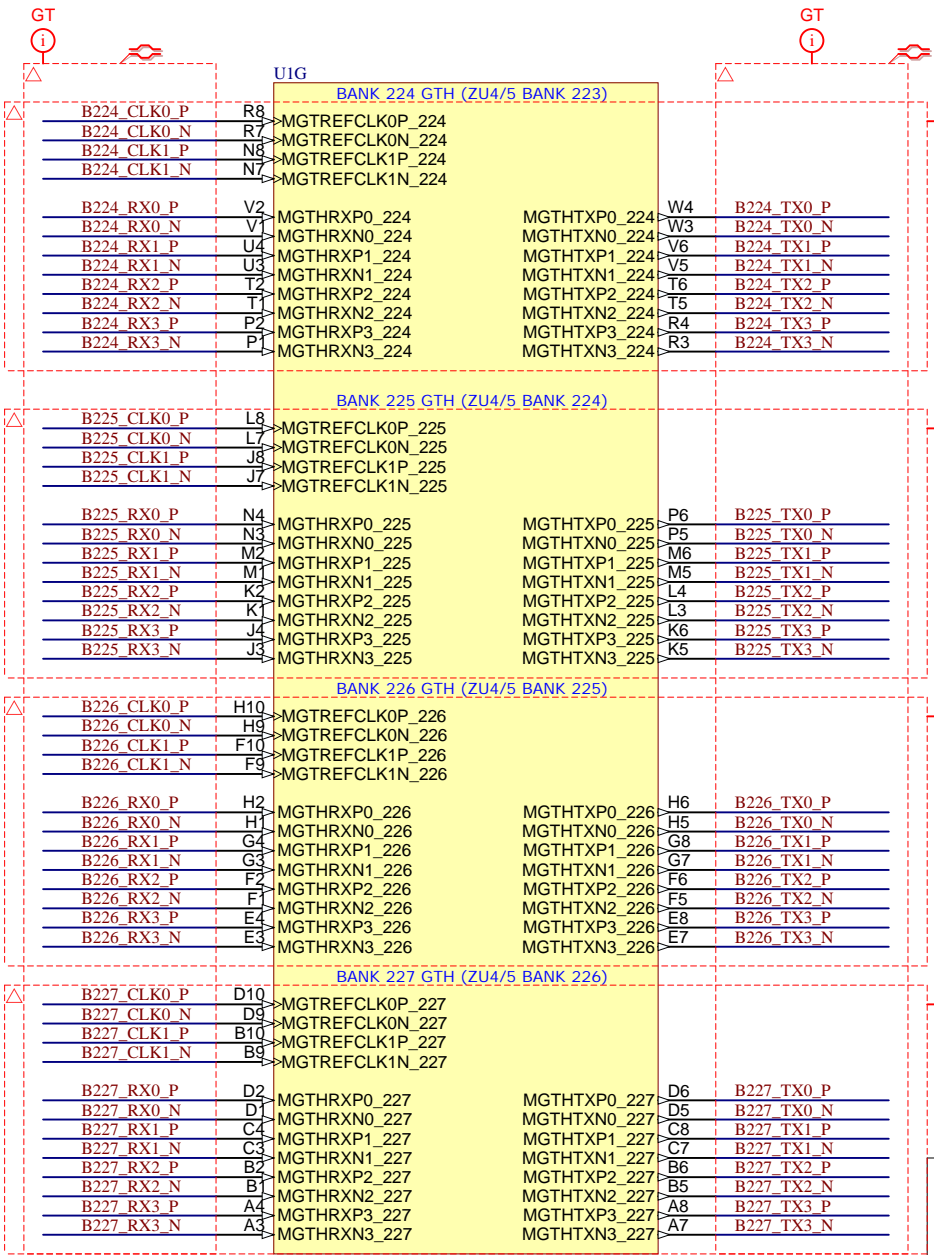
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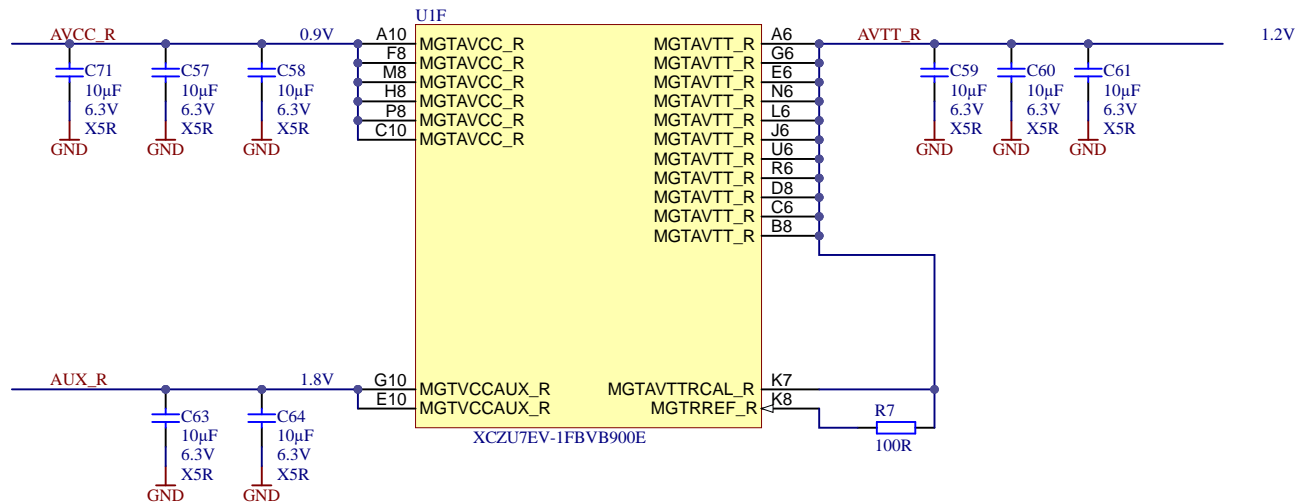
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229

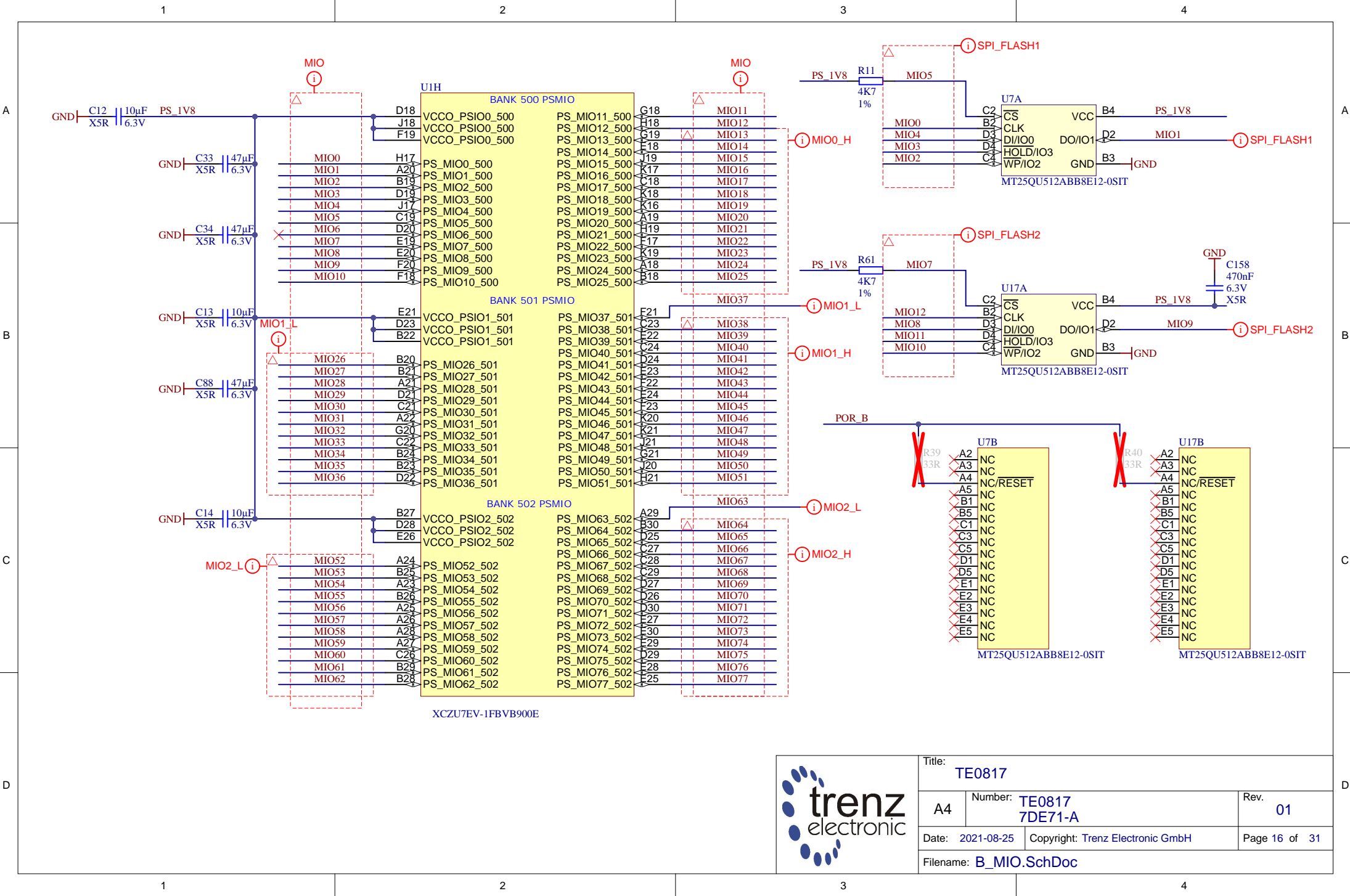
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Filename: <b>B_MIO.SchDoc</b>		Page <b>16</b> of <b>31</b>	



A

A

B

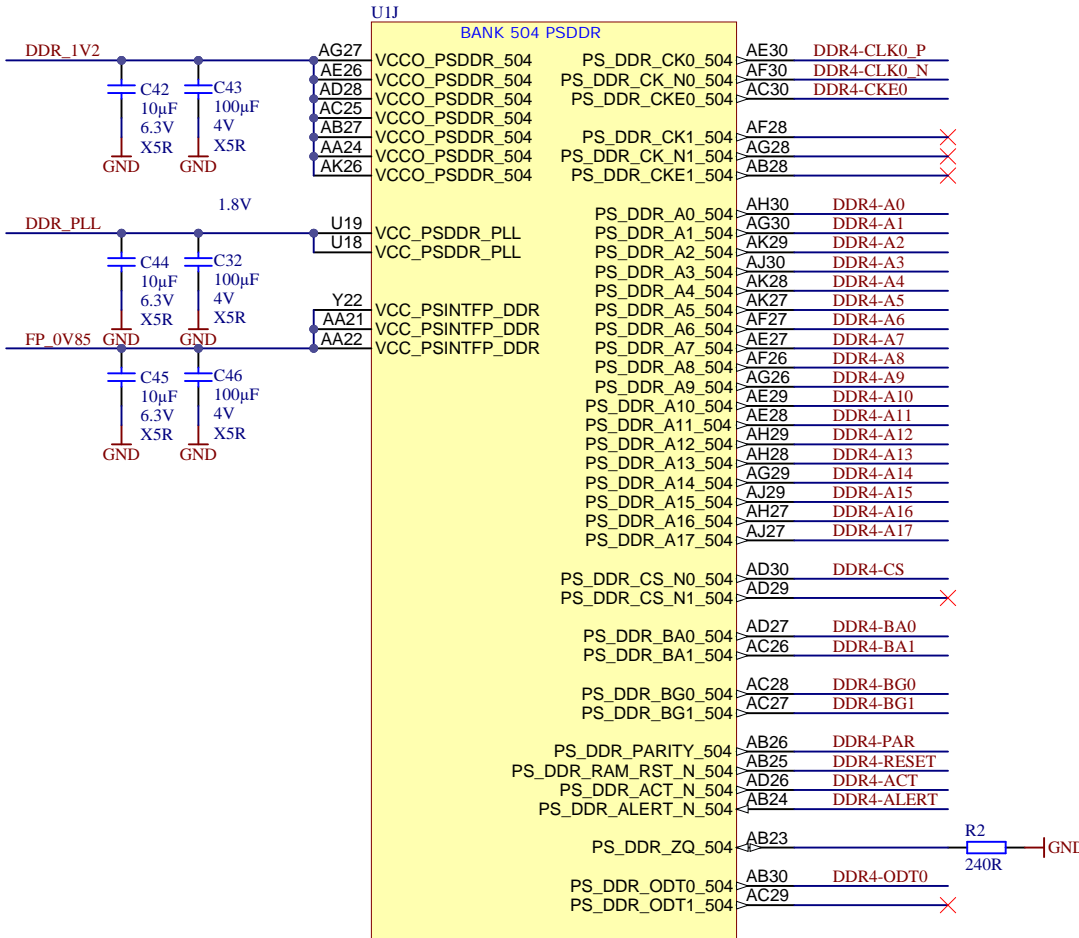
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C

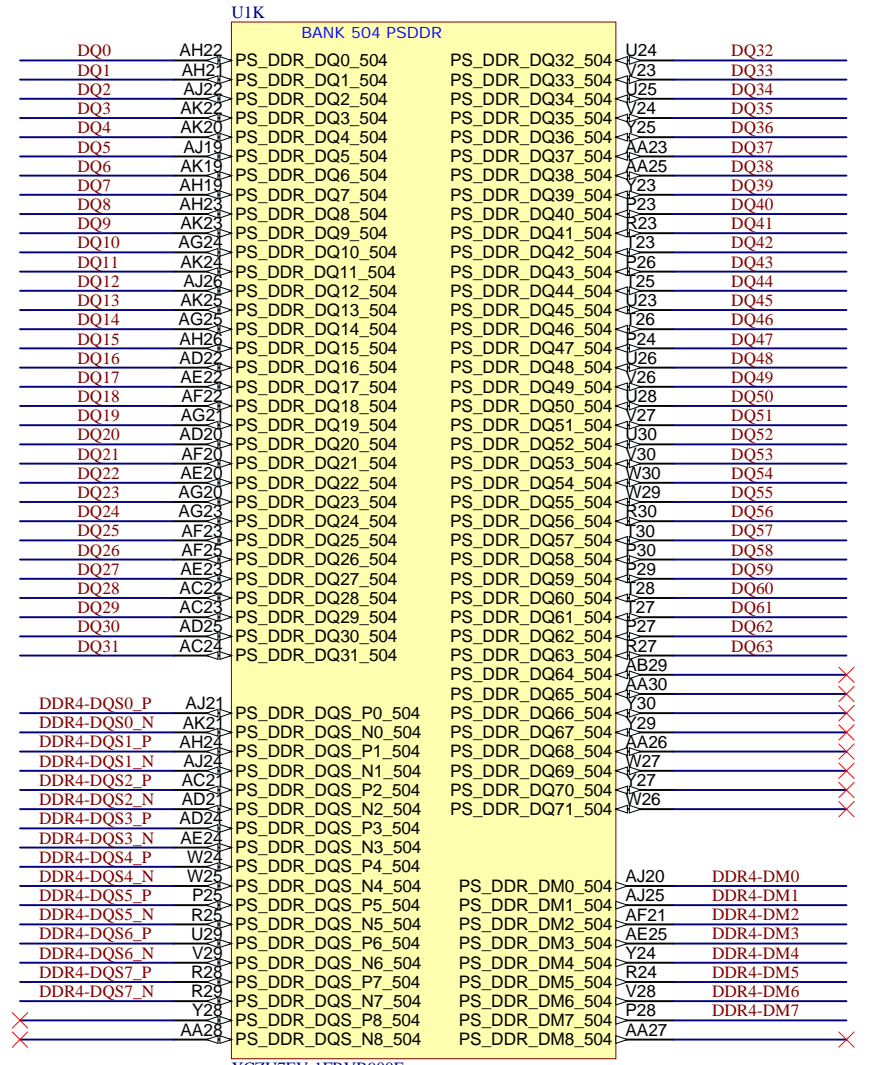
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D



XCZU7EV-1FBVB900E



XCZU7EV-1FBVB900E



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Filename: <b>PS_DDR.SchDoc</b>		

1

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A

A

B

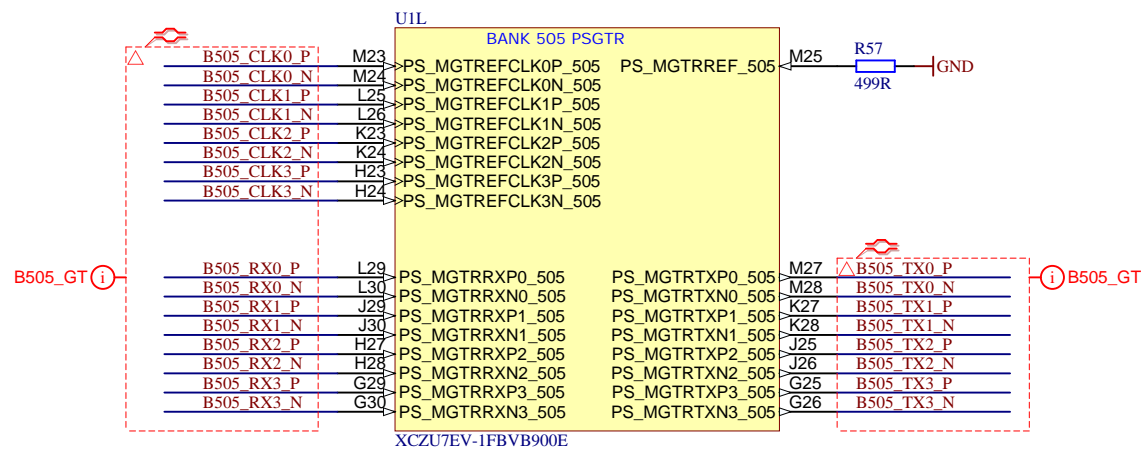
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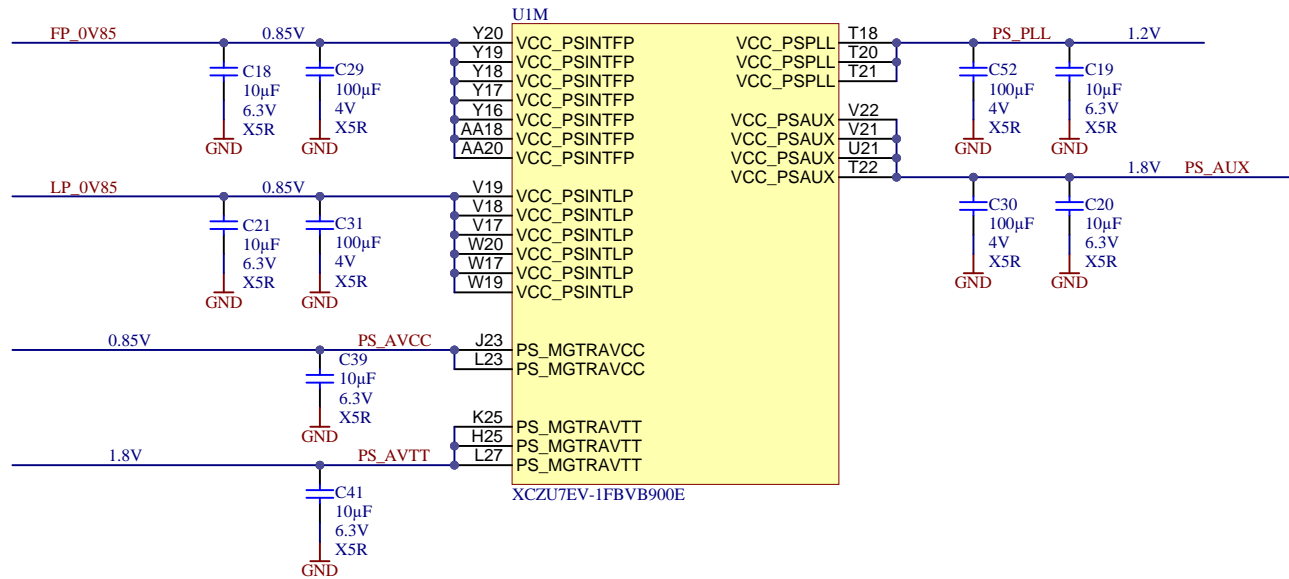
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Filename: ZU_PS_POWER.SchDoc			

A

A

B

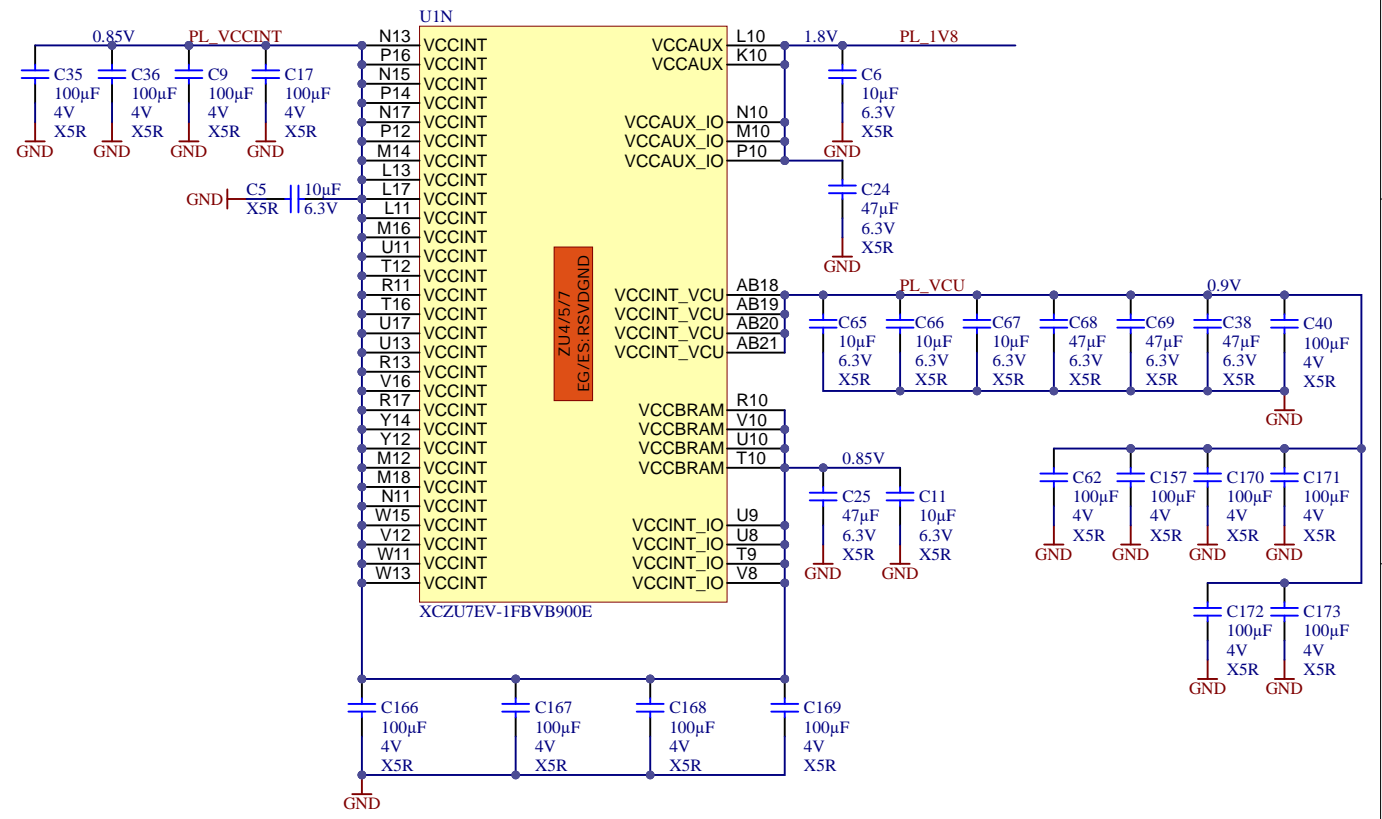
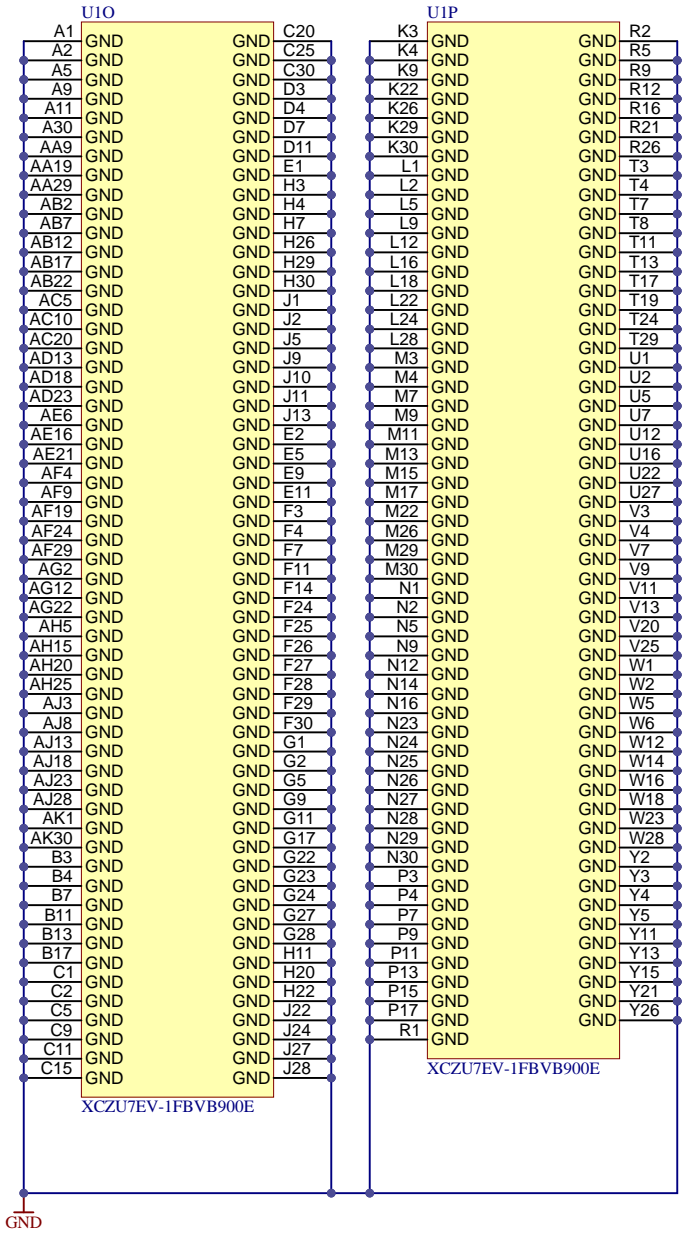
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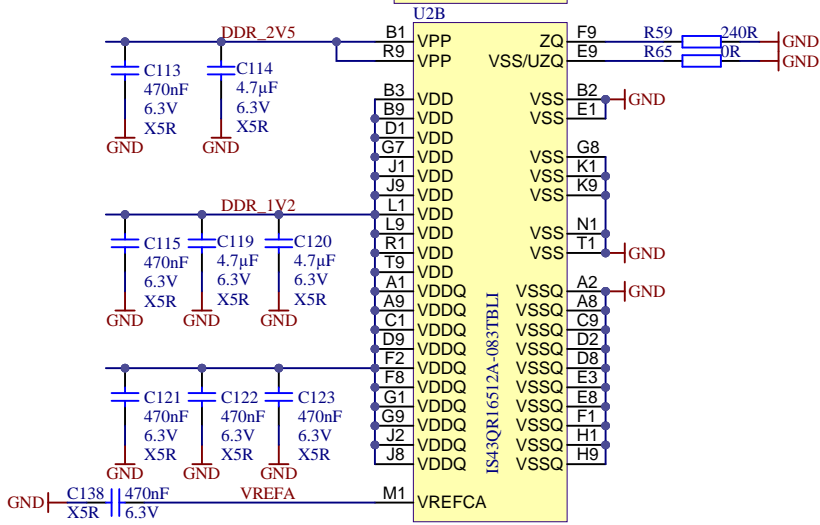
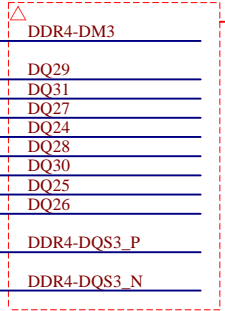
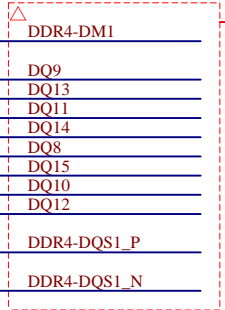
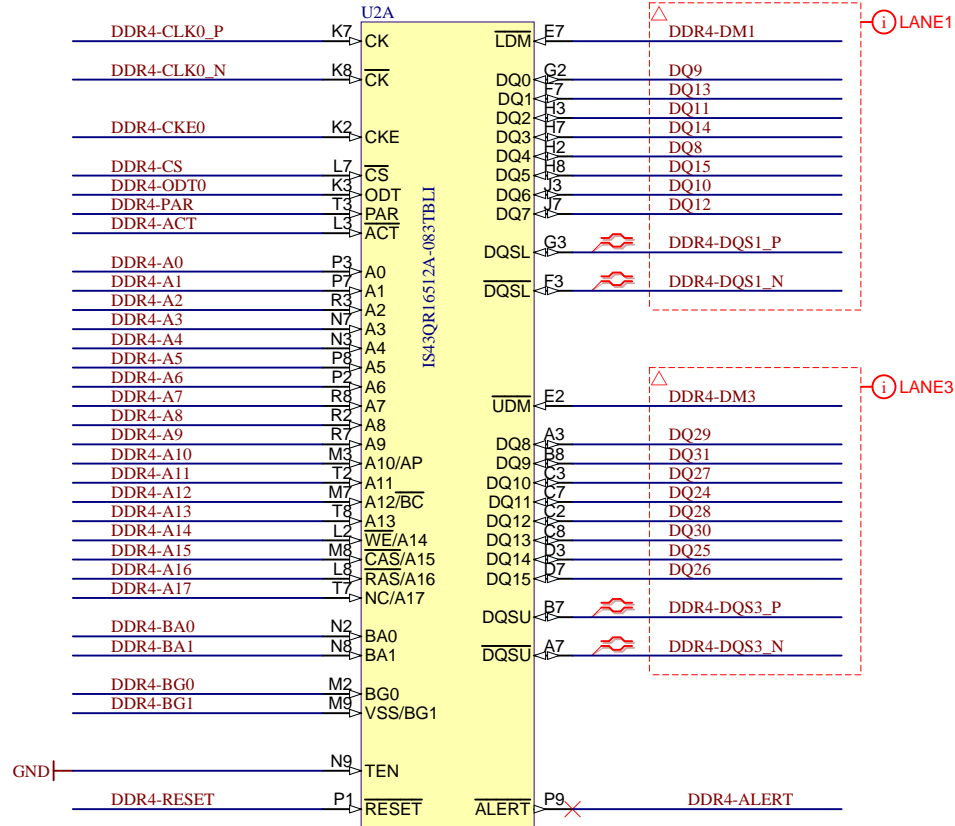
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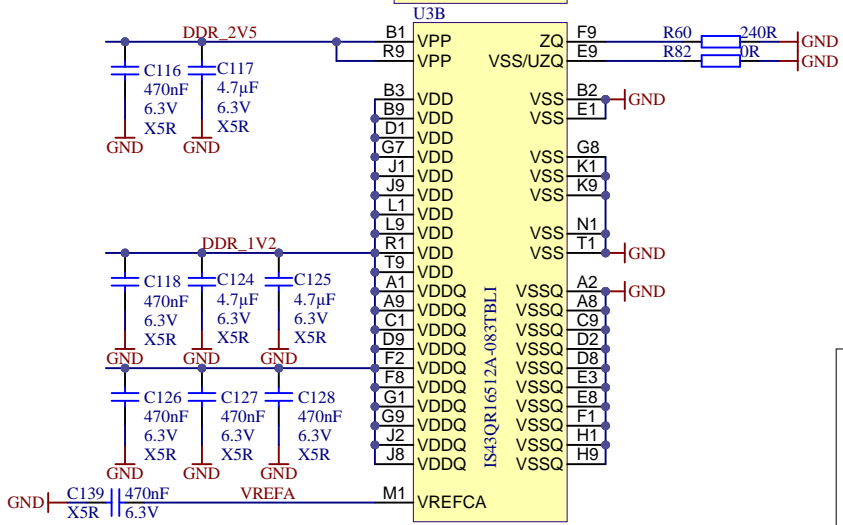
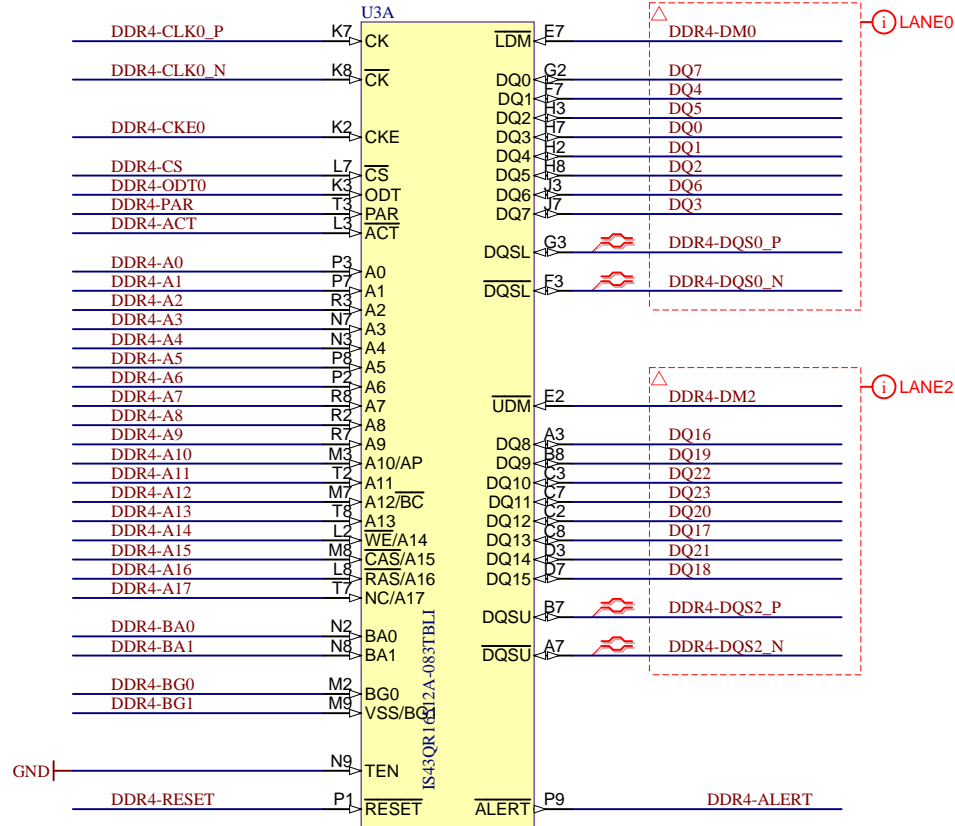
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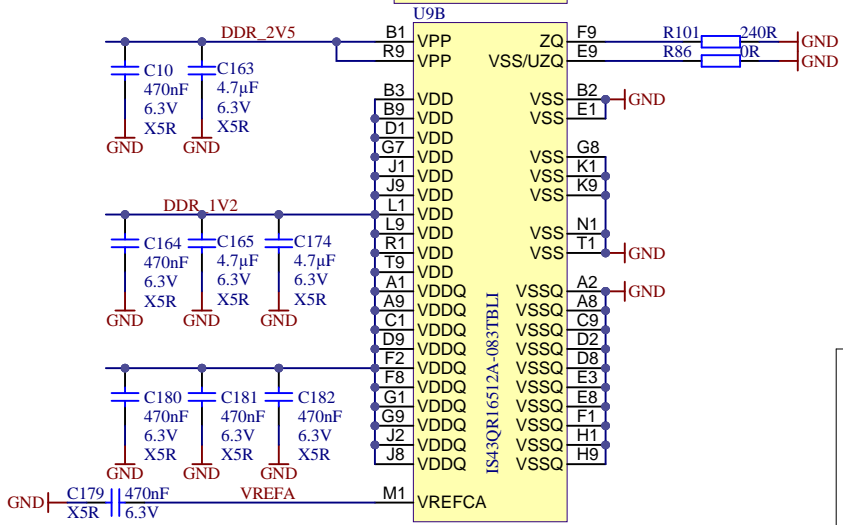
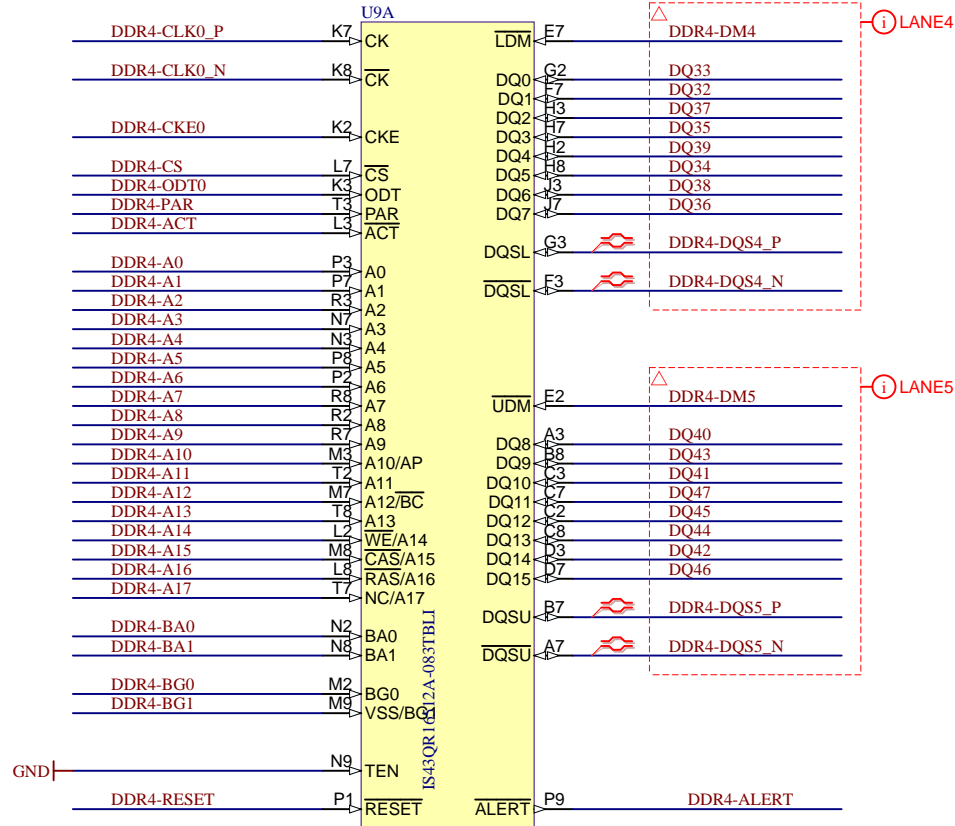
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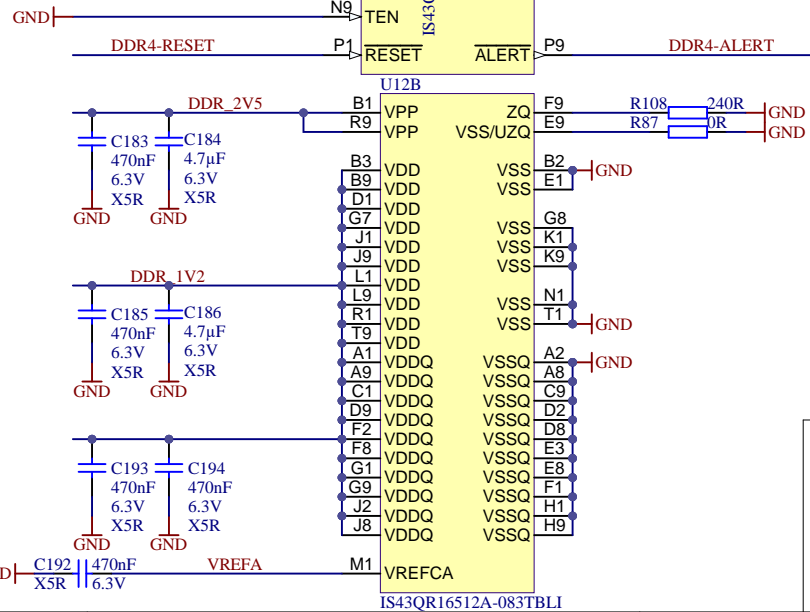
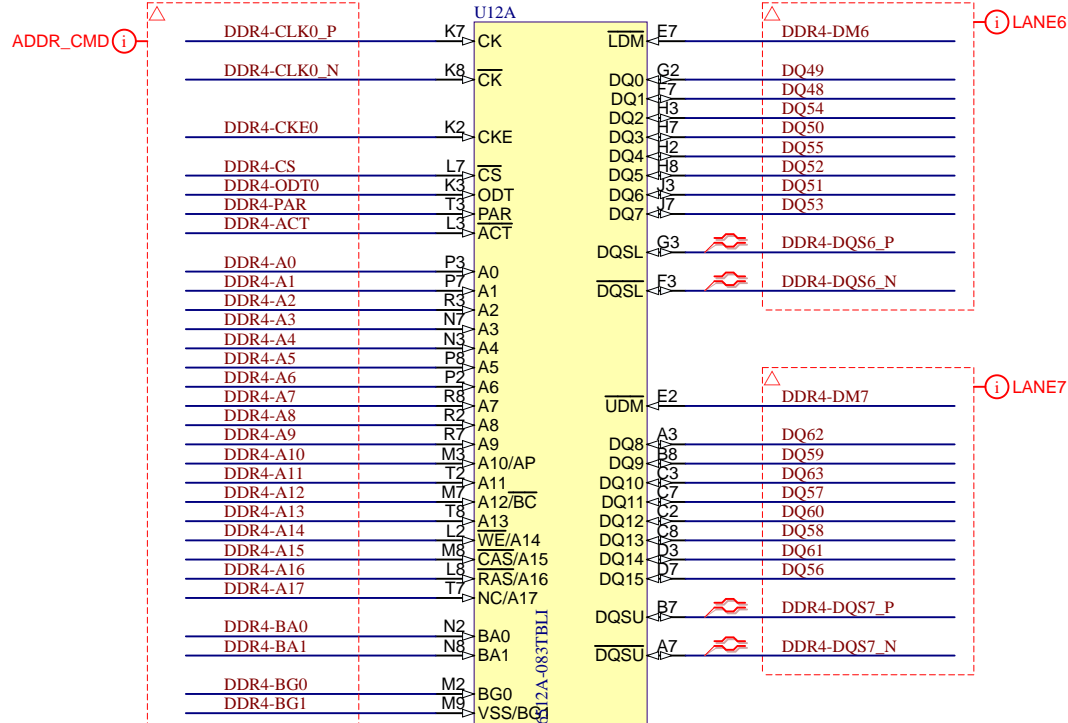
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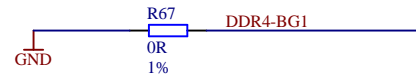
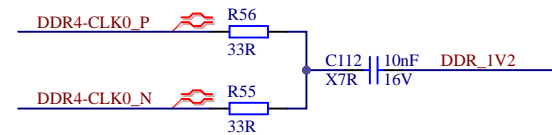
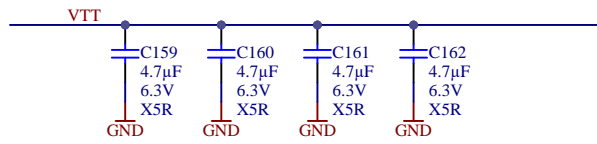
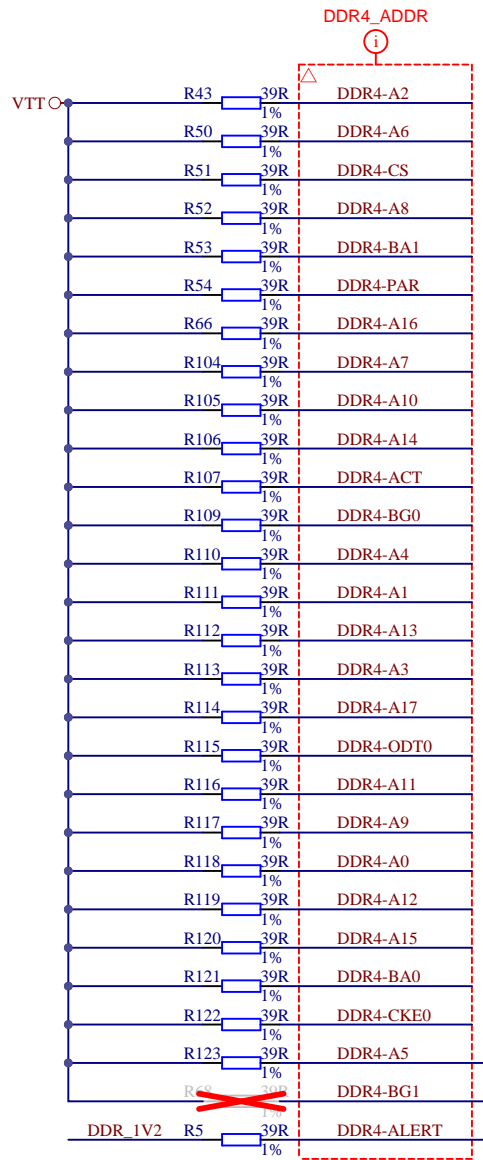


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Filename: <b>DDR4-RAM_3.SchDoc</b>		

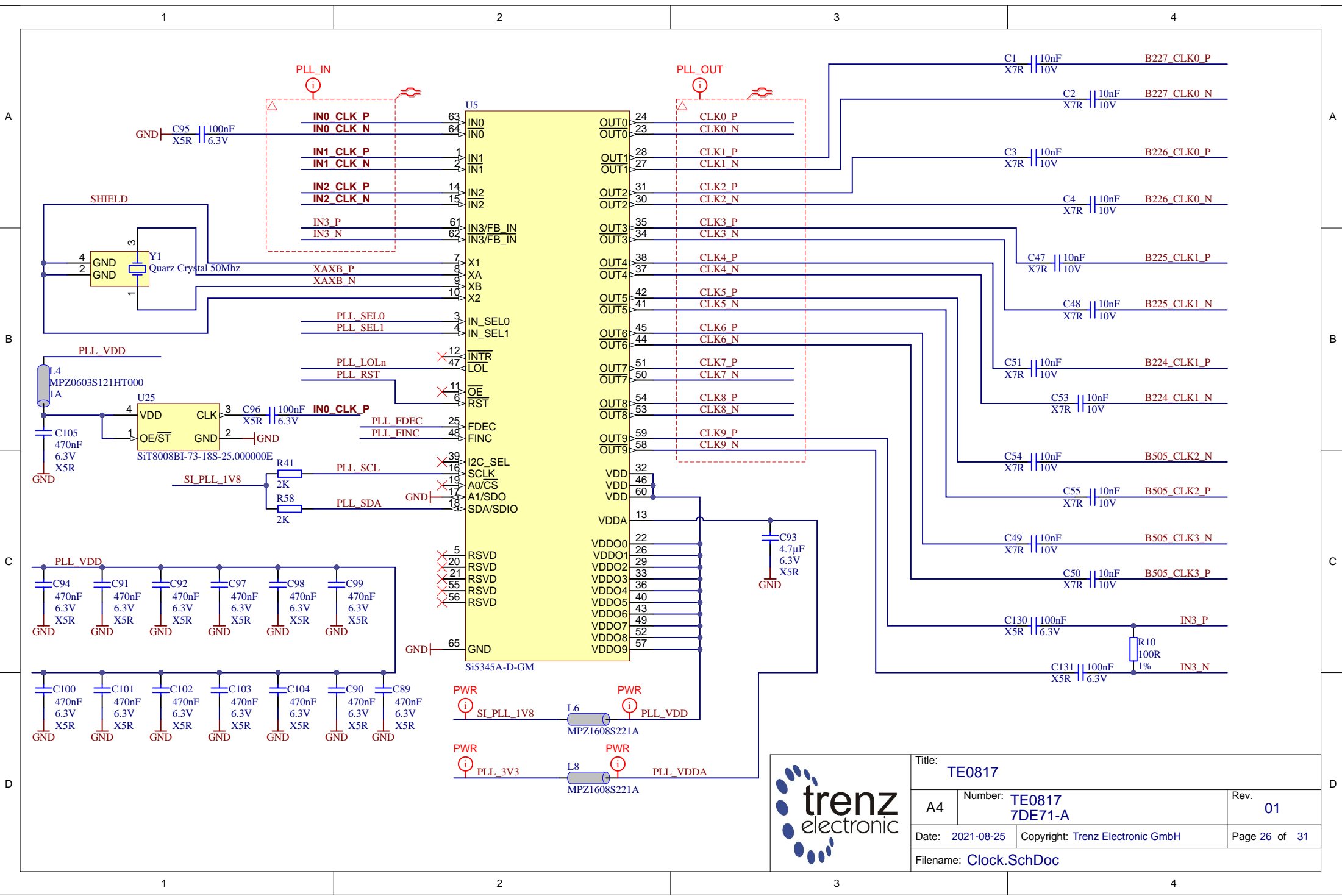


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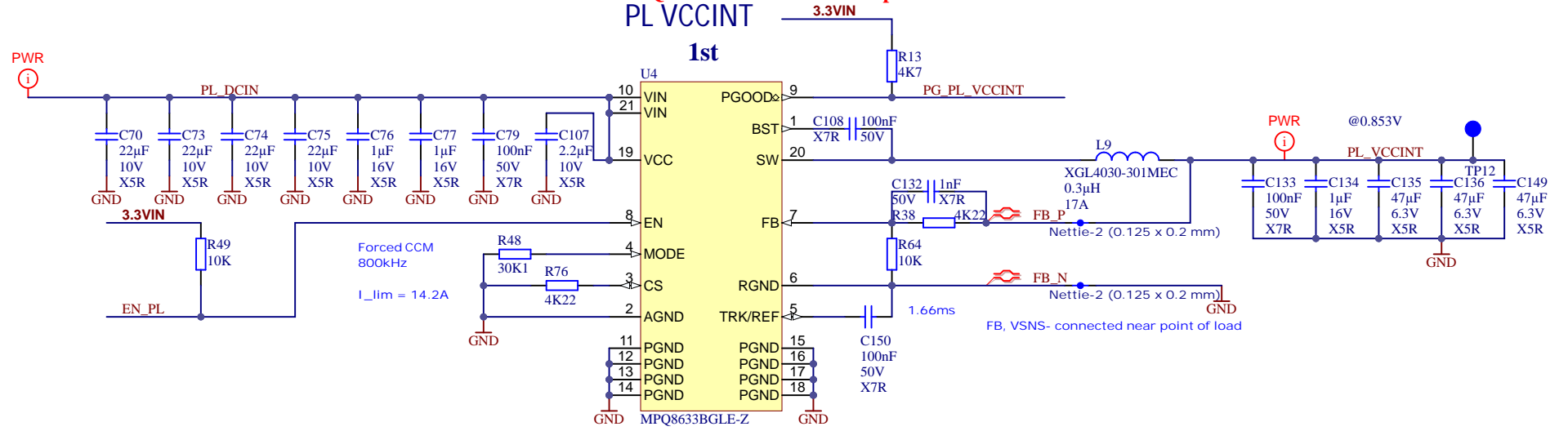


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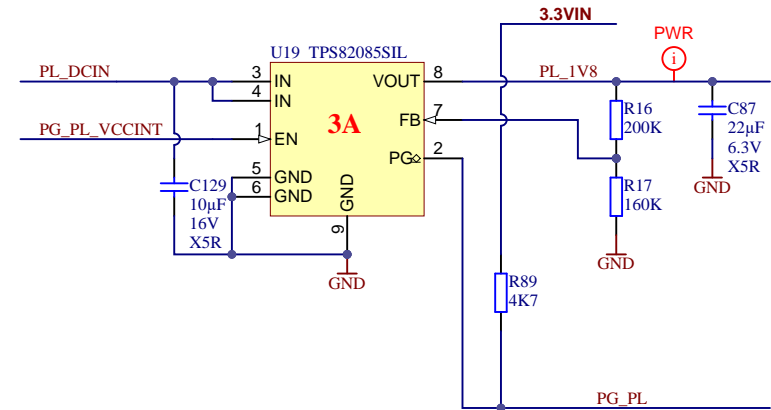
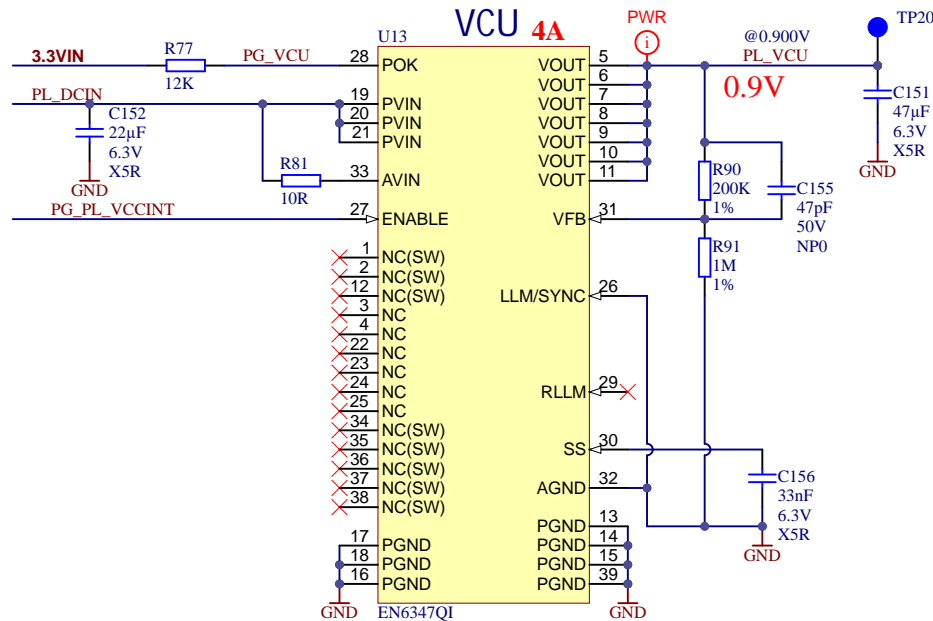


Title: TE0817		
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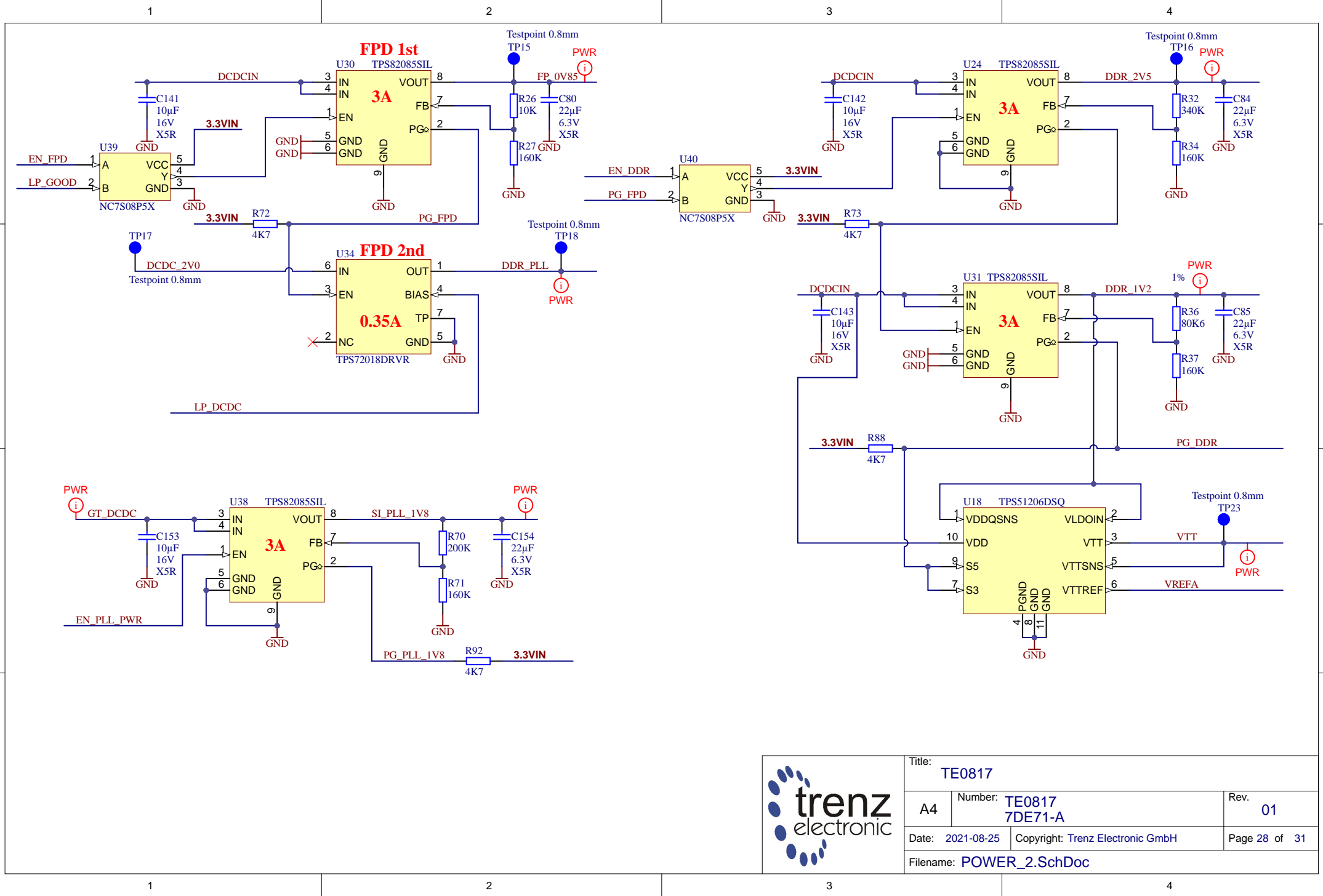
U4 can be TPS548A28RWWR or MPQ8633BGLE-Z which is up to Trenz Electronic GmbH.




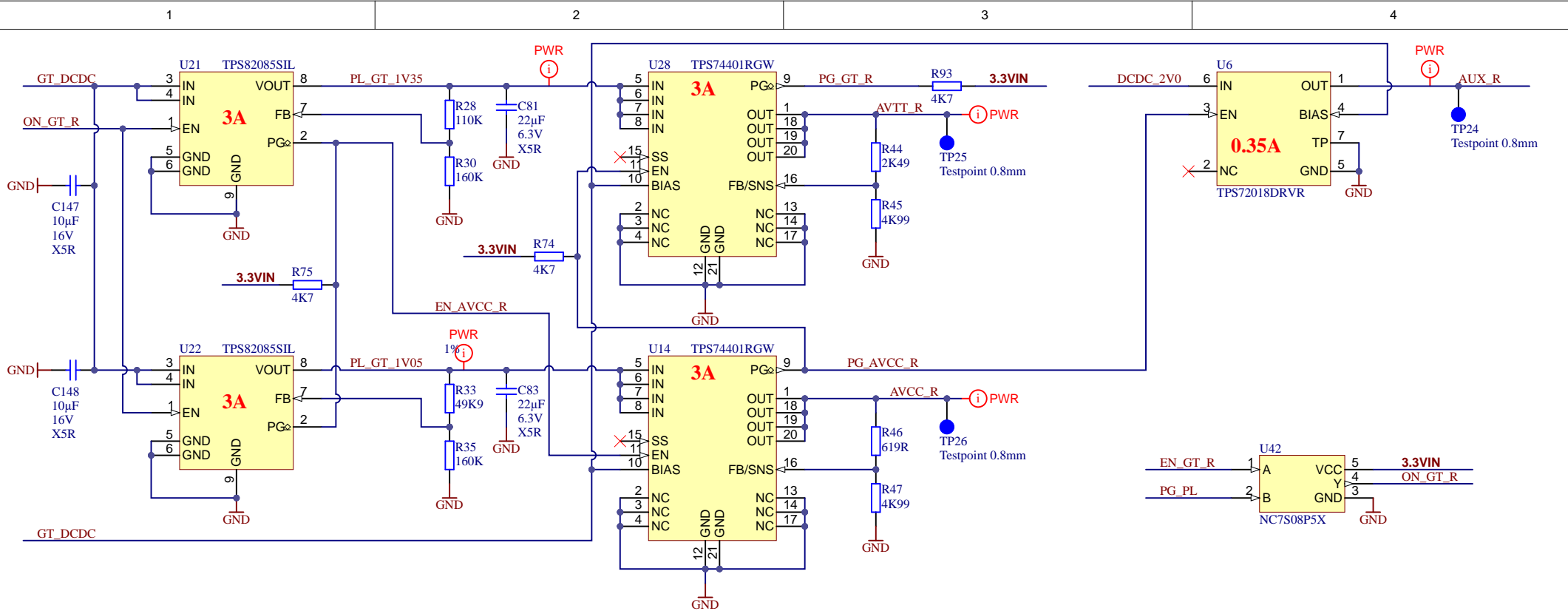
U4 pin compatible with  
 -- TPS54JA20 (12A)  
 -- TPS548A28 (15A)  
 -- TPS548B28 (20A)



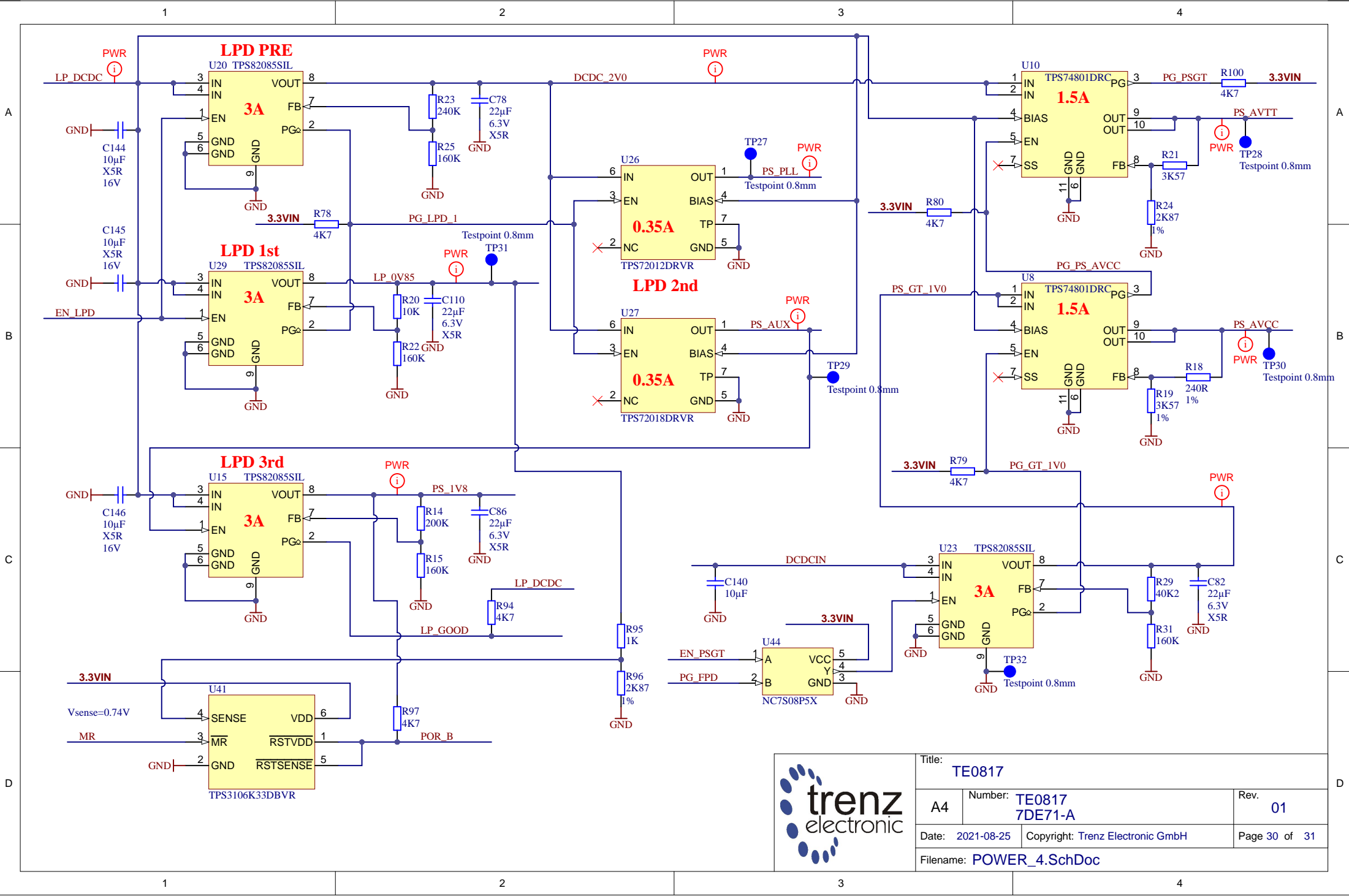
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REV	DATE	Description	
-01	2021-05	Initial revision	VT
	2022-05	Changed DCDC U4 TPS548A28 to MPQ8633BGLE-Z Changed C132 100nF to 1nF	
	2022-11	Added Table with Supported Voltage Ranges	

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