


Regarding the usage of our schematics and alike documentation for Trenz module TE0817.

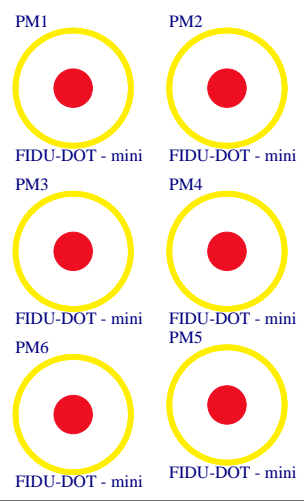
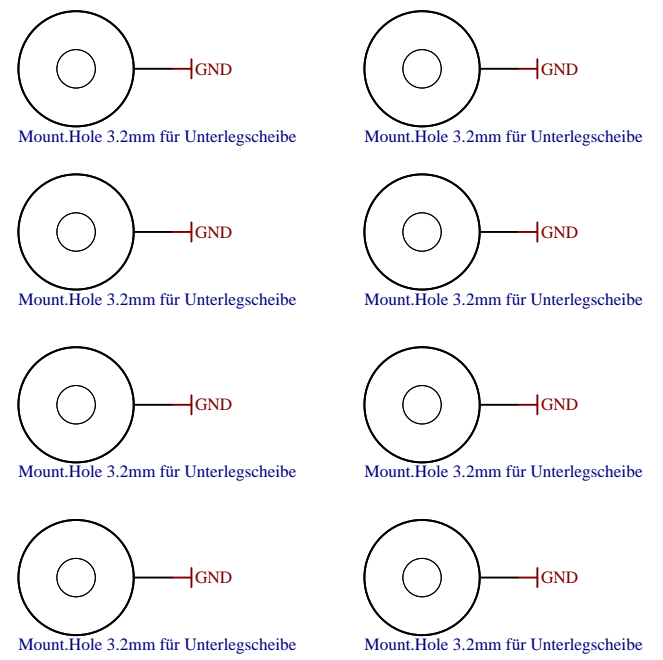
Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0817 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

	Title: TE0817		
	A4	Number: TE0817 7NE21-A	Rev. 01
	Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 1 of 31
	Filename: Legal Notices Modules.SchDoc		

U_J1 J1.SchDoc	U_B_PS_GT B_PS_GT.SchDoc	U_DDR4-TERM DDR4-TERM.SchDoc
U_J2 J2.SchDoc	U_PS_DDR PS_DDR.SchDoc	U_ZU_POWER ZU_POWER.SchDoc
U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	U_POWER_3 POWER_3.SchDoc
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_4.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	U_TE0817-Overview TE0817-Overview.SchDoc
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	U_Power_Diagram Power_Diagram.SchDoc
U_B_GT_2 B_GT_2.SchDoc	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	

Special notes:



LOGO1
TE Logo PRINT Layer
LOGO PRINT

Serial
Serialnumber 6,3 x 6.3mm

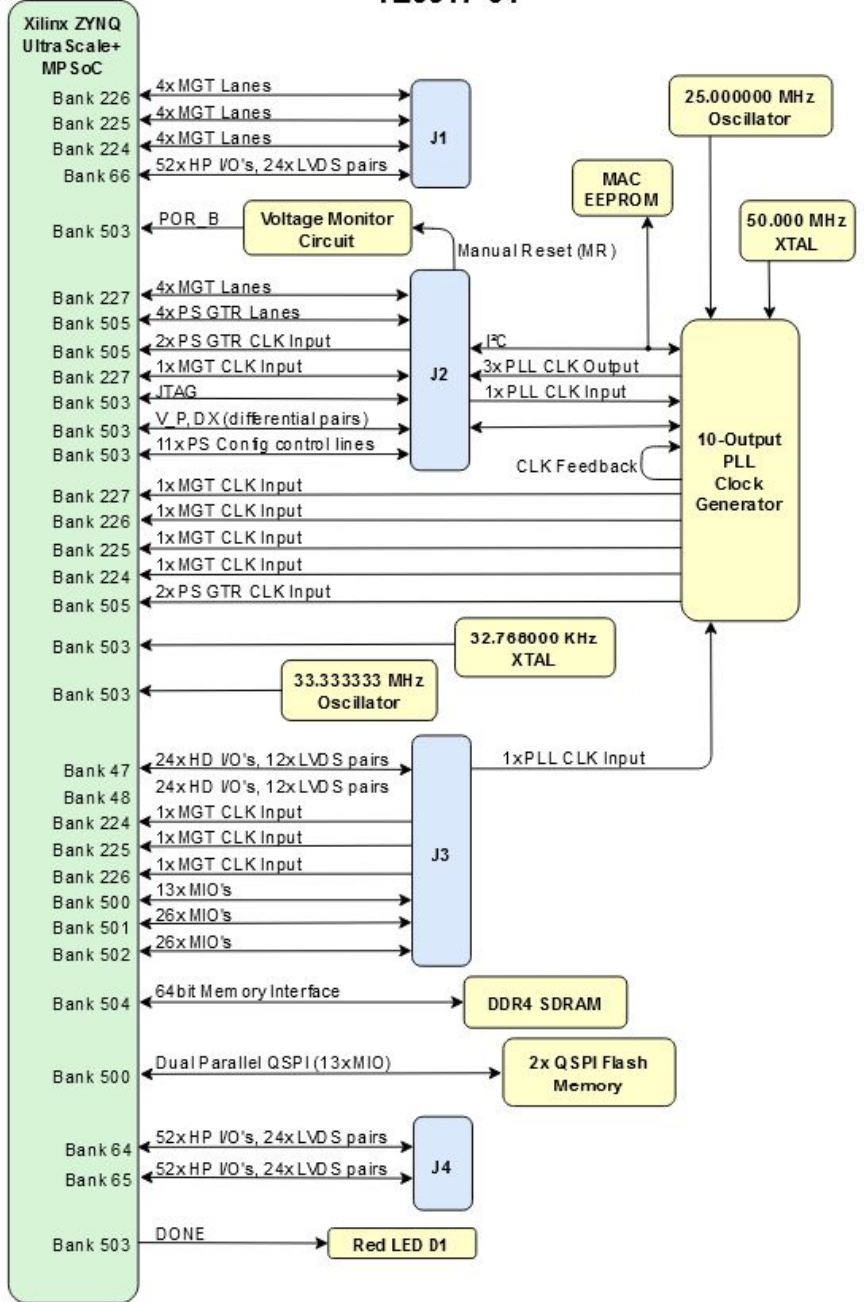
MECH1
TE Address Overlay
LOGO ADDRESS

Assembly variant	7NE21-A
Created by	ED
Modified by	VT
Modified at	2022-05-12
SVN Revision	12508

	Title: TE0817	
	A4	Number: TE0817 7NE21-A
	Date: 2021-08-25	Copyright: Trenz Electronic GmbH
	Filename: TE0817.SchDoc	

Rev.	01
Page 2	of 31

TE0817-01



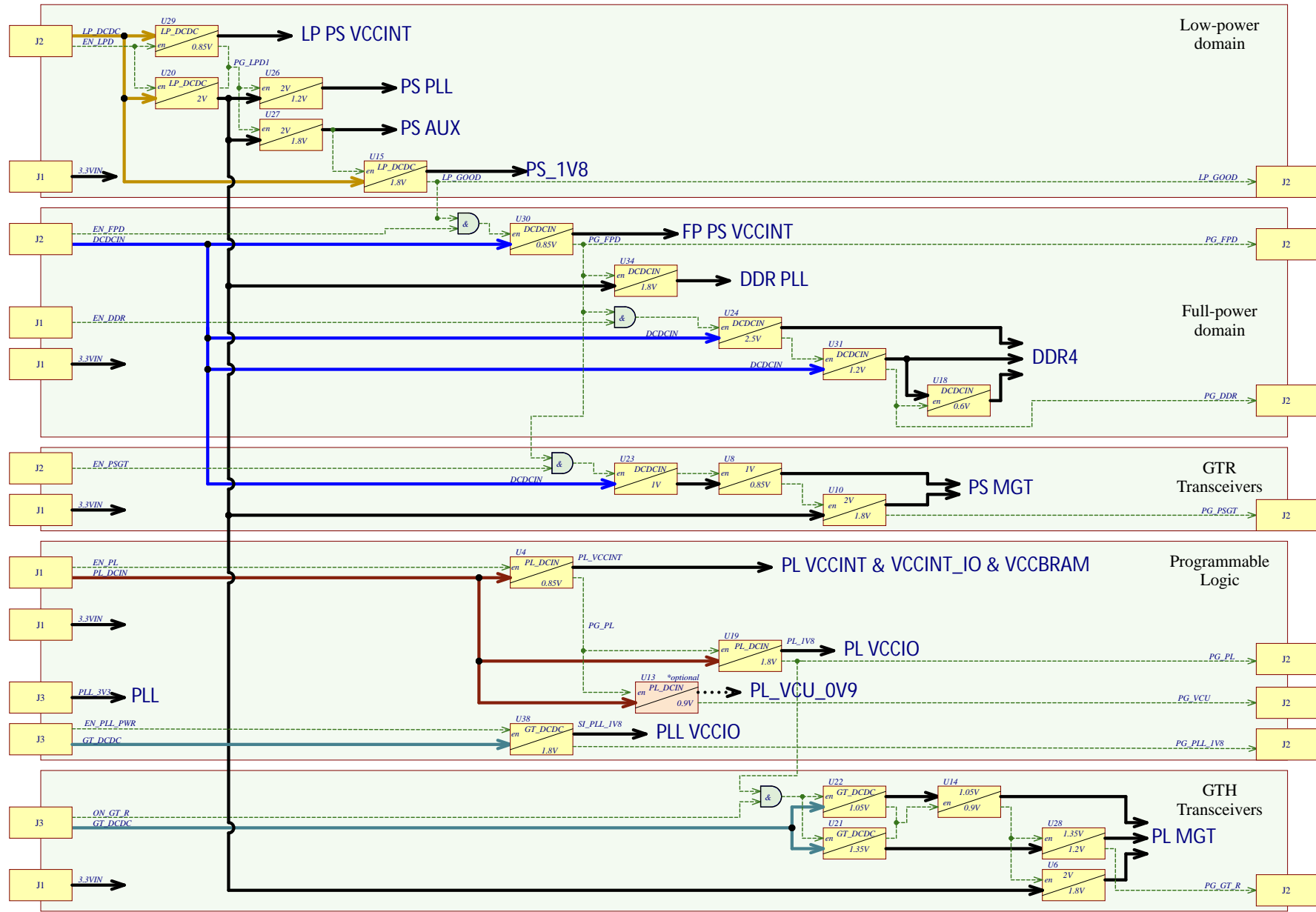
Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
PL_DCIN	IN	3.3 - 5.0V *	+/-5%	Micromodule Power	Programmable Logic, supplied by power rail
LP_DCDC	IN	3.3 - 5.0V	+/-5%	Micromodule Power	Low-Power Domain, supplied by power rail
GT_DCDC	IN	3.3 - 5.0V	+/-5%	Micromodule Power	GTH/GTY Transceiver, supplied by power rail
DCDCIN	IN	3.3 - 5.0V	+/-5%	Micromodule Power	Full-Power Domain and GTR, supplied by power rail
VCCO_64	IN	1.0 - 1.8V	+/-3%	HP IO Bank64	-
VCCO_65	IN	1.0 - 1.8V	+/-3%	HP IO Bank65	-
VCCO_66	IN	1.0 - 1.8V	+/-3%	HP IO Bank66	-
VCCO_47	IN	1.2 - 3.3V	+/-3%	HD IO Bank47	-
VCCO_48	IN	1.2 - 3.3V	+/-3%	HD IO Bank48	-
PSBATT	IN	1.2 - 1.5V	-	RTC / BBRAM	-
PLL_3V3	IN	3.3V	+/-5%	PLL Analog Power	-
PL_1V8	OUT	1.8V	+/-5%	Power for Carrier	Micromodule: Programmable Logic
PS_1V8	OUT	1.8V	+/-5%	Power for Carrier	Micromodule: Processing System
DDR_1V2	OUT	1.2V	+/-5%	Power for Carrier	Micromodule: PS DDR I/O Supply

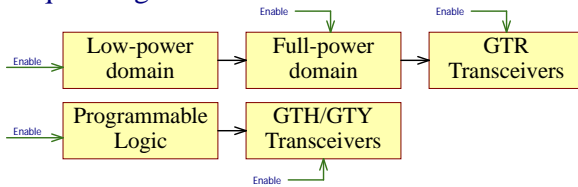
* for Micromodules, where U4 is TPS548A28RWR or MPQ8633BGL-Z maximum Vin range will be 3.3V



Title: TE0817		
A4	Number: TE0817 7NE21-A	Rev. 01
Date: 2022-11-08	Copyright: Trenz Electronic GmbH	Page 3 of 31
Filename: TE0817-Overview.SchDoc		



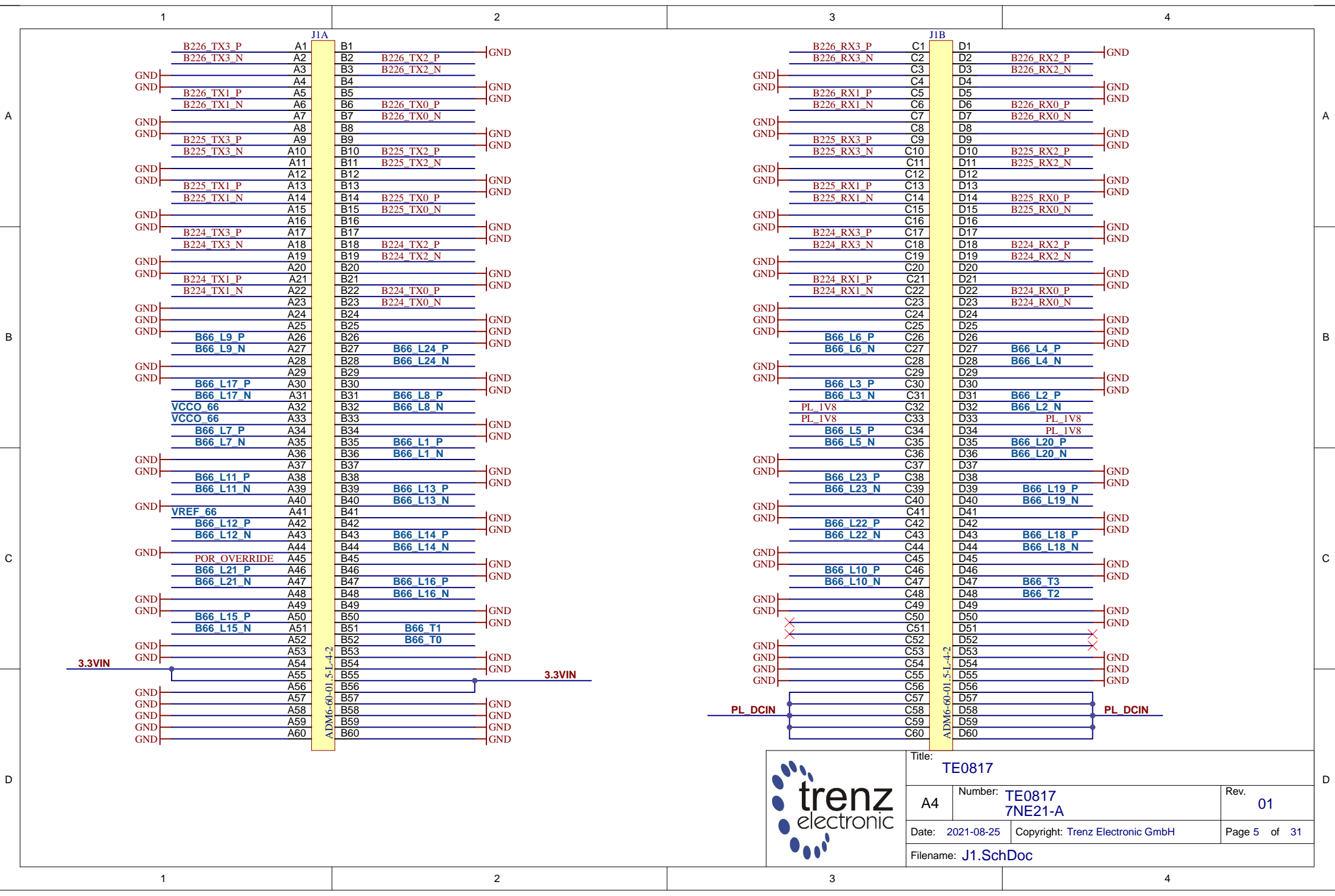
Power-on sequencing:



- EN_GT_R Net name
- Power bus
- Control signal
- Power bus in FPGA speedgrade -1/2/-3 assembly variants
- Power bus in FPGA speedgrade -1L/-2L assembly variants (low power)
- Optional power converter
- Logic AND gate



Title: TE0817		
A3	Number: TE0817 7NE21-A	Rev. 01
Datum: 2021-05-17	Copyright: Trenz Electronic GmbH	Page 4 of 31
Filename: Power_Diagram.SchDoc		



Title: TE0817		
A4	Number: TE0817 7NE21-A	Rev. 01
Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 5 of 31
Filename: J1.SchDoc		

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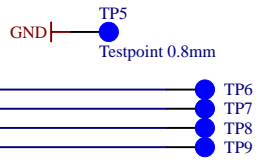
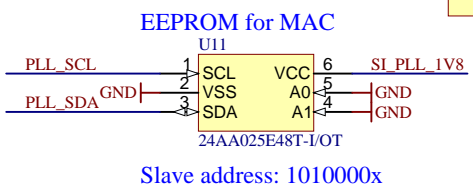
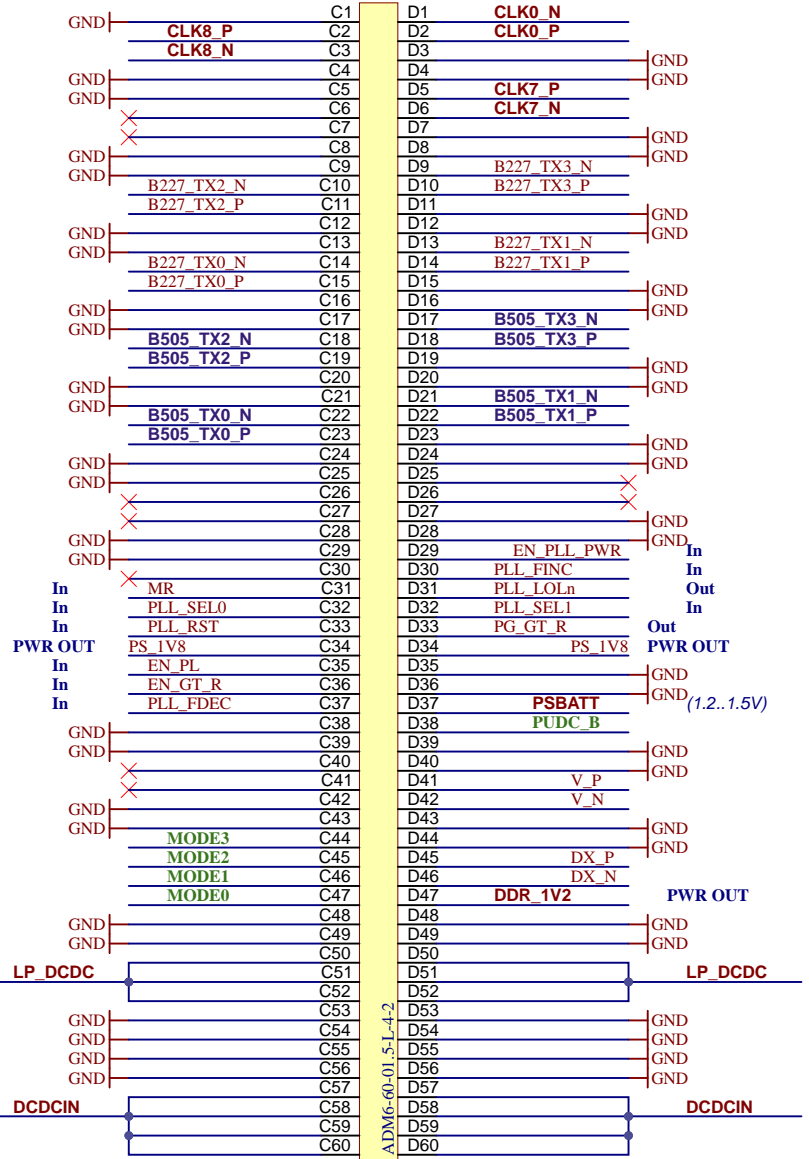
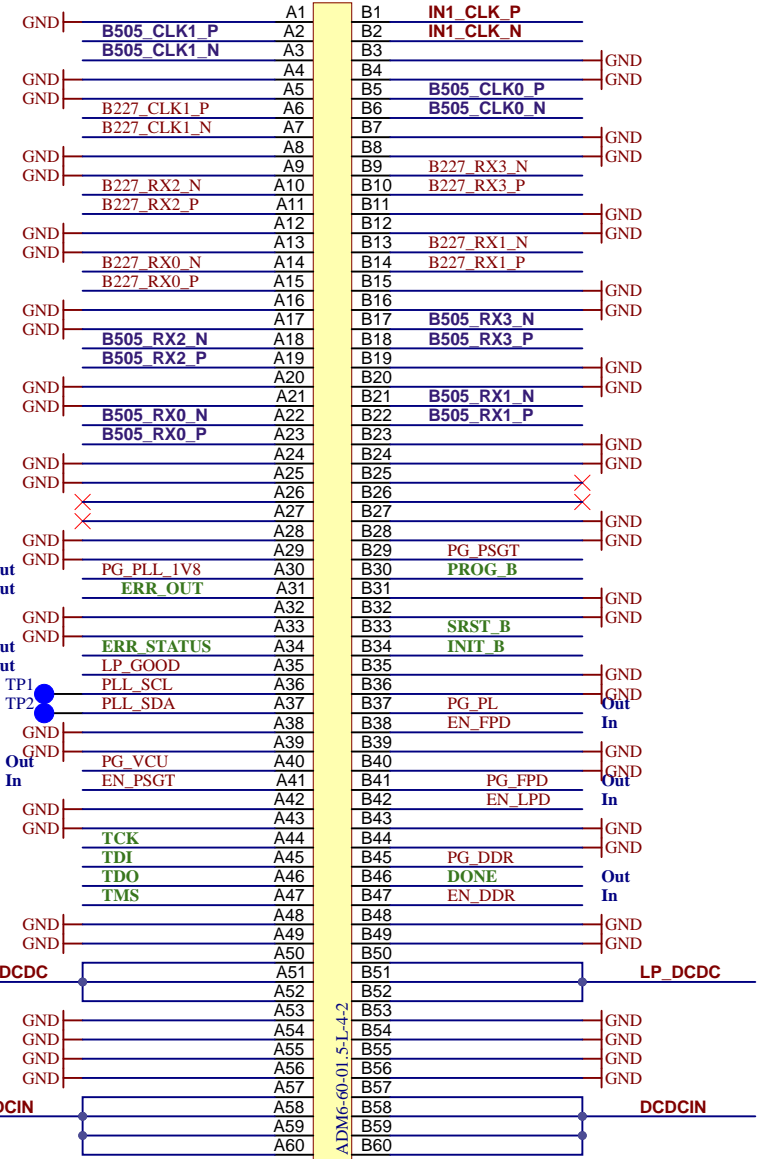
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J2A
ADM6-60-01_5-L-4-2

J2B
ADM6-60-01_5-L-4-2



Title: TE0817		
A4	Number: TE0817 7NE21-A	Rev. 01
Date: 2022-11-08	Copyright: Trenz Electronic GmbH	Page 6 of 31
Filename: J2.SchDoc		

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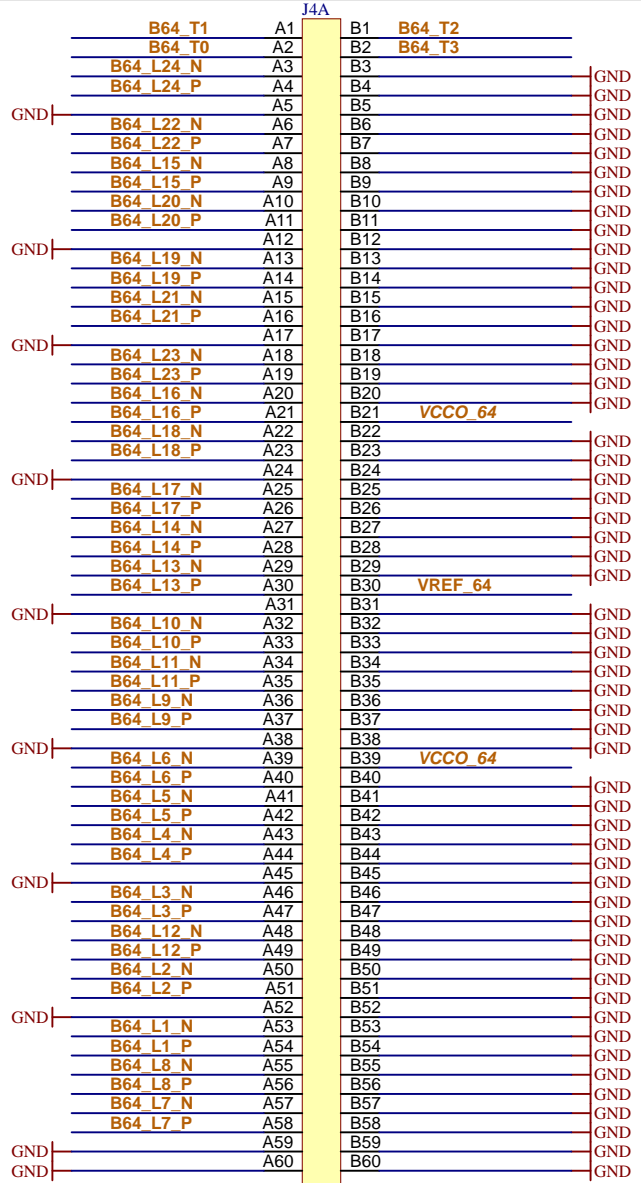
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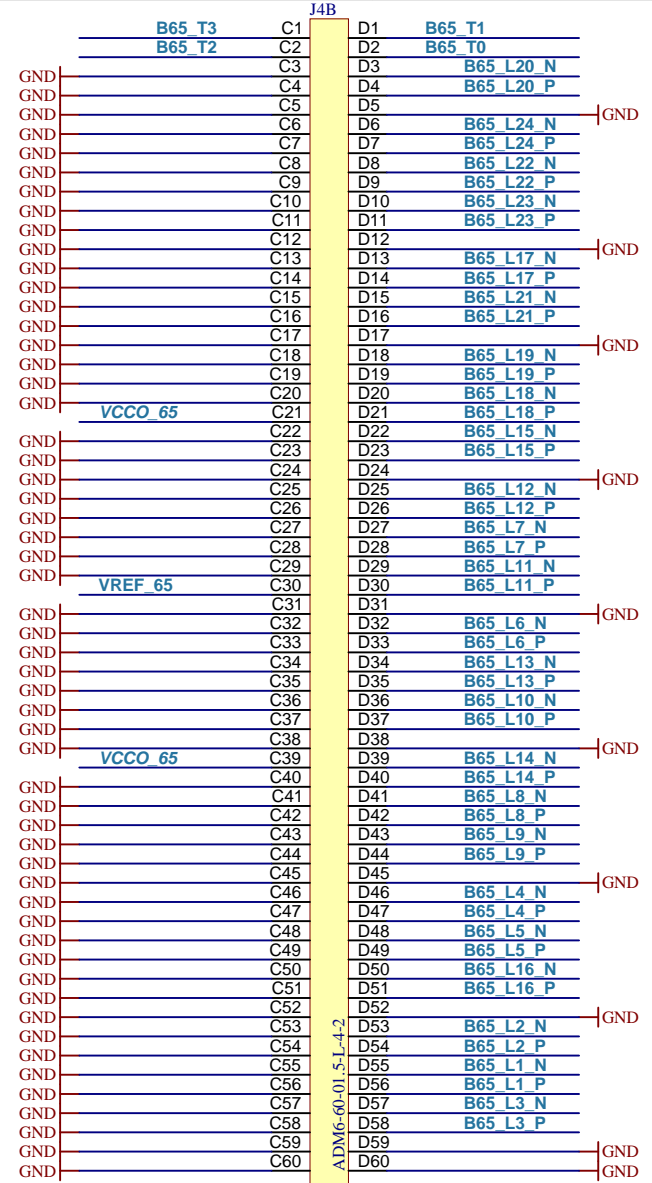
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ADM6-60-01.5-L-4-2



ADM6-60-01.5-L-4-2



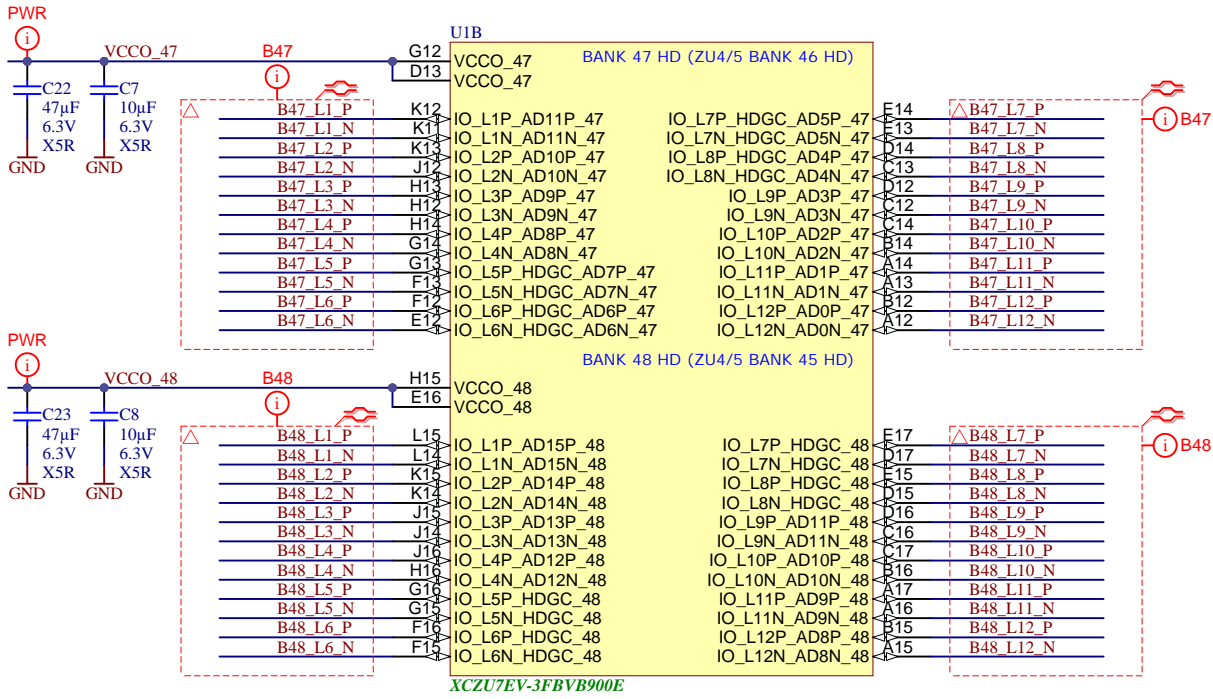

Title: TE0817		
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Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 8 of 31
Filename: J4.SchDoc		

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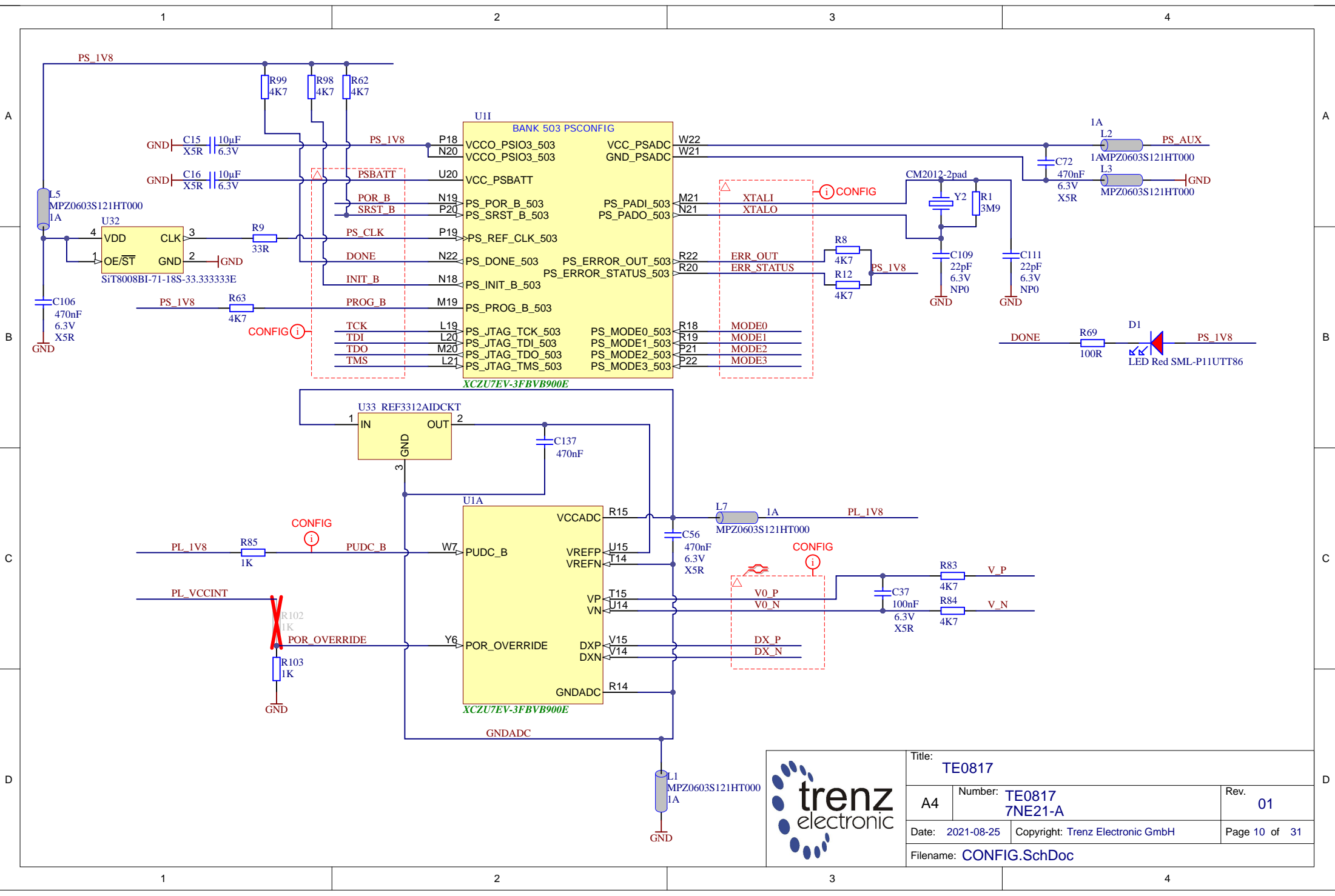
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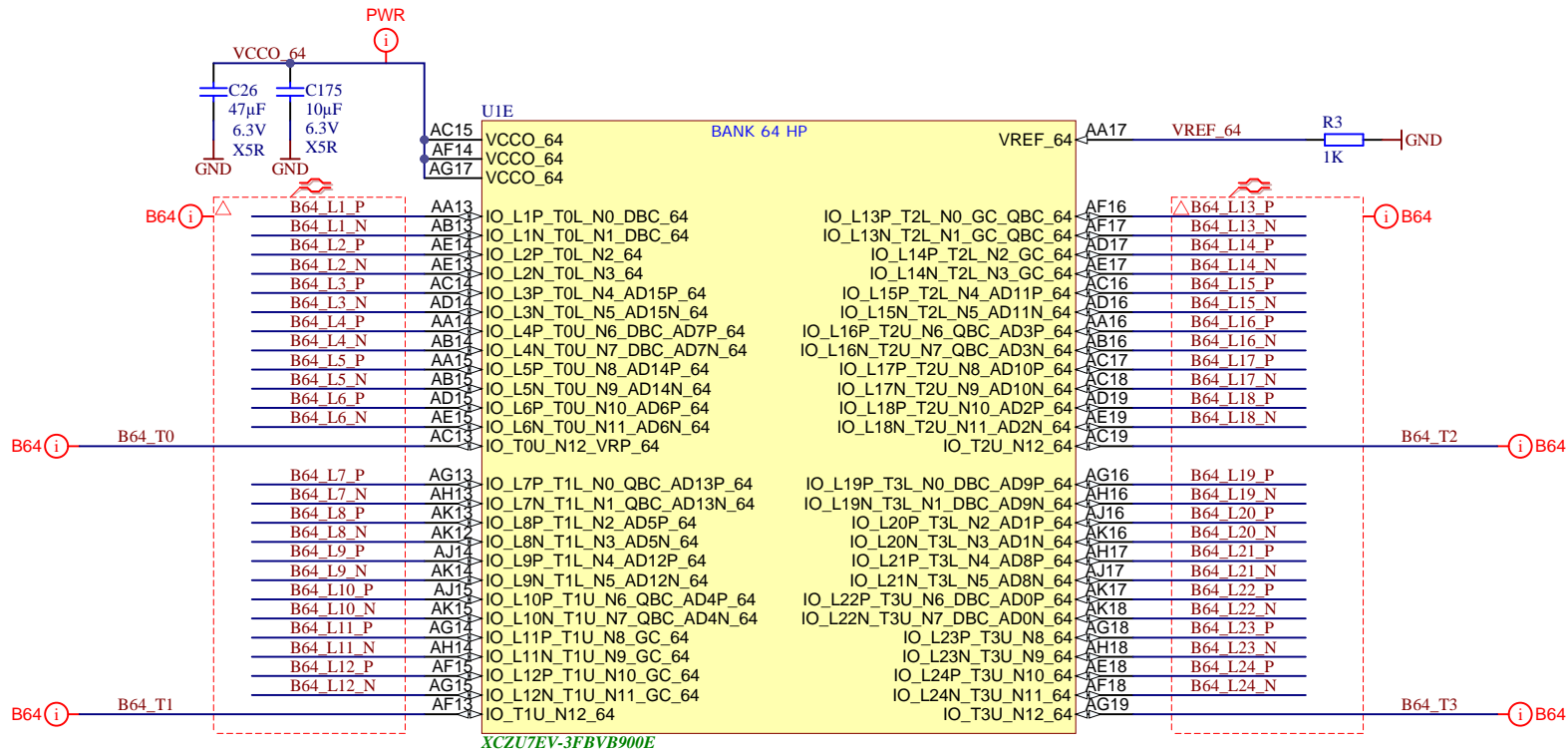
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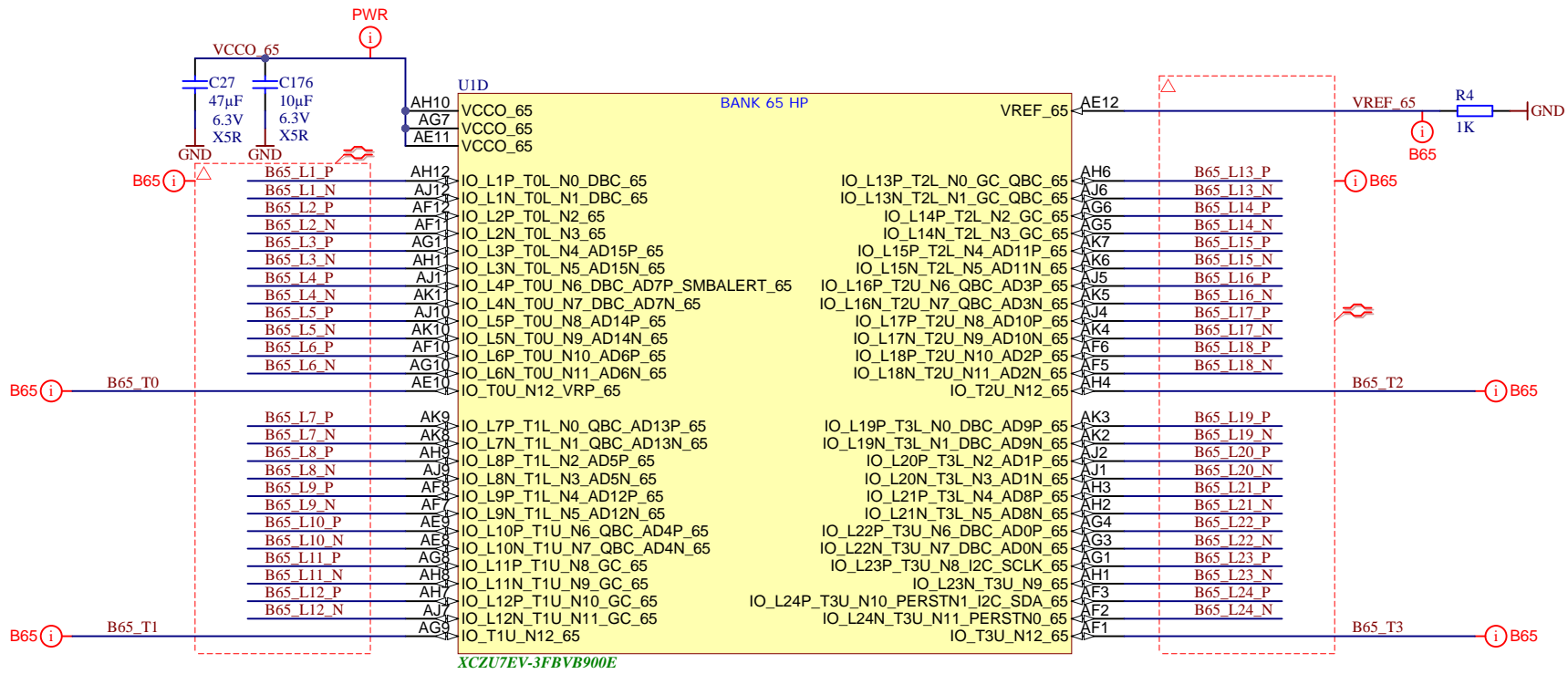
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Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 9 of 31
Filename: B_HD.SchDoc		



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A4	Number: TE0817 7NE21-A	Rev. 01
Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 10 of 31
Filename: CONFIG.SchDoc		



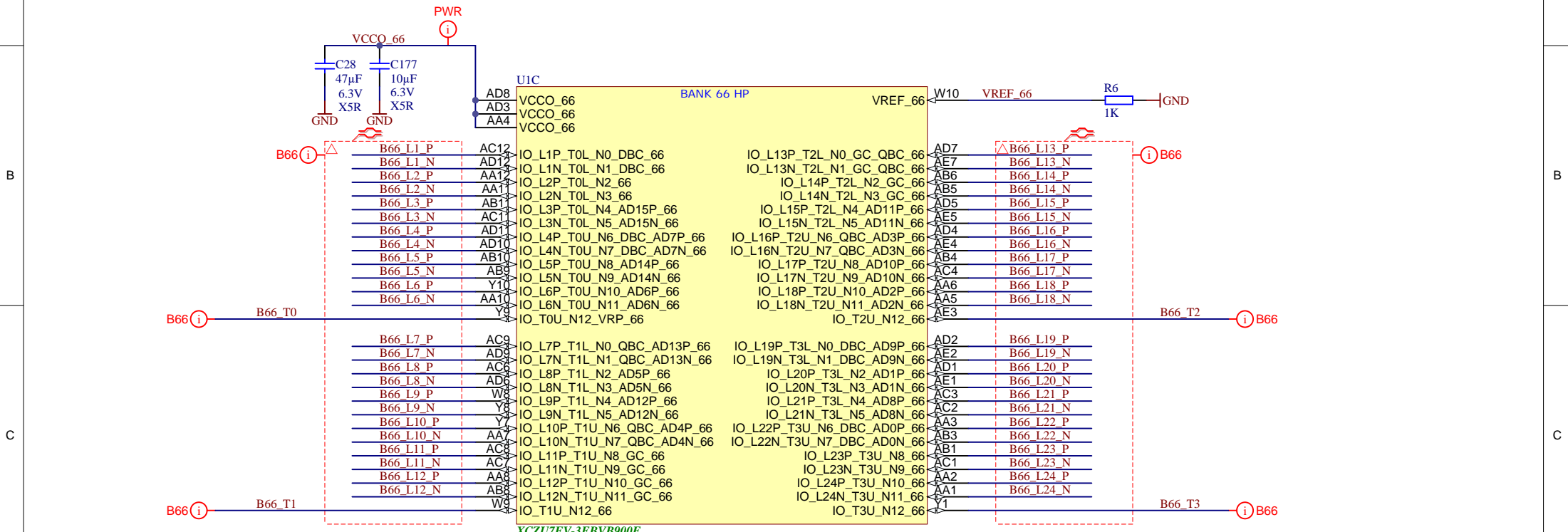
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Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 11 of 31
Filename: B64.SchDoc		




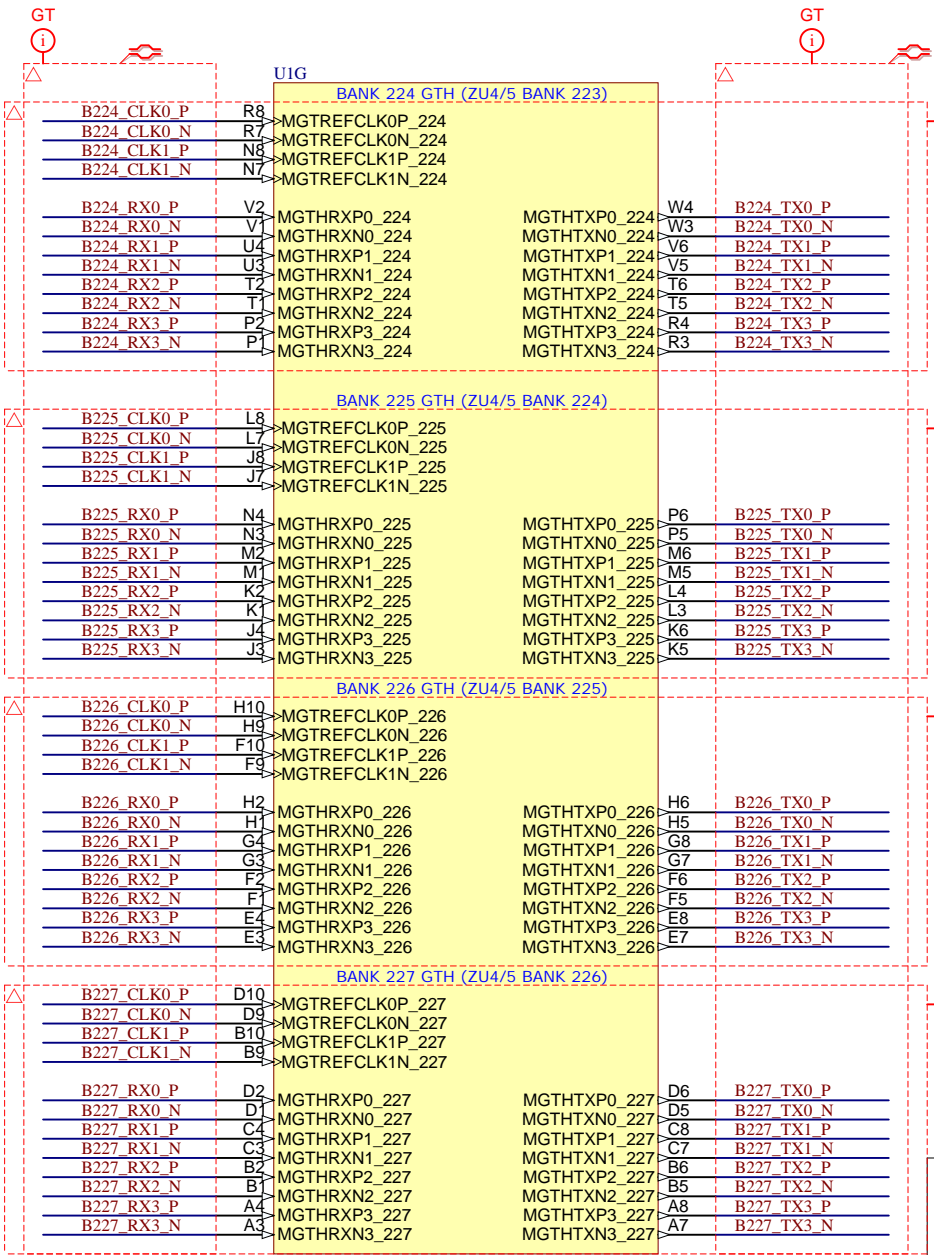
XCZU7EV-3FBVB900E



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Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 12 of 31
Filename: B65.SchDoc		



		Title: TE0817	
		A4	Number: TE0817 7NE21-A
Date: 2021-08-25		Copyright: Trenz Electronic GmbH	
Filename: B66.SchDoc		Rev. 01	
Page 13 of 31			



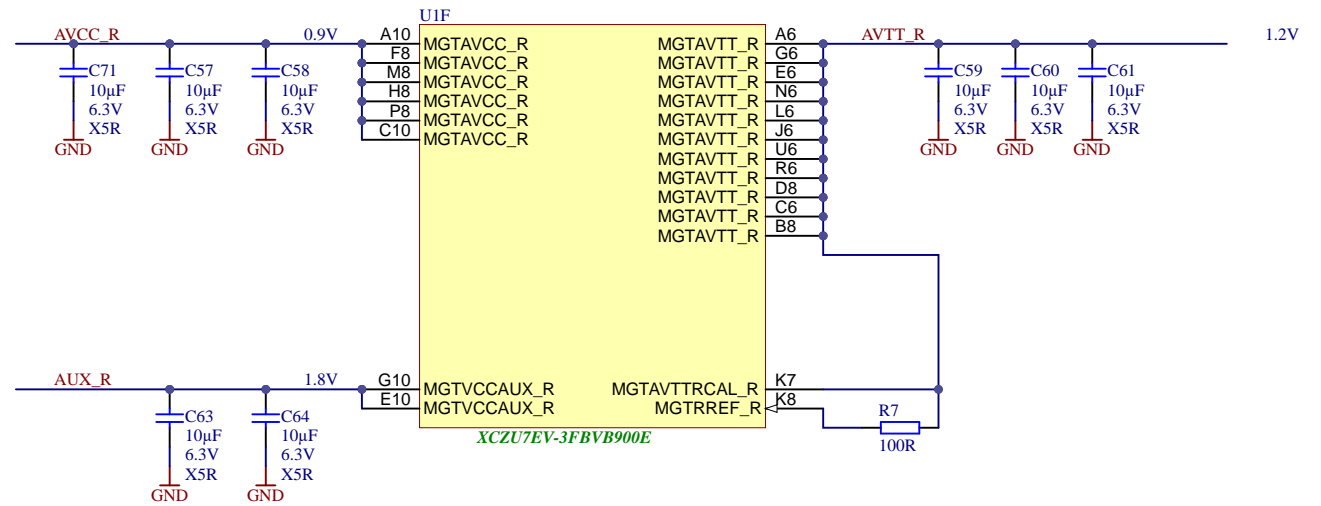
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229

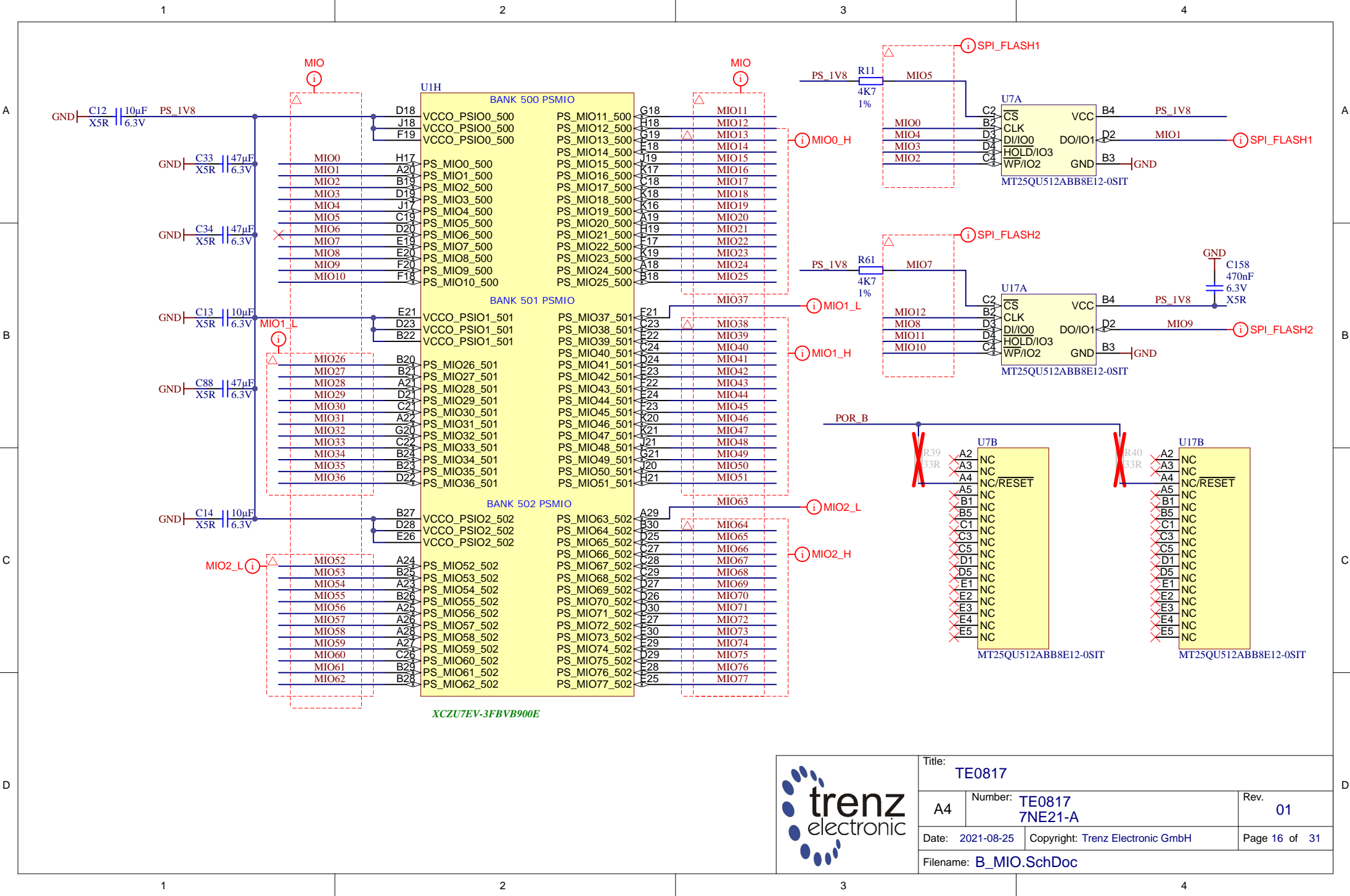
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Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 14 of 31
Filename: B_GT.SchDoc		



		Title: TE0817	
		A4	Number: TE0817 7NE21-A
Date: 2021-08-25		Copyright: Trenz Electronic GmbH	
Date: 2021-08-25		Page 15 of 31	
Filename: B_GT_2.SchDoc			



	Title: TE0817	
	A4	Number: TE0817 7NE21-A
	Date: 2021-08-25	Copyright: Trenz Electronic GmbH
	Filename: B_MIO.SchDoc	

Rev. **01**
Page 16 of 31

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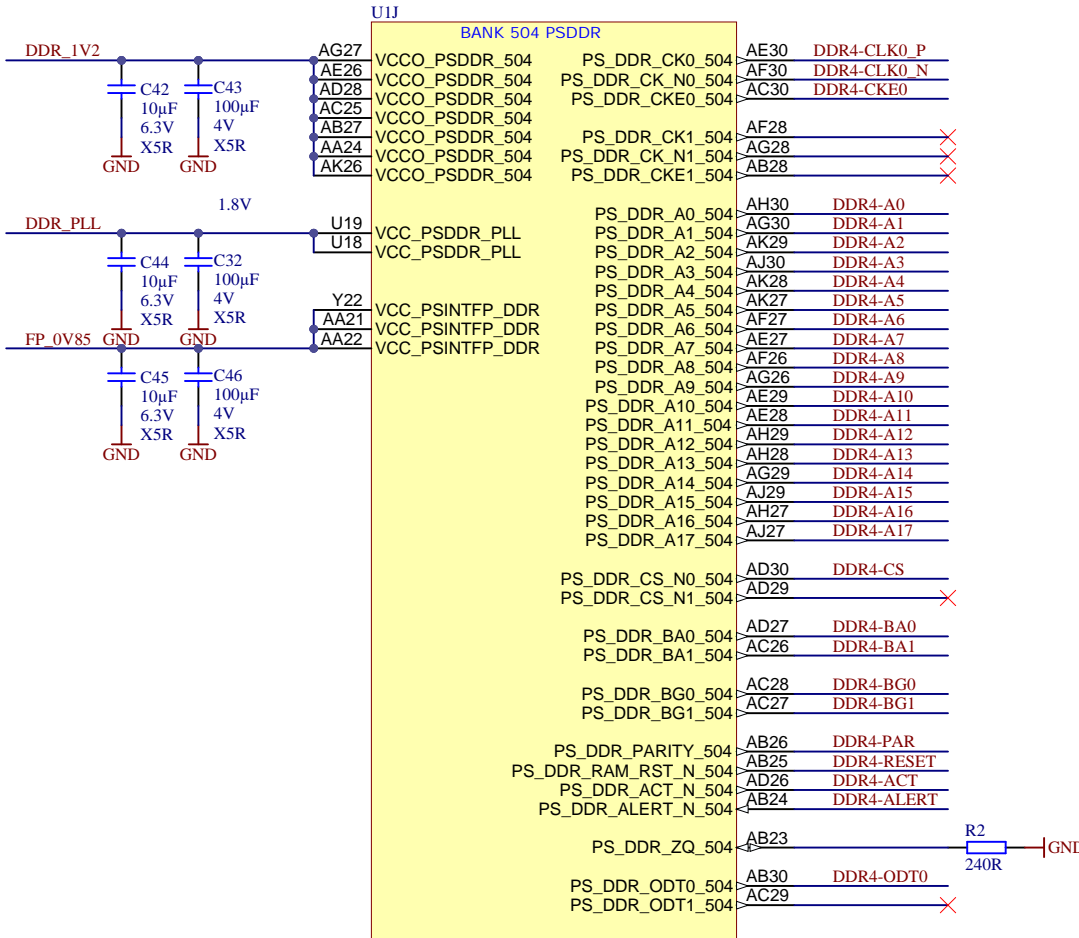
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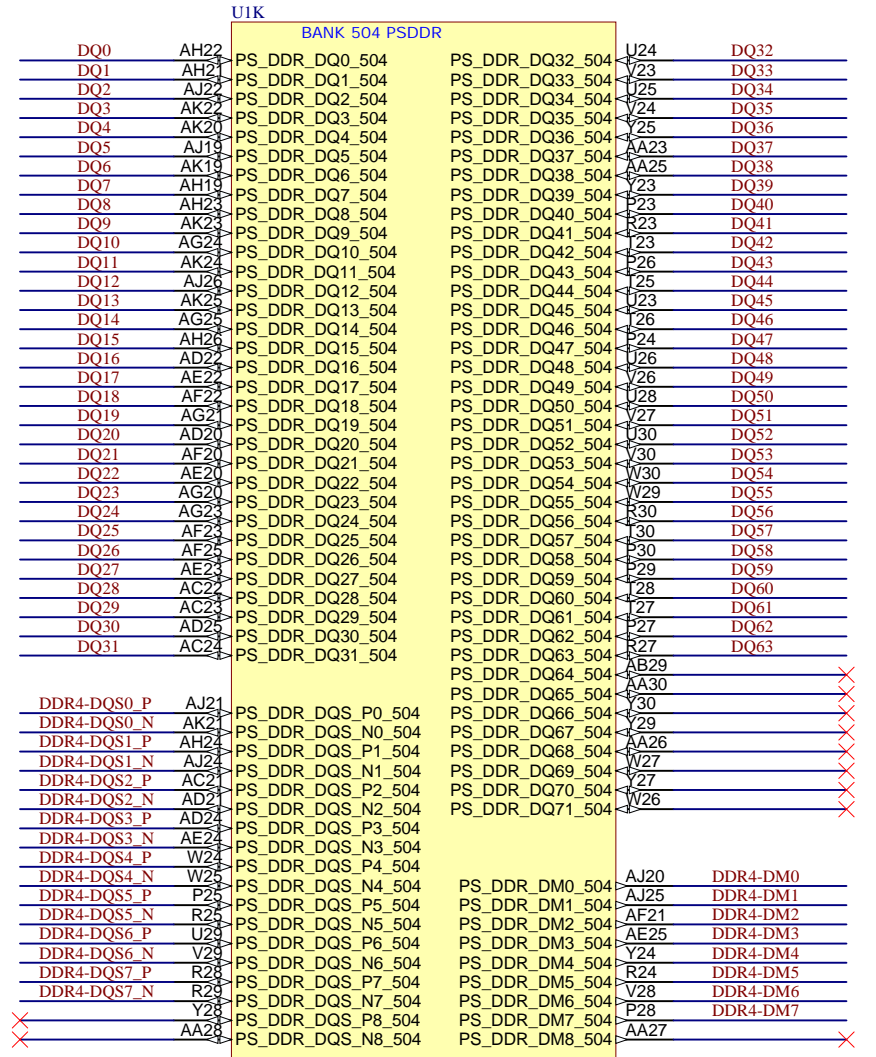
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XCZU7EV-3FBVB900E



XCZU7EV-3FBVB900E



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Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 17 of 31
Filename: PS_DDR.SchDoc		

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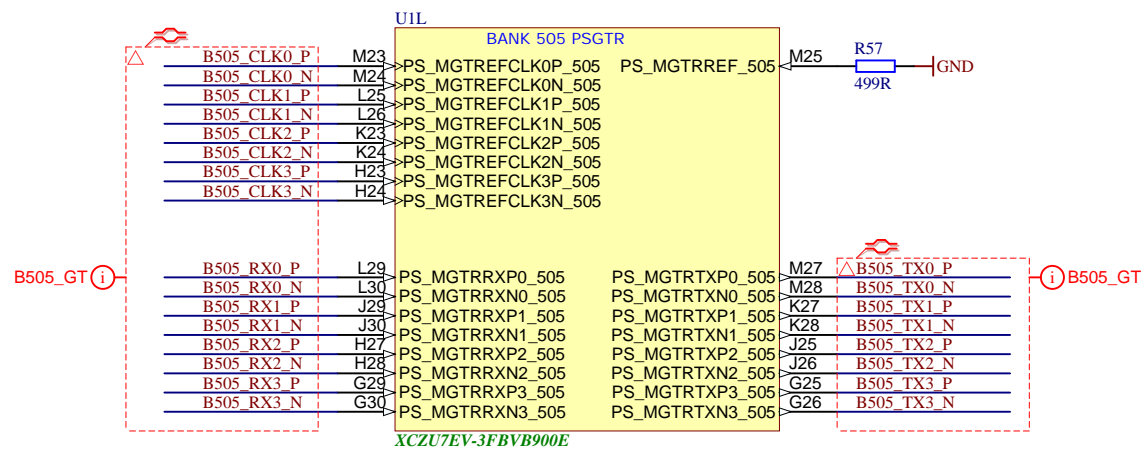
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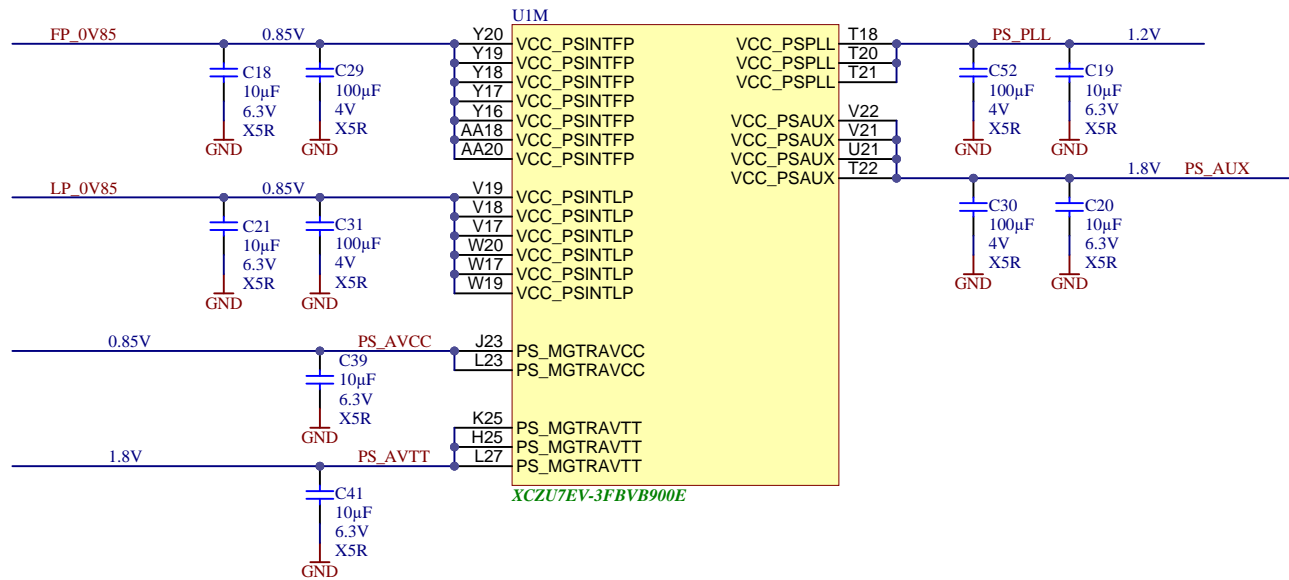
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Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 18 of 31
Filename: B_PS_GT.SchDoc		


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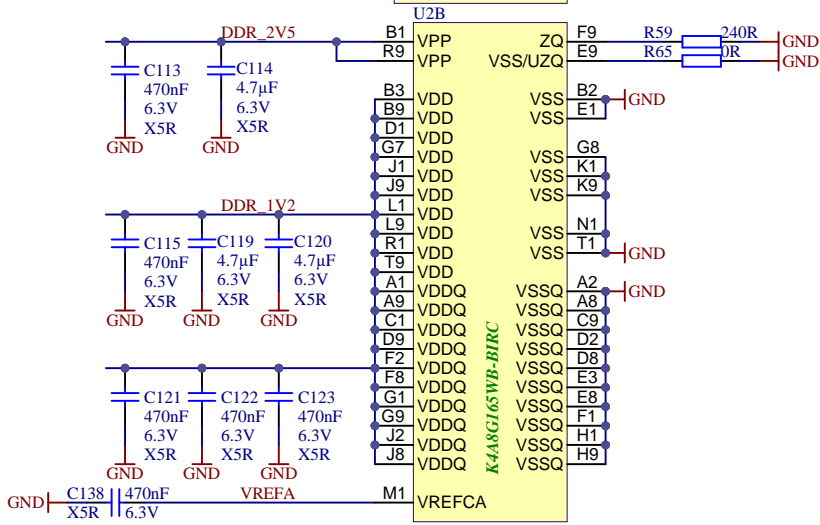
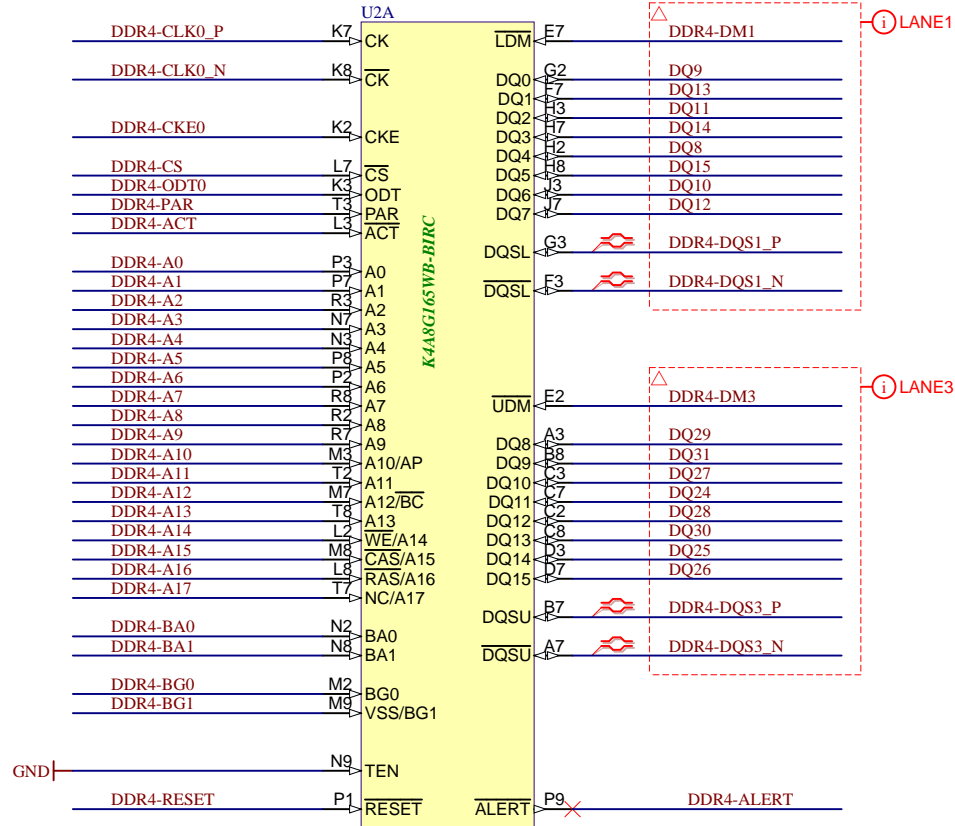
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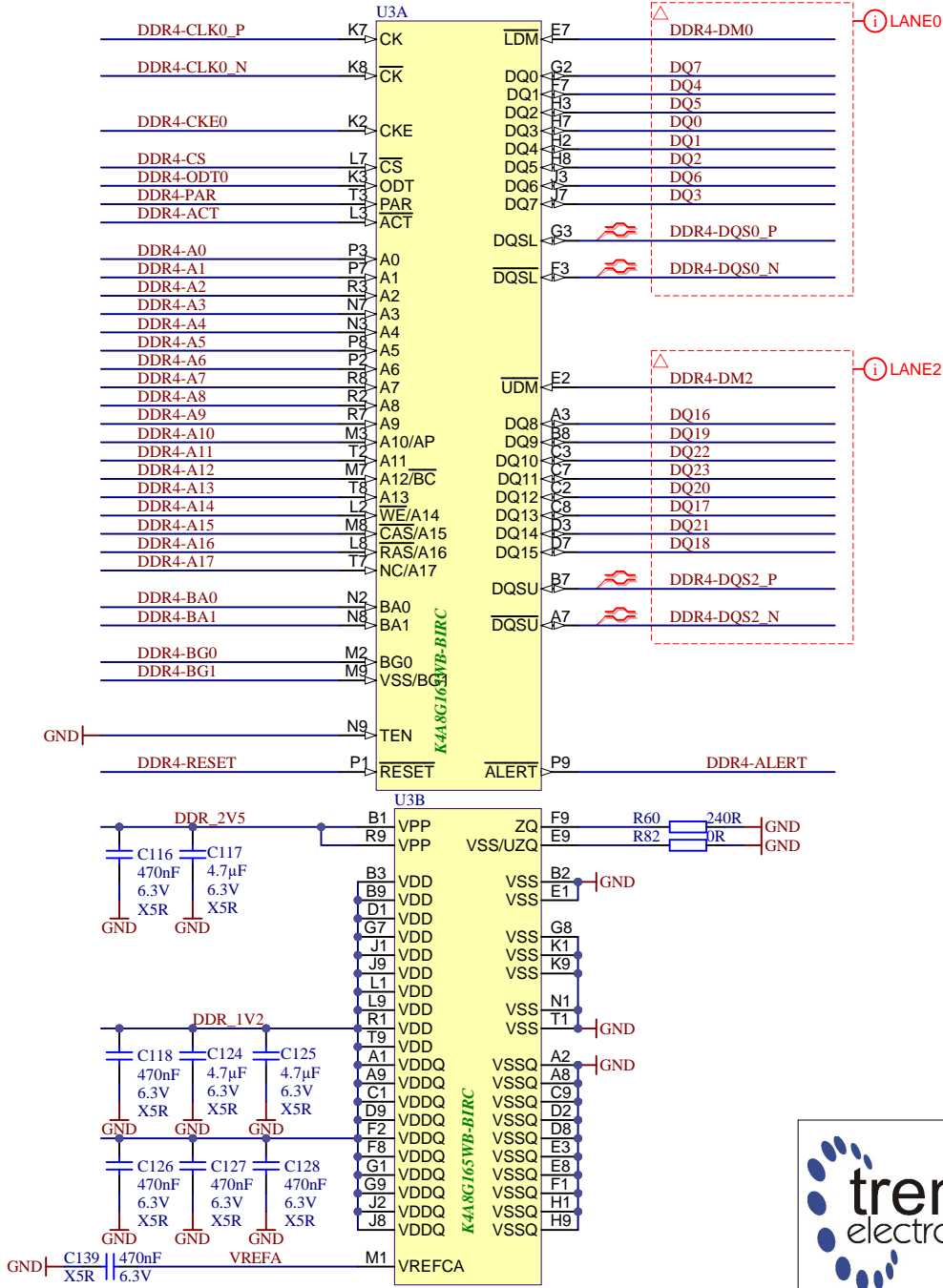
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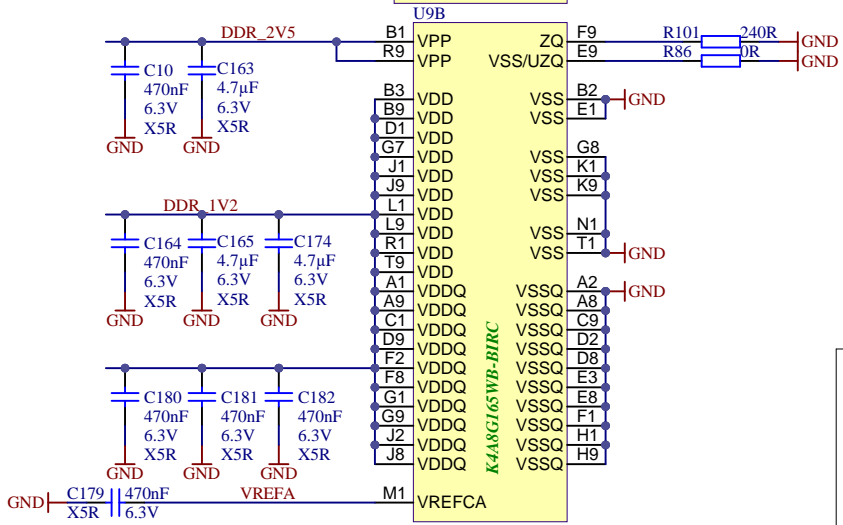
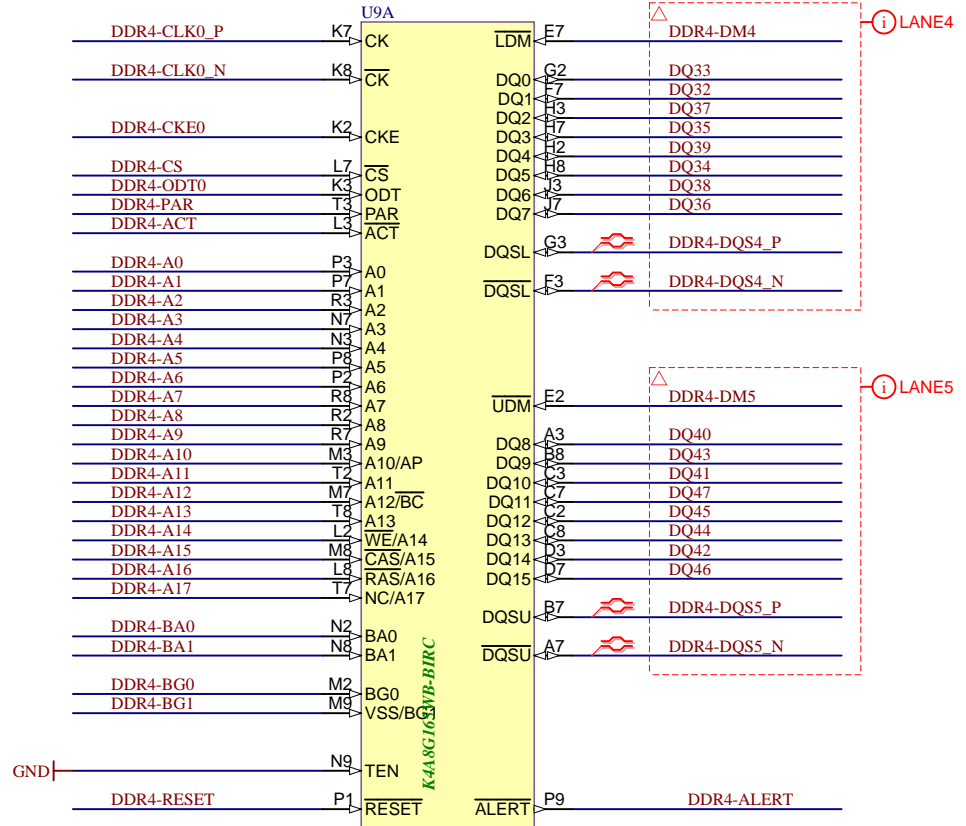
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	Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 19 of 31
	Filename: ZU_PS_POWER.SchDoc		



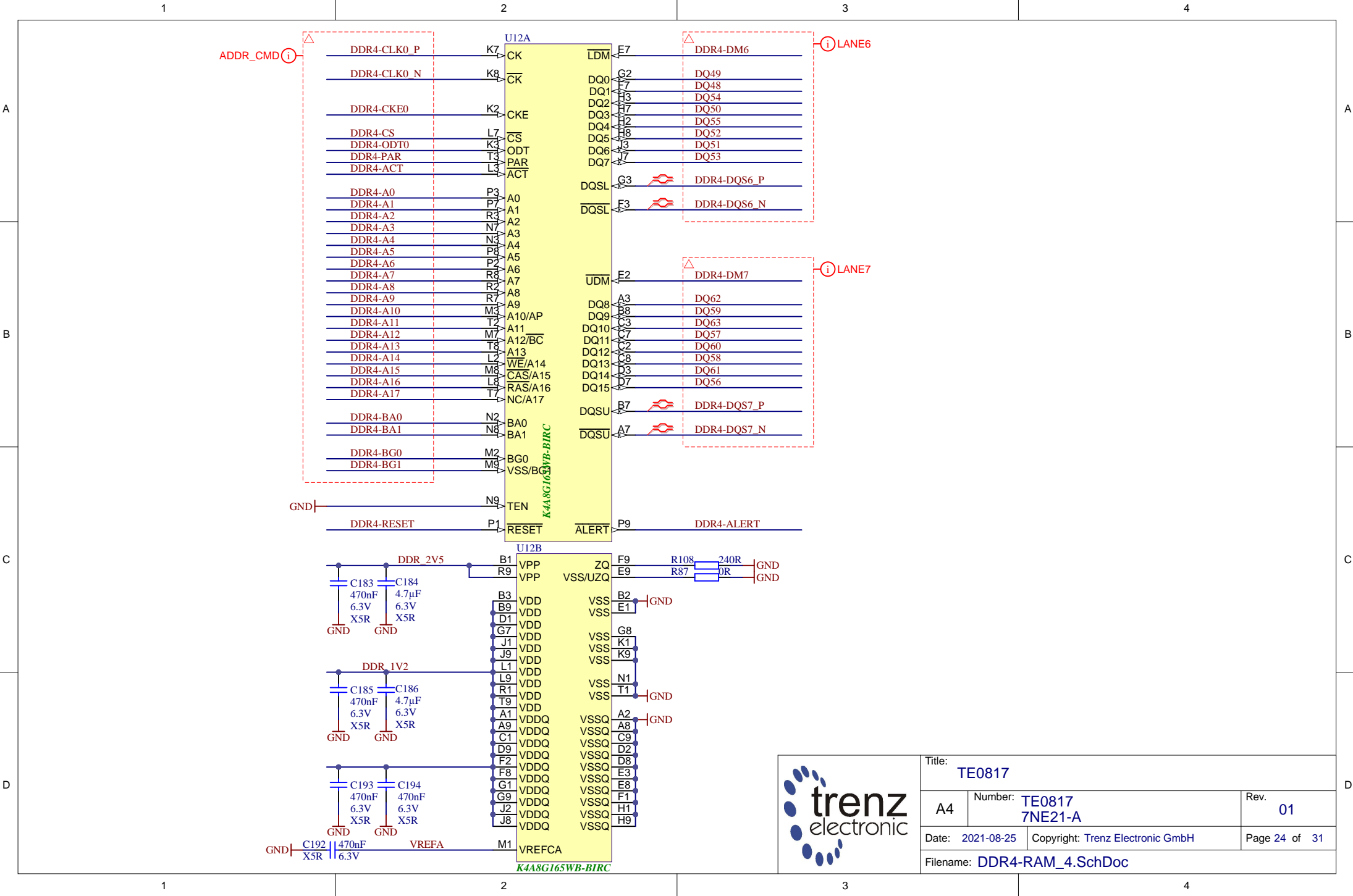
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Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 21 of 31
Filename: DDR4-RAM.SchDoc		



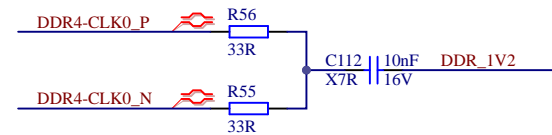
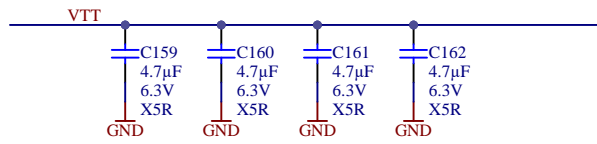
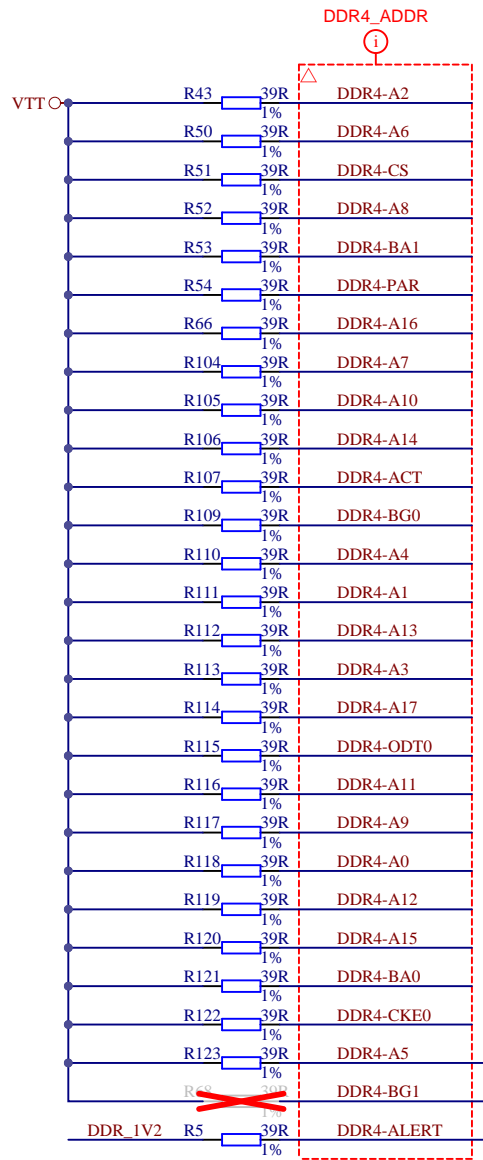
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Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 22 of 31
Filename: DDR4-RAM_2.SchDoc		



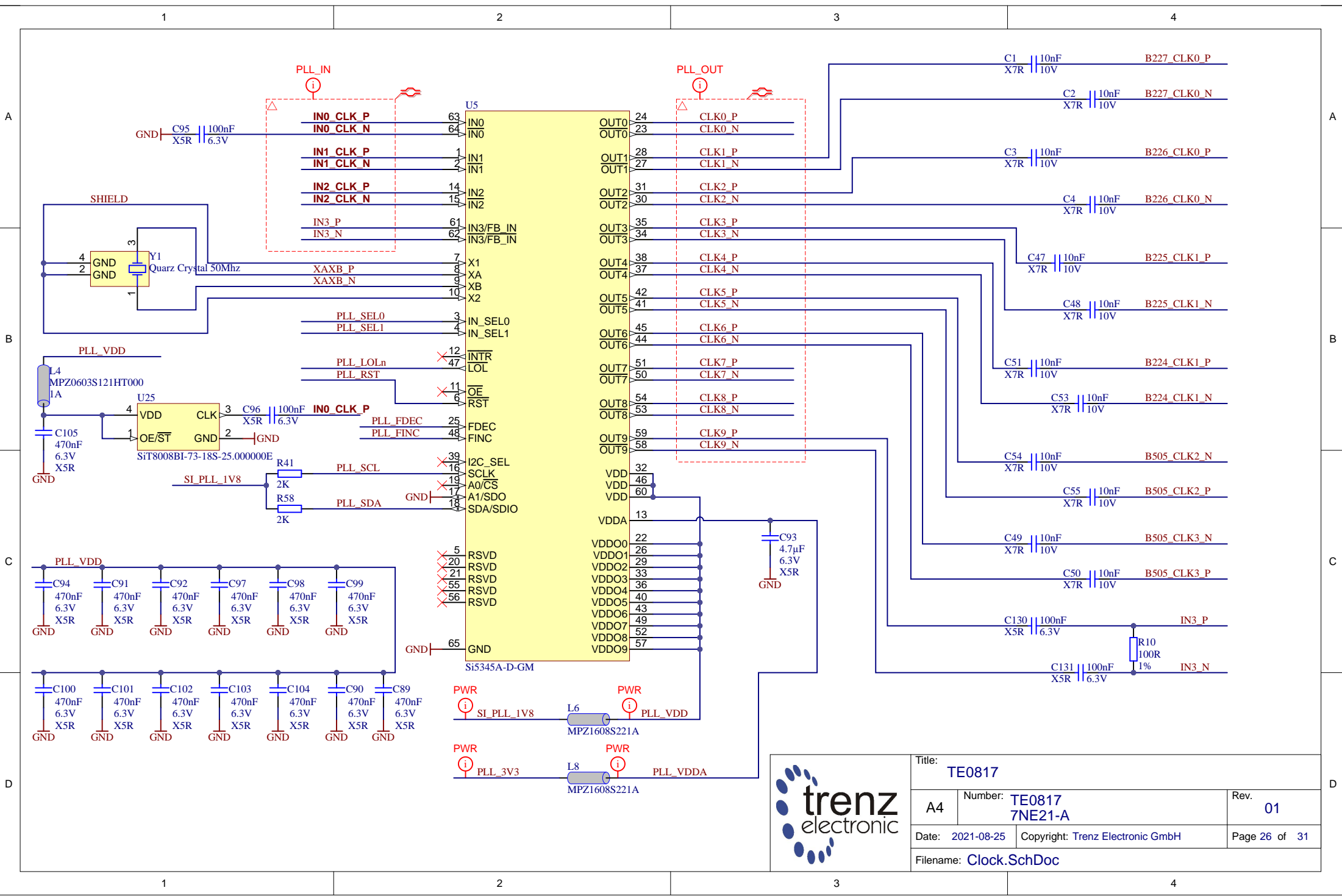
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A4	Number: TE0817 7NE21-A	Rev. 01
Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 23 of 31
Filename: DDR4-RAM_3.SchDoc		



Title: TE0817		
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Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 24 of 31
Filename: DDR4-RAM_4.SchDoc		

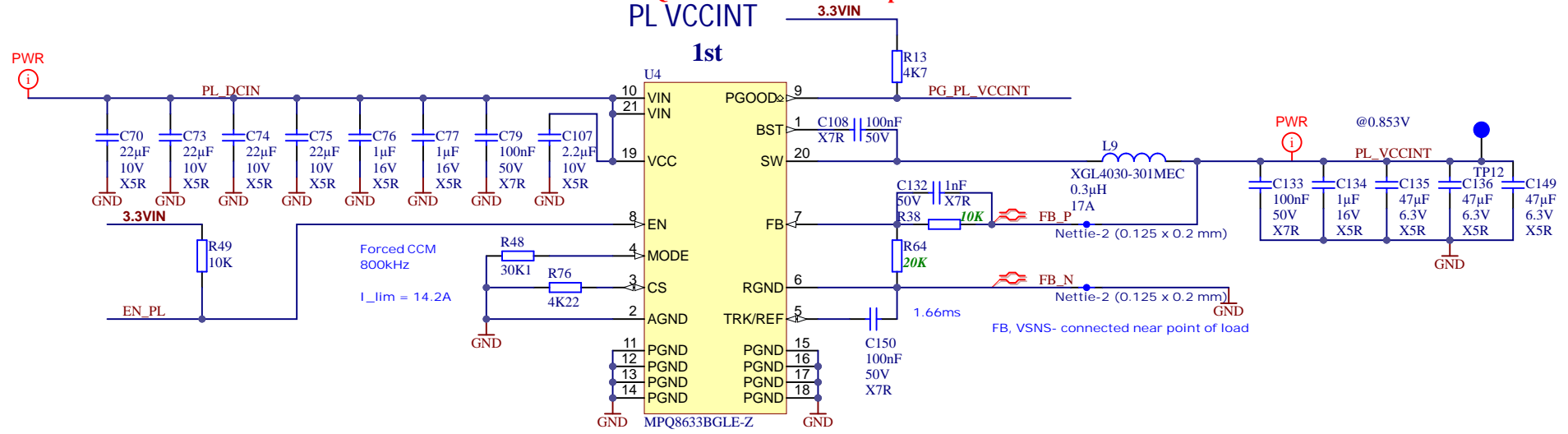


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Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 25 of 31
Filename: DDR4-TERM.SchDoc		

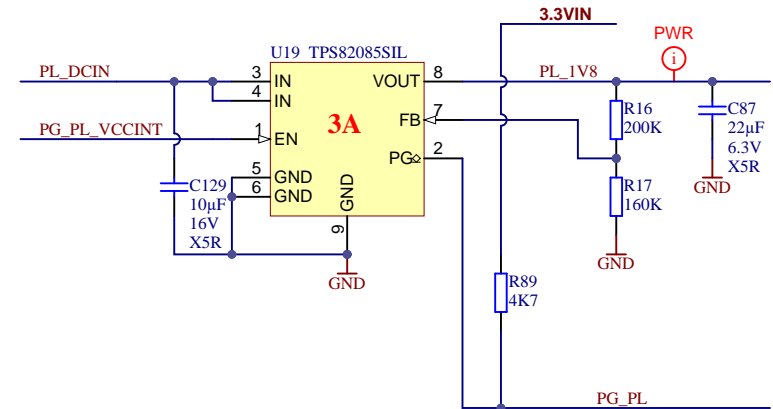
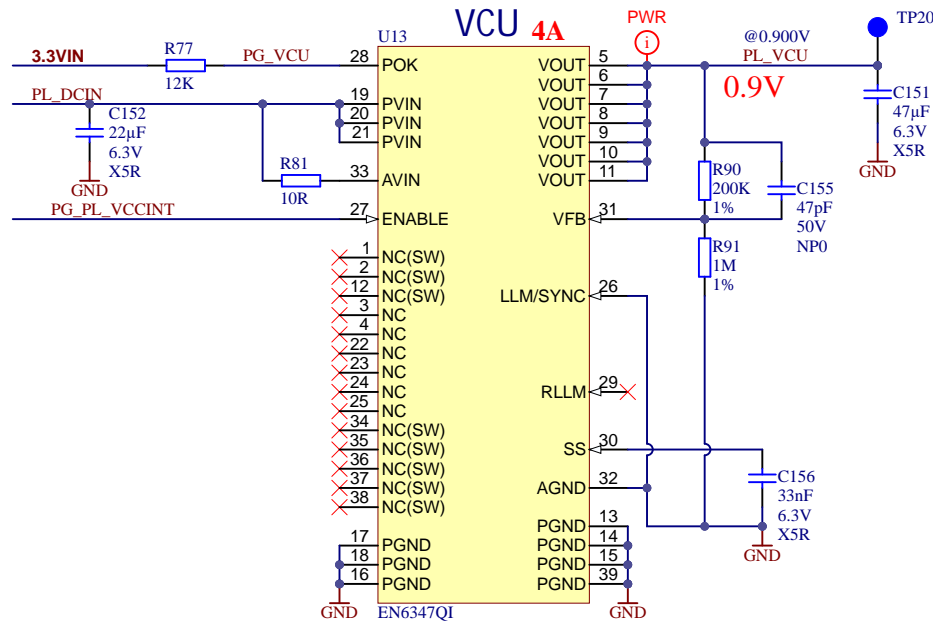


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Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 26 of 31
Filename: Clock.SchDoc		

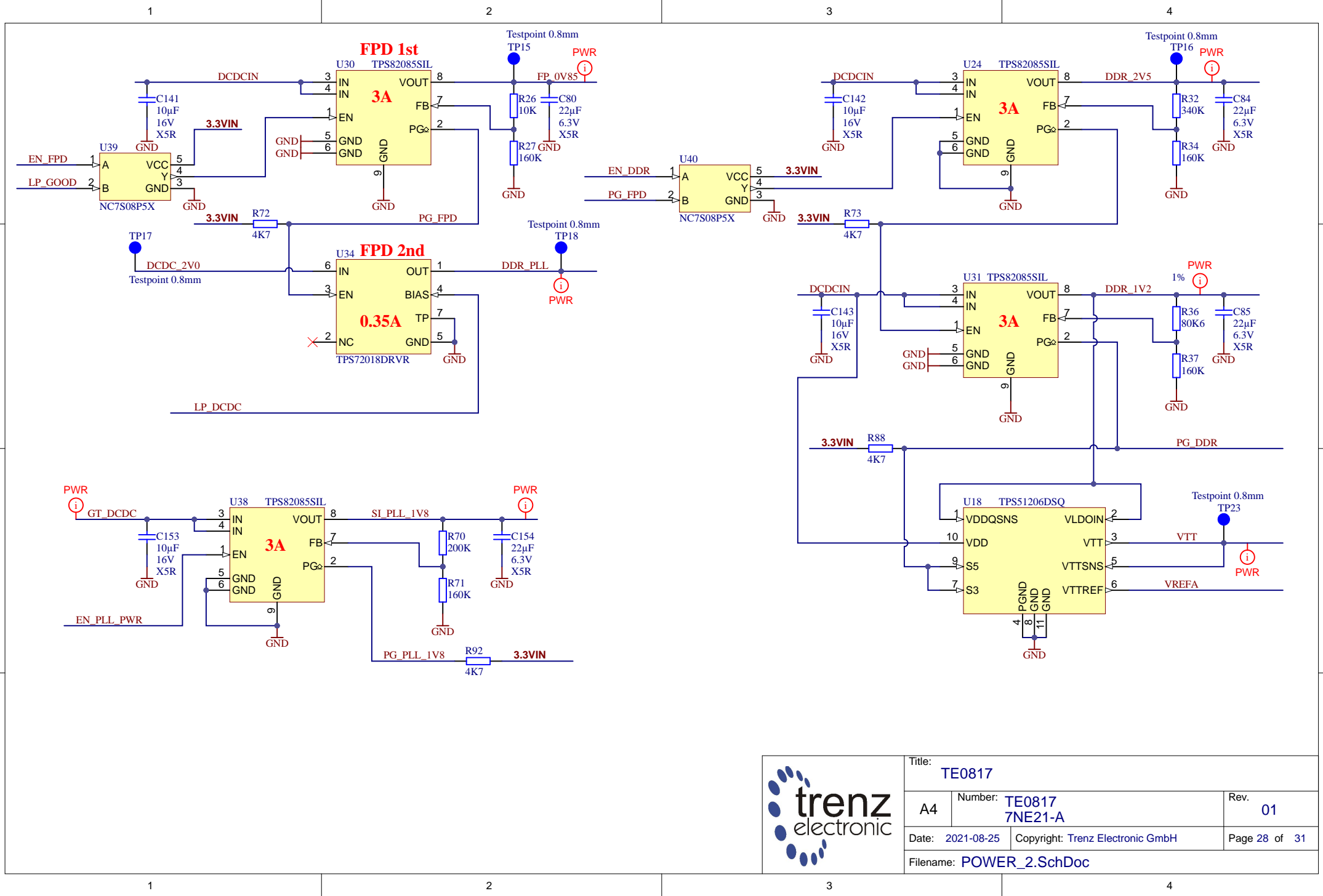
U4 can be TPS548A28RWWR or MPQ8633BGLE-Z which is up to Trenz Electronic GmbH.




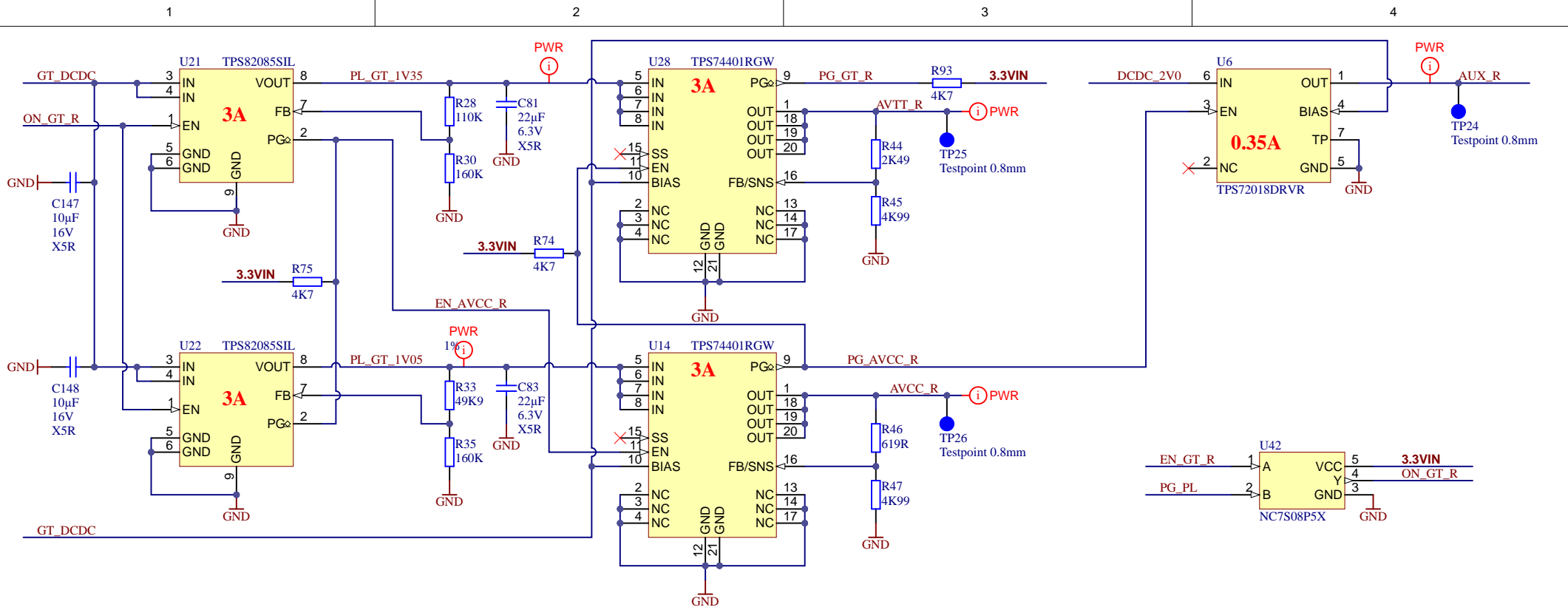
U4 pin compatible with
 -- TPS54JA20 (12A)
 -- TPS548A28 (15A)
 -- TPS548B28 (20A)



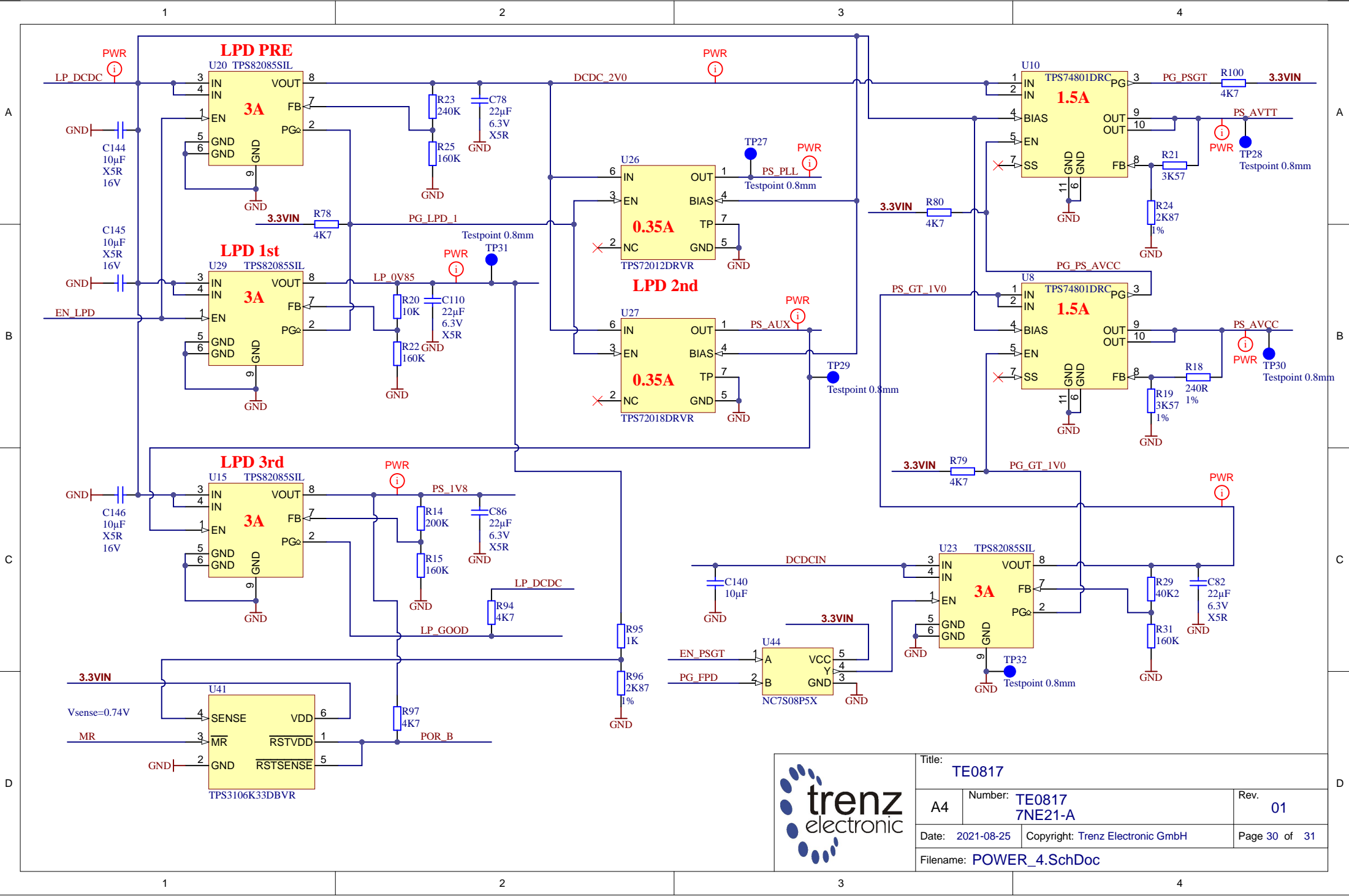
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Date: 2022-11-03	Copyright: Trenz Electronic GmbH	Page 27 of 31
Filename: POWER.SchDoc		



		Title: TE0817	
		A4	Number: TE0817 7NE21-A
Date: 2021-08-25		Copyright: Trenz Electronic GmbH	
Filename: POWER_2.SchDoc		Page 28 of 31	



Title: TE0817		
A4	Number: TE0817 7NE21-A	Rev. 01
Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 29 of 31
Filename: POWER_3.SchDoc		



Title: TE0817		
A4	Number: TE0817 7NE21-A	Rev. 01
Date: 2021-08-25	Copyright: Trenz Electronic GmbH	Page 30 of 31
Filename: POWER_4.SchDoc		

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REV	DATE	Description	
-01	2021-05	Initial revision	VT
	2022-05	Changed DCDC U4 TPS548A28 to MPQ8633BGLE-Z Changed C132 100nF to 1nF	
	2022-11	Added Table with Supported Voltage Ranges	

			Title: TE0817	
			A4	Number: TE0817 7NE21-A
Date: 2022-11-03		Copyright: Trenz Electronic GmbH		Page 31 of 31
Filename: Revision_Changes.SchDoc				

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2

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4