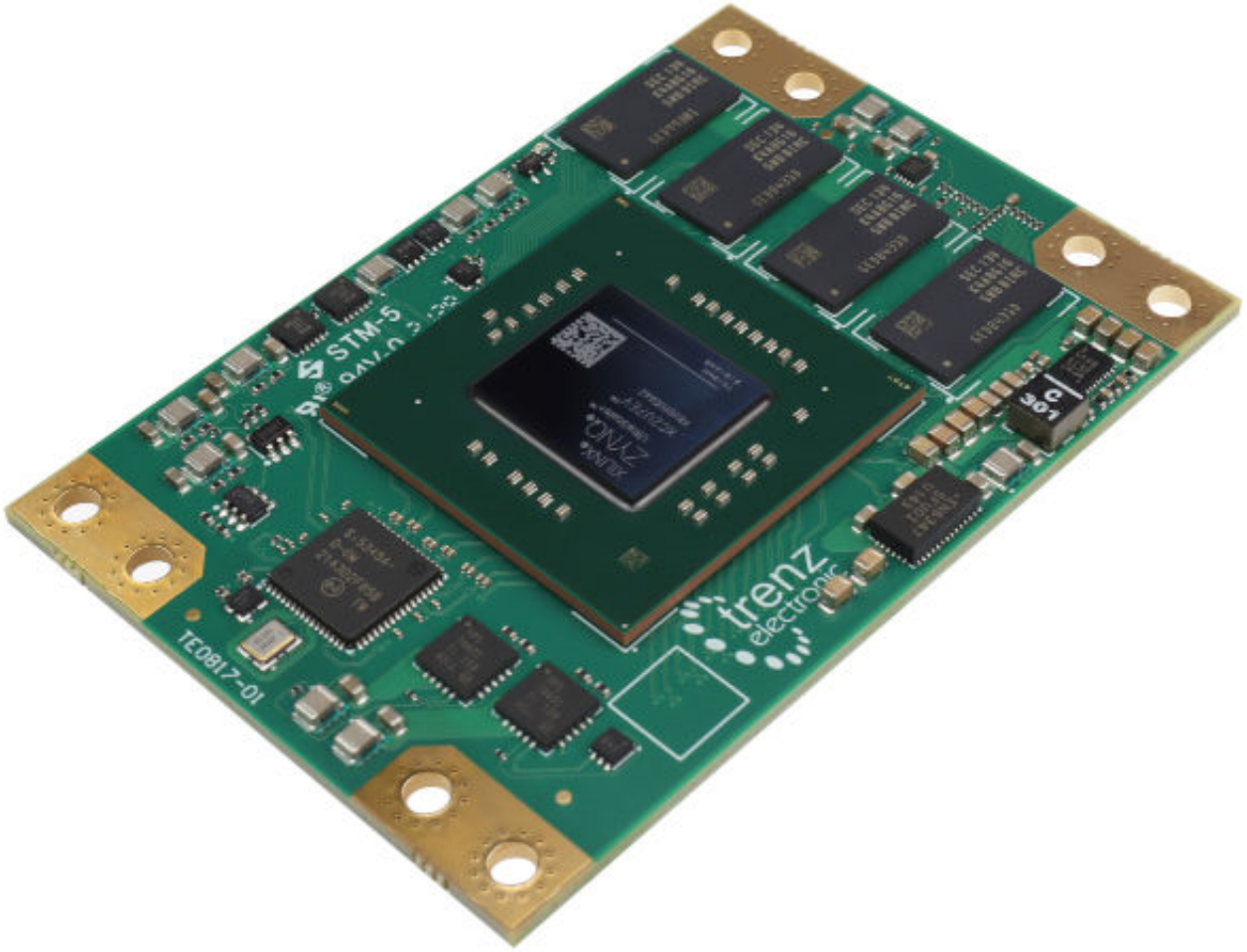

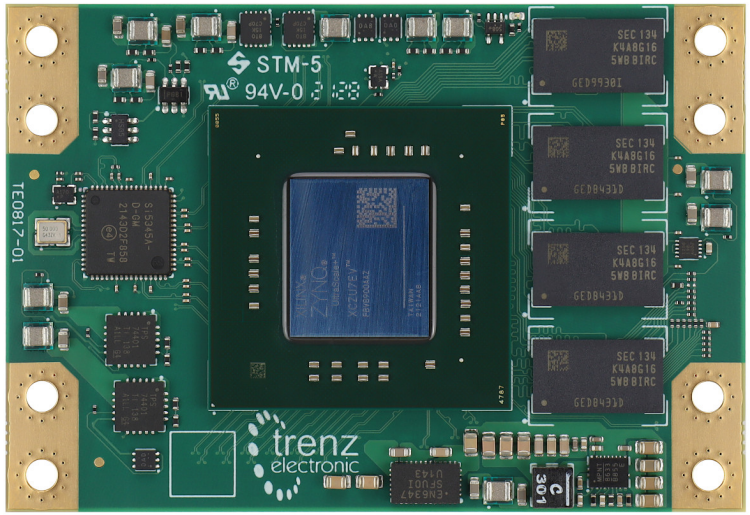

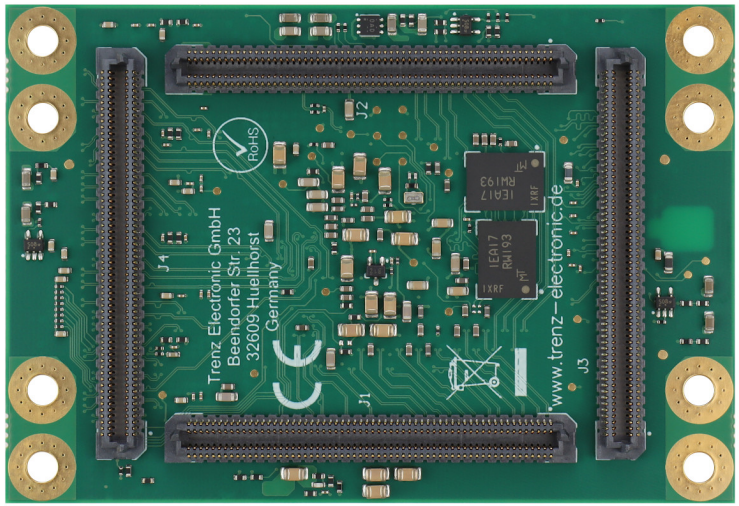

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REV	DATE	Description	
-01	2021-05	Initial revision	VT
	2022-05 2022-11	Changed DCDC U4 TPS548A28 to MPQ8633BGLE-Z Changed C132 100nF to 1nF Added Table with Supported Voltage Ranges	
-02	2024-04	1) Changed DCDC (U13) from EN6347QI to MPM3860GQW-Z and apdated according circuit.. 2) Connected DDR4-TEN signals together for U2A, U3A, U9A, and U12A and pulled them low via 499 Ohm resistor R127. Added testpoint TP3 for signal DDR4-TEN. 3) Changed voltage rail from 1.35 V to 1.45 V via adaption voltage divider resistor R30 and changed voltage rail name PL_GT_1V35 to PL_GT_1V45. 4) Changed voltage rail from 1.05 V to 1.15 V via adaption voltage divider resistors R33 and R35 and changed voltage rail name PL_GT_1V05 to PL_GT_1V15. 5) Added diode D2 between U41 pin 3 net MR and voltage rail 3.3VIN. 6) Added capacitors C202 ... C205 for VTT voltage rail VTT. 7) Added resistors R124 (default: not fitted) and R125 to supply U4 VCC either from PL_DCIN or from 3.3VIN. 8) Changed resistor R76 from 4.22 kOhm to 9.09 kOhm to set current limit to nearly 14.3 A for U4. 9) Changed inductor (L9) from XGL4030-301MEC to XGL5030-351MEC. 10) Added remote sense option (default: not fitted): 10.1) R126 for U30. 10.2) R128 for U29. 10.3) R129 for U31. 11) Added decoupling capacitors: 11.1) C208 for U4. 11.2) C211, C212, and C213 for U6. 11.3) C216 for U10. 11.4) C214 for U26. 11.5) C215 for U27. 11.6) C210 for U34. 11.7) C196 for U39. 11.8) C197 for U40. 11.9) C198 for U42. 11.10) C199 for U41. 11.11) C200 for U44. 11.12) C201, C206, and C207 for U1N. 12) Added pull-up resistors for HOLD (R130) and WP (R131) signals for Flash U7A. 13) Added pull-up resistors for HOLD (R132) and WP (R133) signals for Flash U17A. 14) Changed capacitor (C132) from 1 nF, X7R to 1.2 nF, NP0. 15) Changed 10 nF capacitor (C112) from 16 V, 0402 to 10 V, 0201. 16) Changed 100 nF capacitors (C37, C95, C96, C130, and C131) from 6.3 V, X5R, 0201 to 50 V, X7R, 0402. 17) Changed capacitor (C76, C77, C134, C195) from 1 µF, 16 V to 2.2 µF, 10 V. 18) Changed capacitor (C129, C140, C141, C142, C143, C144, C145, C146, C147, C148, C153) from 10 µF, 16 V to 22 µF, 10 V. 19) Changed 22 uF capacitor (C70, C73, C74, C75) from 0805 to 0603. 20) Changed 22 uF capacitor (C78, C80, C81, C82, C83, C84, C85, C86, C87, C110, C152, C154, C178) from 6.3 V to 10 V. 21) Changed 100 Ohm resistors (R7, R10) from 0201, 0.05 W to 0402, 0.063 W. 22) Changed resistor R77 from 12 kOhm to 10 kOhm. 23) Changed resistors R41 and R58 from 2 kOhm to 2.49 kOhm. 24) Added testpoints TP4, TP10, TP11, TP13, TP14, TP19, TP21, TP22, TP33 ... TP72. 25) Added UKCA logo. 26) Updated from library. 27) Changed signal trace length. 28) Updated documentation.	ED

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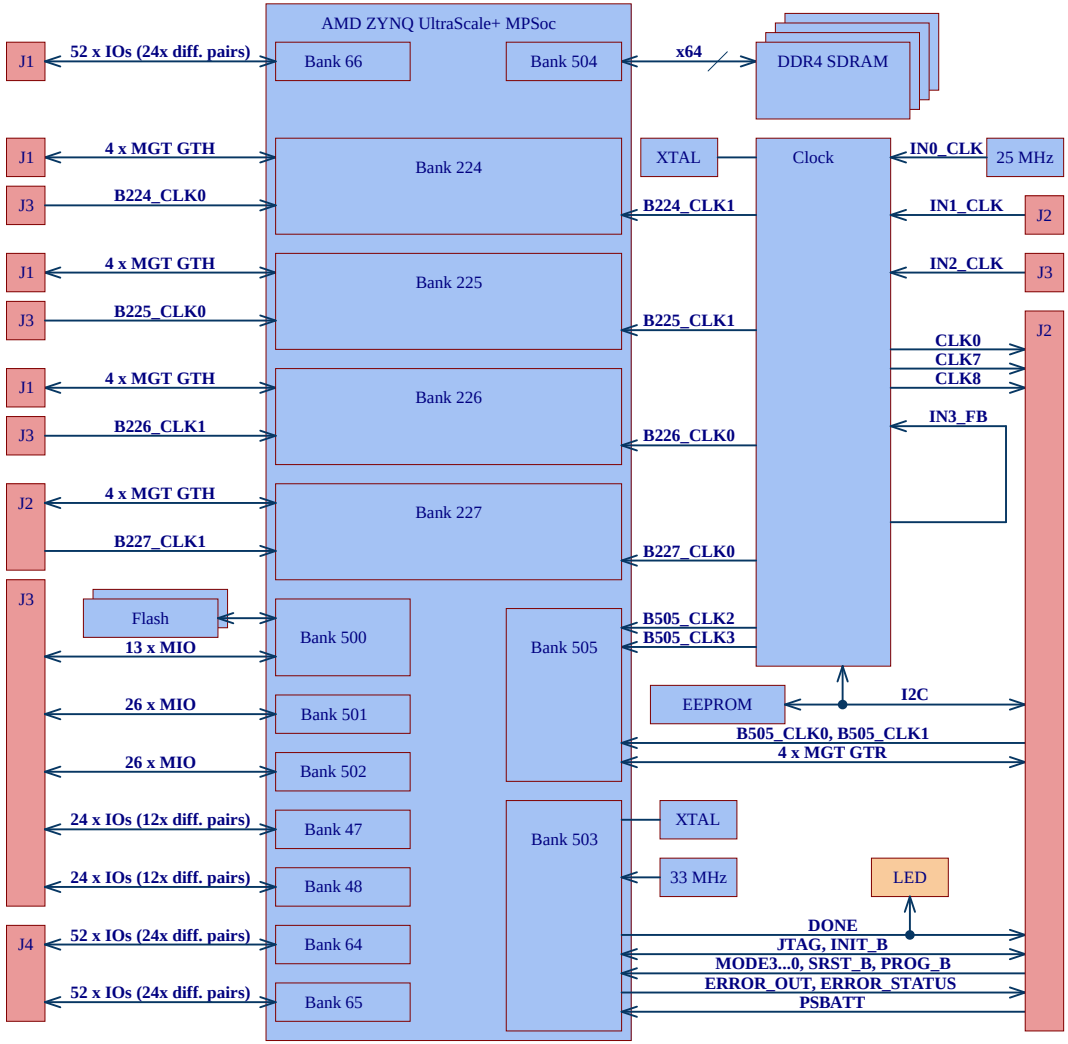

Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3VIN	IN	3.3 V	+/- 5 %	Micromodule Power	-
PL_DCIN	IN	3.3 V - 5.0 V	+/- 5 %	Micromodule Power	Programmable Logic
LP_DCDC	IN	3.3 V - 5.0 V	+/- 3 %	Micromodule Power	Low-Power Domain
GT_DCDC	IN	3.3 V - 5.0 V	+/- 3 %	Micromodule Power	GTH/GTY Transceiver
DCDCIN	IN	3.3 V - 5.0 V	+/- 5 %	Micromodule Power	Full-Power Domain and GTR
VCCO_64	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 64	-
VCCO_65	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 65	-
VCCO_66	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 66	-
VCCO_47	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 47	-
VCCO_48	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 48	-
PSBATT	IN	1.2 V - 1.5 V	-	RTC / BBRAM	-
PLL_3V3	IN	3.3 V	+/- 5 %	PLL Core Power	-
PL_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Programmable Logic
PS_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Processing System
DDR4_1V2	OUT	1.2 V	+/- 3 %	Power for Carrier	PS DDR I/O Supply

I2C Address:

Device	I2C ADDR	Note
PLL U5	0x69	-
EEPROM U11	0x50	-

Legend:

- B2B Connector
- LED Interface
- On-board Components

TE0817		ZU_POWER	POWER	POWER_3
DDR4-TERM	ZU_GT_2	ZU_PS_POWER	POWER_2	POWER_4

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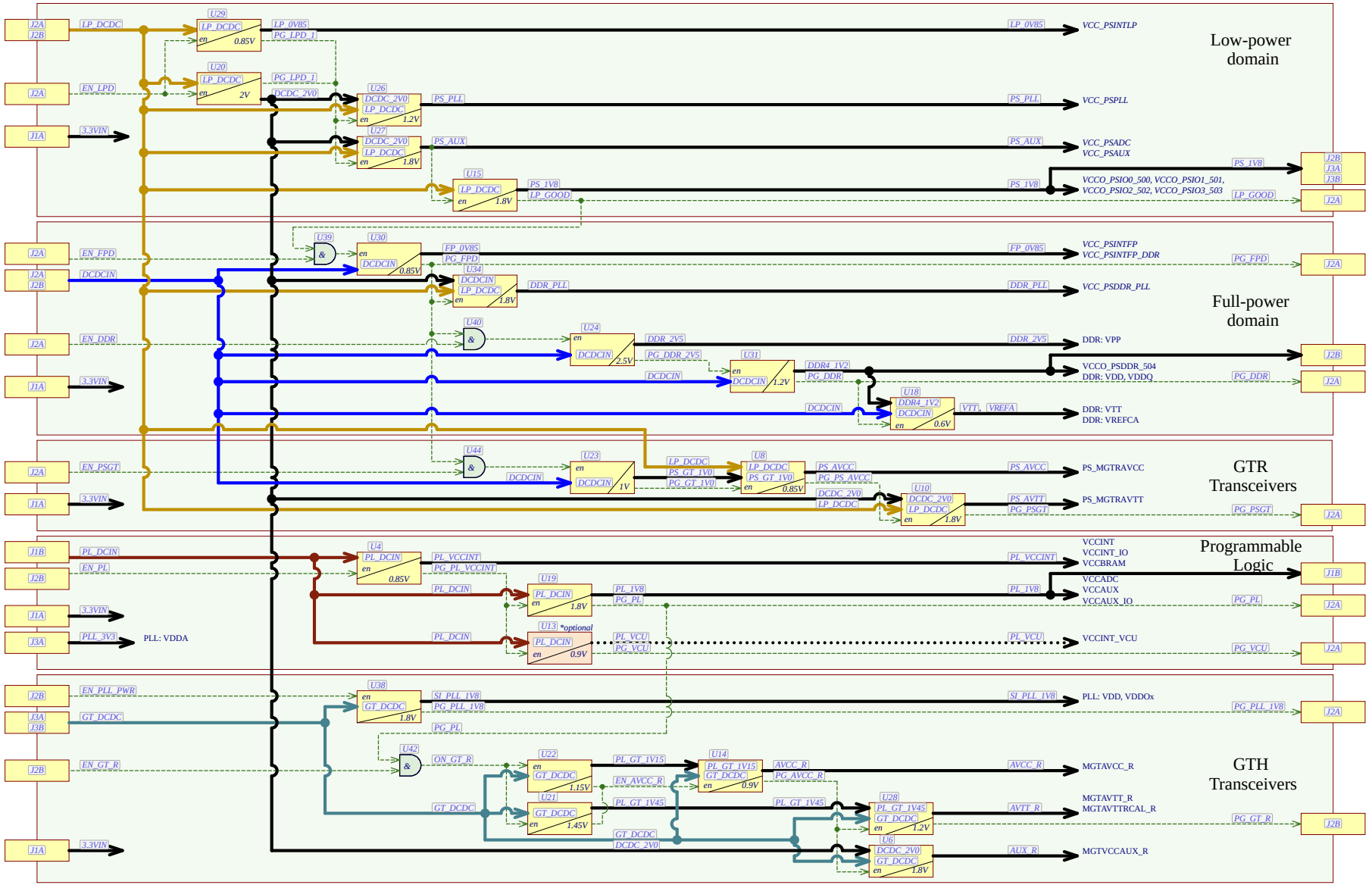
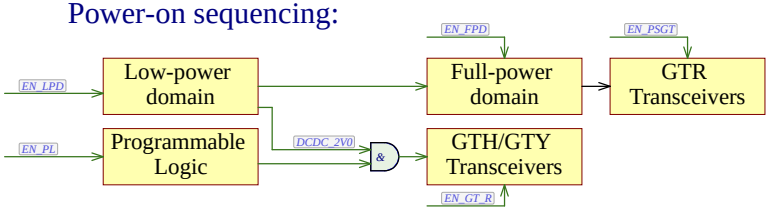


Power-on sequencing:



EN_GT_R — Net name

Power bus

Control signal

PL_DCIN 0.9V — Optional power converter

& — Logic AND gate

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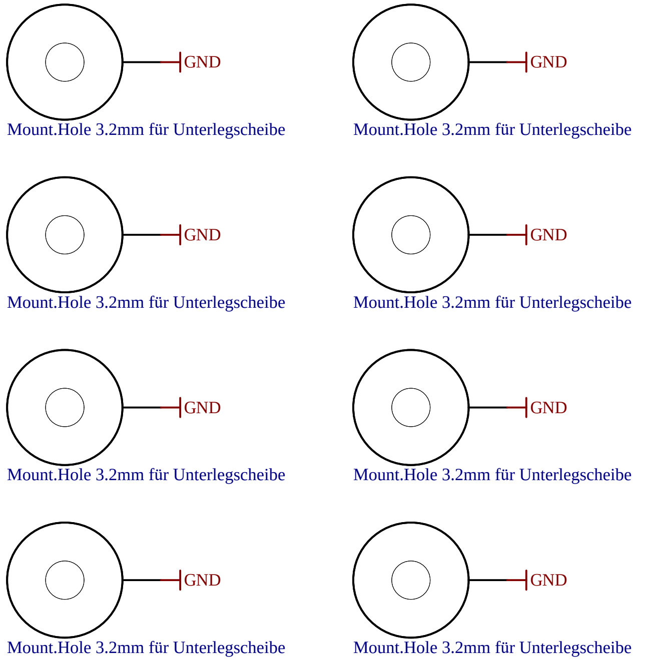
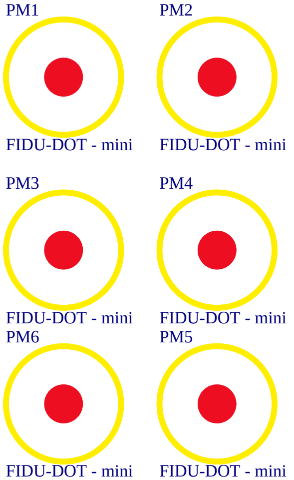
Special notes:





Serial1
Serial
Serialnumber 6,3 x 6.3mm

LOGO1
TE Logo PRINT Layer
LOGO PRINT

MECH1
TE Address Overlay
LOGO ADDRESS

CE
CE Logo on Top Overlay
CE-TOPOVERLAY

RoHS
RoHS Logo on Top Overlay
RoHS-TOPOVERLAY

UKCA
UKCA Logo on Top Overlay
UKCA-TOPOVERLAY

WEEE
WEEE Logo on Top Overlay
WEEE-TOPOVERLAY

Design drawn by:	ED
Checked by:	MT
Assembly variant:	7DE81-A
Created by:	ED
Modified by:	ED
Modified at:	2024-04-17

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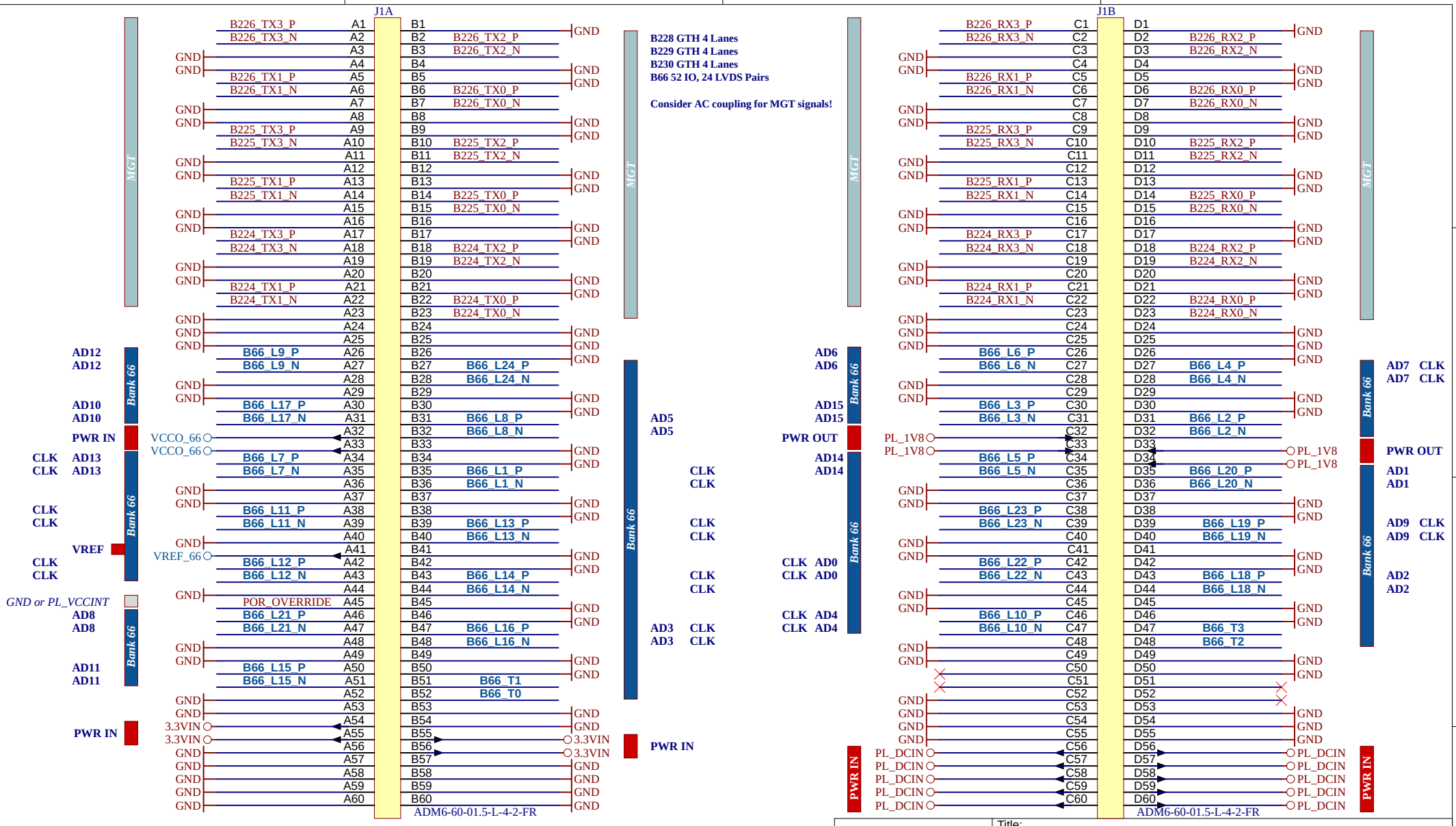

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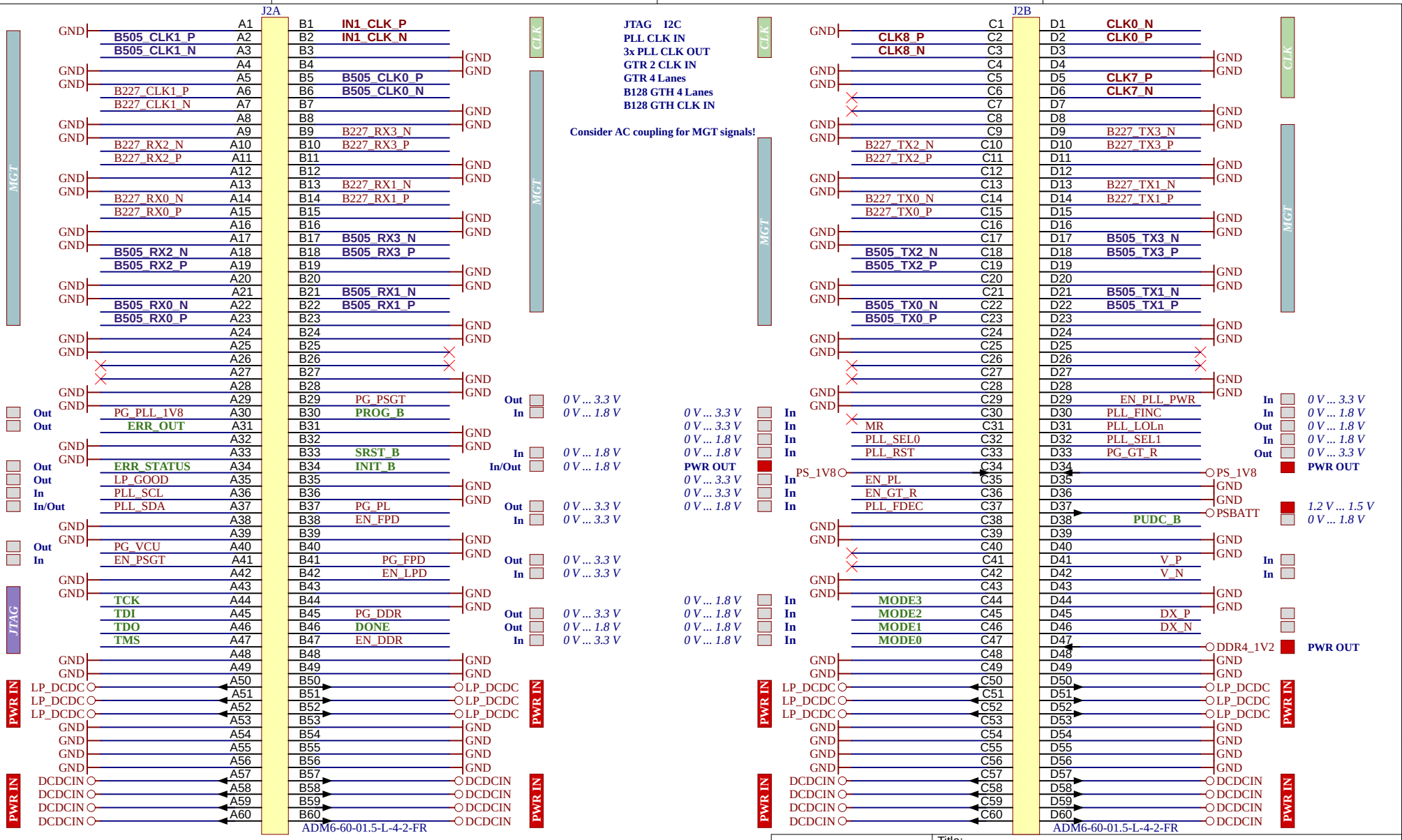

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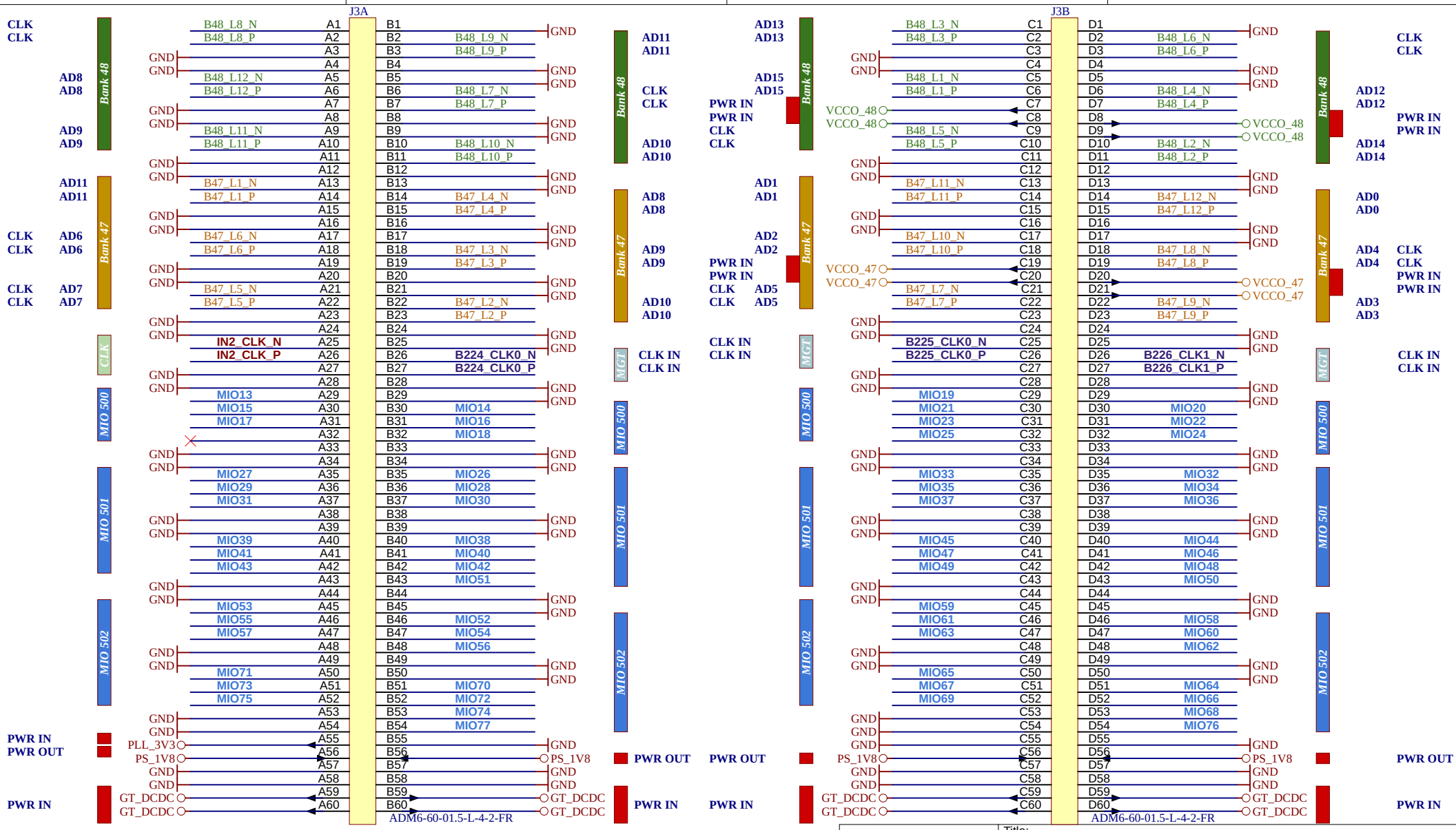

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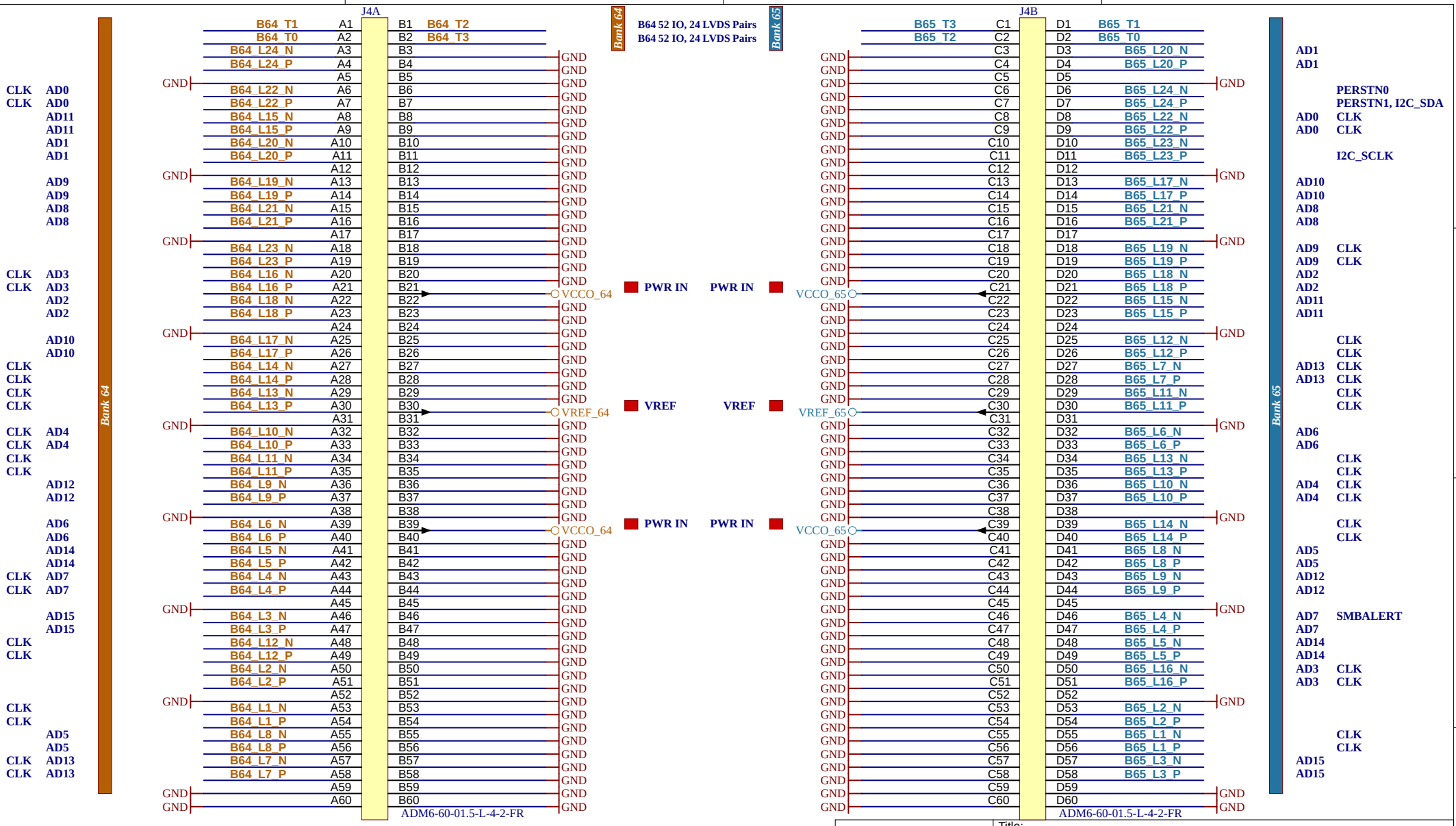

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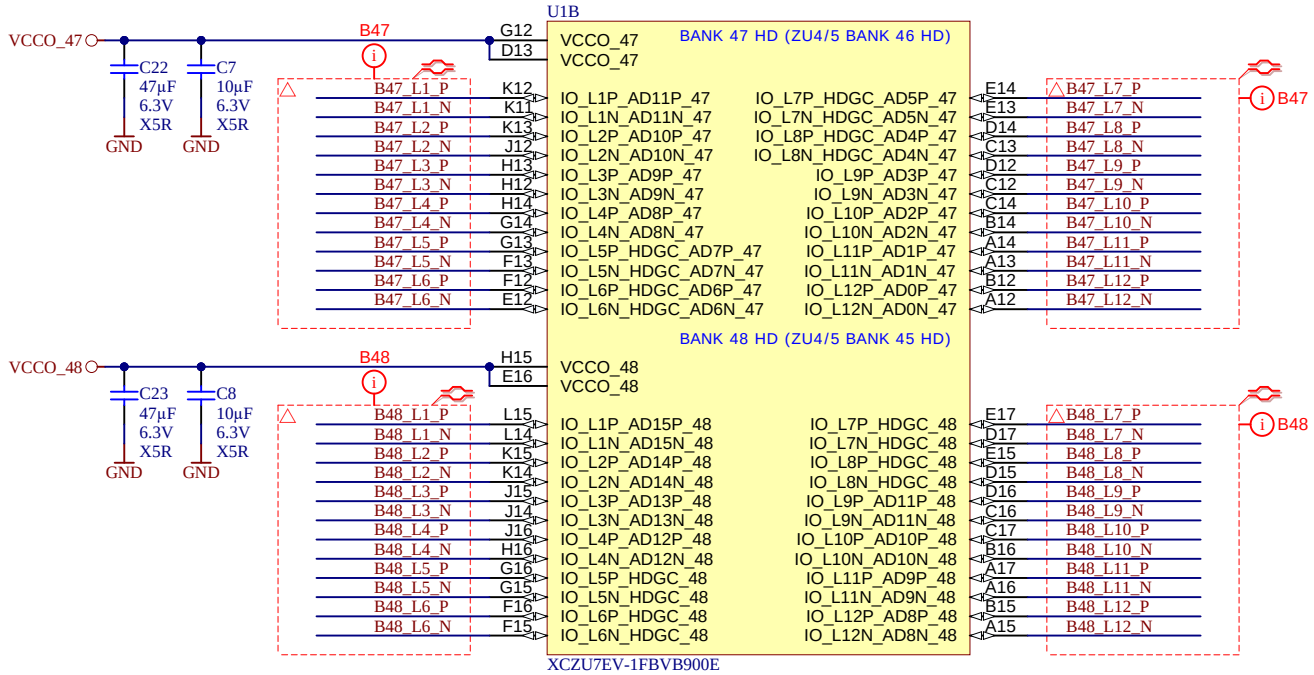

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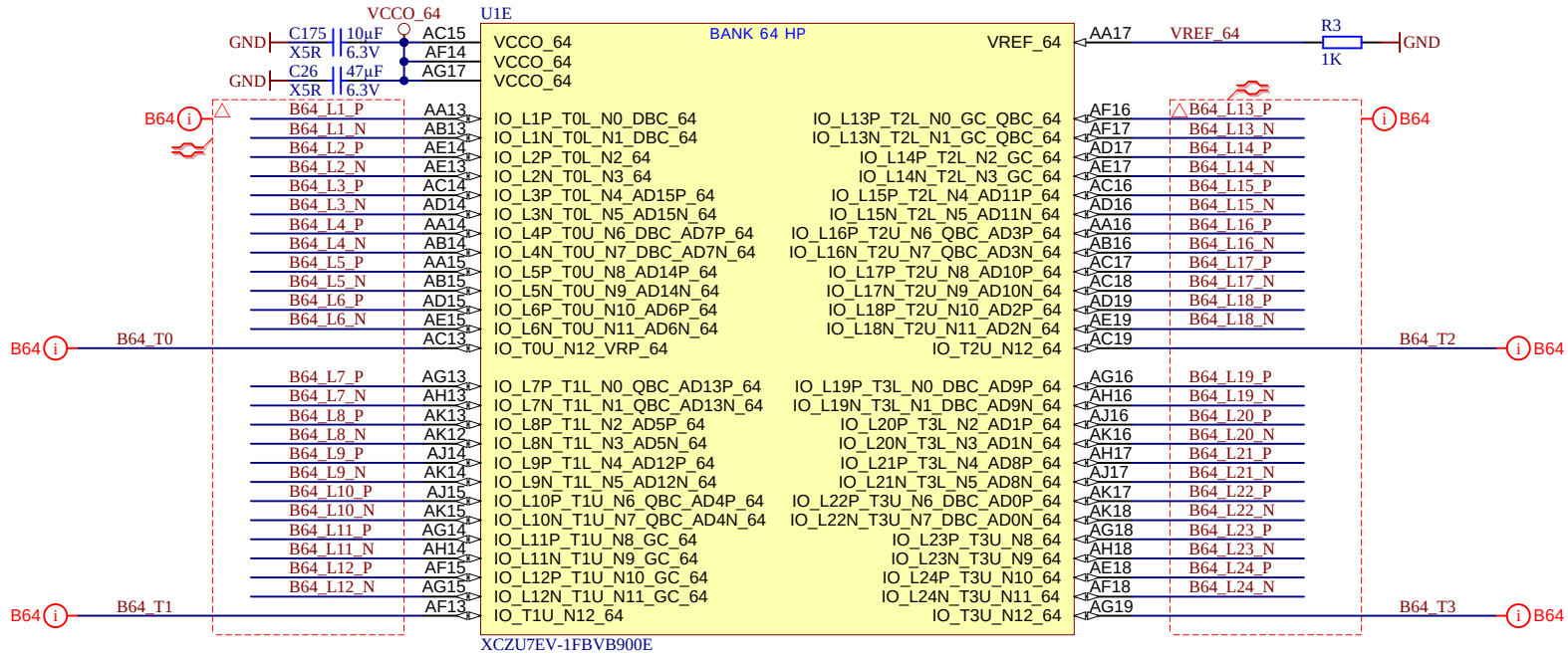

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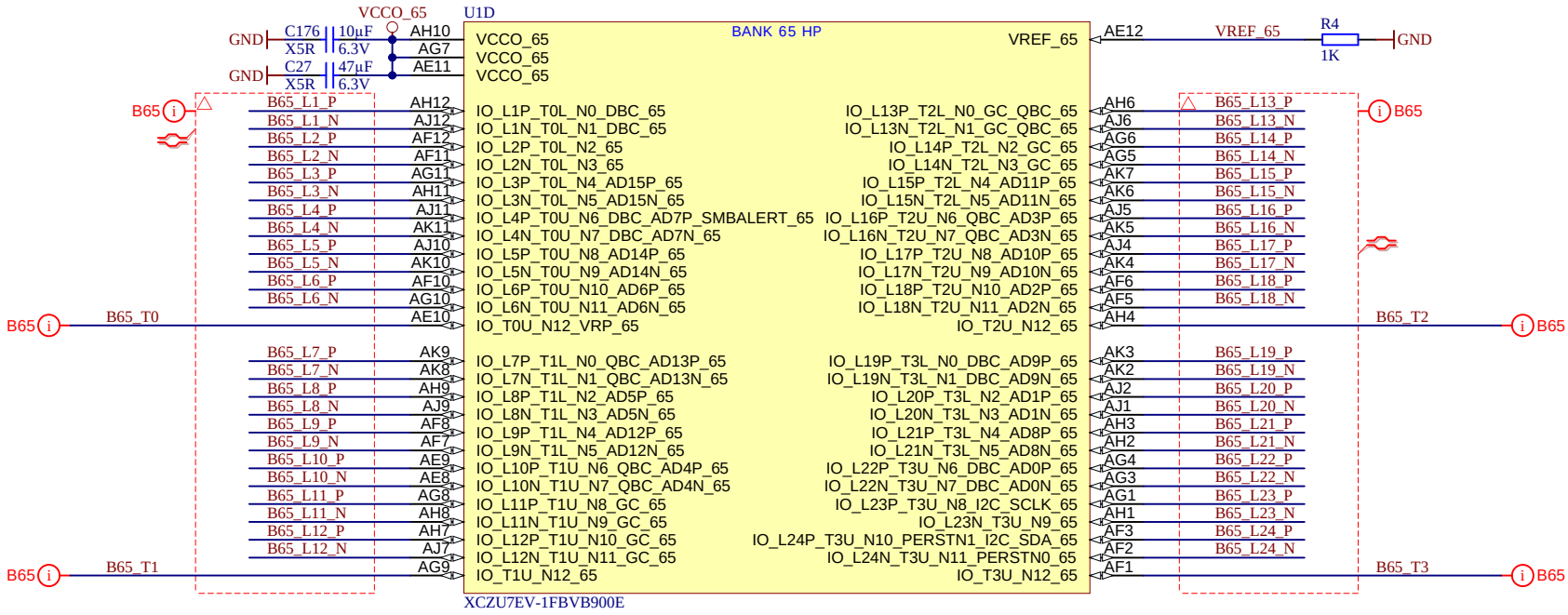

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B65_L1_N	AJ12	IO_L1N_T0L_N1_DBC_65	IO_L13N_T2L_N1_GC_QBC_65	AJ6	B65_L13_N
B65_L2_P	AF12	IO_L2P_T0L_N2_65	IO_L14P_T2L_N2_GC_65	AG6	B65_L14_P
B65_L2_N	AF11	IO_L2N_T0L_N3_65	IO_L14N_T2L_N3_GC_65	AG5	B65_L14_N
B65_L3_P	AG11	IO_L3P_T0L_N4_AD15P_65	IO_L15P_T2L_N4_AD11P_65	AK7	B65_L15_P
B65_L3_N	AH11	IO_L3N_T0L_N5_AD15N_65	IO_L15N_T2L_N5_AD11N_65	AK6	B65_L15_N
B65_L4_P	AJ11	IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65	IO_L16P_T2U_N6_QBC_AD3P_65	AJ5	B65_L16_P
B65_L4_N	AK11	IO_L4N_T0U_N7_DBC_AD7N_65	IO_L16N_T2U_N7_QBC_AD3N_65	AK5	B65_L16_N
B65_L5_P	AJ10	IO_L5P_T0U_N8_AD14P_65	IO_L17P_T2U_N8_AD10P_65	AJ4	B65_L17_P
B65_L5_N	AK10	IO_L5N_T0U_N9_AD14N_65	IO_L17N_T2U_N9_AD10N_65	AK4	B65_L17_N
B65_L6_P	AF10	IO_L6P_T0U_N10_AD6P_65	IO_L18P_T2U_N10_AD2P_65	AF6	B65_L18_P
B65_L6_N	AG10	IO_L6N_T0U_N11_AD6N_65	IO_L18N_T2U_N11_AD2N_65	AF5	B65_L18_N
	AE10	IO_T0U_N12_VRP_65	IO_T2U_N12_65	AH4	
B65_L7_P	AK9	IO_L7P_T1L_N0_QBC_AD13P_65	IO_L19P_T3L_N0_DBC_AD9P_65	AK3	B65_L19_P
B65_L7_N	AK8	IO_L7N_T1L_N1_QBC_AD13N_65	IO_L19N_T3L_N1_DBC_AD9N_65	AK2	B65_L19_N
B65_L8_P	AH9	IO_L8P_T1L_N2_AD5P_65	IO_L20P_T3L_N2_AD1P_65	AJ2	B65_L20_P
B65_L8_N	AJ9	IO_L8N_T1L_N3_AD5N_65	IO_L20N_T3L_N3_AD1N_65	AJ1	B65_L20_N
B65_L9_P	AF8	IO_L9P_T1L_N4_AD12P_65	IO_L21P_T3L_N4_AD8P_65	AH3	B65_L21_P
B65_L9_N	AF7	IO_L9N_T1L_N5_AD12N_65	IO_L21N_T3L_N5_AD8N_65	AH2	B65_L21_N
B65_L10_P	AE9	IO_L10P_T1U_N6_QBC_AD4P_65	IO_L22P_T3U_N6_DBC_AD0P_65	AG4	B65_L22_P
B65_L10_N	AE8	IO_L10N_T1U_N7_QBC_AD4N_65	IO_L22N_T3U_N7_DBC_AD0N_65	AG3	B65_L22_N
B65_L11_P	AG8	IO_L11P_T1U_N8_GC_65	IO_L23P_T3U_N8_I2C_SCLK_65	AG1	B65_L23_P
B65_L11_N	AH8	IO_L11N_T1U_N9_GC_65	IO_L23N_T3U_N9_65	AH1	B65_L23_N
B65_L12_P	AH7	IO_L12P_T1U_N10_GC_65	IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65	AF3	B65_L24_P
B65_L12_N	AJ7	IO_L12N_T1U_N11_GC_65	IO_L24N_T3U_N11_PERSTN0_65	AF2	B65_L24_N
	AG9	IO_T1U_N12_65	IO_T3U_N12_65	AF1	

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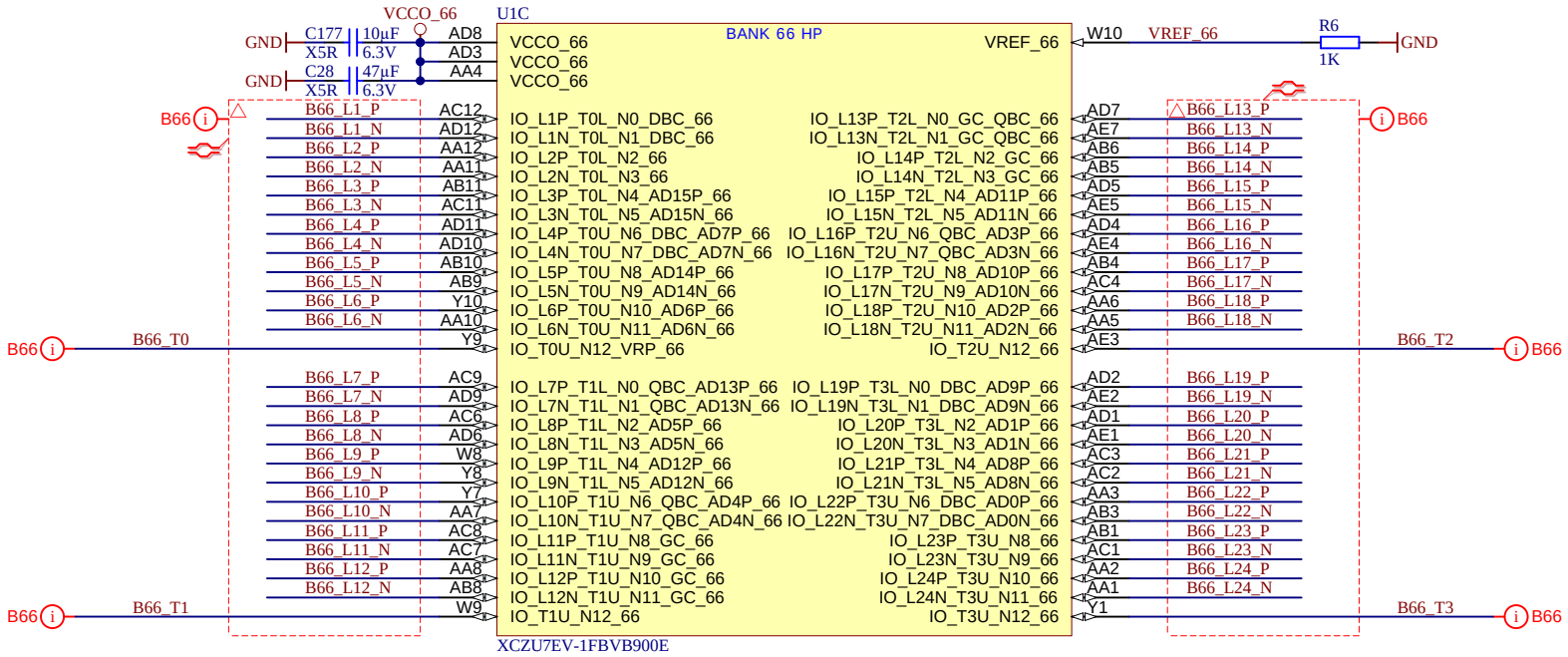

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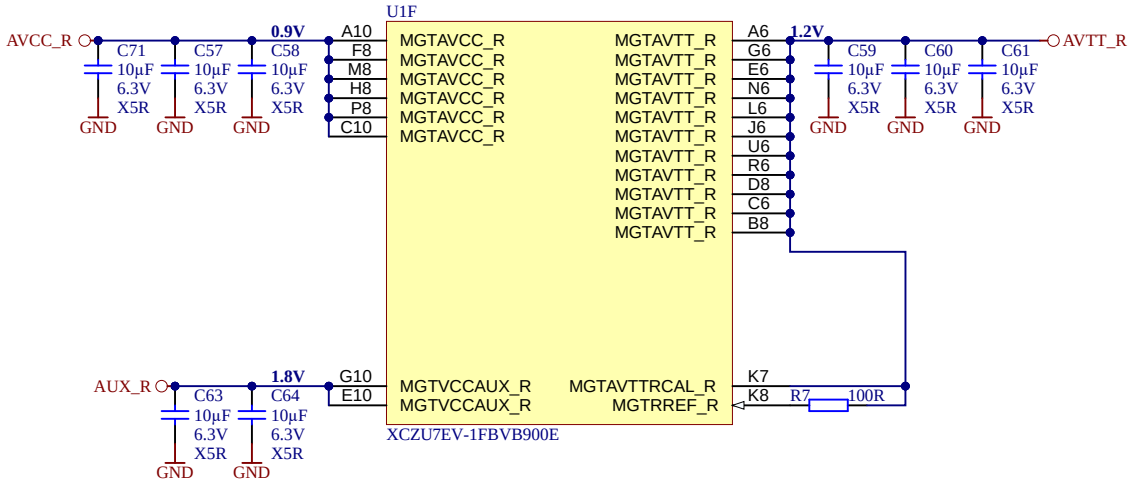

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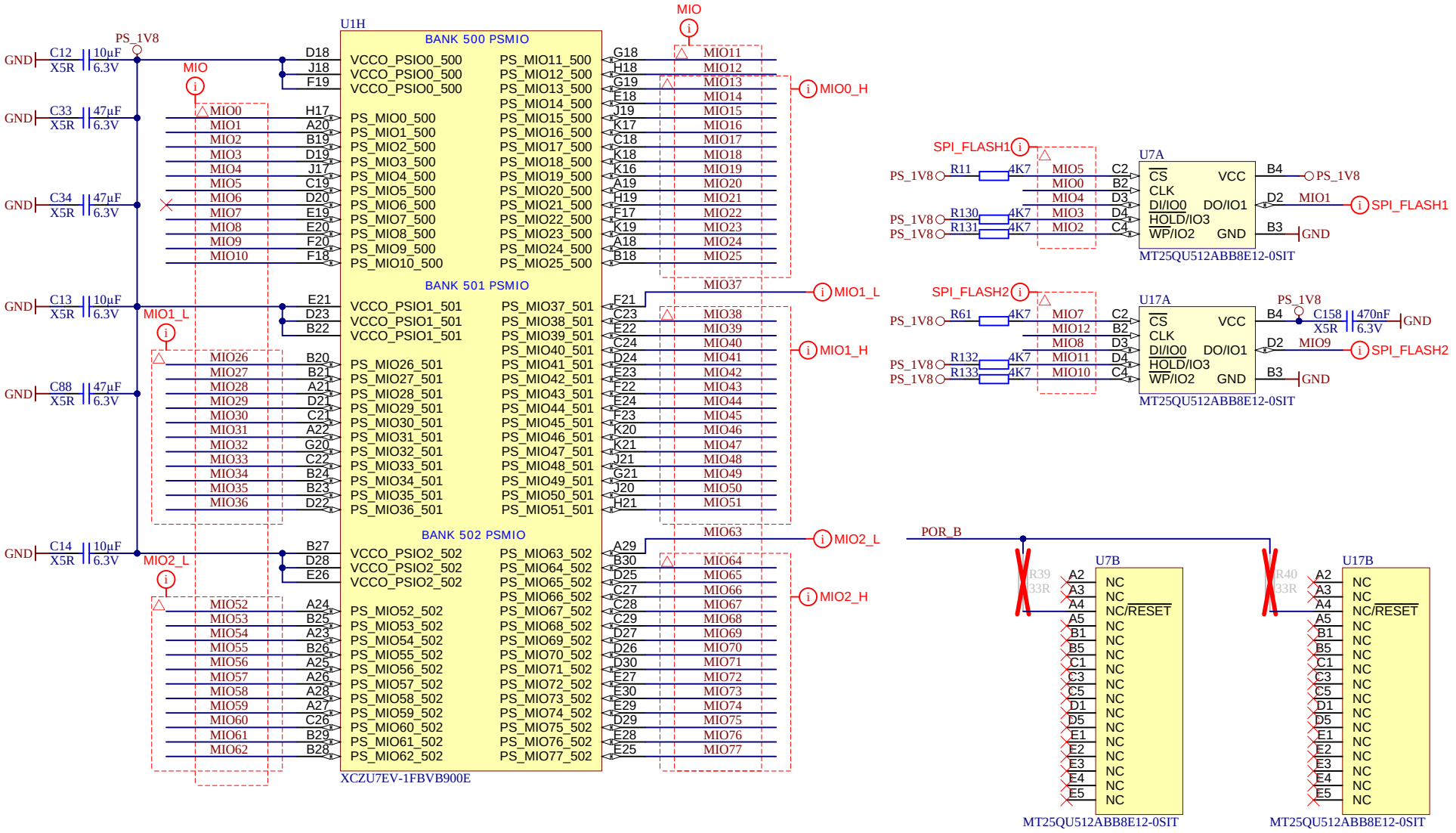

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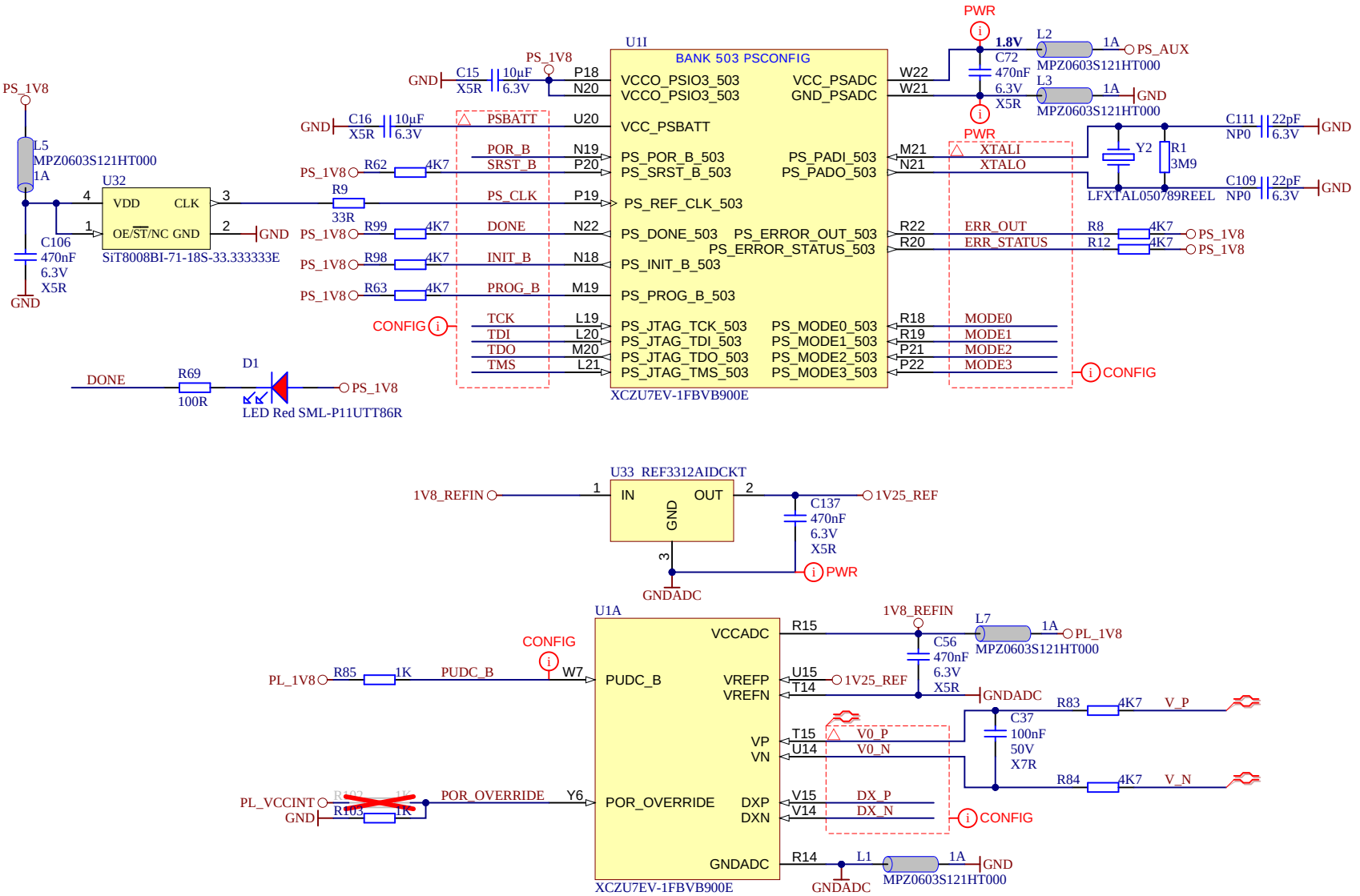

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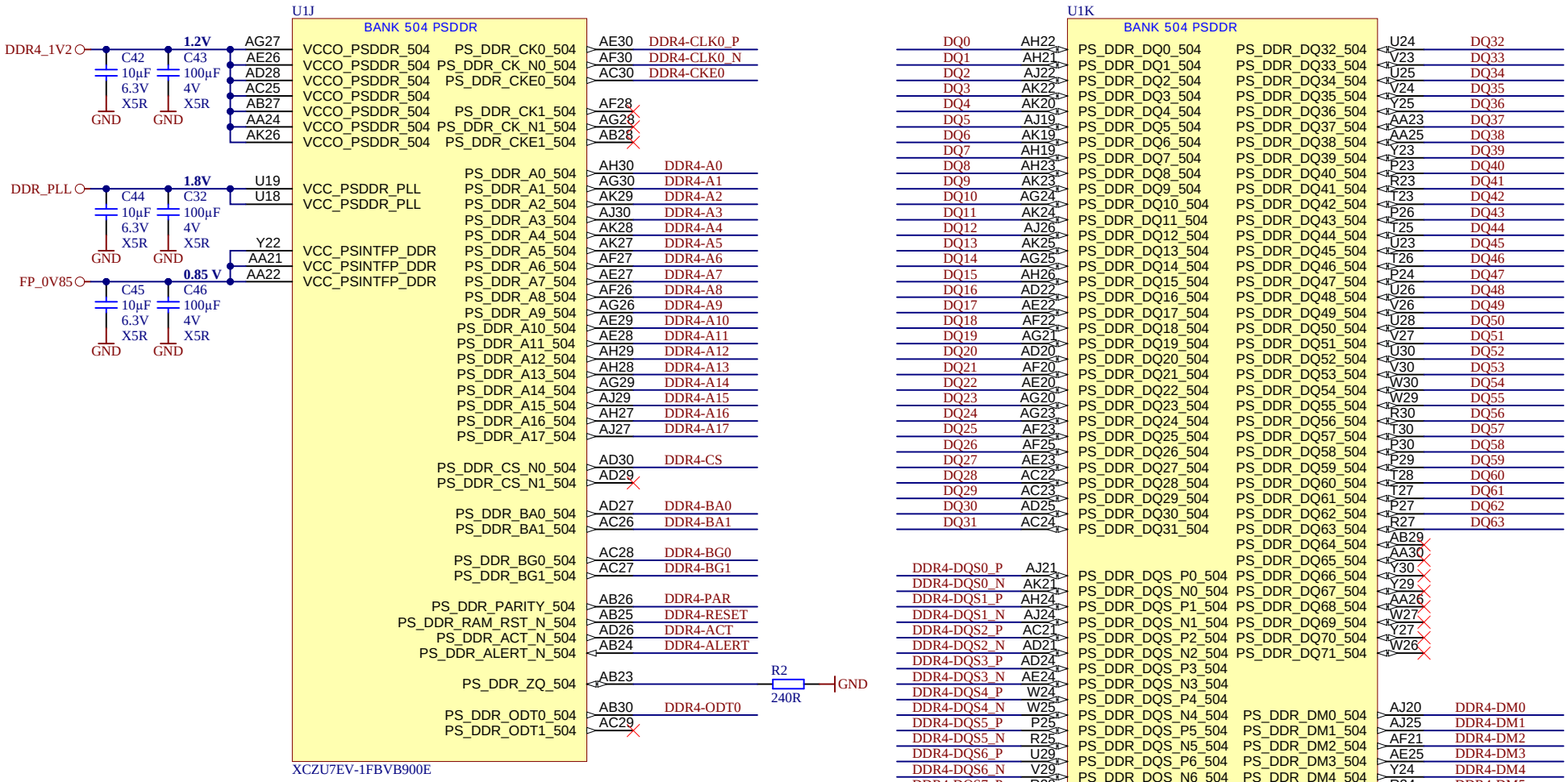

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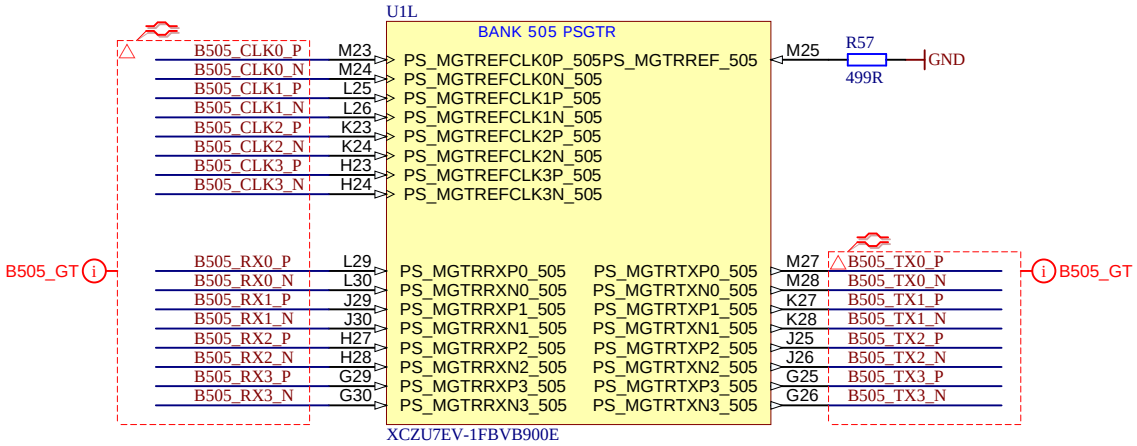

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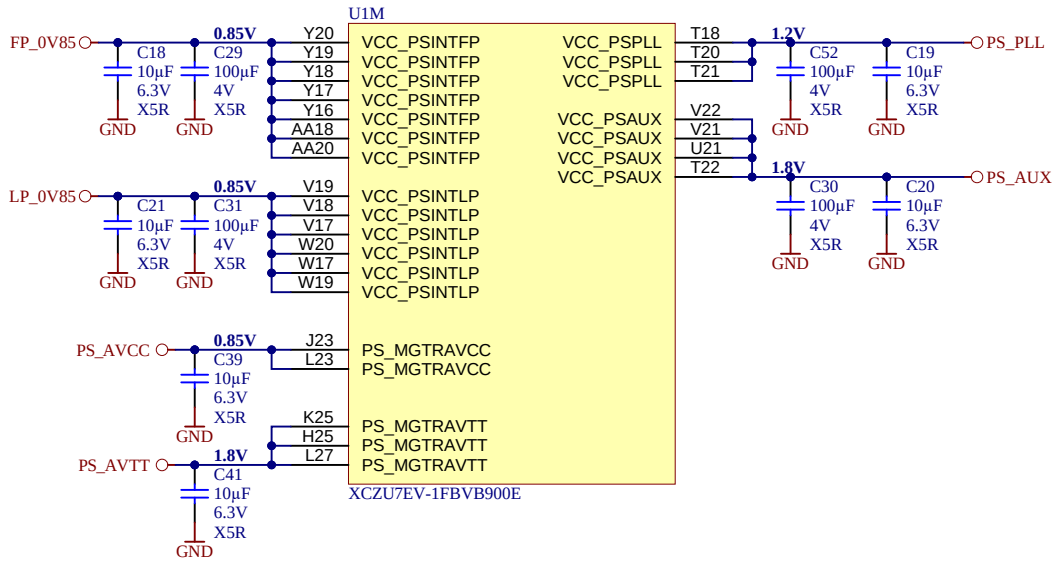

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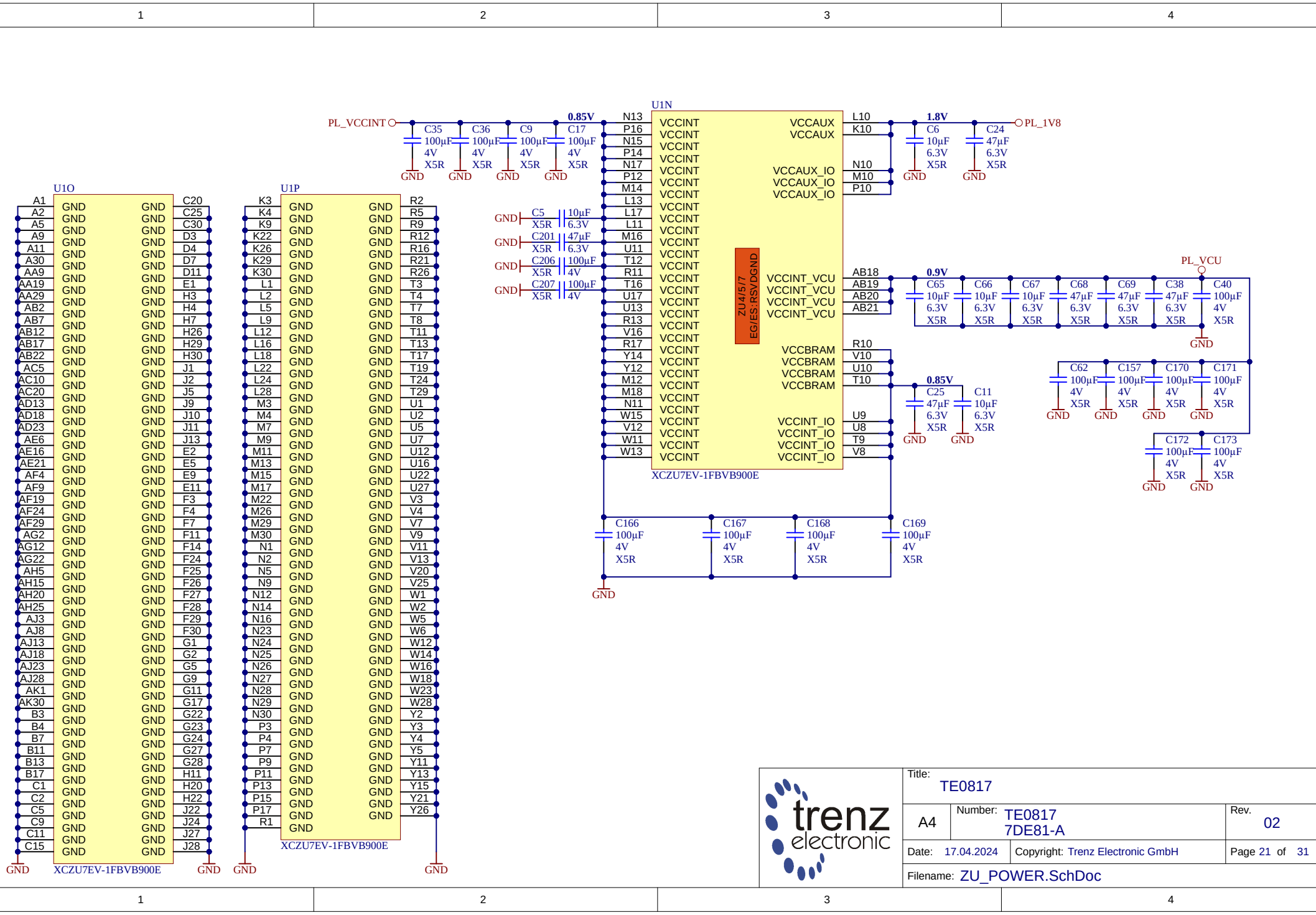

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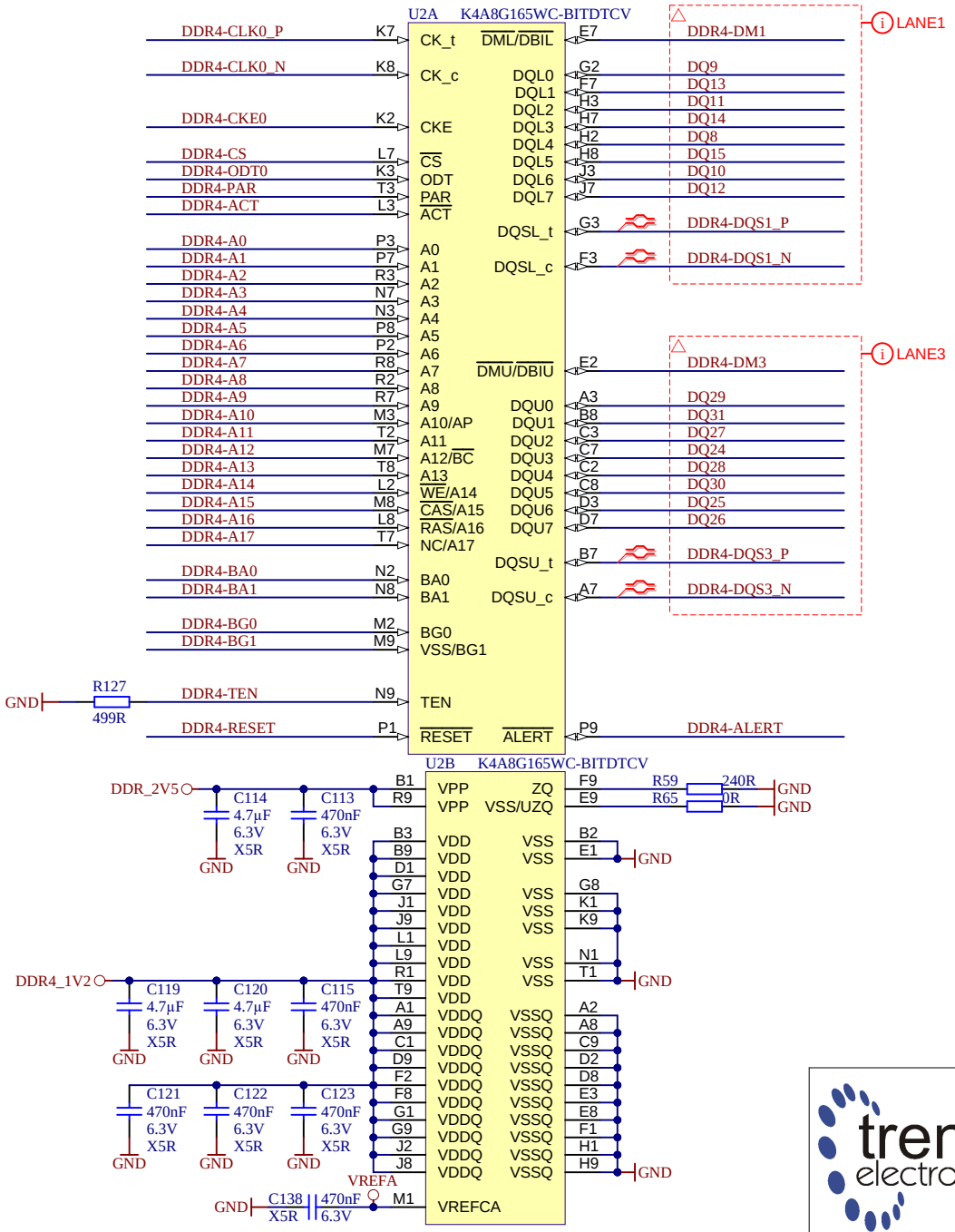

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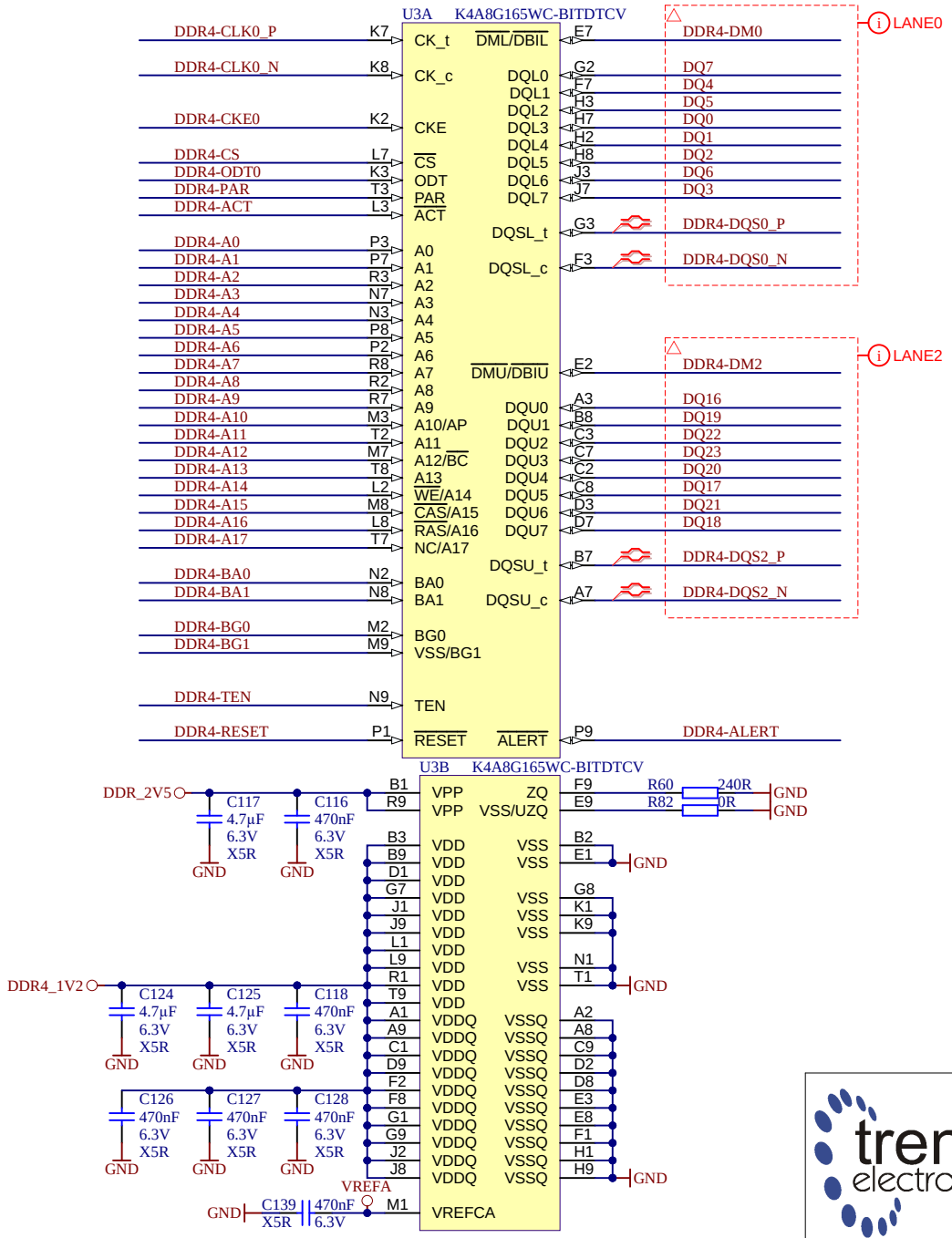
	Filename: DDR4-RAM.SchDoc		



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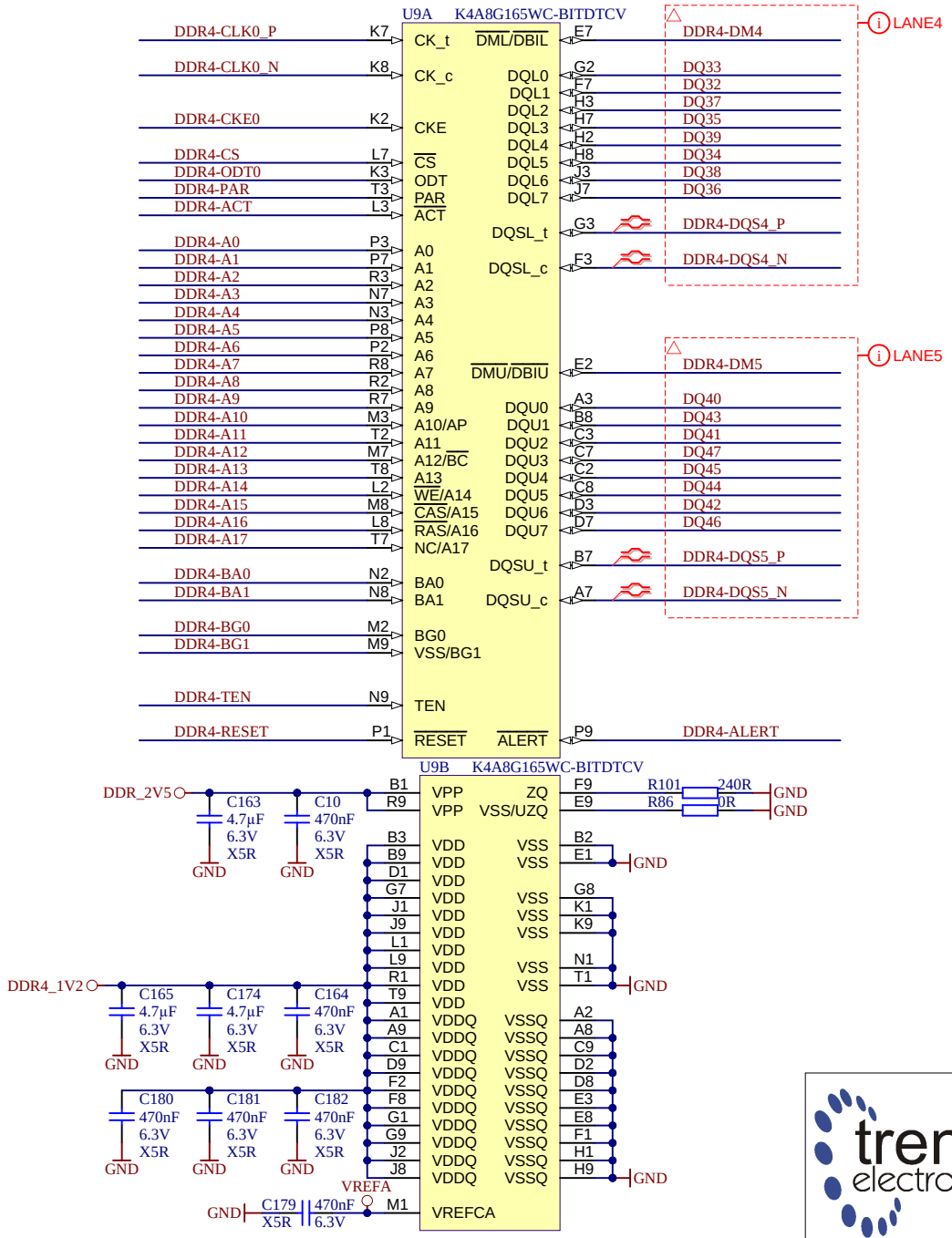
	Filename: DDR4-RAM_2.SchDoc		



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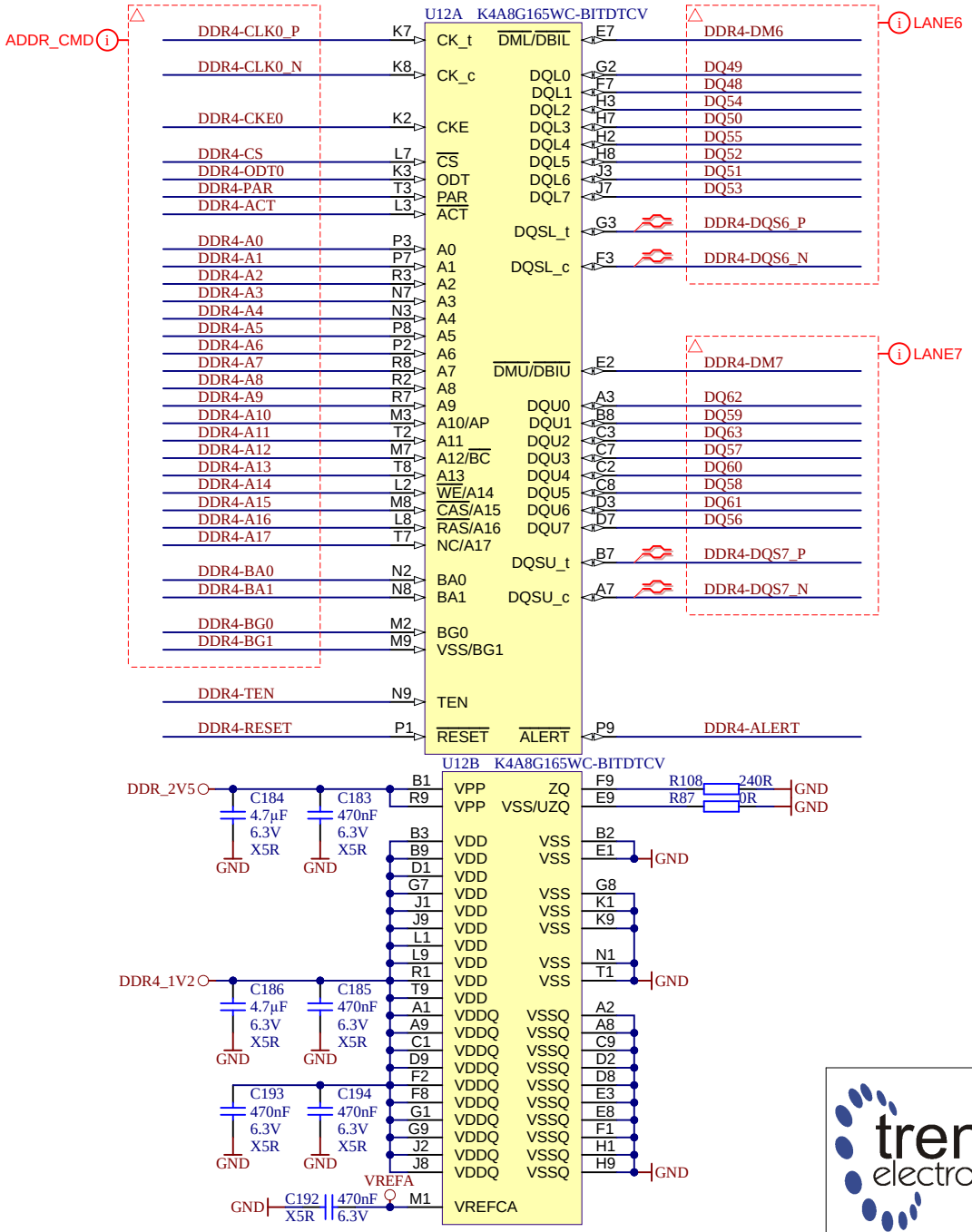

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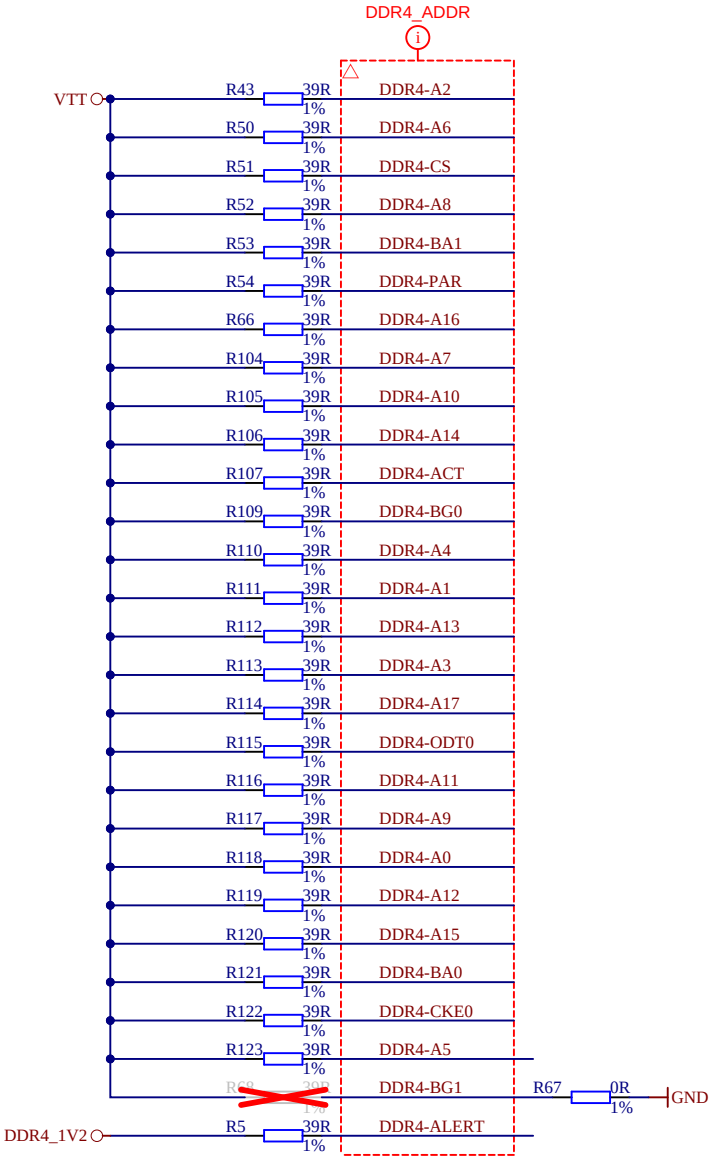

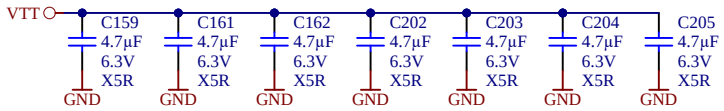

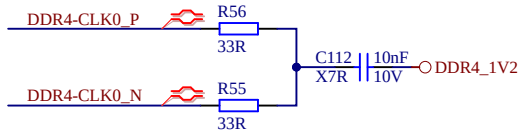

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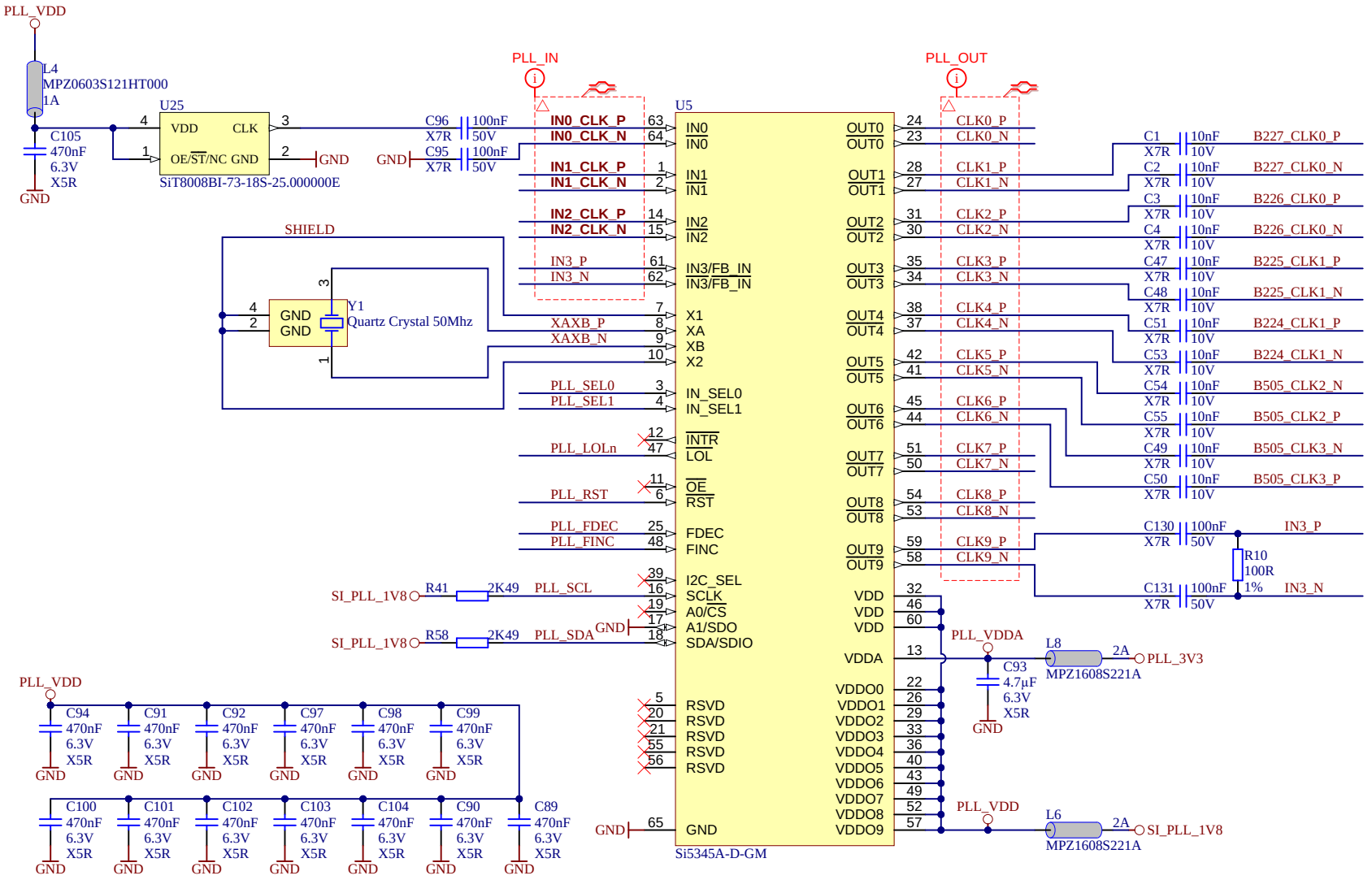
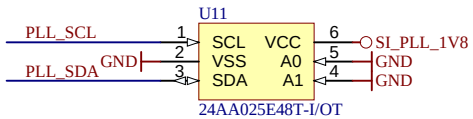


EEPROM for MAC



Slave address: 0b1010000

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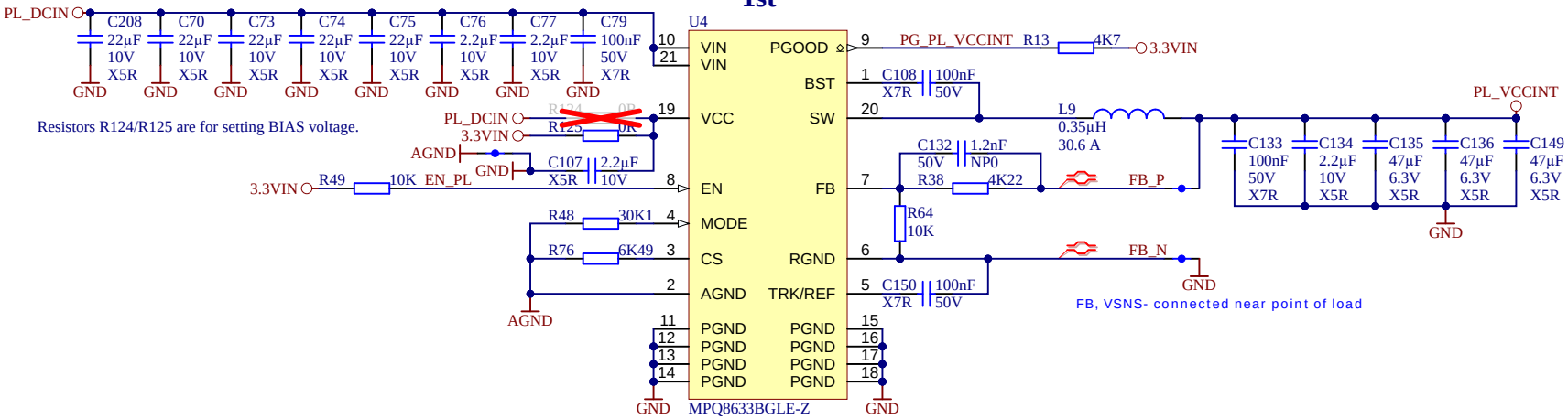
U4 can be TPS548A28RWWR or MPQ8633BGLE-Z which is up to Trenz Electronic GmbH.

PL VCCINT

1st

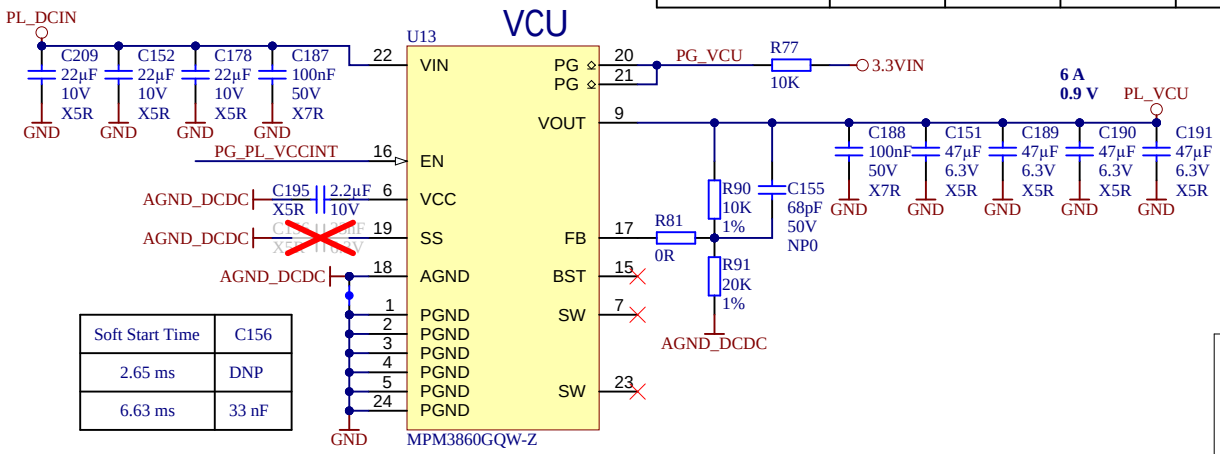


DCDC U4 (pin compatible)	Current Capabililty	Current Limit*	R76	Light-Load Mode	Frequency	R48	Soft Start Time	C150
TPS548A28	15 A	13.9 A	4.70 kOhm	CCM	800 kHz	30.1 kOhm	1.66 ms	100 nF
TPS548B28	20 A	19.7 A	6.49 kOhm	CCM	800 kHz	30.1 kOhm	1.66 ms	100 nF
MPQ8633BGLE-Z	20 A	19.7 A	6.49 kOhm	CCM	800 kHz	30.1 kOhm	1.66 ms	100 nF

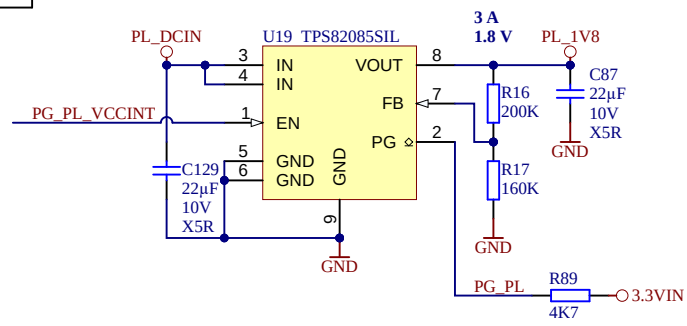
* Current limit depends on input and output voltage.

FPGA Speedgrade	R38	R64	PL_VCCINT	C132
-1	4.22 kOhm	10 kOhm	0.853 V	1.2 nF
-2	4.22 kOhm	10 kOhm	0.853 V	1.2 nF
-3	10 kOhm	20 kOhm	0.900 V	560 pF

VCU



Soft Start Time	C156
2.65 ms	DNP
6.63 ms	33 nF



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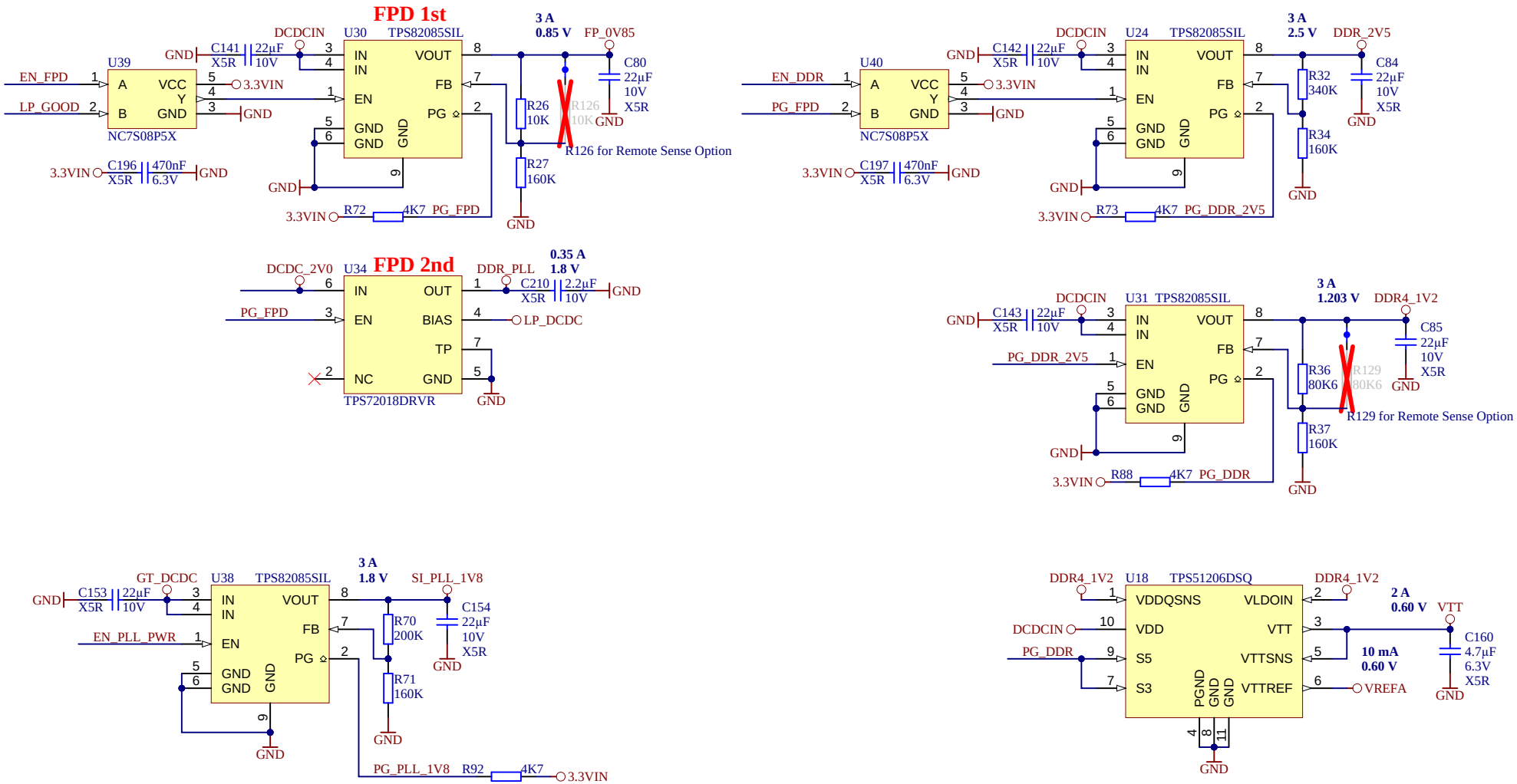

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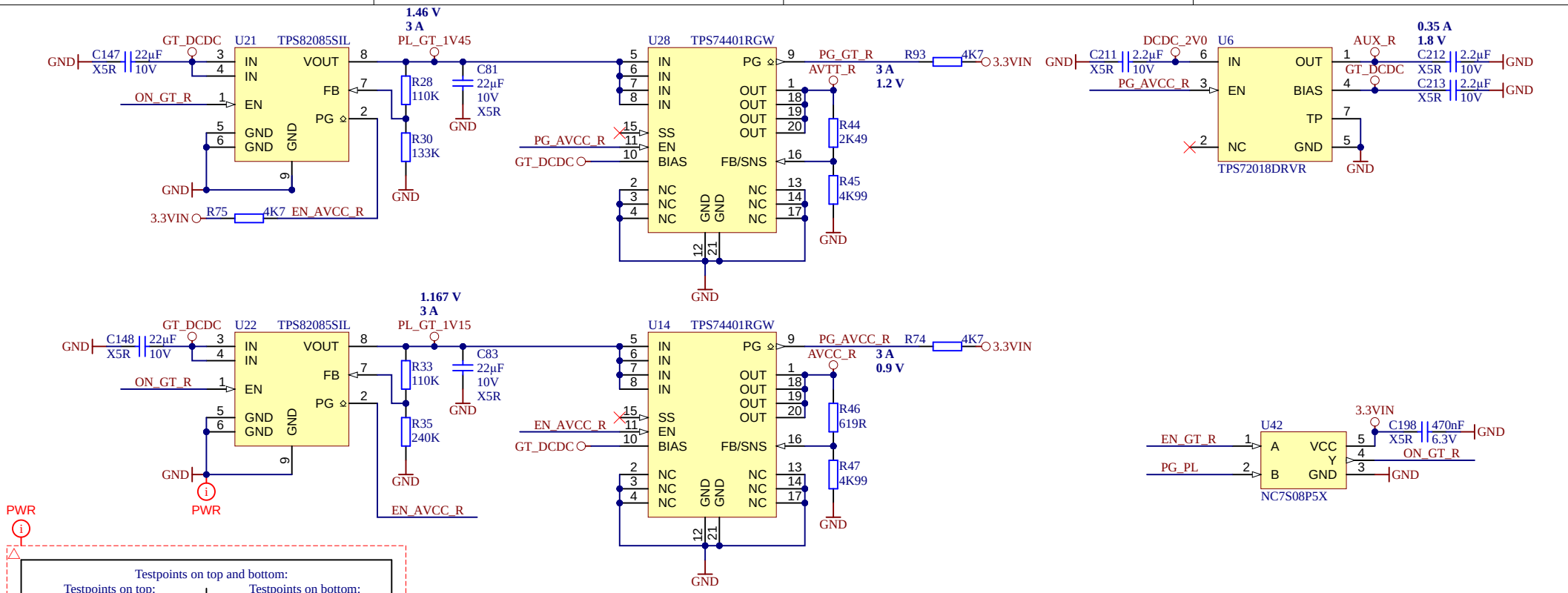

Testpoints on top and bottom:

Testpoints on top:		Testpoints on bottom:	
LP_0V85	TP10	LP_0V85	TP31
FP_0V85	TP11	FP_0V85	TP15
PS_PLL	TP13	PS_PLL	TP27
PS_GT_1V0	TP14	PS_GT_1V0	TP19
PS_AUX	TP21	PS_AUX	TP29
PS_AVCC	TP22	PS_AVCC	TP30
PS_AVTT	TP33	PS_AVTT	TP28
DDR_PLL	TP34	DDR_PLL	TP18
DDR_2V5	TP35	DDR_2V5	TP16
VREFA	TP36	VREFA	TP37
VTT	TP4	VTT	TP23
PL_VCCINT	TP40	PL_VCCINT	TP12
DCDC_2V0	TP42	DCDC_2V0	TP17
PL_GT_1V45	TP44	PL_GT_1V45	TP45
PL_GT_1V15	TP47	PL_GT_1V15	TP48
AUX_R	TP50	AUX_R	TP24
AVCC_R	TP52	AVCC_R	TP26
AVTT_R	TP53	AVTT_R	TP25
PL_VCU	TP55	PL_VCU	TP20
1V8_REFIN	TP57	1V8_REFIN	TP58
1V25_REF	TP60	1V25_REF	TP61
PLL_VDDA	TP64	PLL_VDDA	TP65
PLL_VDD	TP66	PLL_VDD	TP67
SI_PLL_1V8	TP70	SI_PLL_1V8	TP71

Testpoints on top:

3.3VIN	TP38
LP_DCDC	TP39
DCDCIN	TP41
PL_DCIN	TP43
GT_DCDC	TP46
PLL_3V3	TP49
PSBATT	TP51
VCCO_47	TP54
VCCO_48	TP56
VCCO_64	TP59
VCCO_65	TP62
VCCO_66	TP63
PS_1V8	TP68
PL_1V8	TP69
DDR4_1V2	TP72

Testpoints on bottom:

PLL_SCL	TP1
PLL_SDA	TP2
DDR4-TEN	TP3
TCK	TP6
TDI	TP7
TDO	TP8
TMS	TP9
GND	TP5
GND	TP32

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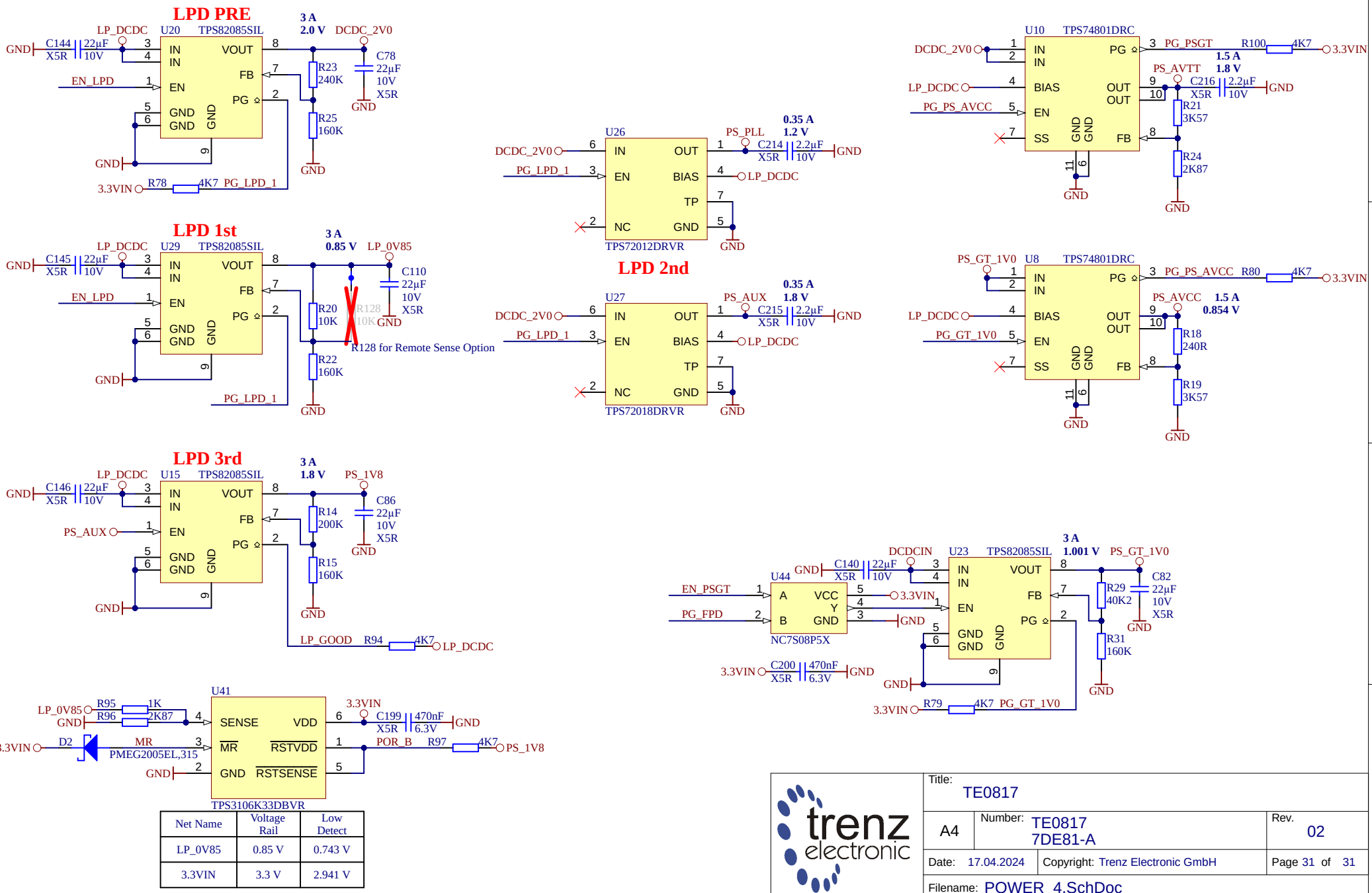

Net Name	Voltage Rail	Low Detect
LP_0V85	0.85 V	0.743 V
3.3VIN	3.3 V	2.941 V

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