

Regarding the usage of our schematics and alike documentation for Trenz module TE0818.


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TE0818 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

	Title: <b>TE0818 - Legal Notices</b>		
	A4	Number: <b>TE0818 9BE81-A</b>	Rev. <b>02</b>
	Date: <b>19.09.2023</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>1</b> of <b>31</b>
	Filename: <b>Legal Notices Modules.SchDoc</b>		

REV	DATE	Description	
-01	2021-05	Initial revision	VT
-02	2023-10	<ol style="list-style-type: none"> <li>Added capacitors <b>C178</b>, <b>C187</b>, <b>C188</b>, <b>C189</b> (470nF) to VTT net.</li> <li>Added <b>U18/U37</b> compensation network: <b>R119</b>, <b>C190</b>, <b>C191</b>. <b>R118</b> is optional jumper and is installed when using the internal compensation network. External compensation network is used by default.</li> <li>Connected all DDR4 TEN pins together and pulled them down with resistor <b>R120</b> and added testpoint <b>TP23</b>.</li> <li>Added testpoints <b>TP25</b>, <b>TP27</b>, <b>TP29</b>, <b>TP35</b>, <b>TP37</b>... <b>TP79</b>.</li> <li>Changed capacitor <b>C112</b> size from 0402 to 0201 and voltage rating from 16 V to 10 V.</li> <li>Changed ferrid beads from MPZ0603S121HT000 to BLM15PX800SZ1D for <b>L1</b>, <b>L2</b>, <b>L3</b>, <b>L4</b>, <b>L5</b>, and <b>L7</b>.</li> <li>Changed ferrid beads from MPZ1608S221A to BLM15PX800SZ1D for <b>L6</b> and <b>L8</b>.</li> <li>Added diode <b>D2</b> between <b>U41</b> pin 3 net <b>MR</b> and voltage rail <b>3.3VIN</b>.</li> <li>Modified trace length.</li> <li>Updated documentation overviews.</li> </ol>	VY/ED
-02a	2023-10-12	1. Changed inductors <b>L1</b> ... <b>L8</b> from BLM15PX800SZ1D to BLM15PX800SN1D.	ED
-02b	2024-06-05	1. Changed the value of resistor <b>R119</b> from 33.2 kOhm to 15 kOhm to improve the stability of <b>U19</b> / <b>U37</b> .	VY

		Title: <b>TE0818 - Revision History</b>	
		A4	Number: <b>TE0818</b> <b>9BE81-A</b>
Date: <b>05.06.2024</b>		Copyright: <b>Trenz Electronic GmbH</b>	
Filename: <b>Revision_Changes.SchDoc</b>		Page <b>2</b> of <b>31</b>	

### Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3VIN	IN	3.3V	+/- 5 %	Micromodule Power	Management voltage rail, supplied by power rail
PL_DCIN	IN	3.3V	+/- 5 %	Micromodule Power	Programmable Logic, supplied by power rail
LP_DCDC	IN	3.3V	+/- 3 %	Micromodule Power	Low-Power Domain, supplied by power rail
GT_DCDC	IN	3.3V	+/- 3 %	Micromodule Power	GTH Transceiver, supplied by power rail
DCDCIN	IN	3.3V	+/- 5 %	Micromodule Power	Full-Power Domain and GTR, supplied by power rail
VCCO_64	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 64	Supplied by external power rail via B2B connector
VCCO_65	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 65	Supplied by external power rail via B2B connector
VCCO_66	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 66	Supplied by external power rail via B2B connector
VCCO_47	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 47	Supplied by external power rail via B2B connector
VCCO_48	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 48	Supplied by external power rail via B2B connector
PSBATT	IN	1.2 V - 1.5 V	-	RTC / BBRAM	Supplied by external power rail via B2B connector
PLL_3V3	IN	3.3 V	+/- 3 %	Power for PLL	Supplied by external power rail via B2B connector
PL_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Micromodule: Programmable Logic
PS_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Micromodule: Processing System
DDR_1V2	OUT	1.2 V	+/- 3 %	Power for Carrier	Micromodule: PS DDR I/O Supply

A

A

B

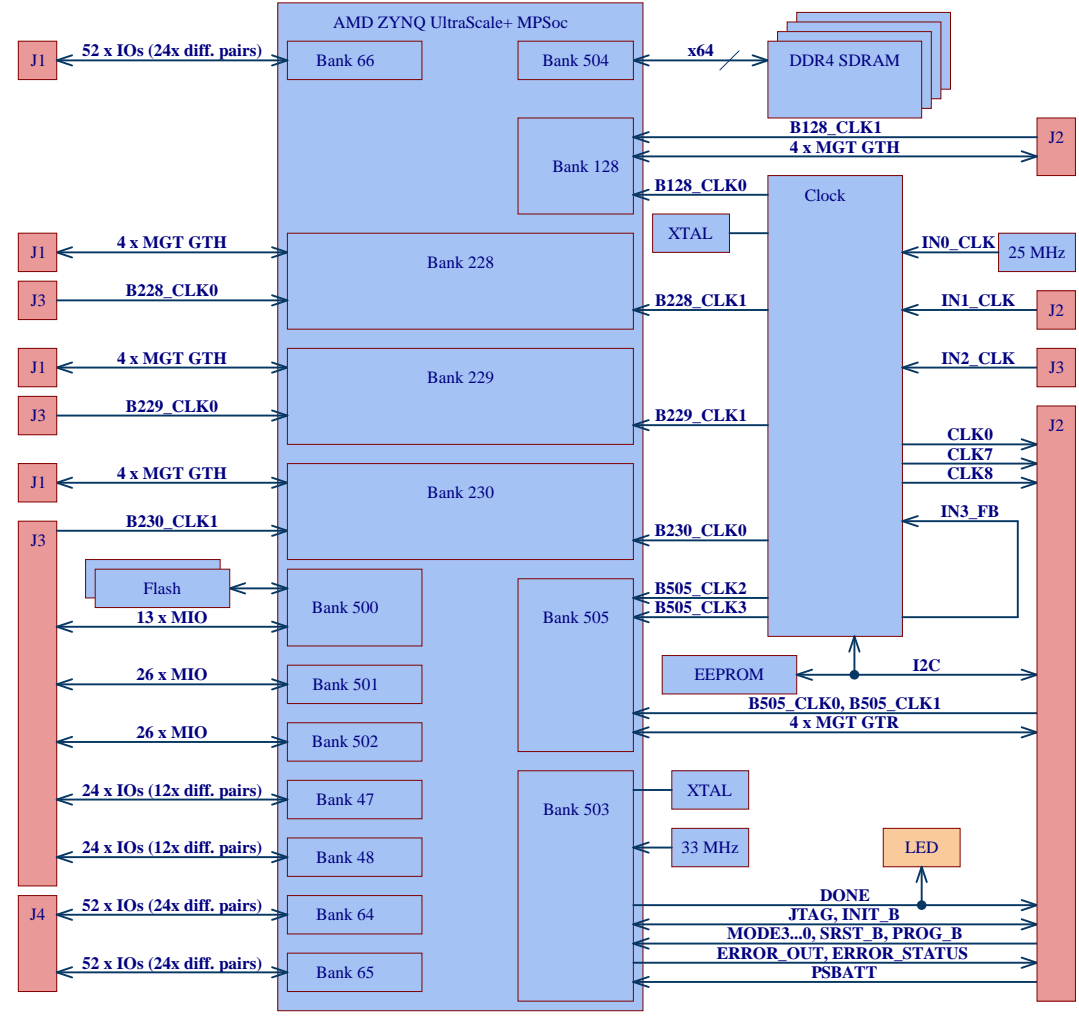
B

C

C

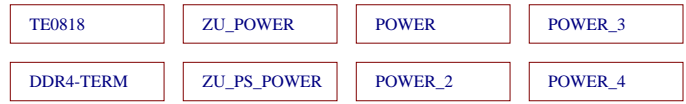
D

D



### Legend:

- B2B Connector
- LED Interface
- On-board Components



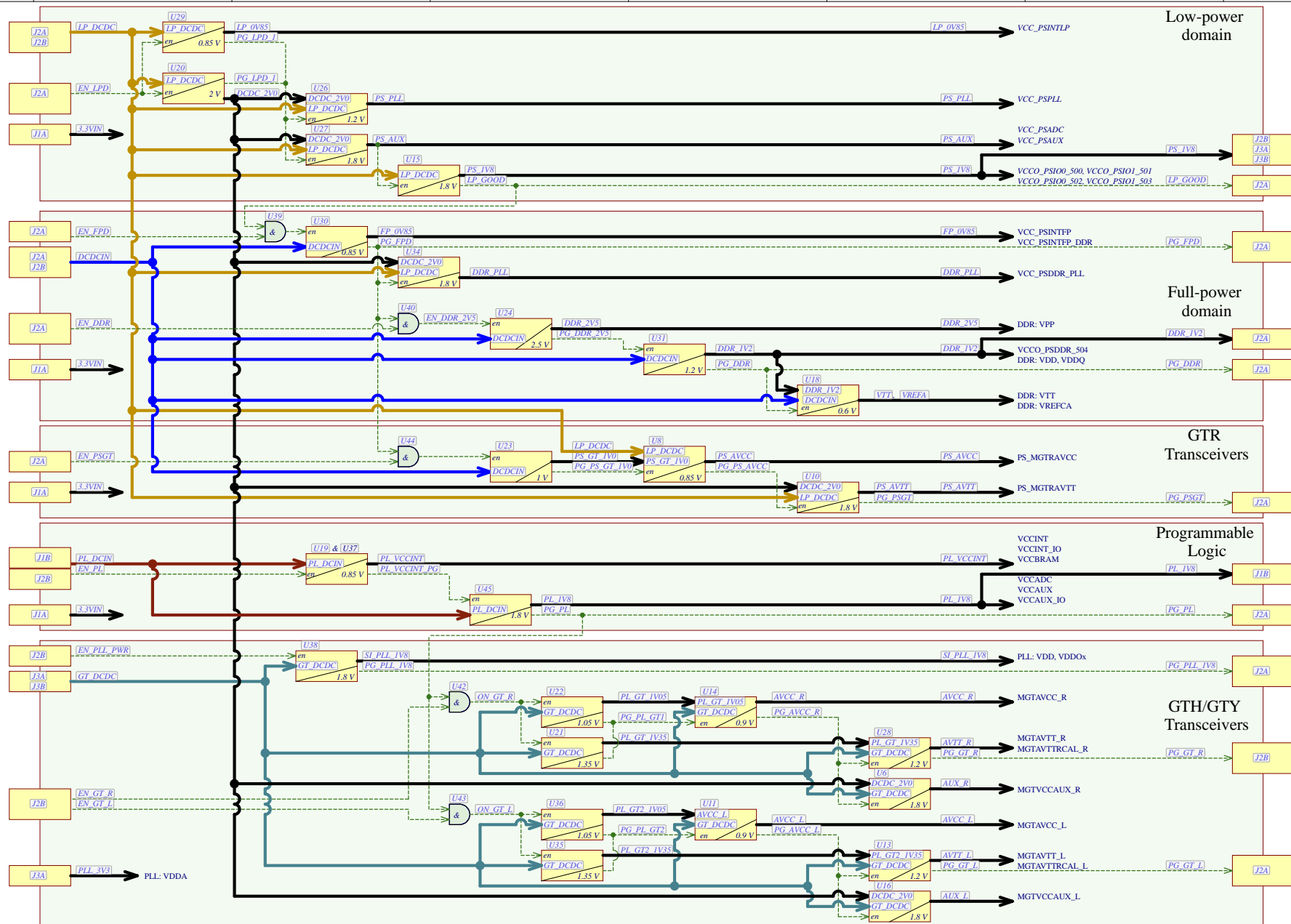
### I2C Address:

Device	I2C ADDR	Note
PLL <b>U5</b>	0x69	-
EEPROM <b>U4</b>	0x50	-

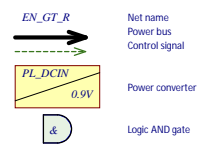
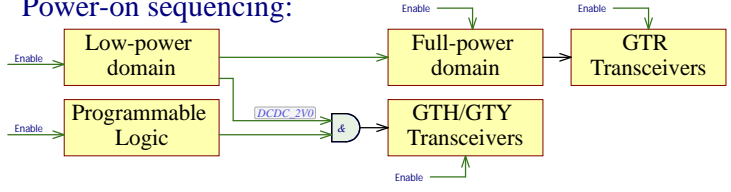


Title: **TE0818 - System Overview**

A4	Number: <b>TE0818 9BE81-A</b>	Rev. <b>02</b>
Date: 19.09.2023	Copyright: Trenz Electronic GmbH	Page 3 of 31
Filename: <b>TE0818-Overview.SchDoc</b>		



**Power-on sequencing:**



Title: TE0818 - Power Diagram		
A3	Number: TE0818 9BE81-A	Rev. 02
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Special notes:

Serial  
 Serialnummer 6,3 x 6.3mm  
 LOGO1

TE Logo PRINT Layer

LOGO PRINT  
 MECH1

TE Address Overlay

LOGO ADDRESS  
 CE

CE Logo on Top Overlay

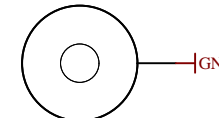
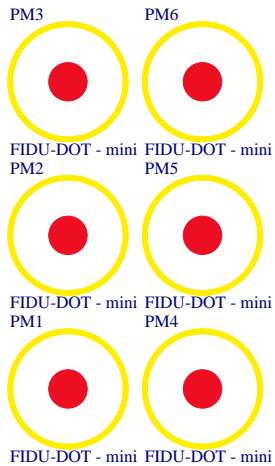
CE-TOPOVERLAY  
 RoHS

RoHS Logo on Top Overlay

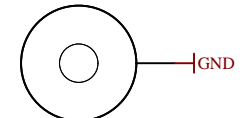
RoHS-TOPOVERLAY  
 WEEE

WEEE Logo on Top Overlay

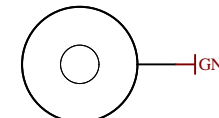
WEEE-TOPOVERLAY



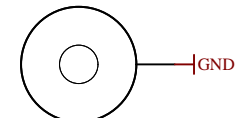
Mount.Hole 3.2mm für Unterlegscheibe



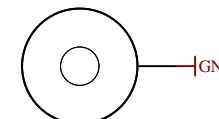
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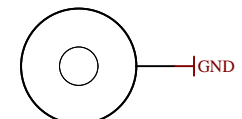
Mount.Hole 3.2mm für Unterlegscheibe



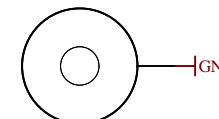
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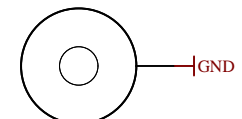
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe

Design drawn by: ED  
 Checked by: VY  
 Assembly variant: 9BE81-A  
 Created by: ED  
 Modified by: ED  
 Modified at: 2023-09-20



Title: <b>TE0818</b>		
A4	Number: <b>TE0818 9BE81-A</b>	Rev. <b>02</b>
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1

2

3

4

A

A

B

B

C

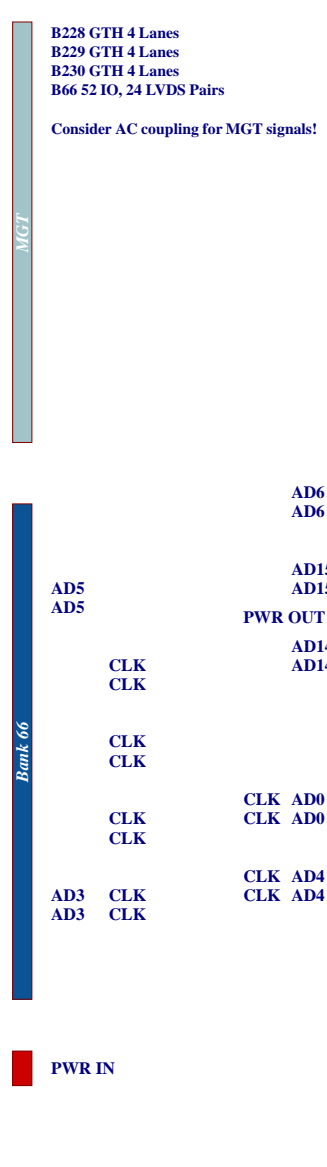
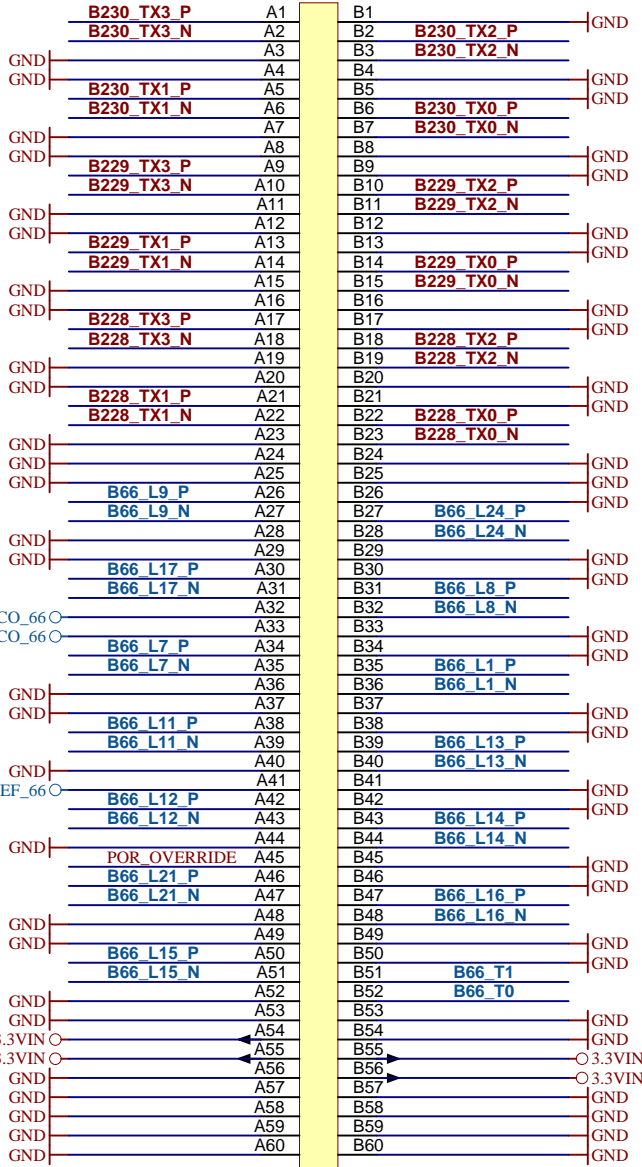
C

D

D

J1A ADM6-60-01.5-L-4-2-FR

J1B ADM6-60-01.5-L-4-2-FR



B228 GTH 4 Lanes  
 B229 GTH 4 Lanes  
 B230 GTH 4 Lanes  
 B66 52 IO, 24 LVDS Pairs

Consider AC coupling for MGT signals!

MGT

MGT

MGT

MGT

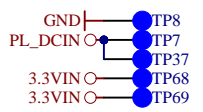
Bank 66

Bank 66

Bank 66

Bank 66

- Bank 47 HD 0..VCC047
- Bank 48 HD 0..VCC048
- Bank 64 HP 0..VCC064
- Bank 65 HP 0..VCC065
- Bank 66 HP 0..VCC066



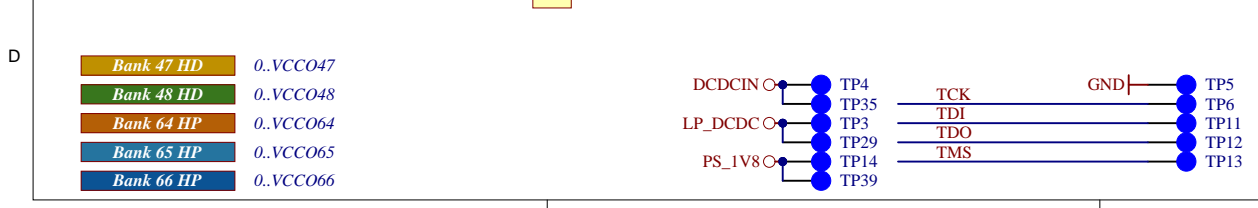
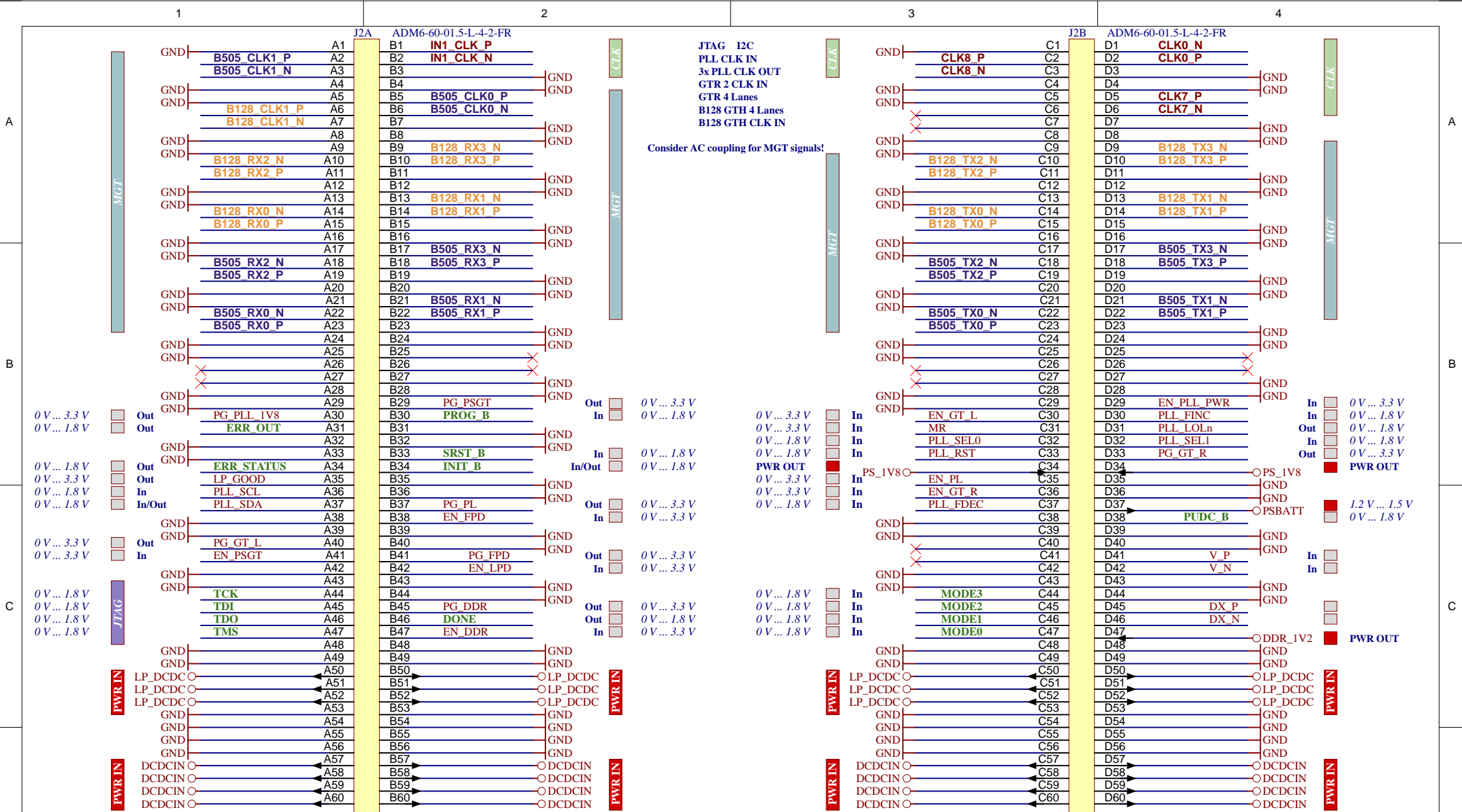
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A4	Number: TE0818 9BE81-A	Rev. 02
Date: 09.10.2023	Copyright: Trenz Electronic GmbH	Page 6 of 31
Filename: J1.SchDoc		

1

2

3

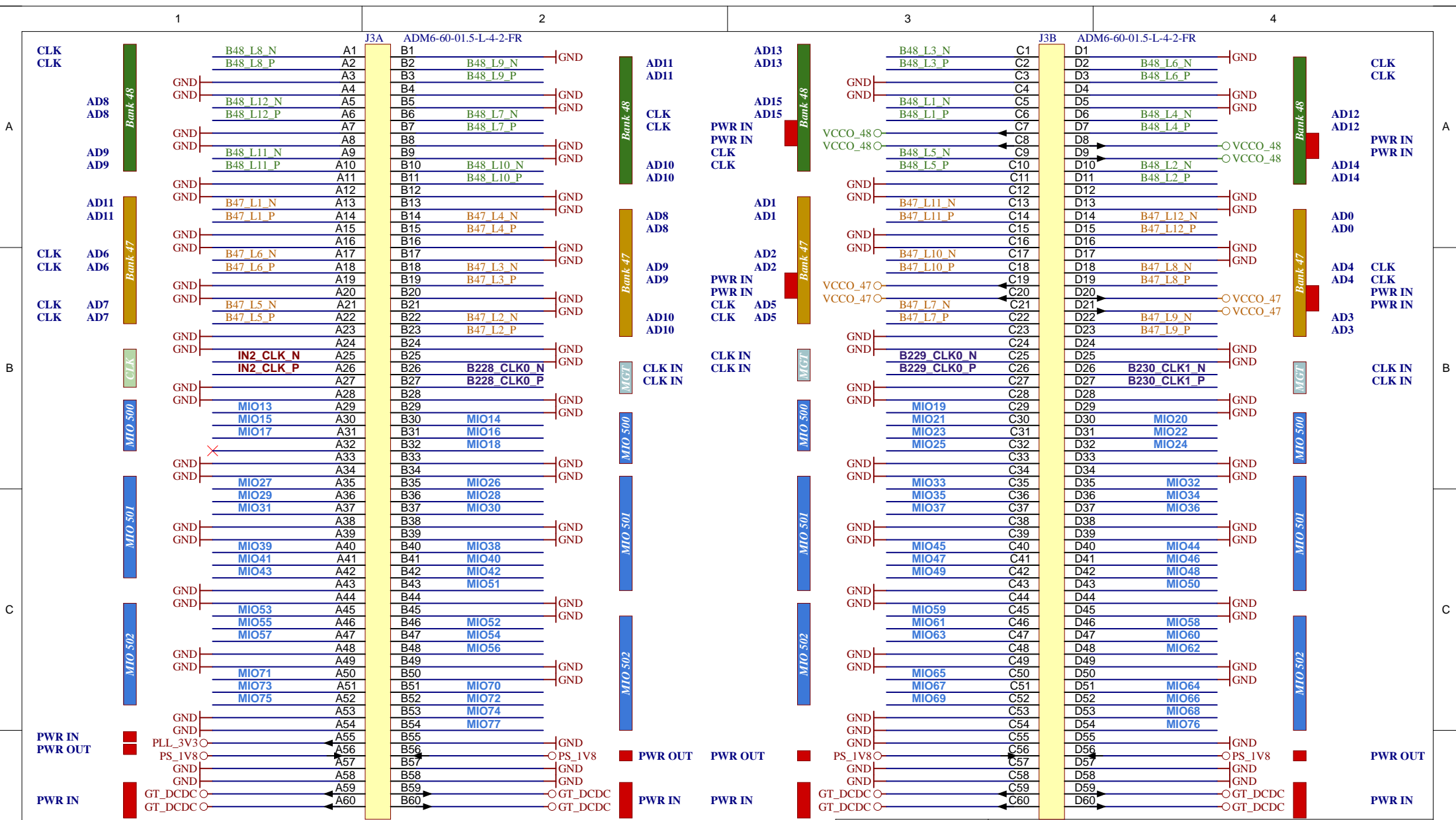
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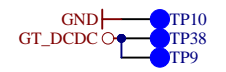
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A4	Number: <b>TE0818 9BE81-A</b>	Rev. <b>02</b>
Date: <b>09.10.2023</b>	Copyright: Trenz Electronic GmbH	
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Filename: **J2.SchDoc**



- Bank 47 HD 0..VCC047
  - Bank 48 HD 0..VCC048
  - Bank 64 HP 0..VCC064
  - Bank 65 HP 0..VCC065
  - Bank 66 HP 0..VCC066
- B47 24 IO, 12 LVDS Pairs  
 B48 24 IO, 12 LVDS Pairs  
 B228 GTH CLK IN  
 B229 GTH CLK IN  
 B230 GTH CLK IN  
 65 MIO  
 PLL CLK IN



Title: TE0818 - Connector J3		
A4	Number: TE0818 9BE81-A	Rev. 02
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Filename: J3.SchDoc		



1

2

3

4

A

B

C

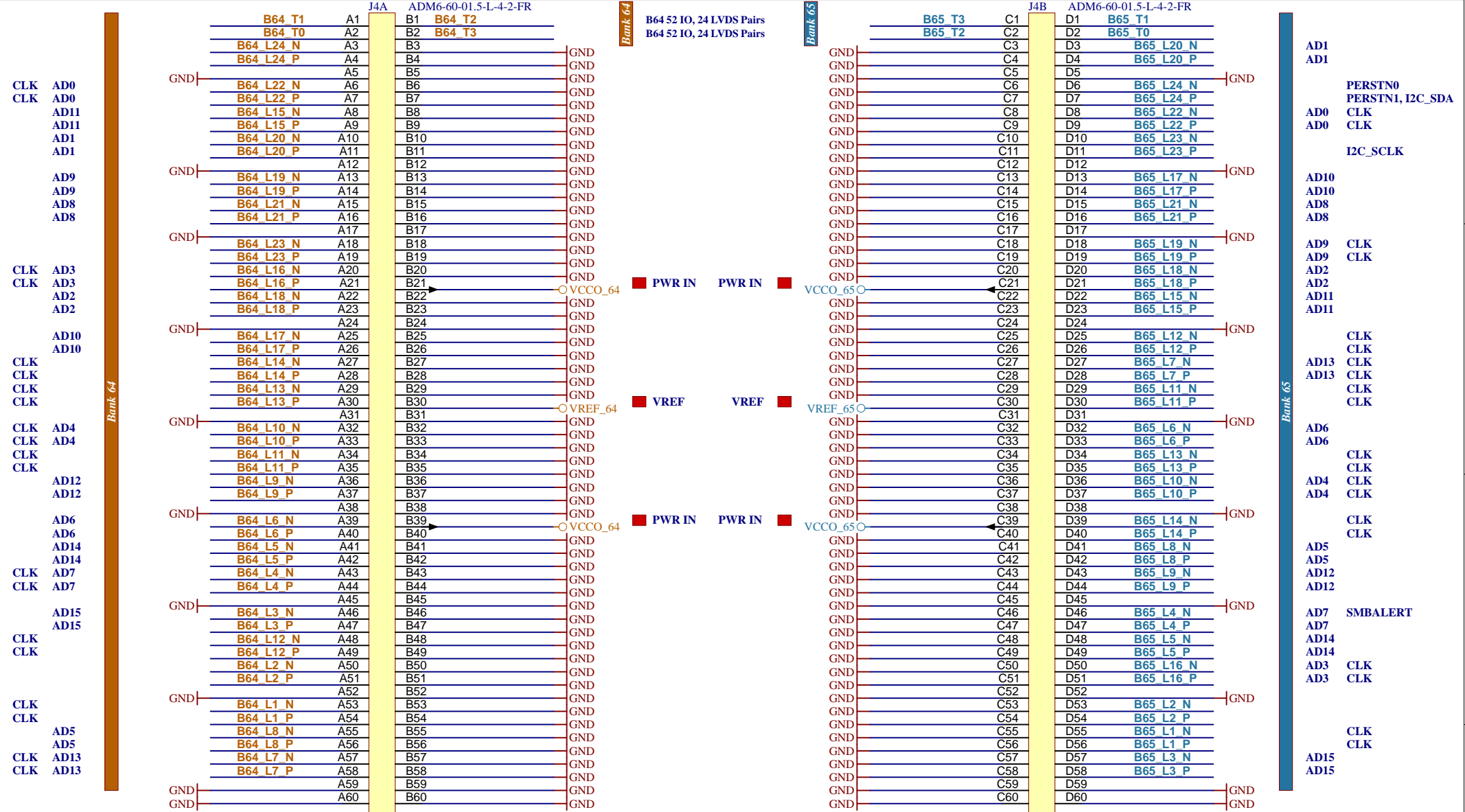
D

A

B

C

D



- Bank 47 HD 0..VCCO47
- Bank 48 HD 0..VCCO48
- Bank 64 HP 0..VCCO64
- Bank 65 HP 0..VCCO65
- Bank 66 HP 0..VCCO66



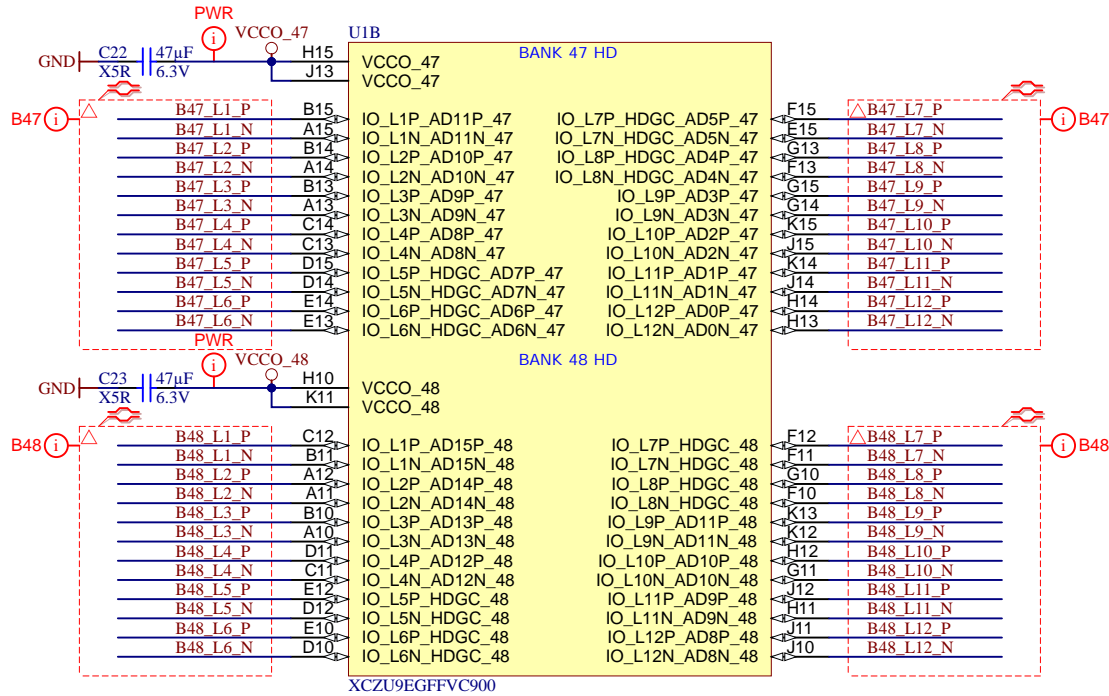
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A4	Number: TE0818 9BE81-A	Rev. 02
Date: 09.10.2023	Copyright: Trenz Electronic GmbH	Page 9 of 31
Filename: J4.SchDoc		


1

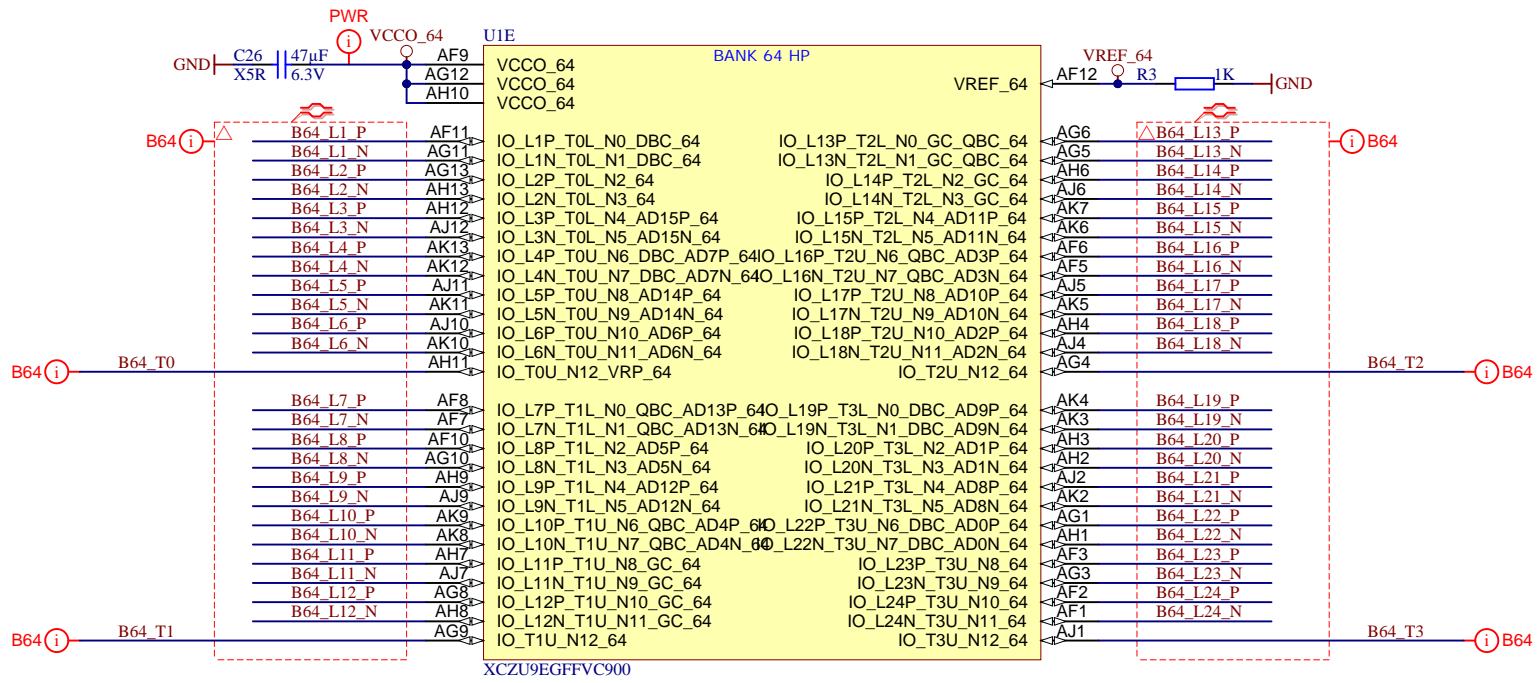
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3

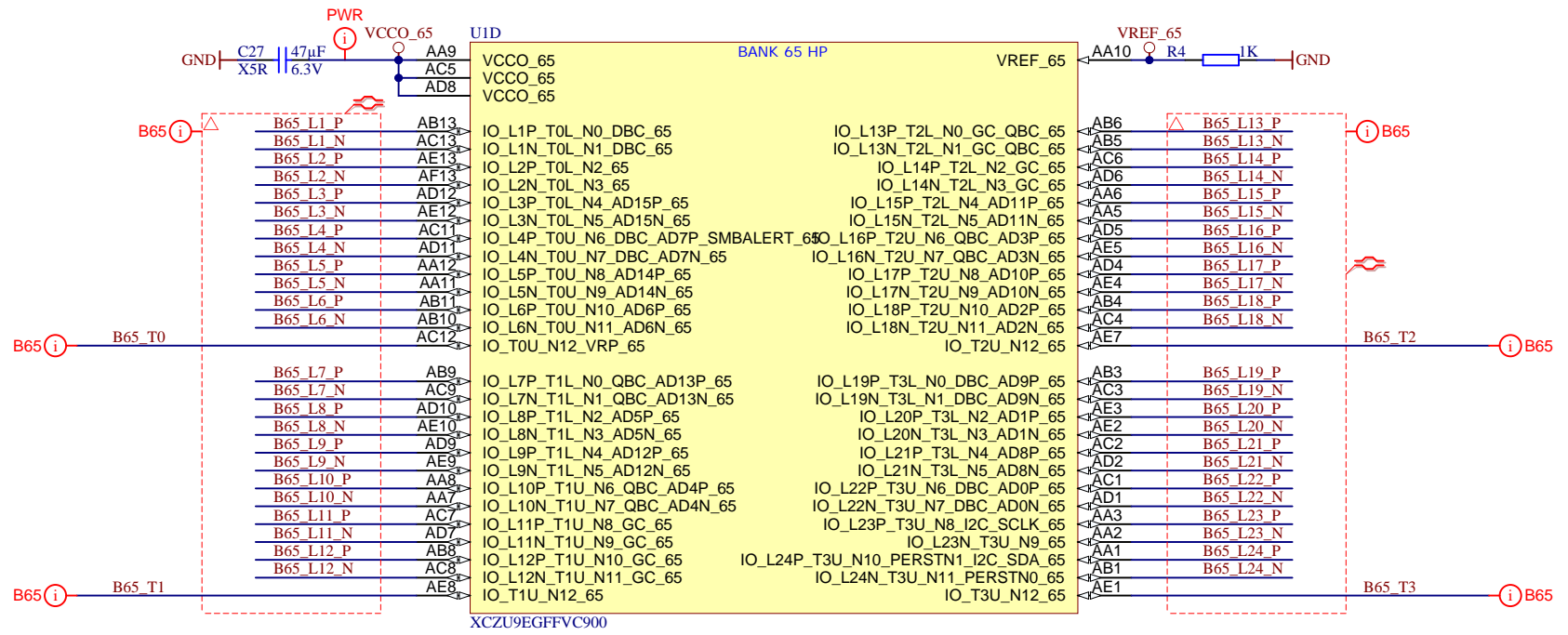
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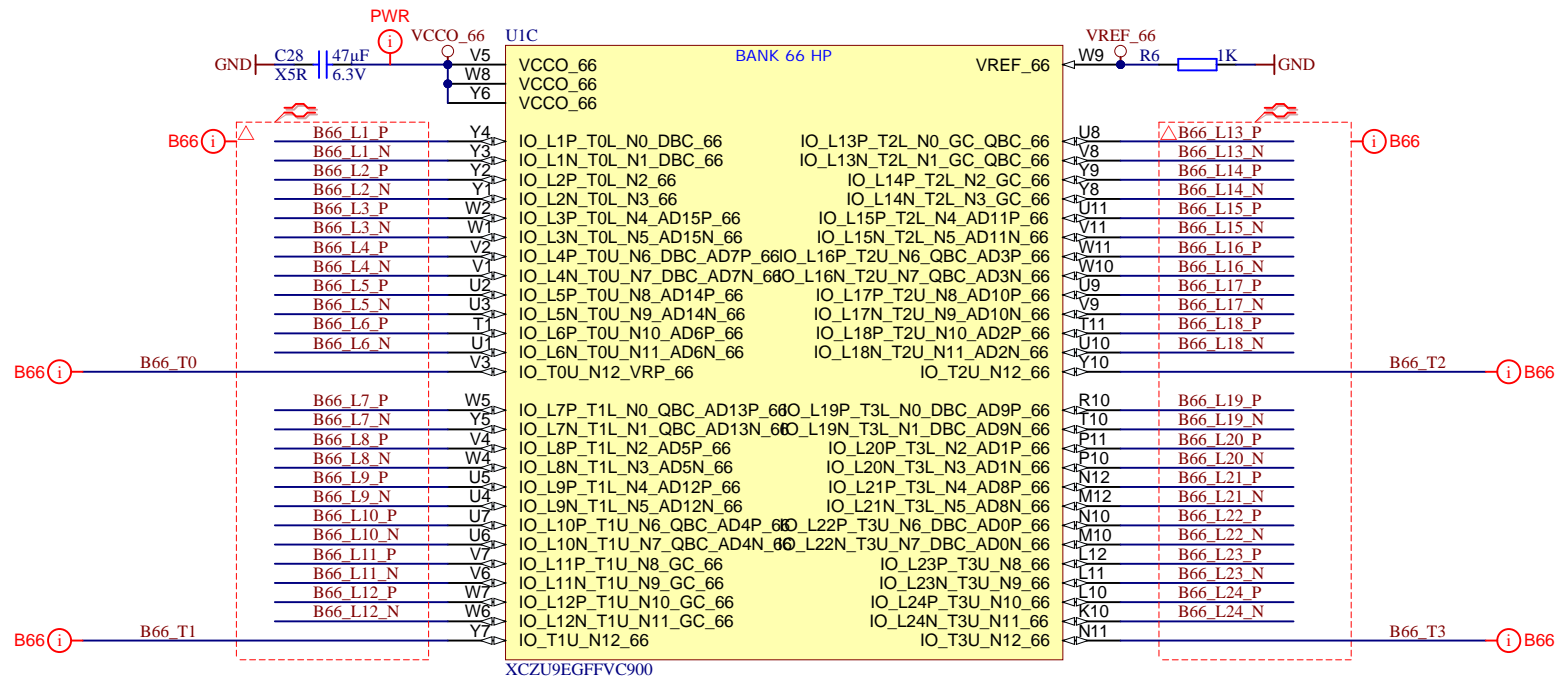
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	A4	Number: TE0818 9BE81-A	Rev. 02
	Date: 09.10.2023	Copyright: Trenz Electronic GmbH	Page 10 of 31
	Filename: B_HD.SchDoc		



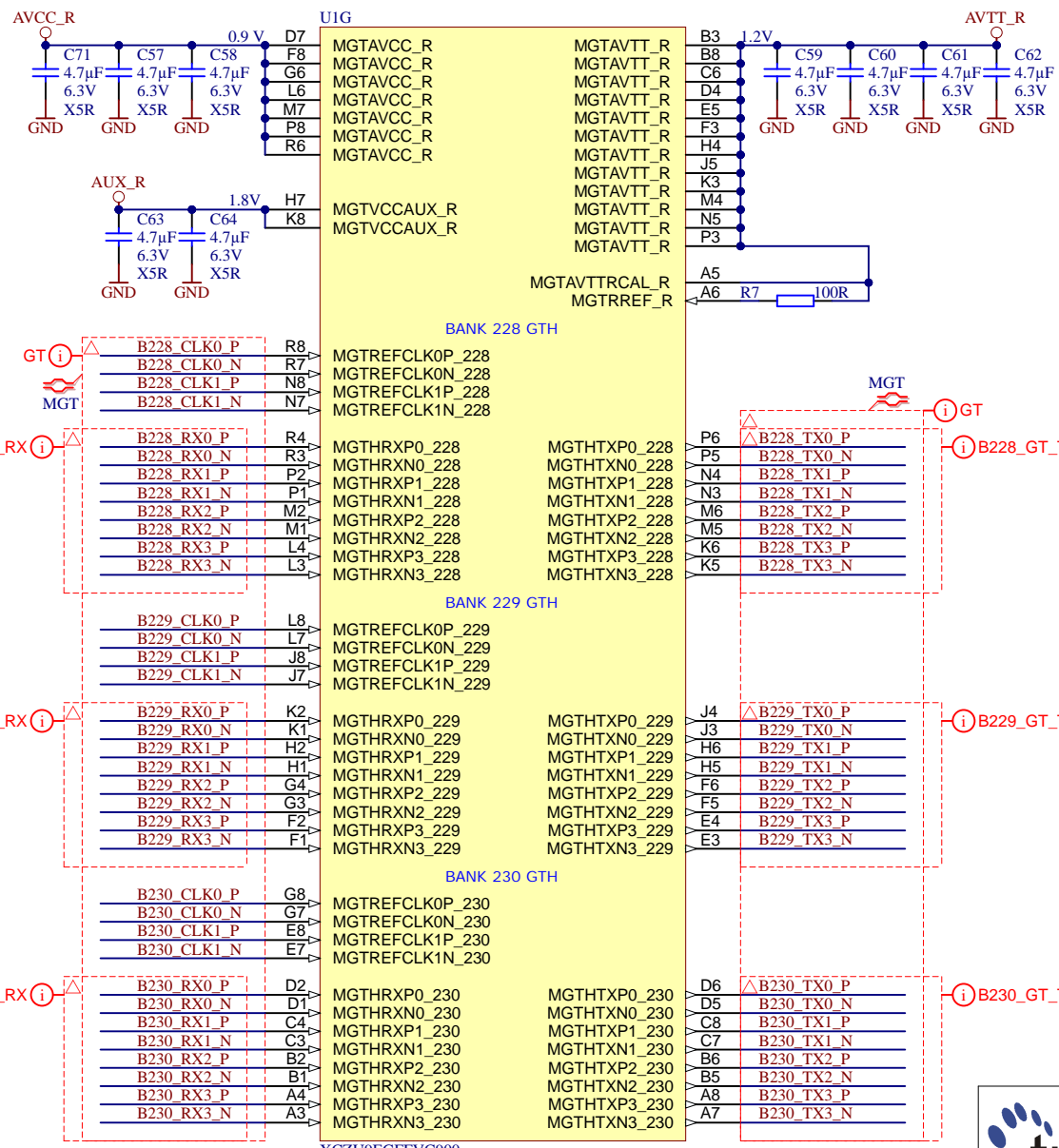
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A4	Number: TE0818 9BE81-A	Rev. 02
Date: 09.10.2023	Copyright: Trenz Electronic GmbH	Page 11 of 31
Filename: B64.SchDoc		



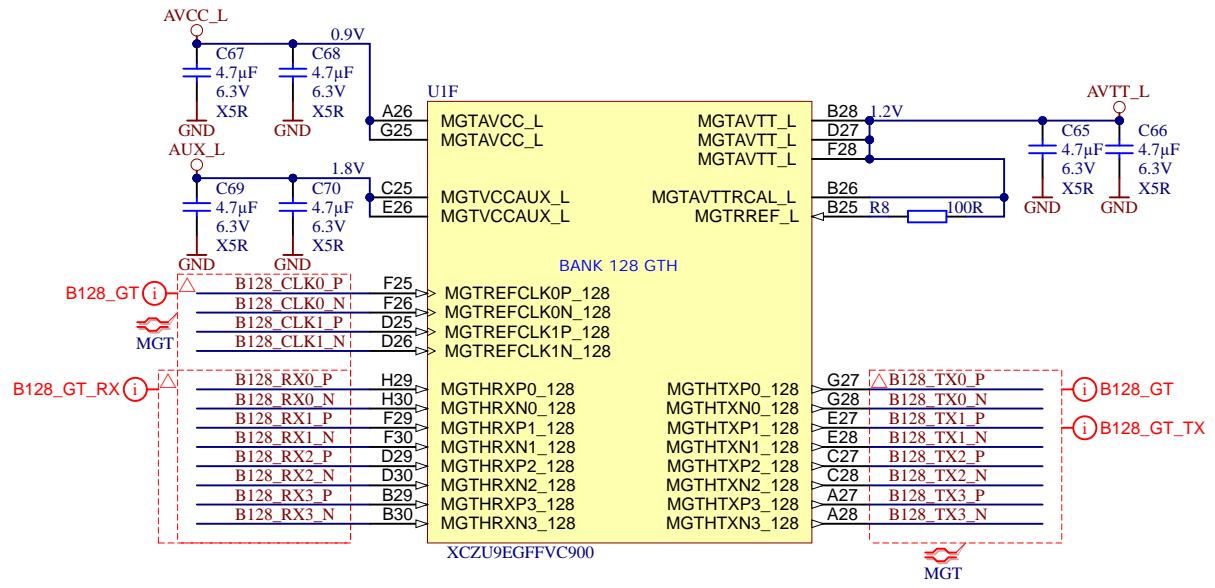
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A4	Number: TE0818 9BE81-A	Rev. 02
Date: 09.10.2023	Copyright: Trenz Electronic GmbH	Page 12 of 31
Filename: B65.SchDoc		



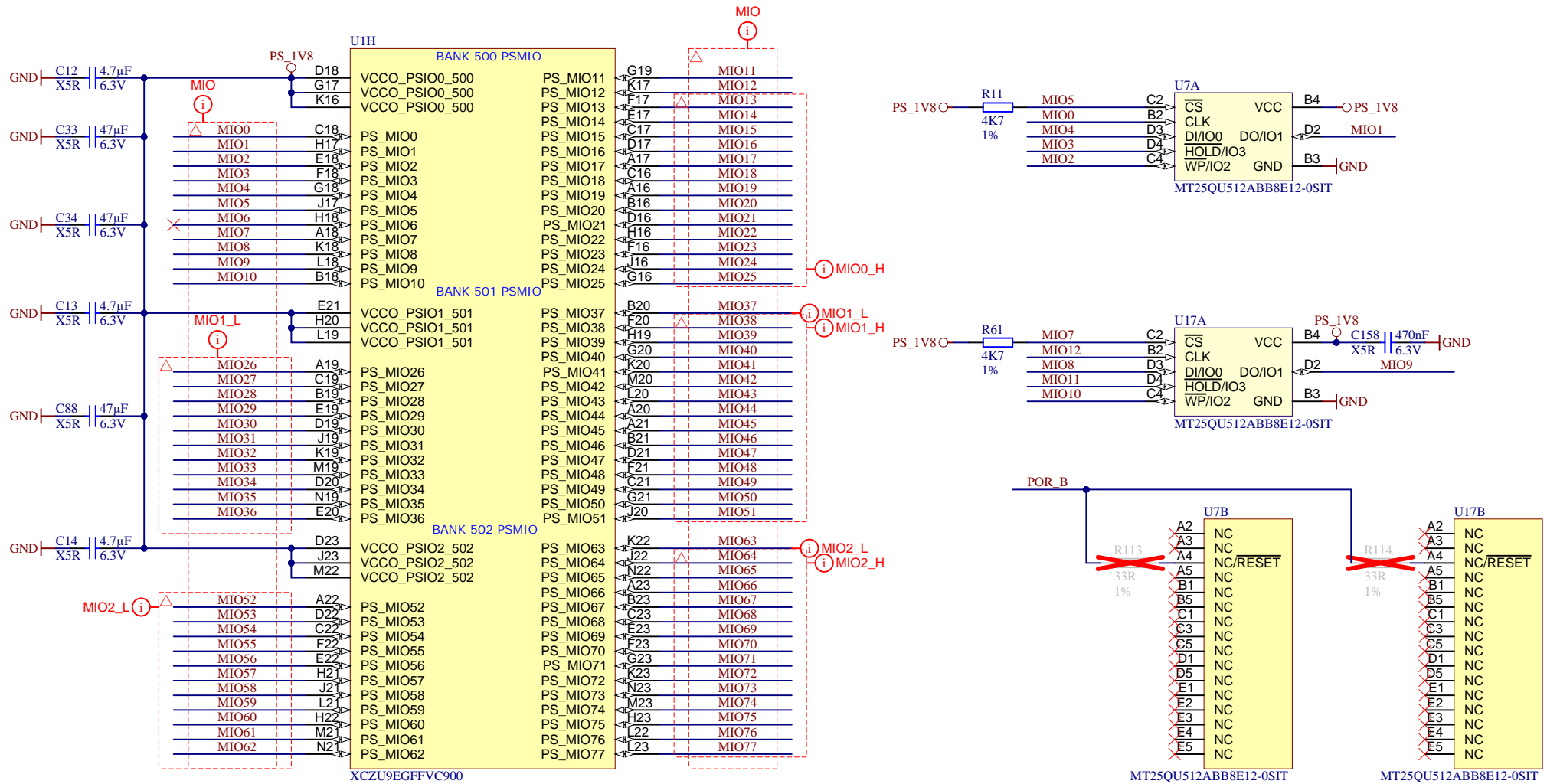
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A4	Number: TE0818 9BE81-A	Rev. 02
Date: 09.10.2023	Copyright: Trenz Electronic GmbH	Page 13 of 31
Filename: B66.SchDoc		



Title: TE0818 - GTH Bank 1		
A4	Number: TE0818 9BE81-A	Rev. 02
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Filename: B_GT.SchDoc		

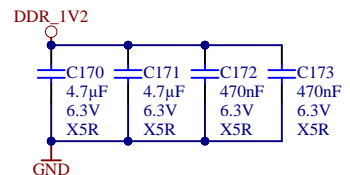
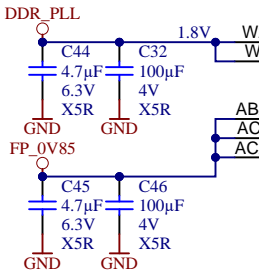
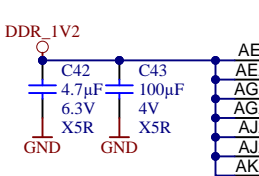


Title: TE0818 - GTH Bank 2		
A4	Number: TE0818 9BE81-A	Rev. 02
Date: 09.10.2023	Copyright: Trenz Electronic GmbH	Page 15 of 31
Filename: B_GT_2.SchDoc		



	Title: <b>TE0818 - MIO Banks</b>	
	A4	Number: <b>TE0818 9BE81-A</b>
	Date: <b>09.10.2023</b>	Copyright: <b>Trenz Electronic GmbH</b>
	Filename: <b>B_MIO.SchDoc</b>	Rev. <b>02</b>
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UIJ		BANK 504 PSDDR	
VCCO_PSDDR_504	PS_DDR_CK0	AJ26	DDR4-CLK0_P
VCCO_PSDDR_504	PS_DDR_CK_N0	AJ27	DDR4-CLK0_N
VCCO_PSDDR_504	PS_DDR_CKE0	AJ25	DDR4-CKE0
VCCO_PSDDR_504		AG23	
VCCO_PSDDR_504	PS_DDR_CK1	AG24	
VCCO_PSDDR_504	PS_DDR_CK_N1	AG24	
VCCO_PSDDR_504	PS_DDR_CKE1	AH27	
VCCO_PSDDR_504		AK25	DDR4-A0
VCCO_PSDDR_504	PS_DDR_A0	AK28	DDR4-A1
VCCO_PSDDR_504	PS_DDR_A1	AK27	DDR4-A2
VCCO_PSDDR_504	PS_DDR_A2	AH24	DDR4-A3
VCCO_PSDDR_504	PS_DDR_A3	AK24	DDR4-A4
VCCO_PSDDR_504	PS_DDR_A4	AJ30	DDR4-A5
VCCO_PSDDR_504	PS_DDR_A5	AE22	DDR4-A6
VCCO_PSDDR_504	PS_DDR_A6	AE25	DDR4-A7
VCCO_PSDDR_504	PS_DDR_A7	AE23	DDR4-A8
VCCO_PSDDR_504	PS_DDR_A8	AE24	DDR4-A9
VCCO_PSDDR_504	PS_DDR_A9	AD22	DDR4-A10
VCCO_PSDDR_504	PS_DDR_A10	AH23	DDR4-A11
VCCO_PSDDR_504	PS_DDR_A11	AF21	DDR4-A12
VCCO_PSDDR_504	PS_DDR_A12	AG21	DDR4-A13
VCCO_PSDDR_504	PS_DDR_A13	AF22	DDR4-A14
VCCO_PSDDR_504	PS_DDR_A14	AF23	DDR4-A15
VCCO_PSDDR_504	PS_DDR_A15	AD21	DDR4-A16
VCCO_PSDDR_504	PS_DDR_A16	AD20	DDR4-A17
VCCO_PSDDR_504	PS_DDR_A17		
VCCO_PSDDR_504	PS_DDR_CS_N0	AJ24	DDR4-CS
VCCO_PSDDR_504	PS_DDR_CS_N1	AG25	
VCCO_PSDDR_504	PS_DDR_BA0	AG26	DDR4-BA0
VCCO_PSDDR_504	PS_DDR_BA1	AF25	DDR4-BA1
VCCO_PSDDR_504	PS_DDR_BG0	AF26	DDR4-BG0
VCCO_PSDDR_504	PS_DDR_BG1	AD26	DDR4-BG1
VCCO_PSDDR_504	PS_DDR_PARITY	AC14	DDR4-PAR
VCCO_PSDDR_504	PS_DDR_RAM_RST_N	AC16	DDR4-RESET
VCCO_PSDDR_504	PS_DDR_ACT_N	AC17	DDR4-ACT
VCCO_PSDDR_504	PS_DDR_ALERT_N	AD19	DDR4-ALERT
VCCO_PSDDR_504	PS_DDR_ZQ	AC23	R2 240R
VCCO_PSDDR_504	PS_DDR_ODT0	AJ29	DDR4-ODT0
VCCO_PSDDR_504	PS_DDR_ODT1	AH26	

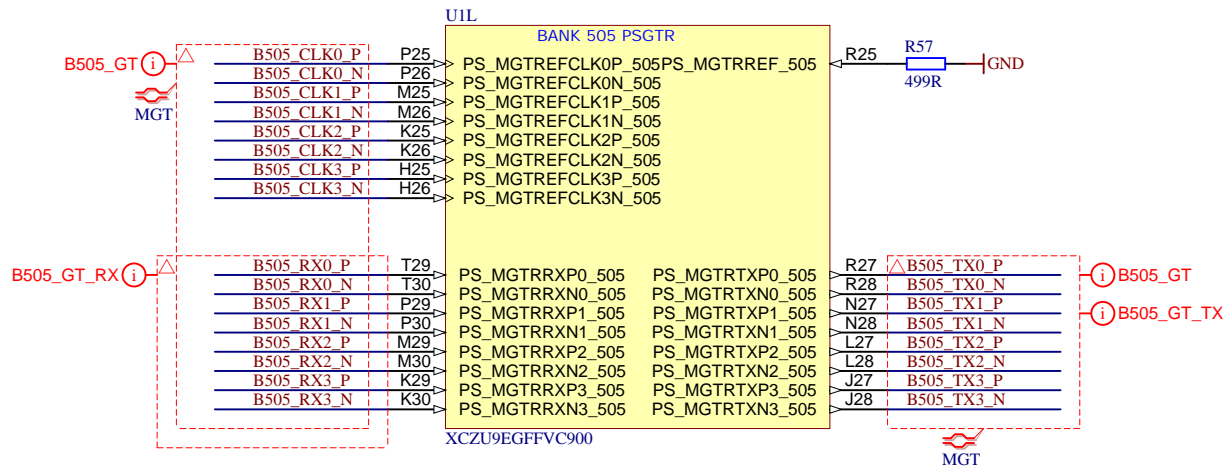
XCZU9EGFFVC900


UIK		BANK 504 PSDDR	
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DQ1	AH17	PS_DDR_DQ1	PS_DDR_DQ33
DQ2	AJ17	PS_DDR_DQ2	PS_DDR_DQ34
DQ3	AH16	PS_DDR_DQ3	PS_DDR_DQ35
DQ4	AK15	PS_DDR_DQ4	PS_DDR_DQ36
DQ5	AK14	PS_DDR_DQ5	PS_DDR_DQ37
DQ6	AJ14	PS_DDR_DQ6	PS_DDR_DQ38
DQ7	AH14	PS_DDR_DQ7	PS_DDR_DQ39
DQ8	AK19	PS_DDR_DQ8	PS_DDR_DQ40
DQ9	AK18	PS_DDR_DQ9	PS_DDR_DQ41
DQ10	AJ19	PS_DDR_DQ10	PS_DDR_DQ42
DQ11	AH19	PS_DDR_DQ11	PS_DDR_DQ43
DQ12	AK21	PS_DDR_DQ12	PS_DDR_DQ44
DQ13	AK22	PS_DDR_DQ13	PS_DDR_DQ45
DQ14	AH21	PS_DDR_DQ14	PS_DDR_DQ46
DQ15	AJ22	PS_DDR_DQ15	PS_DDR_DQ47
DQ16	AG12	PS_DDR_DQ16	PS_DDR_DQ48
DQ17	AG15	PS_DDR_DQ17	PS_DDR_DQ49
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DQ19	AF16	PS_DDR_DQ19	PS_DDR_DQ51
DQ20	AD14	PS_DDR_DQ20	PS_DDR_DQ52
DQ21	AD16	PS_DDR_DQ21	PS_DDR_DQ53
DQ22	AD15	PS_DDR_DQ22	PS_DDR_DQ54
DQ23	AD17	PS_DDR_DQ23	PS_DDR_DQ55
DQ24	AE17	PS_DDR_DQ24	PS_DDR_DQ56
DQ25	AE18	PS_DDR_DQ25	PS_DDR_DQ57
DQ26	AE20	PS_DDR_DQ26	PS_DDR_DQ58
DQ27	AE19	PS_DDR_DQ27	PS_DDR_DQ59
DQ28	AG18	PS_DDR_DQ28	PS_DDR_DQ60
DQ29	AH18	PS_DDR_DQ29	PS_DDR_DQ61
DQ30	AG19	PS_DDR_DQ30	PS_DDR_DQ62
DQ31	AG20	PS_DDR_DQ31	PS_DDR_DQ63
DDR4-DQS0_P	AJ15	PS_DDR_DQS_P0	PS_DDR_DQ64
DDR4-DQS0_N	AJ16	PS_DDR_DQS_N0	PS_DDR_DQ65
DDR4-DQS1_P	AJ20	PS_DDR_DQS_P1	PS_DDR_DQ66
DDR4-DQS1_N	AJ21	PS_DDR_DQS_N1	PS_DDR_DQ67
DDR4-DQS2_P	AE15	PS_DDR_DQS_P2	PS_DDR_DQ68
DDR4-DQS2_N	AF15	PS_DDR_DQS_N2	PS_DDR_DQ69
DDR4-DQS3_P	AF17	PS_DDR_DQS_P3	PS_DDR_DQ70
DDR4-DQS3_N	AF18	PS_DDR_DQS_N3	PS_DDR_DQ71
DDR4-DQS4_P	AB24	PS_DDR_DQS_P4	PS_DDR_DM0
DDR4-DQS4_N	AB25	PS_DDR_DQS_N4	PS_DDR_DM1
DDR4-DQS5_P	V26	PS_DDR_DQS_P5	PS_DDR_DM2
DDR4-DQS5_N	V27	PS_DDR_DQS_N5	PS_DDR_DM3
DDR4-DQS6_P	AC28	PS_DDR_DQS_P6	PS_DDR_DM4
DDR4-DQS6_N	AC29	PS_DDR_DQS_N6	PS_DDR_DM5
DDR4-DQS7_P	W29	PS_DDR_DQS_P7	PS_DDR_DM6
DDR4-DQS7_N	Y29	PS_DDR_DQS_N7	PS_DDR_DM7
	AG29	PS_DDR_DQS_P8	PS_DDR_DM8
	AH29	PS_DDR_DQS_N8	

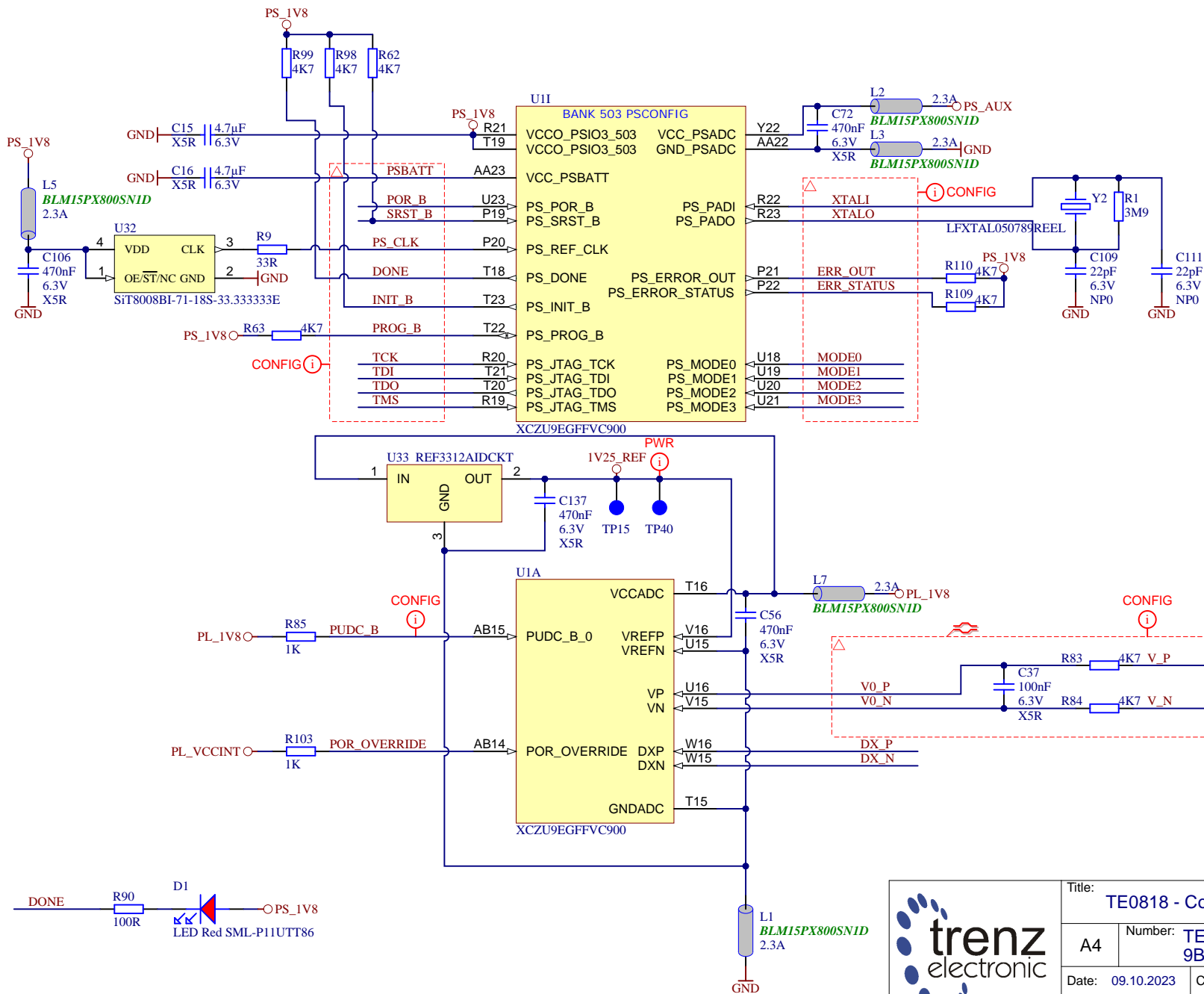
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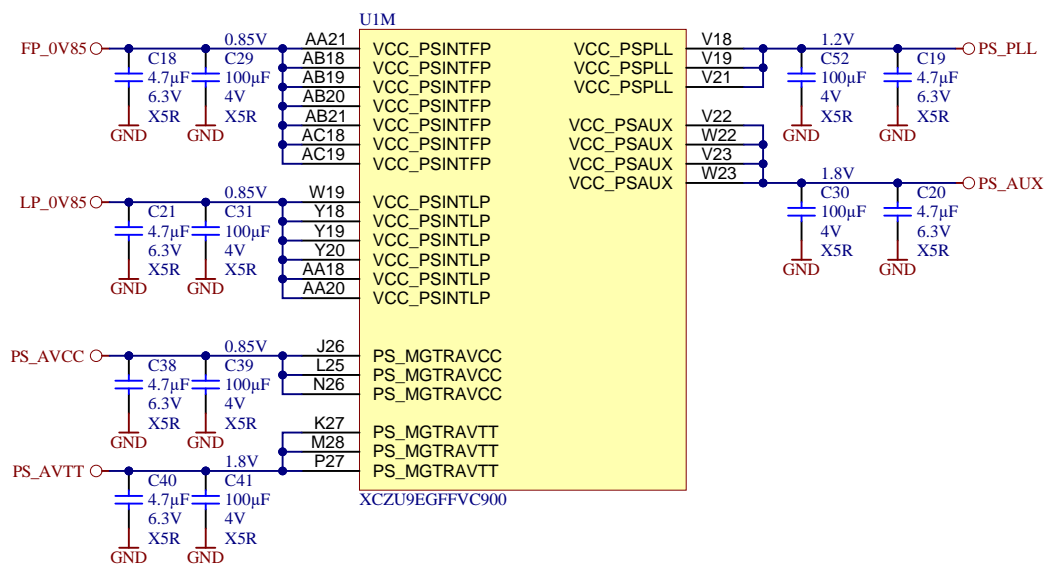

Title: TE0818 - PS DDR		
A4	Number: TE0818 9BE81-A	Rev. 02
Date: 09.10.2023	Copyright: Trenz Electronic GmbH	Page 17 of 31
Filename: PS_DDR.SchDoc		



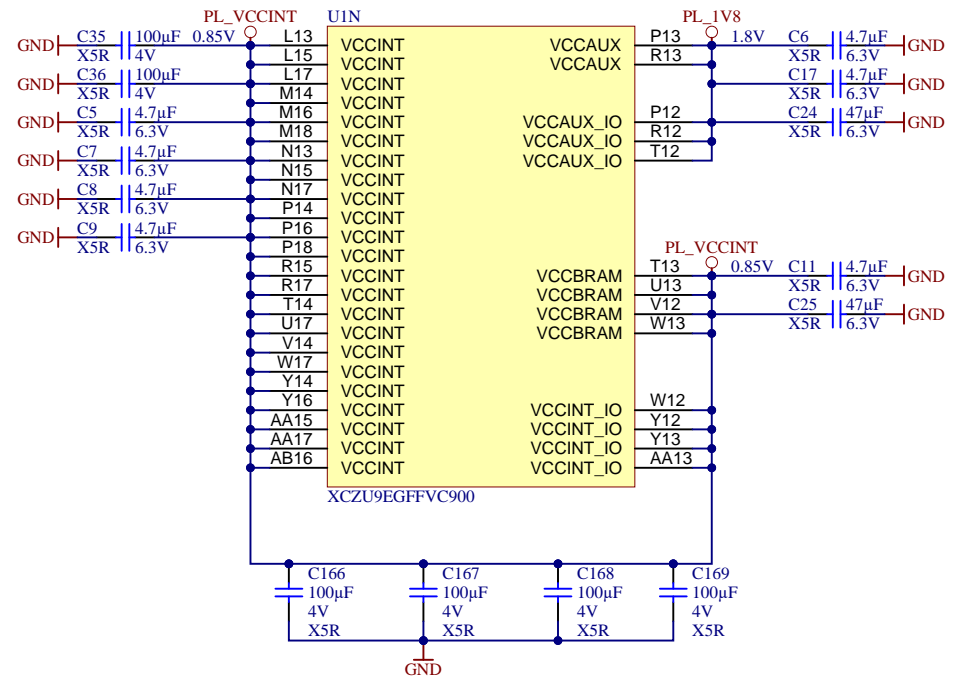
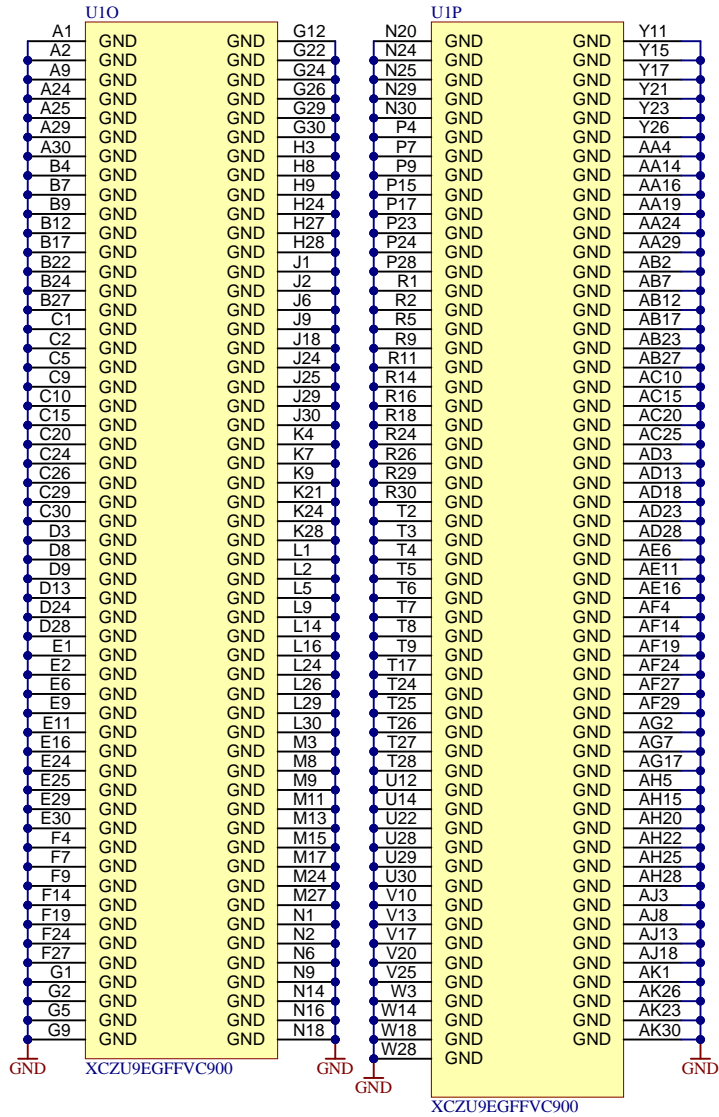
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	A4	Number: TE0818 9BE81-A	Rev. 02
	Date: 09.10.2023	Copyright: Trenz Electronic GmbH	Page 18 of 31
	Filename: B_PS_GT.SchDoc		



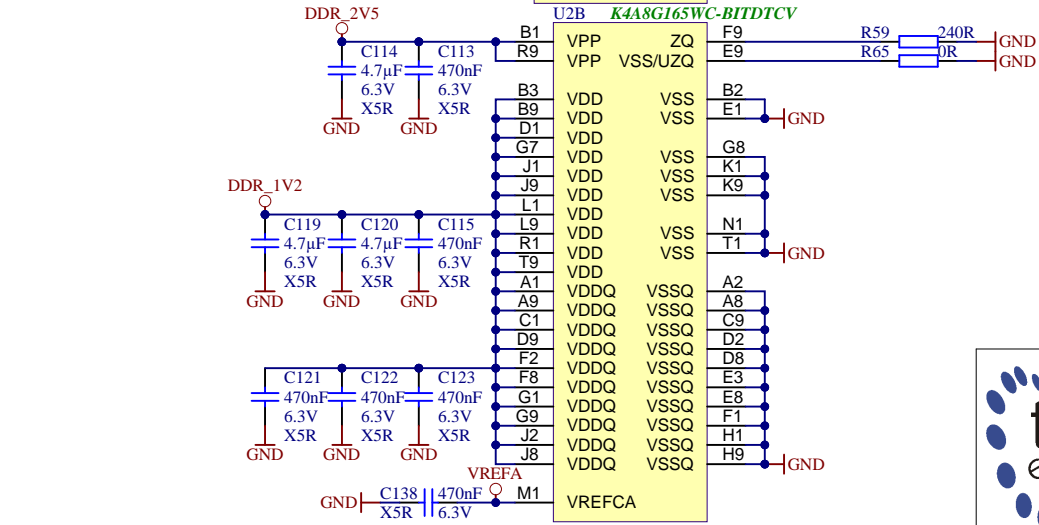
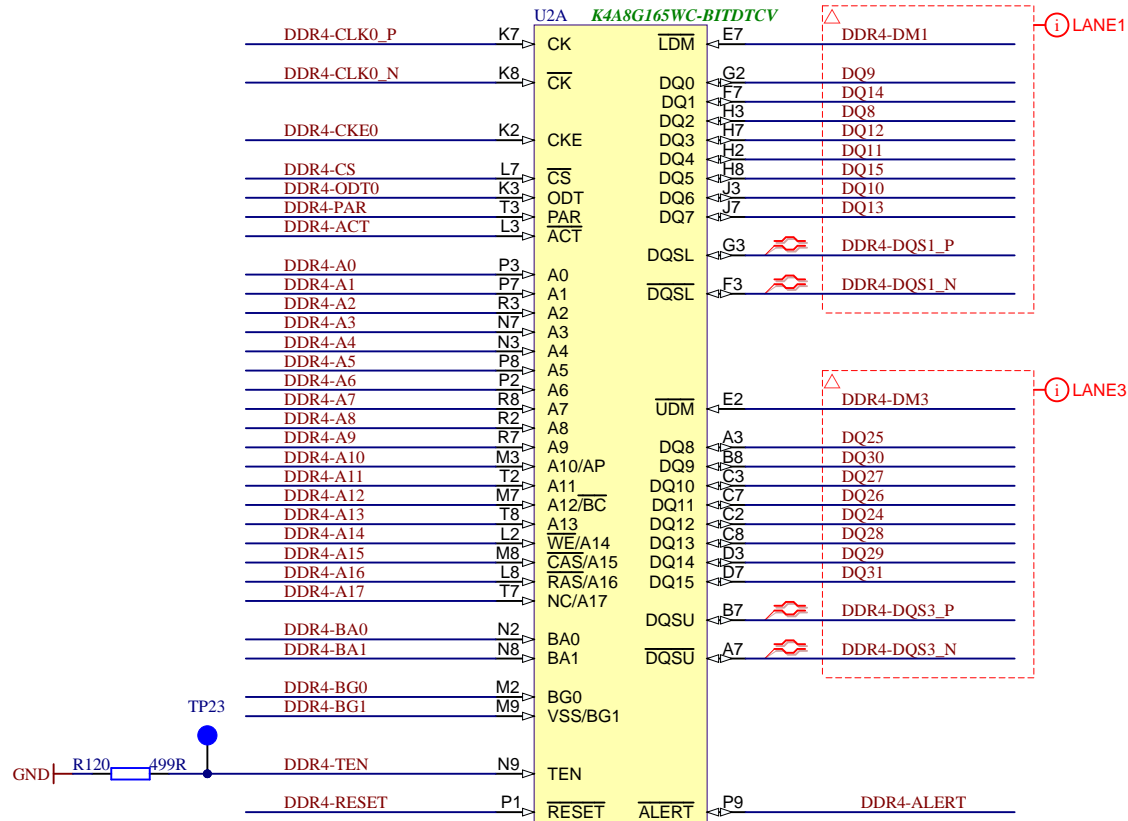
Title: TE0818 - Config		
A4	Number: TE0818 9BE81-A	Rev. 02
Date: 09.10.2023	Copyright: Trenz Electronic GmbH	Page 19 of 31
Filename: CONFIG.SchDoc		

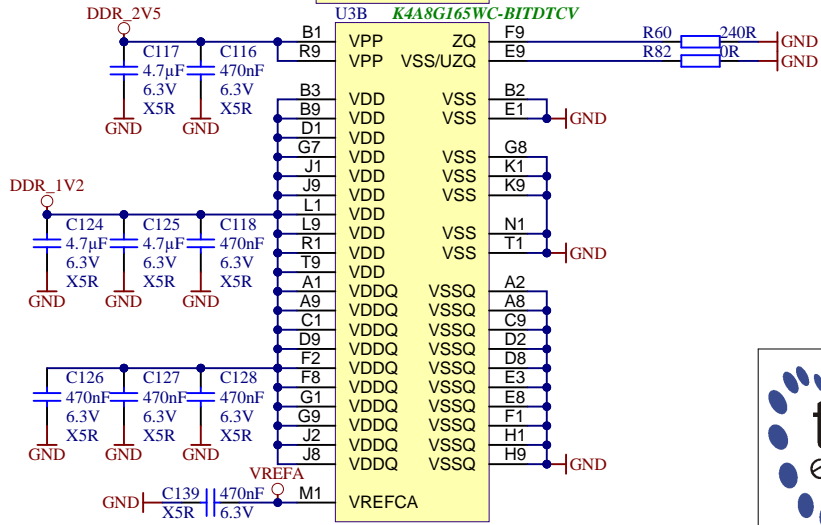
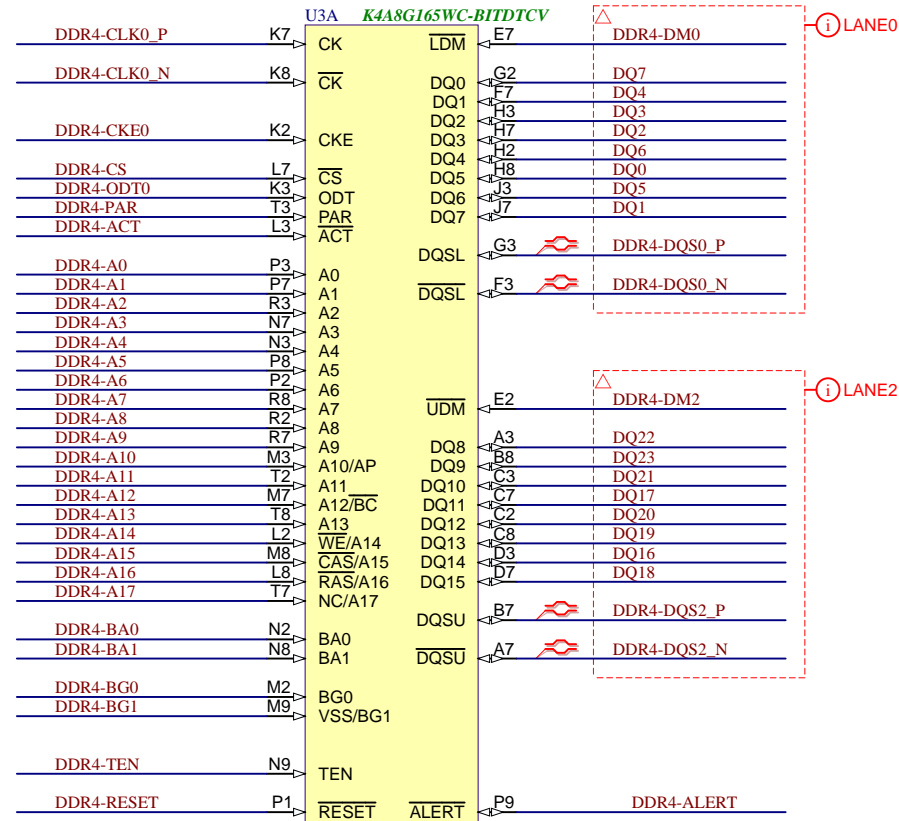
Title: TE0818 - PS Power		
A4	Number: TE0818 9BE81-A	Rev. 02
Date: 09.10.2023	Copyright: Trenz Electronic GmbH	Page 20 of 31
Filename: ZU_PS_POWER.SchDoc		



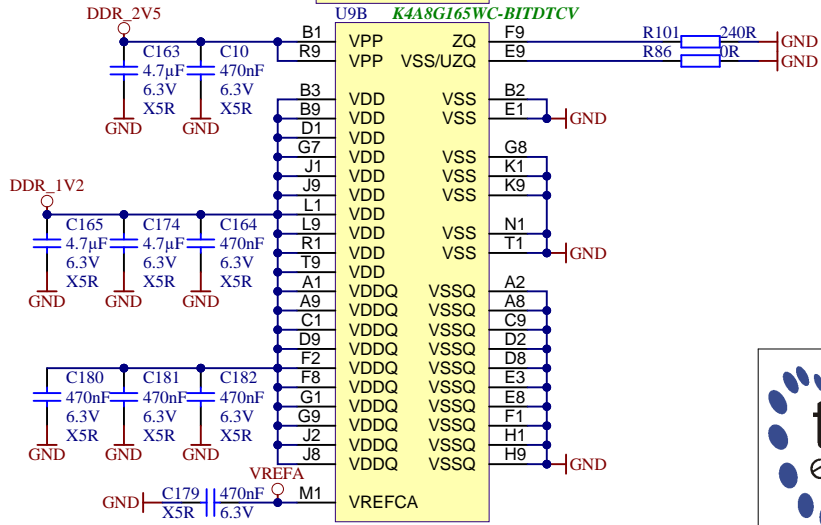
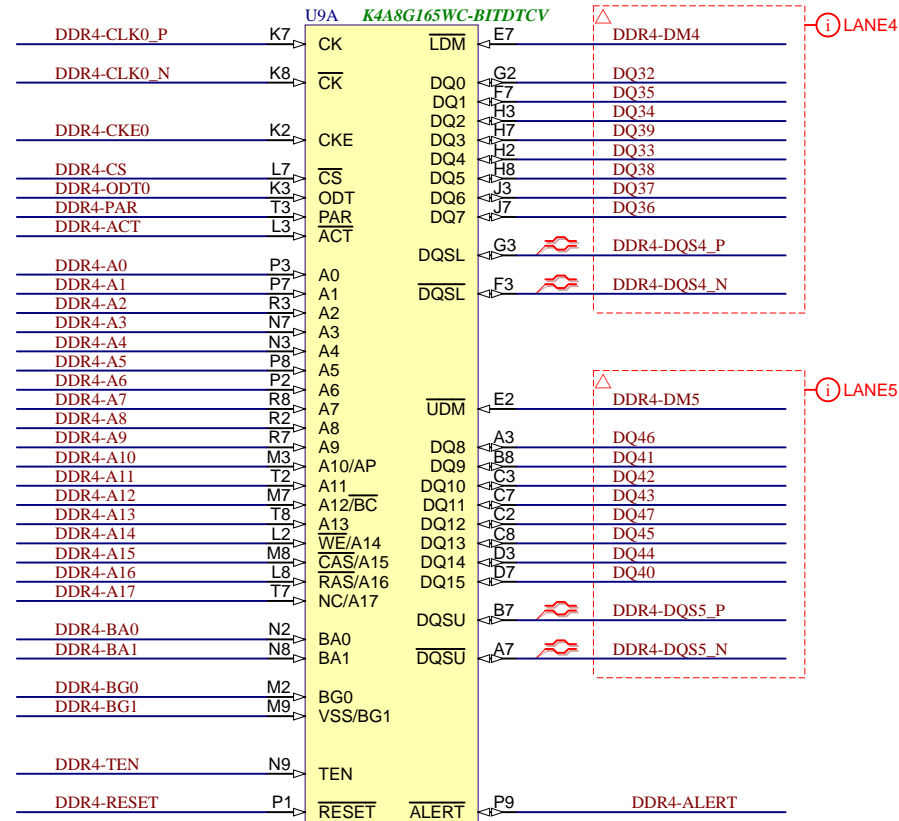
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A4	Number: TE0818 9BE81-A	Rev. 02
Date: 09.10.2023	Copyright: Trenz Electronic GmbH	Page 21 of 31
Filename: ZU_POWER.SchDoc		



Title: TE0818 - DDR4 RAM 1		
A4	Number: TE0818 9BE81-A	Rev. 02
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Filename: DDR4-RAM.SchDoc		

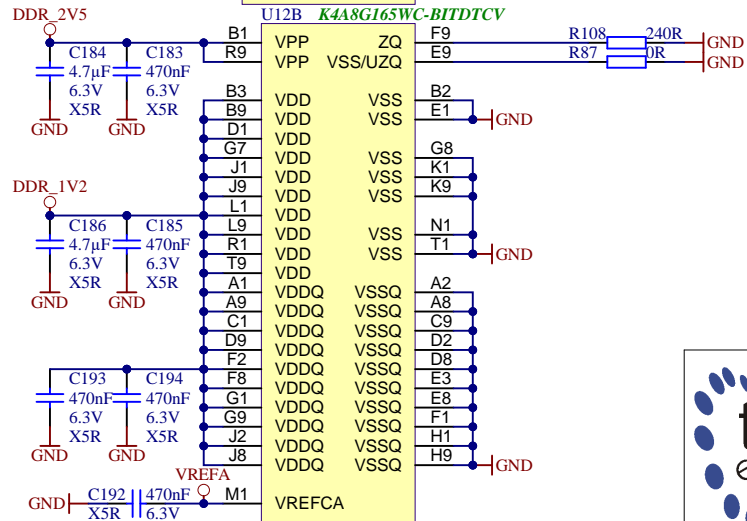
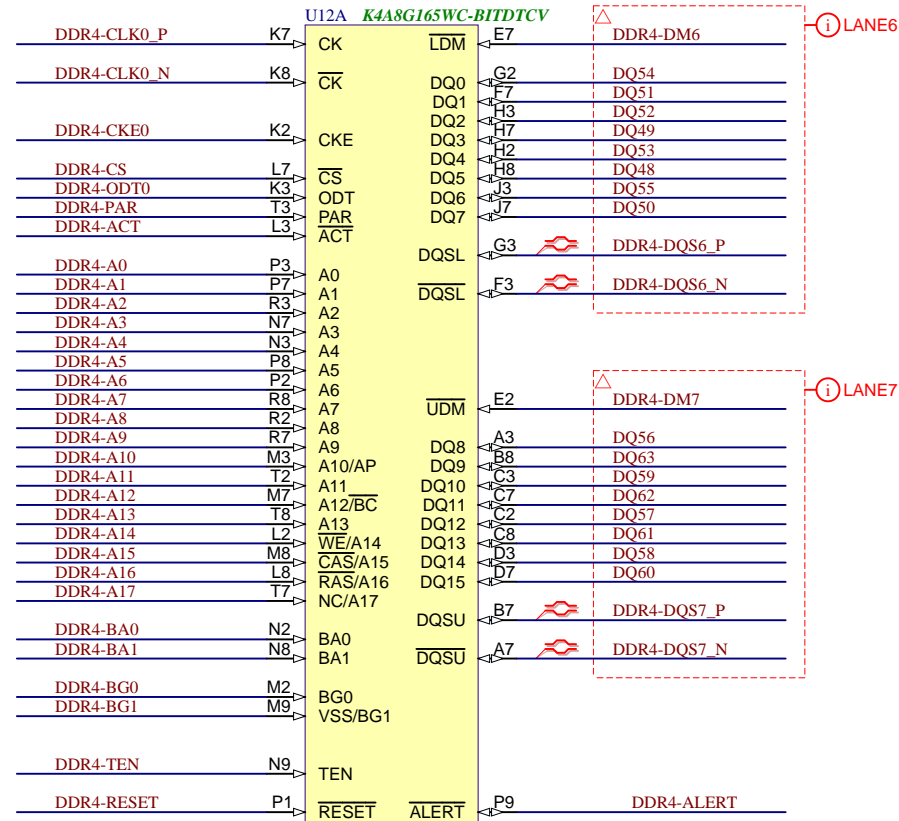


Title: TE0818 - DDR4 RAM 2		
A4	Number: TE0818 9BE81-A	Rev. 02
Date: 09.10.2023	Copyright: Trenz Electronic GmbH	Page 23 of 31
Filename: DDR4-RAM_2.SchDoc		

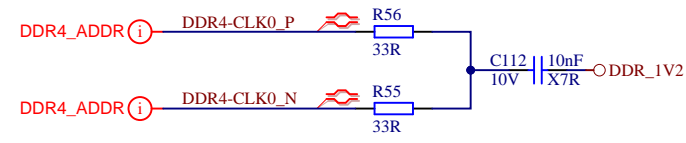
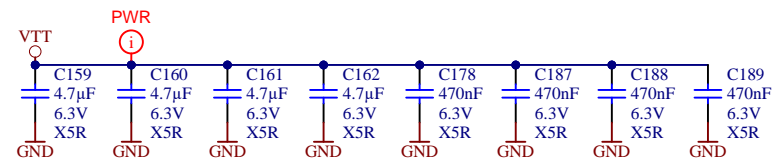
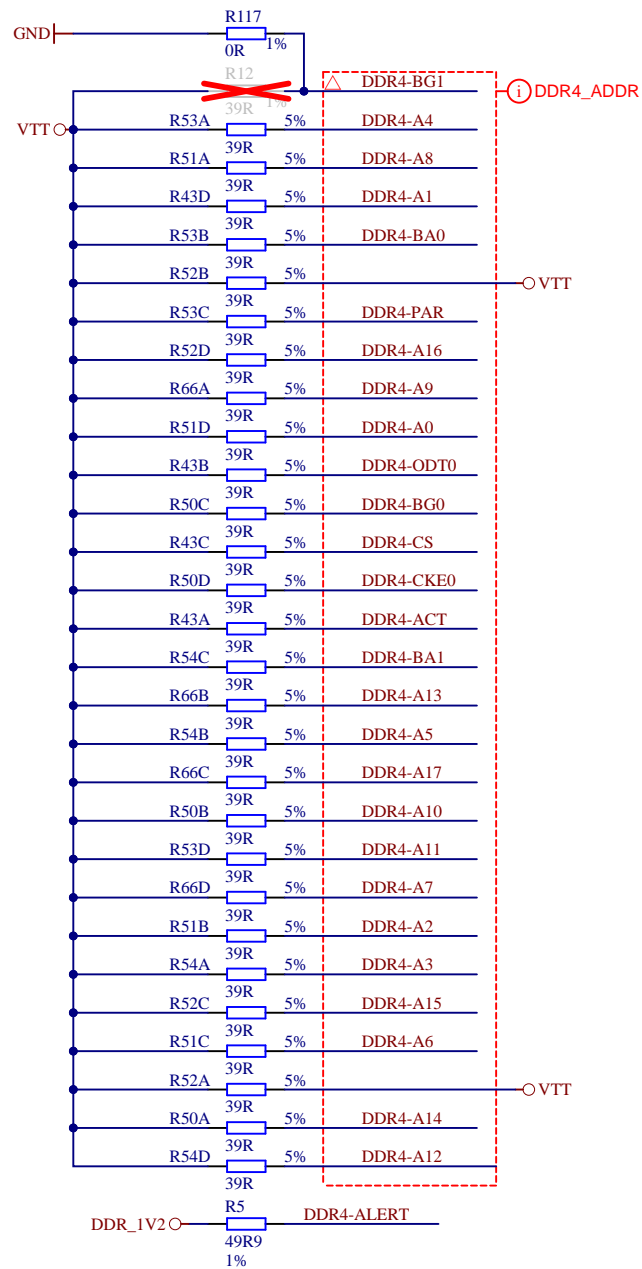


Title: TE0818 - DDR4 RAM 3		
A4	Number: TE0818 9BE81-A	Rev. 02
Date: 09.10.2023	Copyright: Trenz Electronic GmbH	Page 24 of 31
Filename: DDR4-RAM_3.SchDoc		

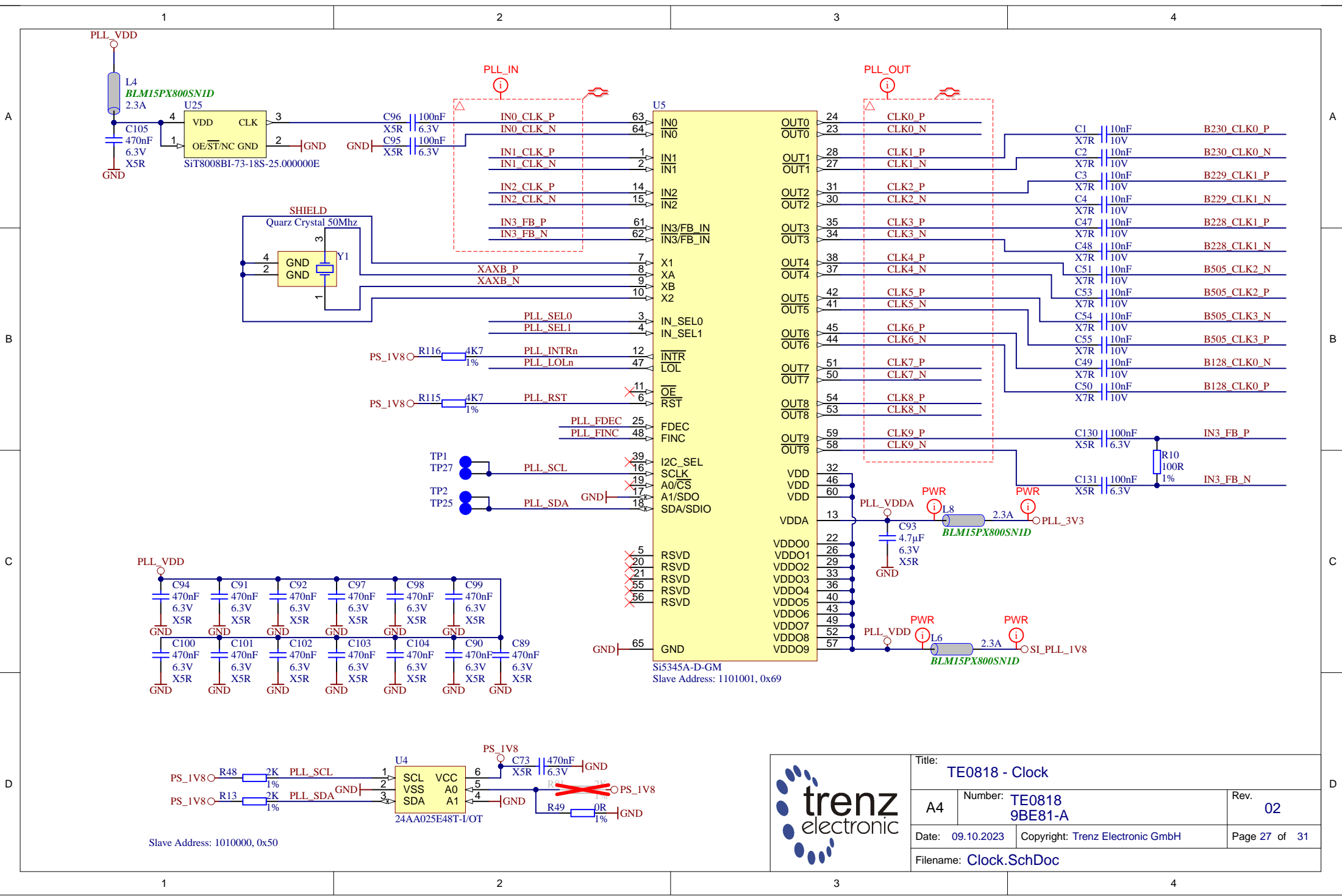




Title: TE0818 - DDR4 RAM 4		
A4	Number: TE0818 9BE81-A	Rev. 02
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Filename: DDR4-RAM_4.SchDoc		



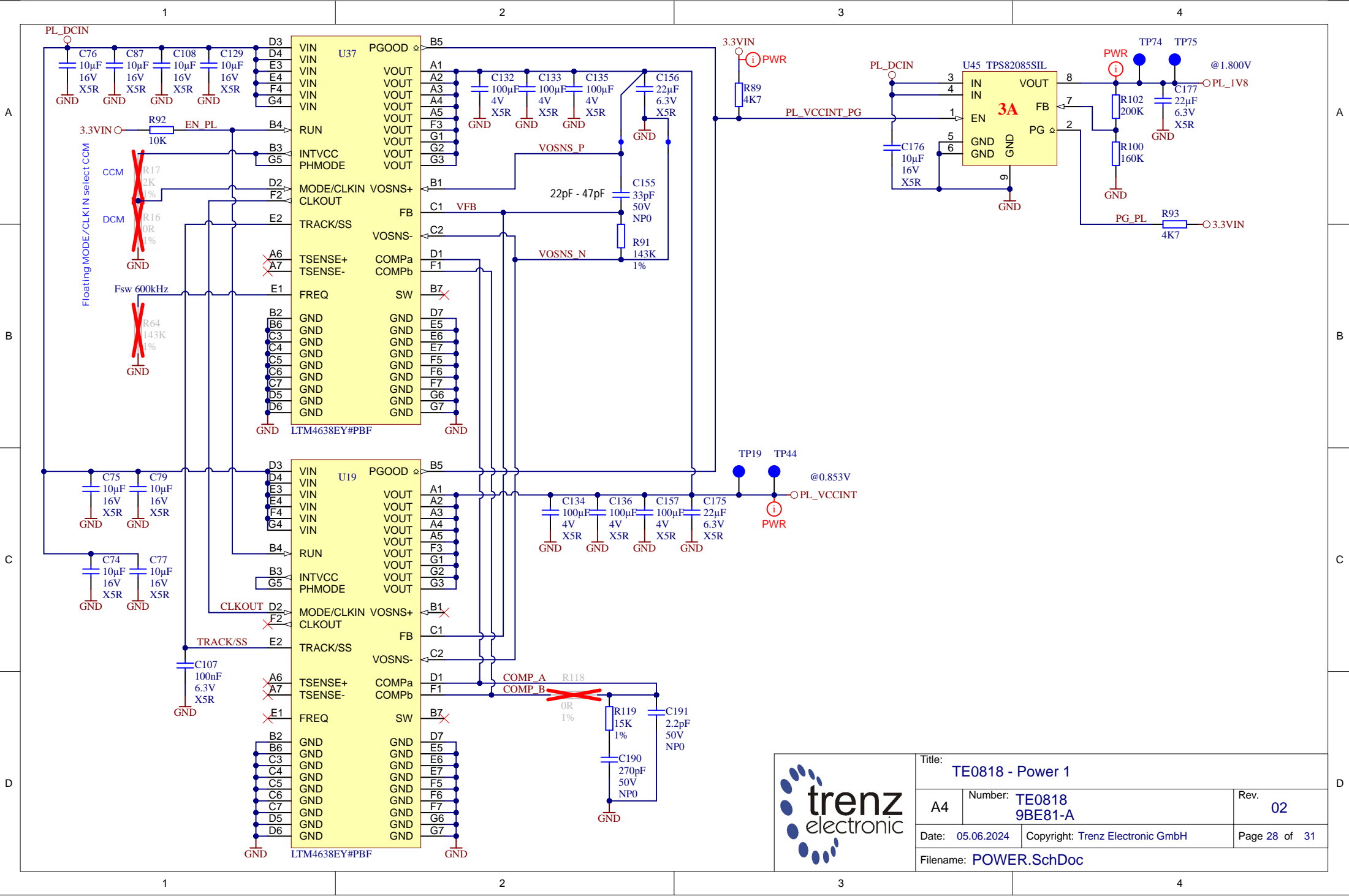
Title: TE0818 - DDR4 Termination		
A4	Number: TE0818 9BE81-A	Rev. 02
Date: 09.10.2023	Copyright: Trenz Electronic GmbH	Page 26 of 31
Filename: DDR4-TERM.SchDoc		



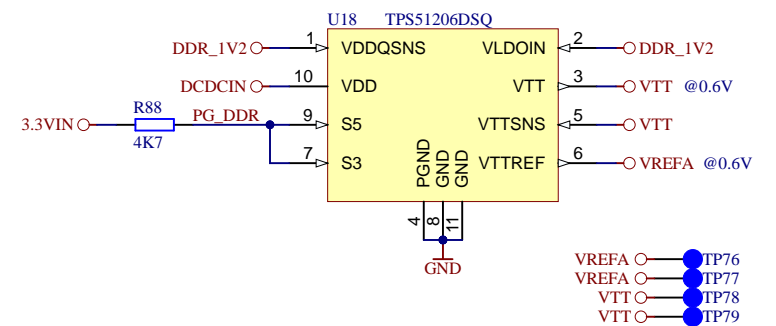
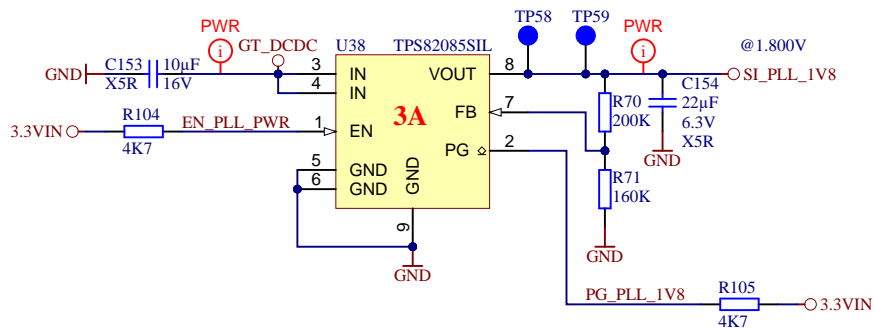
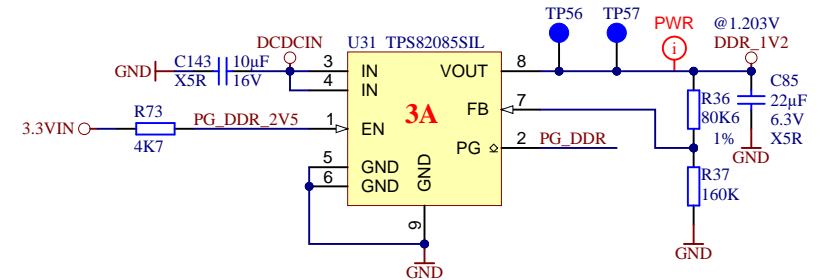
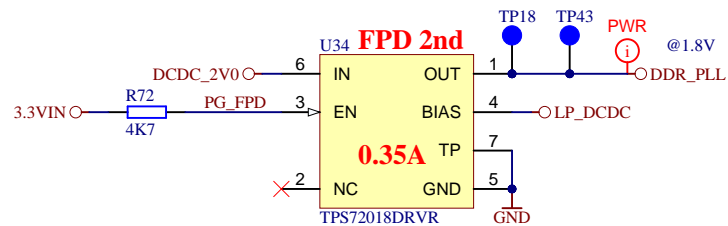
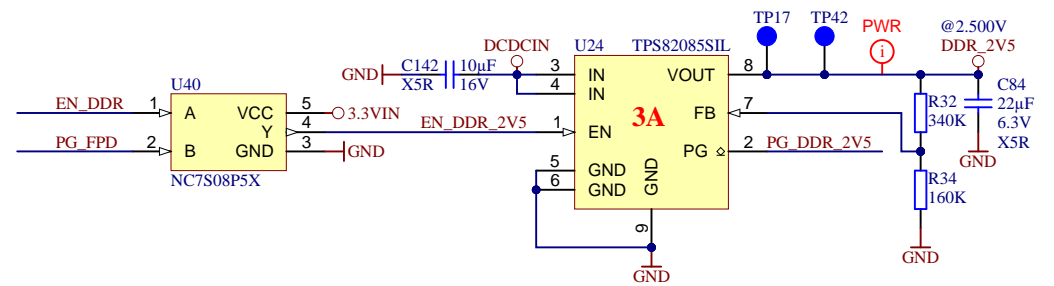
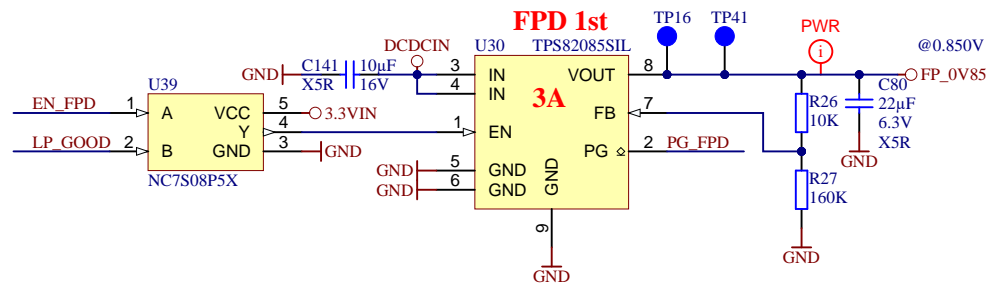
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Title: TE0818 - Clock		
A4	Number: TE0818 9BE81-A	Rev. 02
Date: 09.10.2023	Copyright: Trenz Electronic GmbH	Page 27 of 31
Filename: Clock.SchDoc		



Title: TE0818 - Power 1		
A4	Number: TE0818 9BE81-A	Rev. 02
Date: 05.06.2024	Copyright: Trenz Electronic GmbH	Page 28 of 31
Filename: POWER.SchDoc		



**1** **2** **3** **4**

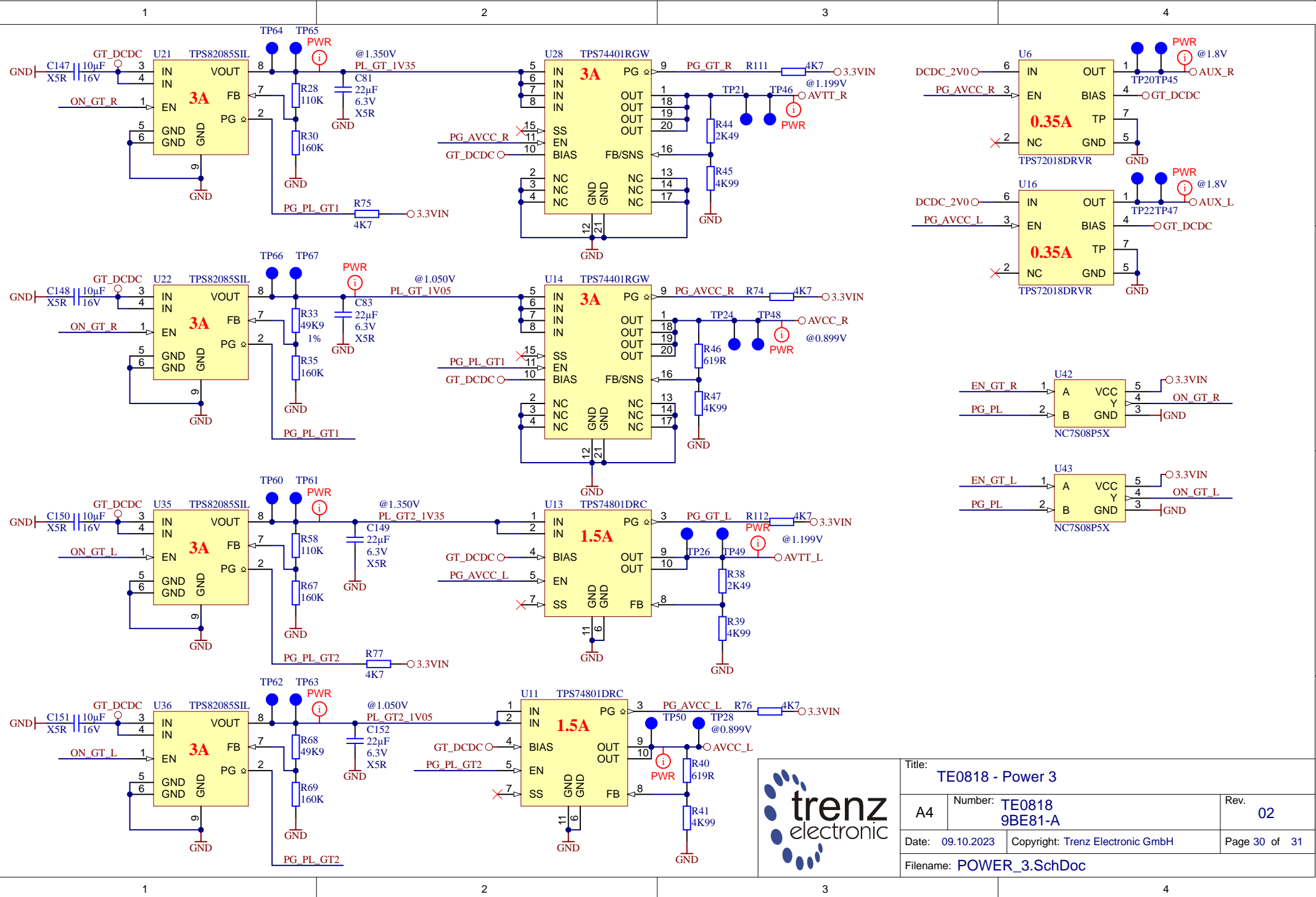
**trenz electronic**

Title: **TE0818 - Power 2**

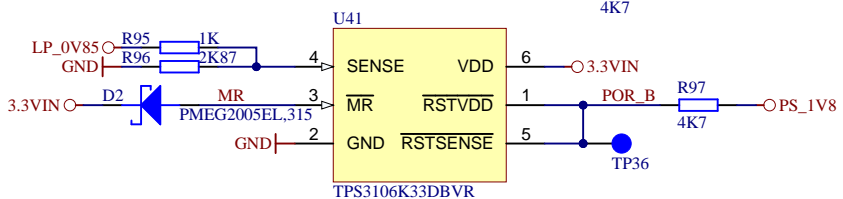
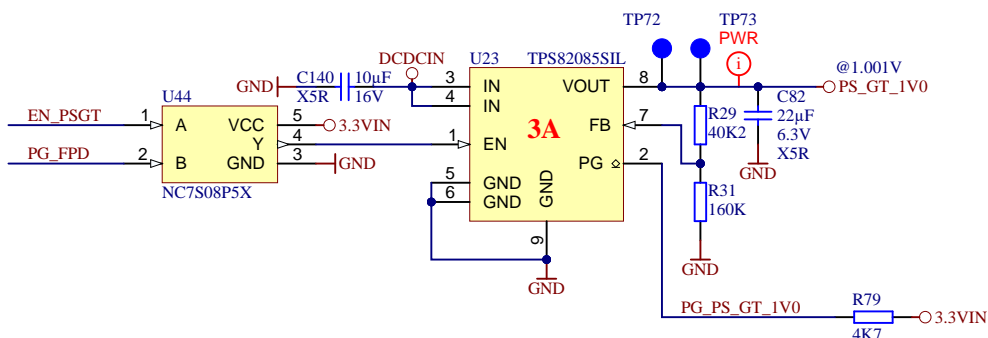
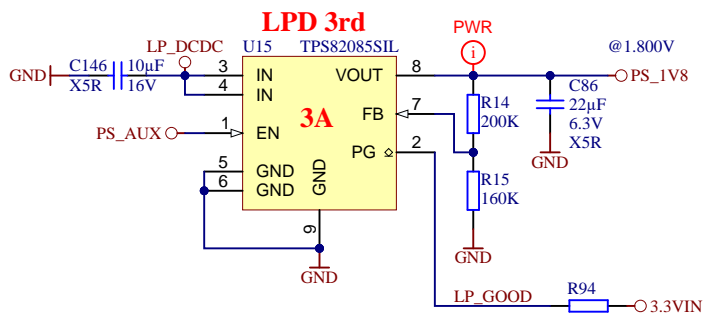
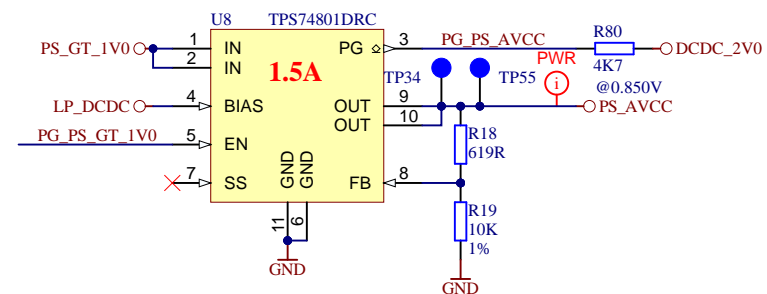
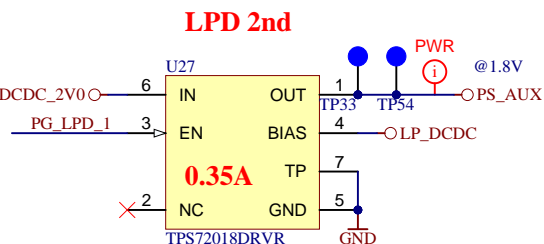
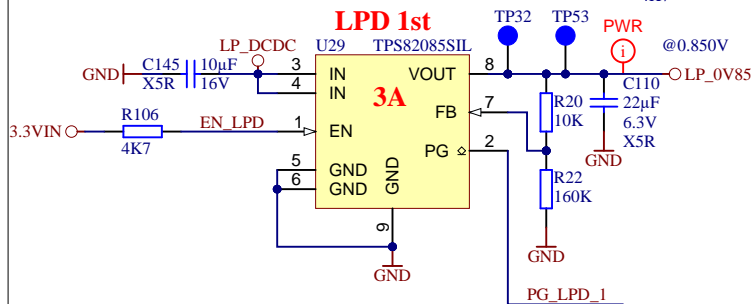
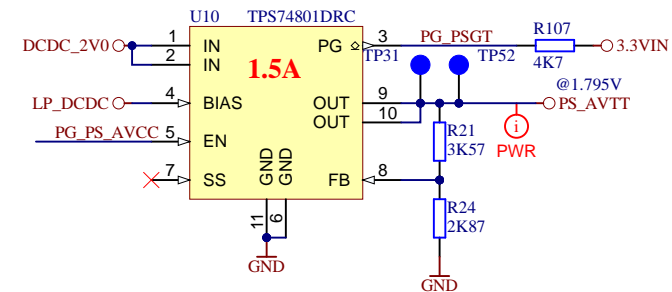
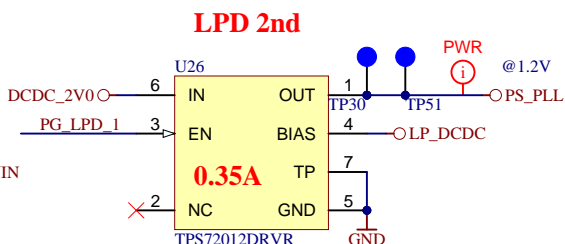
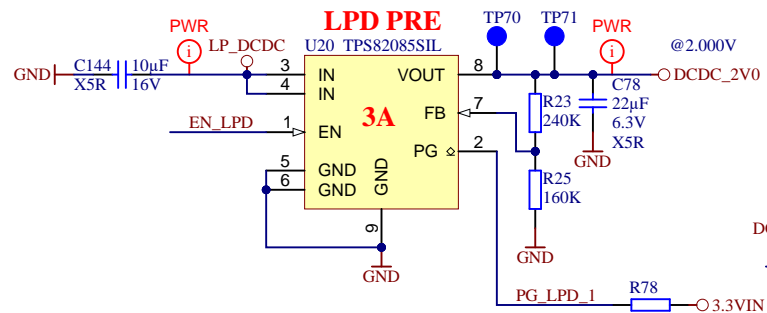
A4 Number: **TE0818 9BE81-A** Rev. **02**

Date: **09.10.2023** Copyright: **Trenz Electronic GmbH** Page **29** of **31**

Filename: **POWER\_2.SchDoc**



Title: TE0818 - Power 3		
A4	Number: TE0818 9BE81-A	Rev. 02
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Net Name	Voltage Rail	Low Detect
LP_OV85	0.85 V	0.743 V
3.3VIN	3.3 V	2.941 V

Title: **TE0818 - Power 4**

A4	Number: <b>TE0818 9BE81-A</b>	Rev. <b>02</b>
Date: 09.10.2023	Copyright: Trenz Electronic GmbH	
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Filename: **POWER\_4.SchDoc**