



TE0818 Test Board

Revision v.11

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<https://wiki.trenz-electronic.de/display/PD/TE0818+Test+Board>

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4 Overview

Design Example with minimum PS Setup (DDR, QSPI, UART0) only for custom boards or easier debug via Vitis.

Refer to <http://trenz.org/te0818-info> for the current online version of this manual and other available documentation.

4.1 Key Features

- Vitis/Vivado 2022.2
- QSPI
- Custom Carrier (minimum PS Design with available module components only)
- Modified FSBL (some additional outputs only)

4.2 Revision History

Expand List

Date	Vivado	Project Built	Authors	Description
2023-08-15	2022.2	TE0818-test_board-vivado_2022.2-build_6_20230815120606.zip TE0818-test_board_noprebuilt-vivado_2022.2-build_6_20230815120606.zip	Manuela Strücker	<ul style="list-style-type: none"> • new assembly variants
2023-06-14	2022.2	TE0818-test_board-vivado_2022.2-build_1_20230614114433.zip TE0818-test_board_noprebuilt-vivado_2022.2-build_1_20230614114433.zip	Manuela Strücker	<ul style="list-style-type: none"> • 2022.2 release • new assembly variants
2023-02-14	2021.2.1	TE0818-test_board-vivado_2021.2-build_20_20230214132934.zip TE0818-	Manuela Strücker	<ul style="list-style-type: none"> • new assembly variants

Date	Vivado	Project Built	Authors	Description
		test_board_noprebuilt -vivado_2021.2- build_20_20230214132 934.zip		
2022-09-12	2021.2.1	TE0818-test_board- vivado_2021.2- build_15_20220912092 602.zip TE0818- test_board_noprebuilt -vivado_2021.2- build_15_20220912092 602.zip	Manuela Strücker	<ul style="list-style-type: none"> • update board part file compatible to Vivado 2021.2.1
2022-05-12	2021.2	TE0818-test_board- vivado_2021.2- build_14_20220512120 419.zip TE0818- test_board_noprebuilt -vivado_2021.2- build_14_20220512120 419.zip	Manuela Strücker	<ul style="list-style-type: none"> • new assembly variants
2022-03-10	2021.2	TE0818-test_board- vivado_2021.2- build_11_20220309105 635.zip TE0818- test_board_noprebuilt -vivado_2021.2- build_11_20220309105 635.zip	Manuela Strücker	<ul style="list-style-type: none"> • update fsbl (switch channel of I2C switch@77)
2022-02-03	2021.2	TE0818-test_board- vivado_2021.2- build_11_20220203082 339.zip TE0818- test_board_noprebuilt -vivado_2021.2-	John Hartfiel	<ul style="list-style-type: none"> • initial release

Date	Vivado	Project Built	Authors	Description
		build_11_20220203082339.zip		

Table 1: Design Revision History

4.3 Release Notes and Known Issues

Issues	Description	Workaround	To be fixed version
Xilinx Software	Incompatibility of board files for ZynqMP with eMMC activated between 2021.2 and 2021.2.1 patch, see Xilinx Forum Request ¹	use corresponding board files for the Vivado versions	--

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2022.2	needed, Vivado is included into Vitis installation

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).²

Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Expand List

¹ https://support.xilinx.com/s/feed/0D54U00005Wbon6SAB?language=en_US

² <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0818-01-9GI21-A*	9eg_2i_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-9BE21-A	9eg_1e_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-S001	6eg_1e_4gb	REV01	4GB	128MB	NA	NA	without PLL
TE0818-01-S002	9eg_2i_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-S003	9eg_2i_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-9BE21-AZ	9eg_1e_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-9GI21-AK	9eg_2i_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-BBE21-A	15eg_1e_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-BBE21-AZ	15eg_1e_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-9BI41-X	9eg_1i_8gb	REV01	8GB	128MB	NA	NA	NA
TE0818-01-T001K	15eg_1e_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-T002K	9eg_2i_4gb	REV01	4GB	128MB	NA	NA	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0818-01-9GI81-A	9eg_2i_4gb_D	REV01	4GB	128MB	NA	NA	NA
TE0818-01-BBE81-A	15eg_1e_4gb_D	REV01	4GB	128MB	NA	NA	NA
TE0818-01-9GI81-AK	9eg_2i_4gb_D	REV01	4GB	128MB	NA	NA	NA
TE0818-01-BBE81-AK	15eg_1e_4gb_D	REV01	4GB	128MB	NA	NA	NA

Table 4: Hardware Modules

*used as reference

Note: Design contains also Board Part Files for TE0818+TEBF0818 configuration, this board part files are not used for this reference design.

Design supports following carriers:

Carrier Model	Notes
TEBT0818	
TEBF0818*	

Table 5: Hardware Carrier

*used as reference

Additional HW Requirements:

Additional Hardware	Notes
---	---

Table 6: Additional Hardware

*used as reference

4.5 Content

For general structure and usage of the reference design, see [Project Delivery - AMD devices](#)³

4.5.1 Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

Table 7: Design sources

4.5.2 Additional Sources

Type	Location	Notes
---	---	---

Table 8: Additional design sources

4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File

³ <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+AMD+devices>

File	File-Extension	Description
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebuilt content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0818 "Test Board" Reference Design](https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0818/Reference_Design/2022.2/test_board)⁴

⁴ https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0818/Reference_Design/2022.2/test_board

5 Design Flow

! Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- [AMD Development Tools](#)⁵
- [Vivado Projects - TE Reference Design](#)⁶
- [Project Delivery](#).⁷

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also be executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)⁸

! **Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
-----Set design paths-----
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
-----
-----TE Reference Design-----
-----
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
-----
Select (ex.: '0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.

⁵ <https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDDevelopmentTools-XilinxSoftware-BasicUserGuides>

⁶ <https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design>

⁷ <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+AMD+devices>

⁸ <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+AMD+devices#ProjectDeliveryAMDdevices-Currentlylimitationsoffunctionality>

- optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_gui mode.cmd"



Note: Select correct one, see also [Vivado Board Part Flow](#)⁹

Important: Use Board Part Files, which **did not** end with *_tebf0818

4. Create hardware description file (.xsa file) and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "\prebuilt\hardware\")

```
\prebuilt\hardware\")">  
TE::hw_build_design -export_prebuilt
```



Using Vivado GUI is the same, except file export to prebuilt folder.

5. Generate Programming Files with Vitis

run on Vivado TCL (Script generates applications and bootable files, which are defined in "test_board\sw_lib\apps_list.csv")

```
TE::sw_run_vitis -all  
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start with TE  
Scripts on Vivado TCL)
```




TCL scripts generate also platform project, this must be done manually in case GUI is used. See [Vitis](#)¹⁰

⁹ <https://wiki.trenz-electronic.de/display/PD/Vivado+Board+Part+Flow>

¹⁰ <https://wiki.trenz-electronic.de/display/PD/Vitis>

6 Launch


6.1 Programming

 Check Module and Carrier TRMs for proper HW configuration before you try any design. Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: [Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging](#)¹¹

6.1.1 Get prebuilt boot binaries

1. Run `_create_win_setup.cmd/_create_linux_setup.sh` and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
 - a. Select assembly version
 - b. Validate selection
 - c. Select create and open delivery binary folder

 Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

6.1.2 QSPI-Boot mode

1. Connect **JTAG** and power on carrier with module
2. Set Boot Mode to **JTAG**
3. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

run on Vivado TCL (Script programs BOOT.bin on QSPI flash)

```
TE::pr_program_flash -swapp hello_te0818
```

4. Set Boot Mode to **QSPI-Boot**
 - Depends on Carrier, see carrier TRM.

6.1.3 SD-Boot mode

This does not work, because SD controller is not selected on PS.


6.1.4 JTAG

Load configuration and Application with Vitis Debugger into device

¹¹ <https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDDevelopmentTools-XilinxSoftwareProgrammingandDebugging>

6.2 Usage

1. Prepare HW like described on section [Programming \(see page 16\)](#)
2. Connect UART USB (most cases same as JTAG)
3. Select QSPI as Boot Mode

 Note: See TRM of the Carrier, which is used.

4. Power On PCB

boot process

1. Zynq Boot ROM loads FSBL from QSPI into OCM,
2. FSBL init PS, programs PL using the bitstream and loads Application into DDR,

7 System Design - Vivado

7.1 Block Design



Figure 1: Block Design

7.1.1 PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
UART0	MIO
SWDT0..1	
TTC0..3	

Table 10: PS Interfaces

7.2 Constraints

7.2.1 Basic module constraints

_i_bitgen.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]  
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

7.2.2 Design specific constrain

Not needed.

8 Software Design - Vitis

For Vitis project creation, follow instructions from:

[Vitis](#)¹²

8.1 Application

Template location: "<project folder>\sw_lib\sw_apps\"

8.1.1 zynqmp_fsbl

TE modified 2022.2 FSBL

General:

- Modified Files: xfsbl_main.c, xfsbl_hooks.h/.c, xfsbl_board.h/.c (search for 'TE Mod' on source code)
- Add Files: te_xfsbl_hooks.h/.c (for hooks and board)
- General Changes:
 - Display FSBL Banner and Device Name

8.1.2 hello_te0818

Hello TE0818 is a Xilinx Hello World example as endless loop instead of one console output.

¹² <https://wiki.trenz-electronic.de/display/PD/Vitis>

9 Additional Software

No additional software is needed.

10 App. A: Change History and Legal Notices

10.1 Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.


Date	Document Revision	Authors	Description
 2023-08-15	v.11 (see page 6)	Manuela Strücker ¹³	<ul style="list-style-type: none"> new assembly variants
2023-08-14	v.10	Manuela Strücker	<ul style="list-style-type: none"> 2022.2 release new assembly variants
2023-02-14	v.8	Manuela Strücker	<ul style="list-style-type: none"> new assembly variants
2022-09-12	v.7	Manuela Strücker	<ul style="list-style-type: none"> update board part file compatible to Vivado 2021.2.1
2022-09-06	v.6	Manuela Strücker	<ul style="list-style-type: none"> new assembly variant
2022-03-10	v.4	Manuela Strücker	<ul style="list-style-type: none"> update fsbl update chapter Design Flow update chapter QSPI-Boot mode
2022-02-03	v.2	John Hartfiel	<ul style="list-style-type: none"> initial release
--	all	John Hartfiel ¹⁴ , Manuela Strücker ¹⁵	--

Table 11: Document change history.

¹³ <https://wiki.trenz-electronic.de/display/~m.struecker>

¹⁴ <https://wiki.trenz-electronic.de/display/~j.hartfiel>

¹⁵ <https://wiki.trenz-electronic.de/display/~m.struecker>

10.2 Legal Notices

10.3 Data Privacy

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10.9 REACH, RoHS and WEEE

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Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

 2019-06-07

¹⁶ <http://guidance.echa.europa.eu/>

¹⁷ <https://echa.europa.eu/candidate-list-table>

¹⁸ <http://www.echa.europa.eu/>