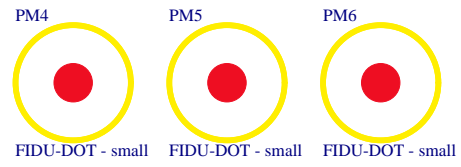
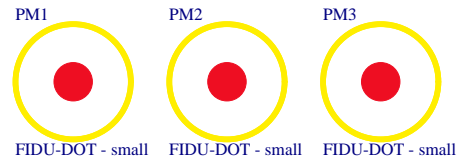
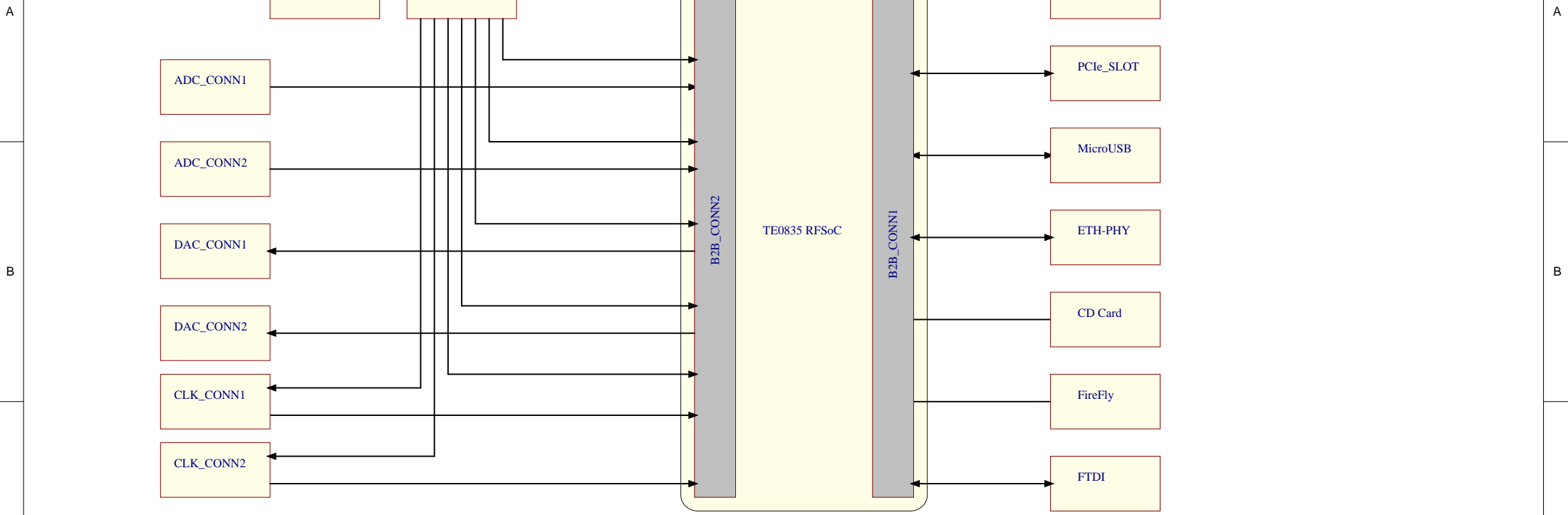


A

B

C

D



Serial1
Serial
Serialnumber 6,3 x 6.3mm

LOGO1
TE Logo PRINT Layer
LOGO PRINT

MISC1
Digilent Serialnumber
Digilent_SN

Regarding the usage of our schematics and alike documentation for Trenz module.

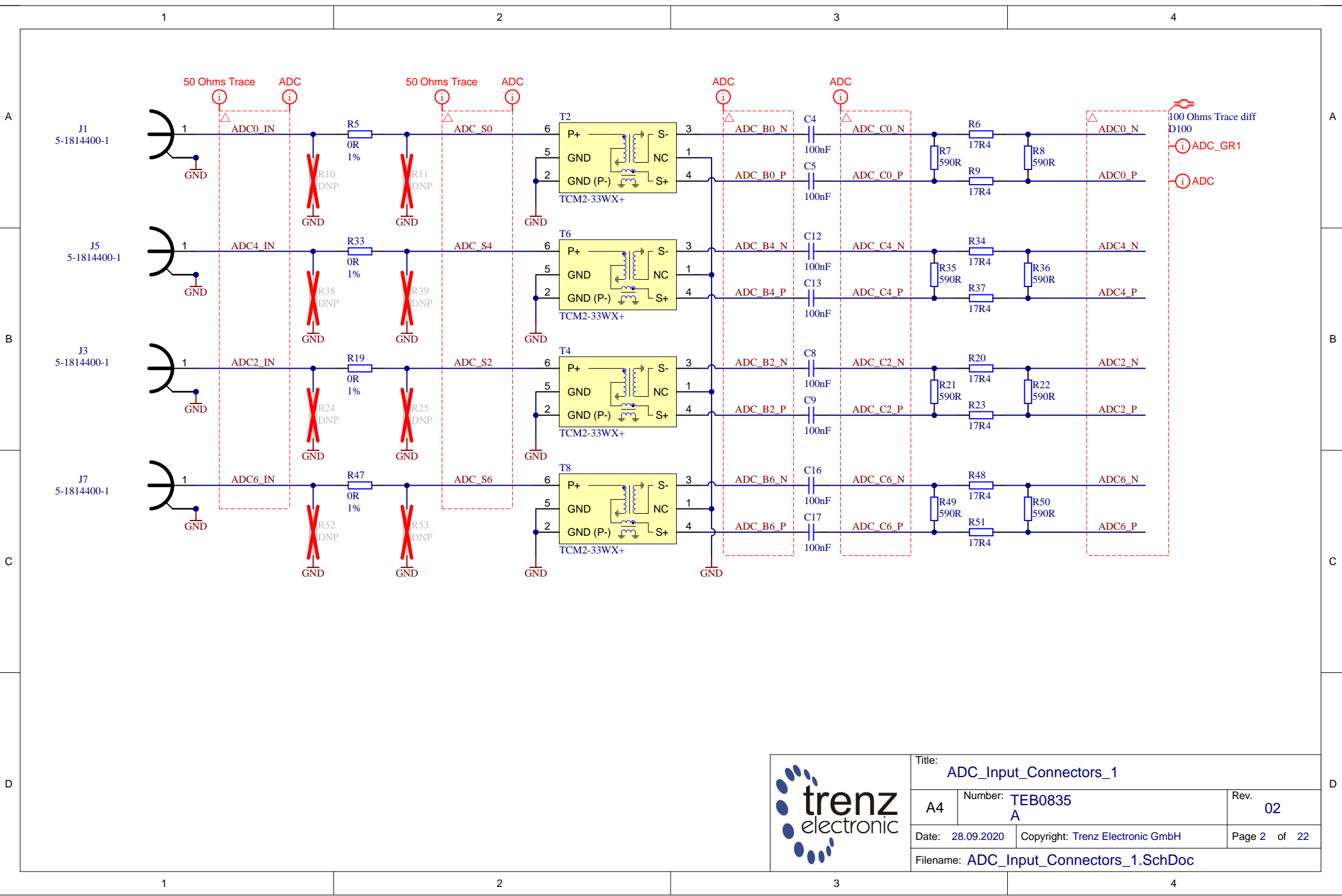
Modules are protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation of any of our modules, even if the design is just adapted or modified. All our modules are protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.


Schematics and other handouts serve for informational purposes only!

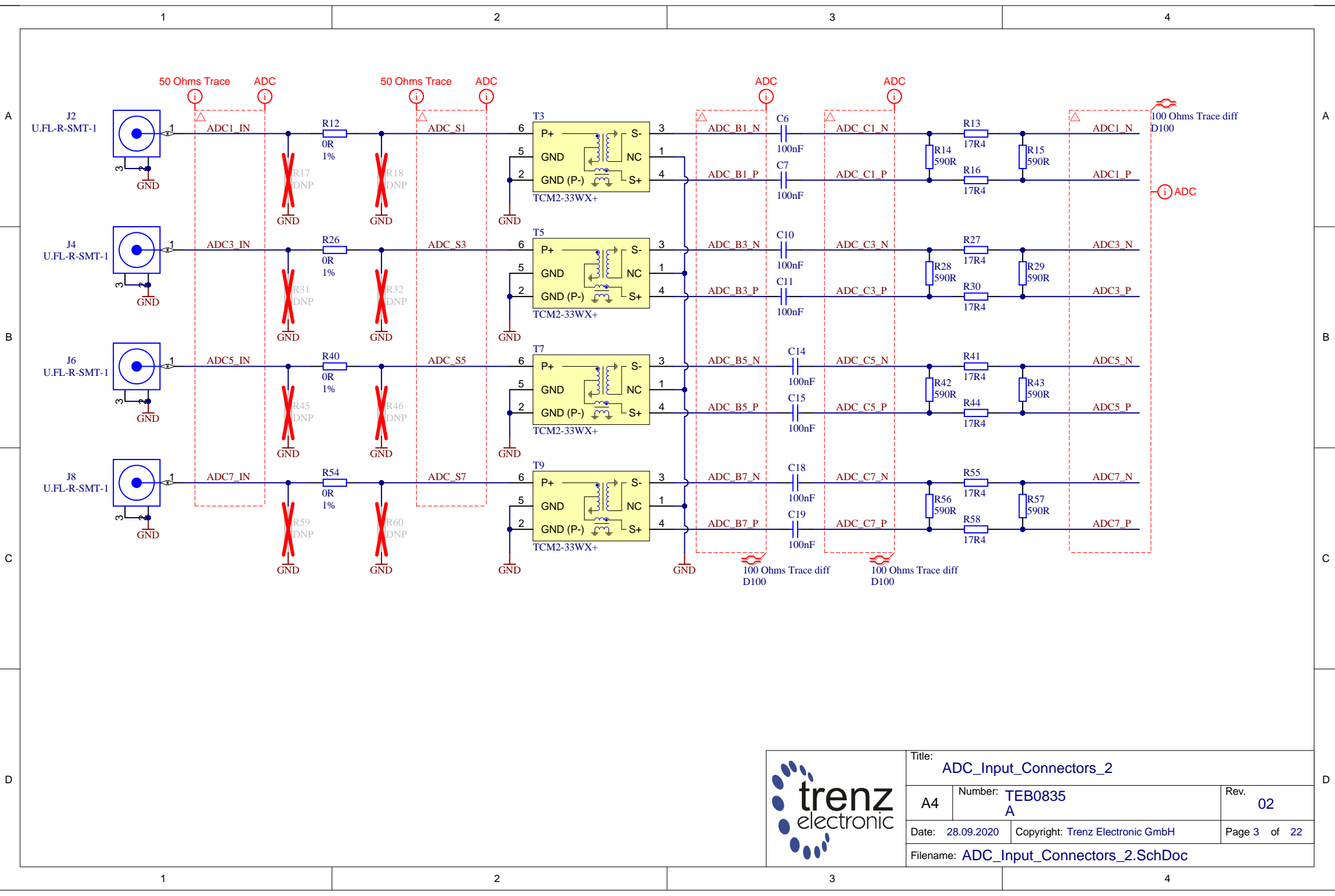
Design drawn by: IG
Checked by: MR
Assembly variant: A
Created by: IG
Modified by: IG
Modified at: 31.07.2020



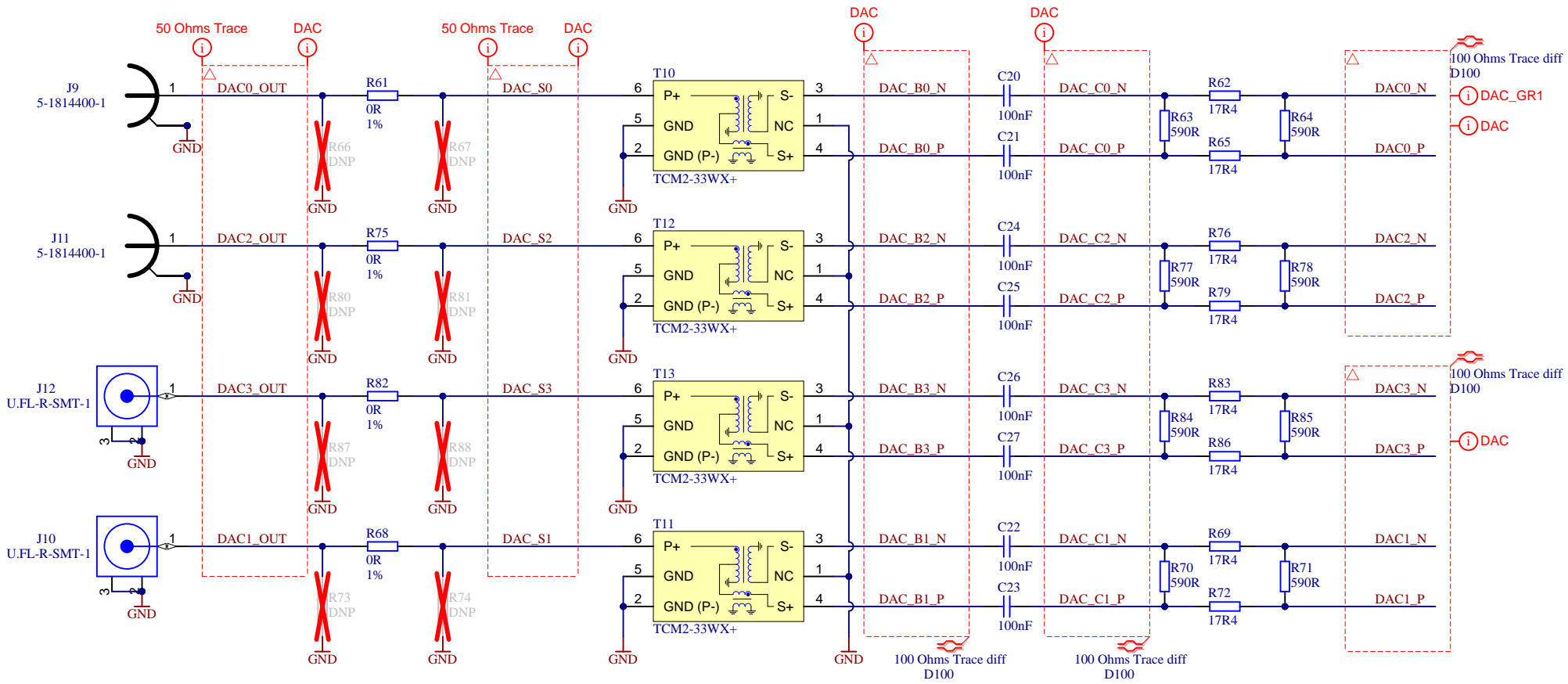
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A4	Number: TEB0835 A	Rev. 02
Date: 28.09.2020	Copyright: Trenz Electronic GmbH	Page 1 of 22
Filename: TEB0835.SchDoc		



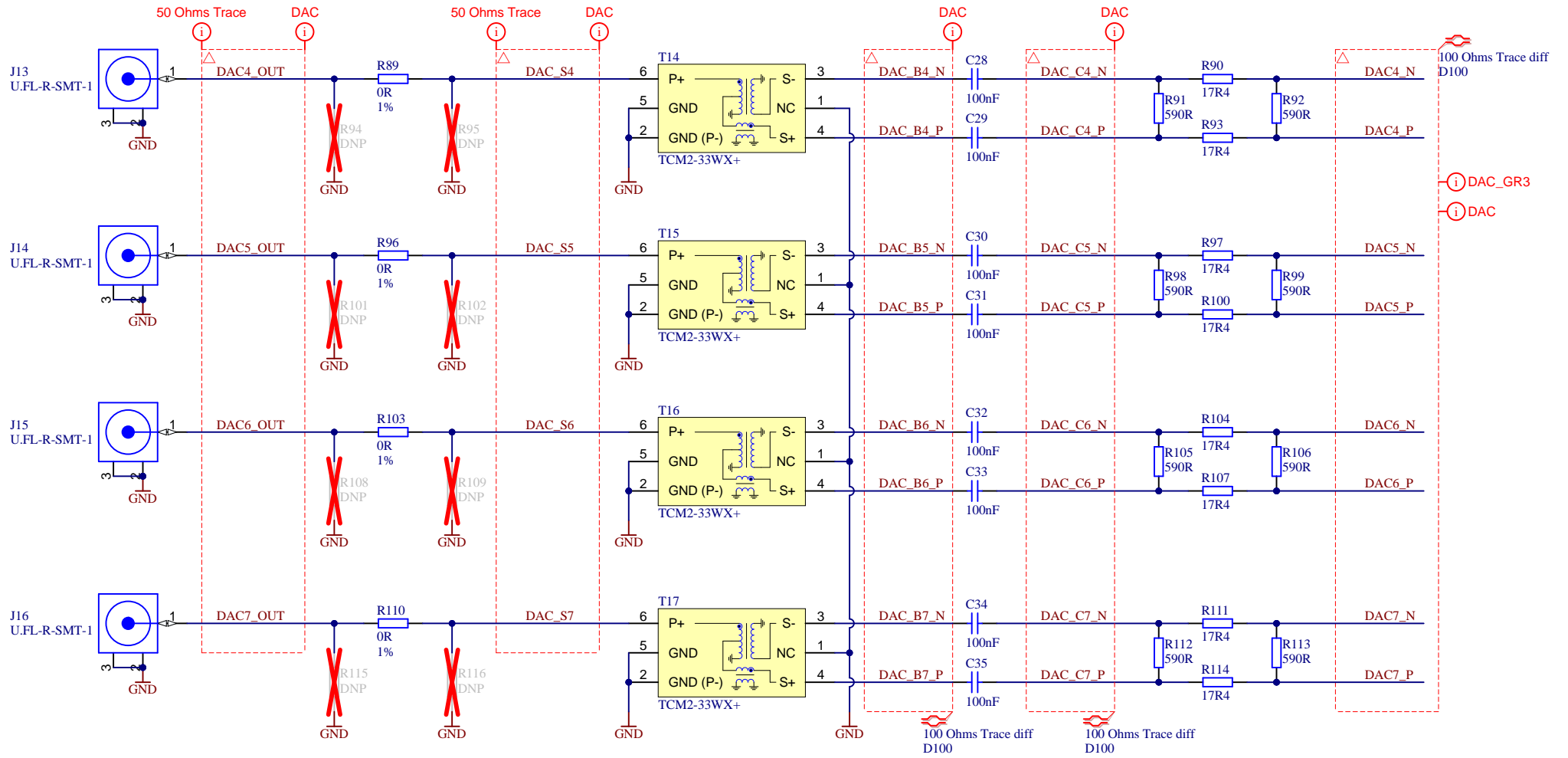
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Date: 28.09.2020		Copyright: Trenz Electronic GmbH		Page 2 of 22
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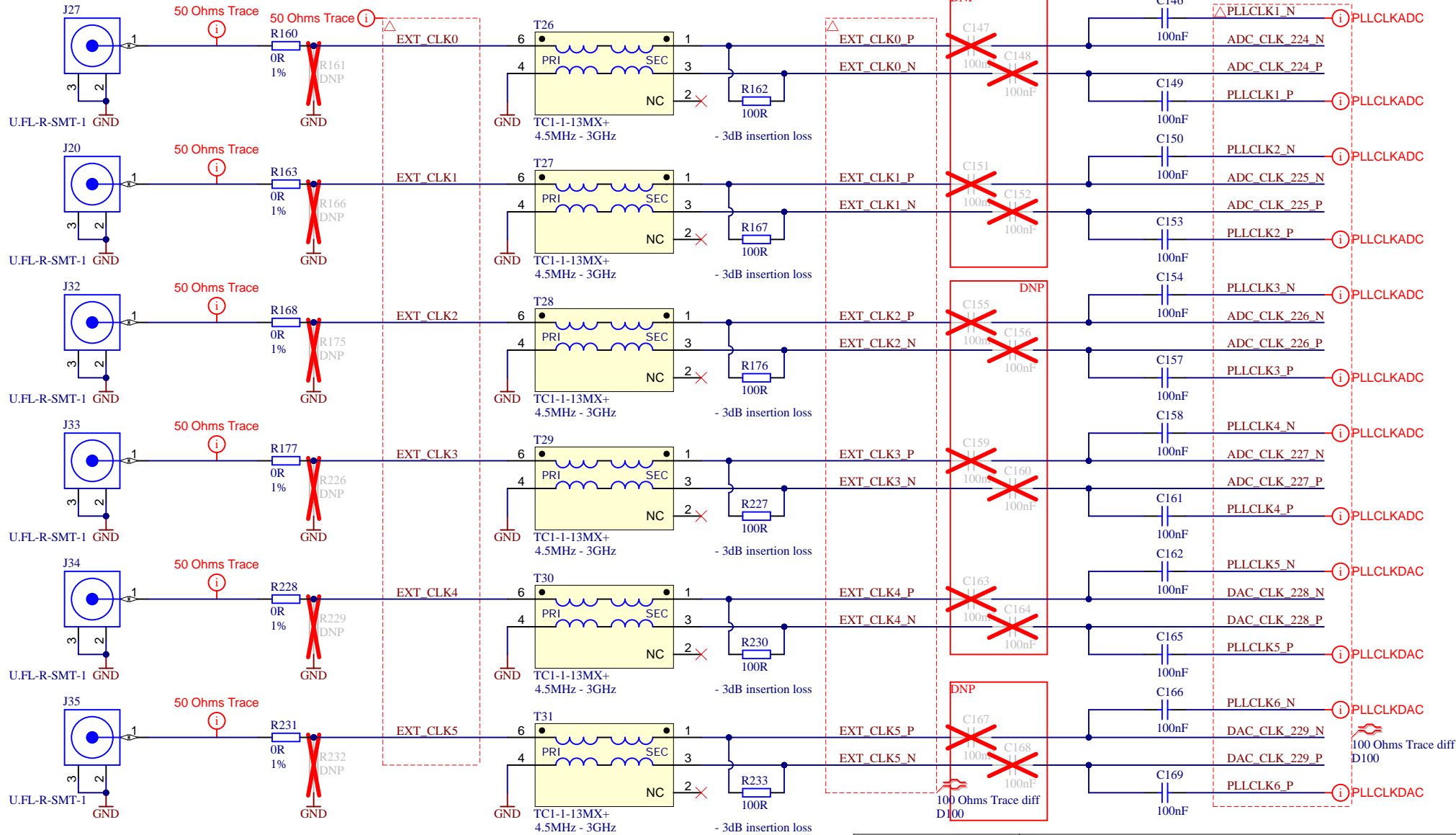
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Date: 28.09.2020	Copyright: Trenz Electronic GmbH	Page 3 of 22
Filename: ADC_Input_Connectors_2.SchDoc		



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A4	Number: TEB0835 A	Rev. 02
Date: 28.09.2020	Copyright: Trenz Electronic GmbH	Page 4 of 22
Filename: DAC_Output_Connectors_1.SchDoc		



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	Date: 28.09.2020	Copyright: Trenz Electronic GmbH	Page 5 of 22
	Filename: DAC_Output_Connectors_2.SchDoc		



Title: DAC_Output_Connectors_2		
A4	Number: TEB0835 A	Rev. 02
Date: 09.01.2023	Copyright: Trenz Electronic GmbH	Page 6 of 22
Filename: CLK_Connectors_1.SchDoc		

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A

A

B

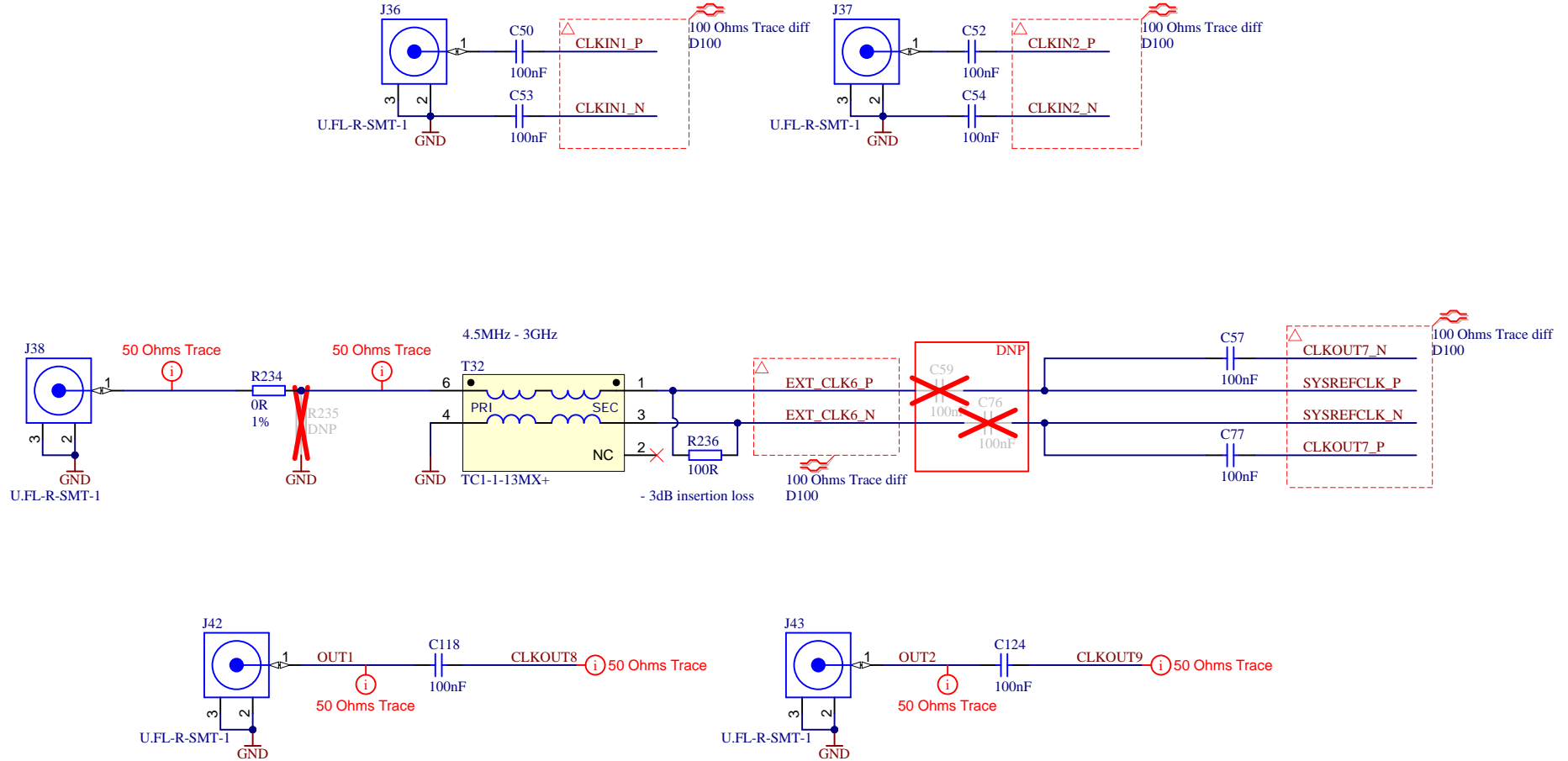
B

C

C

D

D



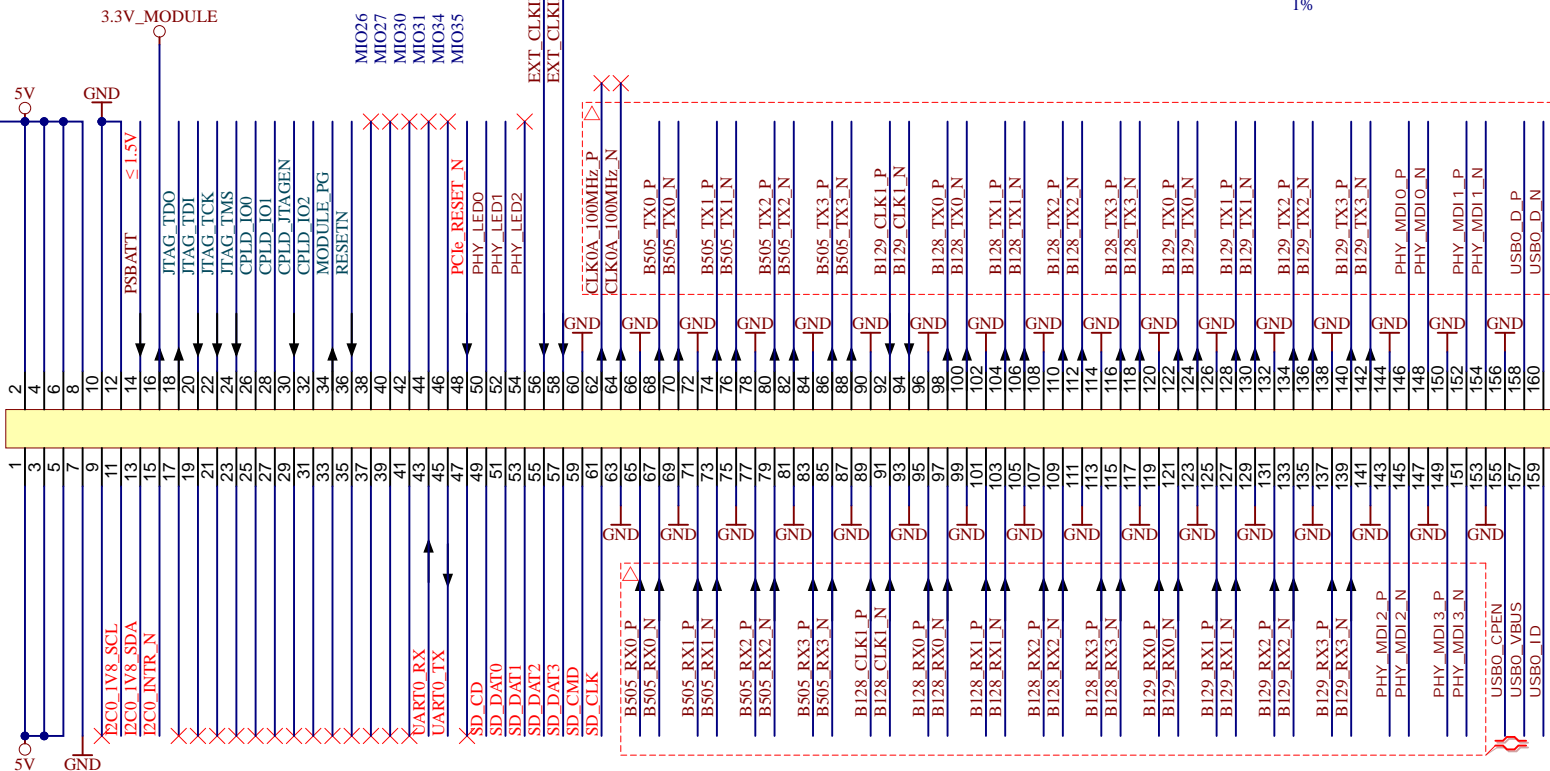
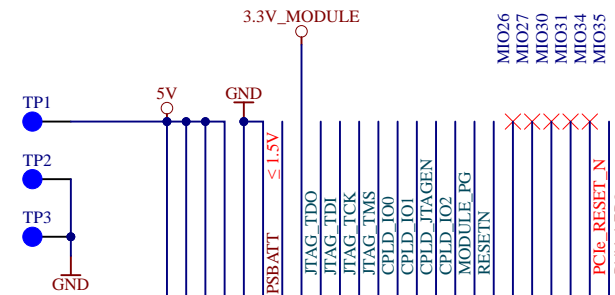
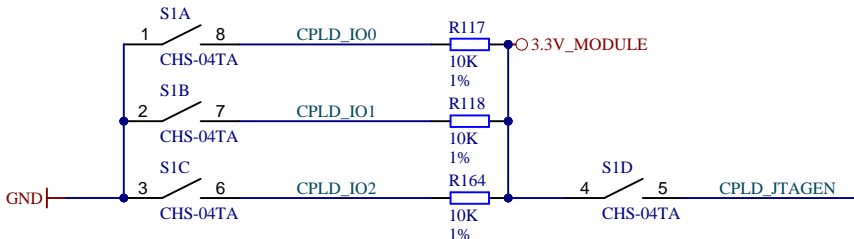
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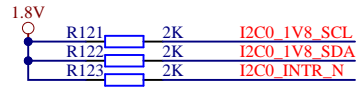
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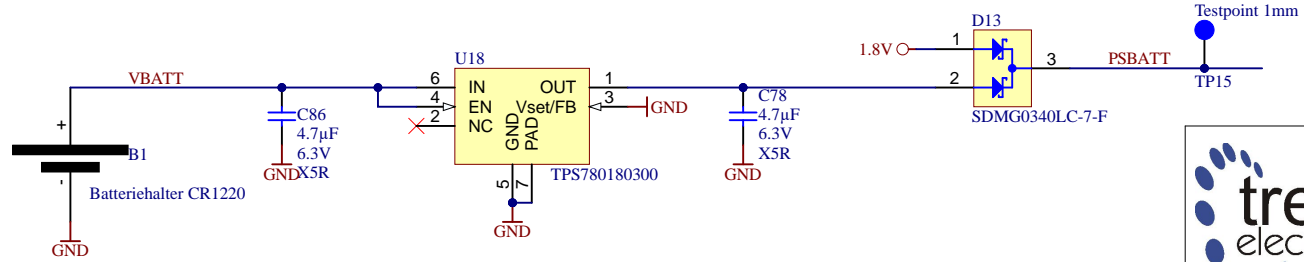
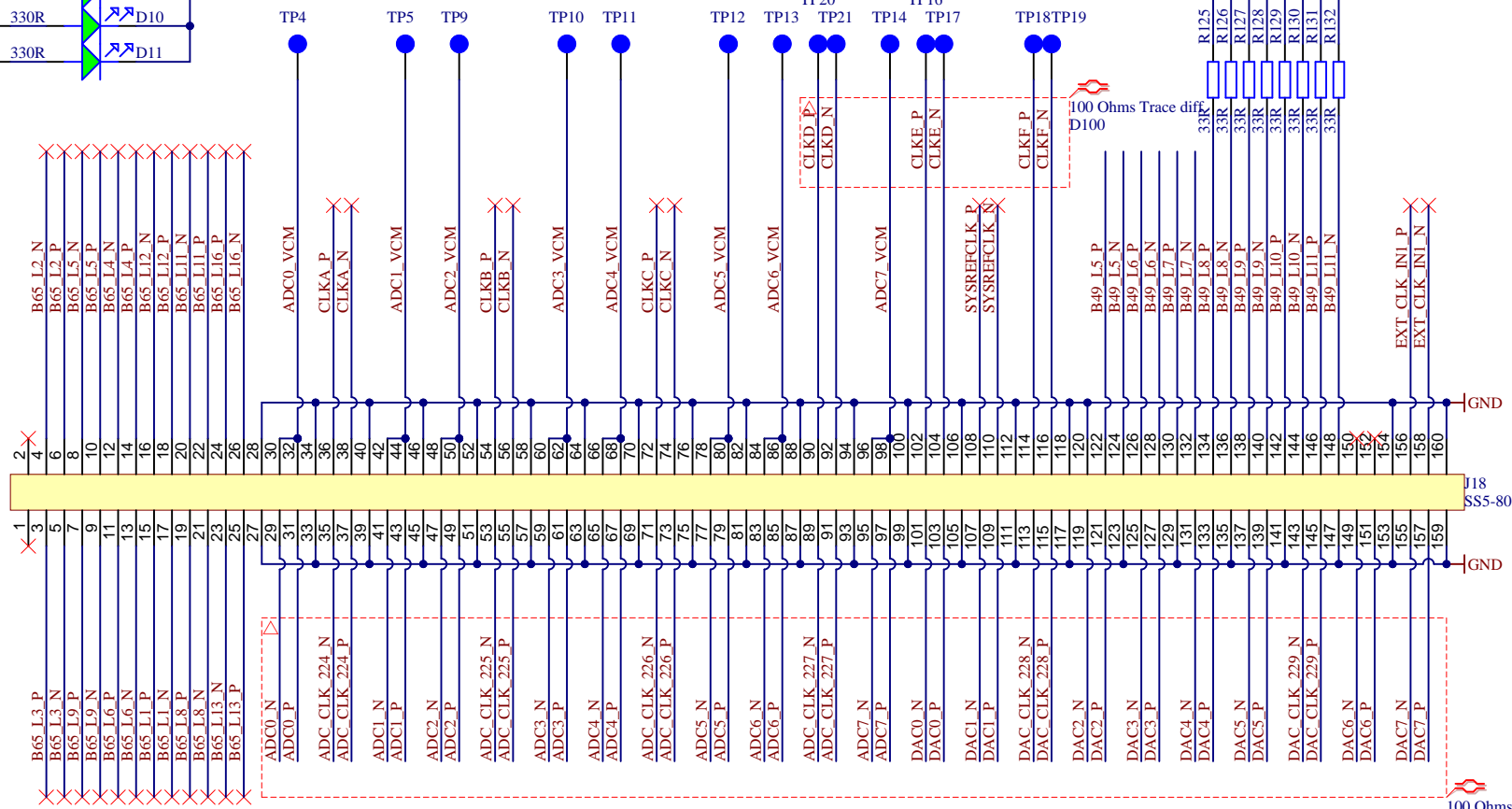
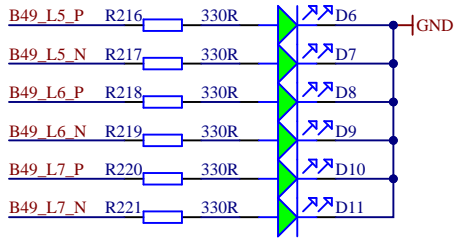
U17 SS5-80-3.00-L-D-K-TR

MIO14
MIO15
MIO16
MIO17
MIO18
MIO19
MIO20
MIO21
MIO22
MIO23
MIO24
MIO13/25
MIO38
MIO39
MIO40
MIO41
MIO42
MIO43
MIO44
MIO45
MIO46
MIO47
MIO48
MIO49
MIO50
MIO51

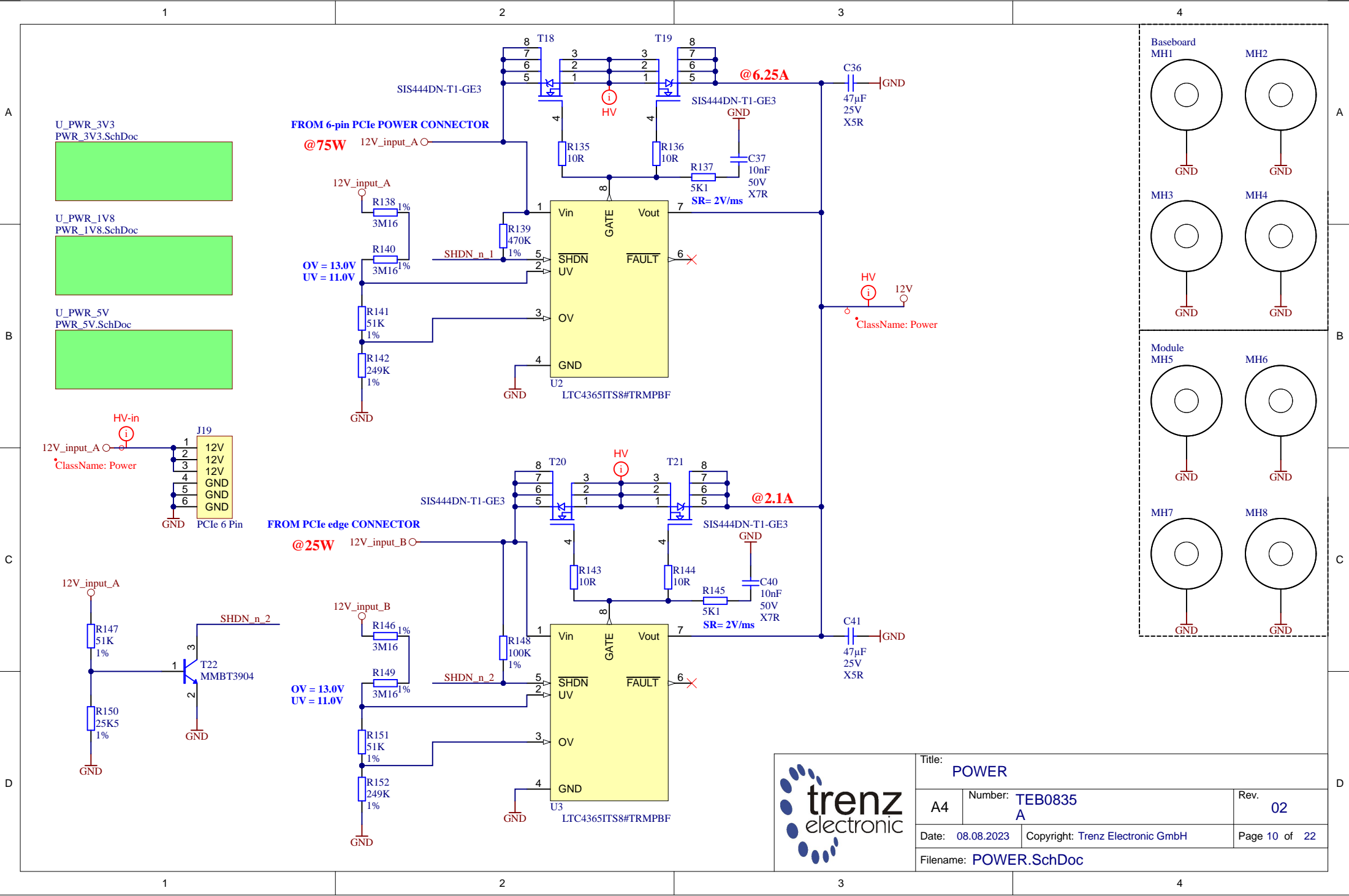
SD1
Slot Type SD2.0



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Date: 28.09.2020	Copyright: Trenz Electronic GmbH	Page 8 of 22
Filename: B2B_1.SchDoc		



Title: B2B_2		
A4	Number: TEB0835 A	Rev. 02
Date: 28.09.2020	Copyright: Trenz Electronic GmbH	Page 9 of 22
Filename: B2B_2.SchDoc		



Title: POWER		
A4	Number: TEB0835 A	Rev. 02
Date: 08.08.2023	Copyright: Trenz Electronic GmbH	
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A

A

B

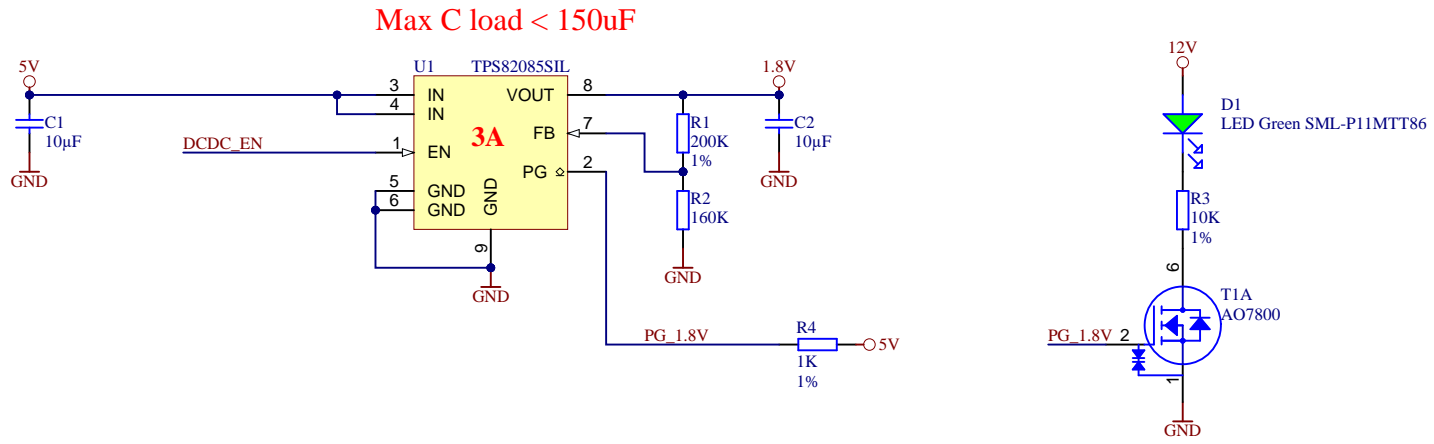
B


C

C

D

D



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	Date: 28.09.2020	Copyright: Trenz Electronic GmbH	
	Filename: PWR_1V8.SchDoc		Page 11 of 22

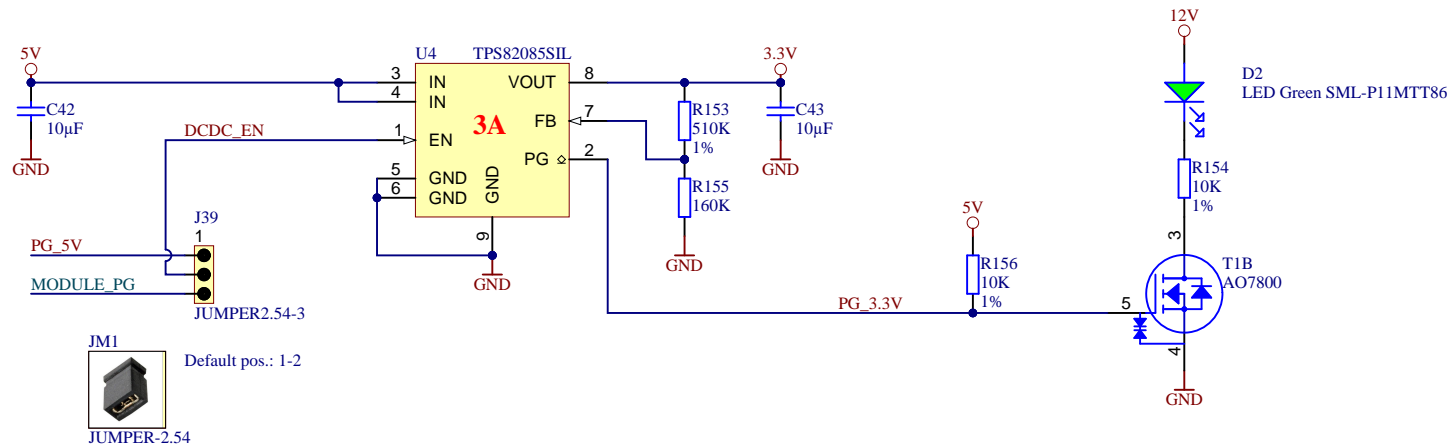
1


2

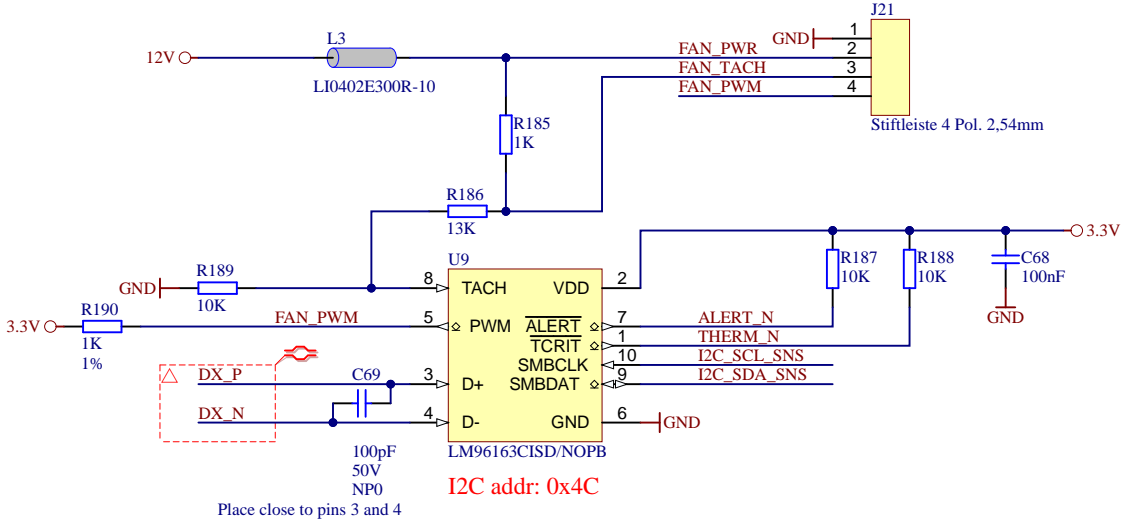
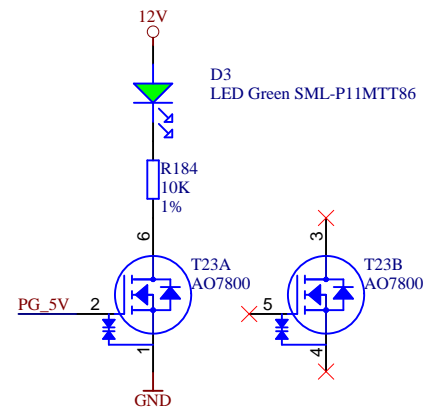
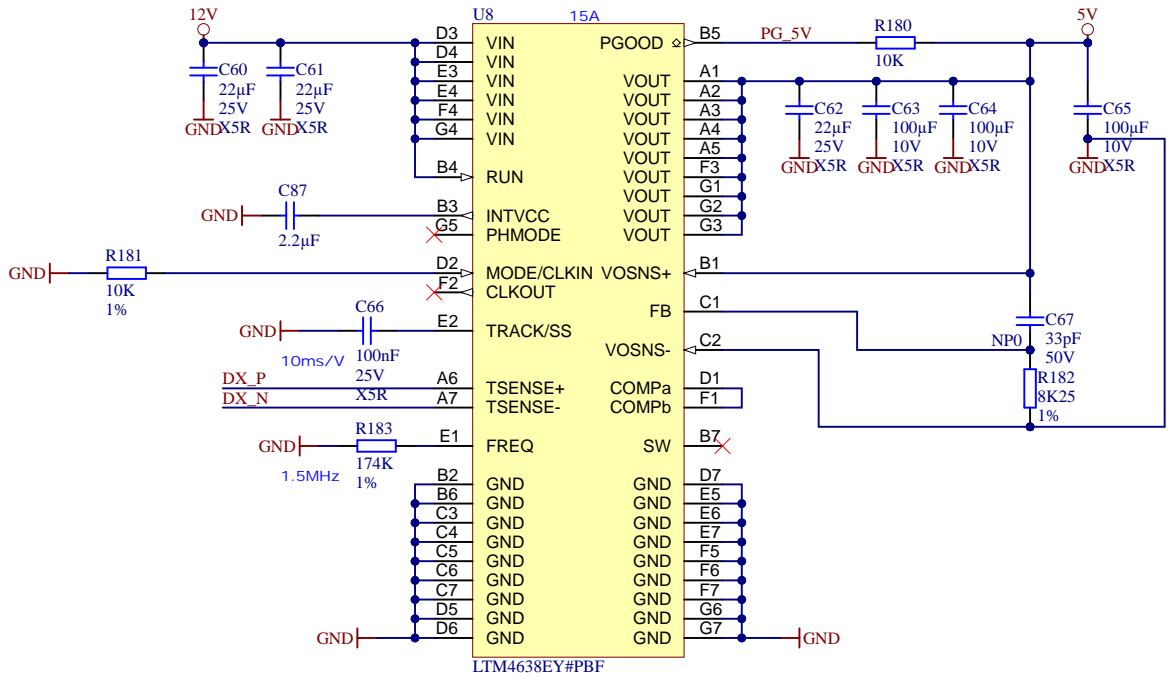
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4

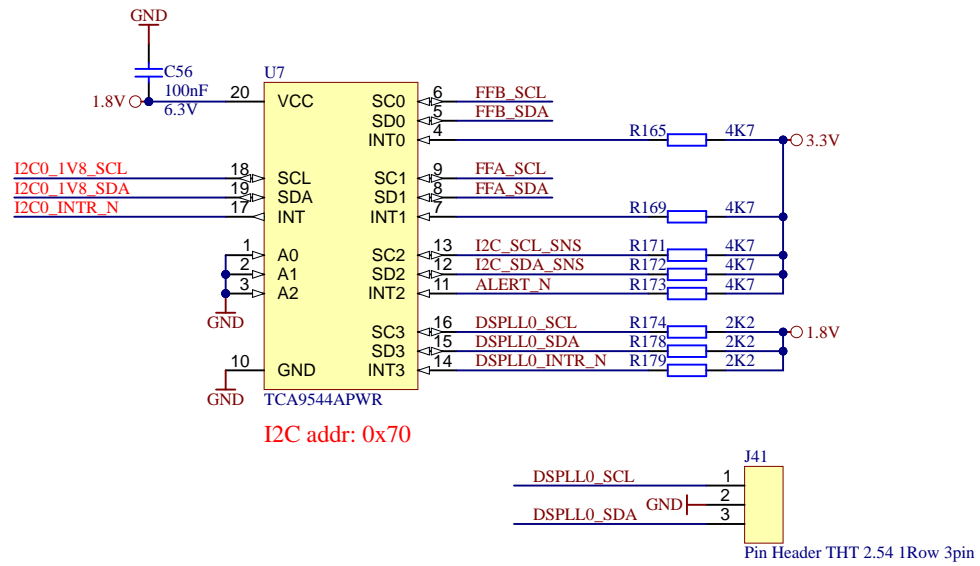
Max C load < 150uF




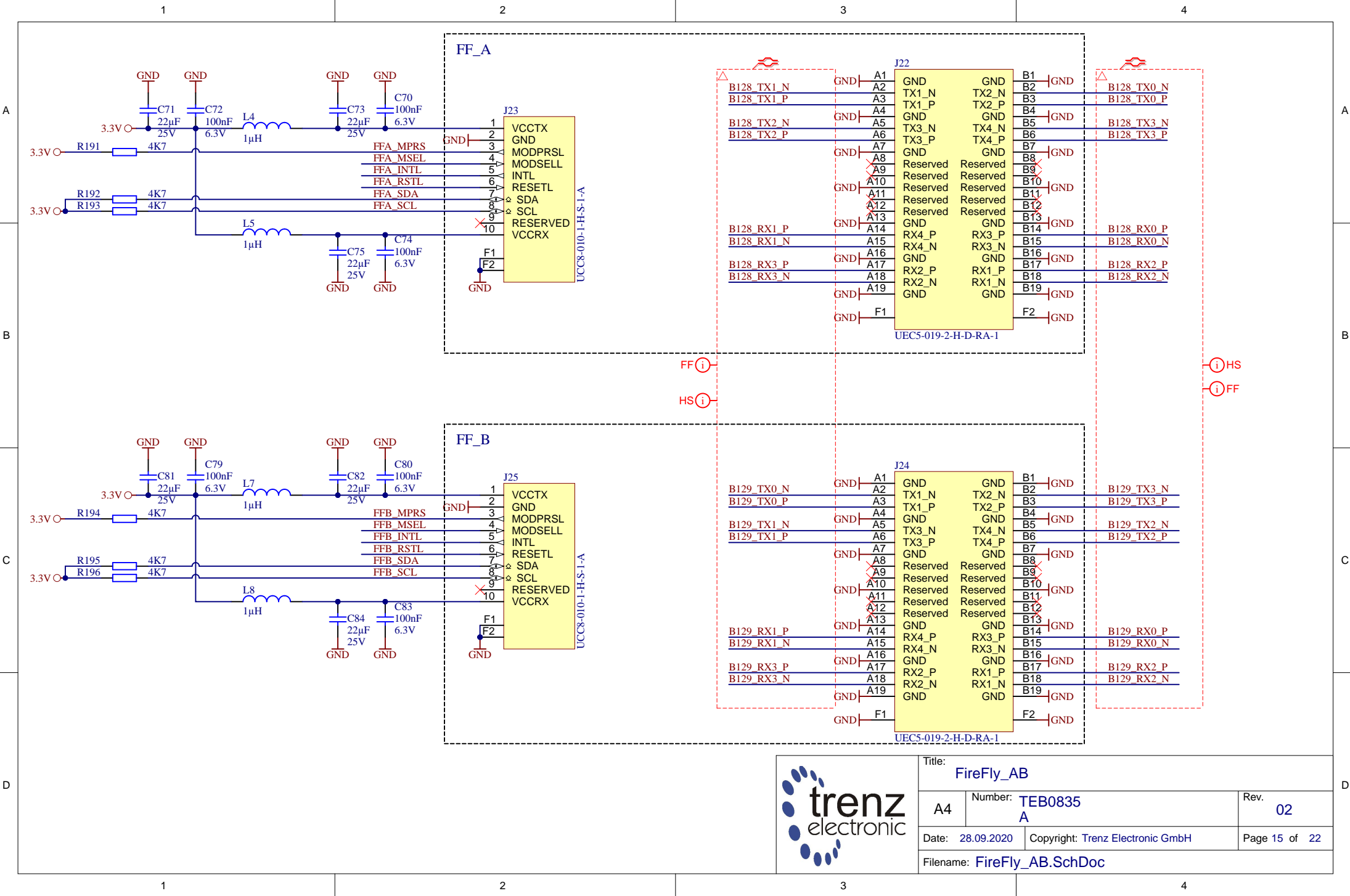
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Date: 28.09.2020		Copyright: Trenz Electronic GmbH	
Page 12 of 22			
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Title: PWR_5V		
A4	Number: TEB0835 A	Rev. 02
Date: 28.09.2020	Copyright: Trenz Electronic GmbH	Page 13 of 22
Filename: PWR_5V.SchDoc		



	Title: CLK-SI5338		
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	Date: 28.09.2020	Copyright: Trenz Electronic GmbH	Page 14 of 22
	Filename: I2C_MUX.SchDoc		



Title: FireFly_AB		
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Date: 28.09.2020	Copyright: Trenz Electronic GmbH	Page 15 of 22
Filename: FireFly_AB.SchDoc		

A

A

B

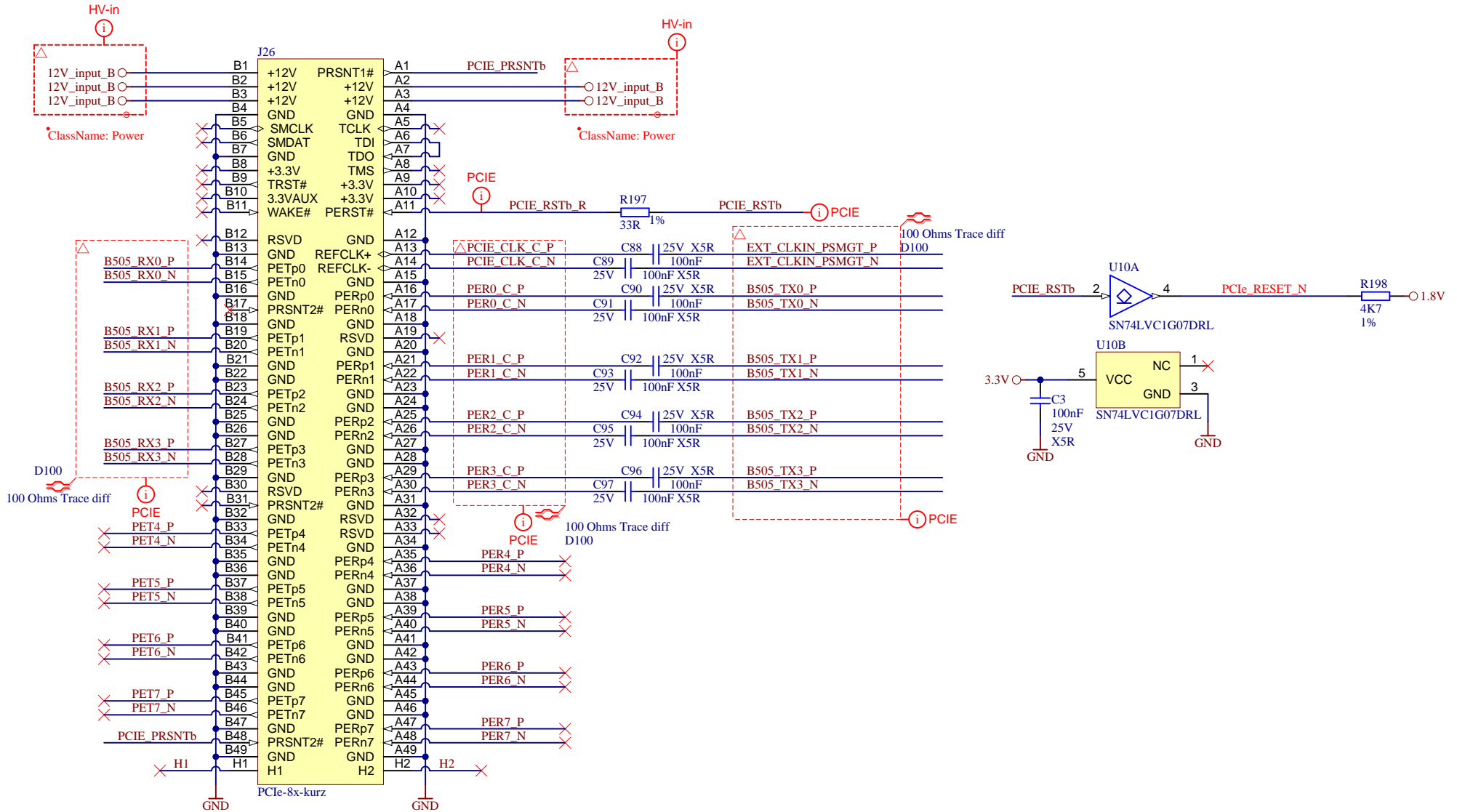
B


C

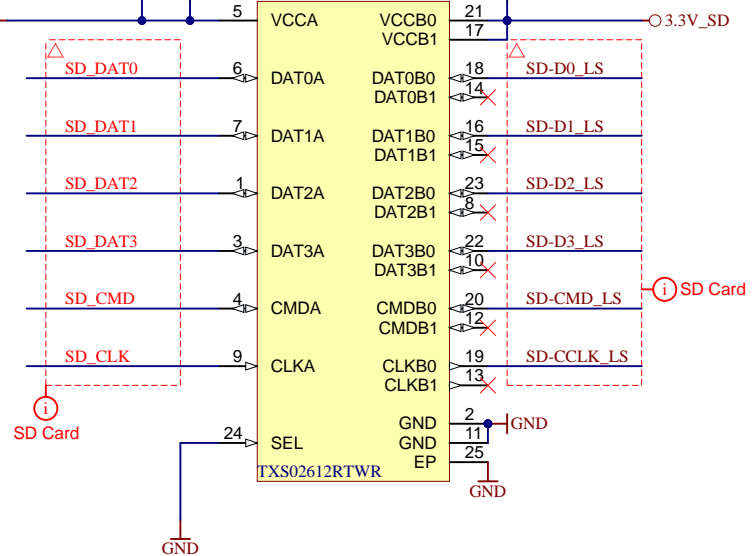
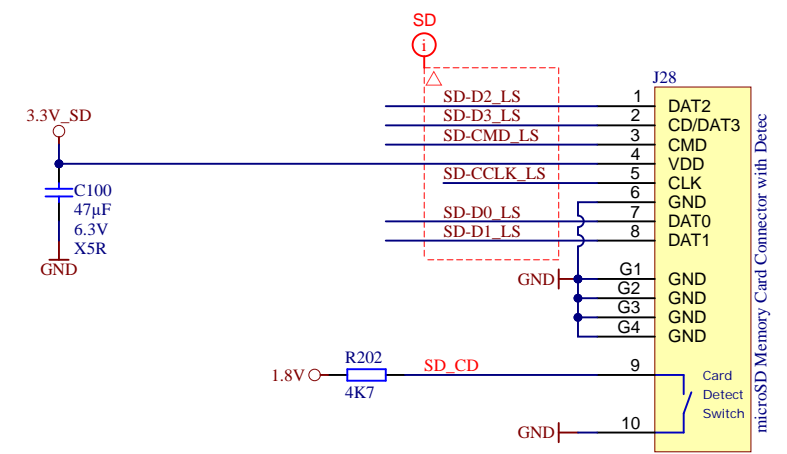
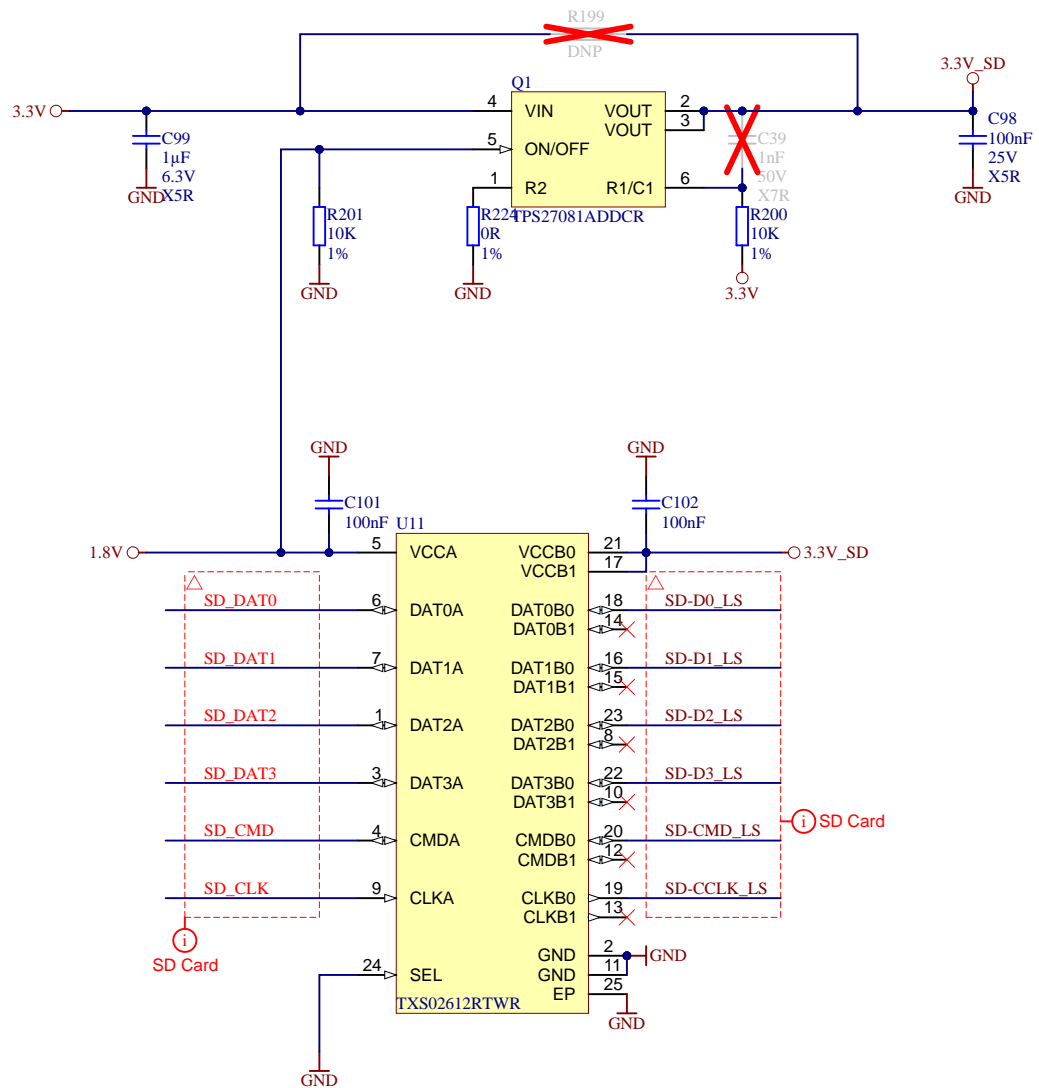
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D

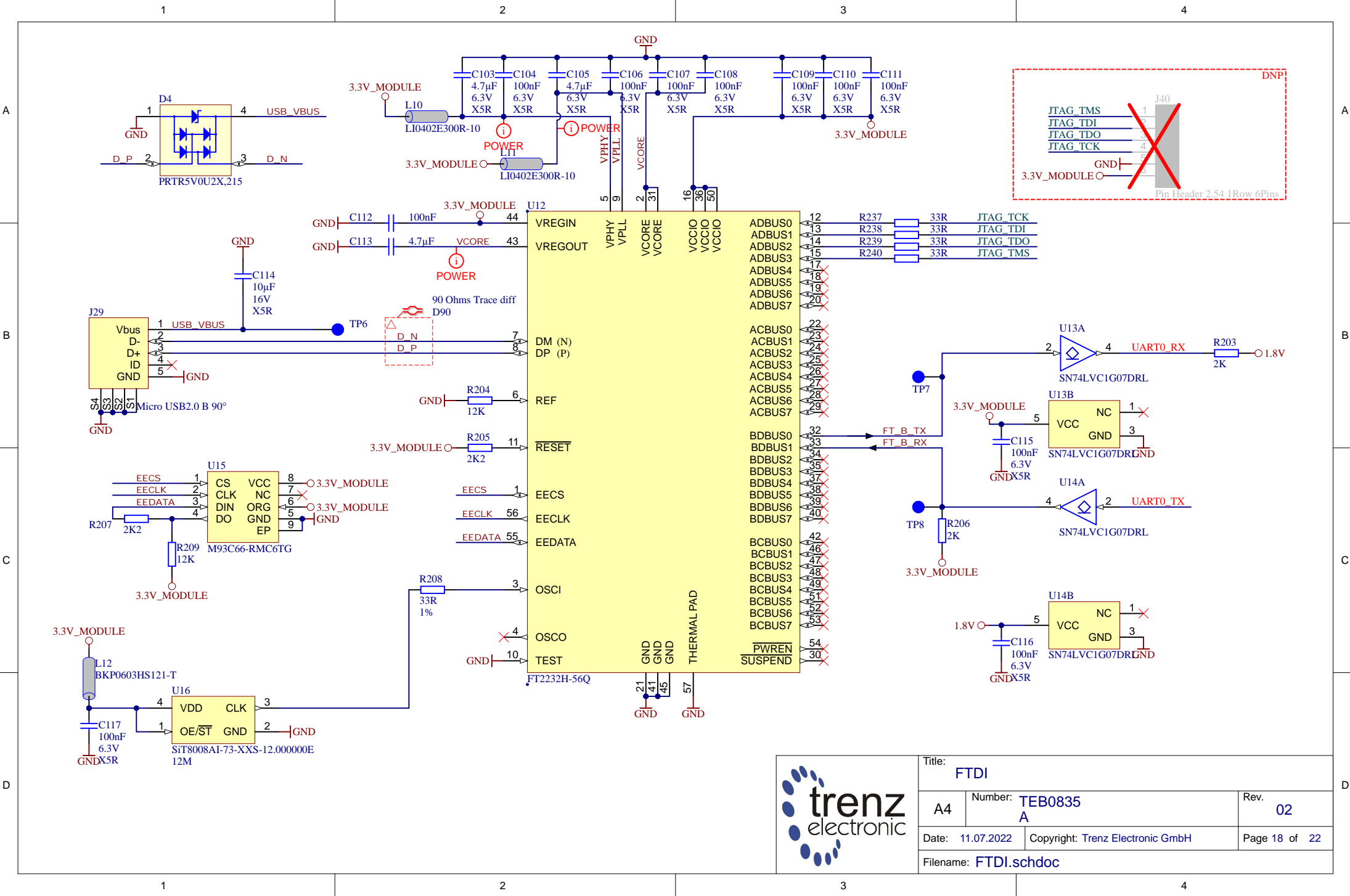
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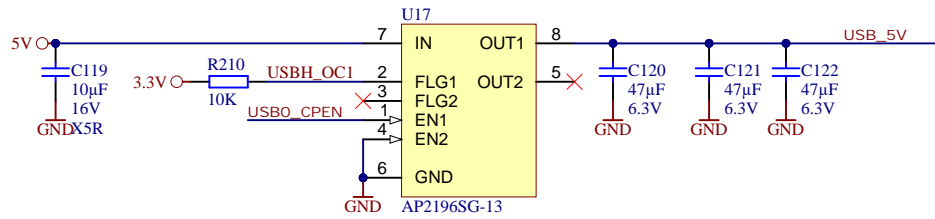
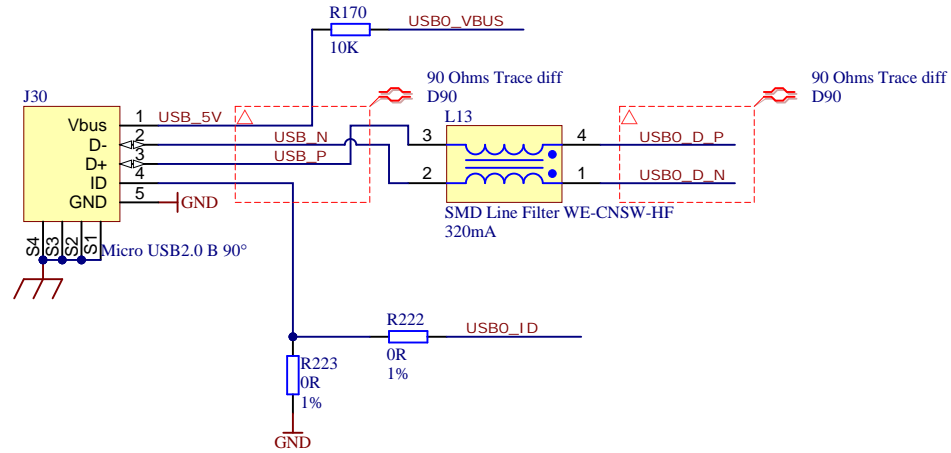
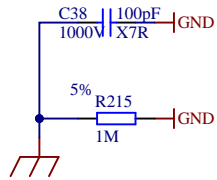
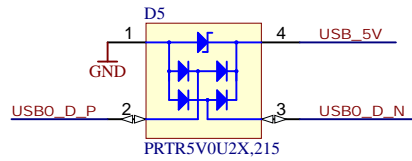
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Date: 28.09.2020		Copyright: Trenz Electronic GmbH		Page 16 of 22
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Title: SD		
A4	Number: TEB0835 A	Rev. 02
Date: 28.09.2020	Copyright: Trenz Electronic GmbH	Page 17 of 22
Filename: SD.SchDoc		



Title: FTDI		
A4	Number: TEB0835 A	Rev. 02
Date: 11.07.2022	Copyright: Trenz Electronic GmbH	
Filename: FTDI.schdoc		Page 18 of 22



Title: MicroUSB		
A4	Number: TEB0835 A	Rev. 02
Date: 28.09.2020	Copyright: Trenz Electronic GmbH	Page 19 of 22
Filename: MicroUSB.SchDoc		

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A

A

B

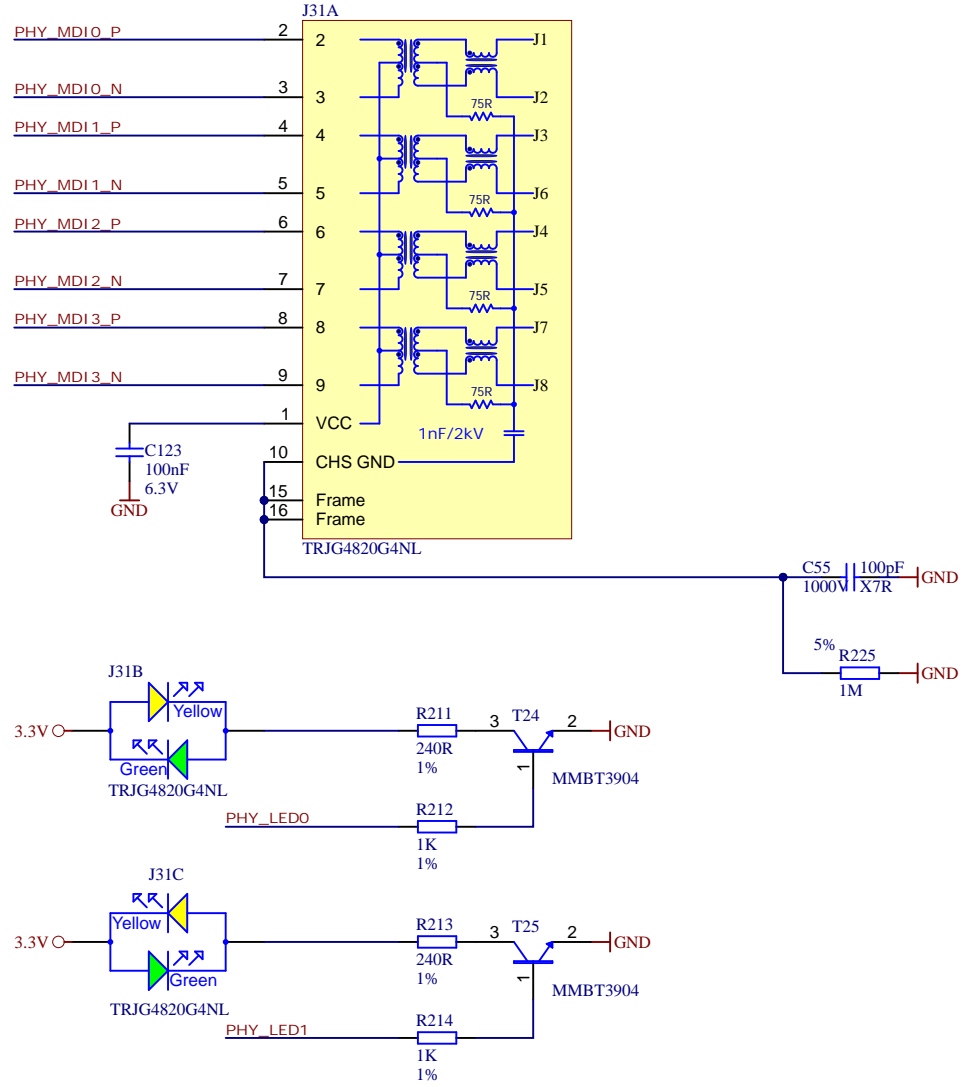
B

C

C

D

D



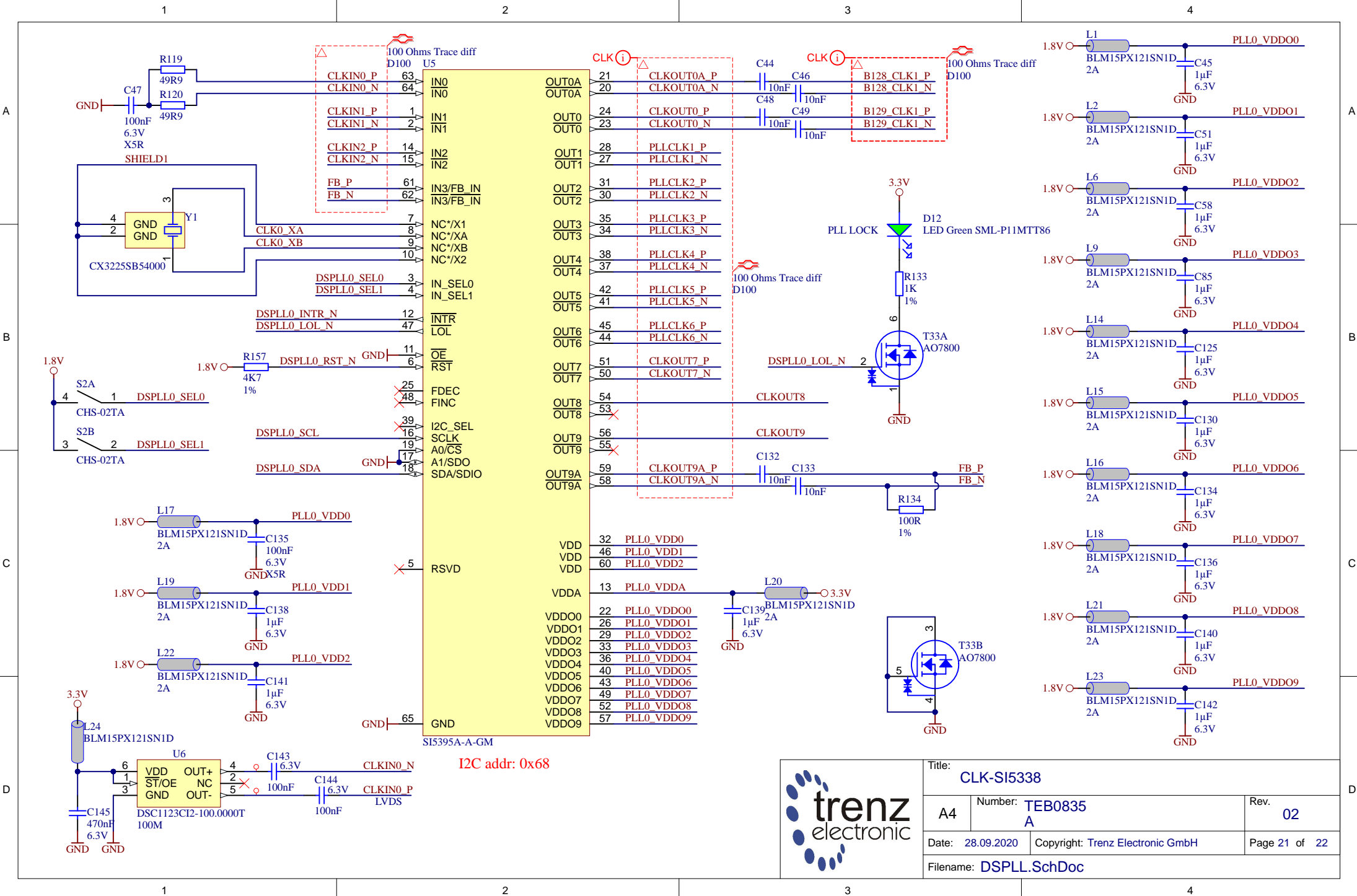
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Date: 28.09.2020	Copyright: Trenz Electronic GmbH	Page 20 of 22
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Title: CLK-SI5338		
A4	Number: TEB0835 A	Rev. 02
Date: 28.09.2020	Copyright: Trenz Electronic GmbH	Page 21 of 22
Filename: DSPLL.SchDoc		

REVISION HISTORY

REV	Description	
-01	Initial revision	IG
-02	<ol style="list-style-type: none"> 1 All module's mount holes are connected to GND; 2 CLK_Connectors. Added baluns for each clock inputs; 3 Internal DSPLL is changed on SI5395A-A-GM; 4 Added ability to use internal DSPLL as a source for each clock; 5 Added clock inputs CLKIN1, CLKIN2 and clock outputs OUT1 , OUT2 connected to DSPLL.; 6 All clock traces are matched with tolerance 0.2 mm; 7 Lengths of inputs ADC0, ADC2, ADC4, ADC6 are matched with tolerance 0.2 mm; 8 Lengths of outputs DAC0 and DAC2 are matched with tolerance 0.2 mm; 9 Lengths of outputs DAC4, DAC5, DAC6, DAC7 are matched with tolerance 0.2 mm; 10 In REV02: FTDI is powered from 3.3V_Module; 11 Signal PLL_INTR_N is removed; 12 Signal BOARD_PG is renamed in MODULE_PG; 13 Added ability to select enable signal for internal DC-DCs 3.3V and 1.8V. 14 Added JTAG connector J40. 15 Added VBAT schematic. Added a holder for CR1220 3V battery. 	IG

	Title: Revision_Changes		
	A4	Number: TEB0835 A	Rev. 02
	Date: 28.09.2020	Copyright: Trenz Electronic GmbH	Page 22 of 22
	Filename: Revision_Changes.SchDoc		