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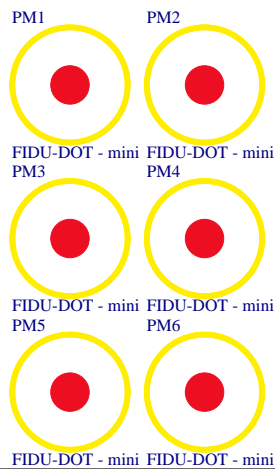
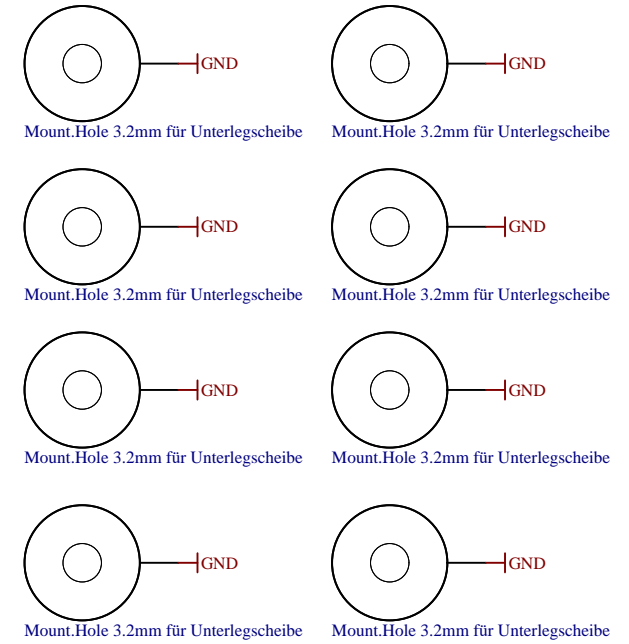
C

C

D

D

- U_Clock
Clock.SchDoc
- U_DDR4-RAM
DDR4-RAM.SchDoc
- U_DDR4-RAM_2
DDR4-RAM_2.SchDoc
- U_DDR4-RAM_3
DDR4-RAM_3.SchDoc
- U_DDR4-RAM_4
DDR4-RAM_4.SchDoc
- U_DDR4-TERM
DDR4-TERM.SchDoc
- CPLD
CPLD.SchDoc
- U_ZU
ZU.SchDoc
- U_USB-PHY
USB-PHY.SchDoc
- U_Ethernet
Ethernet.SchDoc
- U_B2B
B2B.SchDoc
- U_B2B_2
B2B_2.SchDoc
- PWR_Structure
PWR_Structure.SchDoc



LOGO1
TE Logo PRINT Layer
LOGO PRINT

Serial
Serialnumber 6,3 x 6.3mm

Design drawn by:	IG
Checked by:	MR
Assembly variant:	NYE21-A
Created by:	IG
Modified by:	IG
Modified at:	2020-06-10



Title: TE0835		
A4	Number: TE0835 NYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 1 of 34
Filename: TE0835.SchDoc		

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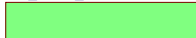
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A

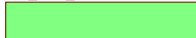
HD
ZU_HD.SchDoc



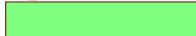
MGT_L
ZU_MGT_L.SchDoc



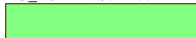
ZU_B65_B66
ZU_B65_B66.SchDoc



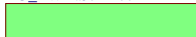
MIO
ZU_MIO.SchDoc



PSDDR
ZU_PSDDR.SchDoc



ZU_PWR
ZU_PWR.SchDoc



ZU_PWR2
ZU_PWR2.SchDoc



ZU_PWR3
ZU_PWR3.SchDoc



ZU_ADC
ZU_ADC.SchDoc



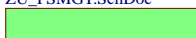
ZU_DAC
ZU_DAC.SchDoc



ZU_CFG
ZU_CFG.SchDoc



ZU_PSMGT
ZU_PSMGT.SchDoc



B

B

C

C

D

D

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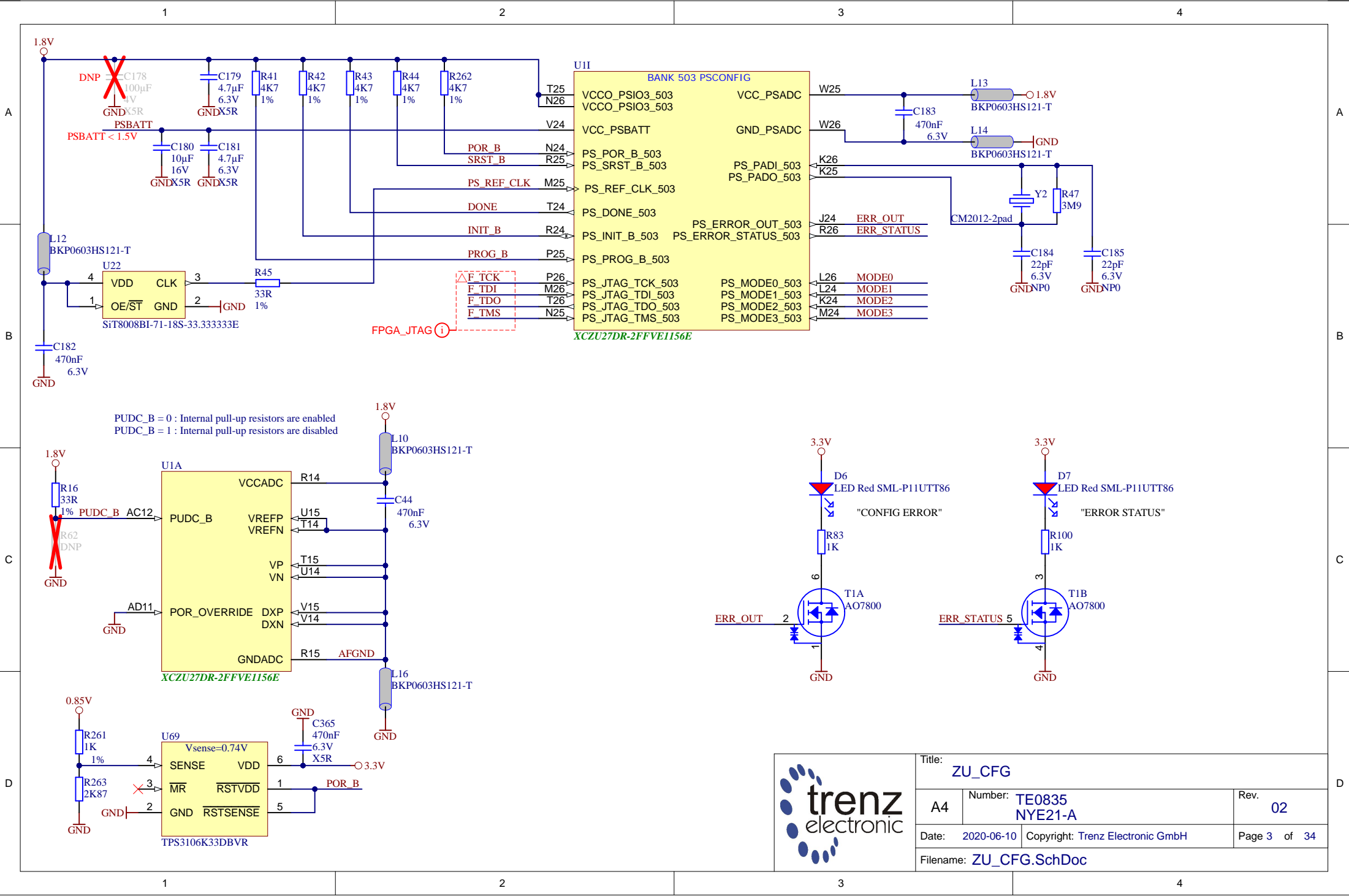
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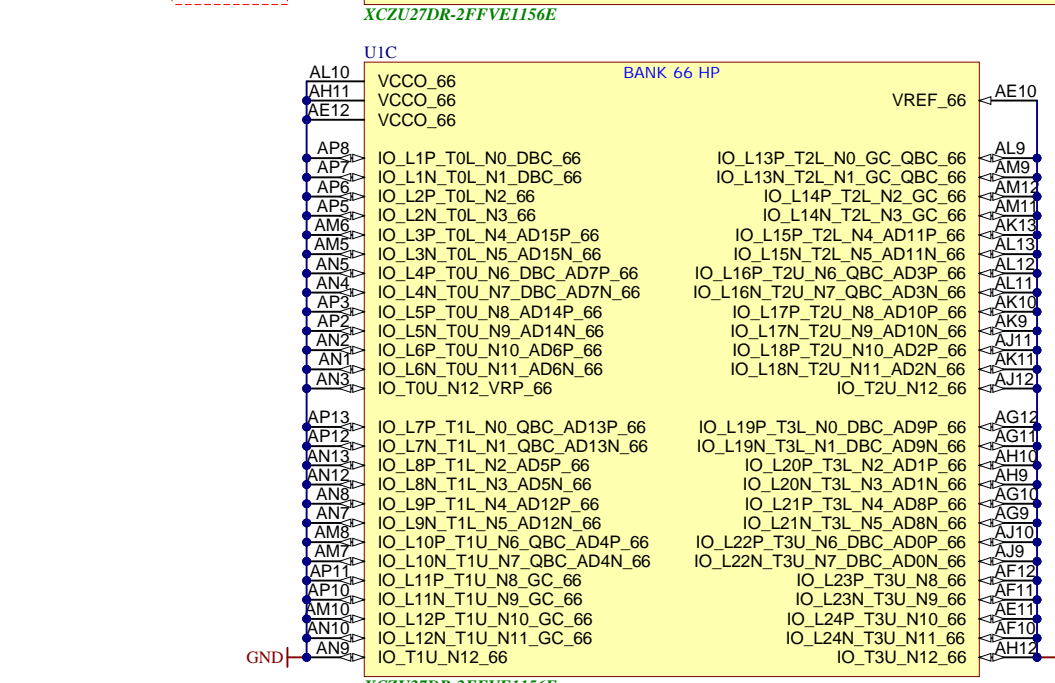
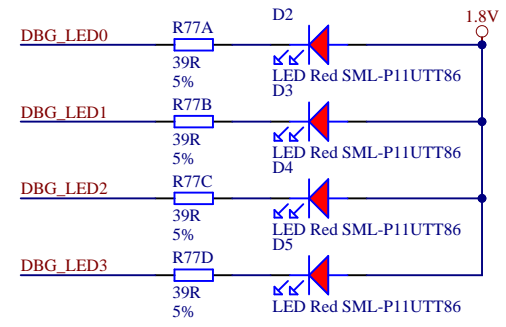
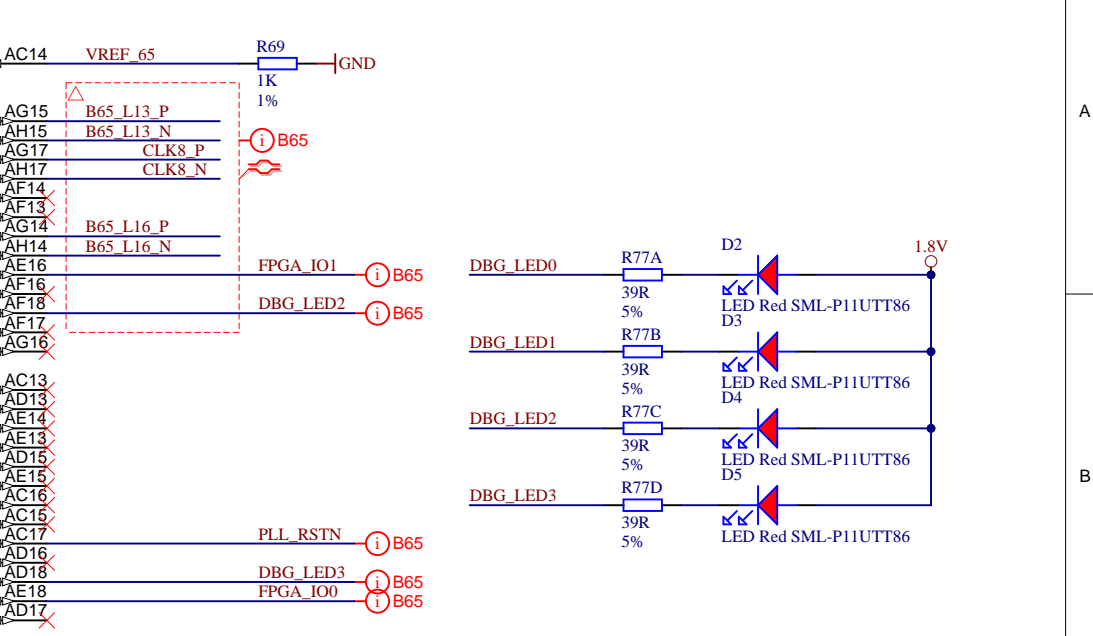
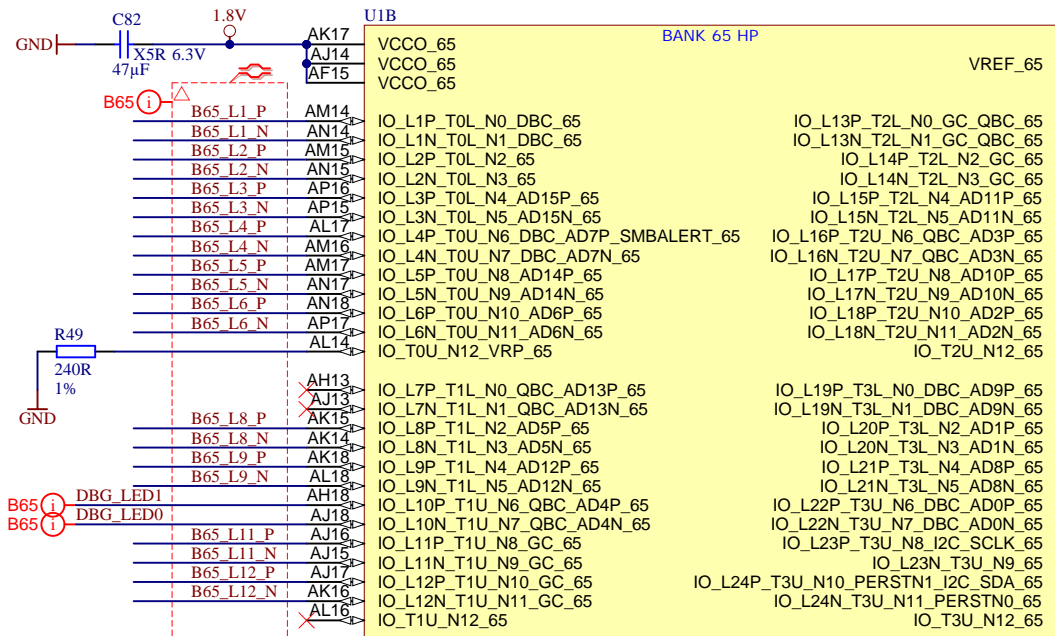
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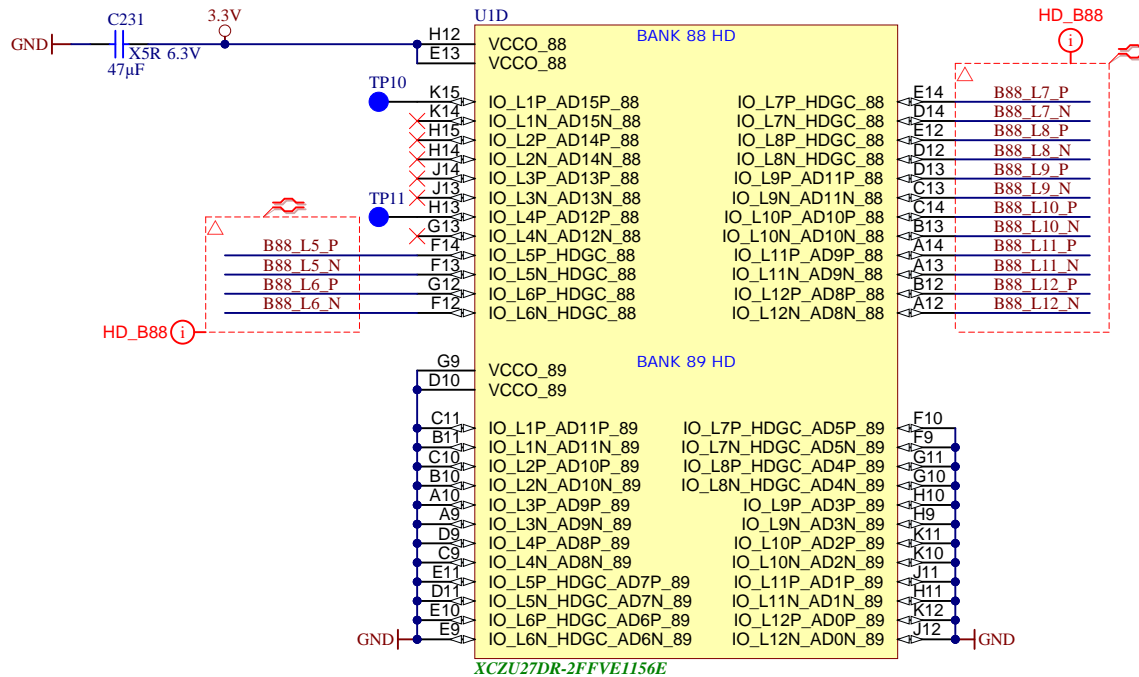
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A4	Number: TE0835 NYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 2 of 34
Filename: ZU.SchDoc		




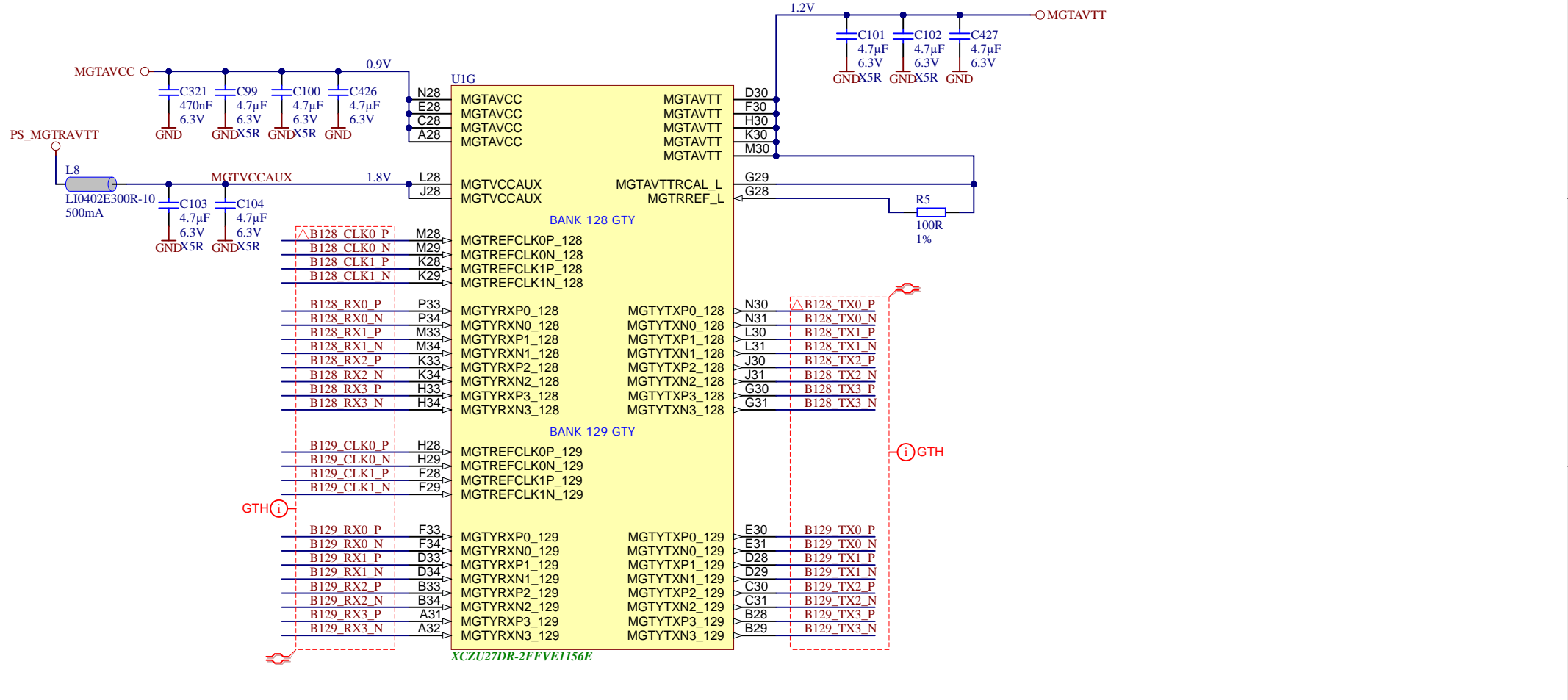
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Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 3 of 34
Filename: ZU_CFG.SchDoc		



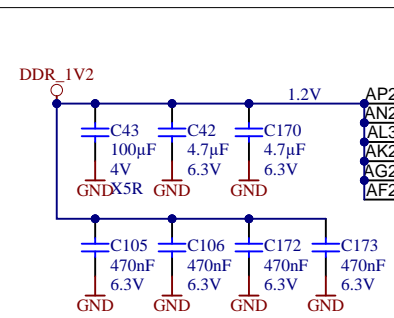
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A4	Number: TE0835 NYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 4 of 34
Filename: ZU_B65_B66.SchDoc		



			Title: ZU_HD	
			A4	Number: TE0835 NYE21-A
Date: 2020-06-10		Copyright: Trenz Electronic GmbH		Page 5 of 34
Filename: ZU_HD.SchDoc				



	Title: ZU_MGT_L	
	A4	Number: TE0835 NYE21-A
	Date: 2020-06-10	Copyright: Trenz Electronic GmbH
	Filename: ZU_MGT_L.SchDoc	
	Rev. 02	Page 6 of 34



UIJ

BANK 504 PSDDR

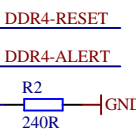
VCCO_PSDDR_504	PS_DDR_CK0_504
VCCO_PSDDR_504	PS_DDR_CK_N0_504
VCCO_PSDDR_504	PS_DDR_CKE0_504
VCCO_PSDDR_504	PS_DDR_CK1_504
VCCO_PSDDR_504	PS_DDR_CK_N1_504
VCCO_PSDDR_504	PS_DDR_CKE1_504
PS_DDR_A0_504	PS_DDR_A0_504
PS_DDR_A1_504	PS_DDR_A1_504
PS_DDR_A2_504	PS_DDR_A2_504
PS_DDR_A3_504	PS_DDR_A3_504
PS_DDR_A4_504	PS_DDR_A4_504
PS_DDR_A5_504	PS_DDR_A5_504
PS_DDR_A6_504	PS_DDR_A6_504
PS_DDR_A7_504	PS_DDR_A7_504
PS_DDR_A8_504	PS_DDR_A8_504
PS_DDR_A9_504	PS_DDR_A9_504
PS_DDR_A10_504	PS_DDR_A10_504
PS_DDR_A11_504	PS_DDR_A11_504
PS_DDR_A12_504	PS_DDR_A12_504
PS_DDR_A13_504	PS_DDR_A13_504
PS_DDR_A14_504	PS_DDR_A14_504
PS_DDR_A15_504	PS_DDR_A15_504
PS_DDR_A16_504	PS_DDR_A16_504
PS_DDR_A17_504	PS_DDR_A17_504
PS_DDR_CS_N0_504	PS_DDR_CS_N0_504
PS_DDR_CS_N1_504	PS_DDR_CS_N1_504
PS_DDR_BA0_504	PS_DDR_BA0_504
PS_DDR_BA1_504	PS_DDR_BA1_504
PS_DDR_BG0_504	PS_DDR_BG0_504
PS_DDR_BG1_504	PS_DDR_BG1_504
PS_DDR_PARITY_504	PS_DDR_PARITY_504
PS_DDR_RAM_RST_N_504	PS_DDR_RAM_RST_N_504
PS_DDR_ACT_N_504	PS_DDR_ACT_N_504
PS_DDR_ALERT_N_504	PS_DDR_ALERT_N_504
PS_DDR_ZQ_504	PS_DDR_ZQ_504
PS_DDR_ODT0_504	PS_DDR_ODT0_504
PS_DDR_ODT1_504	PS_DDR_ODT1_504

XCZU27DR-2FFVE1156E

ADDR_CMD_CTRL



AN28	DDR4-CLK0_P
AP28	DDR4-CLK0_N
AP31	DDR4-CKE0
AL27	DDR4-A0
AM27	DDR4-A1
AK28	DDR4-A2
AN29	DDR4-A3
AP27	DDR4-A4
AP26	DDR4-A5
AN27	DDR4-A6
AN25	DDR4-A7
AK26	DDR4-A8
AJ26	DDR4-A9
AJ25	DDR4-A10
AL28	DDR4-A11
AM26	DDR4-A12
AL29	DDR4-A13
AM25	DDR4-A14
AM29	DDR4-A15
AL26	DDR4-A16
AH25	DDR4-A17
AG25	DDR4-A17
AN30	DDR4-CS
AM30	DDR4-CS
AG26	DDR4-BA0
AK28	DDR4-BA1
AJ27	DDR4-BG0
AJ28	DDR4-BG1
AG27	DDR4-PAR
AF27	DDR4-PAR
AH27	DDR4-ACT
AE26	DDR4-ACT
AF26	DDR4-ZQ
AP30	DDR4-ODT0
AM31	DDR4-ODT0



UIK

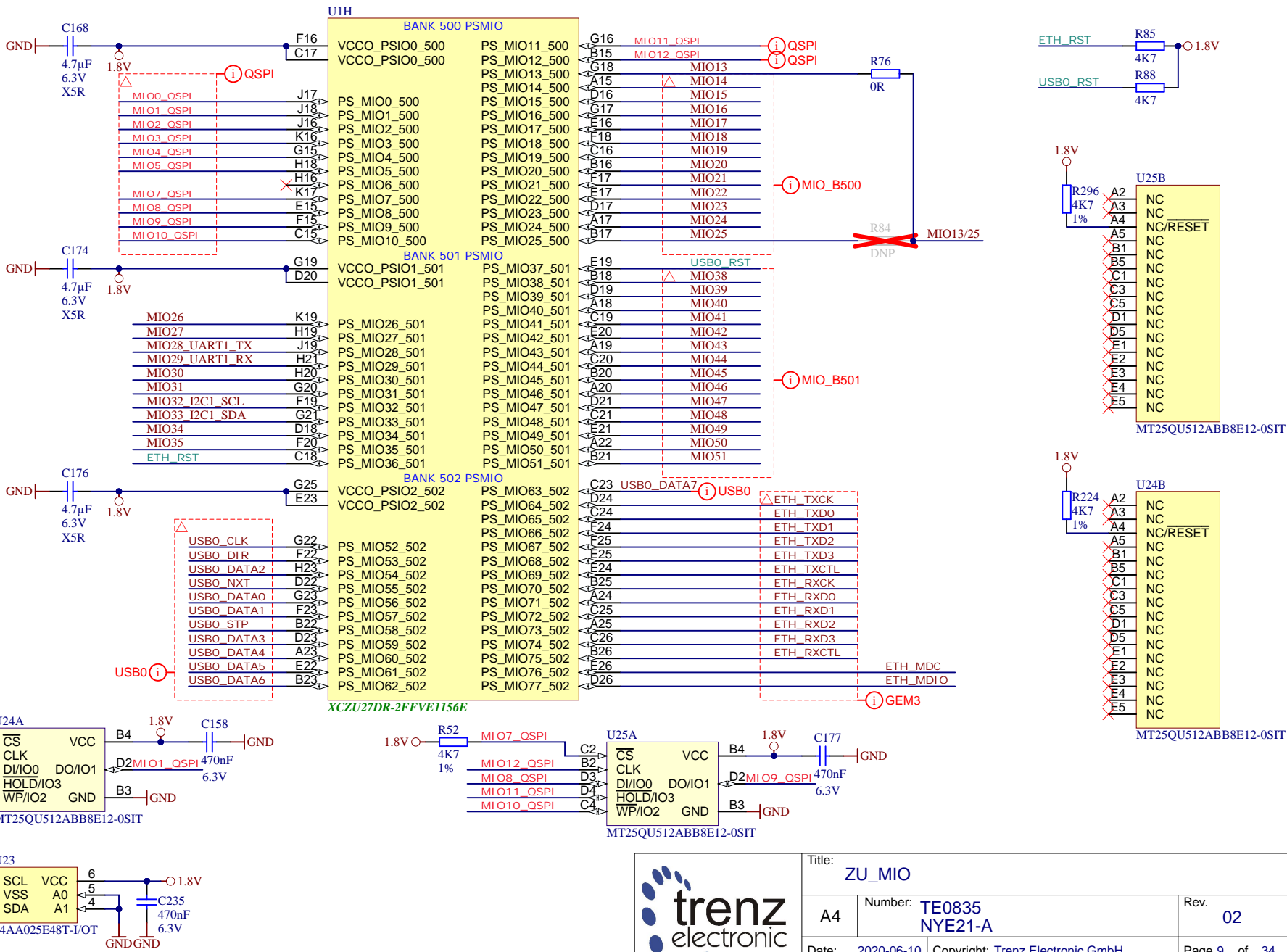
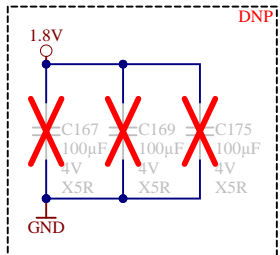
BANK 504 PSDDR

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DQ1	PS_DDR_DQ1_504
DQ2	PS_DDR_DQ2_504
DQ3	PS_DDR_DQ3_504
DQ4	PS_DDR_DQ4_504
DQ5	PS_DDR_DQ5_504
DQ6	PS_DDR_DQ6_504
DQ7	PS_DDR_DQ7_504
DQ8	PS_DDR_DQ8_504
DQ9	PS_DDR_DQ9_504
DQ10	PS_DDR_DQ10_504
DQ11	PS_DDR_DQ11_504
DQ12	PS_DDR_DQ12_504
DQ13	PS_DDR_DQ13_504
DQ14	PS_DDR_DQ14_504
DQ15	PS_DDR_DQ15_504
DQ16	PS_DDR_DQ16_504
DQ17	PS_DDR_DQ17_504
DQ18	PS_DDR_DQ18_504
DQ19	PS_DDR_DQ19_504
DQ20	PS_DDR_DQ20_504
DQ21	PS_DDR_DQ21_504
DQ22	PS_DDR_DQ22_504
DQ23	PS_DDR_DQ23_504
DQ24	PS_DDR_DQ24_504
DQ25	PS_DDR_DQ25_504
DQ26	PS_DDR_DQ26_504
DQ27	PS_DDR_DQ27_504
DQ28	PS_DDR_DQ28_504
DQ29	PS_DDR_DQ29_504
DQ30	PS_DDR_DQ30_504
DQ31	PS_DDR_DQ31_504
DDR4-DQS0_P	PS_DDR_DQS_P0_504
DDR4-DQS0_N	PS_DDR_DQS_N0_504
DDR4-DQS1_P	PS_DDR_DQS_P1_504
DDR4-DQS1_N	PS_DDR_DQS_N1_504
DDR4-DQS2_P	PS_DDR_DQS_P2_504
DDR4-DQS2_N	PS_DDR_DQS_N2_504
DDR4-DQS3_P	PS_DDR_DQS_P3_504
DDR4-DQS3_N	PS_DDR_DQS_N3_504
DDR4-DQS4_P	PS_DDR_DQS_P4_504
DDR4-DQS4_N	PS_DDR_DQS_N4_504
DDR4-DQS5_P	PS_DDR_DQS_P5_504
DDR4-DQS5_N	PS_DDR_DQS_N5_504
DDR4-DQS6_P	PS_DDR_DQS_P6_504
DDR4-DQS6_N	PS_DDR_DQS_N6_504
DDR4-DQS7_P	PS_DDR_DQS_P7_504
DDR4-DQS7_N	PS_DDR_DQS_N7_504
AN32	PS_DDR_DQS_P8_504
AN33	PS_DDR_DQS_N8_504
AE29	PS_DDR_DQ32_504
AF29	PS_DDR_DQ33_504
AE28	PS_DDR_DQ34_504
AF28	PS_DDR_DQ35_504
AJ30	PS_DDR_DQ36_504
AH29	PS_DDR_DQ37_504
AH30	PS_DDR_DQ38_504
AH28	PS_DDR_DQ39_504
AE30	PS_DDR_DQ40_504
AD30	PS_DDR_DQ41_504
AD28	PS_DDR_DQ42_504
AD27	PS_DDR_DQ43_504
AB29	PS_DDR_DQ44_504
AC28	PS_DDR_DQ45_504
AB28	PS_DDR_DQ46_504
AC27	PS_DDR_DQ47_504
AG34	PS_DDR_DQ48_504
AH33	PS_DDR_DQ49_504
AH34	PS_DDR_DQ50_504
AH32	PS_DDR_DQ51_504
AK34	PS_DDR_DQ52_504
AK33	PS_DDR_DQ53_504
AK31	PS_DDR_DQ54_504
AK30	PS_DDR_DQ55_504
AG32	PS_DDR_DQ56_504
AF31	PS_DDR_DQ57_504
AF34	PS_DDR_DQ58_504
AE34	PS_DDR_DQ59_504
AD32	PS_DDR_DQ60_504
AE31	PS_DDR_DQ61_504
AD34	PS_DDR_DQ62_504
AD33	PS_DDR_DQ63_504
AP32	PS_DDR_DQ64_504
AM32	PS_DDR_DQ65_504
AL31	PS_DDR_DQ66_504
AL32	PS_DDR_DQ67_504
AP33	PS_DDR_DQ68_504
AM34	PS_DDR_DQ69_504
AN34	PS_DDR_DQ70_504
AL34	PS_DDR_DQ71_504
AM20	PS_DDR_DM0_504
AL23	PS_DDR_DM1_504
AH20	PS_DDR_DM2_504
AG22	PS_DDR_DM3_504
AG31	PS_DDR_DM4_504
AD31	PS_DDR_DM5_504
AJ31	PS_DDR_DM6_504
AE33	PS_DDR_DM7_504
AL33	PS_DDR_DM8_504

XCZU27DR-2FFVE1156E



Title: ZU_PSDDR		
A4	Number: TE0835 NYE21-A	Rev. 02
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Filename: ZU_PSDDR.SchDoc		



Title: ZU_MIO		
A4	Number: TE0835 NYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 9 of 34
Filename: ZU_MIO.SchDoc		

A

B

C

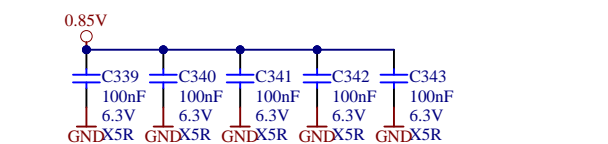
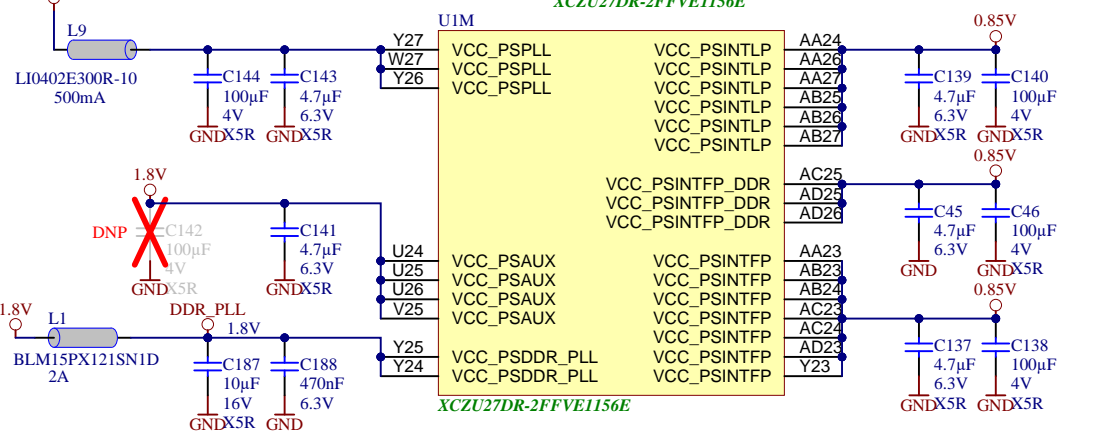
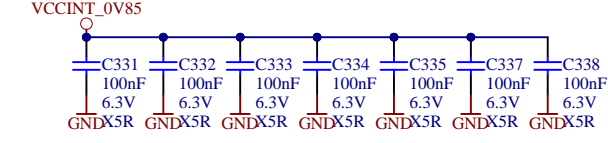
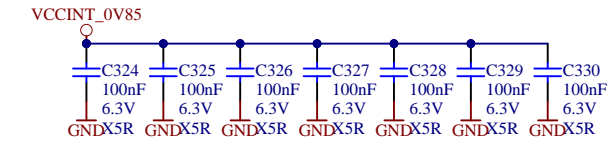
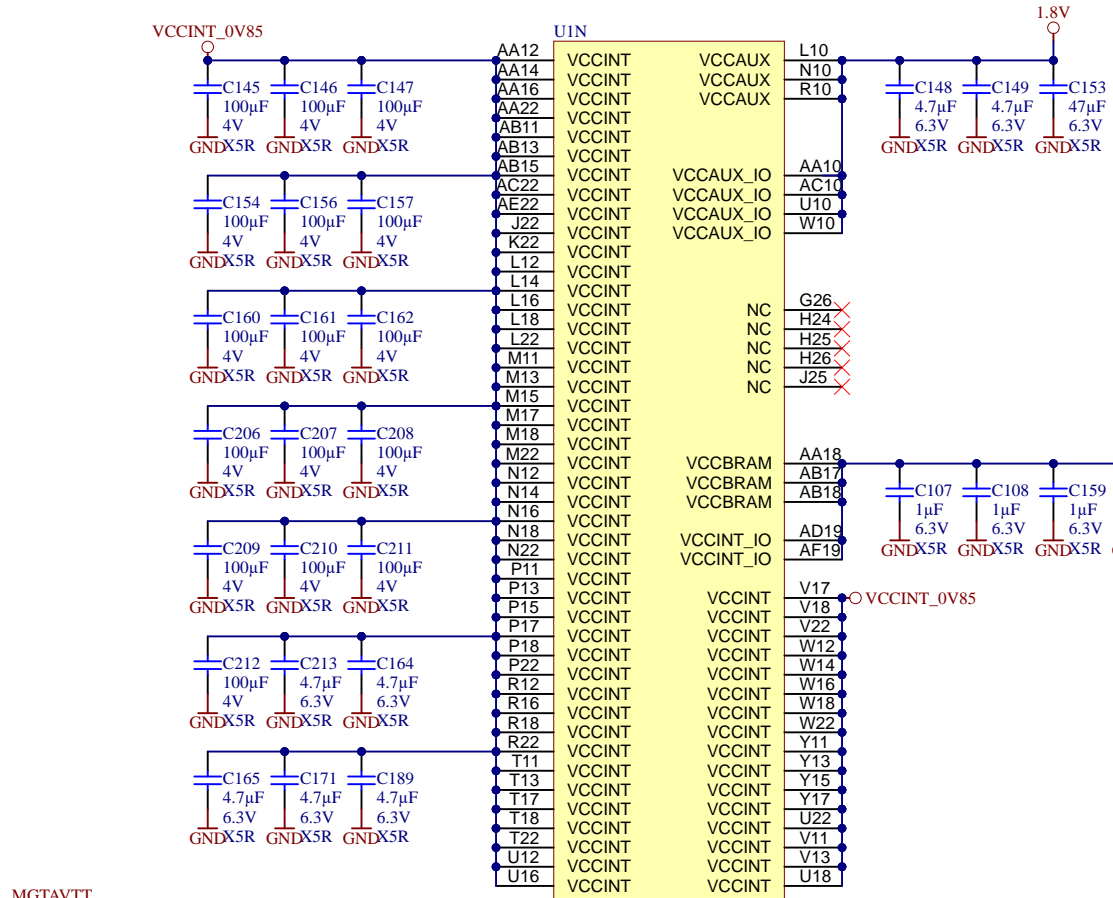
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A

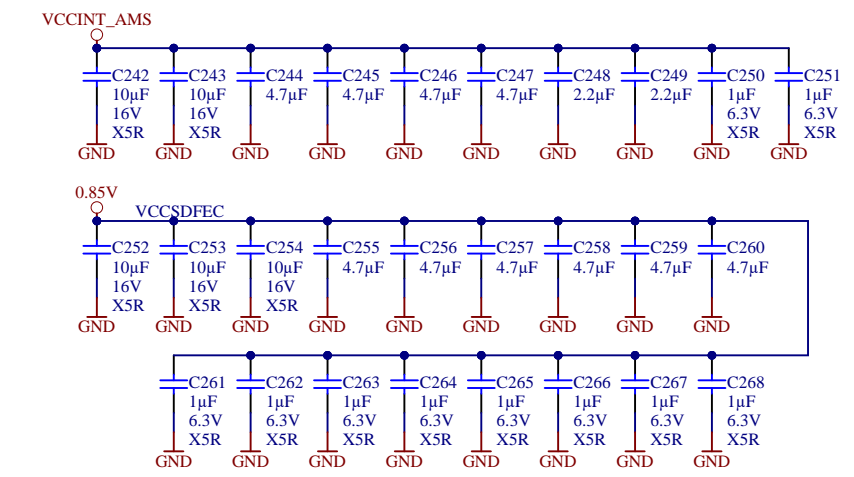
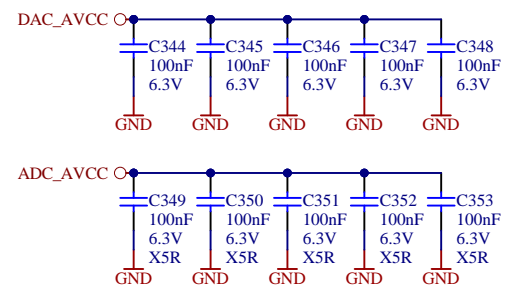
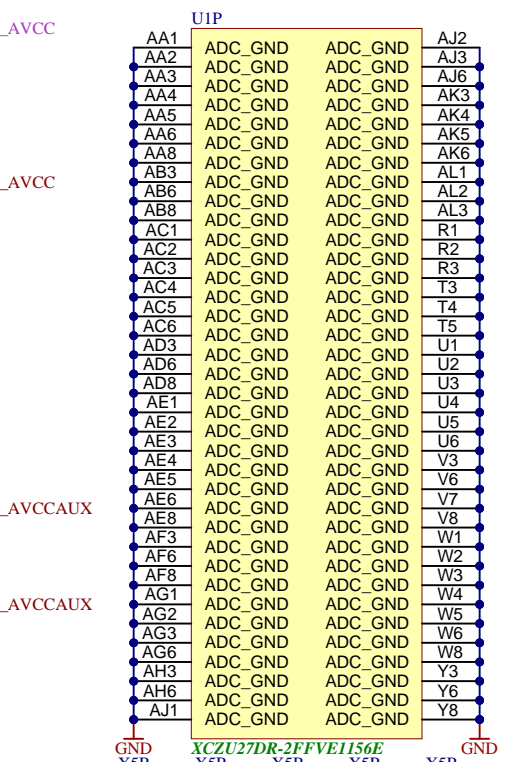
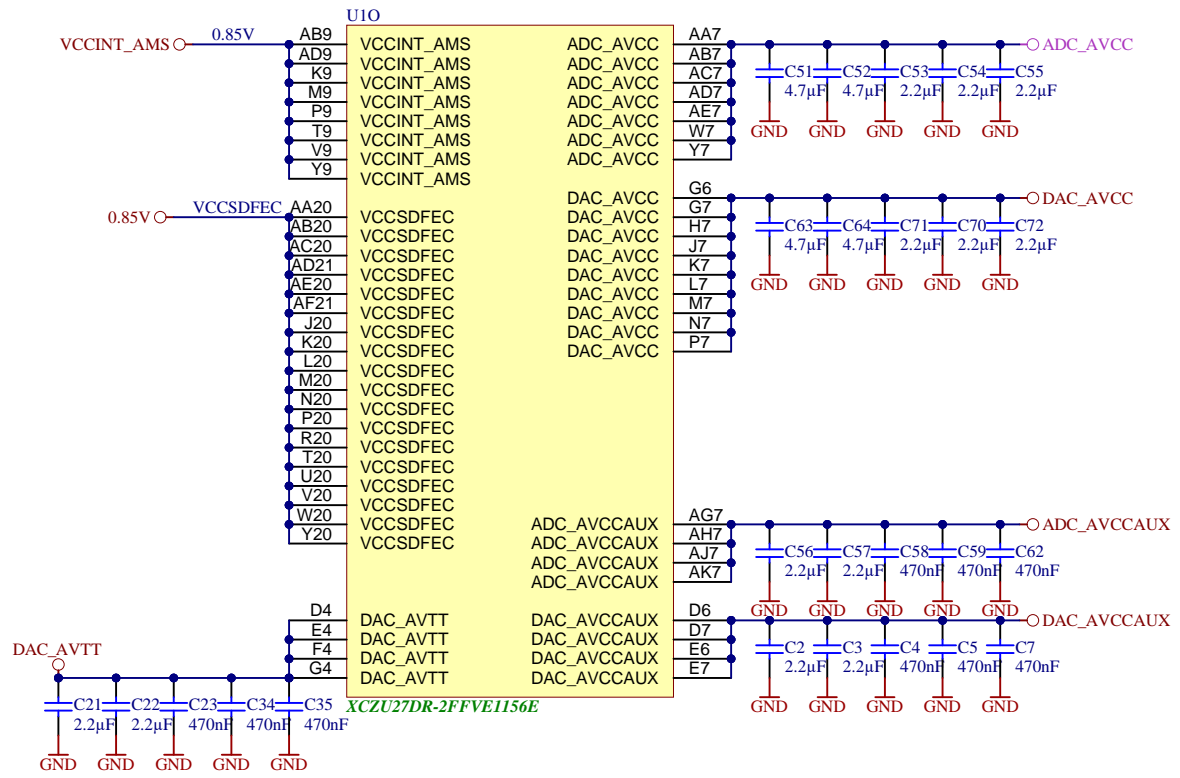
B

C

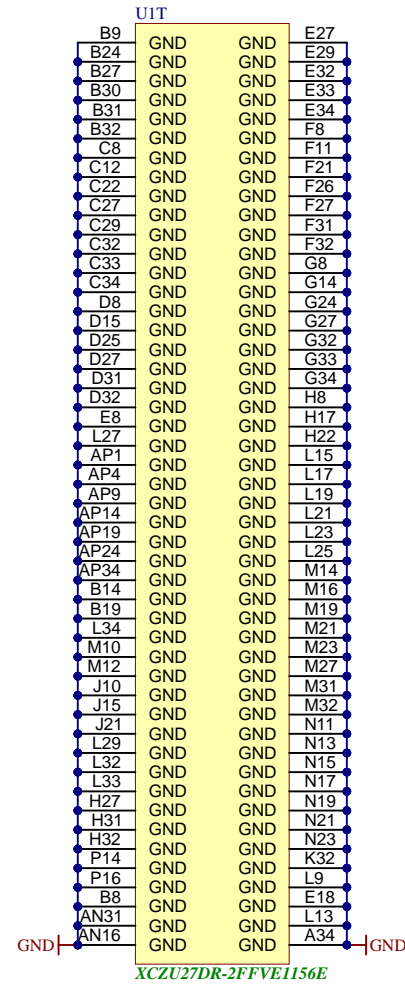
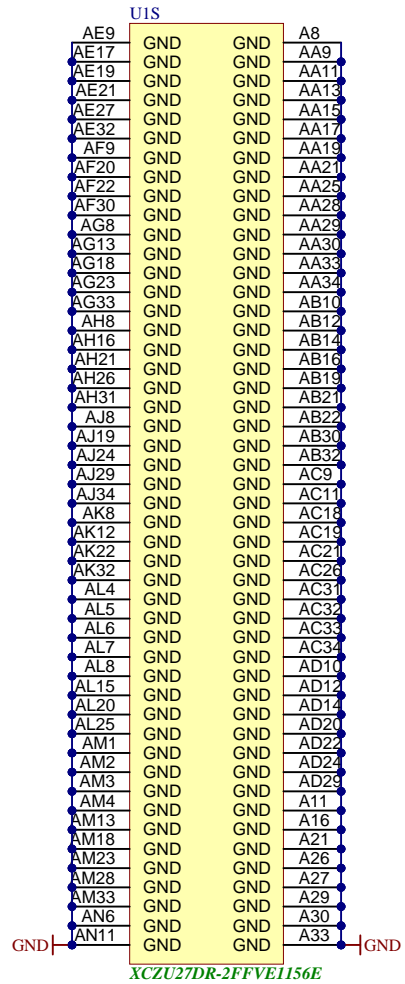
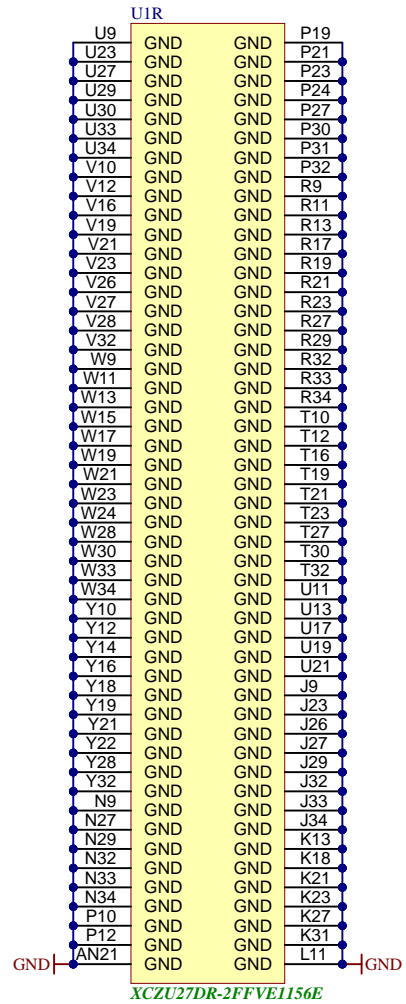
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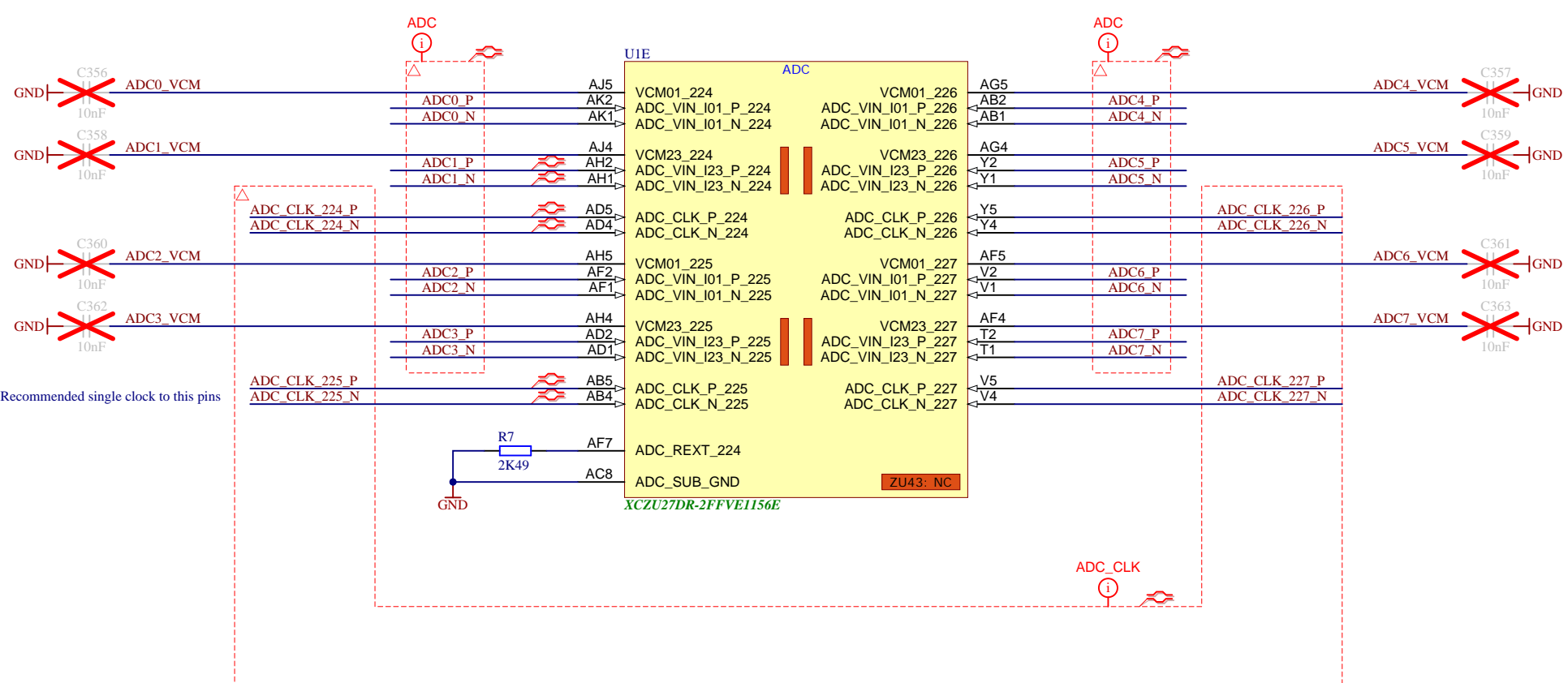
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A4	Number: TE0835 NYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 10 of 34
Filename: ZU_PWR.SchDoc		




Title: ZU_PWR2		
A4	Number: TE0835 NYE21-A	Rev. 02
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Title: ZU_PWR3		
A4	Number: TE0835 NYE21-A	Rev. 02
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Filename: ZU_PWR3.SchDoc		



Recommended single clock to this pins

	Title: ZU_ADC		
	A4	Number: TE0835 NYE21-A	Rev. 02
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	Filename: ZU_ADC.SchDoc		

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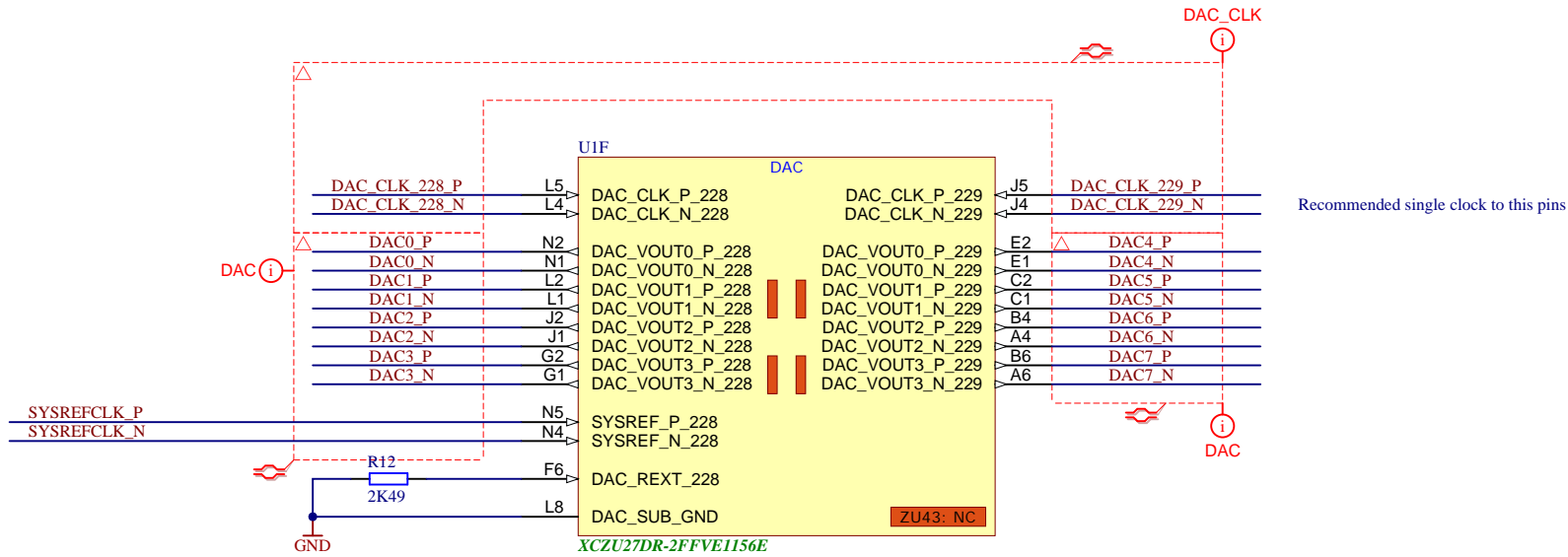
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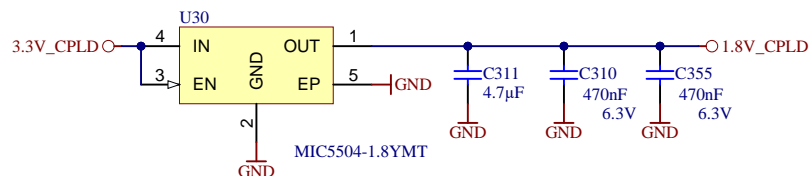
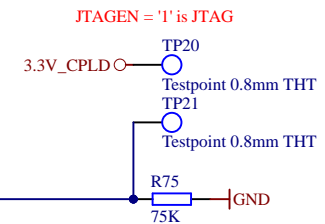
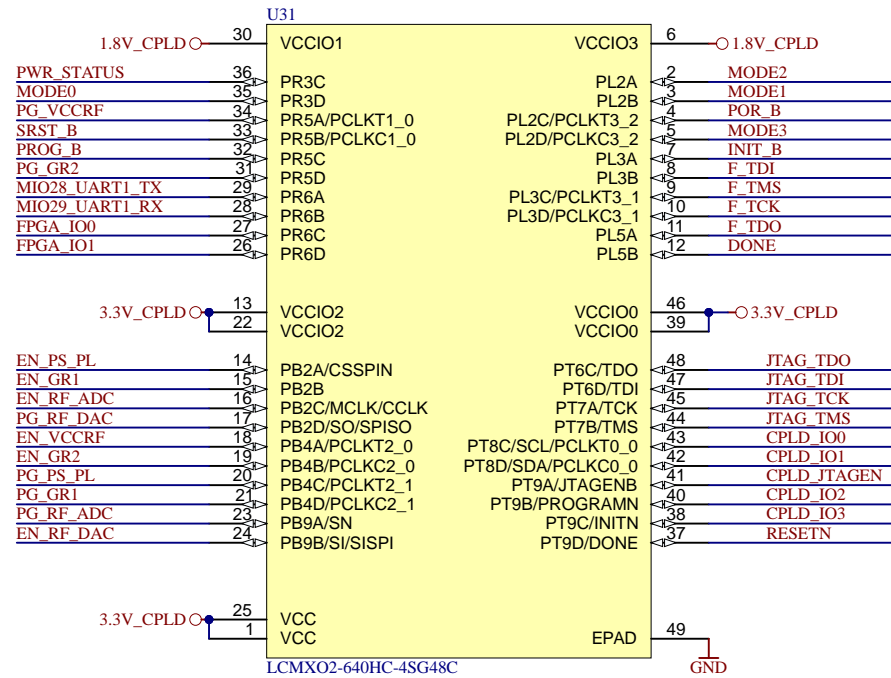
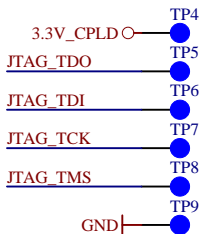
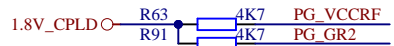
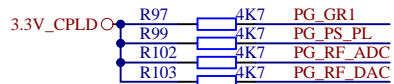
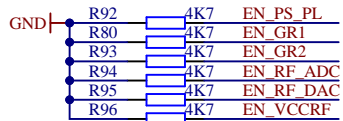
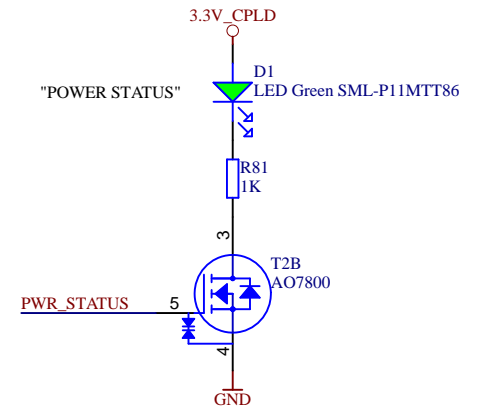
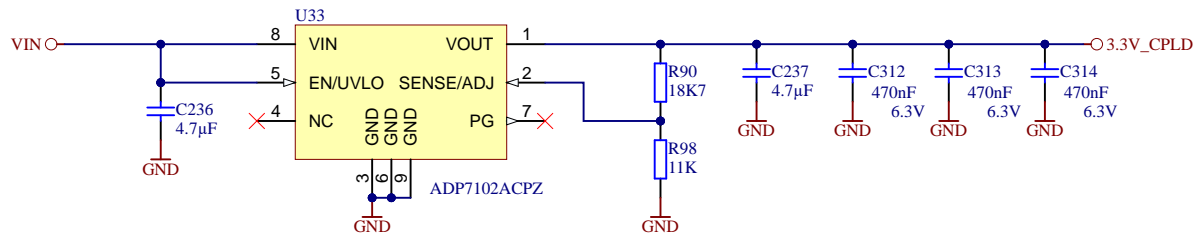
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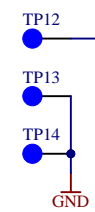


	Title: ZU_DAC	
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	Date: 2020-06-10	Rev. 02
	Copyright: Trenz Electronic GmbH	
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Filename: ZU_DAC.SchDoc		

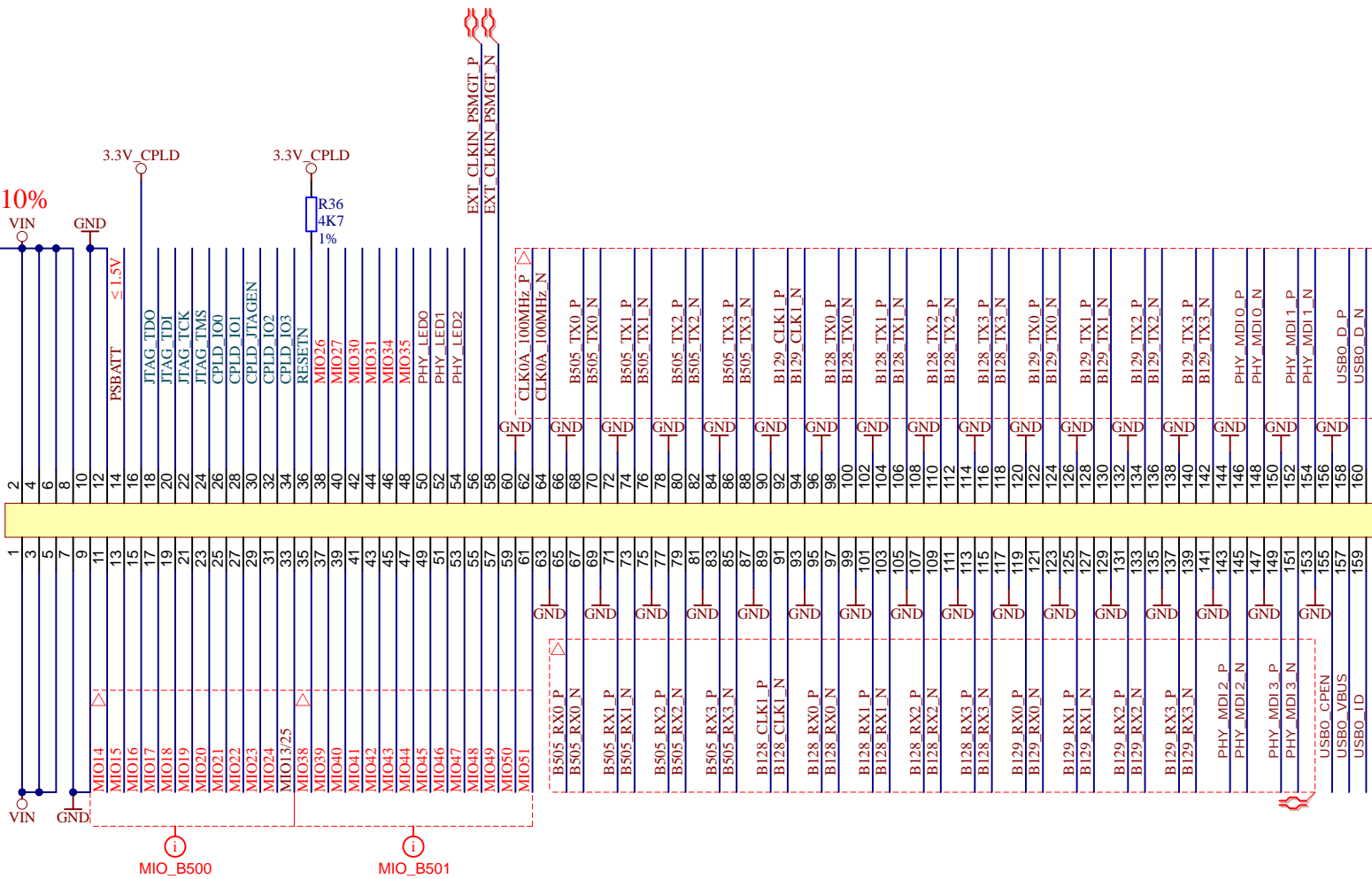


Title: CPLD		
A4	Number: TE0835 NYE21-A	Rev. 02
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Filename: CPLD.SchDoc		

VIN=5V±10%



J1



MIO_B500

MIO_B501

ST5-80-1.50-L-D-P-TR



Title: B2B		
A4	Number: TE0835 NYE21-A	Rev. 02
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B

C

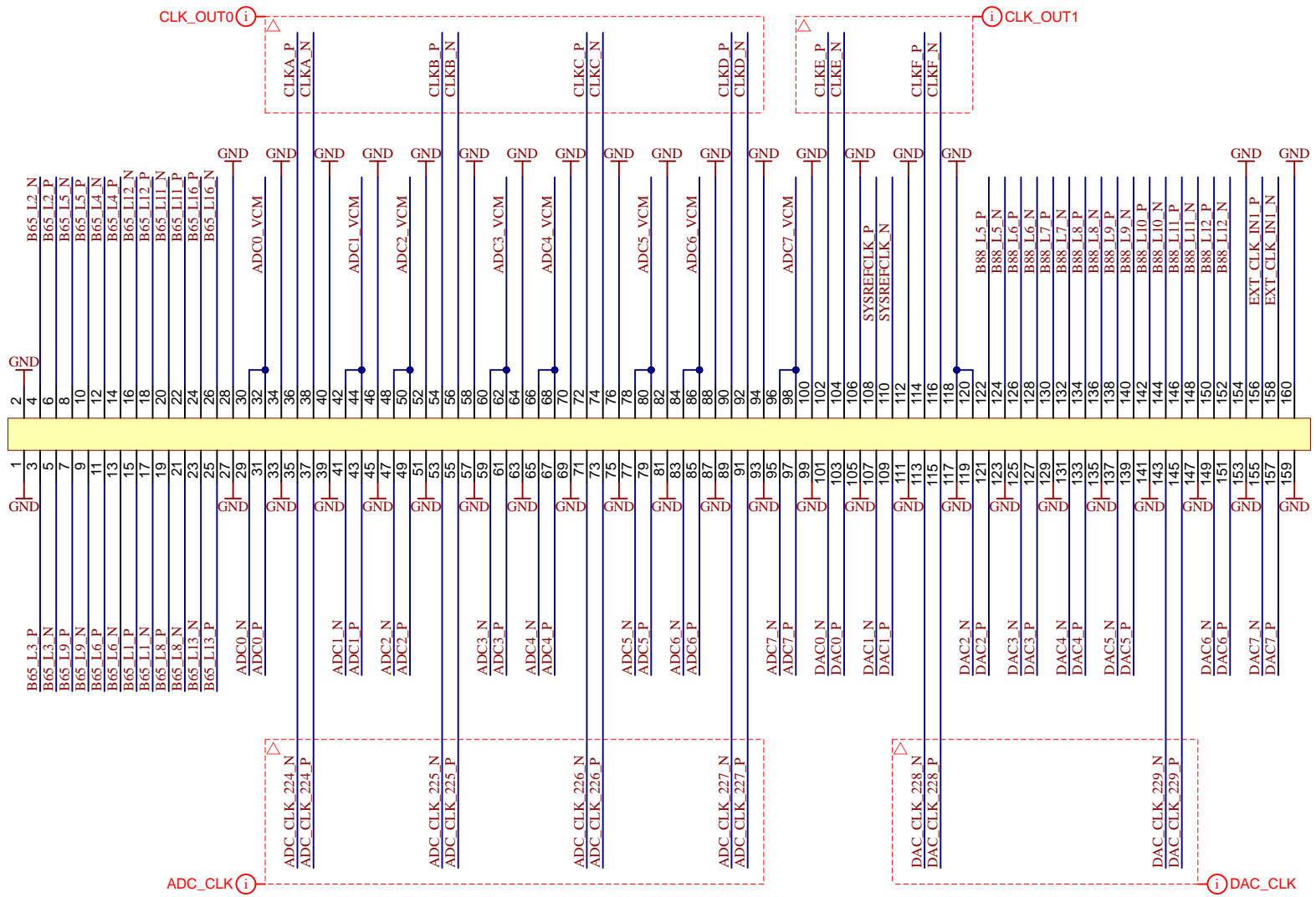
C

D

D

J2

ST5-80-1.50-L-D-P-TR



CLK_OUT0

CLK_OUT1

ADC_CLK

DAC_CLK



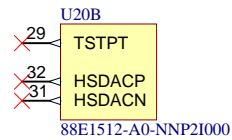
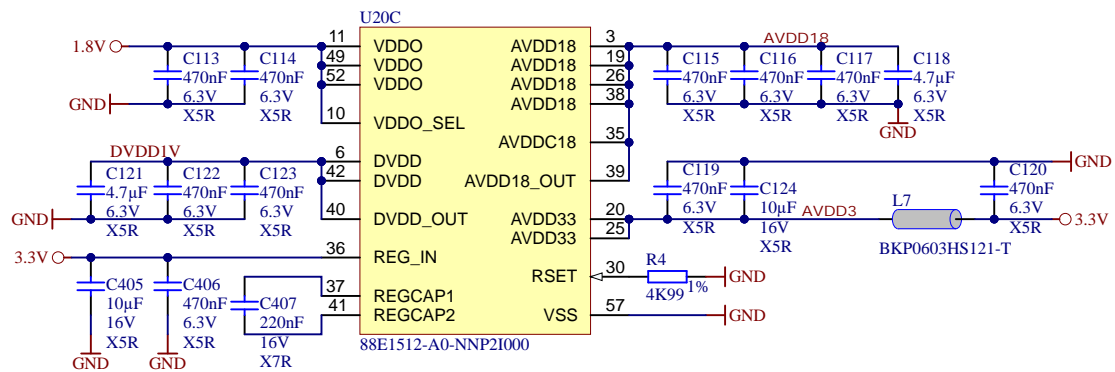
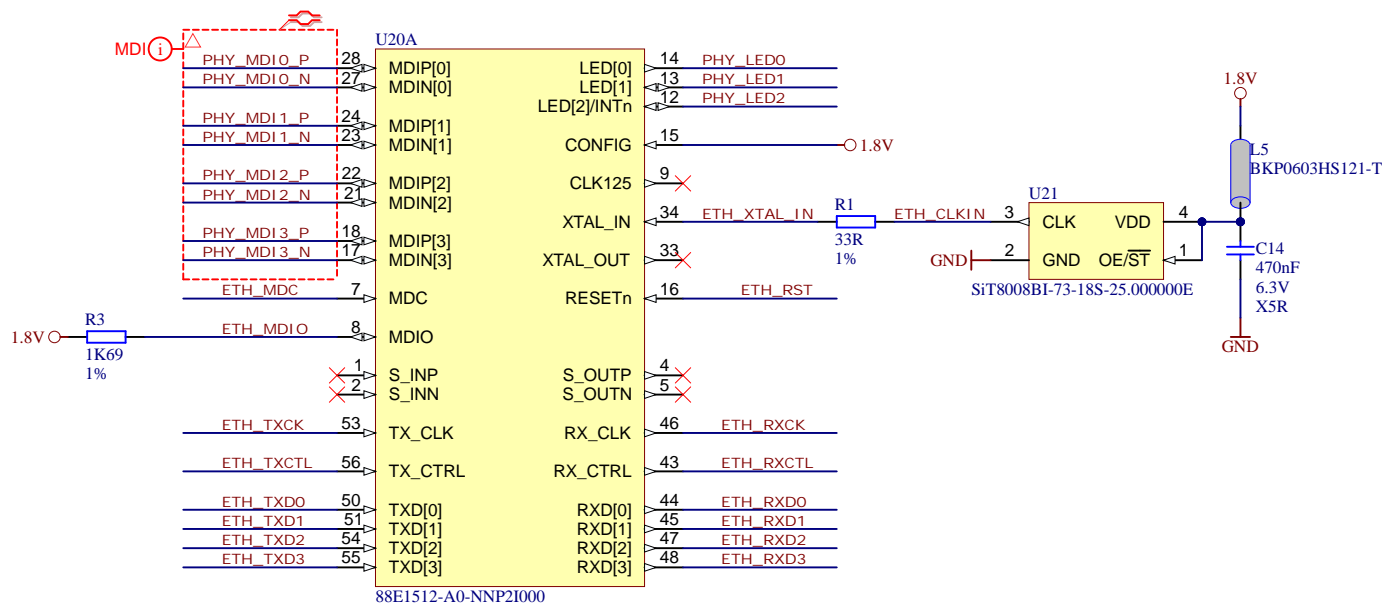
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A4	Number: TE0835 NYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 17 of 34
Filename: B2B_2.SchDoc		

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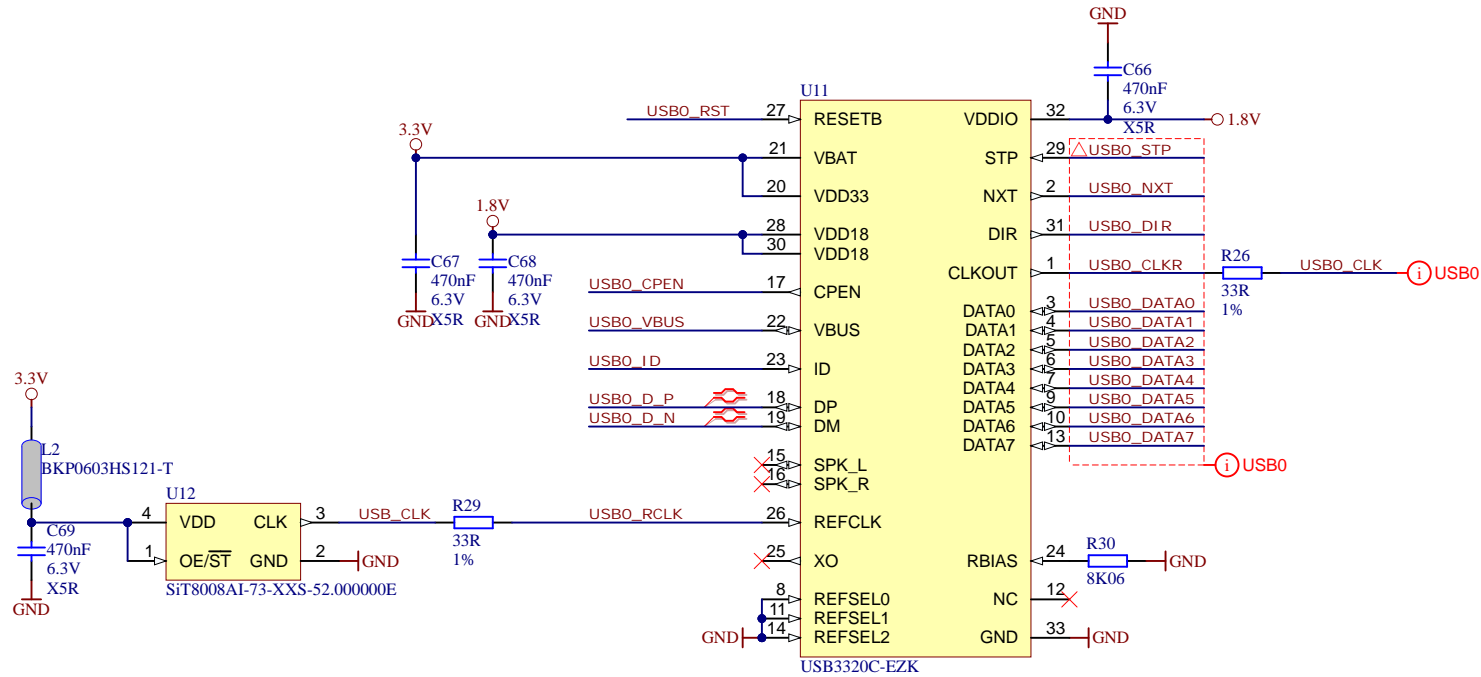
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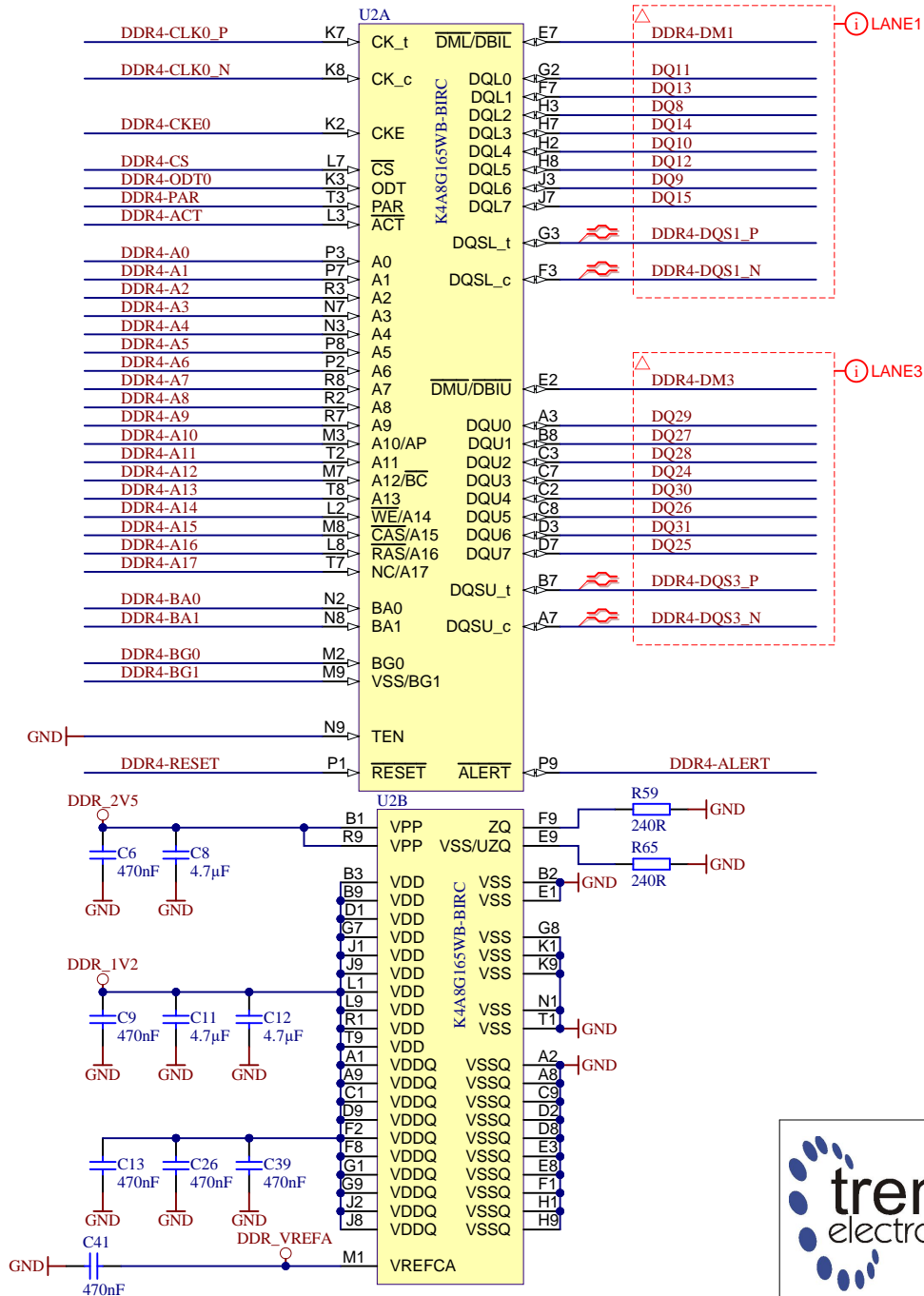

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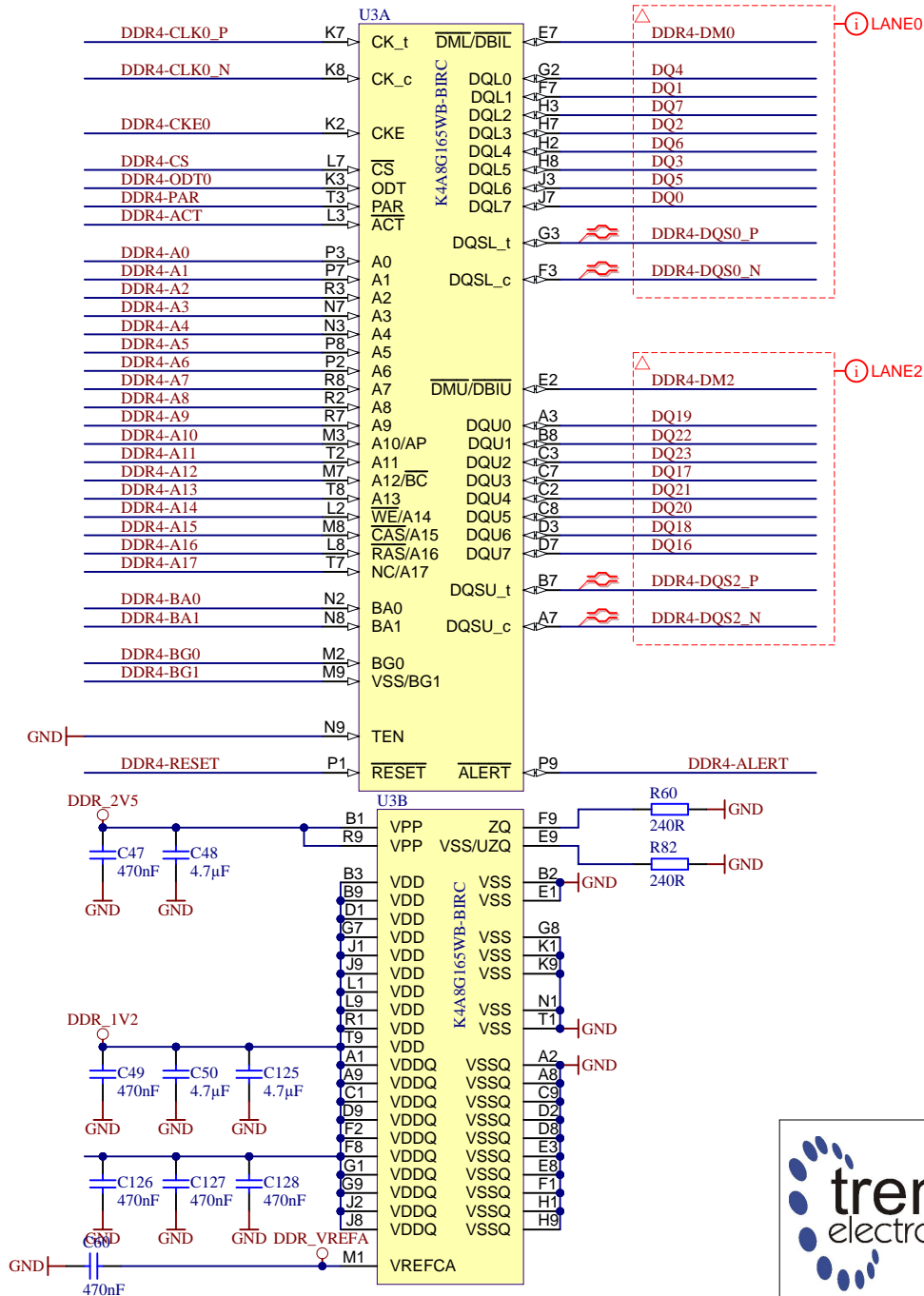
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Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 18 of 34
Filename: Ethernet.SchDoc		



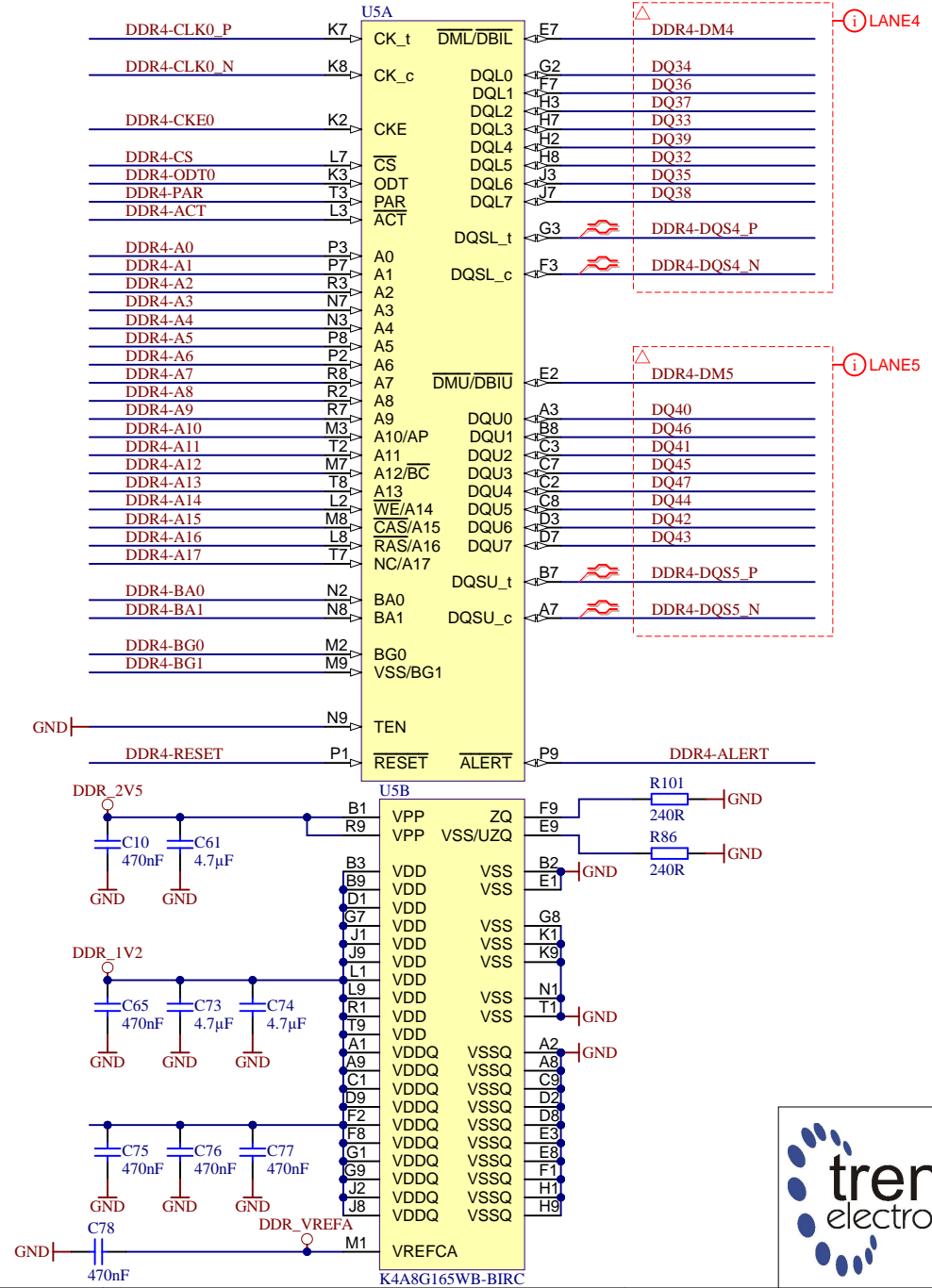
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	Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 19 of 34
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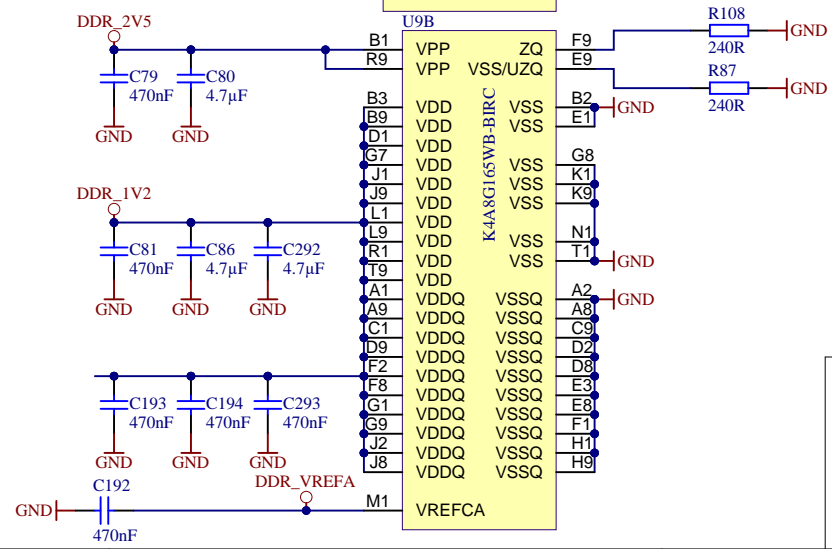
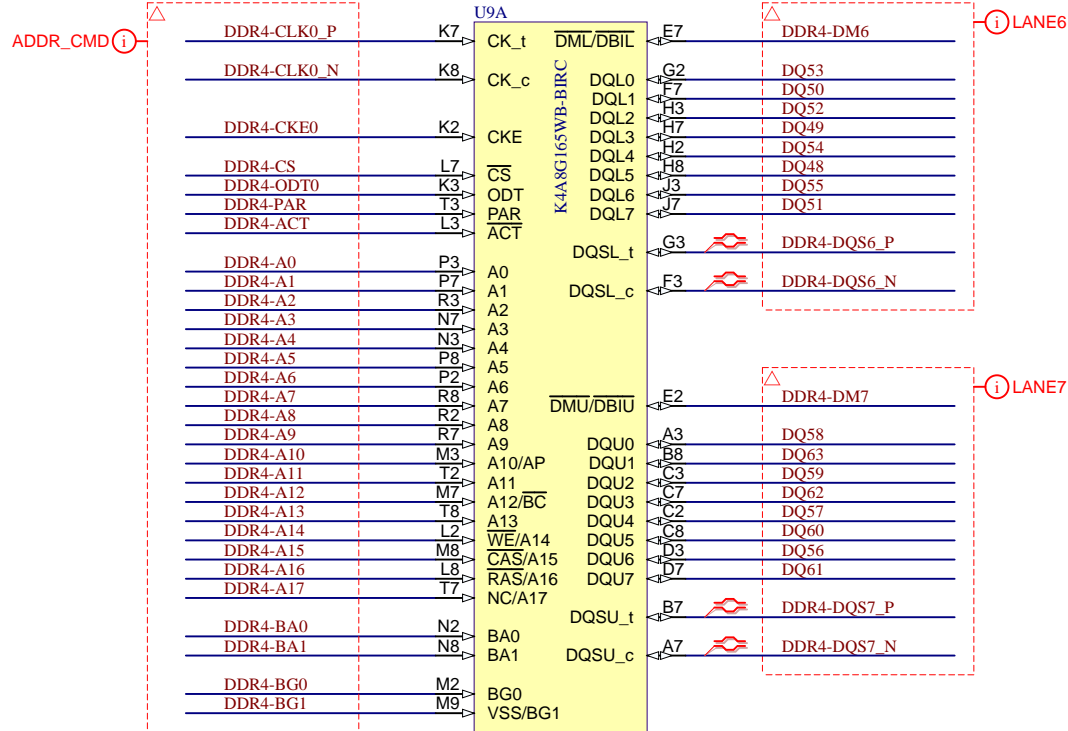
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Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 20 of 34
Filename: DDR4-RAM.SchDoc		



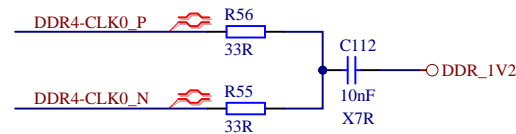
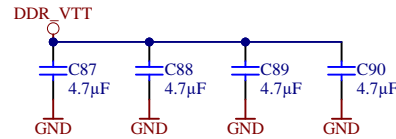
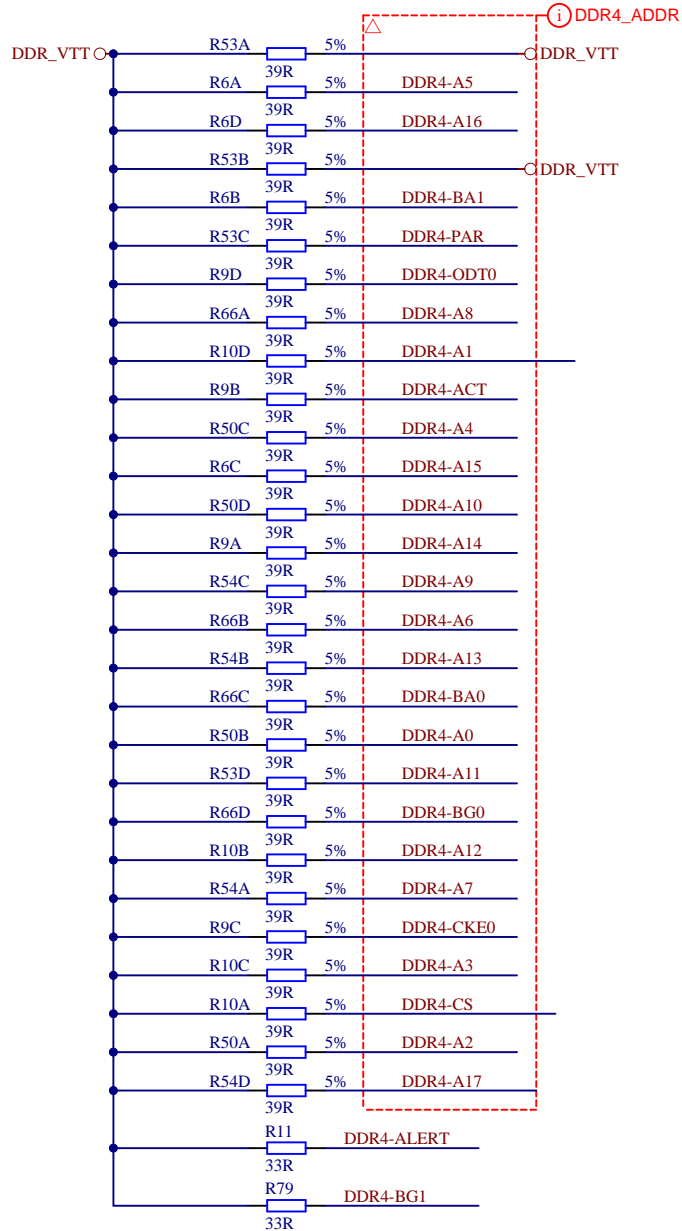
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Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 21 of 34
Filename: DDR4-RAM_2.SchDoc		



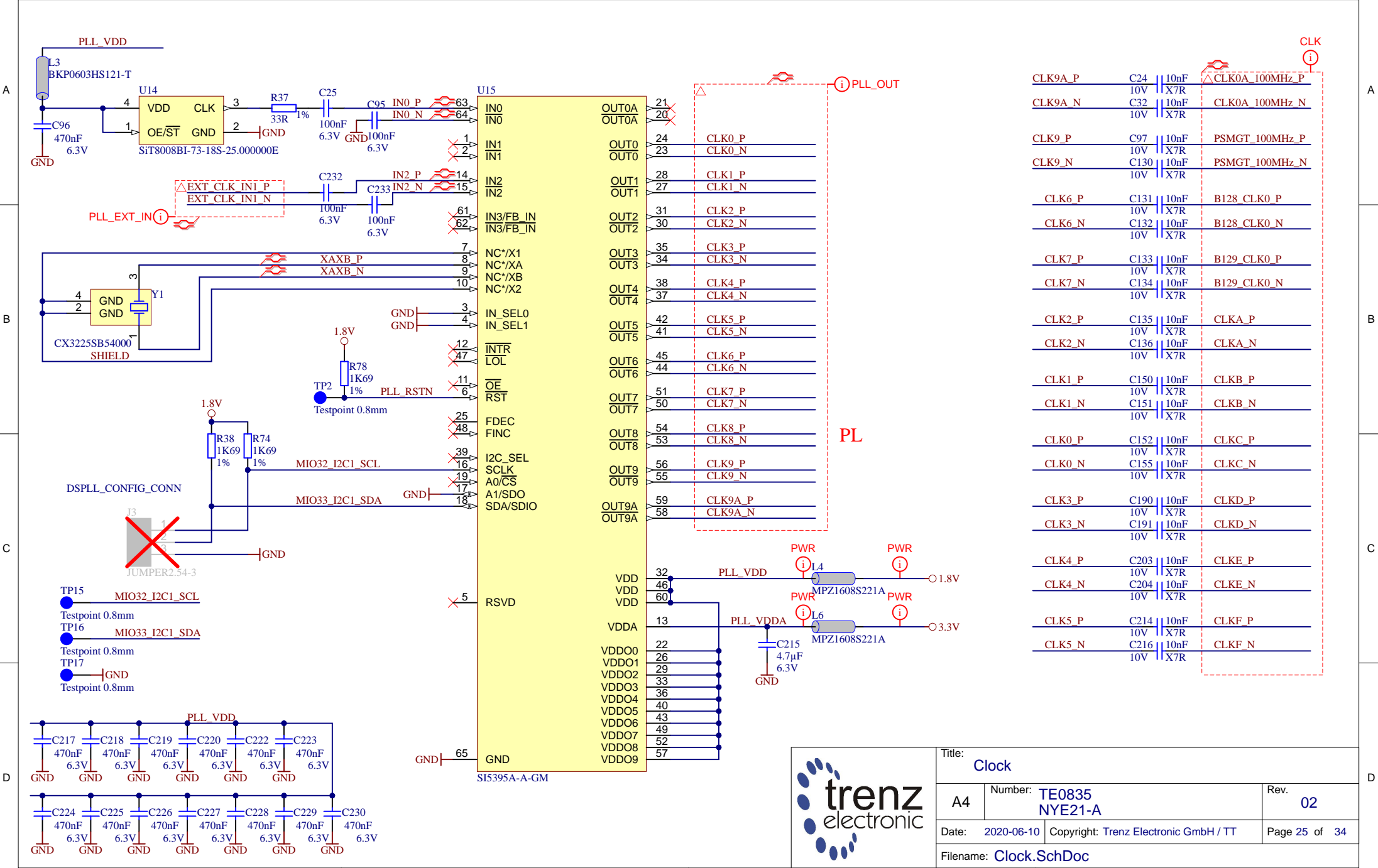
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Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 22 of 34
Filename: DDR4-RAM_3.SchDoc		



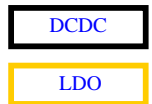
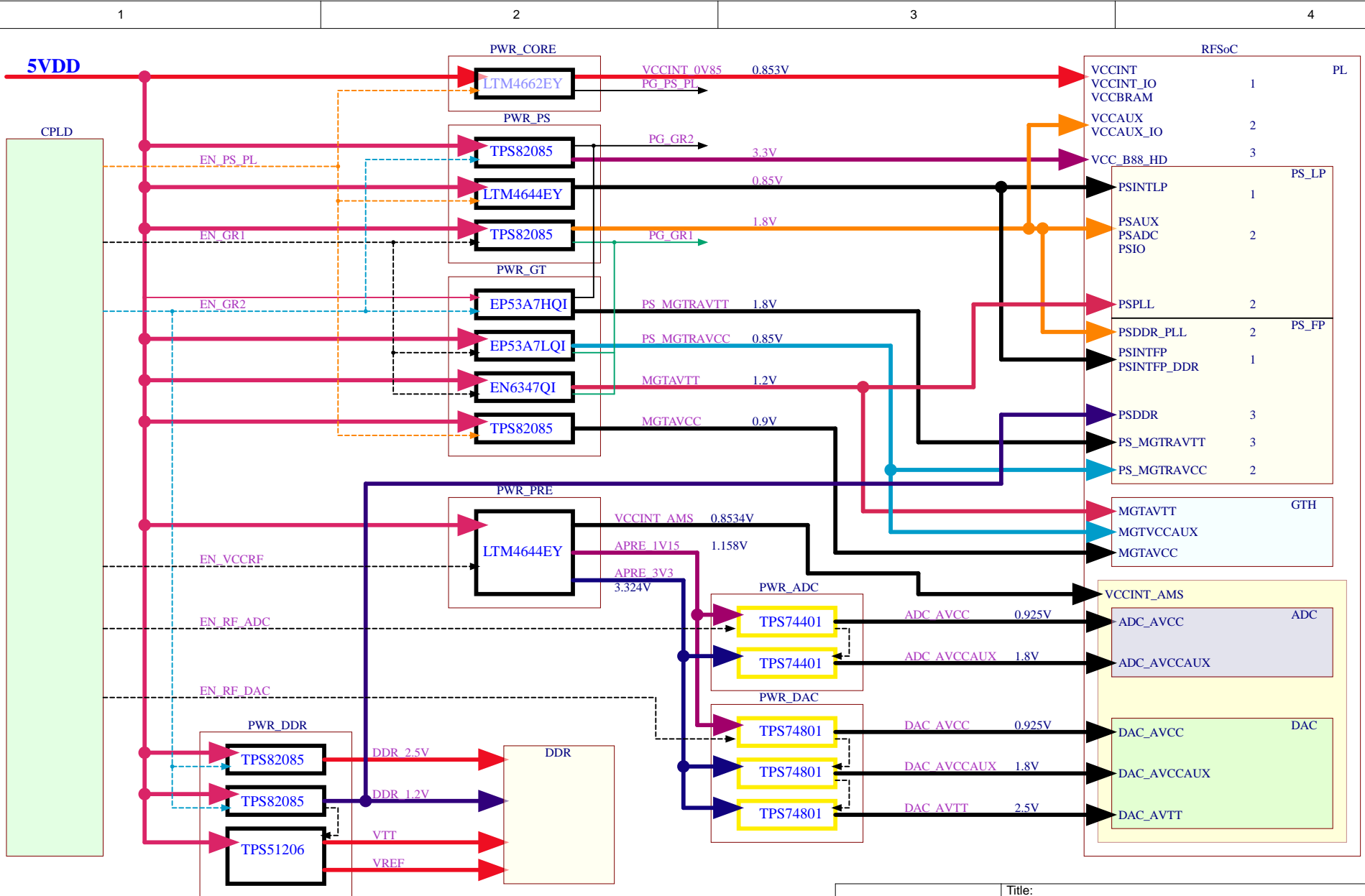
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Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 23 of 34
Filename: DDR4-RAM_4.SchDoc		



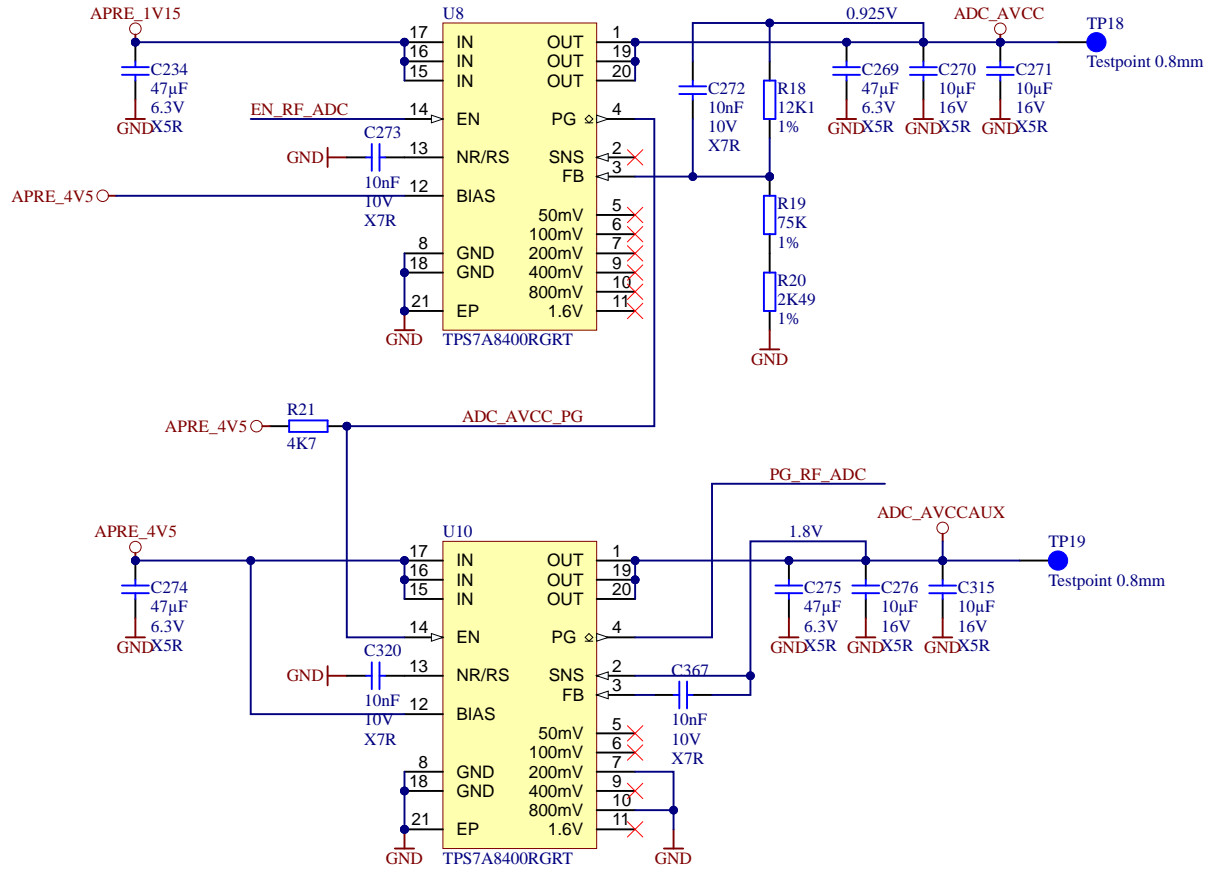
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Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 24 of 34
Filename: DDR4-TERM.SchDoc		




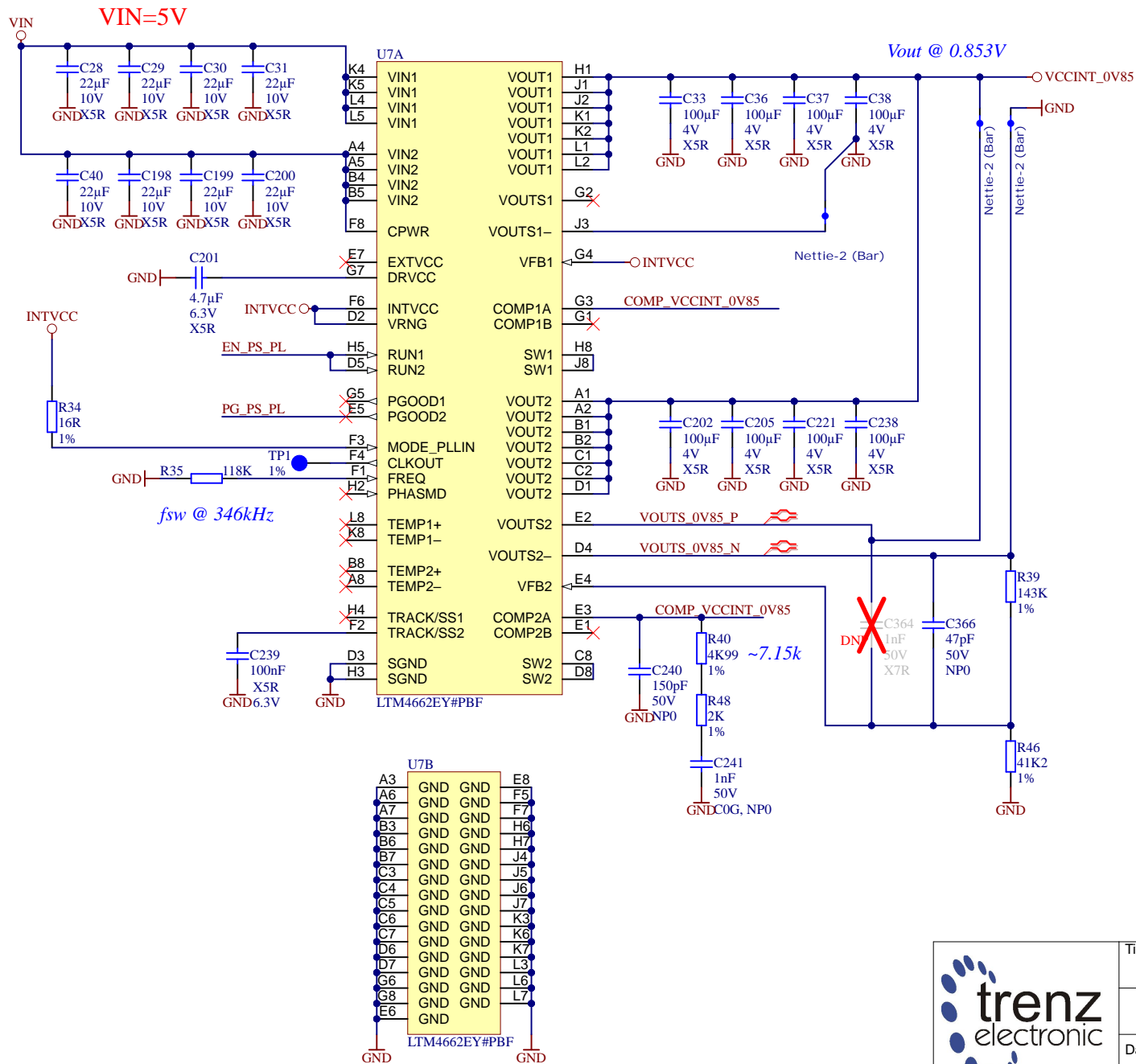
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Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 25 of 34
Filename: Clock.SchDoc		



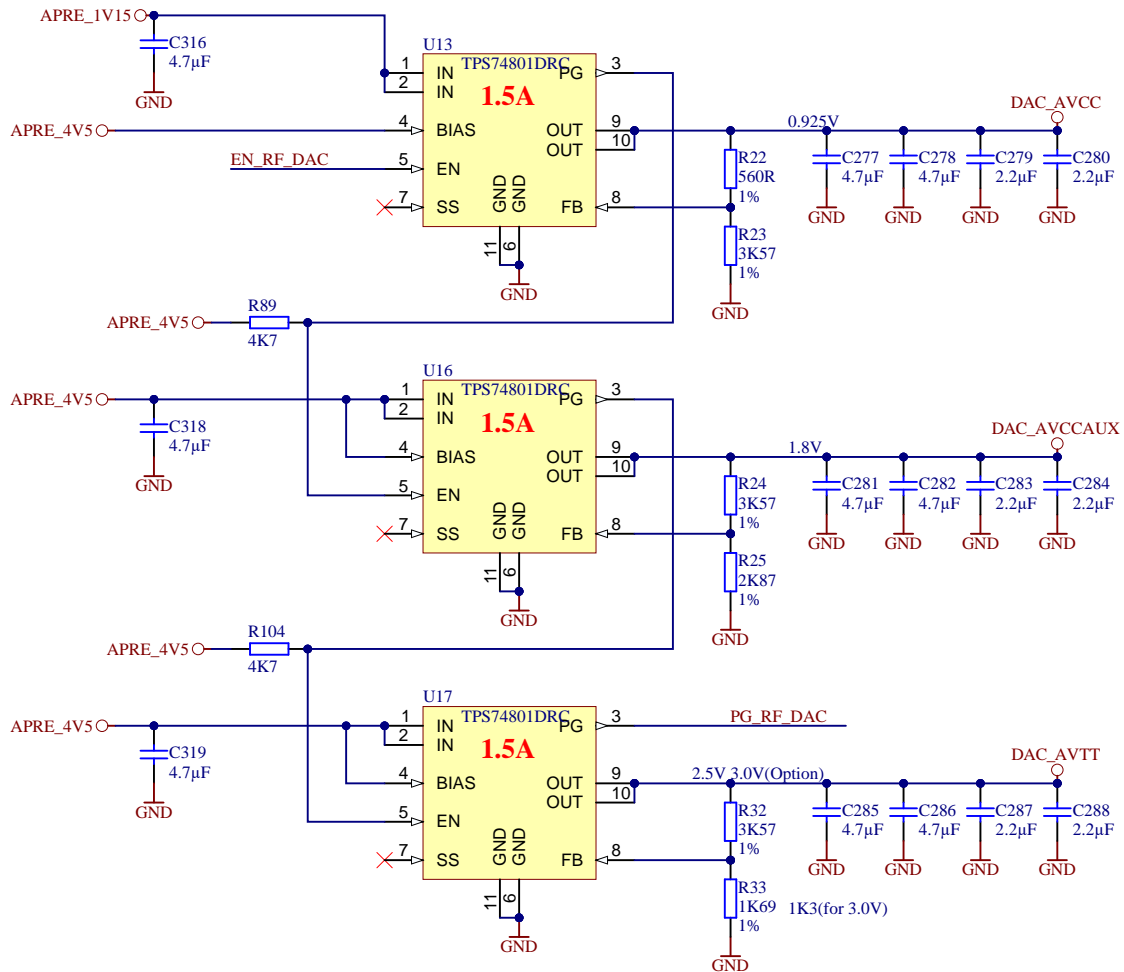
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Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 26 of 34
Filename: PWR_Structure.SchDoc		




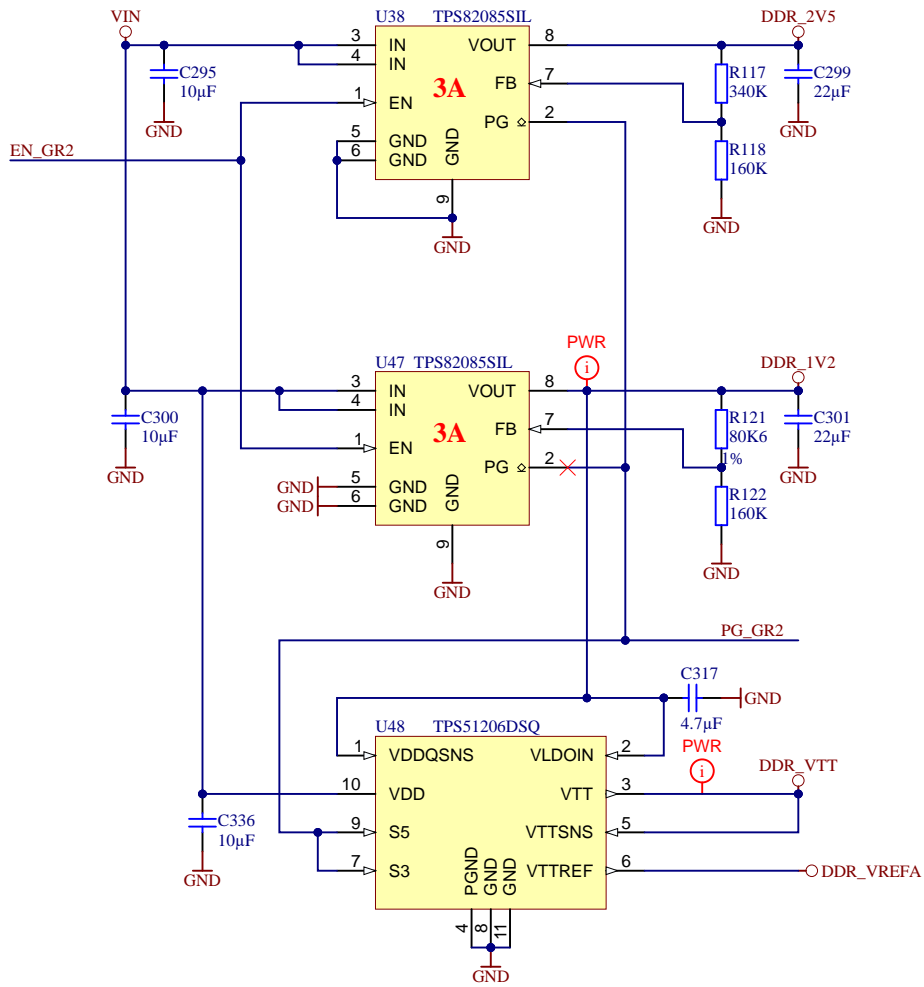
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Date: 2020-06-10		Copyright: Trenz Electronic GmbH		Page 27 of 34
Filename: PWR_ADC.SchDoc				




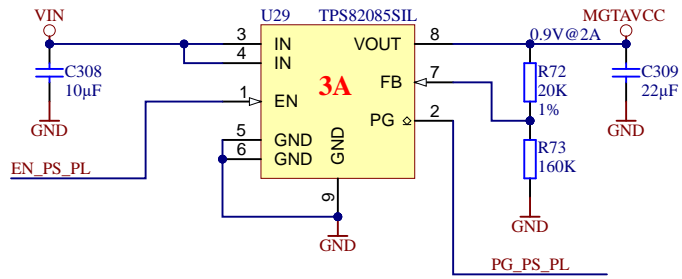
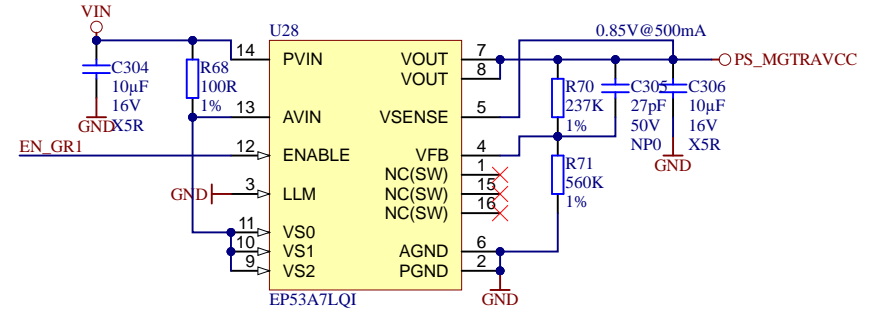
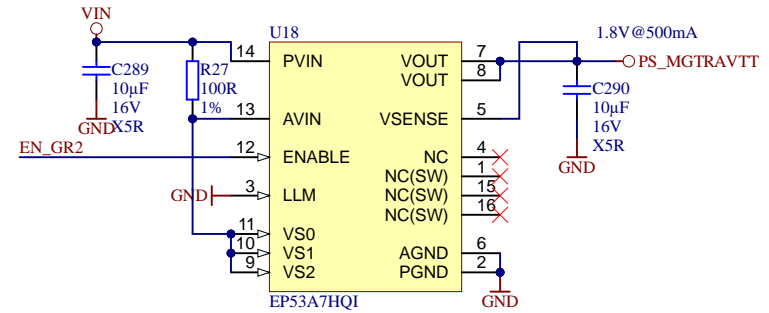
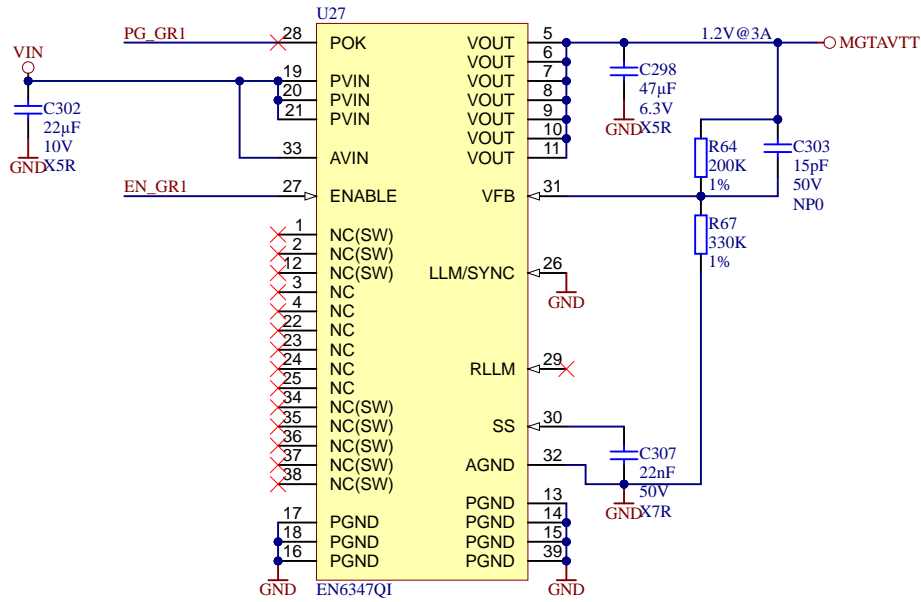
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Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 28 of 34
Filename: PWR_CORE.SchDoc		



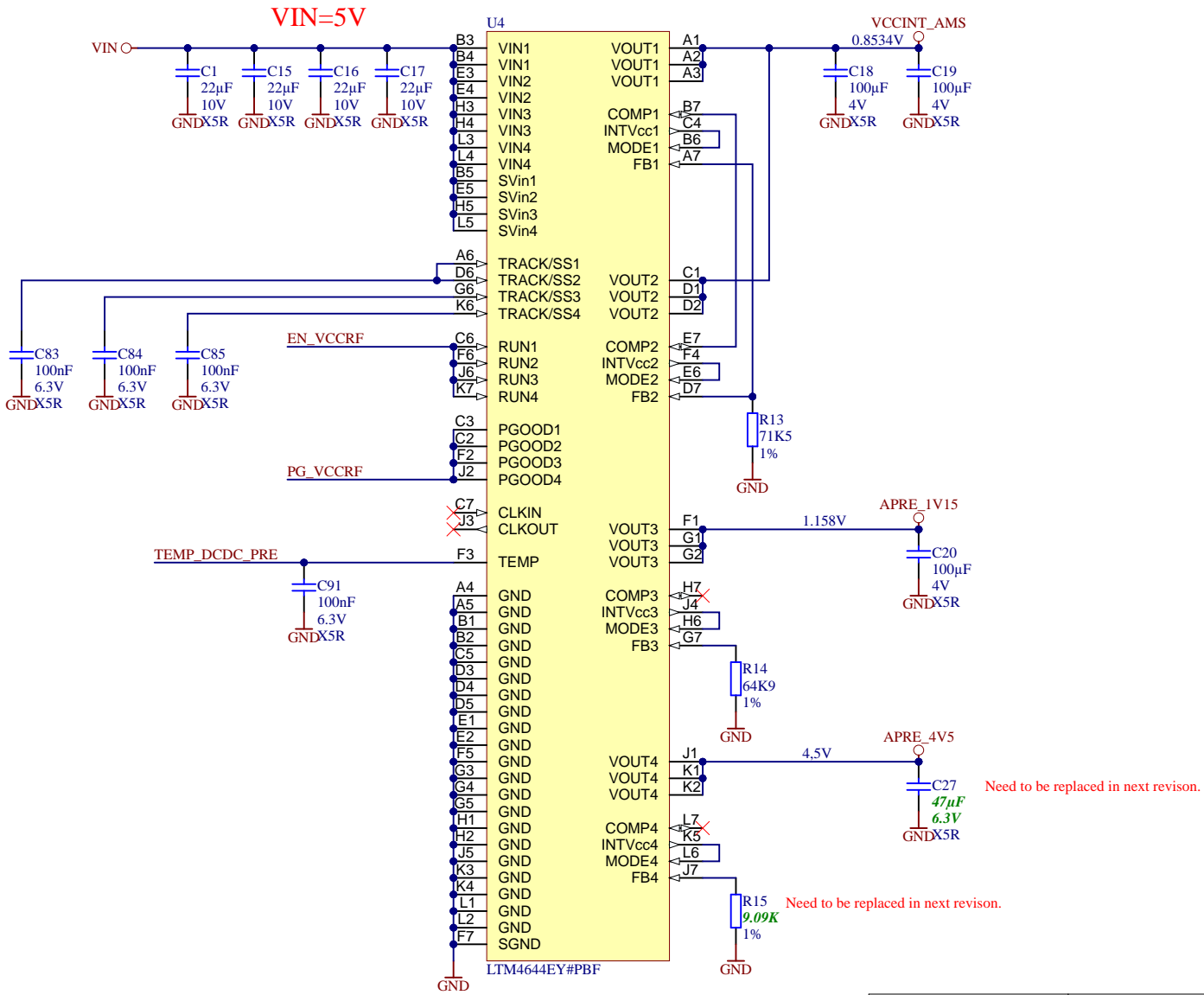
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	Date: 2020-06-10	Copyright: Trenz Electronic GmbH
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Filename: PWR_DAC.SchDoc		




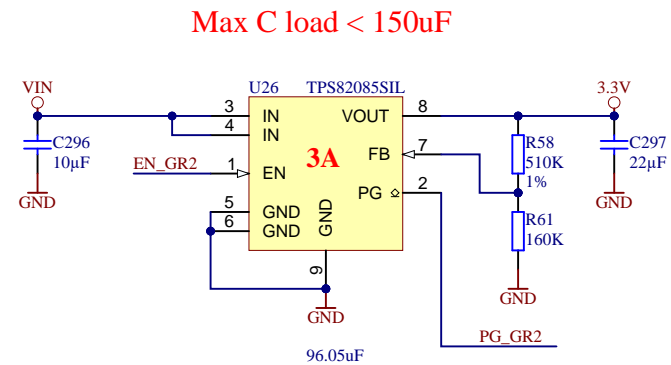
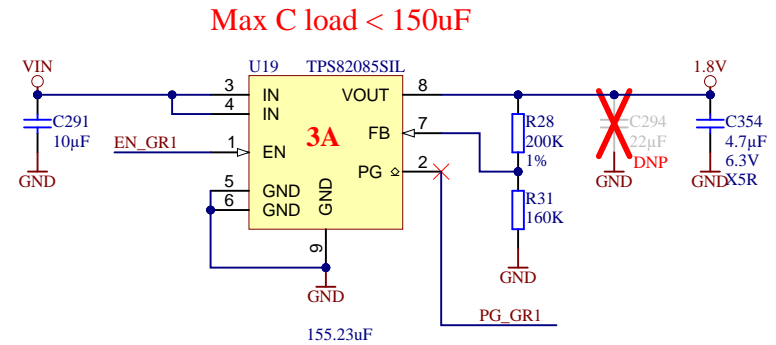
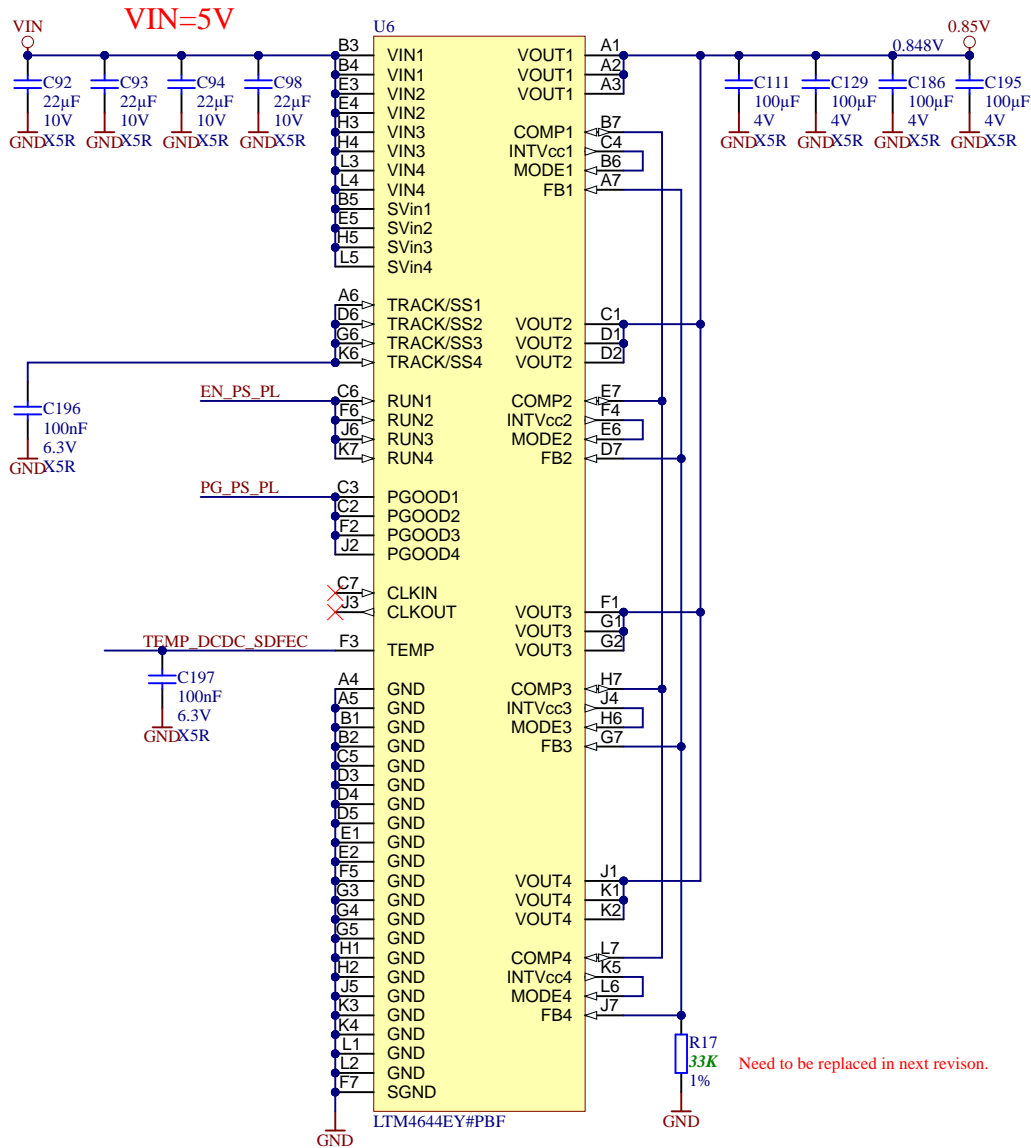
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Date: 2020-06-10		Copyright: Trenz Electronic GmbH	
Filename: PWR_DDR.SchDoc		Page 30 of 34	




Title: PWR_GT		
A4	Number: TE0835 NYE21-A	Rev. 02
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Filename: PWR_GT.SchDoc		



		Title: PWR_PRE	
		A4	Number: TE0835 NYE21-A
Date: 2020-06-10		Copyright: Trenz Electronic GmbH	
Filename: PWR_PRE.SchDoc		Page 32 of 34	



		Title: PWR_PS	
		A4	Number: TE0835 NYE21-A
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Filename: PWR_PS.SchDoc		Page 33 of 34	

REVISION HISTORY

REV	Description	
-01	Initial revision	IG
-02	1. Added a VRP resistor on bank 65; 2. LDO U33 is changed on ADP7102ACPZ; 3. Signal FPGA IO0 is connected on AE18 pin of FPGA; 4. Signal DBG_LED3 is connected on AD18 pin of FPGA; 5. Signal MIO13_25 connected to J1 pin 33 instead MIO25. 6. Resistor R84 is removed; 7. LED D1 moved on edge of PCB; 8. Added THT testpoints J4 on CPLD_JTAGEN, R76 was removed; 9. Signals B49_XX_X are renamed in B88_XX_X; 10. C241 is changed on 1nF; 11. Length of CLK signals on RFADC and RFDAC are adjusted; 12. Wrong connection on U8 is fixed (PCB); 13. Wrong connection PGOOD1 pin of U7 is fixed; 14. R17 is changed from 35,5K to 33K for VCC_PL_PS correction.	IG
	15. APRE_3V3 ranamed to APRE_4V5, voltage of the power rail incised from 3.3V to 4,58V. 16. Resistor R15 is changed from 13,3K to 9,09K. AN: 24671->25969 17. Capasitor C27 is changed from 100uF x 4V to 47uF x 6,3V. AN: 28940->24718	IG

A

A

B


B

C

C

D

D

	Title: Revision_Changes		
	A4	Number: TE0835 NYE21-A	Rev. 02
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	Filename: Revision_Changes.SchDoc		