U_Clock
Clock.SchDoc

U_DDR4-RAM
DDR4-RAM.SchDoc

U_DDR4-RAM_2
DDR4-RAM_2.SchDoc

U_DDR4-RAM_3
DDR4-RAM_3.SchDoc

U_DDR4-RAM_4
DDR4-RAM_4.SchDoc

U_DDR4-TERM
DDR4-TERM.SchDoc

CPLD
CPLD.SchDoc

U_ZU
ZU.SchDoc

U_USB-PHY
USB-PHY.SchDoc

U_Ethernet
Ethernet.SchDoc

U_B2B
B2B.SchDoc

U_B2B_2
B2B_2.SchDoc

PWR_Structure
PWR_Structure.SchDoc

GND Mount.Hole 3.2mm für Unterlegscheibe

GND Mount.Hole 3.2mm für Unterlegscheibe

GND Mount.Hole 3.2mm für Unterlegscheibe

GND Mount.Hole 3.2mm für Unterlegscheibe

GND Mount.Hole 3.2mm für Unterlegscheibe

GND Mount.Hole 3.2mm für Unterlegscheibe

GND Mount.Hole 3.2mm für Unterlegscheibe

GND Mount.Hole 3.2mm für Unterlegscheibe

LOGO1

TE Logo PRINT Layer

LOGO PRINT

Serial

Serial

Serialnumber 6,3 x 6.3mm

PM1 FIDU-DOT - mini

PM2 FIDU-DOT - mini

PM3 FIDU-DOT - mini

PM4 FIDU-DOT - mini

PM5 FIDU-DOT - mini

PM6 FIDU-DOT - mini

| | |
|---|---|
| Design drawn by: | IG |
| Checked by: | MR |
| Assembly variant: | TXE21-A |
| Created by: | |
| Modified by: | |
| Modified at: | |

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| | | |
|---|---|---|
| Title: TE0835 | | |
| A4 | Number: TE0835 TXE21-A | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH / TT | Page 1 of 34 |
| Filename: TE0835.SchDoc | | |

HD
ZU_HD.SchDoc

MGT_L
ZU_MGT_L.SchDoc

ZU_B65_B66
ZU_B65_B66.SchDoc

MIO
ZU_MIO.SchDoc

PSDDR
ZU_PSDDR.SchDoc

ZU_PWR
ZU_PWR.SchDoc

ZU_PWR2
ZU_PWR2.SchDoc

ZU_PWR3
ZU_PWR3.SchDoc

ZU_ADC
ZU_ADC.SchDoc

ZU_DAC
ZU_DAC.SchDoc

ZU_CFG
ZU_CFG.SchDoc

ZU_PSMGT
ZU_PSMGT.SchDoc

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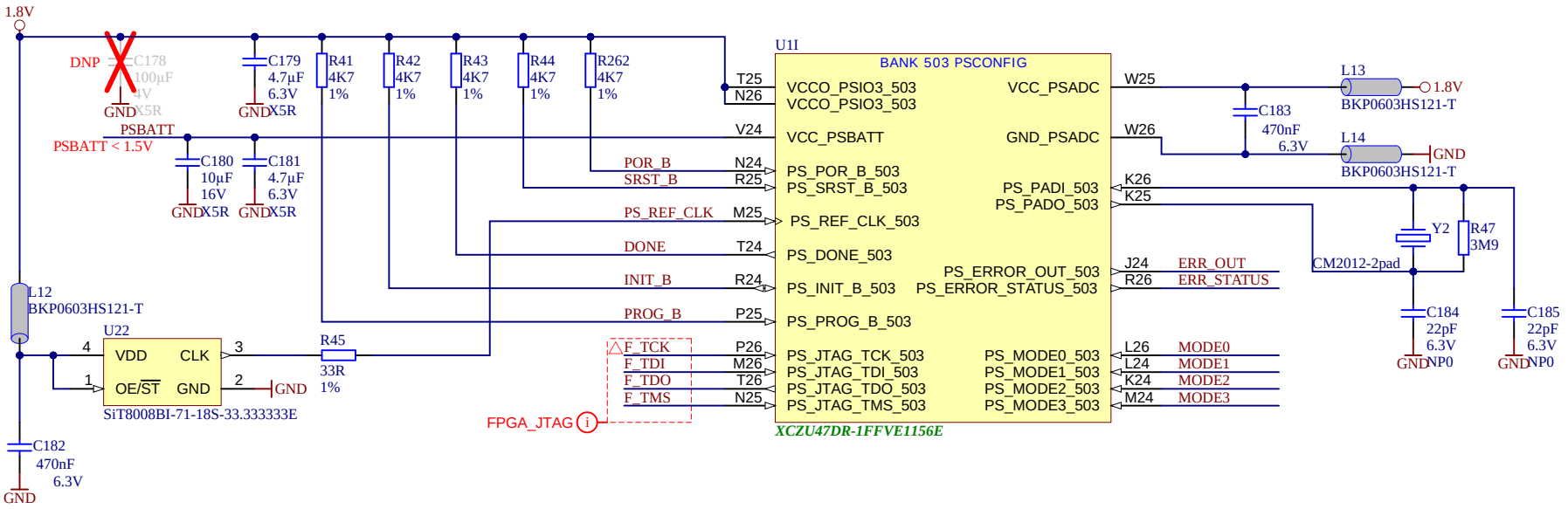
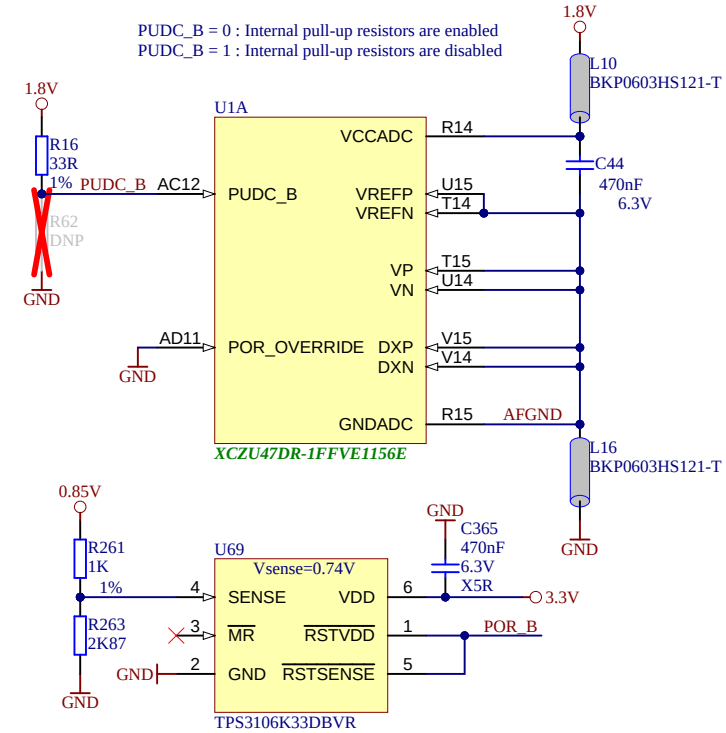
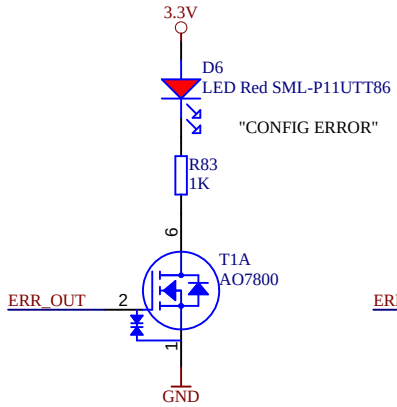
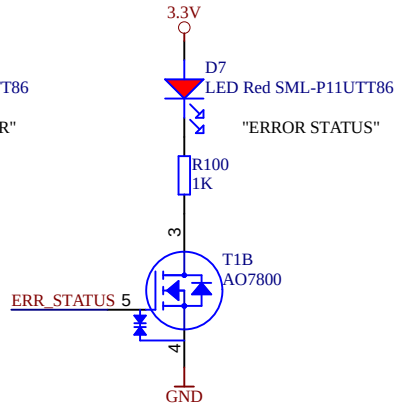
| | | |
|---|---|---|
| Title: ZU | | |
| A4 | Number: TE0835 TXE21-A | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | Page 2 of 34 |
| Filename: ZU.SchDoc | | |

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|---|---|---|---|
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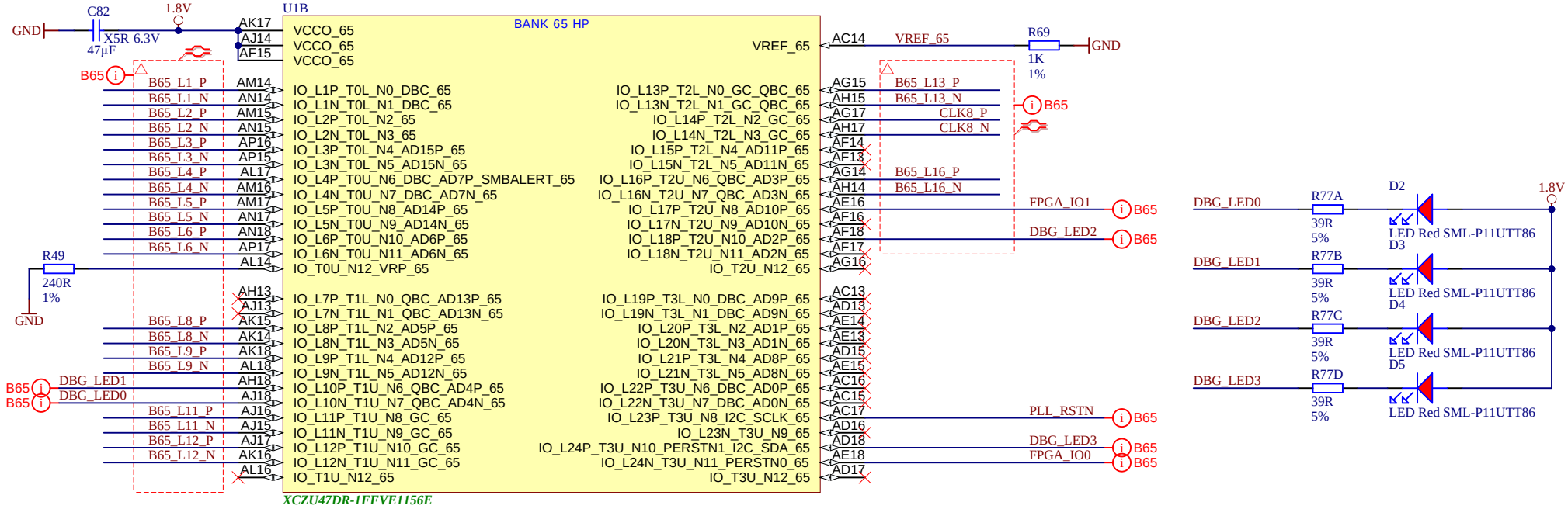
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | | Page 3 of 34 |
| Filename: ZU_CFG.SchDoc | | | |

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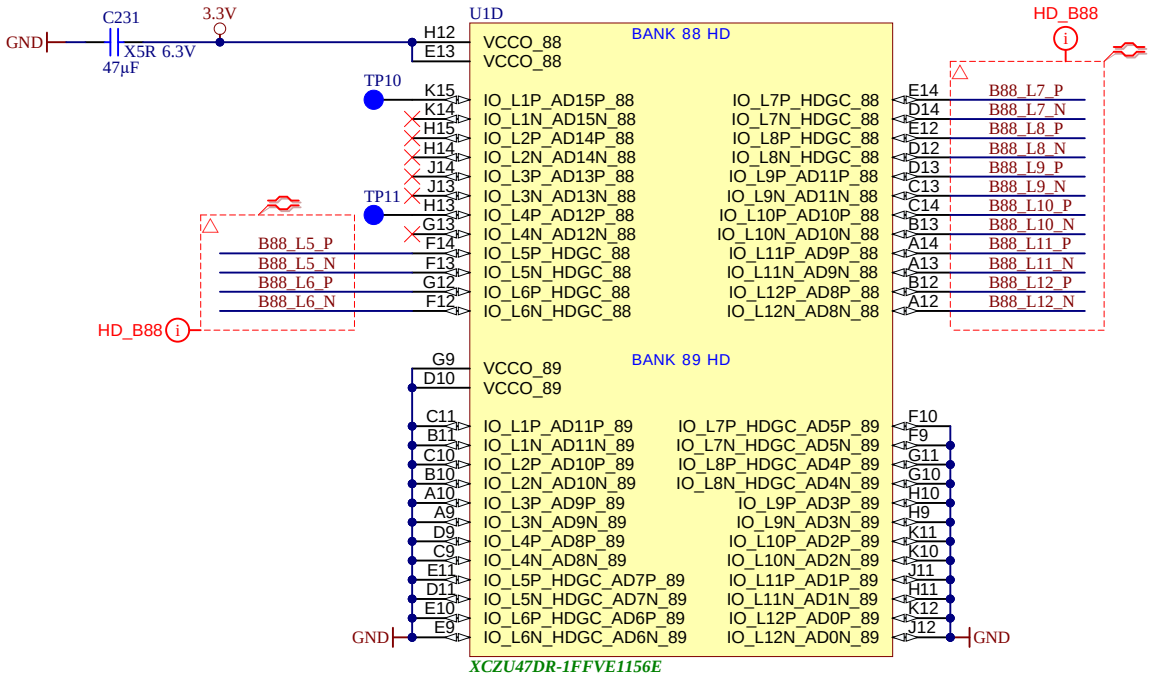
|---|---|---|---|
| Title: ZU_B65_B66 | | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | | Page 4 of 34 |
| Filename: ZU_B65_B66.SchDoc | | | |

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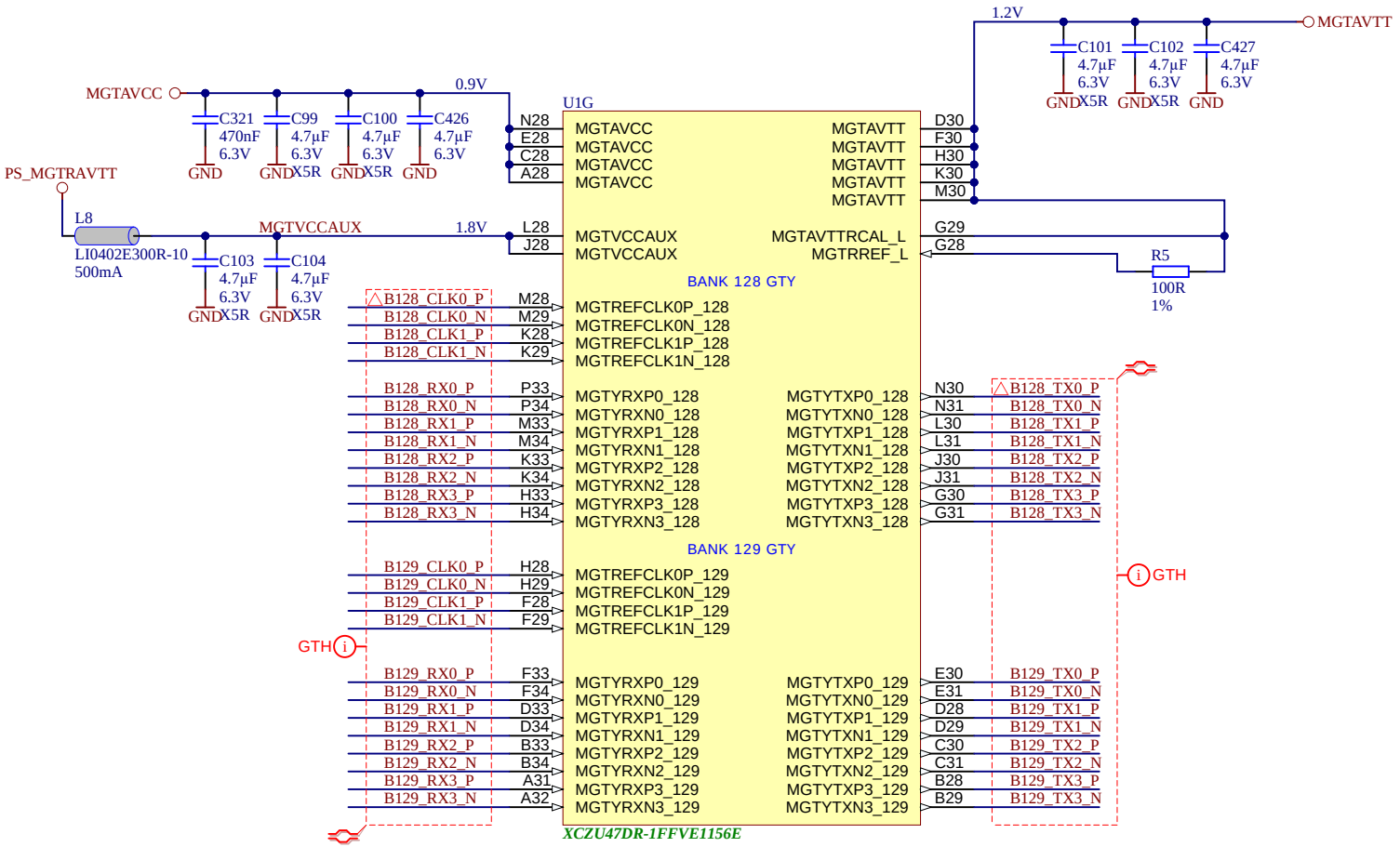
|---|---|---|---|
| Title: ZU_HD | | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | | Page 5 of 34 |
| Filename: ZU_HD.SchDoc | | | |

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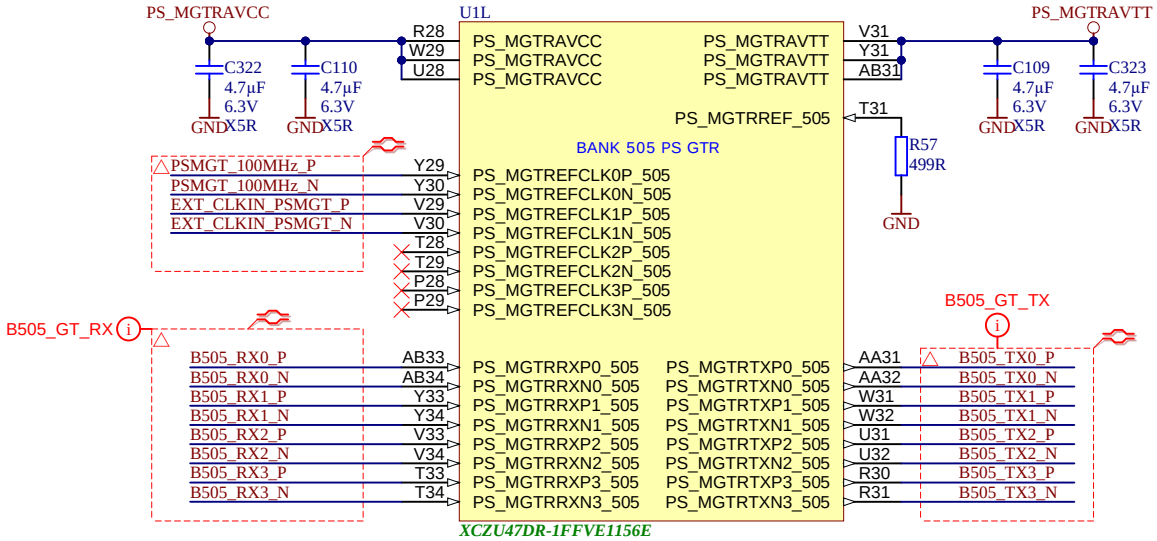
| trenz electronic | Title: ZU_MGT_L | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | | Page 6 of 34 |
| Filename: ZU_MGT_L.SchDoc | | | |

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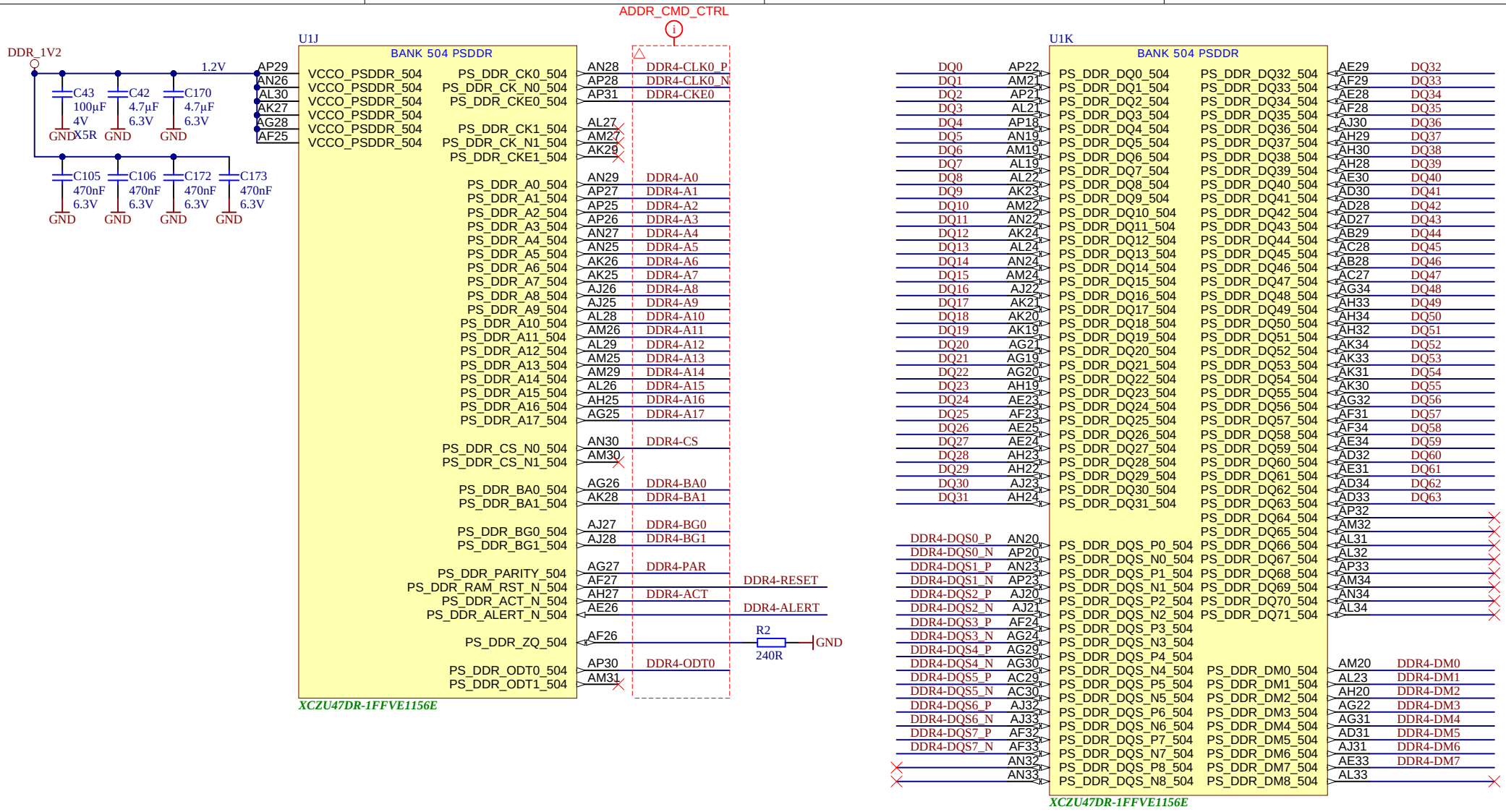
|---|---|---|---|
| trenz electronic | Title: ZU_PSMGT | | |
| | A4 | Number: TE0835 TXE21-A | Rev. 02 |
| | Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | Page 7 of 34 |
| | Filename: ZU_PSMGT.SchDoc | | |

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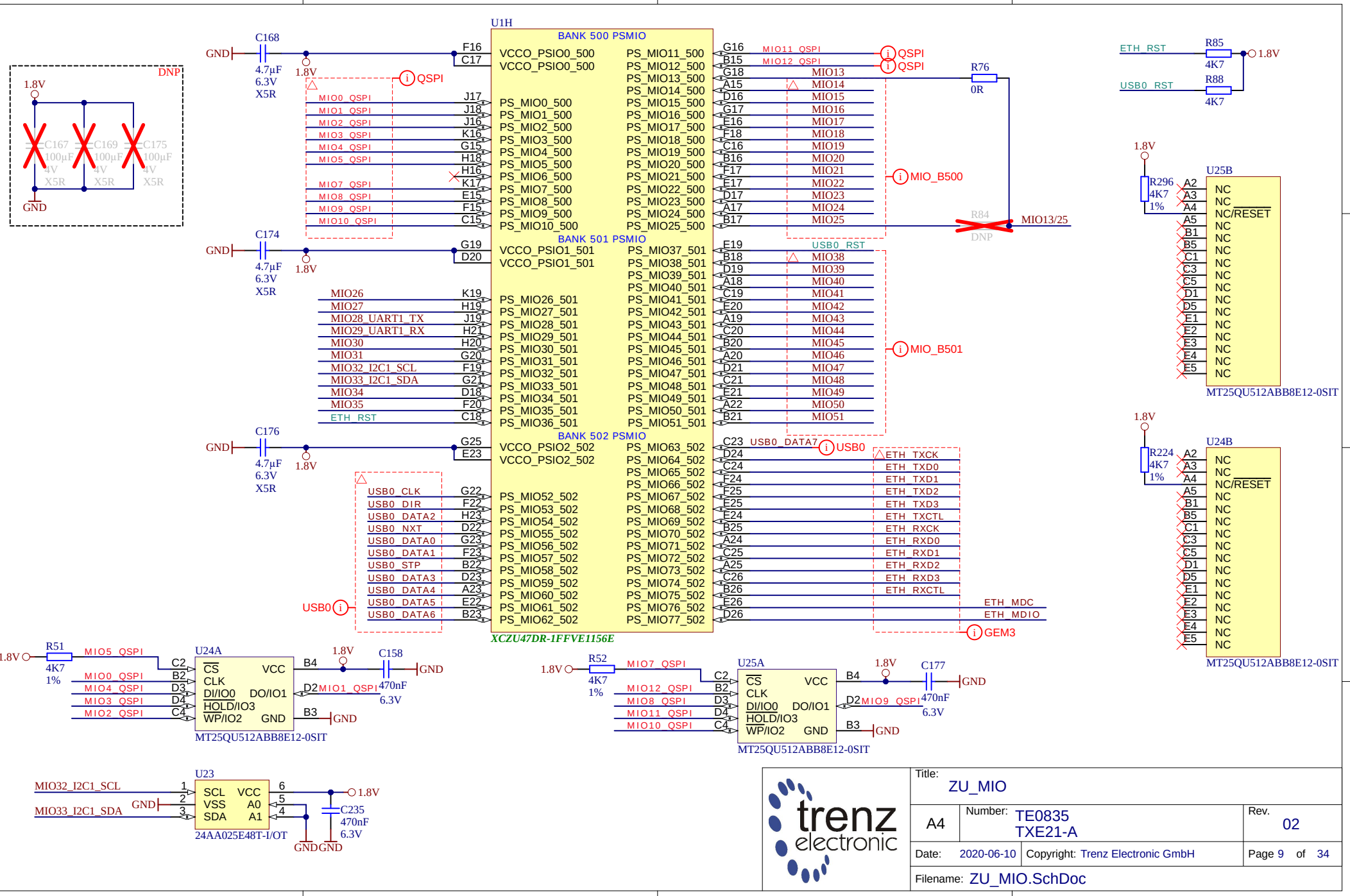
|---|---|
| Title: | ZU_PSDDR |
| A4 | Number: TE0835 TXE21-A |
| Rev. | 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH |
| Page 8 of 34 | |
| Filename: | ZU_PSDDR.SchDoc |


U1H
BANK 500 PSMIO
BANK 501 PSMIO
BANK 502 PSMIO
XCZU47DR-1FFVE1156E
C168
C174
C176
4.7µF
6.3V
X5R
1.8V
GND
DNP
C167
C169
C175
100µF
4V
X5R
QSPI
MIO_B500
MIO_B501
R76
0R
R84
MIO13/25
R85
R88
4K7
ETH_RST
USB0_RST
U25B
U24B
R296
R224
1%
MT25QU512ABB8E12-0SIT
U24A
U25A
R51
R52
C158
C177
470nF
6.3V
U23
24AA025E48T-I/OT
C235
USB0
GEM3
ETH_MDC
ETH_MDIO
Title: ZU_MIO
A4
Number: TE0835 TXE21-A
Rev. 02
Date: 2020-06-10
Copyright: Trenz Electronic GmbH
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Filename: ZU_MIO.SchDoc
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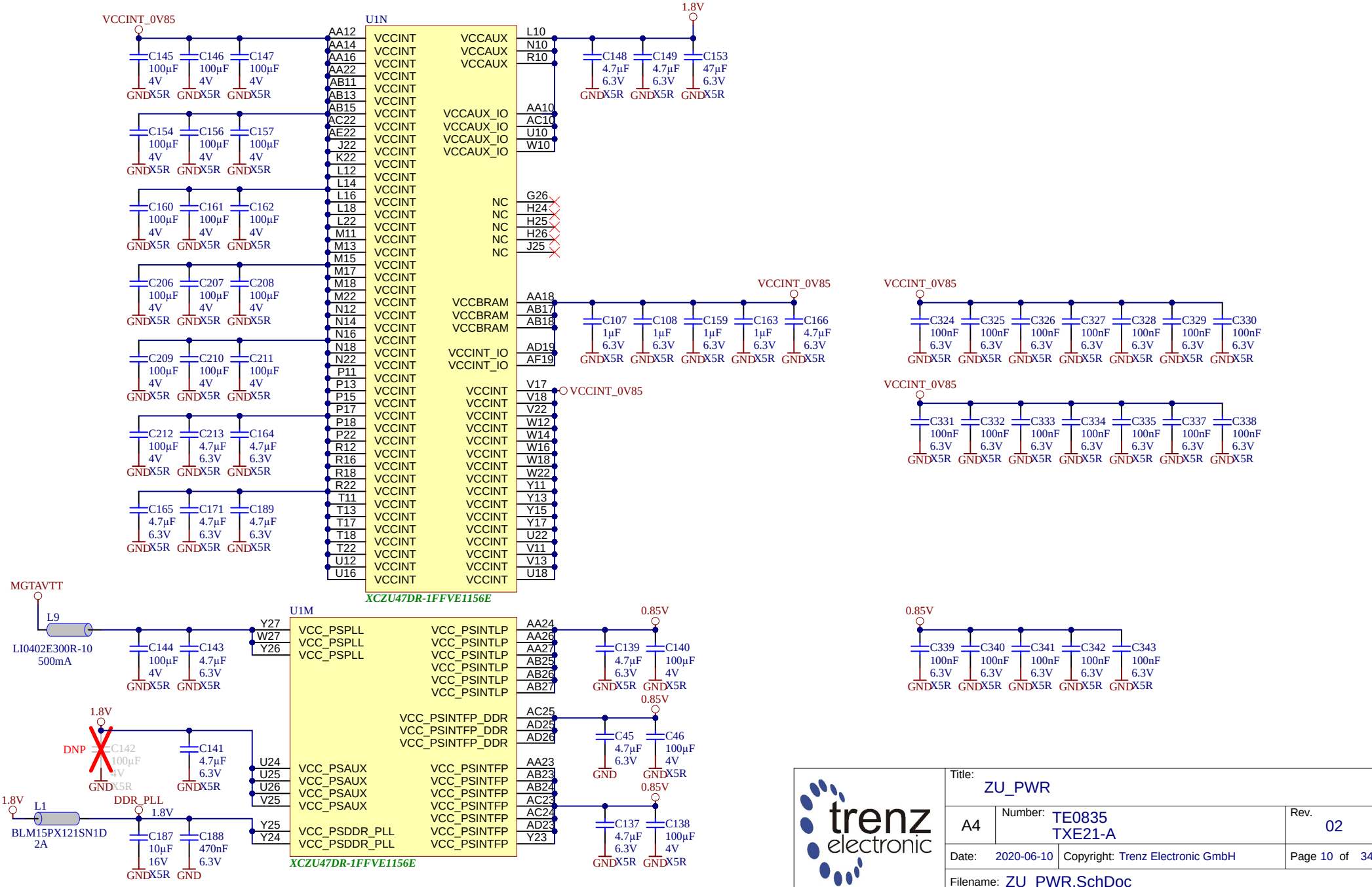
VCCINT_0V85
U1N
XCZU47DR-1FFVE1156E
1.8V
0.85V
MGTAVTT
L9
LI0402E300R-10
500mA
U1M
XCZU47DR-1FFVE1156E
DNP
DDR_PLL
L1
BLM15PX121SN1D
2A
Title: ZU_PWR
A4
Number: TE0835 TXE21-A
Rev. 02
Date: 2020-06-10
Copyright: Trenz Electronic GmbH
Page 10 of 34
Filename: ZU_PWR.SchDoc
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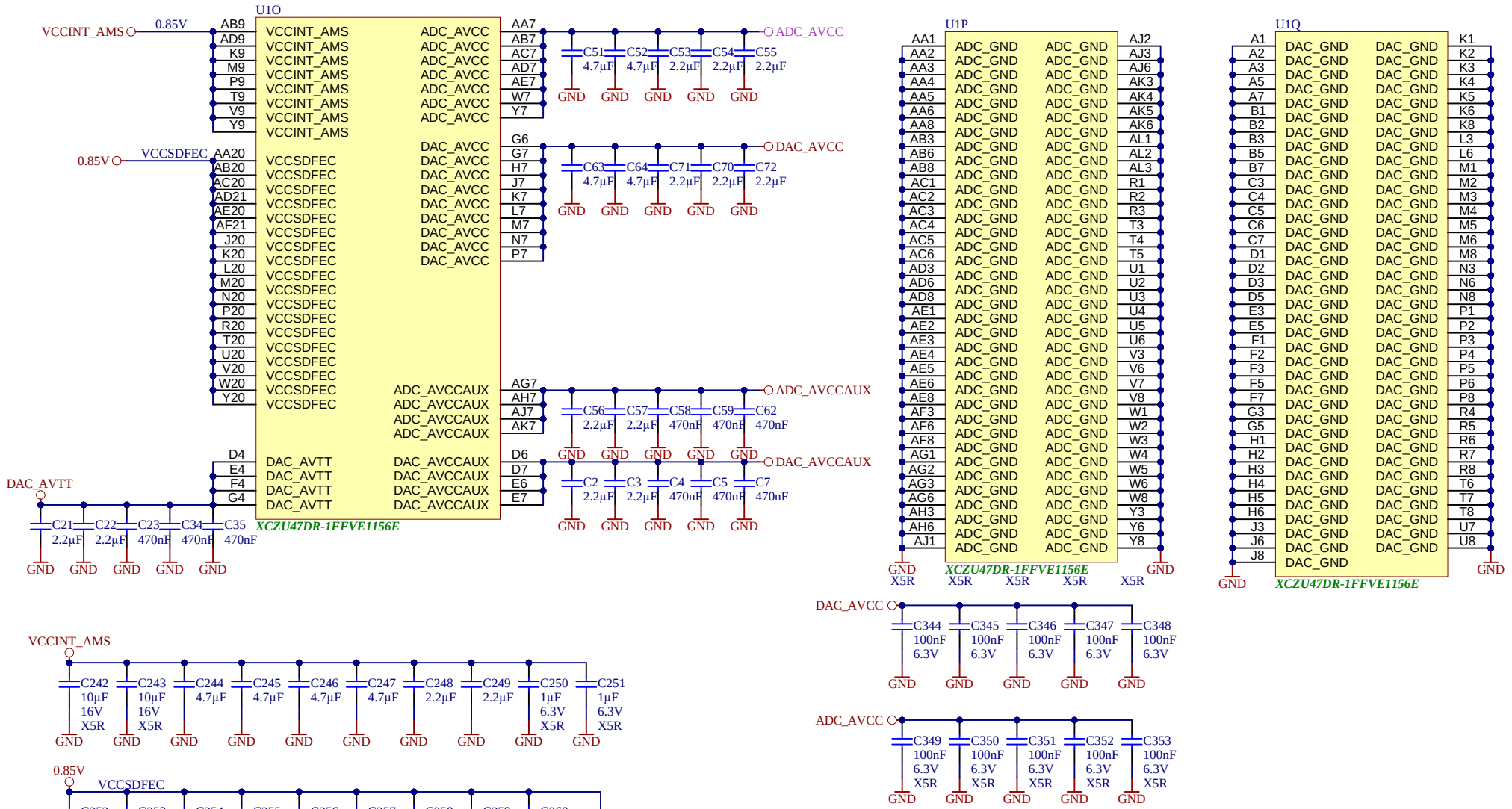


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|---|---|---|---|
| Title: ZU_PWR2 | | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | | Page 11 of 34 |
| Filename: ZU_PWR2.SchDoc | | | |


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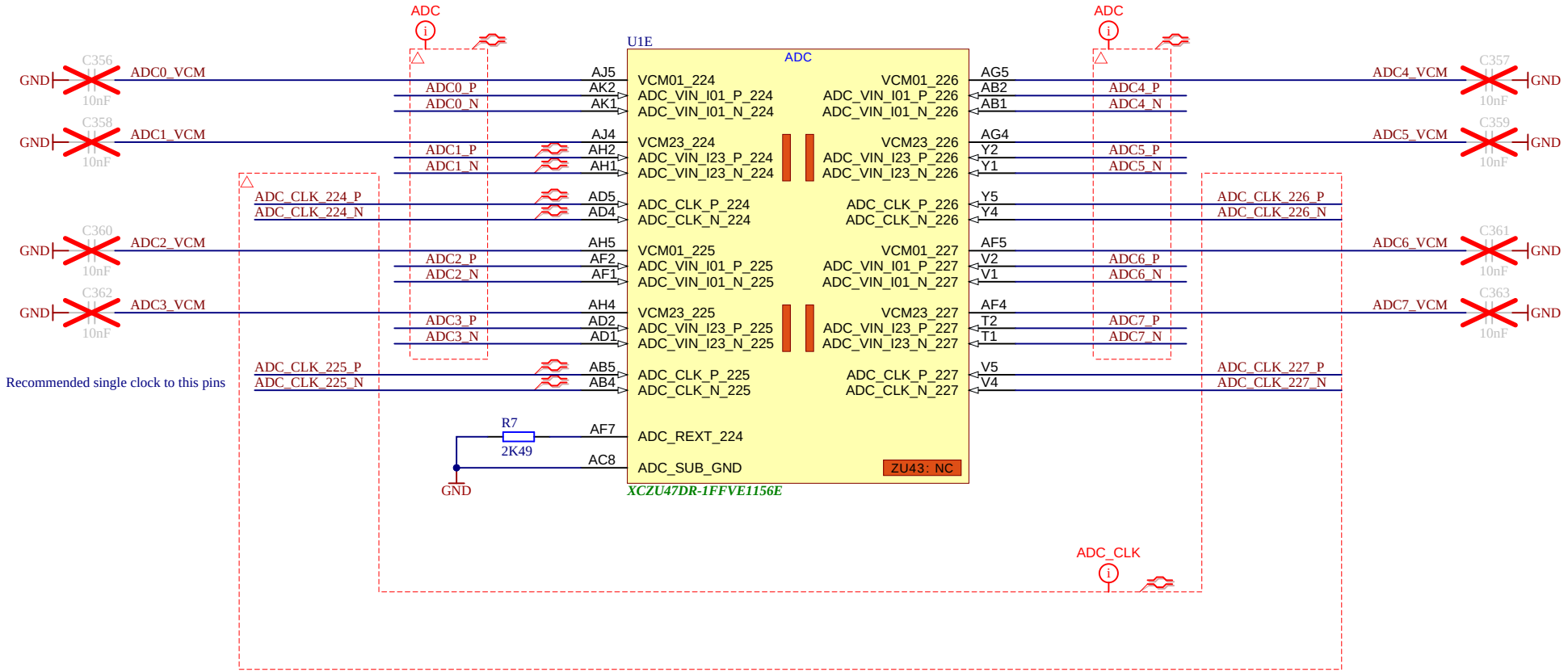
| | | |
|---|---|---|
| Title: ZU_PWR3 | | |
| A4 | Number: TE0835 TXE21-A | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | Page 12 of 34 |
| Filename: ZU_PWR3.SchDoc | | |

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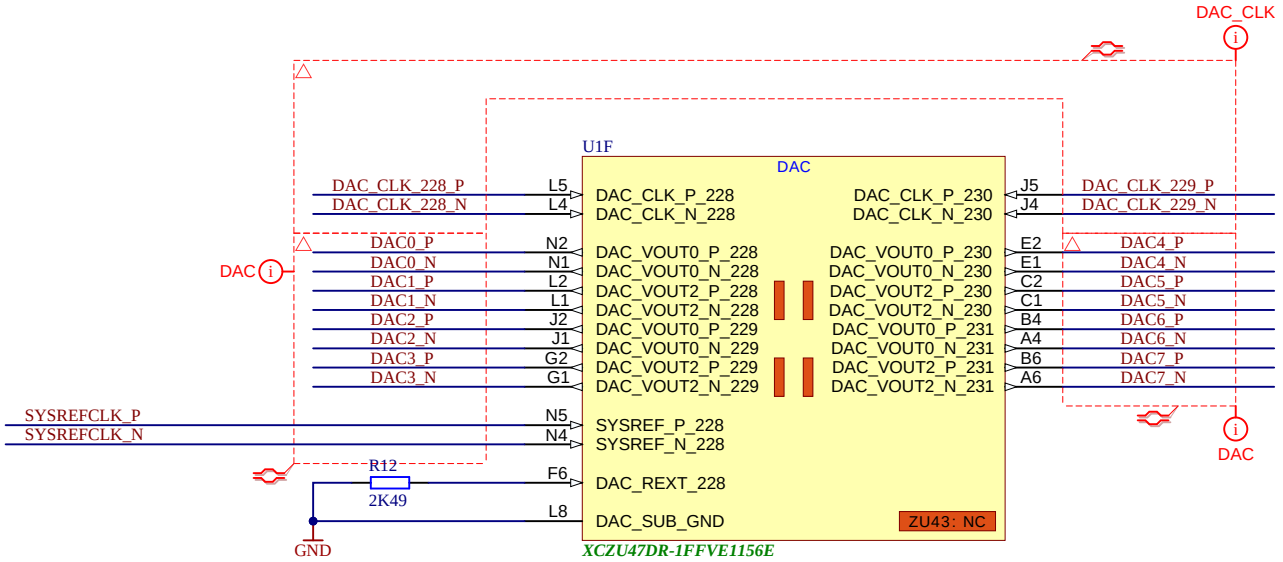
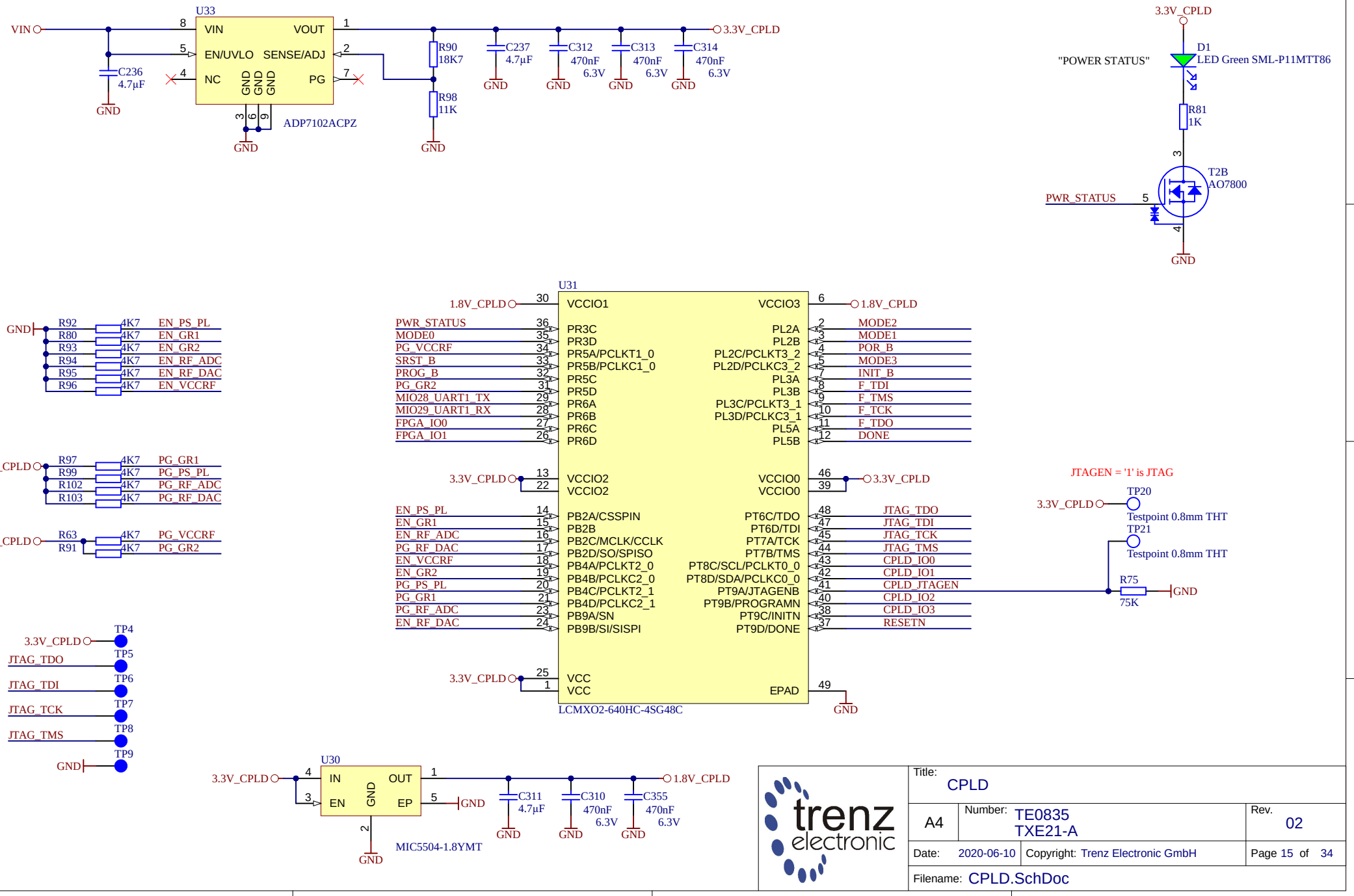
|---|---|---|---|
| trenz electronic | Title: ZU_ADC | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | | Page 13 of 34 |
| Filename: ZU_ADC.SchDoc | | | |




Recommended single clock to this pins

| | | | |
|---|---|---|---|
| trenz electronic | Title: ZU_DAC | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | | Page 14 of 34 |
| Filename: ZU_DAC.SchDoc | | | |

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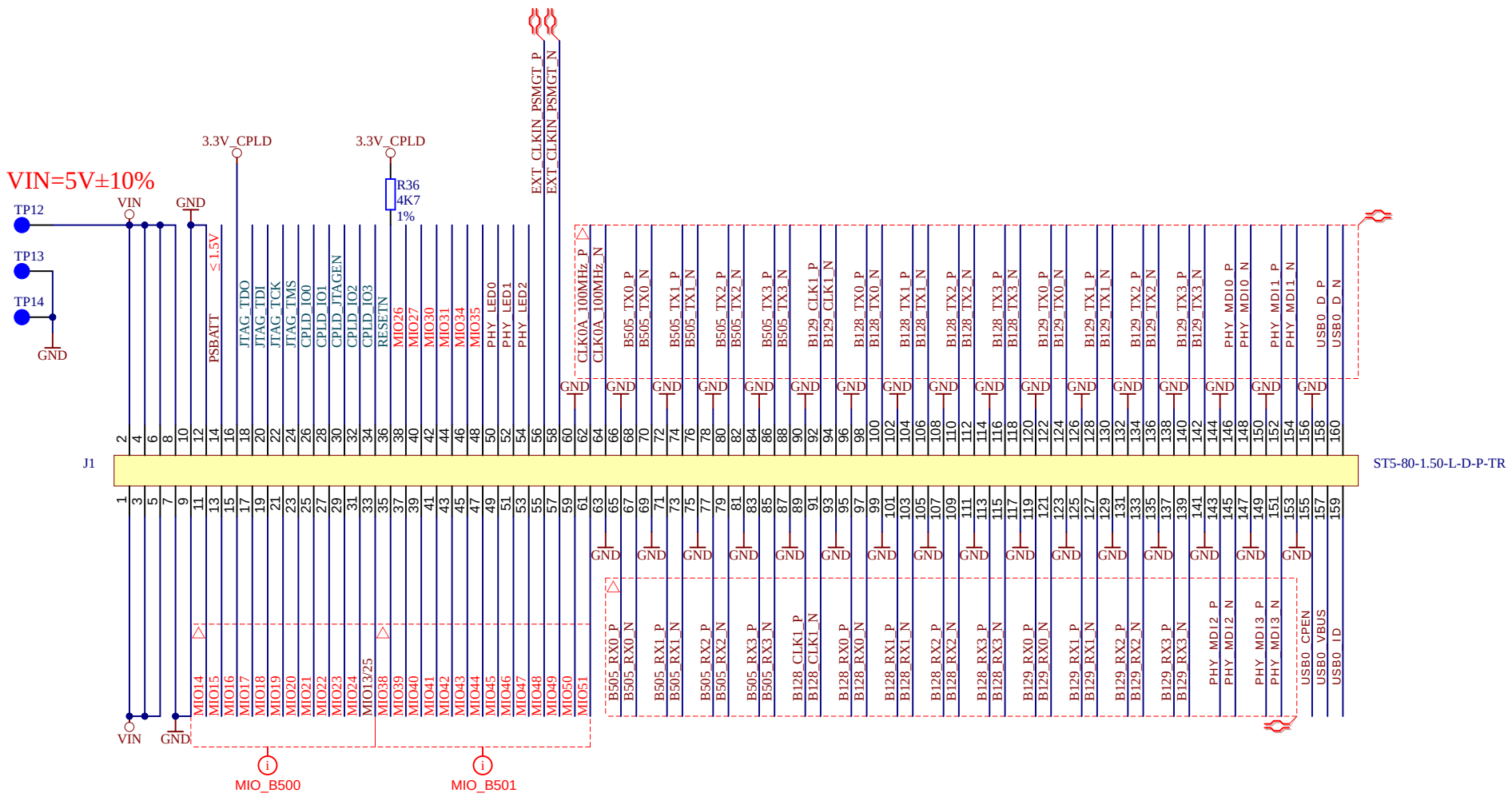
| | | | |
|---|---|---|---|
| Title: CPLD | | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | | Page 15 of 34 |
| Filename: CPLD.SchDoc | | | |

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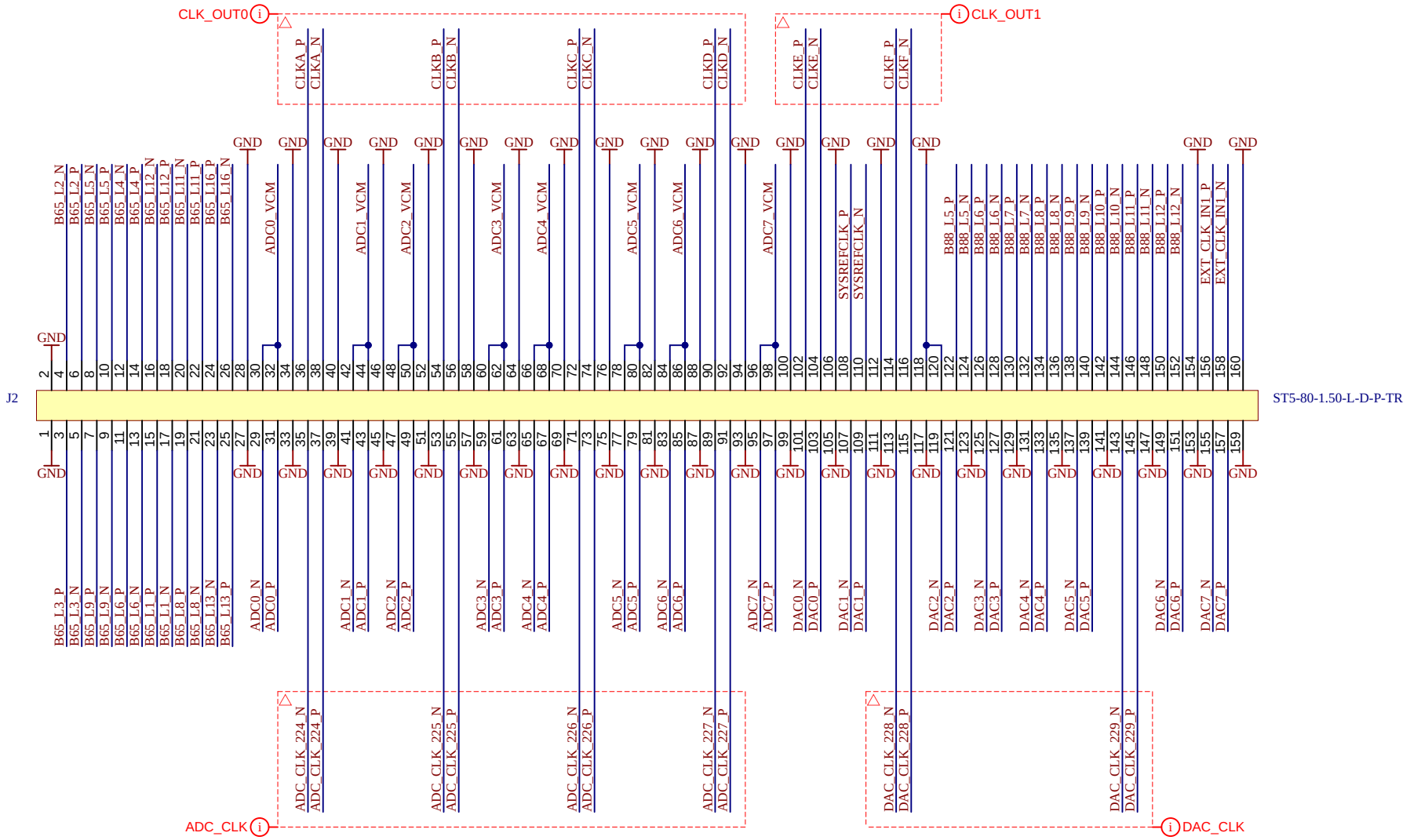
|---|---|---|---|
| Title: B2B | | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | | Page 16 of 34 |
| Filename: B2B.SchDoc | | | |

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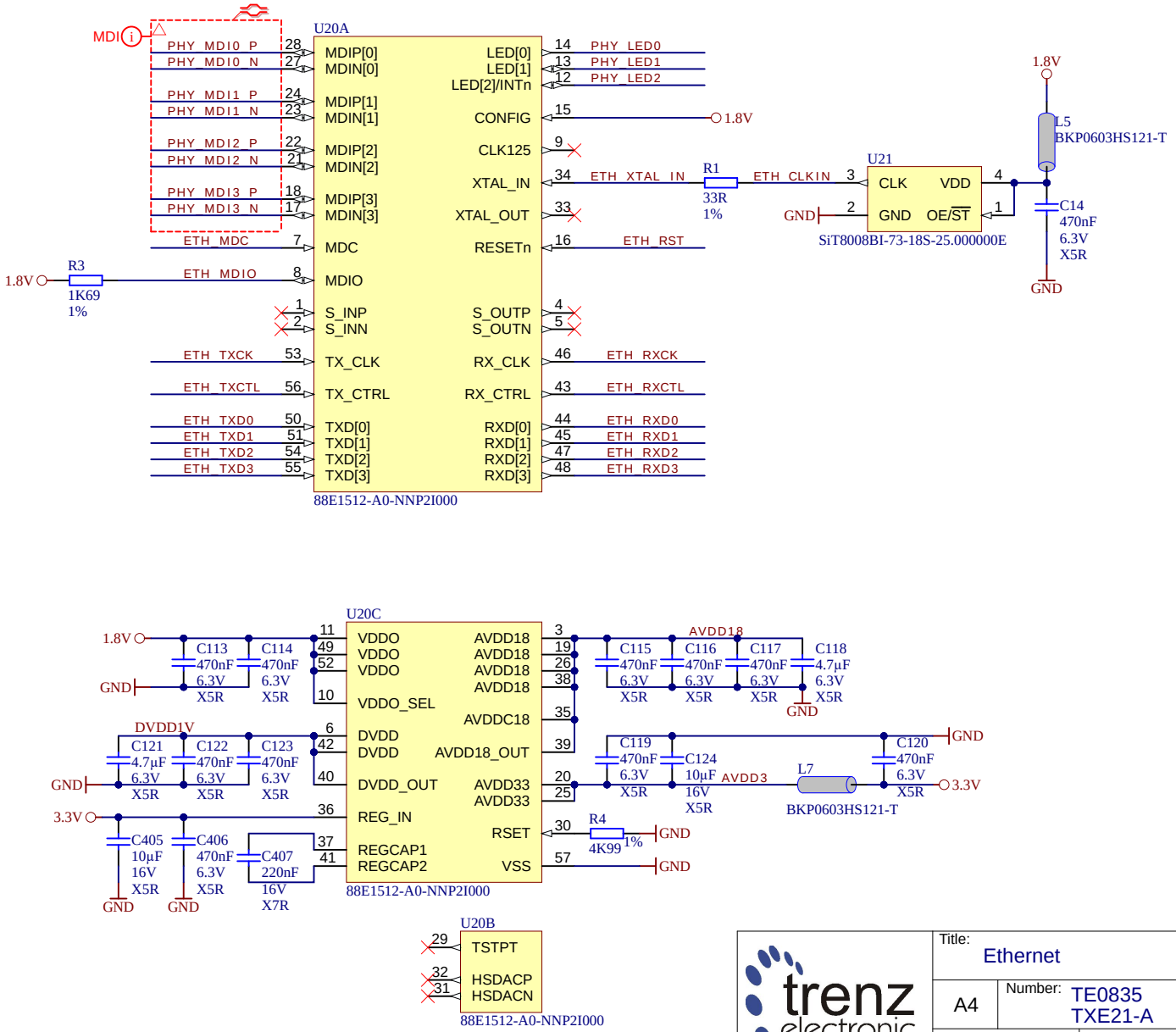
|---|---|---|---|
| Title: B2B_2 | | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | | Page 17 of 34 |
| Filename: B2B_2.SchDoc | | | |

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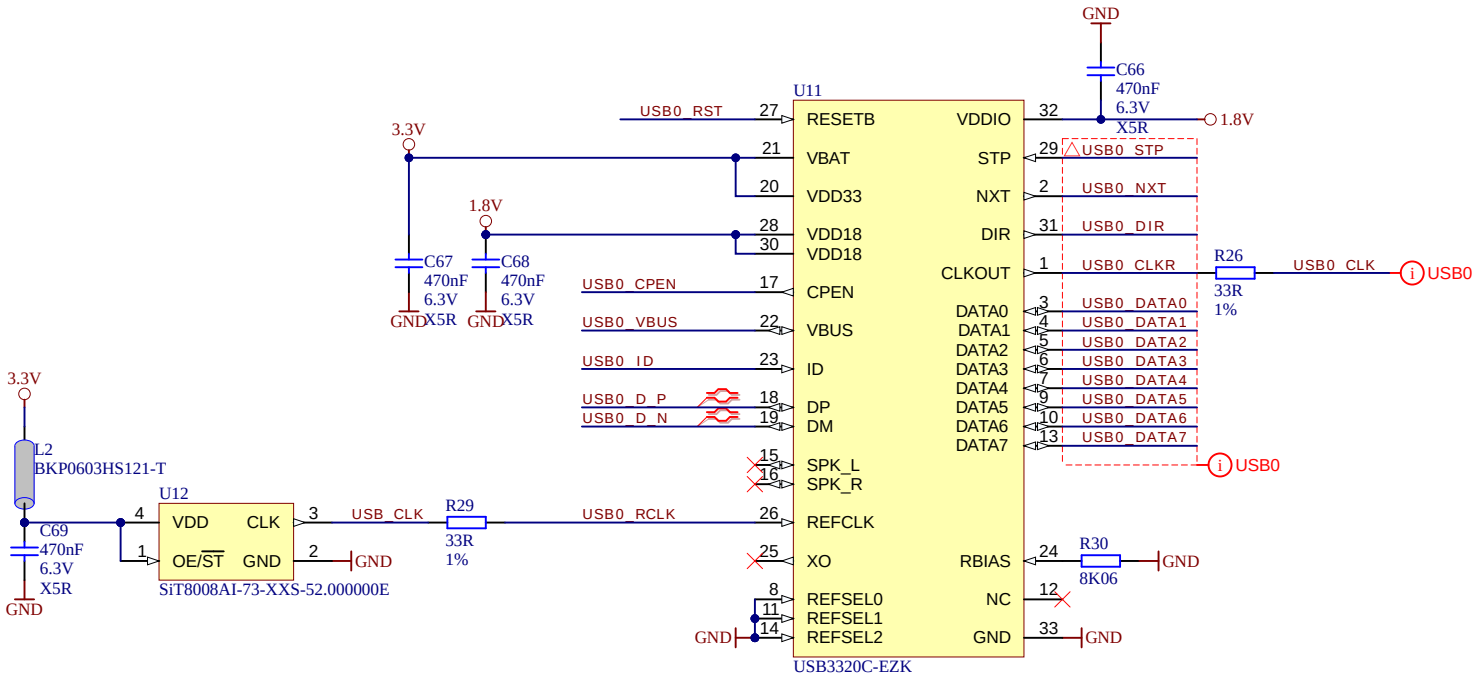
|---|---|---|---|
| trenz electronic | Title: Ethernet | | |
| | A4 | Number: TE0835 TXE21-A | Rev. 02 |
| | Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | Page 18 of 34 |
| | Filename: Ethernet.SchDoc | | |

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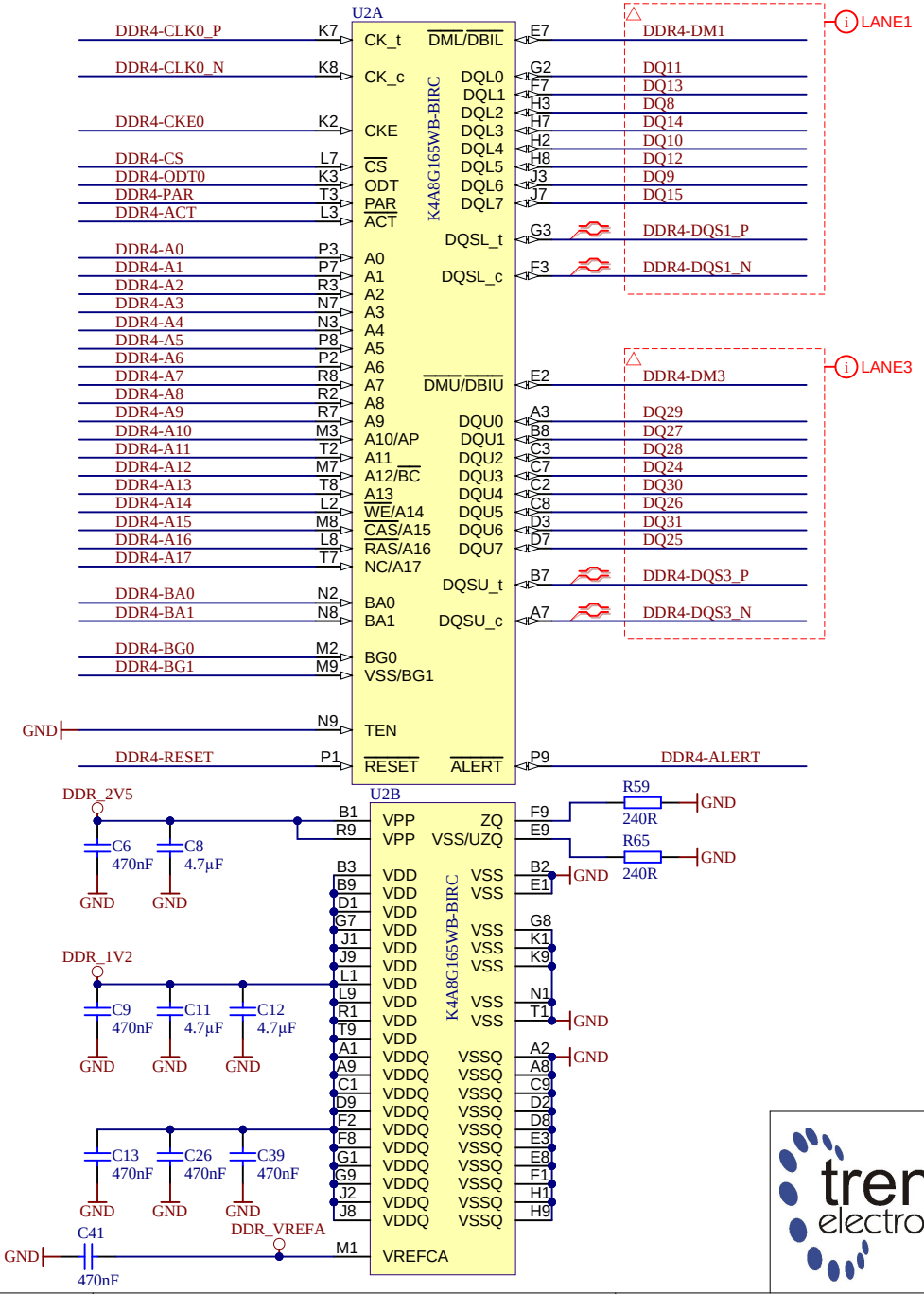
|---|---|---|---|
| trenz electronic | Title: USB-PHY | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | | Page 19 of 34 |
| Filename: USB-PHY.SchDoc | | | |

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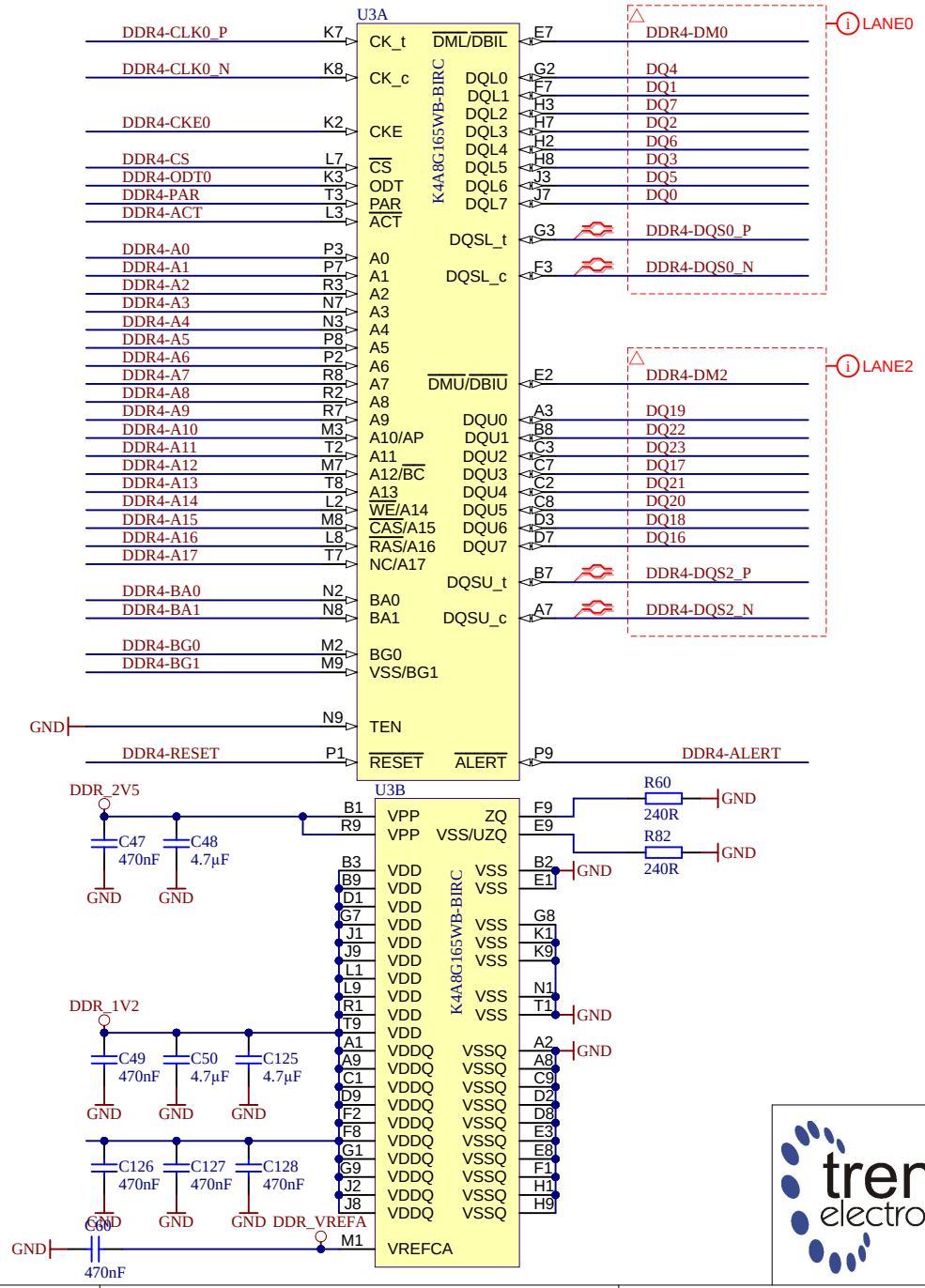
|---|---|---|---|
| Title: DDR4-RAM | | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH / TT | | Page 20 of 34 |
| Filename: DDR4-RAM.SchDoc | | | |

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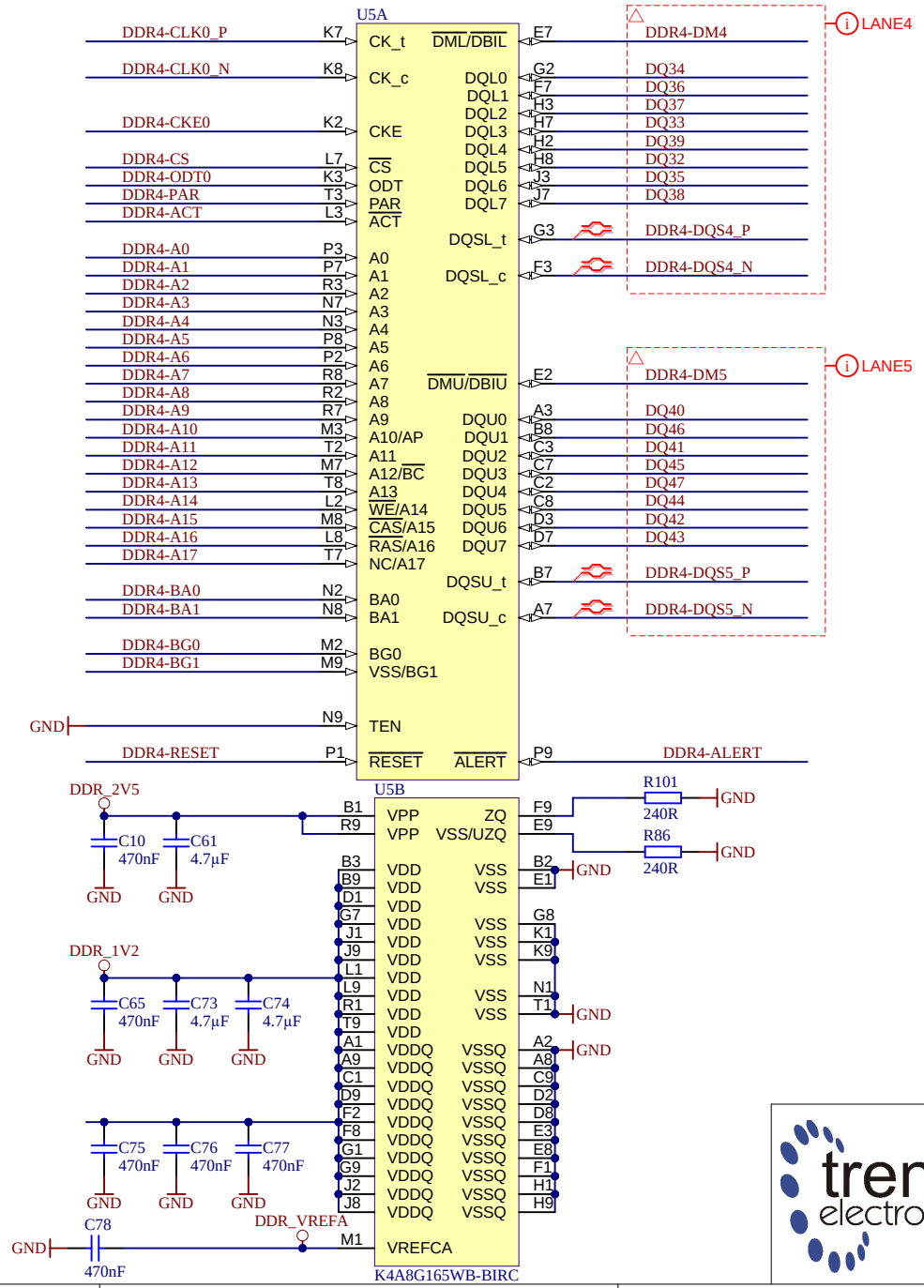
|---|---|---|---|
| Title: DDR4-RAM_2 | | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH / TT | | Page 21 of 34 |
| Filename: DDR4-RAM_2.SchDoc | | | |

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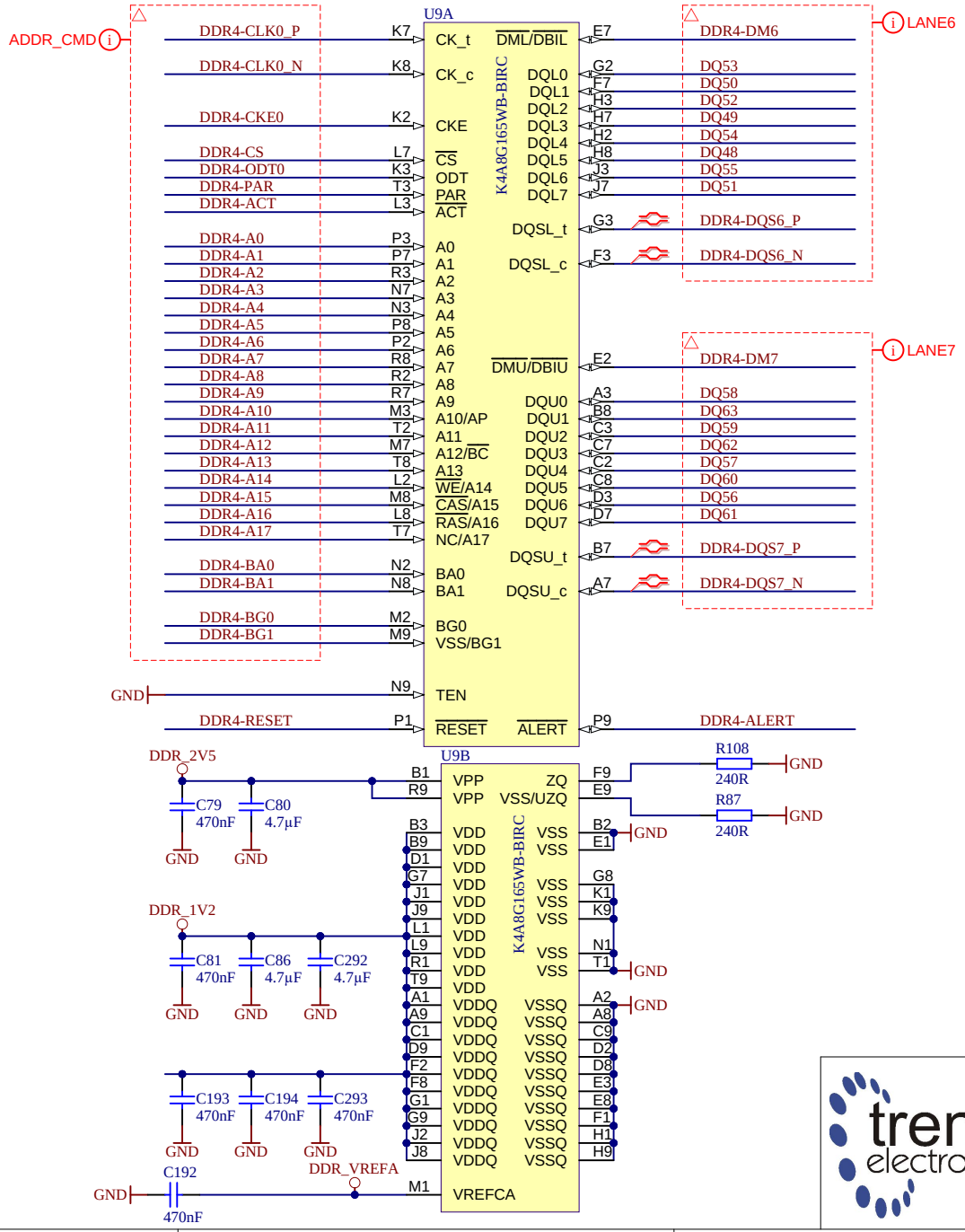
| trenz electronic | Title: DDR4-RAM_3 | | |
| | A4 | Number: TE0835 TXE21-A | Rev. 02 |
| | Date: 2020-06-10 | Copyright: Trenz Electronic GmbH / TT | Page 22 of 34 |
| | Filename: DDR4-RAM_3.SchDoc | | |

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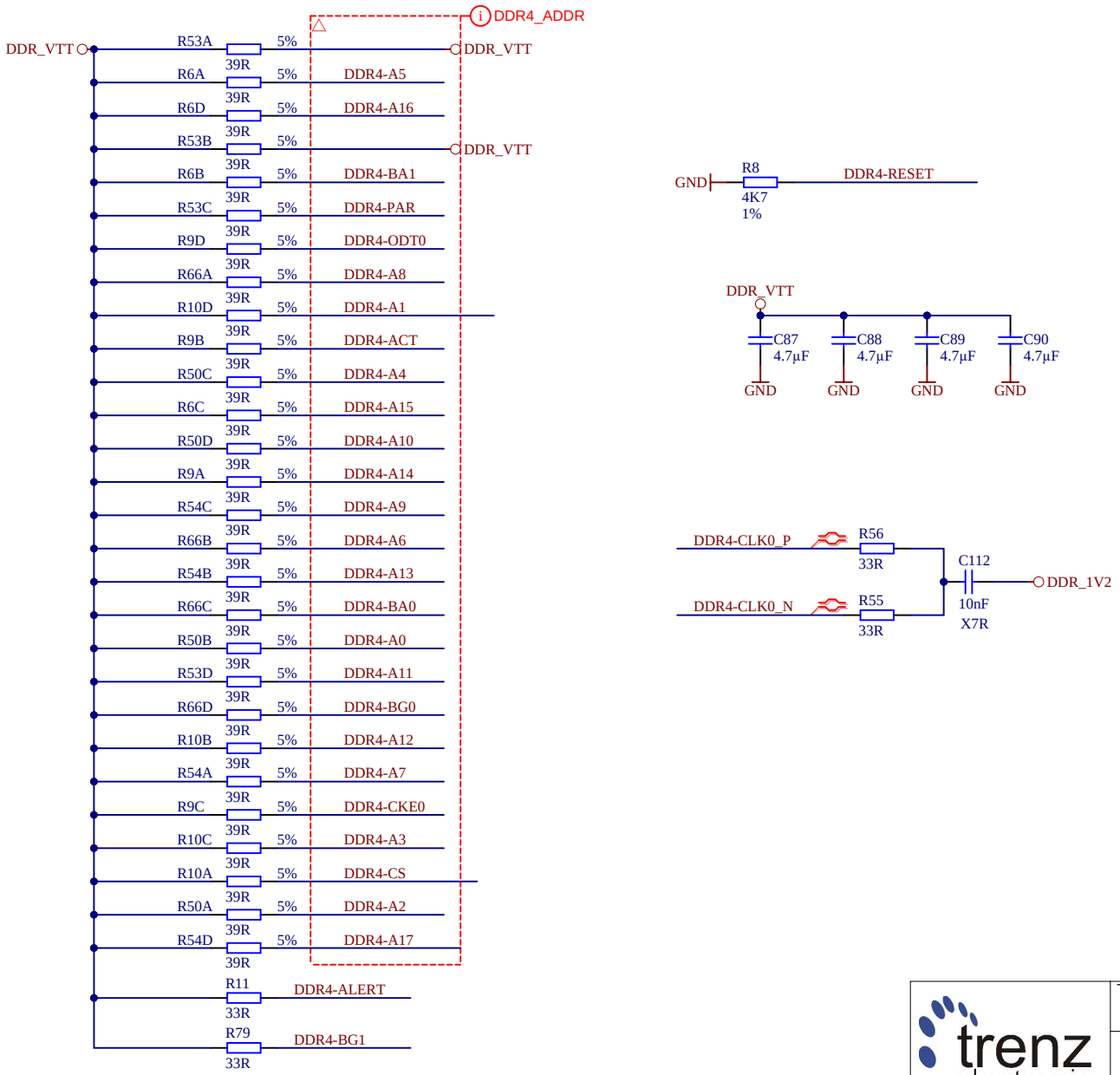
| trenz electronic | Title: DDR4-RAM_4 | | |
| | A4 | Number: TE0835 TXE21-A | Rev. 02 |
| | Date: 2020-06-10 | Copyright: Trenz Electronic GmbH / TT | Page 23 of 34 |
| | Filename: DDR4-RAM_4.SchDoc | | |

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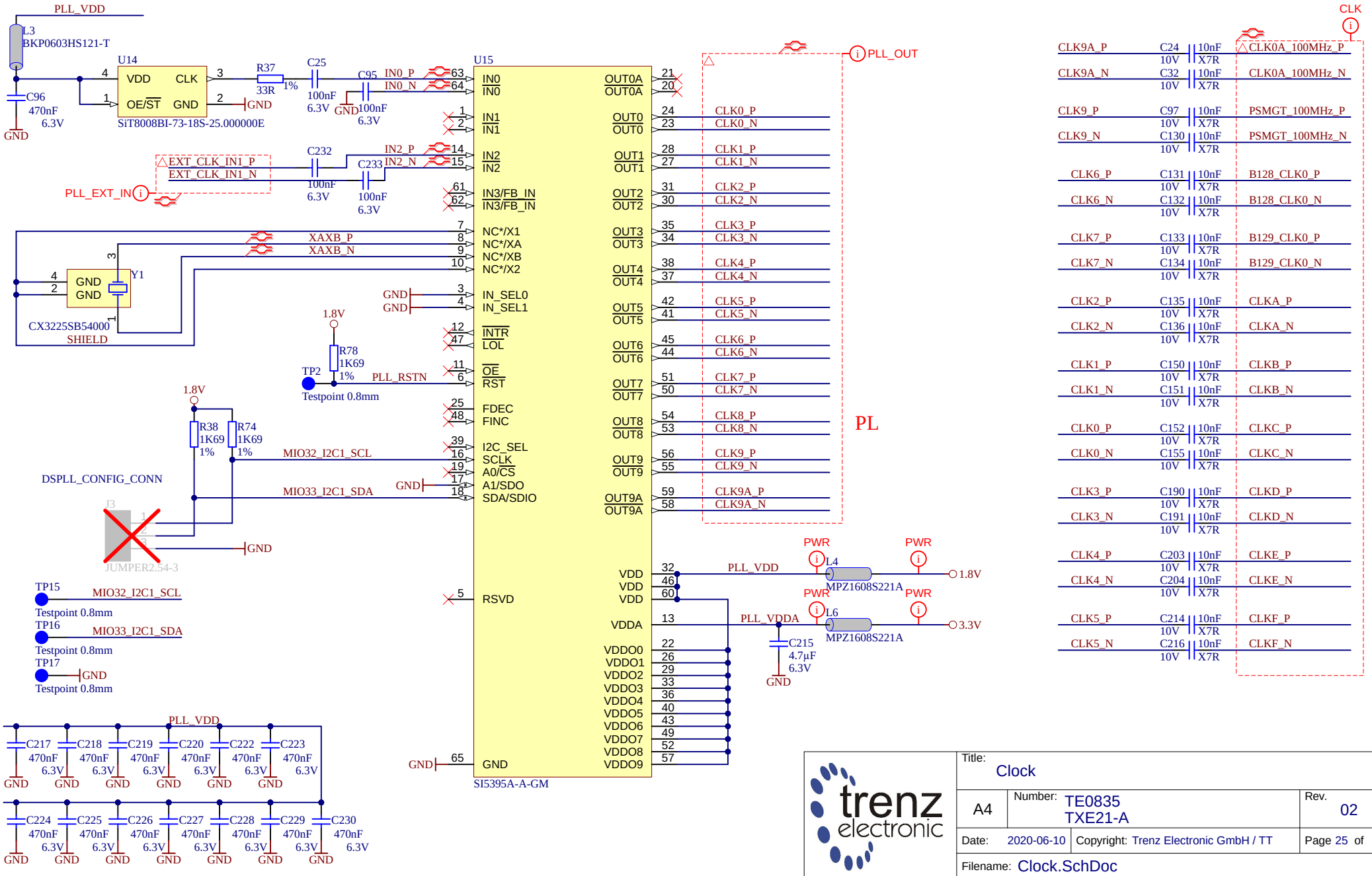
| trenz electronic | Title: DDR4-TERM | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH / TT | | Page 24 of 34 |
| Filename: DDR4-TERM.SchDoc | | | |

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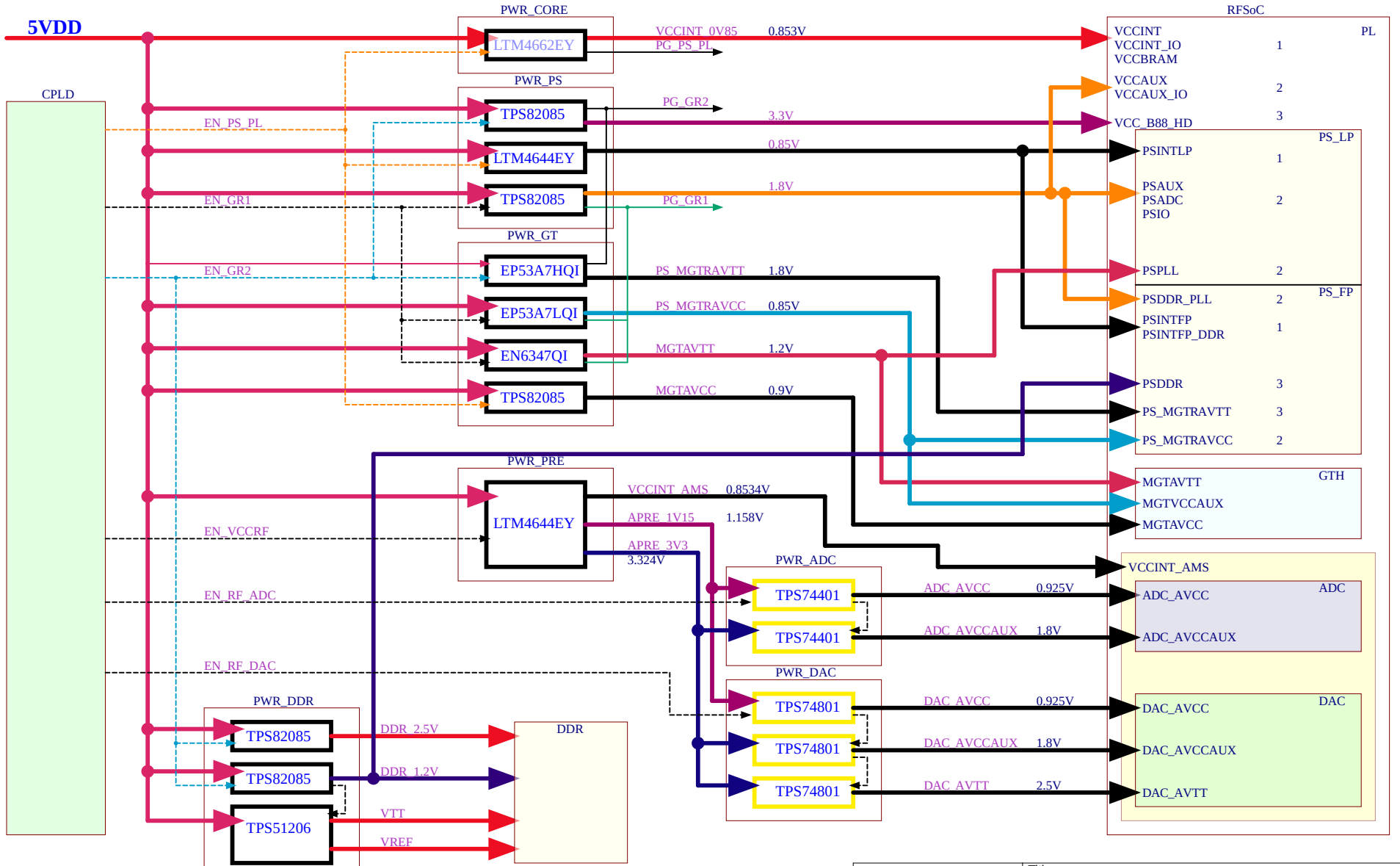
| | | | |
|---|---|---|---|
| Title: Clock | | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH / TT | | Page 25 of 34 |
| Filename: Clock.SchDoc | | | |

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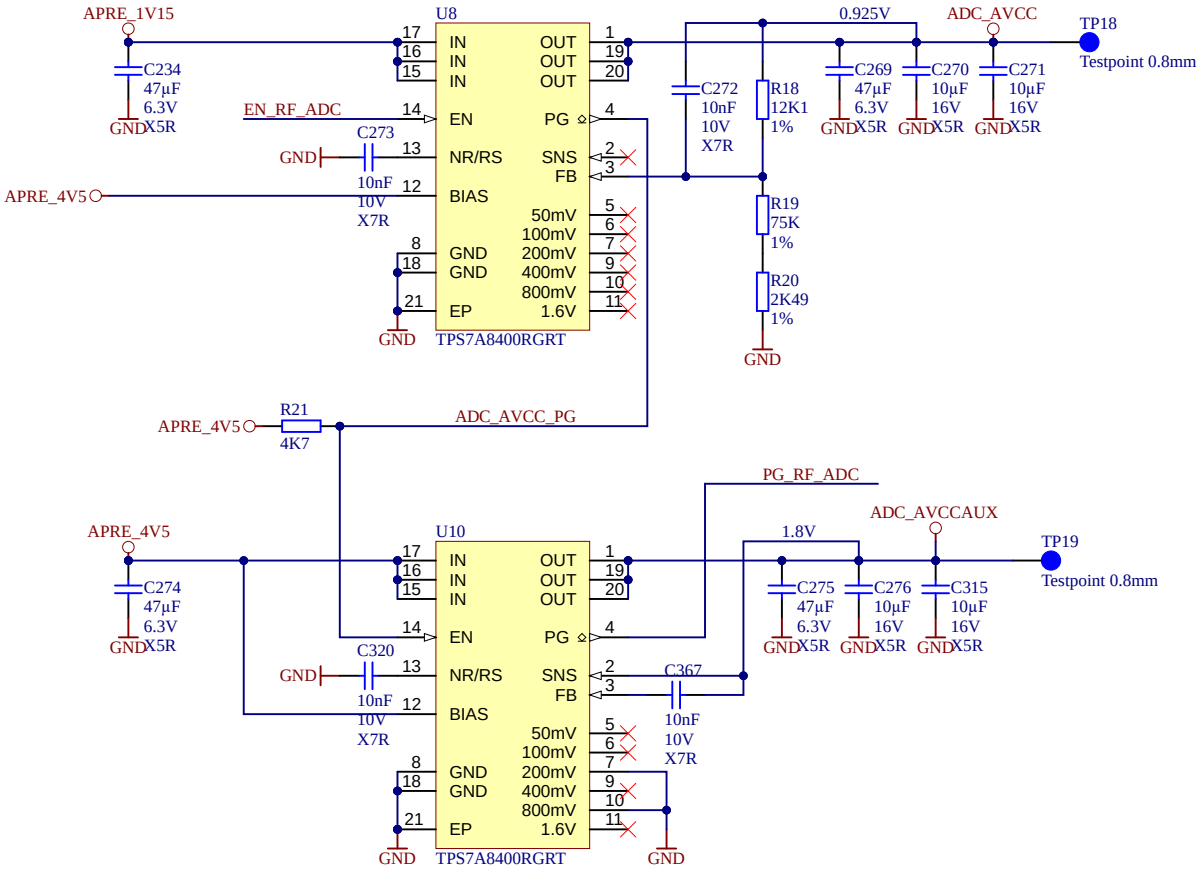
|---|---|---|---|
| Title: PWR_Structure | | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | | Page 26 of 34 |
| Filename: PWR_Structure.SchDoc | | | |

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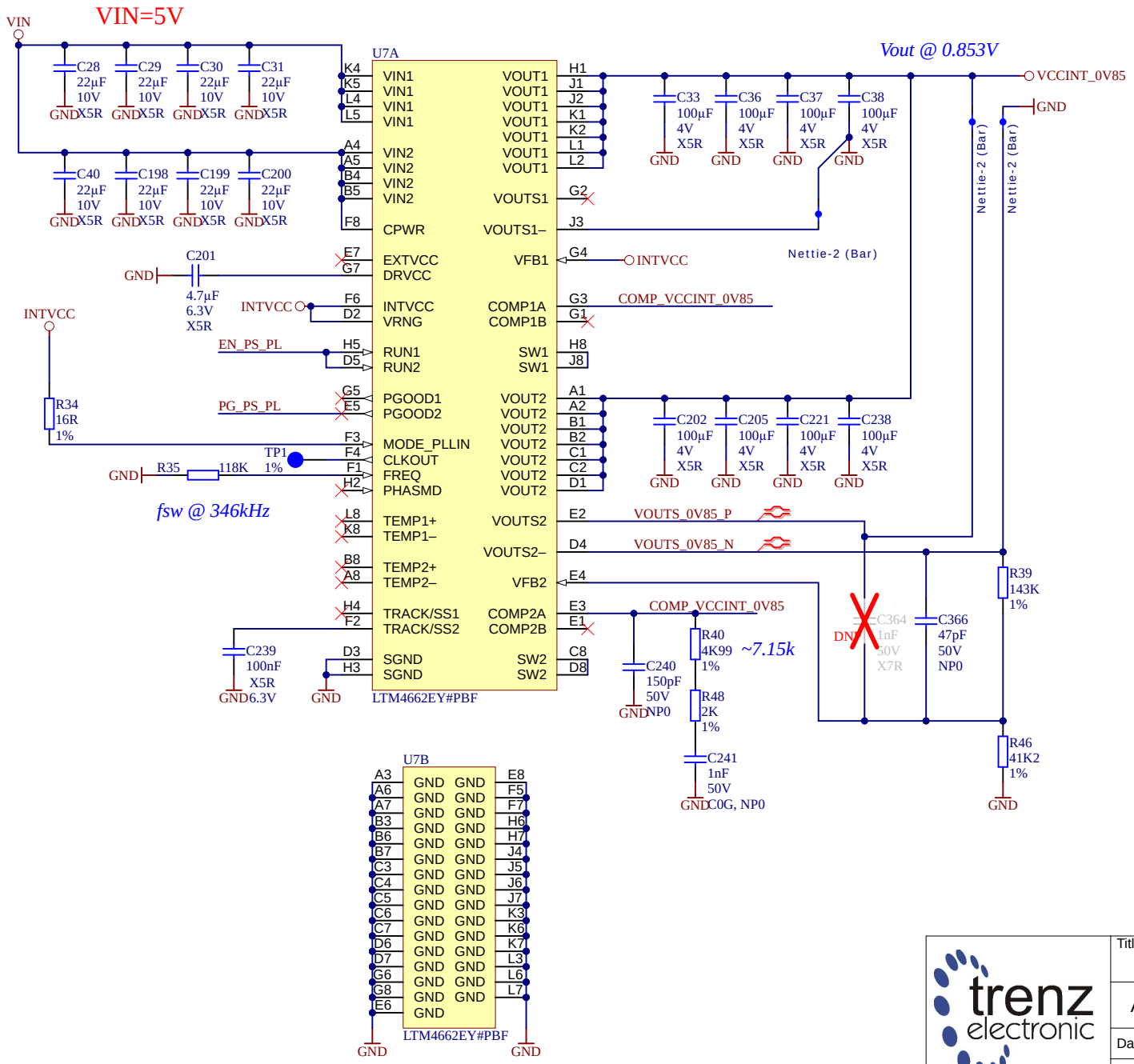
|---|---|---|---|
| Title: PWR_ADC | | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | | Page 27 of 34 |
| Filename: PWR_ADC.SchDoc | | | |

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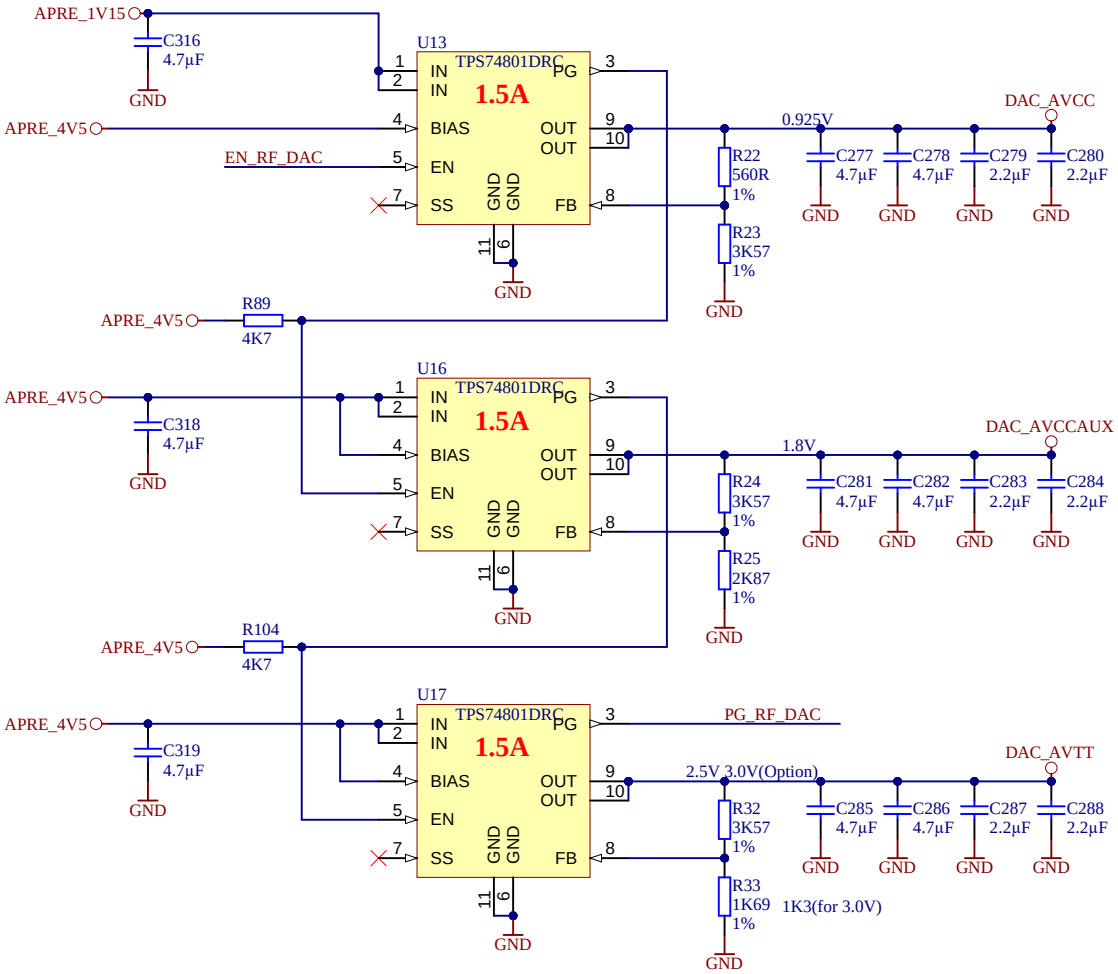
|---|---|---|---|
| Title: PWR_CORE | | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | | Page 28 of 34 |
| Filename: PWR_CORE.SchDoc | | | |

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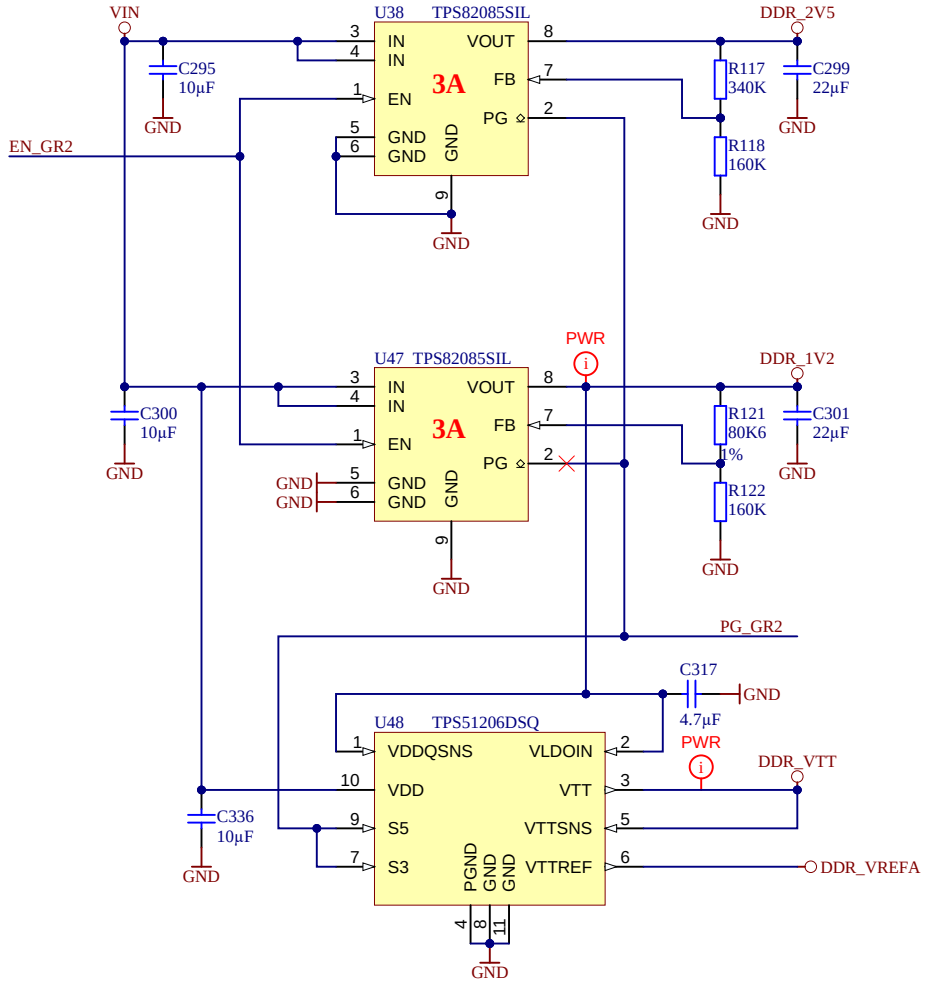
|---|---|---|---|
| Title: PWR_DAC | | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | | Page 29 of 34 |
| Filename: PWR_DAC.SchDoc | | | |

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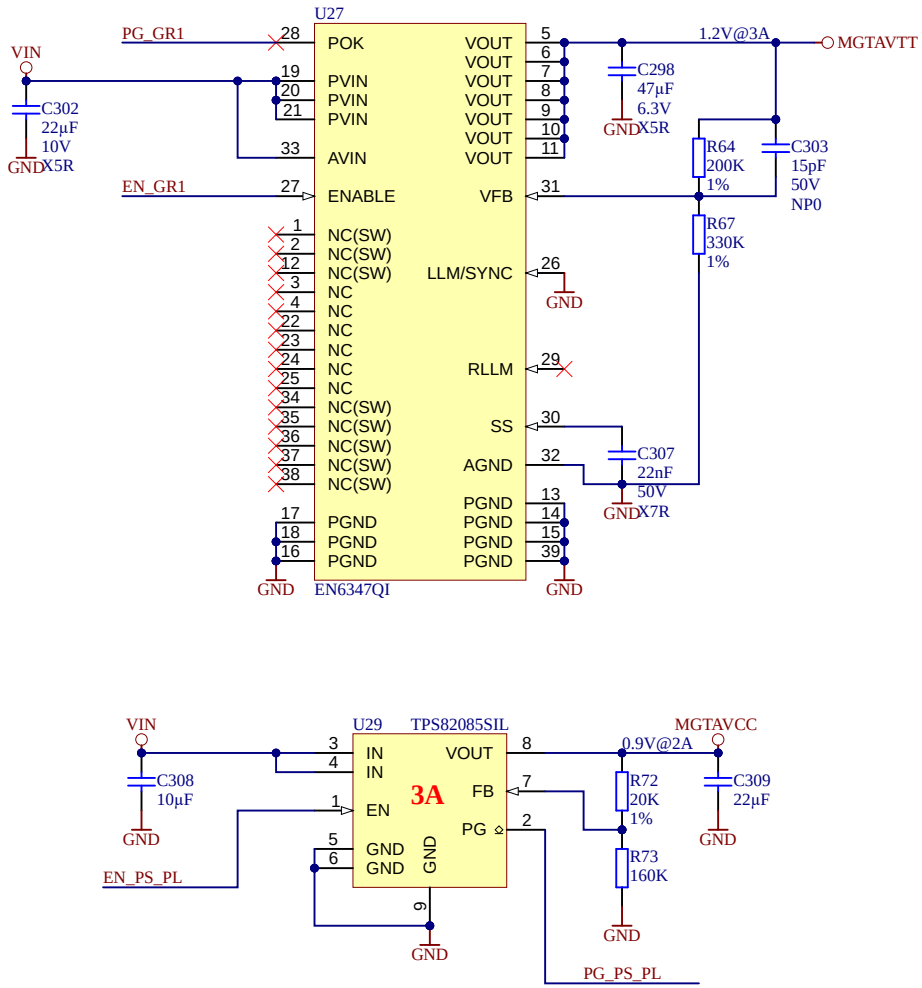
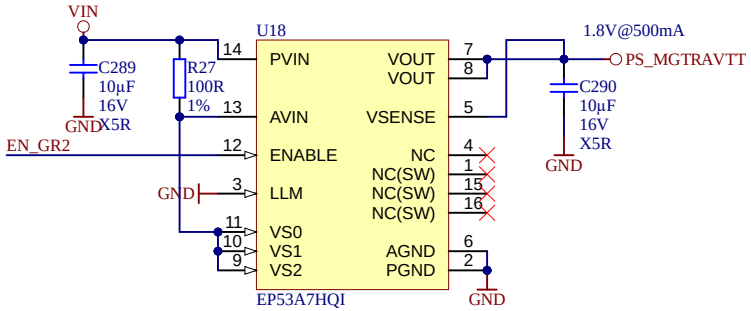
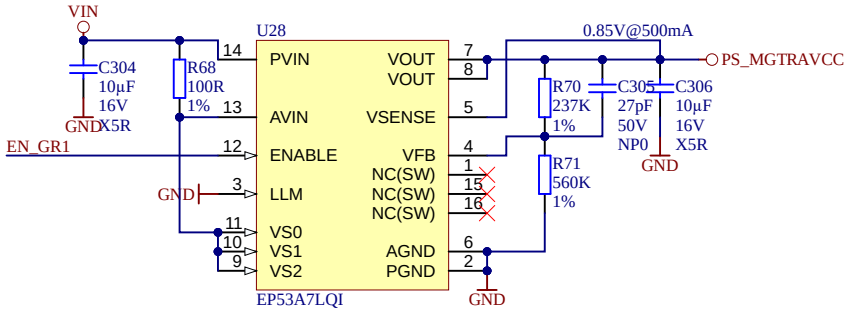
|---|---|---|---|
| trenz electronic | Title: PWR_DDR | | |
| A4 | Number: TE0835 TXE21-A | | Rev. 02 |
| Date: 2020-06-10 | Copyright: Trenz Electronic GmbH | | Page 30 of 34 |
| Filename: PWR_DDR.SchDoc | | | |







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| trenz electronic | Title: PWR_GT | | |
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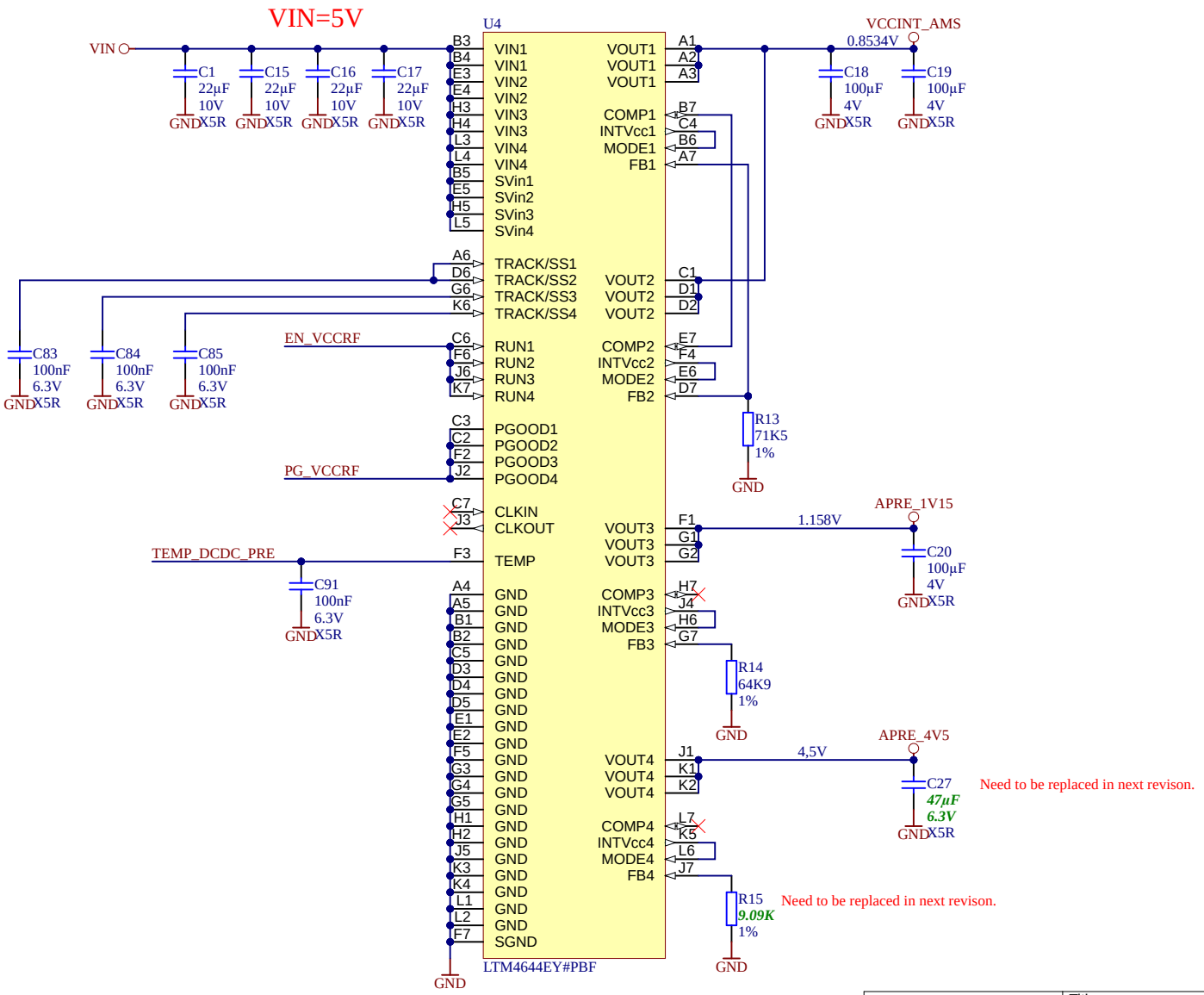


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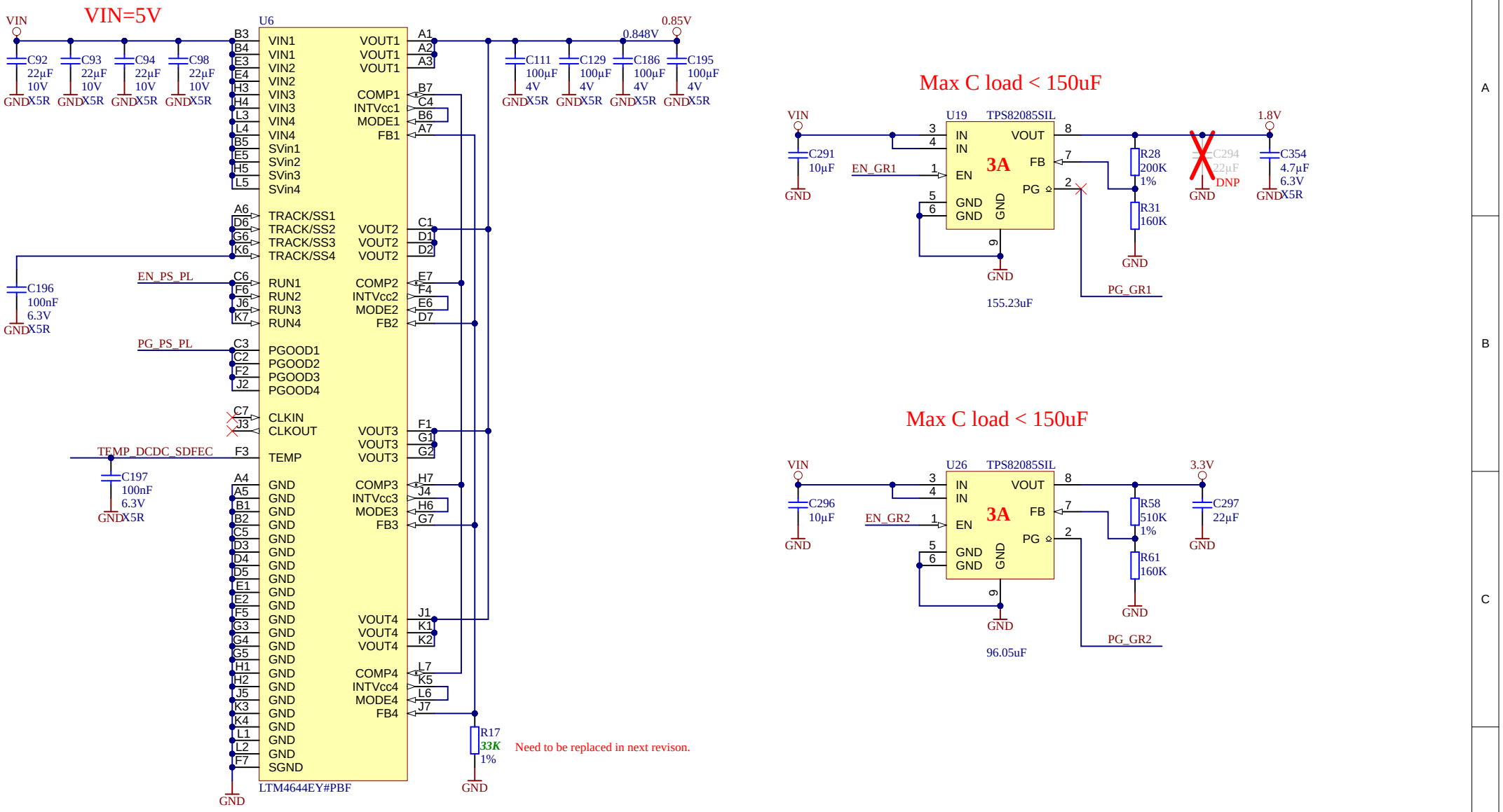


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| Title: PWR_PS | | | |
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REVISION HISTORY

| REV | Description | |
|---|---|---|
| -01 | Initial revision | IG |
| -02 | 1. Added a VRP resistor on bank 65;<br>2. LDO U33 is changed on ADP7102ACPZ;<br>3. Signal FPGA IO0 is connected on AE18 pin of FPGA;<br>4. Signal DBG_LED3 is connected on AD18 pin of FPGA;<br>5. Signal MIO13_25 connected to J1 pin 33 instead MIO25.<br>6. Resistor R84 is removed;<br>7. LED D1 moved on edge of PCB;<br>8. Added THT testpoints J4 on CPLD_JTAGEN, R76 was removed;<br>9. Signals B49_XX_X are renamed in B88_XX_X;<br>10. C241 is changed on 1nF;<br>11. Length of CLK signals on RFADC and RFDAC are adjusted;<br>12. Wrong connection on U8 is fixed (PCB);<br>13. Wrong connection PGOOD1 pin of U7 is fixed;<br>14. R17 is changed from 35,5K to 33K for VCC_PL_PS correction. | IG |
| | 15. APRE_3V3 ranamed to APRE_4V5, voltage of the power rail incrised from 3.3V to 4,58V.<br>16. Resistor R15 is changed from 13,3K to 9,09K. AN: 24671->25969<br>17. Capasitor C27 is changed from 100uF x 4V to 47uF x 6,3V. AN: 28940->24718 | IG |

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