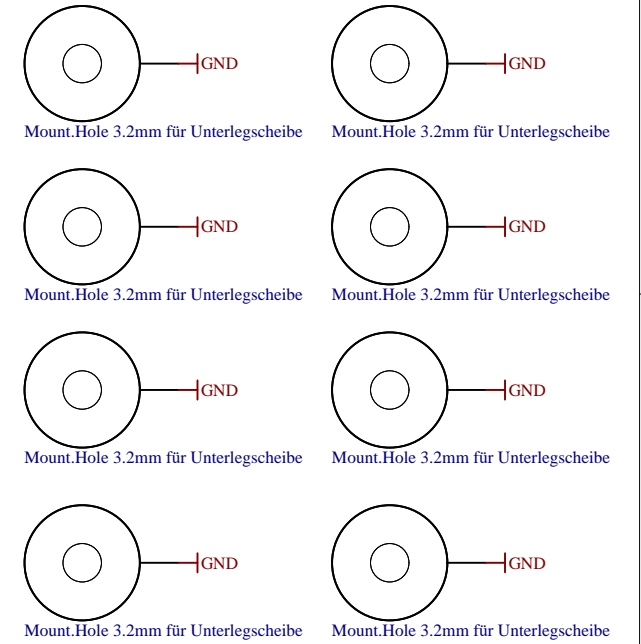
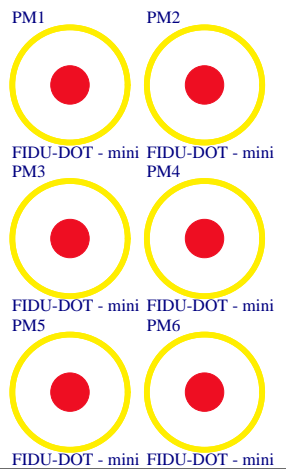


U_Clock Clock.SchDoc	U_ZU ZU.SchDoc
U_DDR4-RAM DDR4-RAM.SchDoc	U_USB-PHY USB-PHY.SchDoc
U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	U_Ethernet Ethernet.SchDoc
U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	U_B2B B2B.SchDoc
U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	U_B2B_2 B2B_2.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	PWR_Structure PWR_Structure.SchDoc
CPLD CPLD.SchDoc	



LOGO1
TE Logo PRINT Layer
LOGO PRINT

Serial
Serial
Serialnumber 6,3 x 6.3mm



Design drawn by: IG
Checked by: MR
Assembly variant: TYE21-A
Created by:
Modified by:
Modified at:



Title: TE0835		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 1 of 34
Filename: TE0835.SchDoc		

1

2

3

4

A

A

HD
ZU_HD.SchDoc



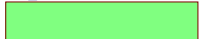
MGT_L
ZU_MGT_L.SchDoc



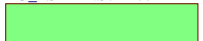
ZU_B65_B66
ZU_B65_B66.SchDoc



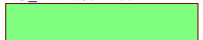
MIO
ZU_MIO.SchDoc



PSDDR
ZU_PSDDR.SchDoc



ZU_PWR
ZU_PWR.SchDoc



ZU_PWR2
ZU_PWR2.SchDoc



ZU_PWR3
ZU_PWR3.SchDoc



ZU_ADC
ZU_ADC.SchDoc



ZU_DAC
ZU_DAC.SchDoc



ZU_CFG
ZU_CFG.SchDoc



ZU_PSMGT
ZU_PSMGT.SchDoc



B

B

C

C

D

D

1

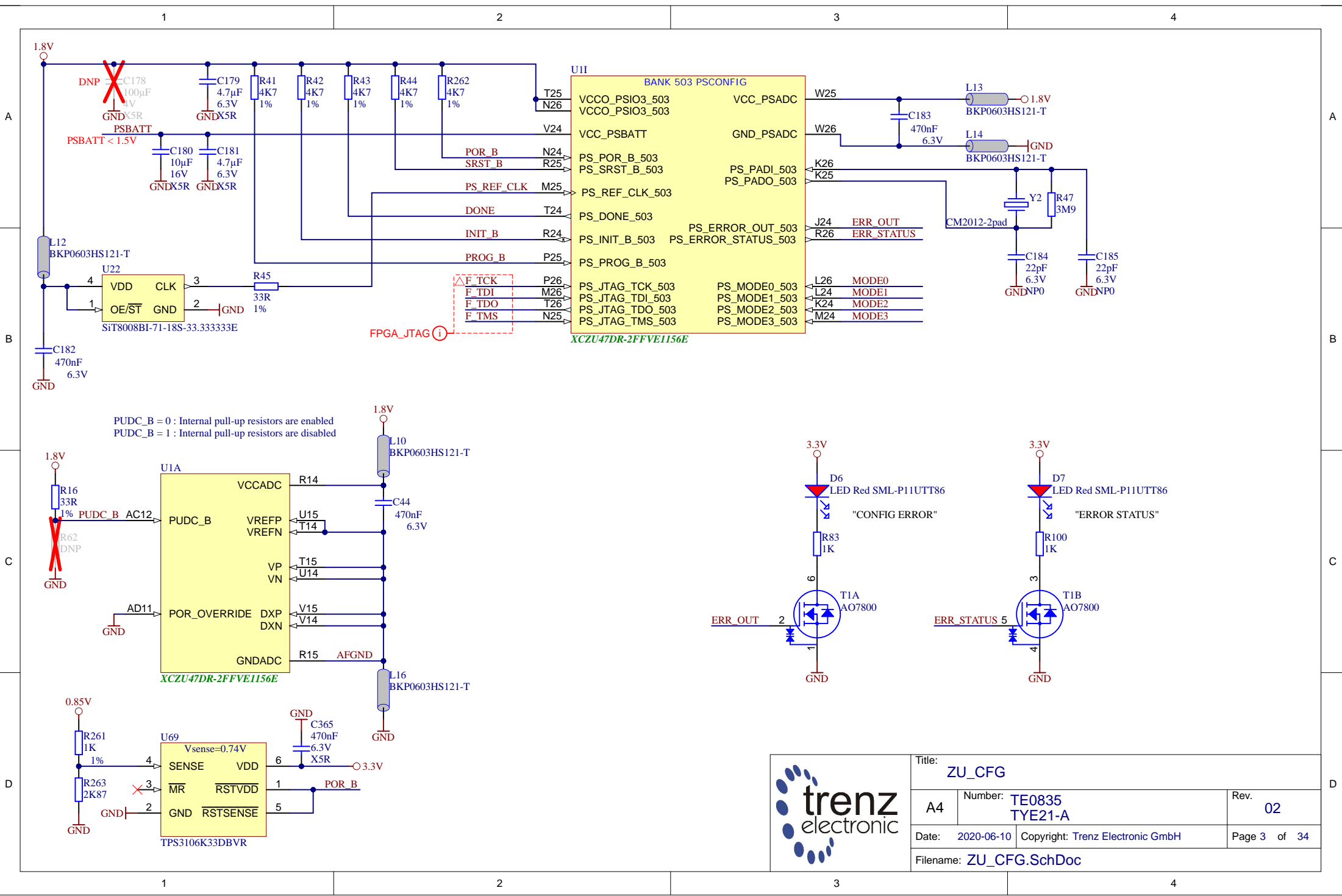
2

3

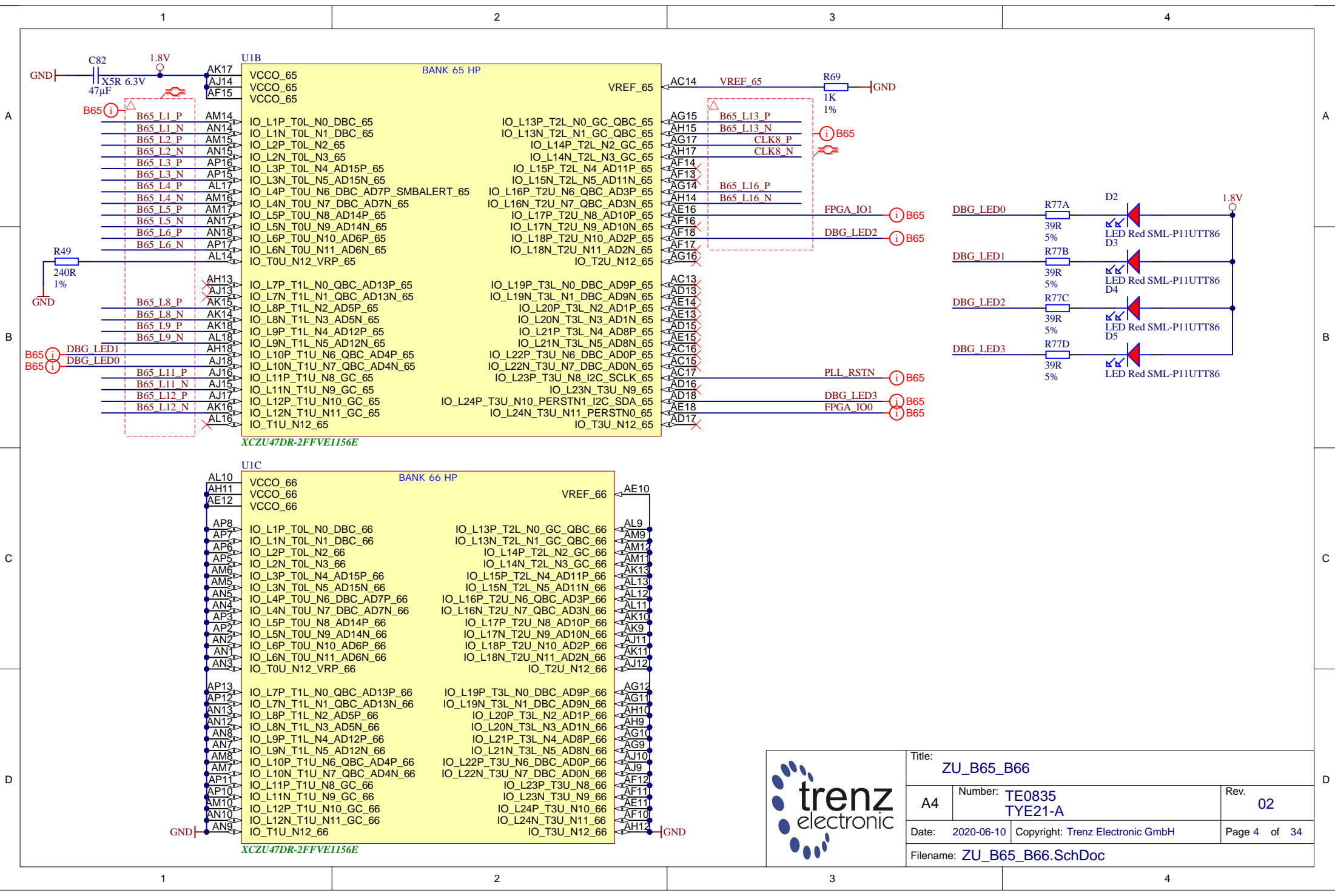
4



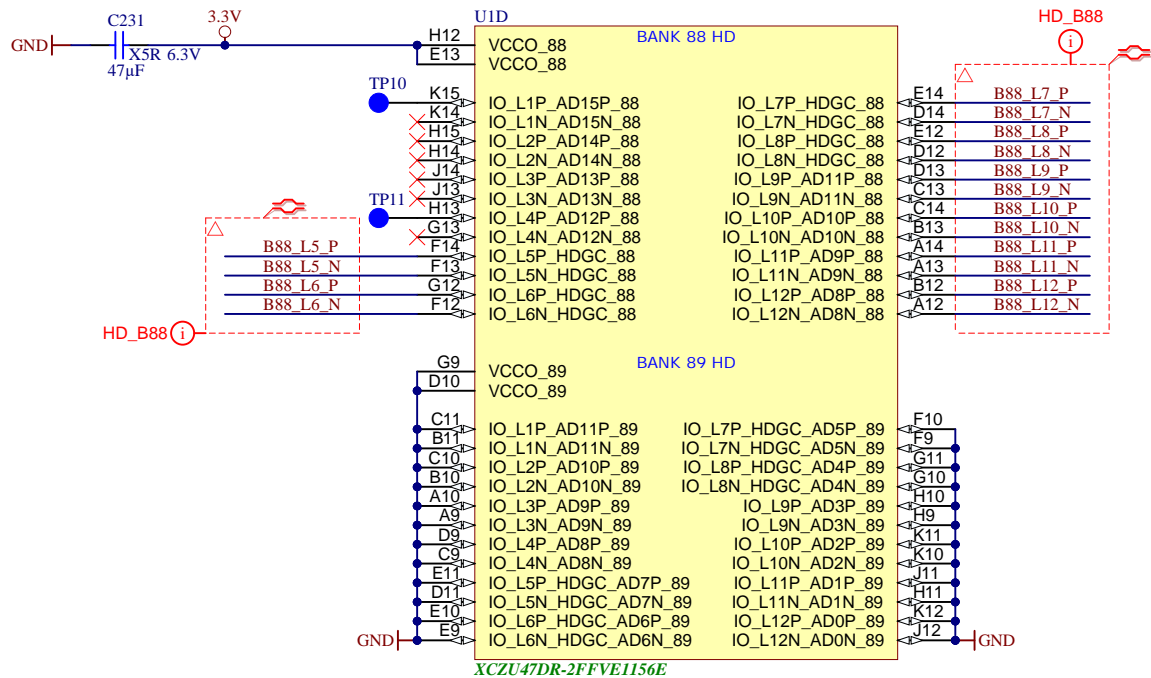
Title: ZU		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 2 of 34
Filename: ZU.SchDoc		



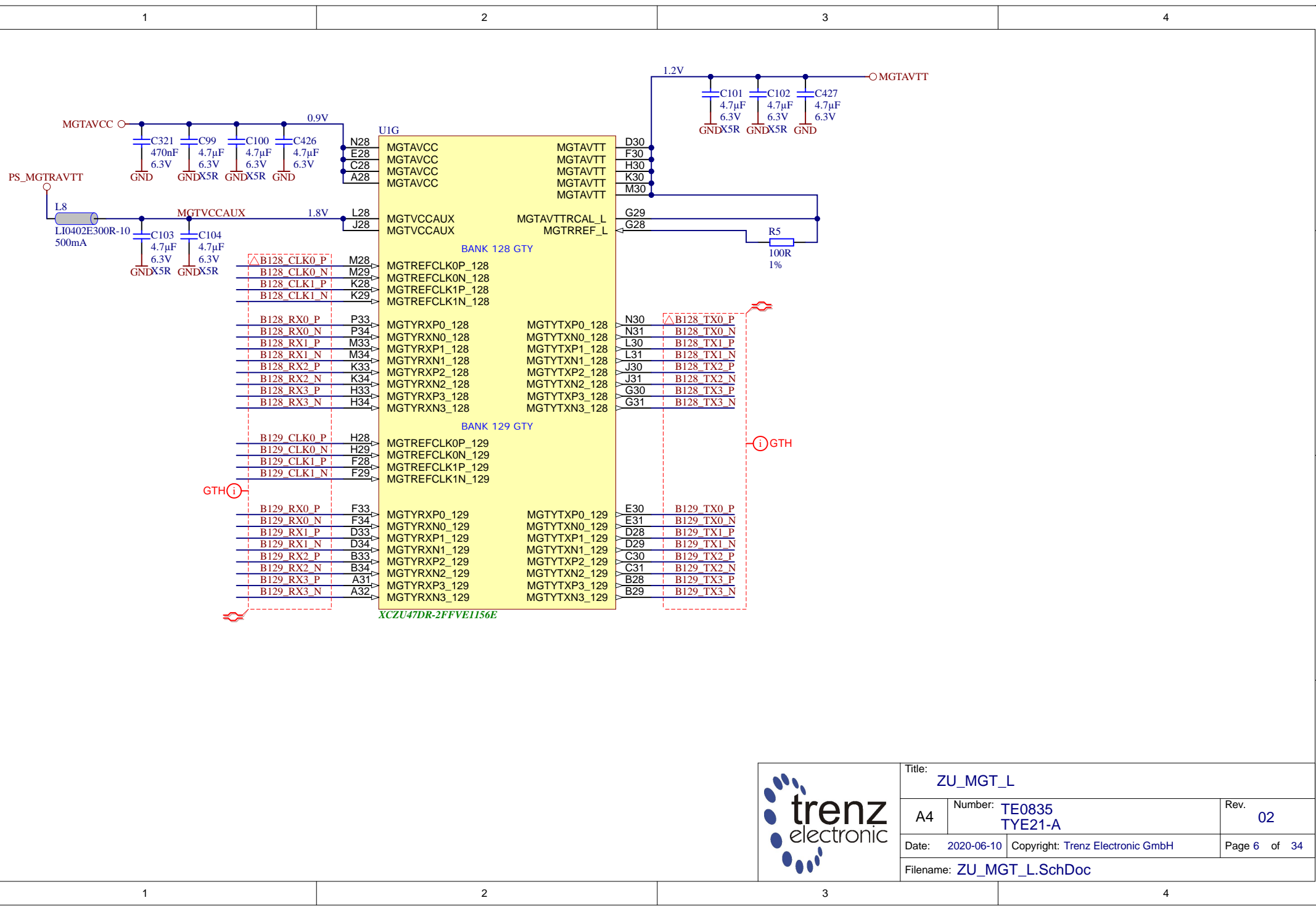
Title: ZU_CFG		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 3 of 34
Filename: ZU_CFG.SchDoc		



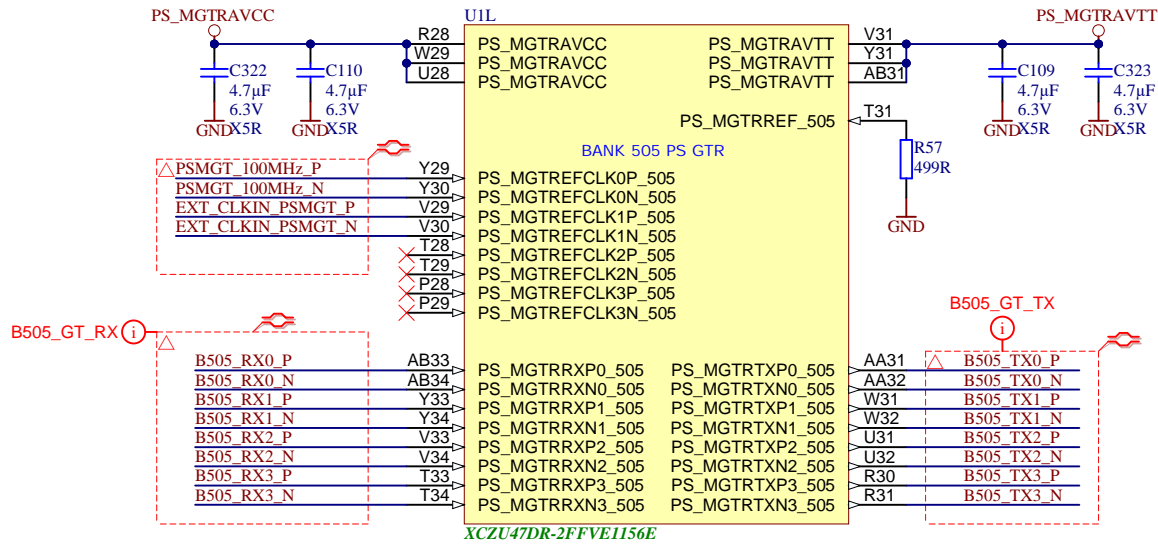
Title: ZU_B65_B66		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 4 of 34
Filename: ZU_B65_B66.SchDoc		




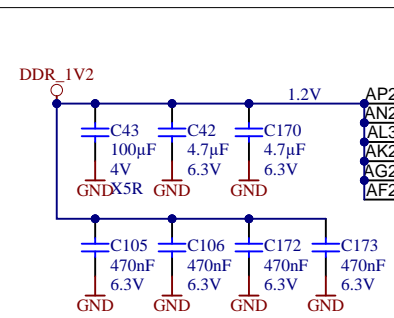
Title: ZU_HD		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 5 of 34
Filename: ZU_HD.SchDoc		



Title: ZU_MGT_L		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 6 of 34
Filename: ZU_MGT_L.SchDoc		



		Title: ZU_PSMGT	
		A4	Number: TE0835 TYE21-A
Date: 2020-06-10		Copyright: Trenz Electronic GmbH	
Filename: ZU_PSMGT.SchDoc		Page 7 of 34	



UIJ

BANK 504 PSDDR

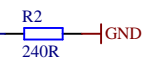
VCCO_PSDDR_504	PS_DDR_CK0_504	AN28	DDR4-CLK0_P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	AP28	DDR4-CLK0_N
VCCO_PSDDR_504	PS_DDR_CKE0_504	AP31	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1_504	AL27	
VCCO_PSDDR_504	PS_DDR_CK_N1_504	AM27	
VCCO_PSDDR_504	PS_DDR_CKE1_504	AK28	
	PS_DDR_A0_504	AN29	DDR4-A0
	PS_DDR_A1_504	AP27	DDR4-A1
	PS_DDR_A2_504	AP25	DDR4-A2
	PS_DDR_A3_504	AP26	DDR4-A3
	PS_DDR_A4_504	AN27	DDR4-A4
	PS_DDR_A5_504	AN25	DDR4-A5
	PS_DDR_A6_504	AK26	DDR4-A6
	PS_DDR_A7_504	AK25	DDR4-A7
	PS_DDR_A8_504	AJ26	DDR4-A8
	PS_DDR_A9_504	AJ25	DDR4-A9
	PS_DDR_A10_504	AL28	DDR4-A10
	PS_DDR_A11_504	AM26	DDR4-A11
	PS_DDR_A12_504	AL29	DDR4-A12
	PS_DDR_A13_504	AM25	DDR4-A13
	PS_DDR_A14_504	AM29	DDR4-A14
	PS_DDR_A15_504	AL26	DDR4-A15
	PS_DDR_A16_504	AH25	DDR4-A16
	PS_DDR_A17_504	AG25	DDR4-A17
	PS_DDR_CS_N0_504	AN30	DDR4-CS
	PS_DDR_CS_N1_504	AM30	
	PS_DDR_BA0_504	AG26	DDR4-BA0
	PS_DDR_BA1_504	AK28	DDR4-BA1
	PS_DDR_BG0_504	AJ27	DDR4-BG0
	PS_DDR_BG1_504	AJ28	DDR4-BG1
	PS_DDR_PARITY_504	AG27	DDR4-PAR
PS_DDR_RAM_RST_N_504		AF27	DDR4-RESET
PS_DDR_ACT_N_504		AH27	DDR4-ACT
PS_DDR_ALERT_N_504		AE26	DDR4-ALERT
PS_DDR_ZQ_504		AF26	
PS_DDR_ODT0_504		AP30	DDR4-ODT0
PS_DDR_ODT1_504		AM31	

XCZU47DR-2FFVE1156E

ADDR_CMD_CTRL



AN28	DDR4-CLK0_P
AP28	DDR4-CLK0_N
AP31	DDR4-CKE0
AL27	
AM27	
AK28	
AN29	DDR4-A0
AP27	DDR4-A1
AP25	DDR4-A2
AP26	DDR4-A3
AN27	DDR4-A4
AN25	DDR4-A5
AK26	DDR4-A6
AK25	DDR4-A7
AJ26	DDR4-A8
AJ25	DDR4-A9
AL28	DDR4-A10
AM26	DDR4-A11
AL29	DDR4-A12
AM25	DDR4-A13
AM29	DDR4-A14
AL26	DDR4-A15
AH25	DDR4-A16
AG25	DDR4-A17
AN30	DDR4-CS
AM30	
AG26	DDR4-BA0
AK28	DDR4-BA1
AJ27	DDR4-BG0
AJ28	DDR4-BG1
AG27	DDR4-PAR
AF27	DDR4-RESET
AH27	DDR4-ACT
AE26	DDR4-ALERT
AF26	
AP30	DDR4-ODT0
AM31	



UIK

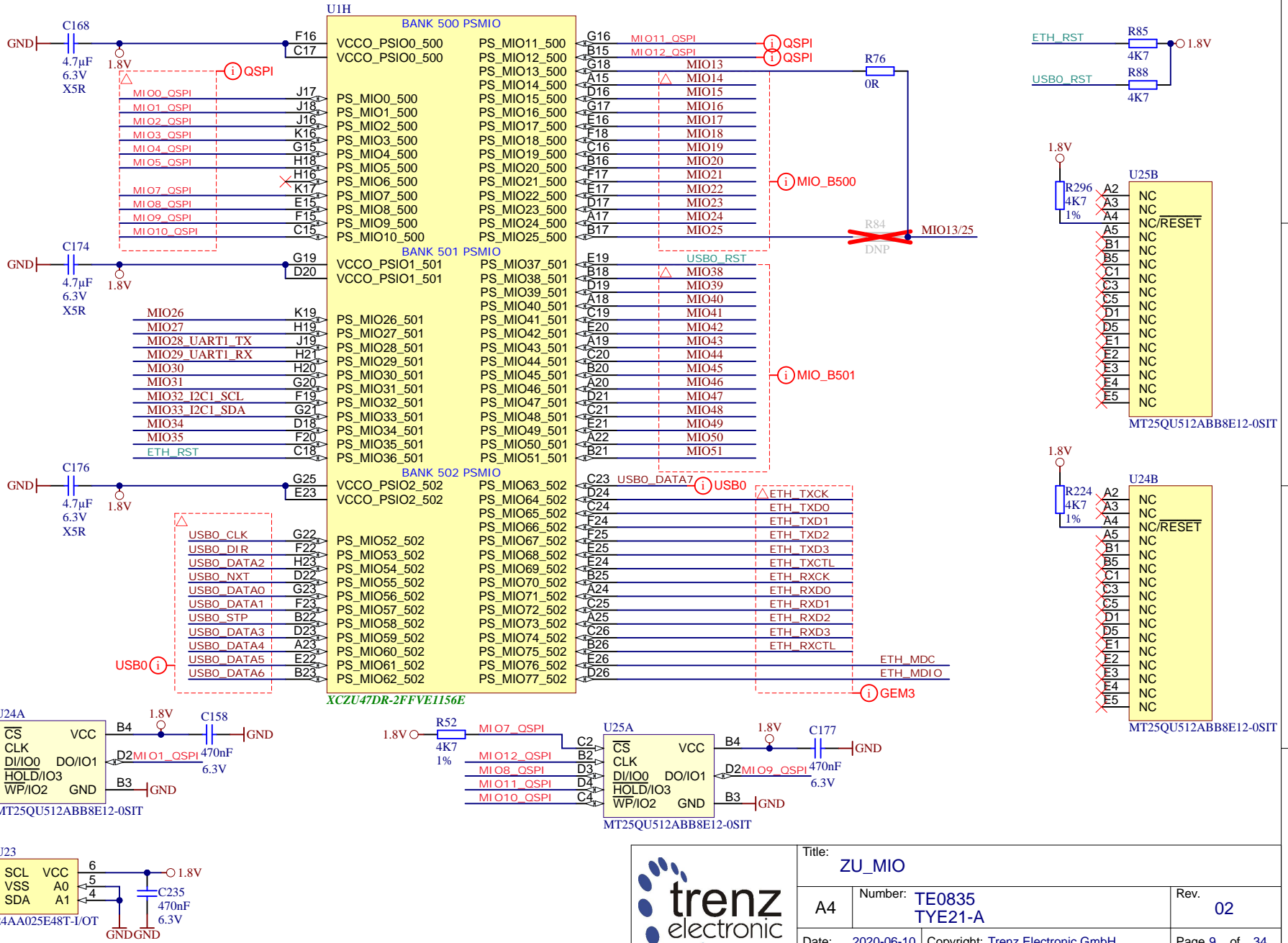
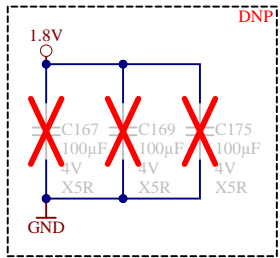
BANK 504 PSDDR

DQ0	AP22	PS_DDR_DQ0_504	PS_DDR_DQ32_504	AE29	DQ32
DQ1	AM21	PS_DDR_DQ1_504	PS_DDR_DQ33_504	AF29	DQ33
DQ2	AP21	PS_DDR_DQ2_504	PS_DDR_DQ34_504	AE28	DQ34
DQ3	AL21	PS_DDR_DQ3_504	PS_DDR_DQ35_504	AF28	DQ35
DQ4	AP18	PS_DDR_DQ4_504	PS_DDR_DQ36_504	AJ30	DQ36
DQ5	AN19	PS_DDR_DQ5_504	PS_DDR_DQ37_504	AH29	DQ37
DQ6	AM19	PS_DDR_DQ6_504	PS_DDR_DQ38_504	AH30	DQ38
DQ7	AL19	PS_DDR_DQ7_504	PS_DDR_DQ39_504	AH28	DQ39
DQ8	AL22	PS_DDR_DQ8_504	PS_DDR_DQ40_504	AE30	DQ40
DQ9	AK23	PS_DDR_DQ9_504	PS_DDR_DQ41_504	AD30	DQ41
DQ10	AM22	PS_DDR_DQ10_504	PS_DDR_DQ42_504	AD28	DQ42
DQ11	AN21	PS_DDR_DQ11_504	PS_DDR_DQ43_504	AD27	DQ43
DQ12	AK24	PS_DDR_DQ12_504	PS_DDR_DQ44_504	AB29	DQ44
DQ13	AL24	PS_DDR_DQ13_504	PS_DDR_DQ45_504	AC28	DQ45
DQ14	AN24	PS_DDR_DQ14_504	PS_DDR_DQ46_504	AB28	DQ46
DQ15	AM24	PS_DDR_DQ15_504	PS_DDR_DQ47_504	AC27	DQ47
DQ16	AJ25	PS_DDR_DQ16_504	PS_DDR_DQ48_504	AG34	DQ48
DQ17	AK21	PS_DDR_DQ17_504	PS_DDR_DQ49_504	AH33	DQ49
DQ18	AK20	PS_DDR_DQ18_504	PS_DDR_DQ50_504	AH34	DQ50
DQ19	AK19	PS_DDR_DQ19_504	PS_DDR_DQ51_504	AH32	DQ51
DQ20	AG21	PS_DDR_DQ20_504	PS_DDR_DQ52_504	AK34	DQ52
DQ21	AG19	PS_DDR_DQ21_504	PS_DDR_DQ53_504	AK33	DQ53
DQ22	AG20	PS_DDR_DQ22_504	PS_DDR_DQ54_504	AK31	DQ54
DQ23	AH19	PS_DDR_DQ23_504	PS_DDR_DQ55_504	AK30	DQ55
DQ24	AE23	PS_DDR_DQ24_504	PS_DDR_DQ56_504	AG32	DQ56
DQ25	AF23	PS_DDR_DQ25_504	PS_DDR_DQ57_504	AF31	DQ57
DQ26	AE25	PS_DDR_DQ26_504	PS_DDR_DQ58_504	AF34	DQ58
DQ27	AE24	PS_DDR_DQ27_504	PS_DDR_DQ59_504	AE34	DQ59
DQ28	AH23	PS_DDR_DQ28_504	PS_DDR_DQ60_504	AD32	DQ60
DQ29	AH22	PS_DDR_DQ29_504	PS_DDR_DQ61_504	AE31	DQ61
DQ30	AJ23	PS_DDR_DQ30_504	PS_DDR_DQ62_504	AD34	DQ62
DQ31	AH24	PS_DDR_DQ31_504	PS_DDR_DQ63_504	AD33	DQ63
			PS_DDR_DQ64_504	AP32	
			PS_DDR_DQ65_504	AM32	
DDR4-DQS0_P	AN20	PS_DDR_DQS_P0_504	PS_DDR_DQ66_504	AL31	
DDR4-DQS0_N	AP20	PS_DDR_DQS_N0_504	PS_DDR_DQ67_504	AL32	
DDR4-DQS1_P	AN23	PS_DDR_DQS_P1_504	PS_DDR_DQ68_504	AP33	
DDR4-DQS1_N	AP23	PS_DDR_DQS_N1_504	PS_DDR_DQ69_504	AM34	
DDR4-DQS2_P	AJ20	PS_DDR_DQS_P2_504	PS_DDR_DQ70_504	AN34	
DDR4-DQS2_N	AJ21	PS_DDR_DQS_N2_504	PS_DDR_DQ71_504	AL34	
DDR4-DQS3_P	AF21	PS_DDR_DQS_P3_504			
DDR4-DQS3_N	AG21	PS_DDR_DQS_N3_504			
DDR4-DQS4_P	AG29	PS_DDR_DQS_P4_504			
DDR4-DQS4_N	AG30	PS_DDR_DQS_N4_504	PS_DDR_DM0_504	AM20	DDR4-DM0
DDR4-DQS5_P	AC29	PS_DDR_DQS_P5_504	PS_DDR_DM1_504	AL23	DDR4-DM1
DDR4-DQS5_N	AC30	PS_DDR_DQS_N5_504	PS_DDR_DM2_504	AH20	DDR4-DM2
DDR4-DQS6_P	AJ32	PS_DDR_DQS_P6_504	PS_DDR_DM3_504	AG22	DDR4-DM3
DDR4-DQS6_N	AJ33	PS_DDR_DQS_N6_504	PS_DDR_DM4_504	AG31	DDR4-DM4
DDR4-DQS7_P	AF32	PS_DDR_DQS_P7_504	PS_DDR_DM5_504	AD31	DDR4-DM5
DDR4-DQS7_N	AF33	PS_DDR_DQS_N7_504	PS_DDR_DM6_504	AJ31	DDR4-DM6
	AN32	PS_DDR_DQS_P8_504	PS_DDR_DM7_504	AE33	DDR4-DM7
	AN33	PS_DDR_DQS_N8_504	PS_DDR_DM8_504	AL33	

XCZU47DR-2FFVE1156E



Title: ZU_PSDDR			
A4	Number: TE0835 TYE21-A	Rev. 02	
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 8 of 34	
Filename: ZU_PSDDR.SchDoc			



Title: ZU_MIO		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 9 of 34
Filename: ZU_MIO.SchDoc		

A

B

C

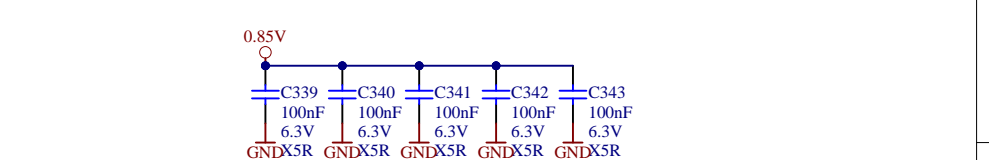
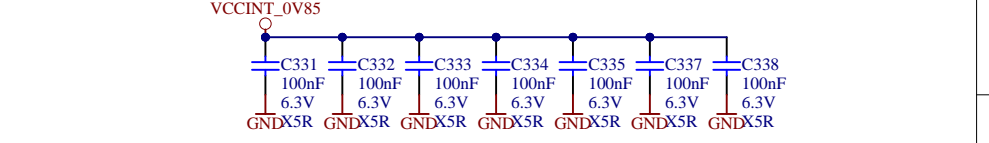
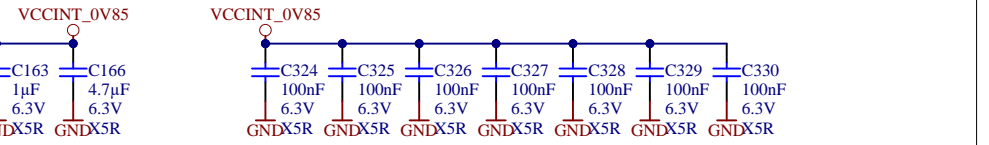
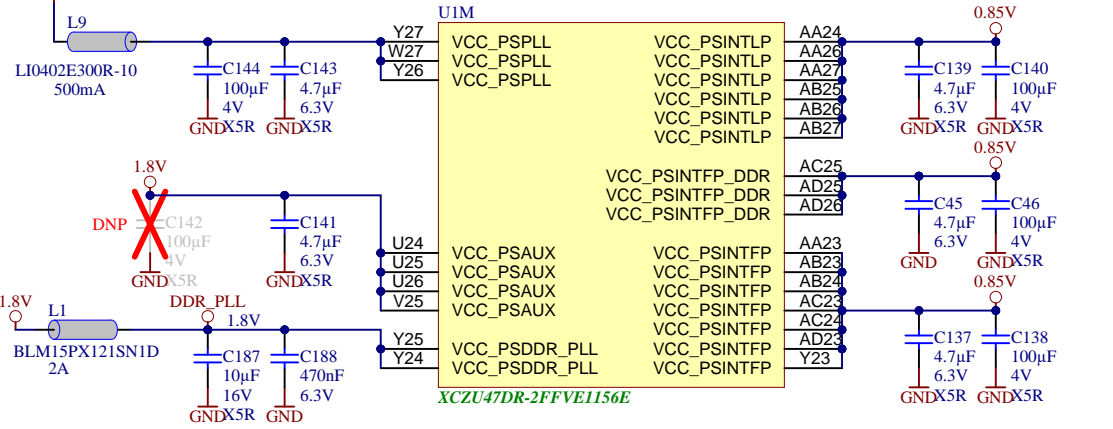
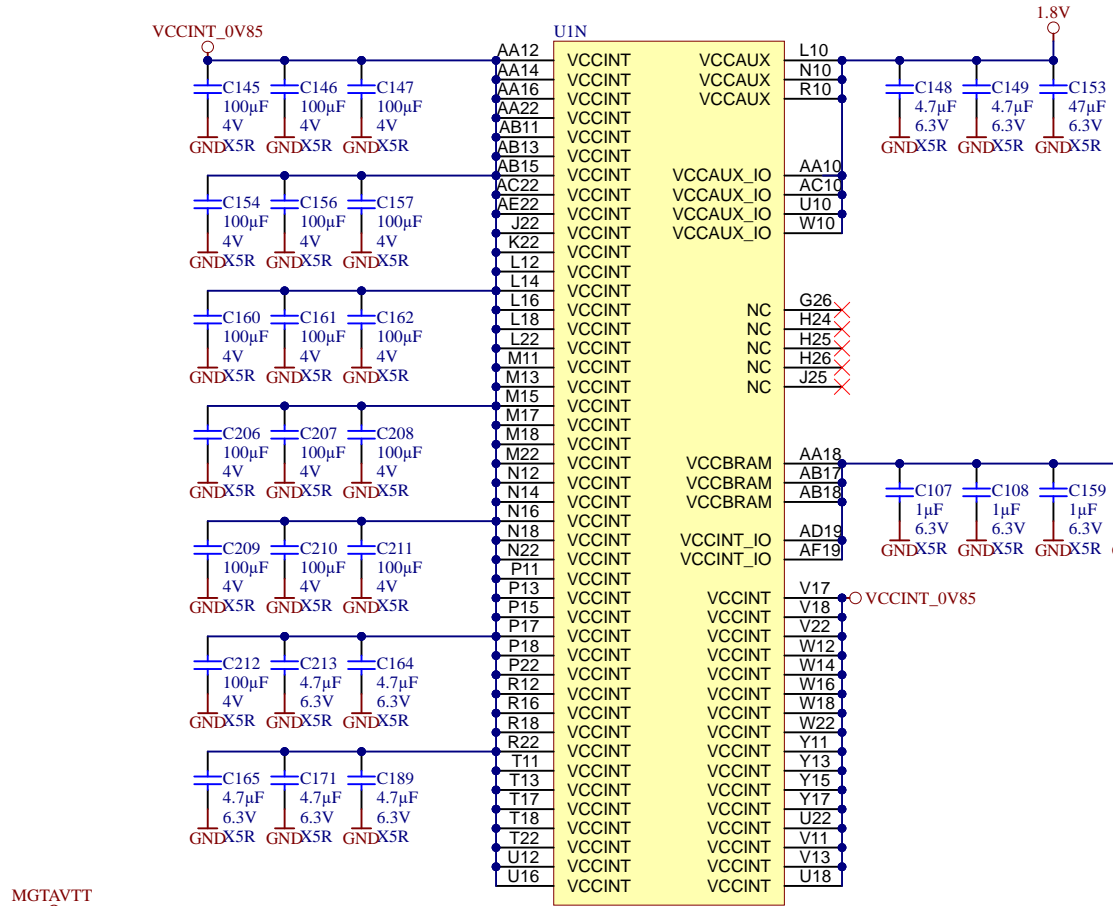
D

A

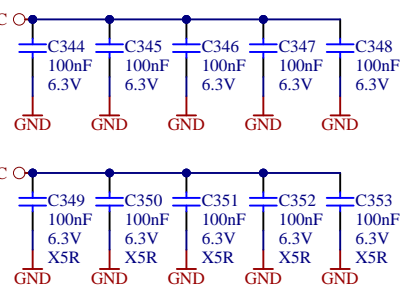
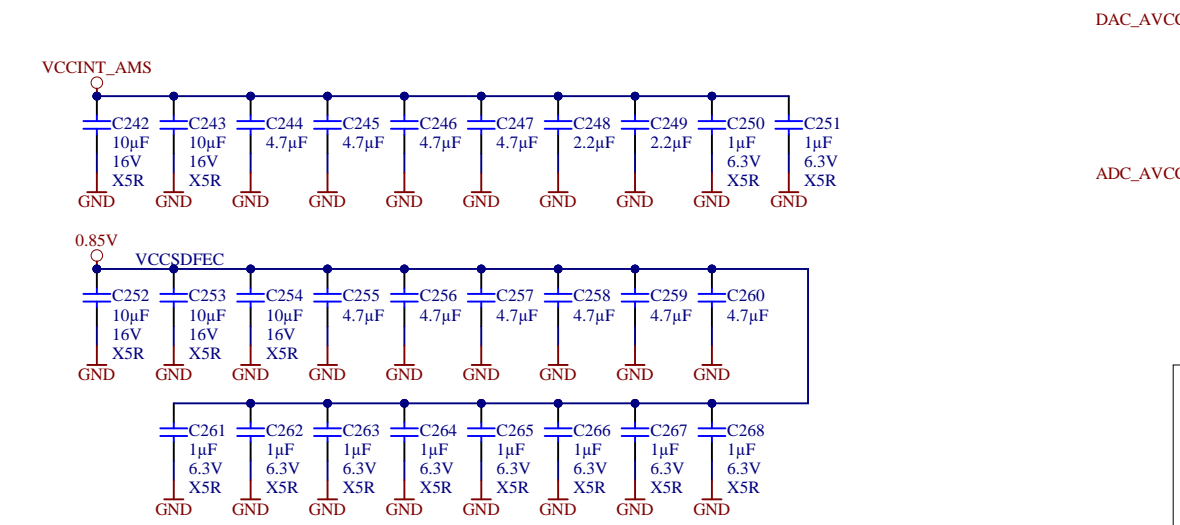
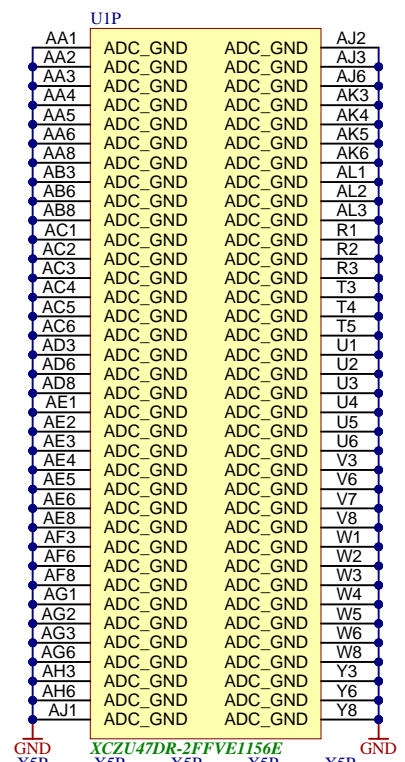
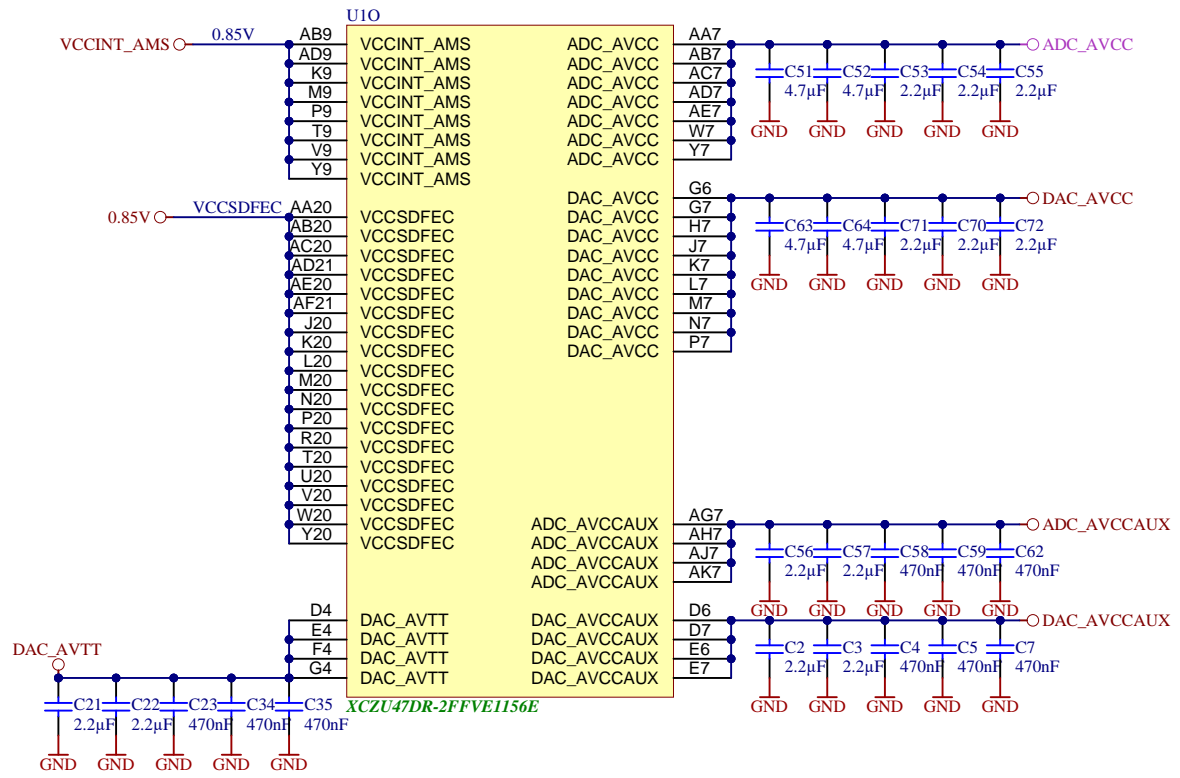

B

C

D

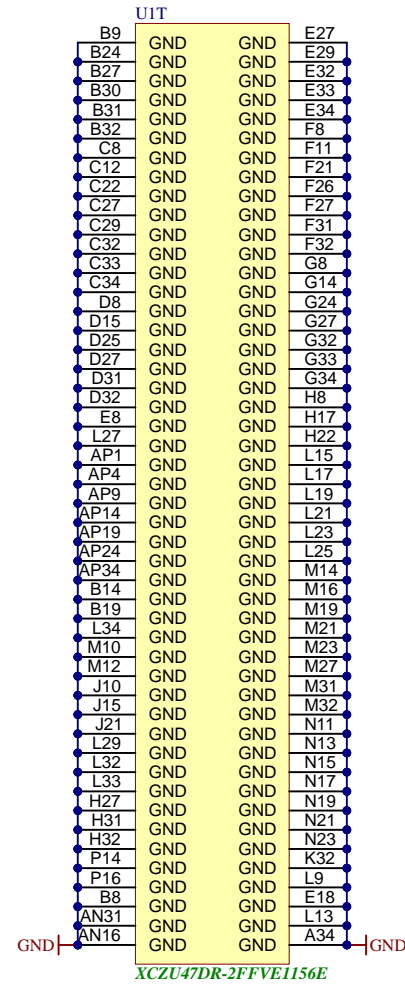
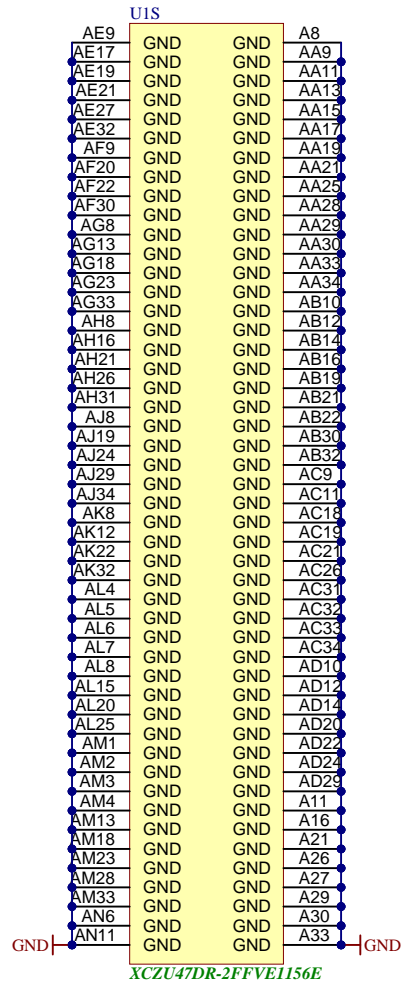
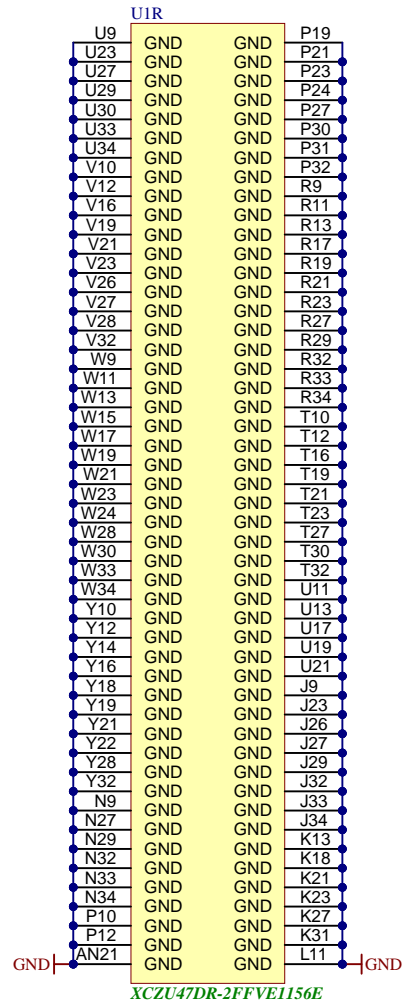


Title: ZU_PWR		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	
Filename: ZU_PWR.SchDoc		Page 10 of 34

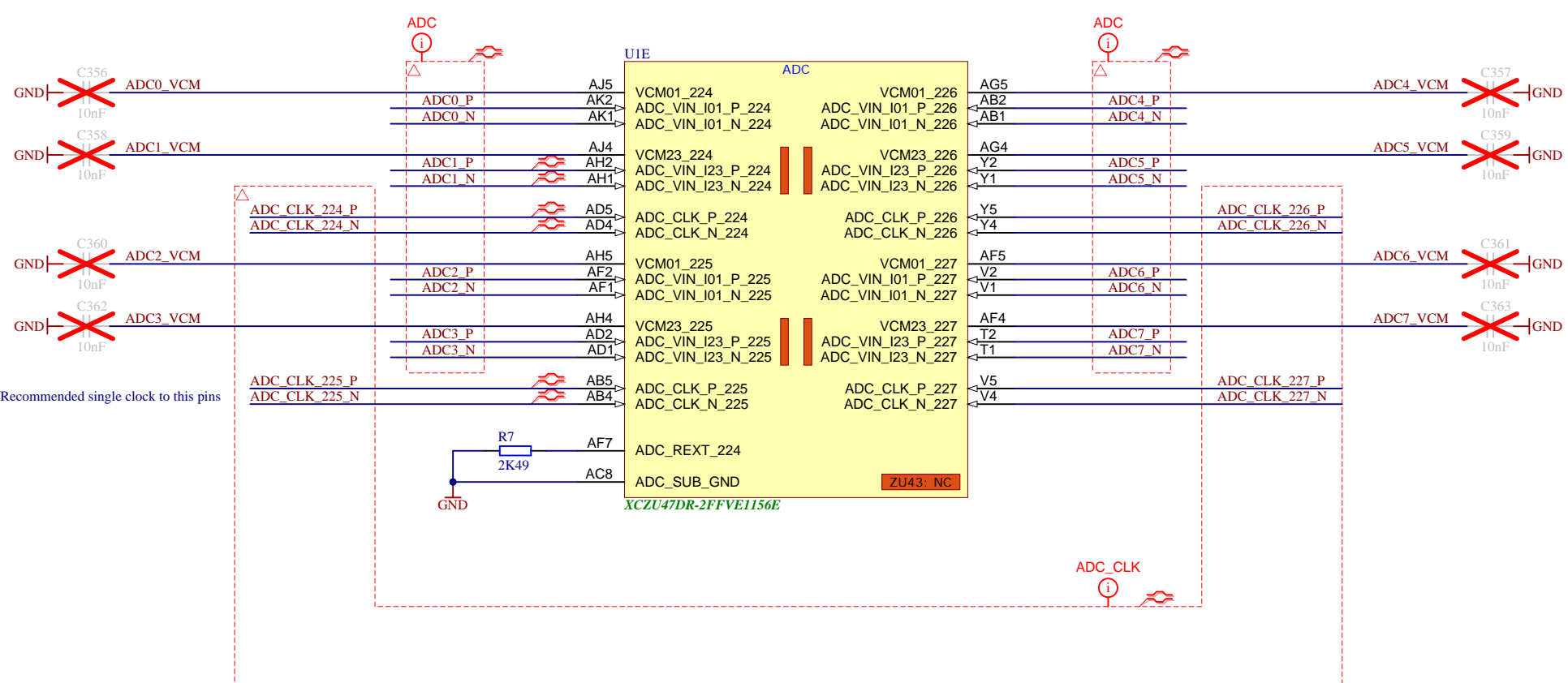



trenz electronic

Title: ZU_PWR2		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 11 of 34
Filename: ZU_PWR2.SchDoc		



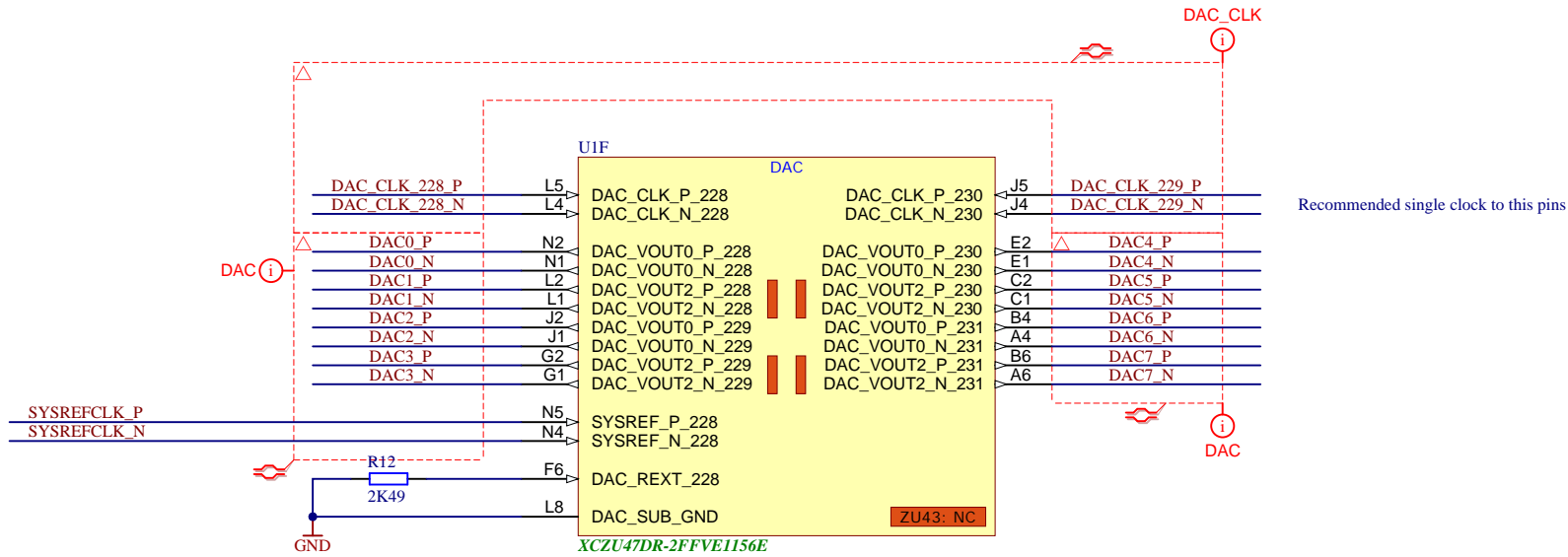
Title: ZU_PWR3		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 12 of 34
Filename: ZU_PWR3.SchDoc		



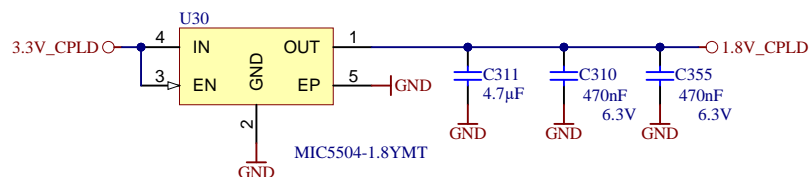
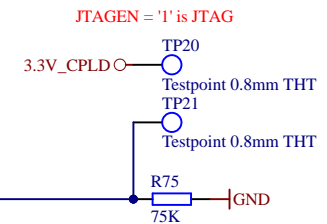
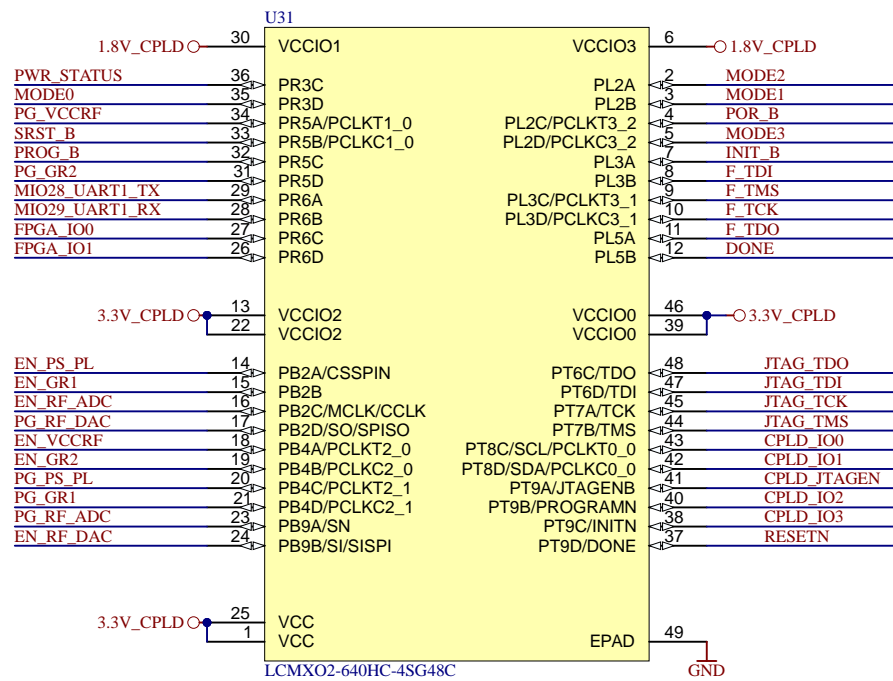
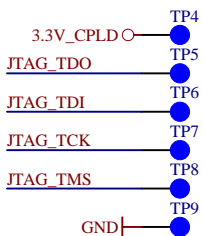
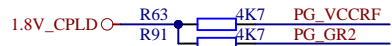
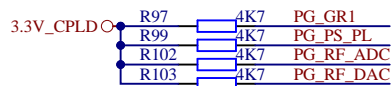
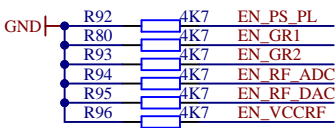
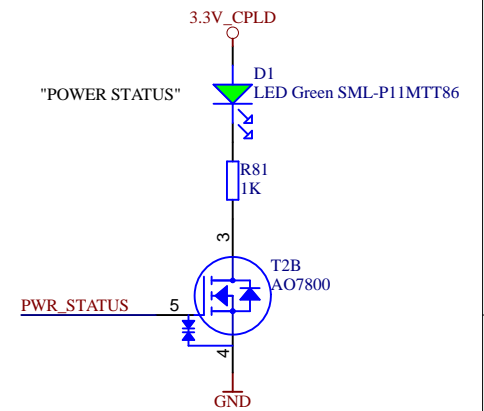
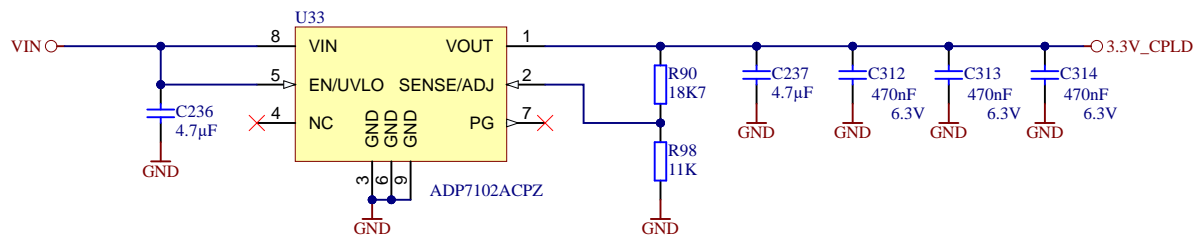
	Title: ZU_ADC	
	A4	Number: TE0835 TYE21-A
	Date: 2020-06-10	Copyright: Trenz Electronic GmbH
	Filename: ZU_ADC.SchDoc	

Rev. 02

Page 13 of 34

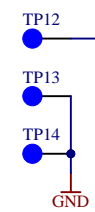


	Title: ZU_DAC	
	A4	Number: TE0835 TYE21-A
	Date: 2020-06-10	Copyright: Trenz Electronic GmbH
	Filename: ZU_DAC.SchDoc	
	Rev. 02	Page 14 of 34

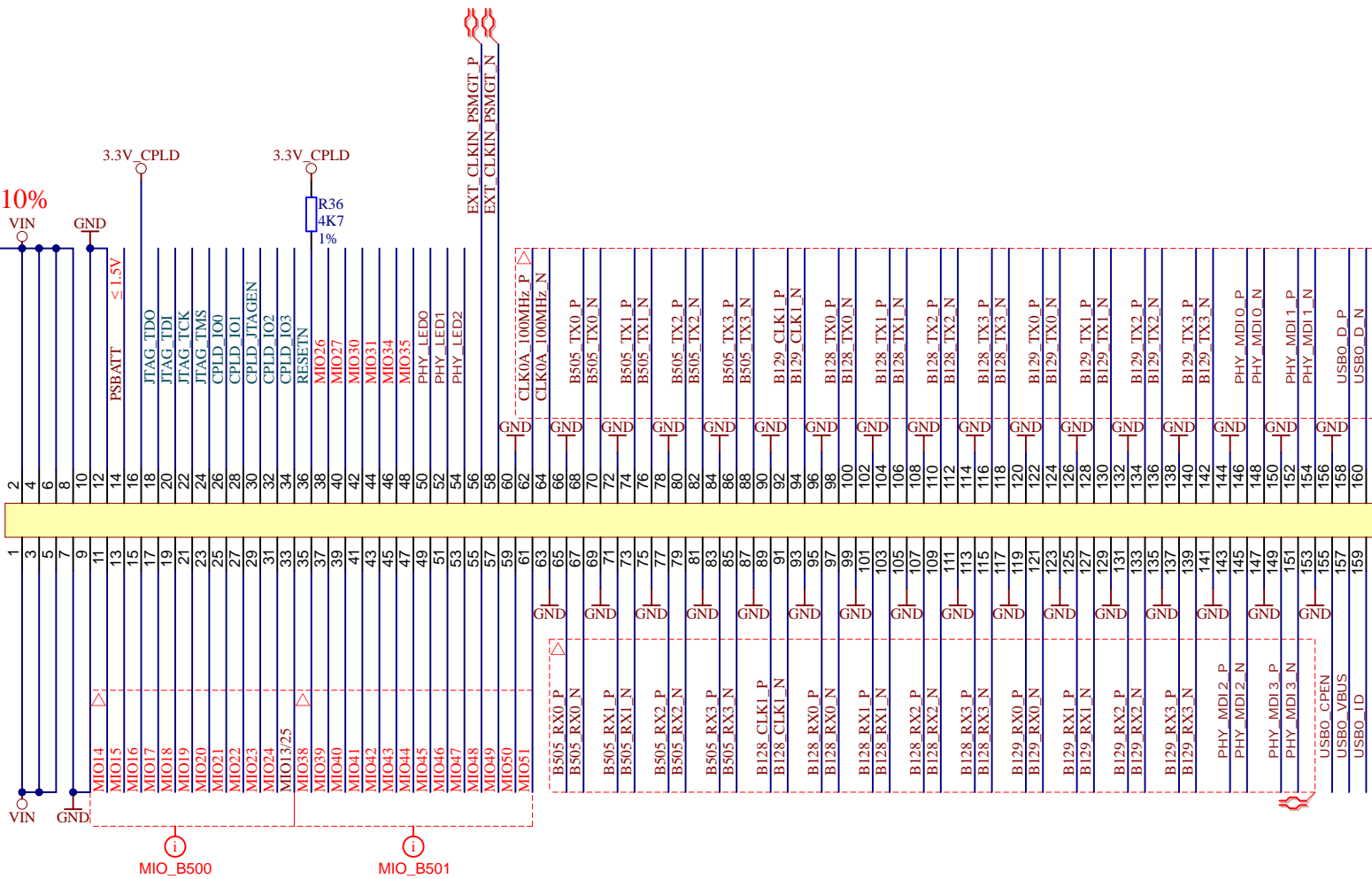


Title: CPLD		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 15 of 34
Filename: CPLD.SchDoc		

VIN=5V±10%



J1



MIO_B500

MIO_B501

ST5-80-1.50-L-D-P-TR



Title: B2B		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	
Filename: B2B.SchDoc		Page 16 of 34

1

2

3

4

A

A

B

B

C

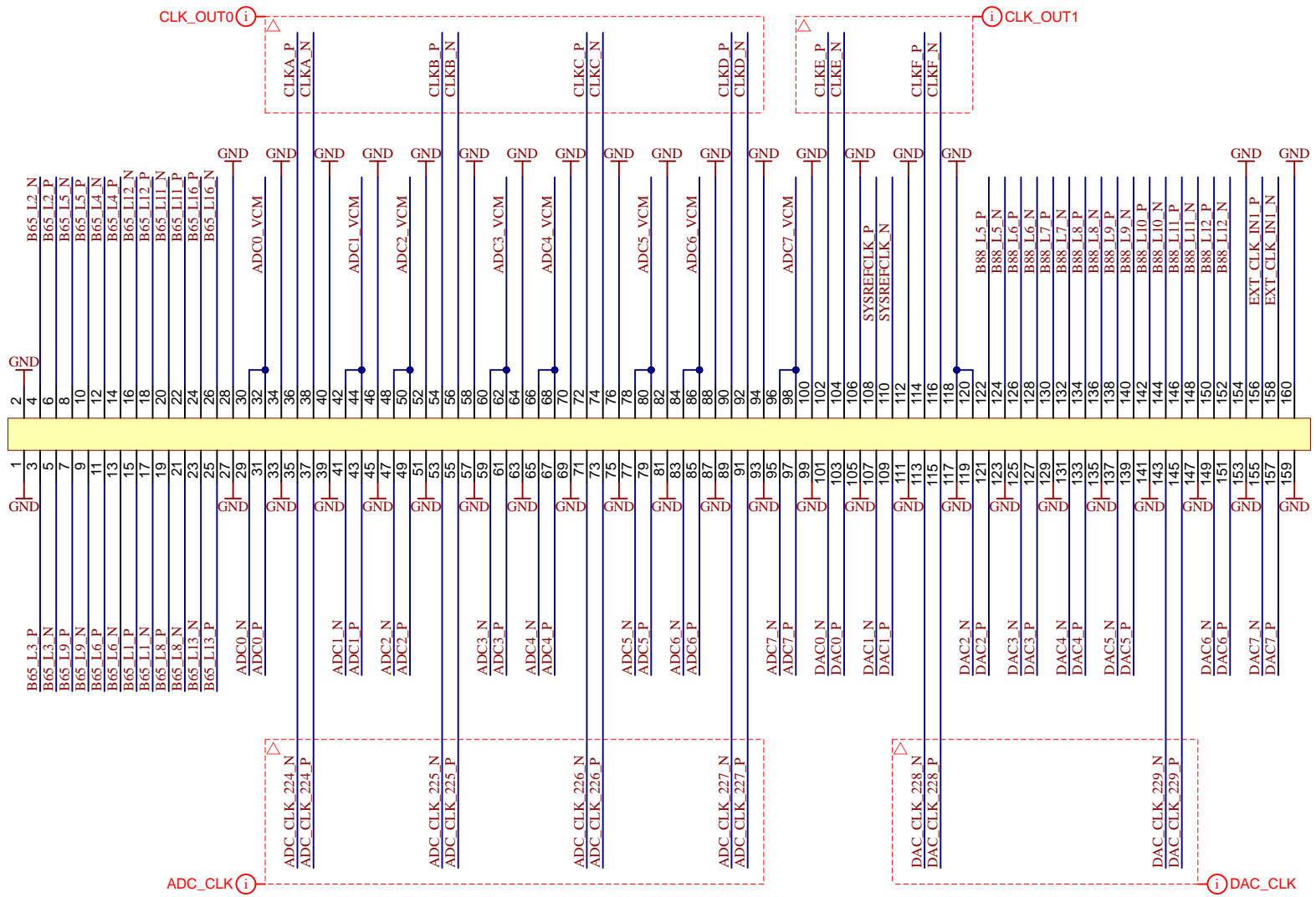
C

D

D

J2

ST5-80-1.50-L-D-P-TR



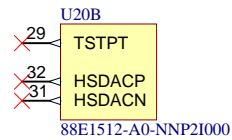
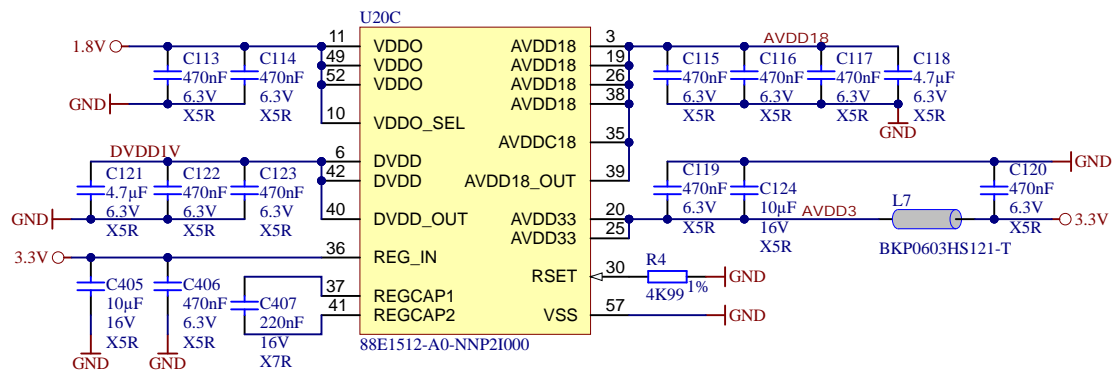
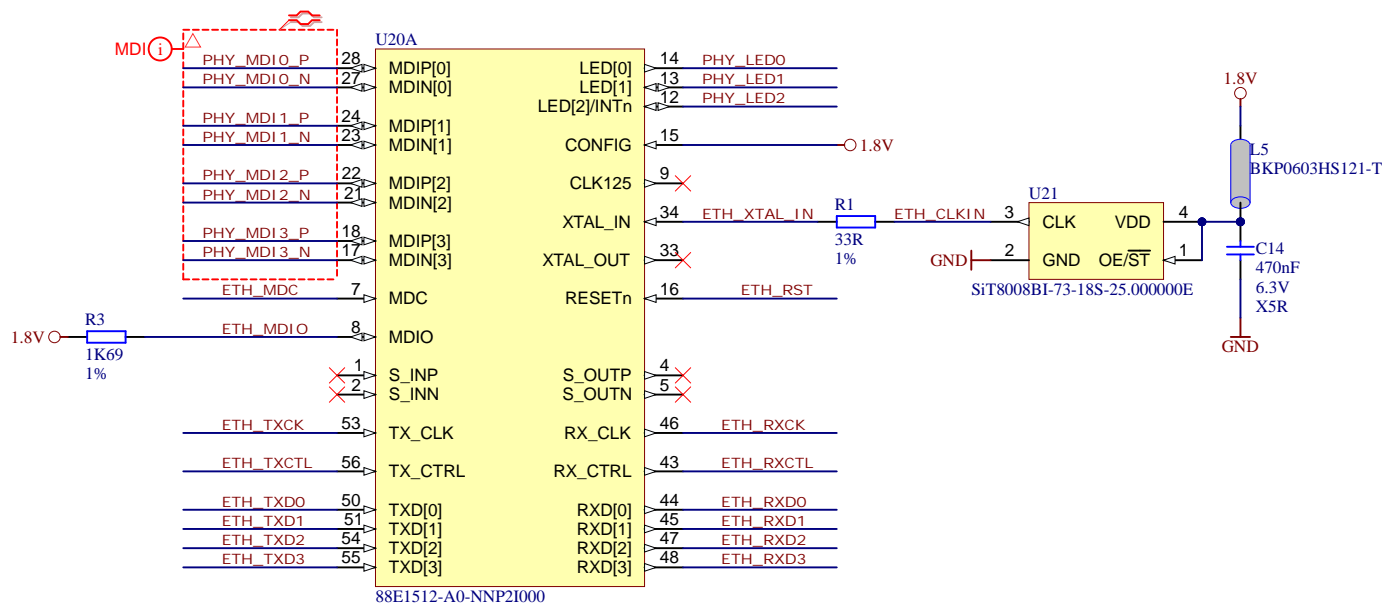
Title: B2B_2		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 17 of 34
Filename: B2B_2.SchDoc		

1

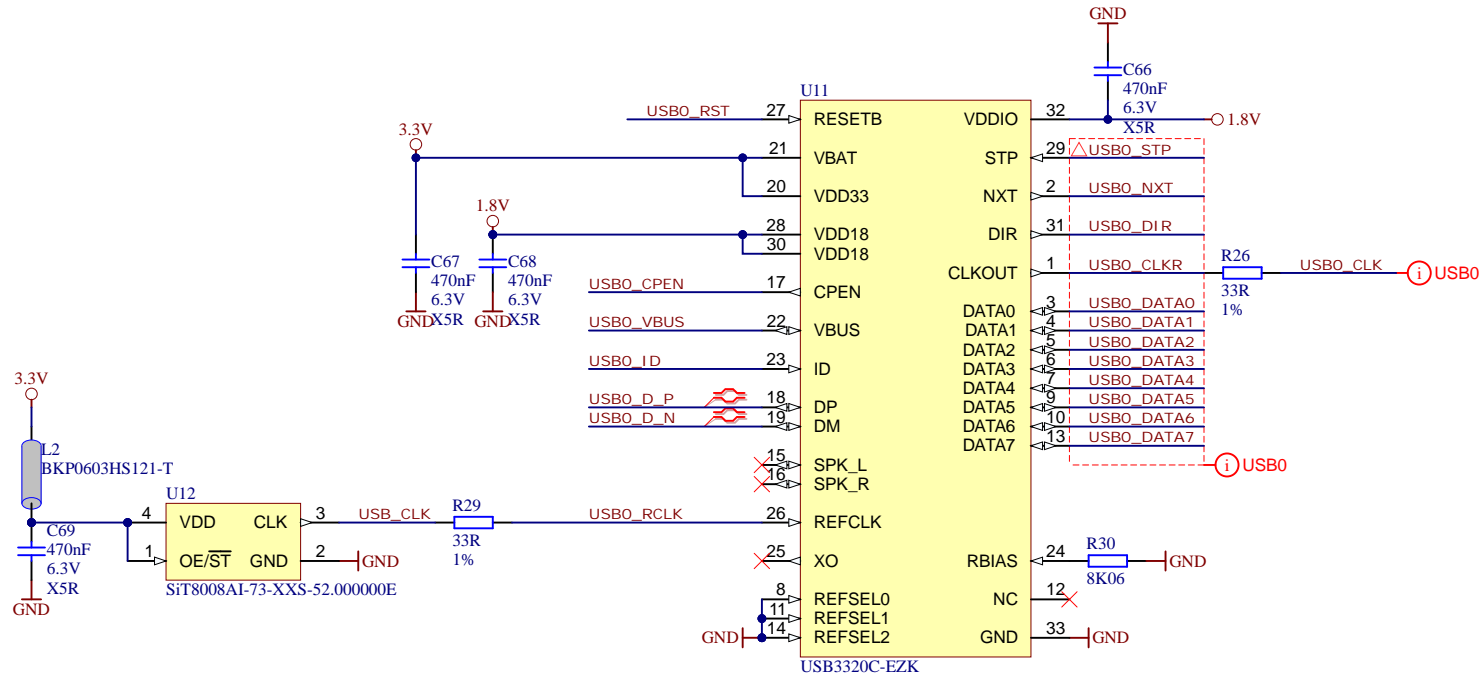
2


3

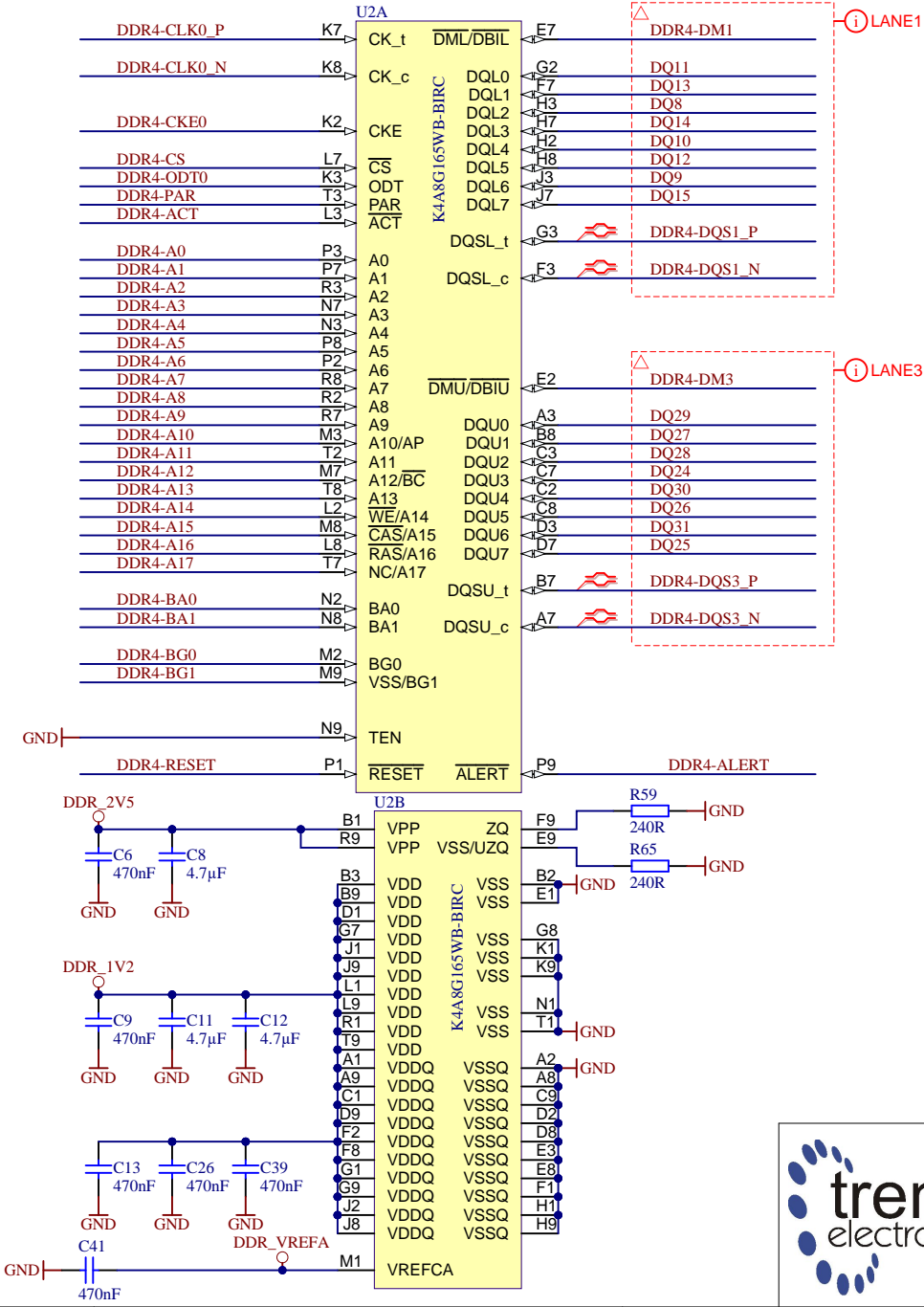
4



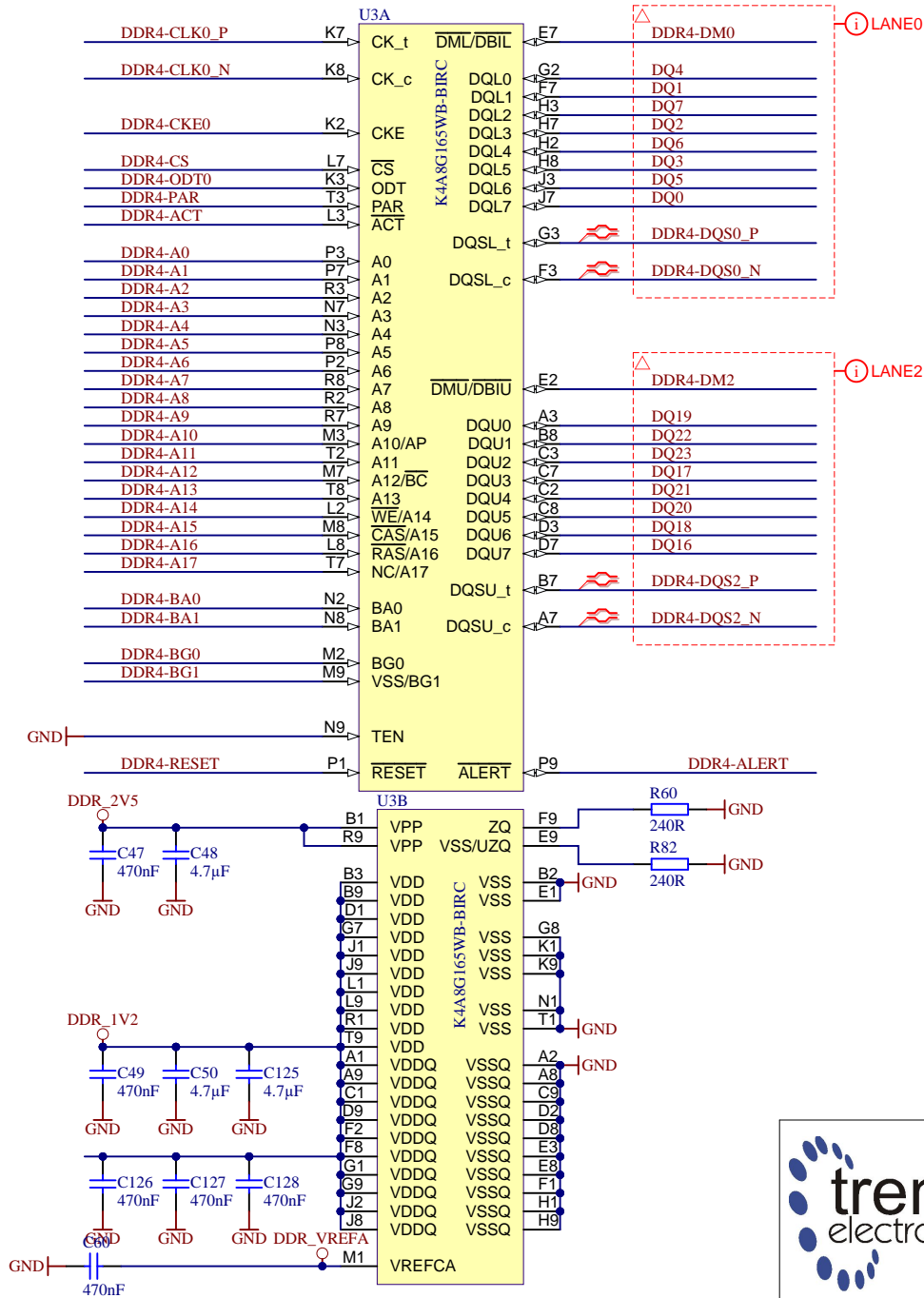
Title: Ethernet		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 18 of 34
Filename: Ethernet.SchDoc		



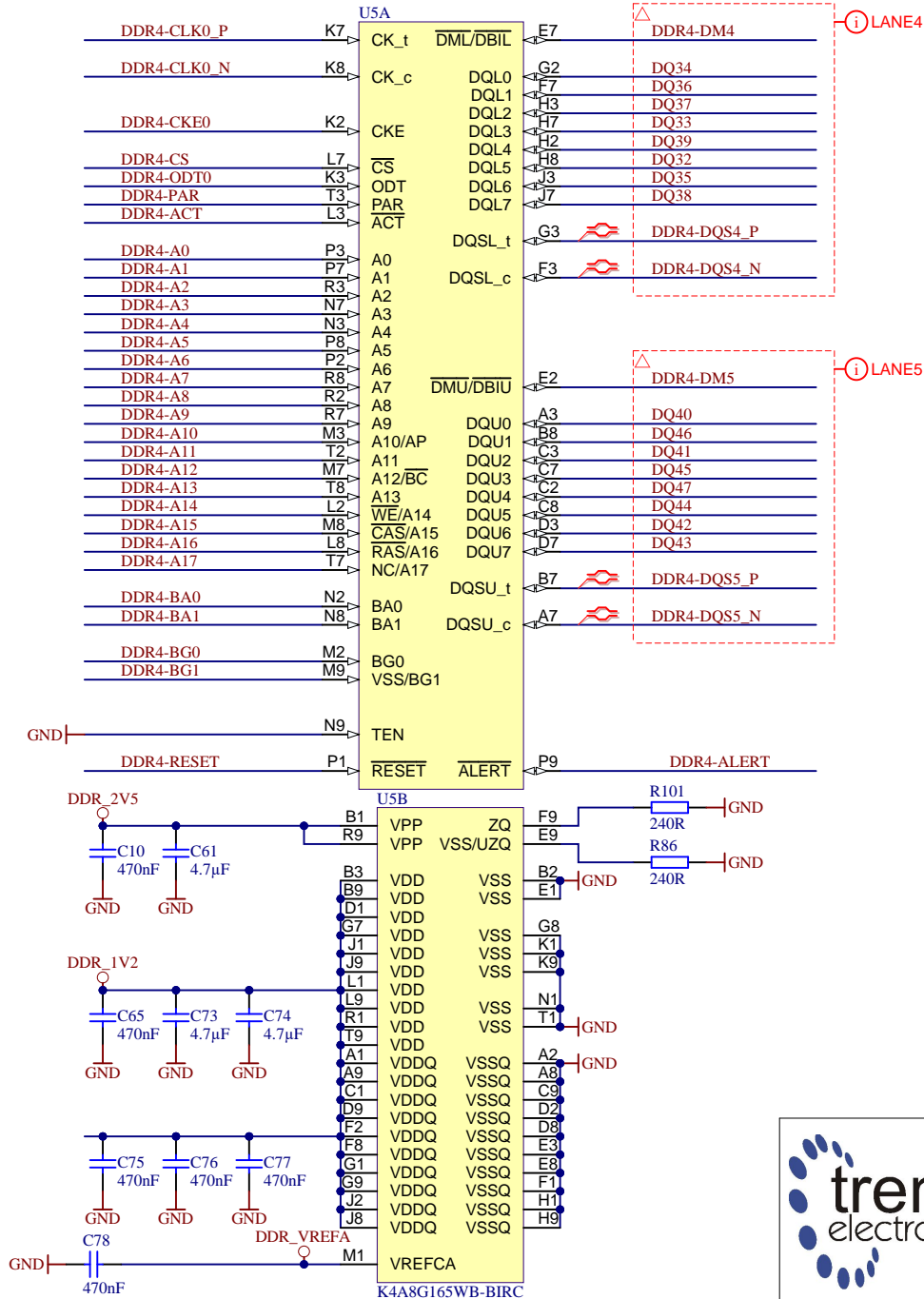
			Title: USB-PHY	
			A4	Number: TE0835 TYE21-A
Date: 2020-06-10		Copyright: Trenz Electronic GmbH		Page 19 of 34
Filename: USB-PHY.SchDoc				



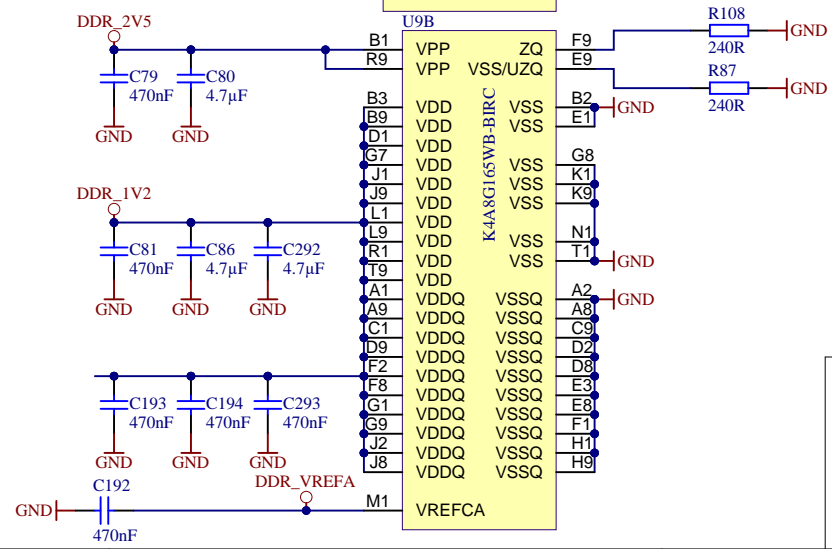
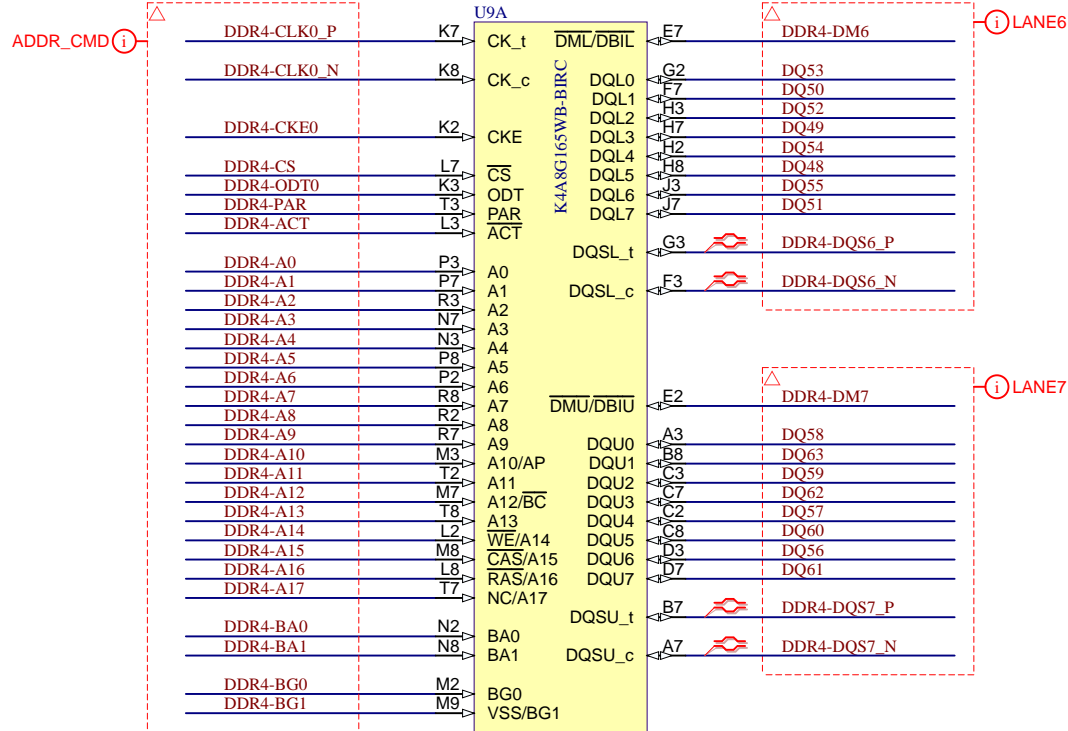
Title: DDR4-RAM		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 20 of 34
Filename: DDR4-RAM.SchDoc		



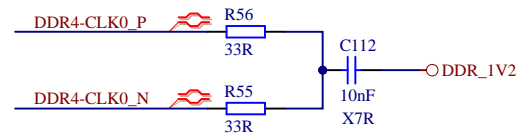
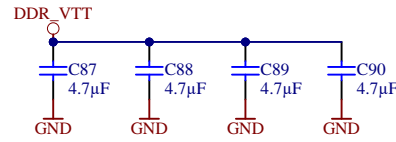
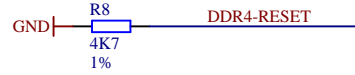
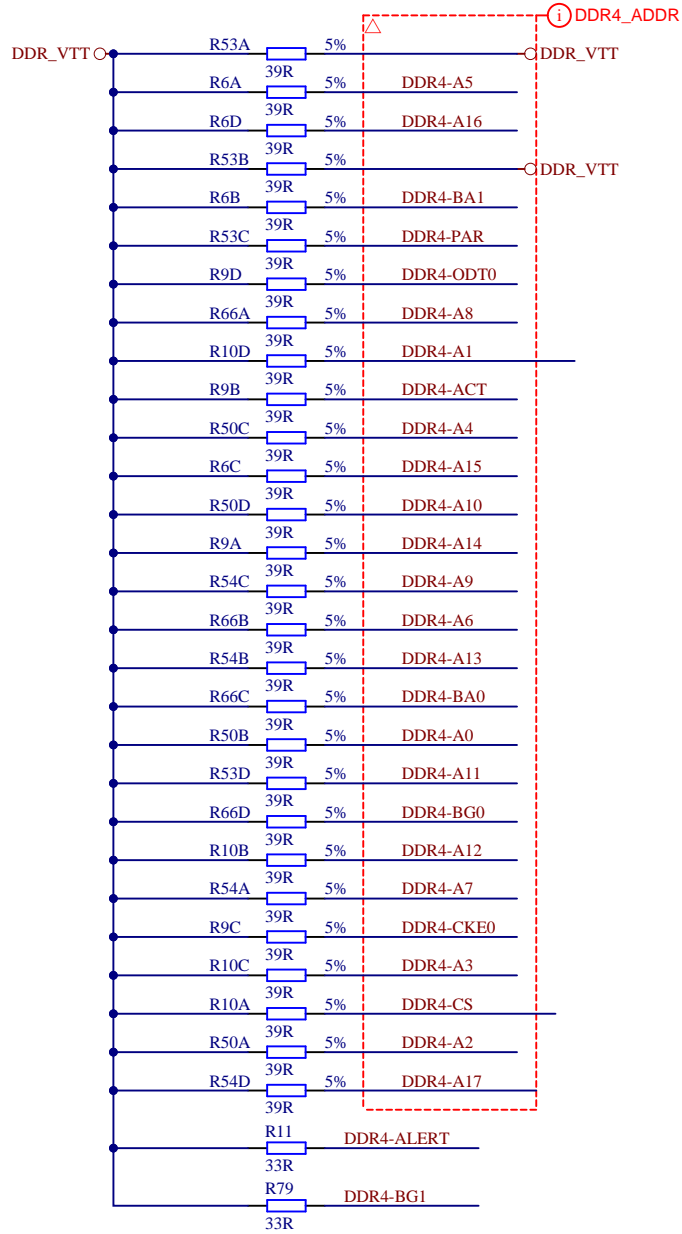
Title: DDR4-RAM_2		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 21 of 34
Filename: DDR4-RAM_2.SchDoc		



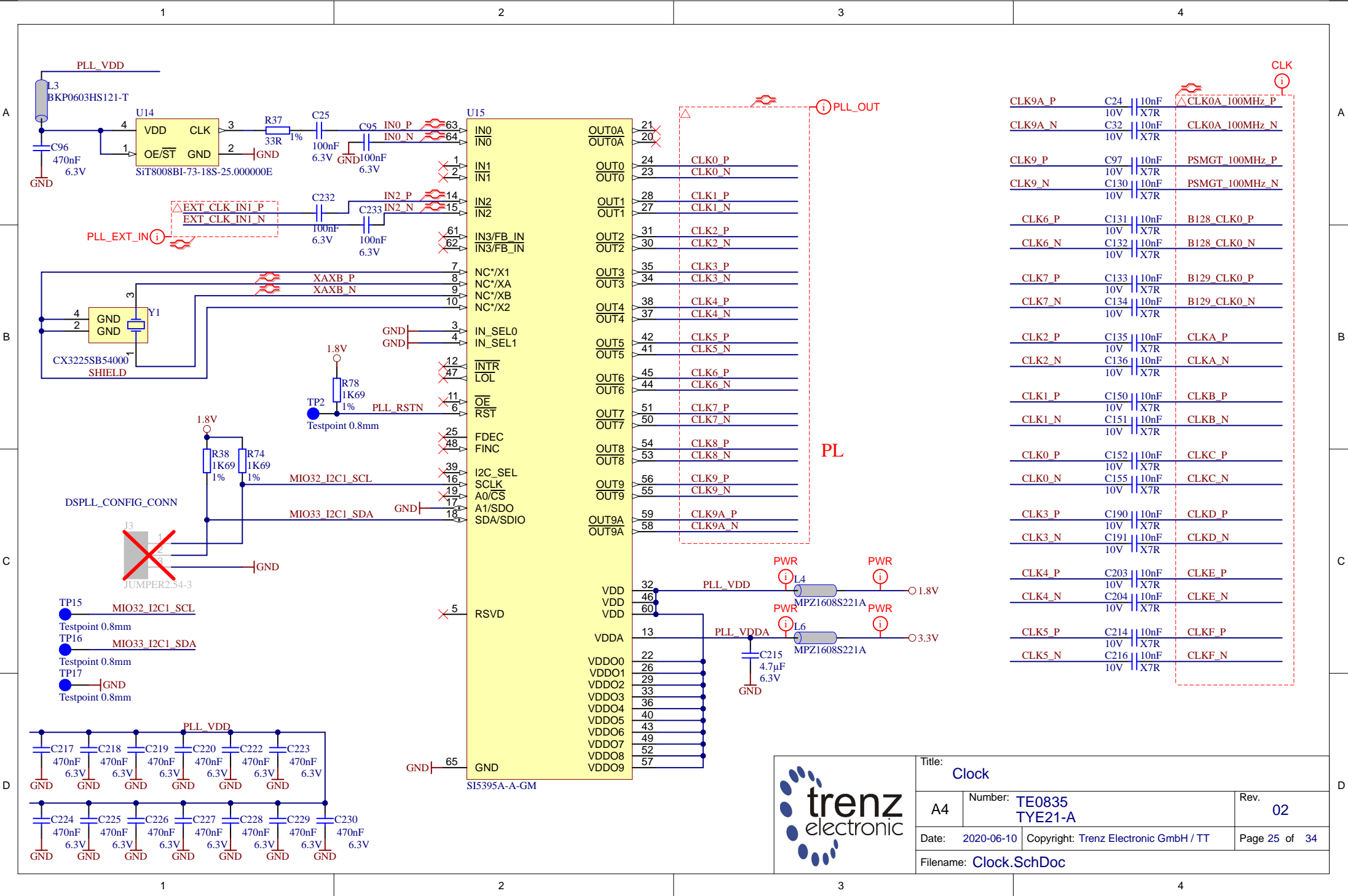
Title: DDR4-RAM_3		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 22 of 34
Filename: DDR4-RAM_3.SchDoc		



Title: DDR4-RAM_4		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 23 of 34
Filename: DDR4-RAM_4.SchDoc		



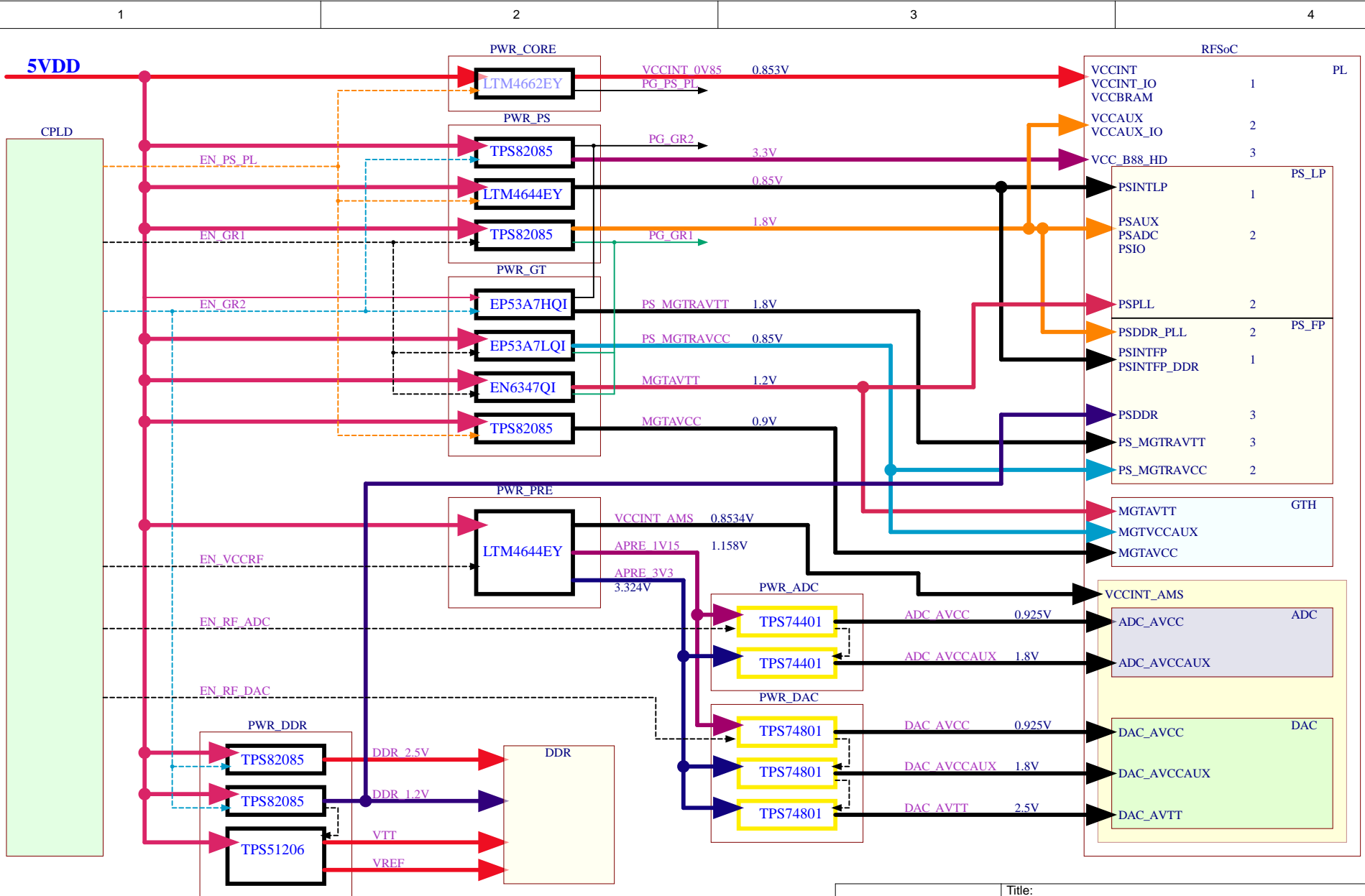
Title: DDR4-TERM		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 24 of 34
Filename: DDR4-TERM.SchDoc		



CLK9A_P	C24	10nF	CLK0A_100MHz_P
CLK9A_N	C32	10nF	CLK0A_100MHz_N
CLK9_P	C97	10nF	PSMGT_100MHz_P
CLK9_N	C130	10nF	PSMGT_100MHz_N
CLK6_P	C131	10nF	B128_CLK0_P
CLK6_N	C132	10nF	B128_CLK0_N
CLK7_P	C133	10nF	B129_CLK0_P
CLK7_N	C134	10nF	B129_CLK0_N
CLK2_P	C135	10nF	CLKA_P
CLK2_N	C136	10nF	CLKA_N
CLK1_P	C150	10nF	CLKB_P
CLK1_N	C151	10nF	CLKB_N
CLK0_P	C152	10nF	CLKC_P
CLK0_N	C155	10nF	CLKC_N
CLK3_P	C190	10nF	CLKD_P
CLK3_N	C191	10nF	CLKD_N
CLK4_P	C203	10nF	CLKE_P
CLK4_N	C204	10nF	CLKE_N
CLK5_P	C214	10nF	CLKF_P
CLK5_N	C216	10nF	CLKF_N



Title: Clock		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 25 of 34
Filename: Clock.SchDoc		

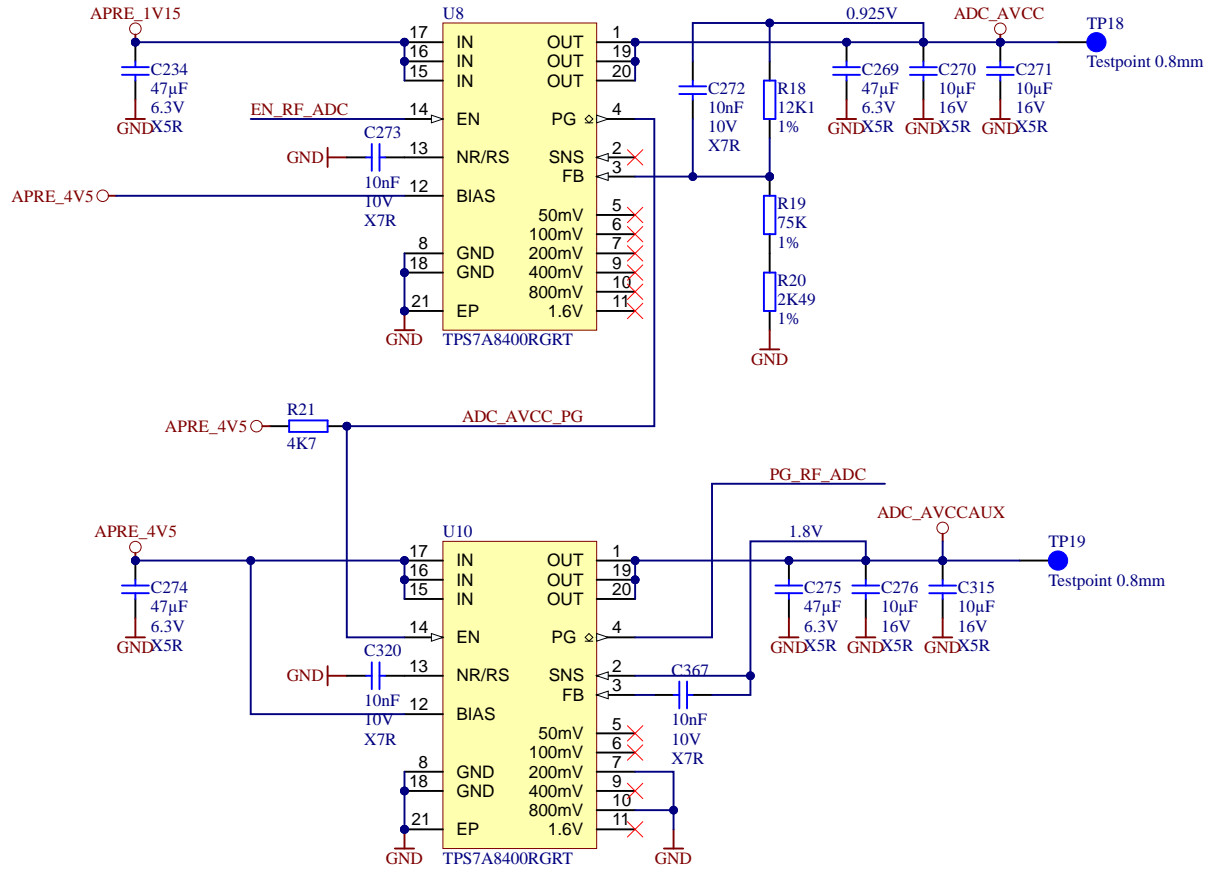



Legend for regulator types:

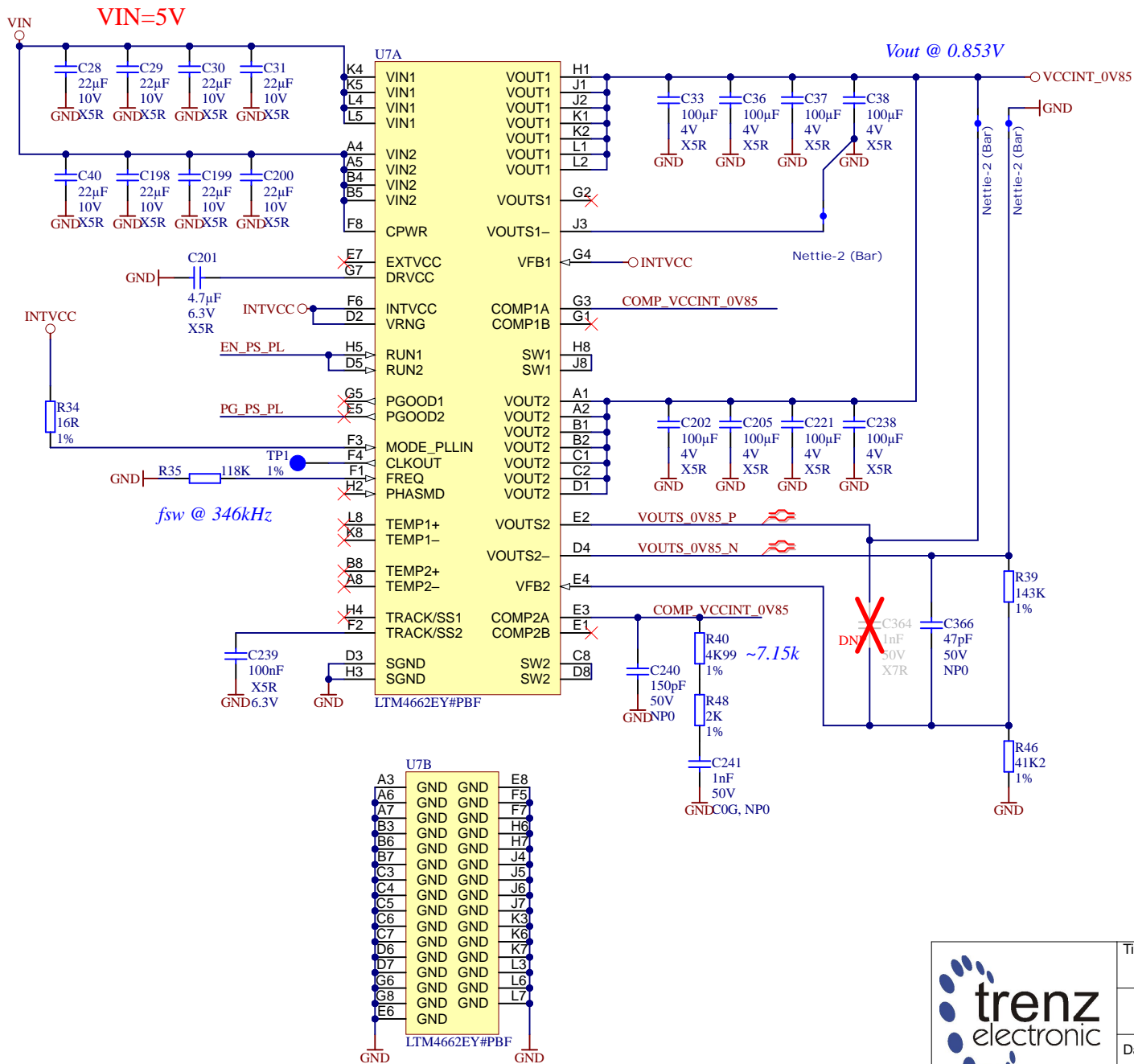
- DCDC (black box)
- LDO (yellow box)



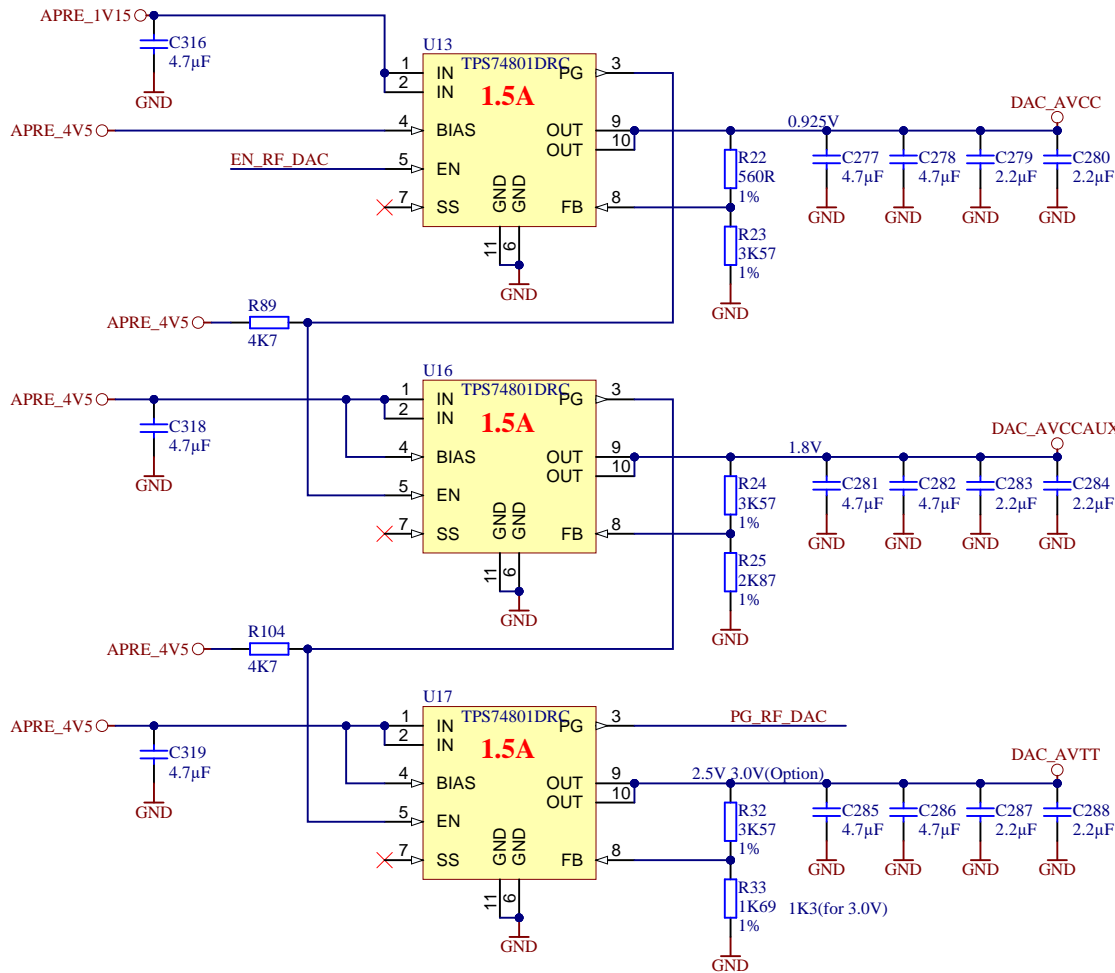
Title: PWR_Structure		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	
Filename: PWR_Structure.SchDoc		Page 26 of 34





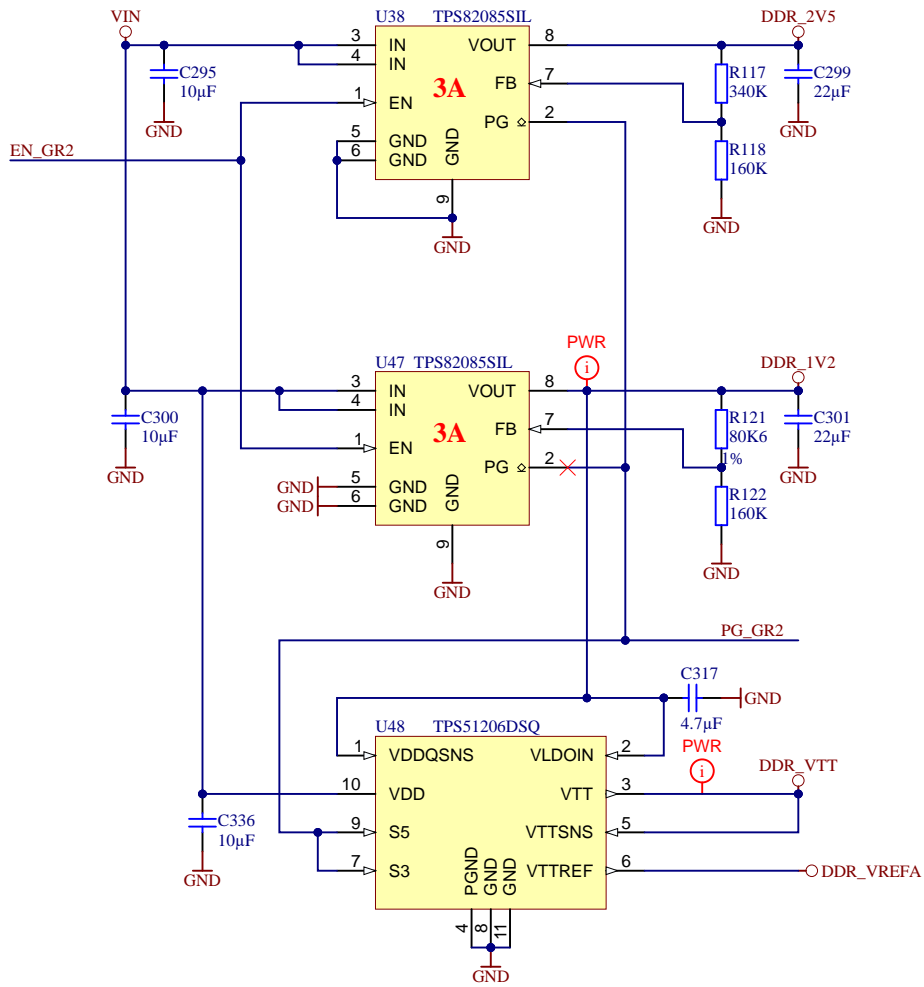
Title: PWR_ADC		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 27 of 34
Filename: PWR_ADC.SchDoc		




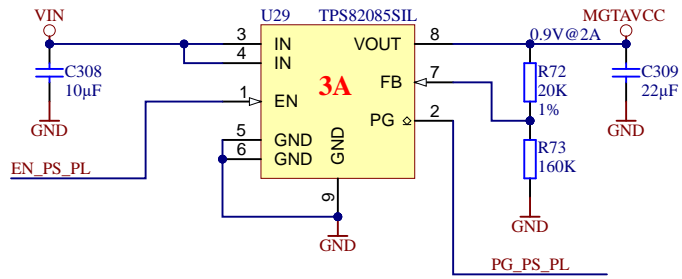
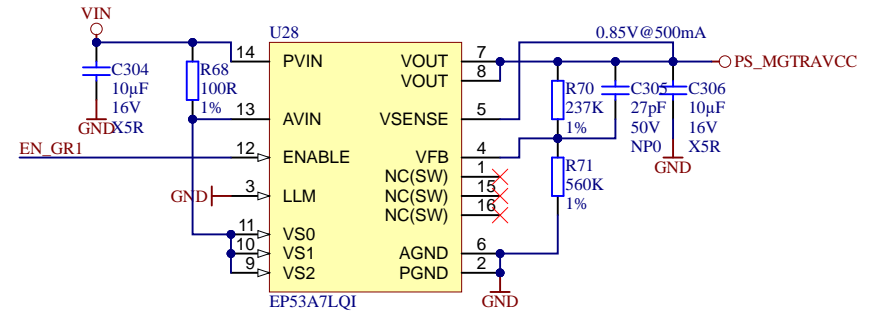
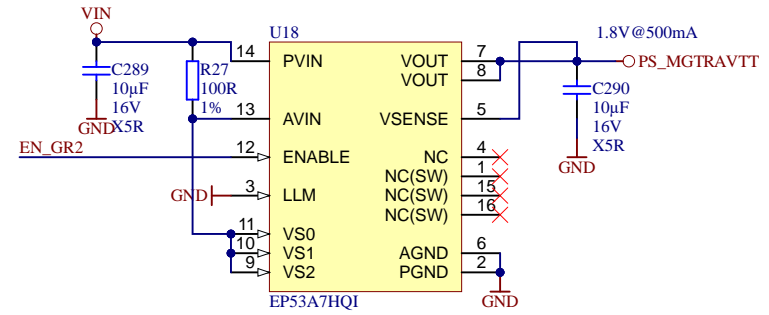
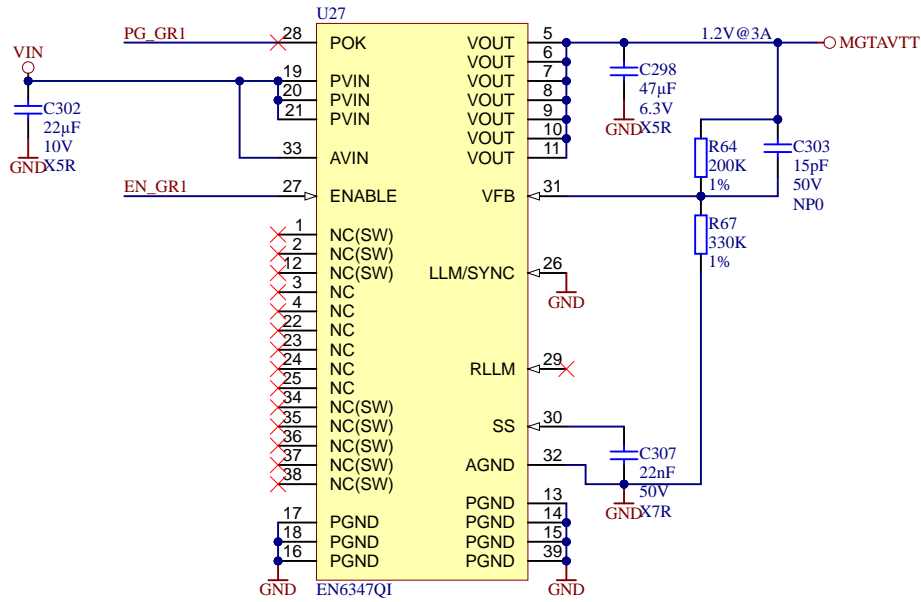
Title: PWR_CORE		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 28 of 34
Filename: PWR_CORE.SchDoc		




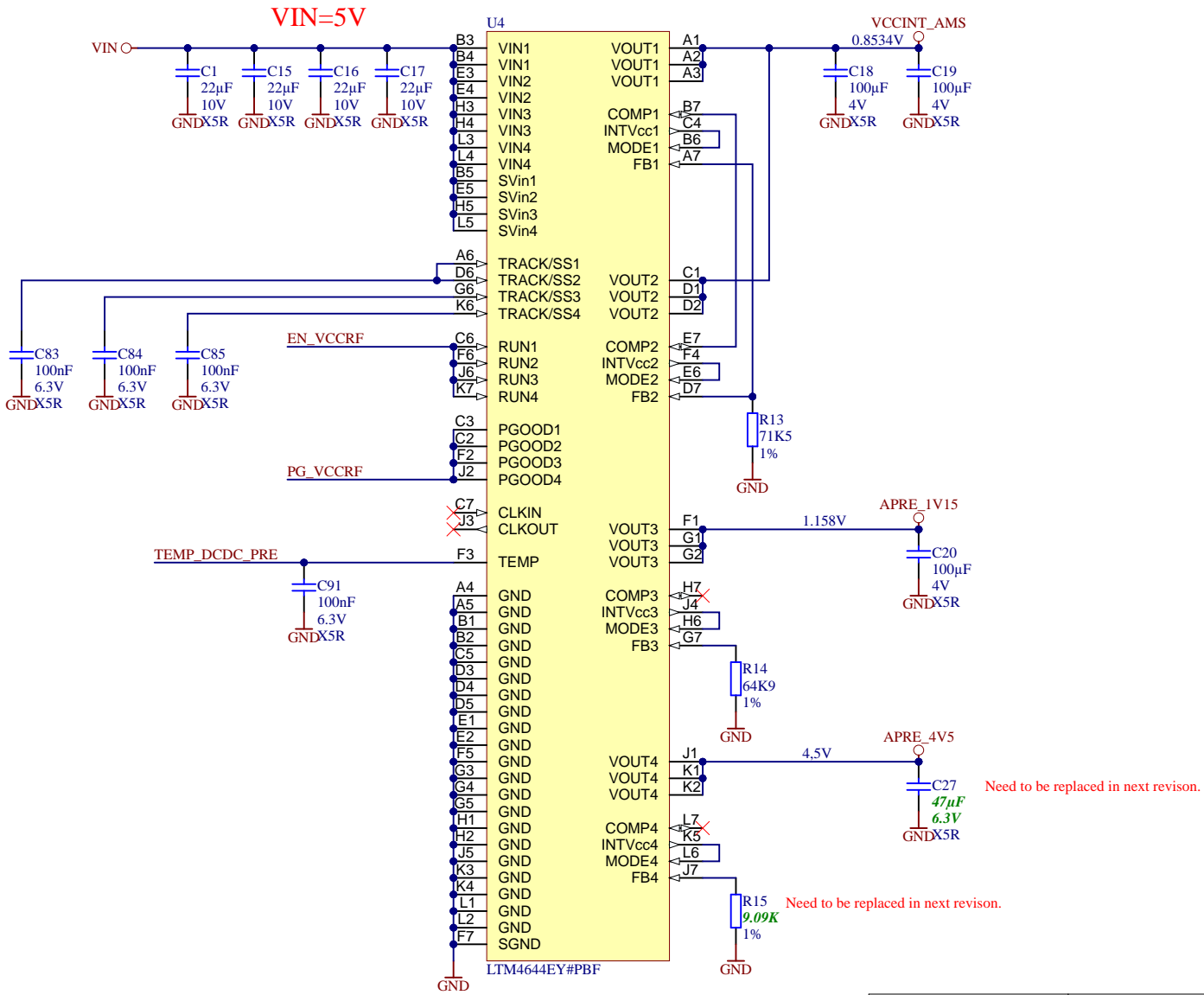
		Title: PWR_DAC	
		A4	Number: TE0835 TYE21-A
Date: 2020-06-10		Copyright: Trenz Electronic GmbH	
Filename: PWR_DAC.SchDoc		Page 29 of 34	




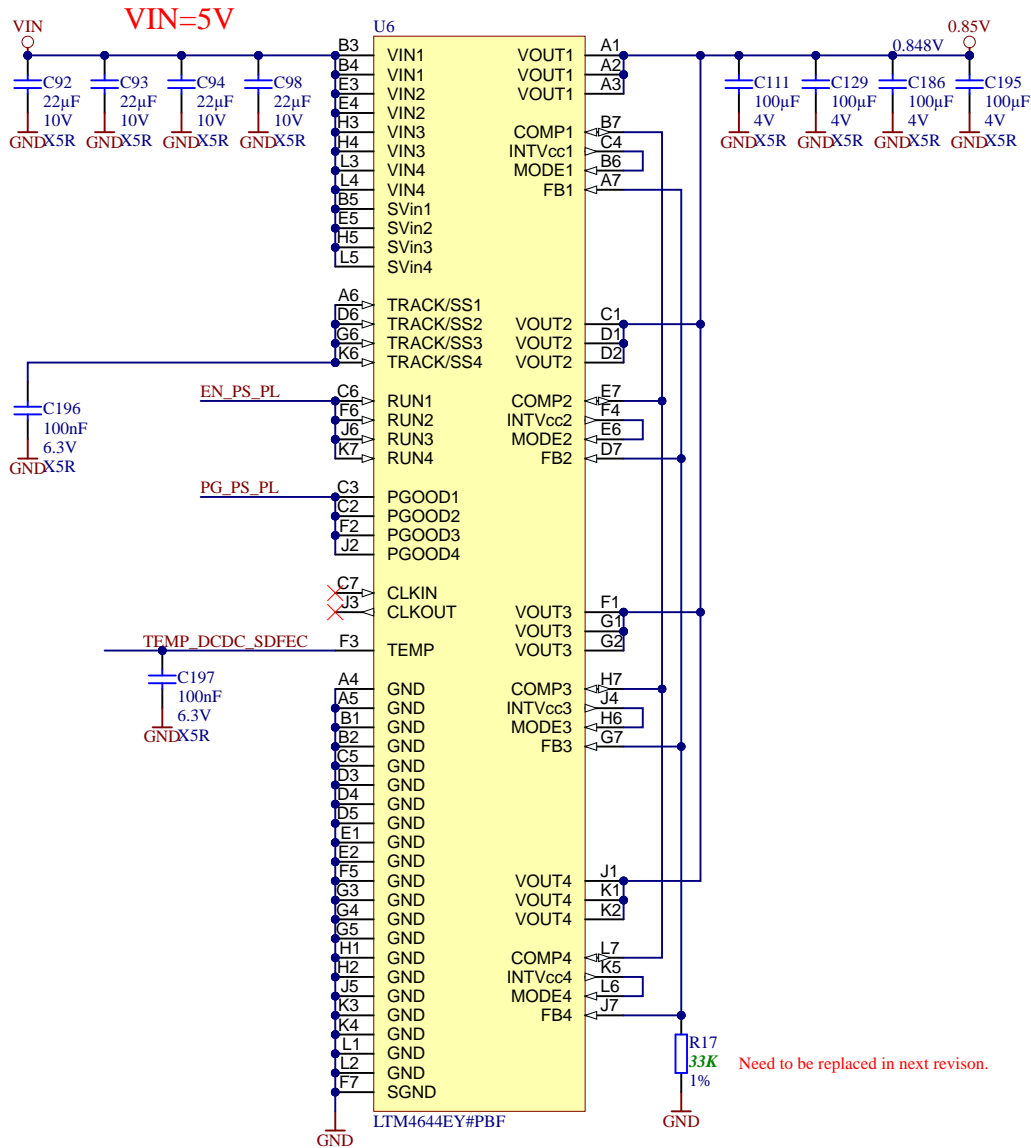
		Title: PWR_DDR	
		A4	Number: TE0835 TYE21-A
Date: 2020-06-10		Copyright: Trenz Electronic GmbH	
Date: 2020-06-10		Page 30 of 34	
Filename: PWR_DDR.SchDoc			



	Title: PWR_GT		
	A4	Number: TE0835 TYE21-A	Rev. 02
	Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 31 of 34
	Filename: PWR_GT.SchDoc		

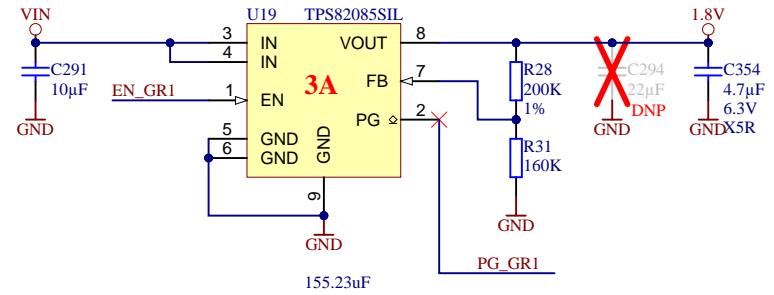


			Title: PWR_PRE	
			A4	Number: TE0835 TYE21-A
Date: 2020-06-10		Copyright: Trenz Electronic GmbH		Page 32 of 34
Filename: PWR_PRE.SchDoc				

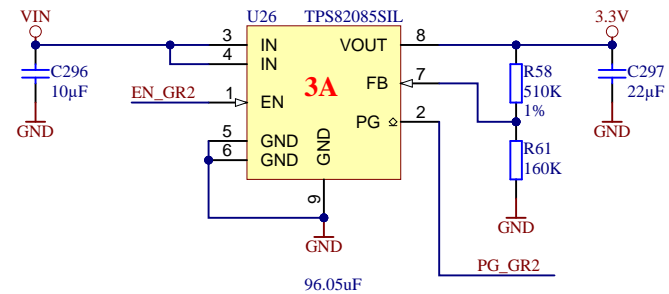


Need to be replaced in next revision.

Max C load < 150uF




Max C load < 150uF



Title: PWR_PS		
A4	Number: TE0835 TYE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 33 of 34
Filename: PWR_PS.SchDoc		

REVISION HISTORY

REV	Description	
-01	Initial revision	IG
-02	<ol style="list-style-type: none"> 1. Added a VRP resistor on bank 65; 2. LDO U33 is changed on ADP7102ACPZ; 3. Signal FPGA IO0 is connected on AE18 pin of FPGA; 4. Signal DBG_LED3 is connected on AD18 pin of FPGA; 5. Signal MIO13_25 connected to J1 pin 33 instead MIO25. 6. Resistor R84 is removed; 7. LED D1 moved on edge of PCB; 8. Added THT testpoints J4 on CPLD_JTAGEN, R76 was removed; 9. Signals B49_XX_X are renamed in B88_XX_X; 10. C241 is changed on 1nF; 11. Length of CLK signals on RFADC and RFDAC are adjusted; 12. Wrong connection on U8 is fixed (PCB); 13. Wrong connection PGOOD1 pin of U7 is fixed; 14. R17 is changed from 35,5K to 33K for VCC_PL_PS correction. 	IG
	<ol style="list-style-type: none"> 15. APRE_3V3 ranamed to APRE_4V5, voltage of the power rail incrsed from 3.3V to 4,58V. 16. Resistor R15 is changed from 13,3K to 9,09K. AN: 24671->25969 17. Capasitor C27 is changed from 100uF x 4V to 47uF x 6,3V. AN: 28940->24718 	IG

	Title: Revision_Changes		
	A4	Number: TE0835 TYE21-A	Rev. 02
	Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 34 of 34
	Filename: Revision_Changes.SchDoc		