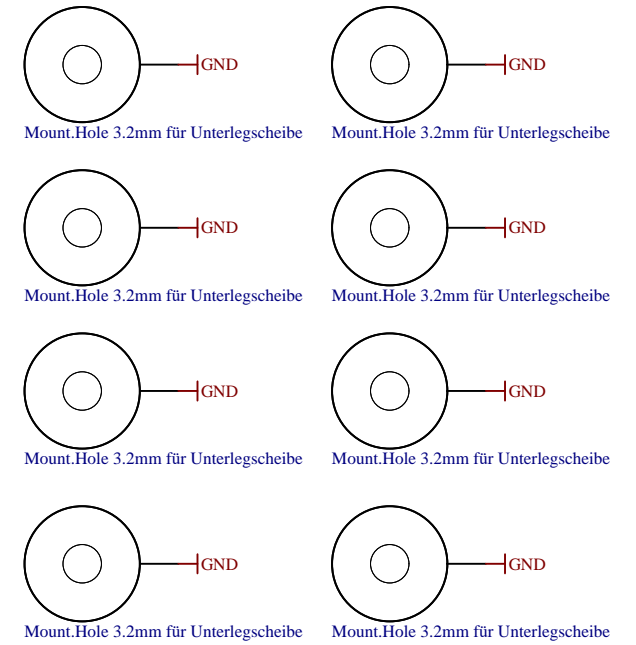


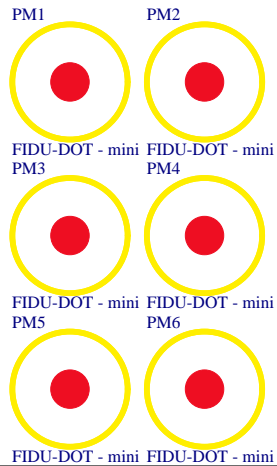
- | | |
|-----------------------------------|---------------------------------------|
| U_Clock
Clock.SchDoc | U_ZU
ZU.SchDoc |
| U_DDR4-RAM
DDR4-RAM.SchDoc | U_USB-PHY
USB-PHY.SchDoc |
| U_DDR4-RAM_2
DDR4-RAM_2.SchDoc | U_Ethernet
Ethernet.SchDoc |
| U_DDR4-RAM_3
DDR4-RAM_3.SchDoc | U_B2B
B2B.SchDoc |
| U_DDR4-RAM_4
DDR4-RAM_4.SchDoc | U_B2B_2
B2B_2.SchDoc |
| U_DDR4-TERM
DDR4-TERM.SchDoc | PWR_Structure
PWR_Structure.SchDoc |
| CPLD
CPLD.SchDoc | |

Special notes:



LOGO1
TE Logo PRINT Layer
LOGO PRINT

Serial
Serial
Serialnumber 6,3 x 6.3mm



Design drawn by: IG
Checked by: MR
Assembly variant: UXE21-A
Created by:
Modified by:
Modified at:



Title: TE0835		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 1 of 34
Filename: TE0835.SchDoc		

1

2

3

4

A

A

HD
ZU_HD.SchDoc



MGT_L
ZU_MGT_L.SchDoc



ZU_B65_B66
ZU_B65_B66.SchDoc



MIO
ZU_MIO.SchDoc



PSDDR
ZU_PSDDR.SchDoc



ZU_PWR
ZU_PWR.SchDoc



ZU_PWR2
ZU_PWR2.SchDoc



ZU_PWR3
ZU_PWR3.SchDoc



ZU_ADC
ZU_ADC.SchDoc



ZU_DAC
ZU_DAC.SchDoc



ZU_CFG
ZU_CFG.SchDoc



ZU_PSMGT
ZU_PSMGT.SchDoc



B


B

C

C

D

D

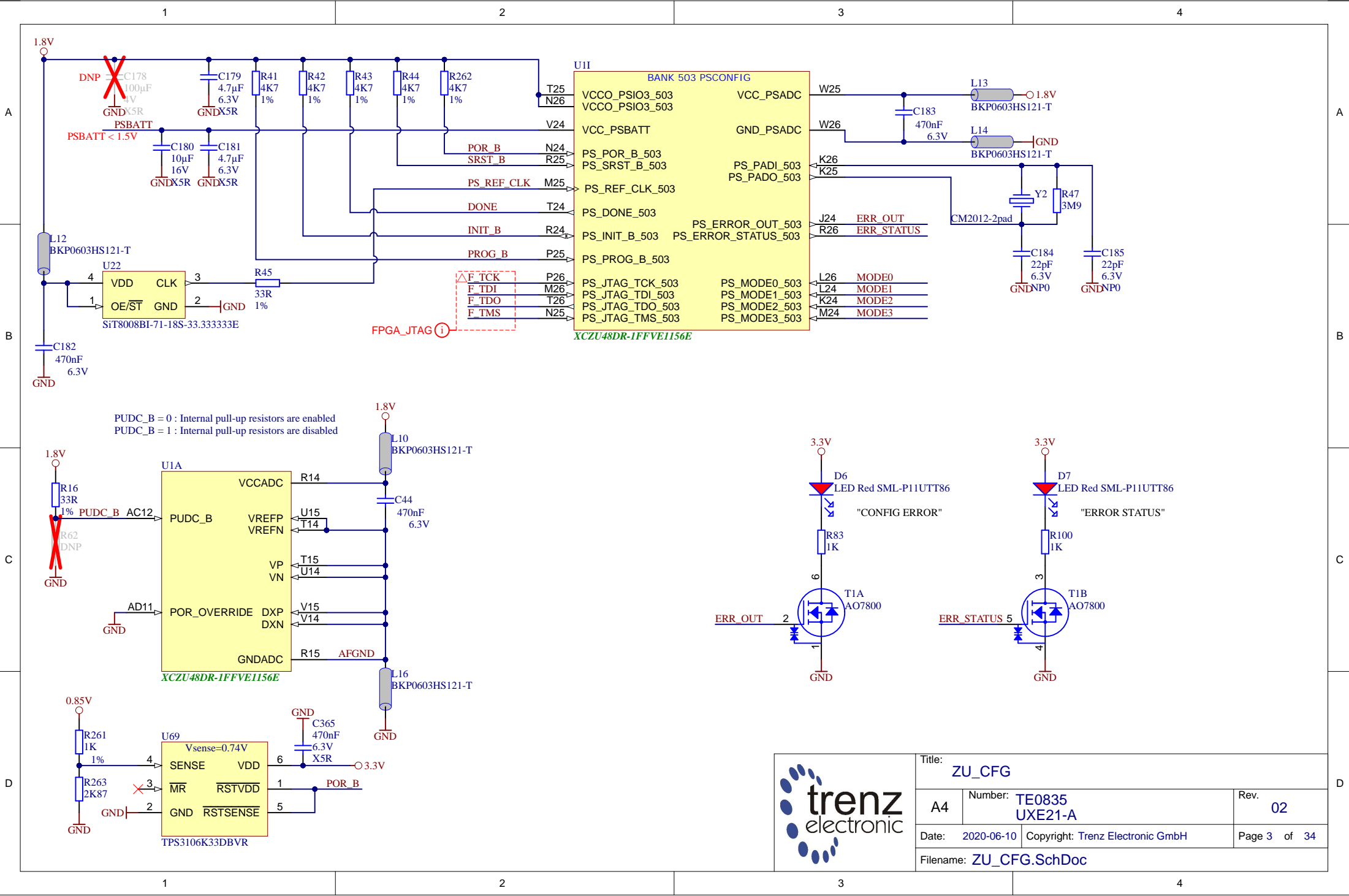
		Title: ZU	
		A4	Number: TE0835 UXE21-A
Date: 2020-06-10		Copyright: Trenz Electronic GmbH	
Filename: ZU.SchDoc		Page 2 of 34	

1

2

3

4



Title: ZU_CFG		
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Filename: ZU_CFG.SchDoc		

A

B

C

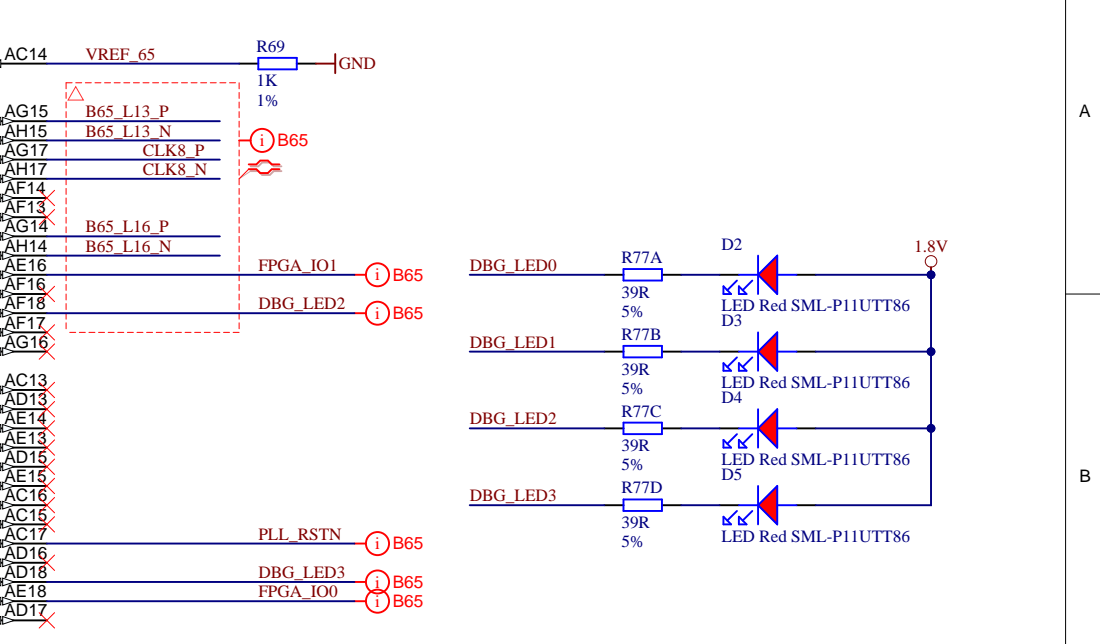
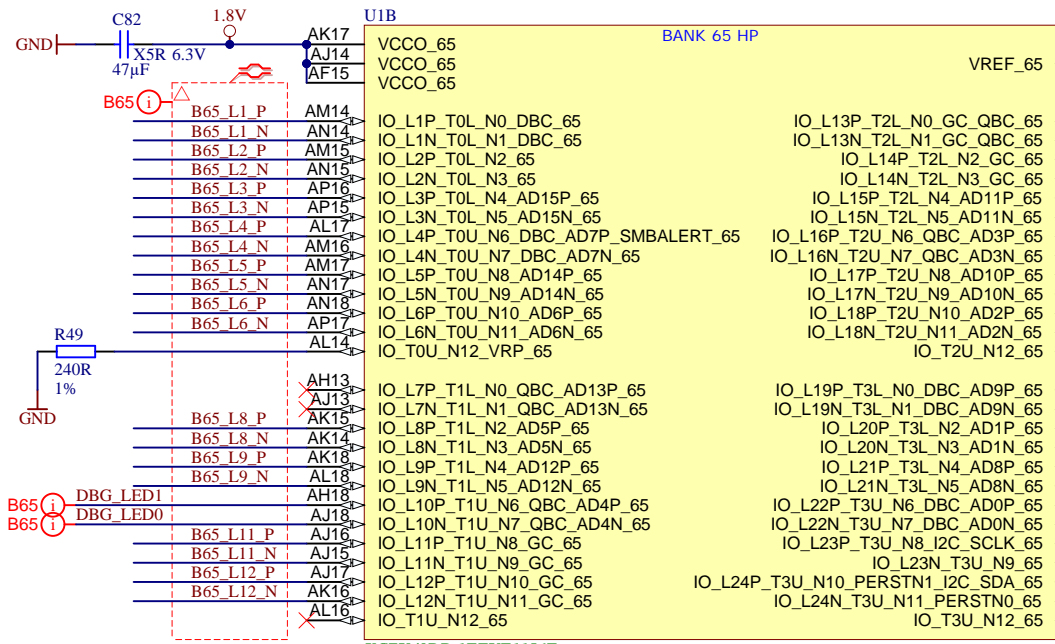
D

A

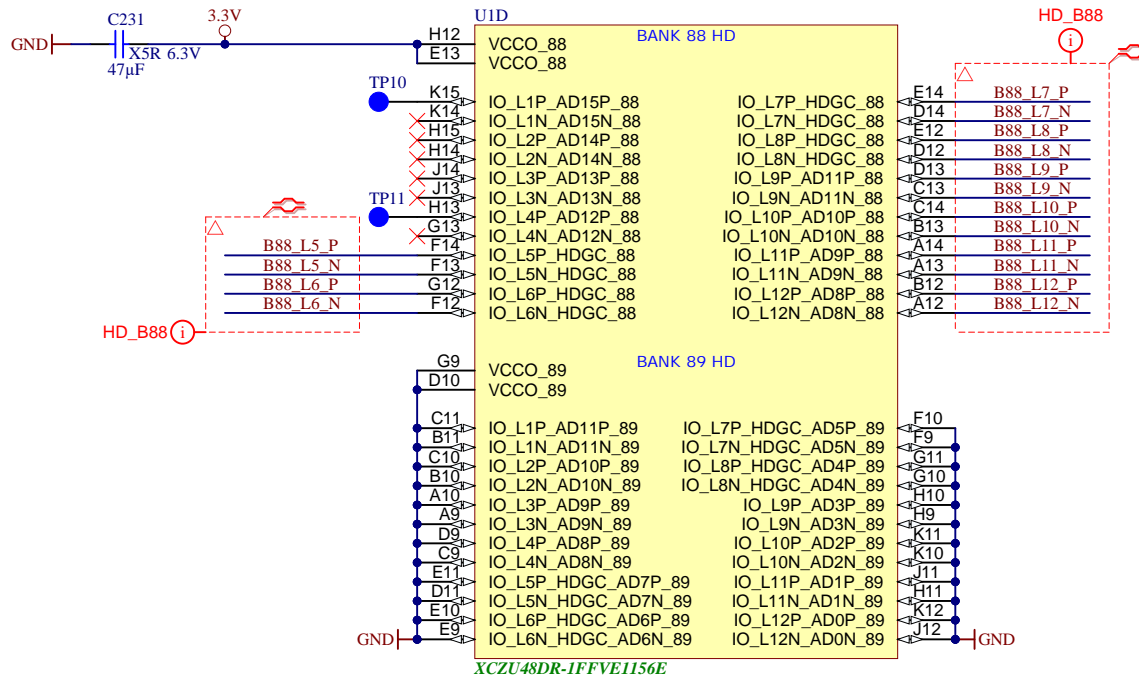
B

C

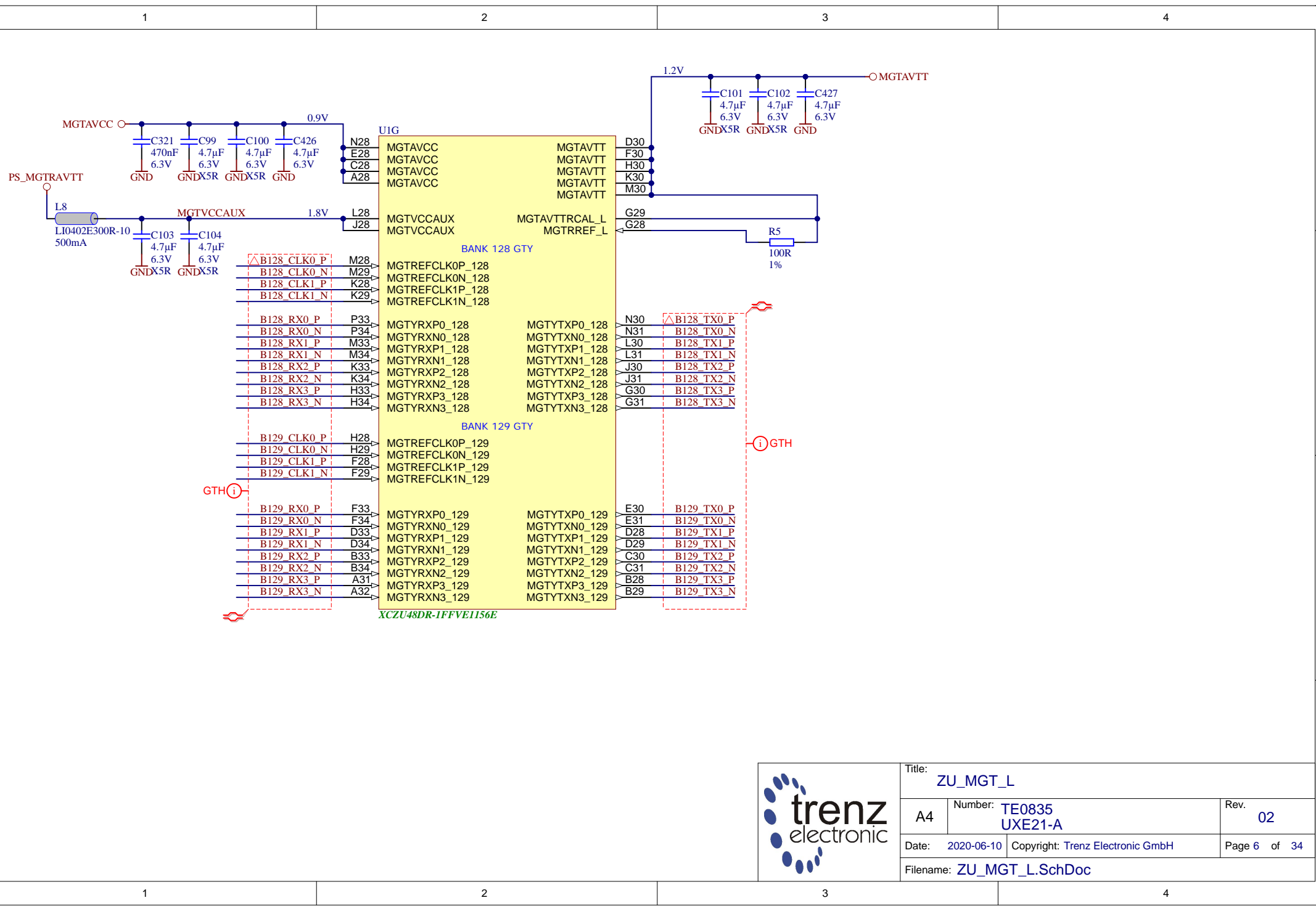
D



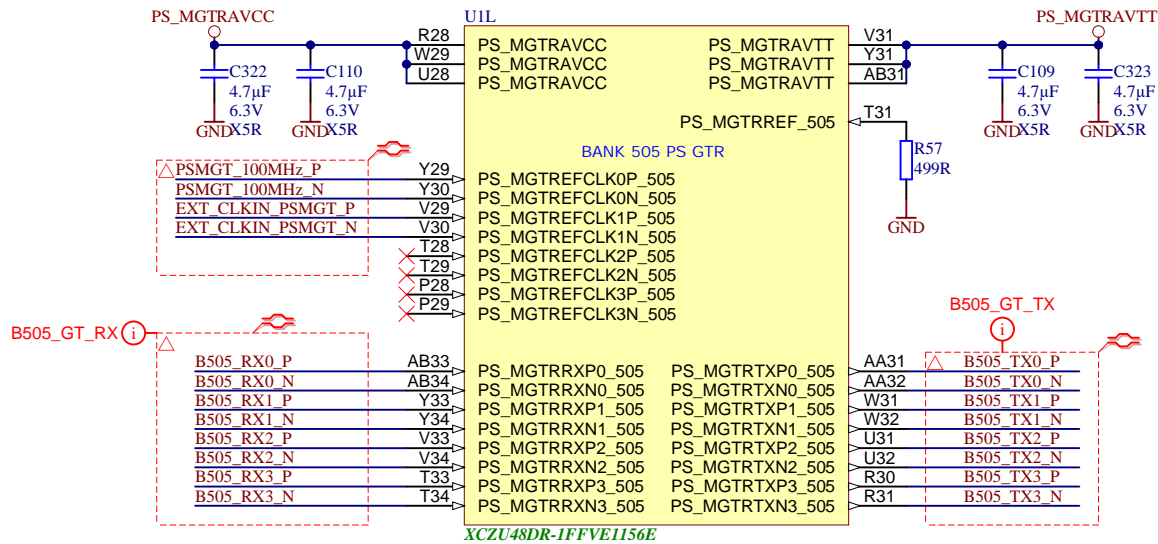
Title: ZU_B65_B66		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 4 of 34
Filename: ZU_B65_B66.SchDoc		



	Title: ZU_HD	
	A4	Number: TE0835 UXE21-A
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	Copyright: Trenz Electronic GmbH	
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Filename: ZU_HD.SchDoc		



Title: ZU_MGT_L		
A4	Number: TE0835 UXE21-A	Rev. 02
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Filename: ZU_MGT_L.SchDoc		



Title: ZU_PSMGT		
A4	Number: TE0835 UXE21-A	Rev. 02
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Filename: ZU_PSMGT.SchDoc		

A

B

C

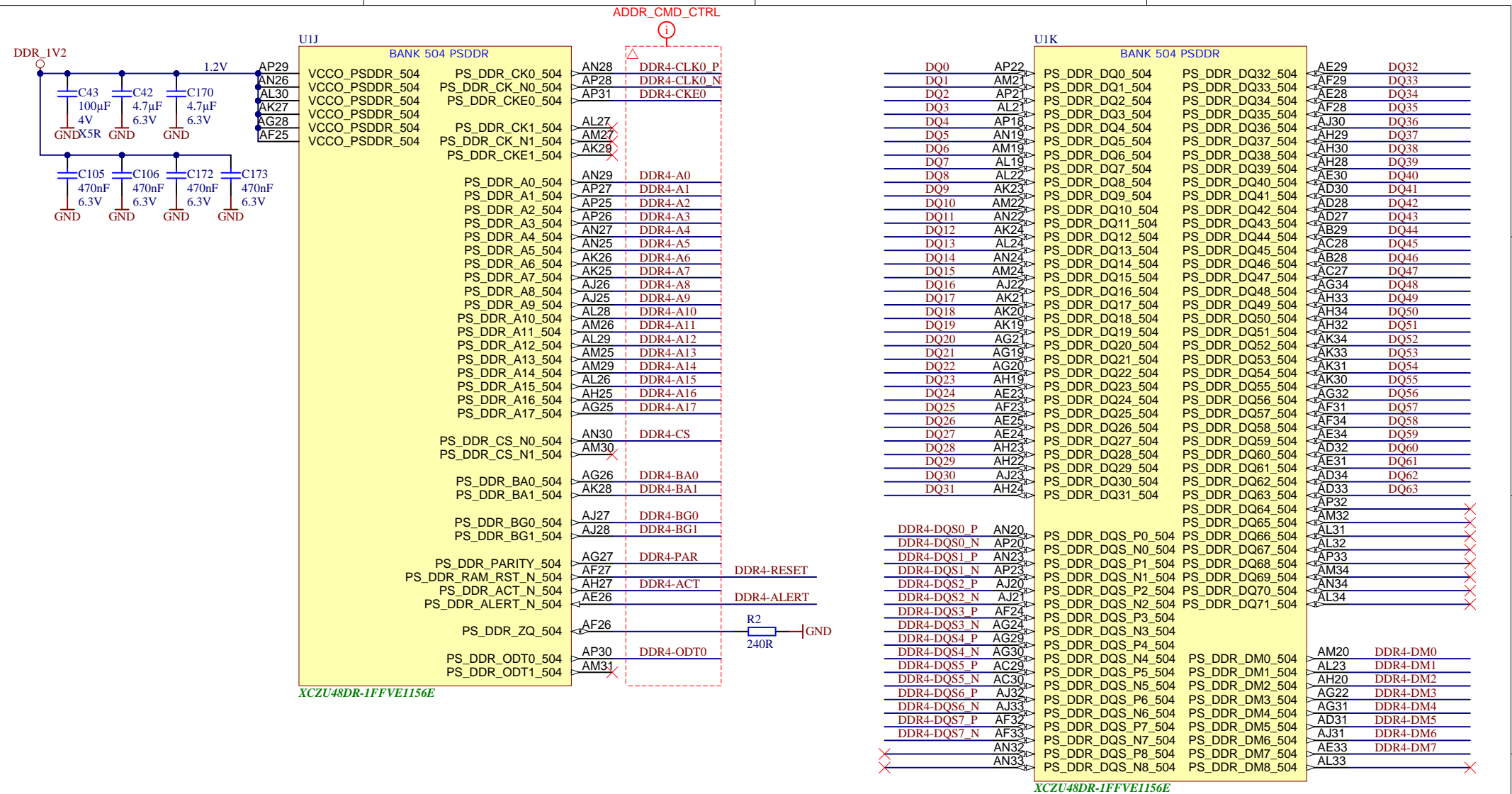
D

A

B

C

D

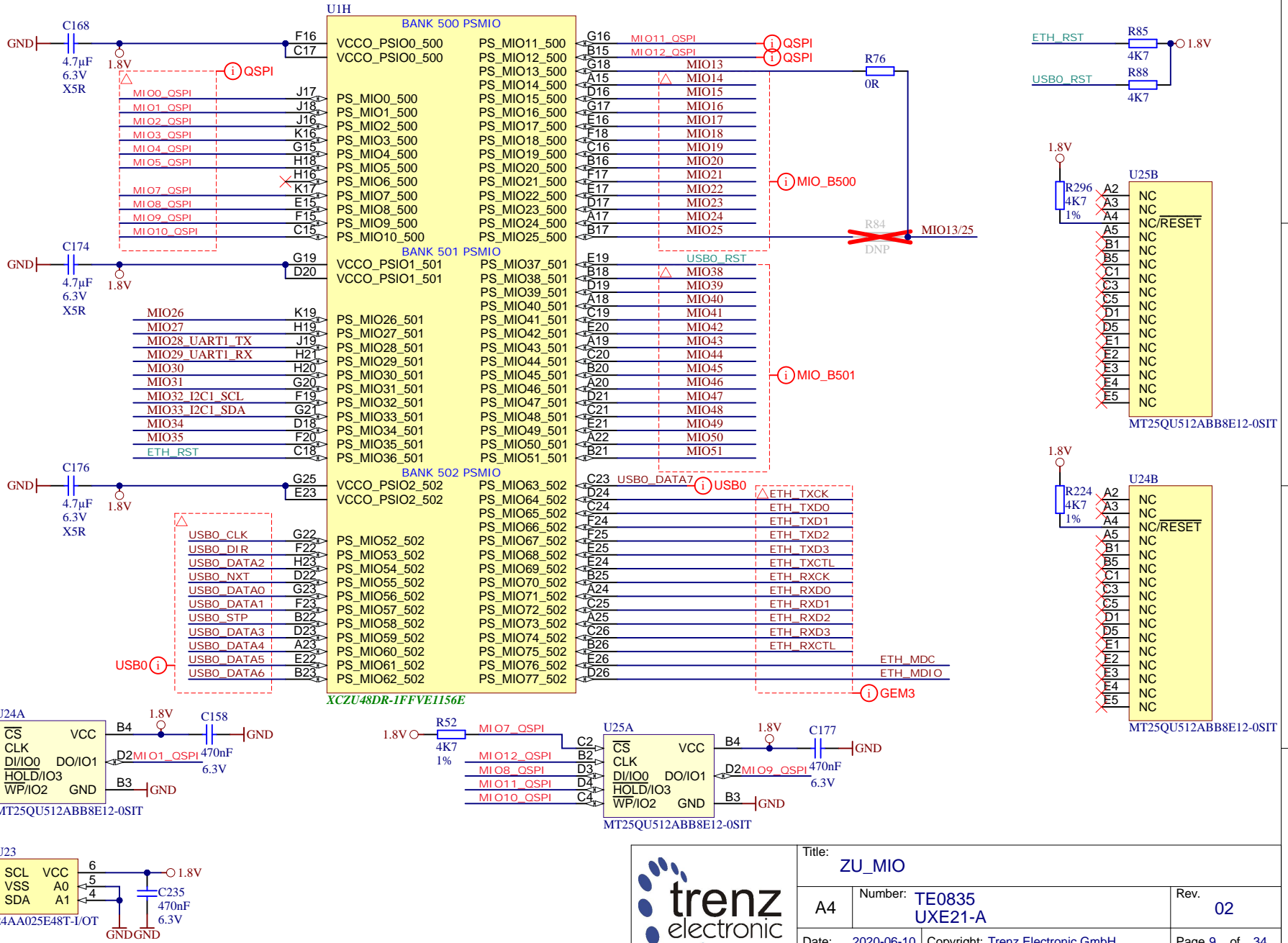
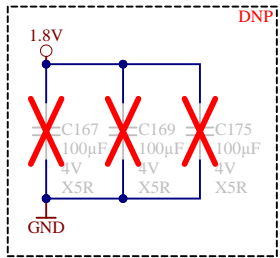


XCZU48DR-1FFVE1156E

XCZU48DR-1FFVE1156E



Title: ZU_PSDDR		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 8 of 34
Filename: ZU_PSDDR.SchDoc		



Title: ZU_MIO		
A4	Number: TE0835 UXE21-A	Rev. 02
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Filename: ZU_MIO.SchDoc		

A

B

C

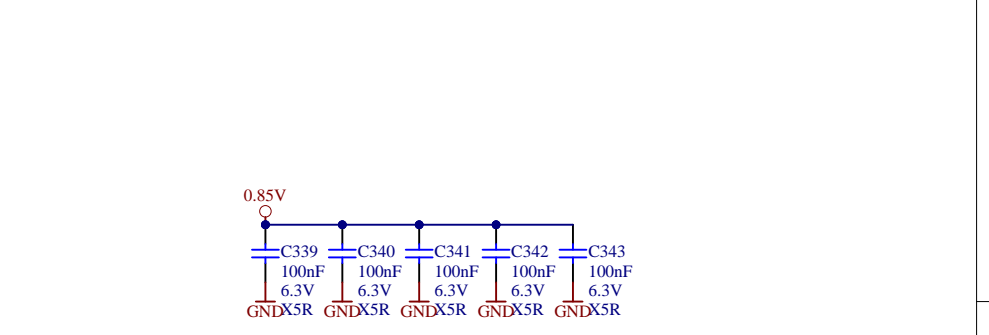
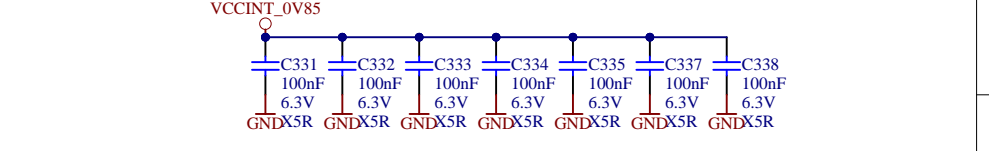
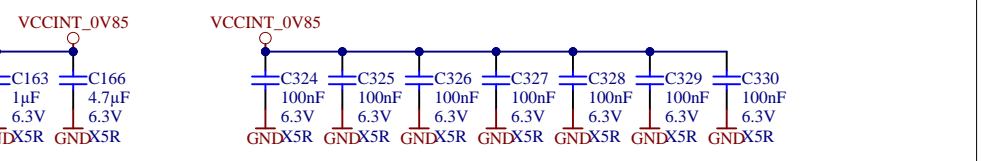
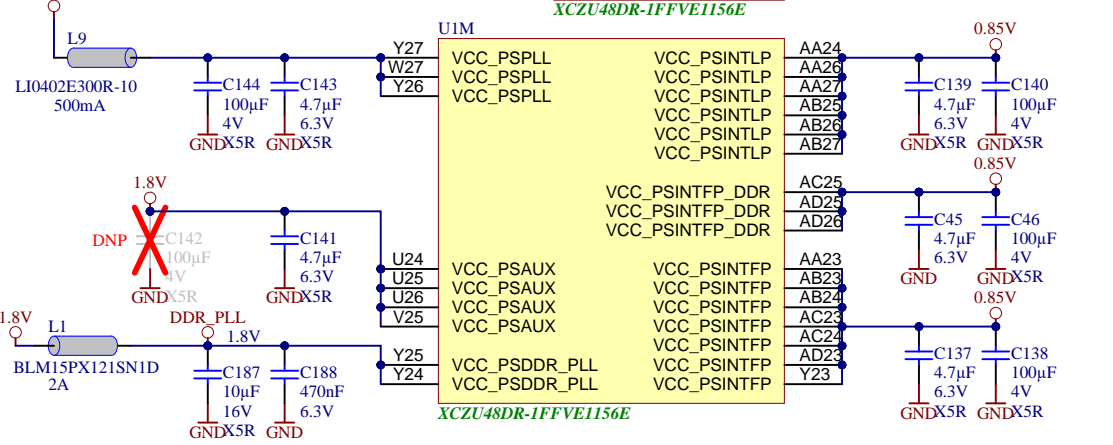
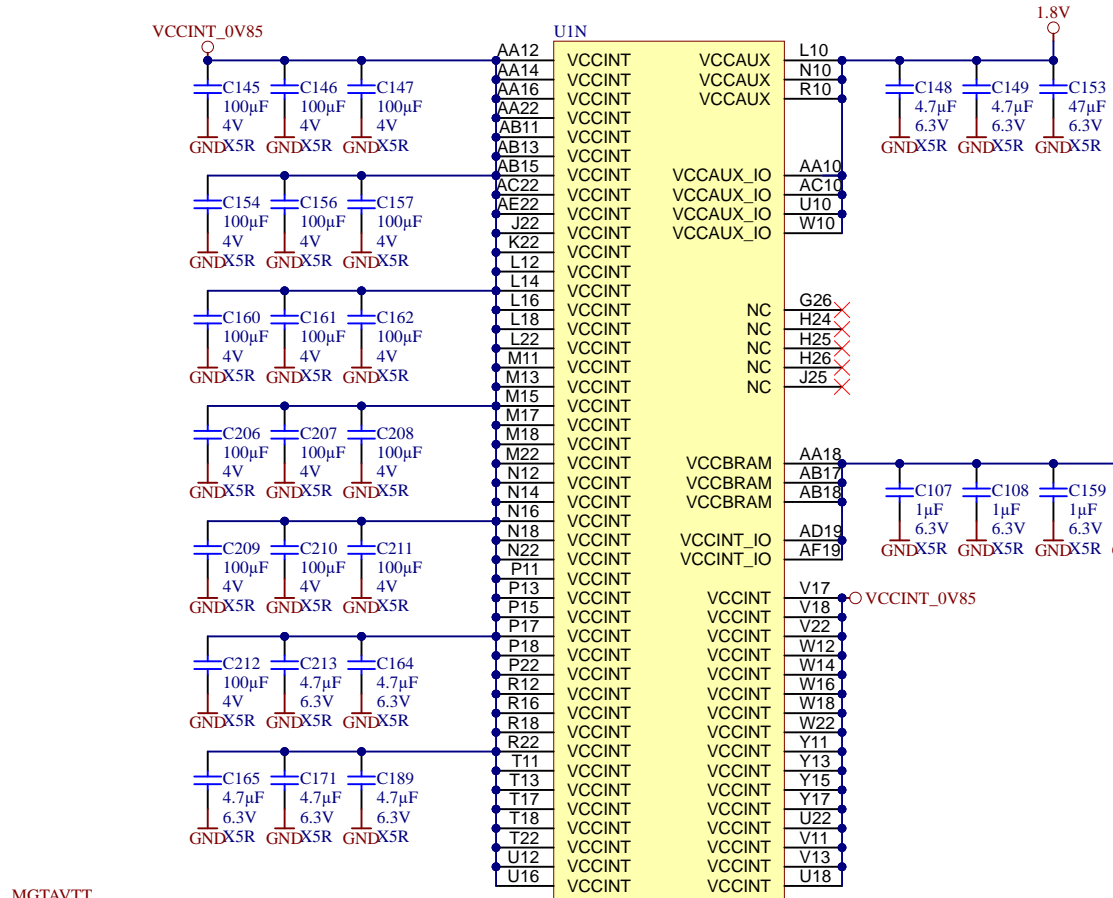
D

A

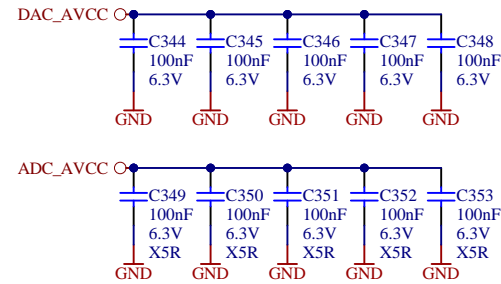
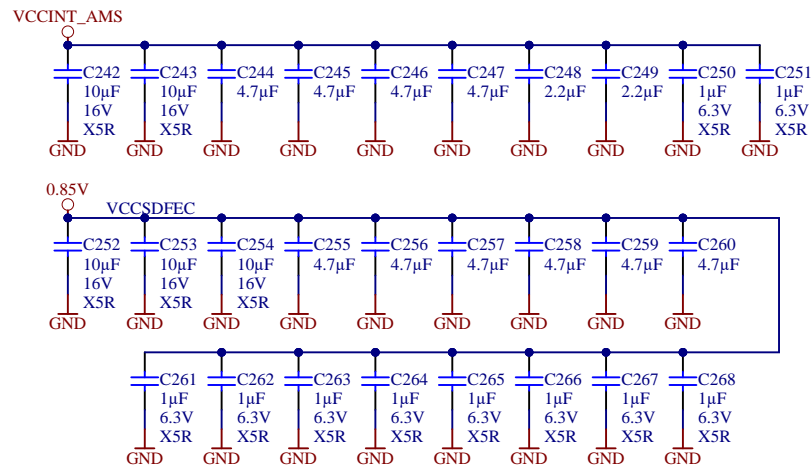
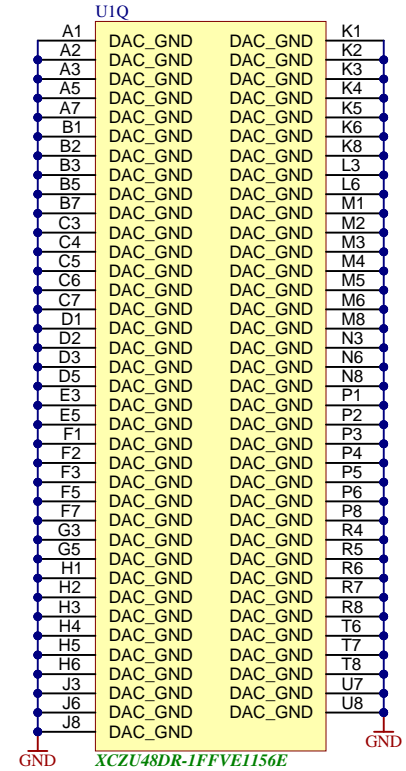
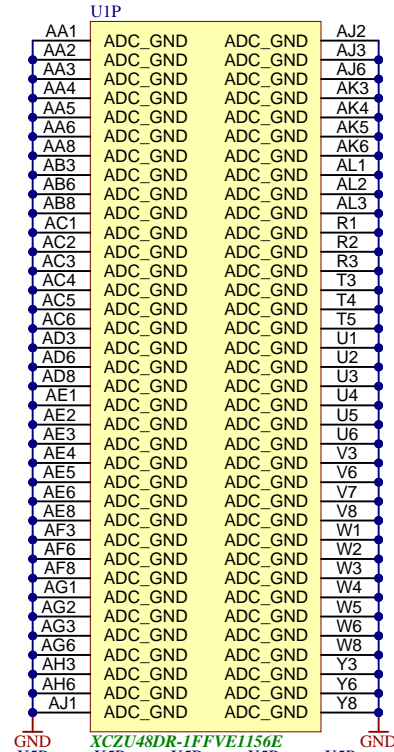
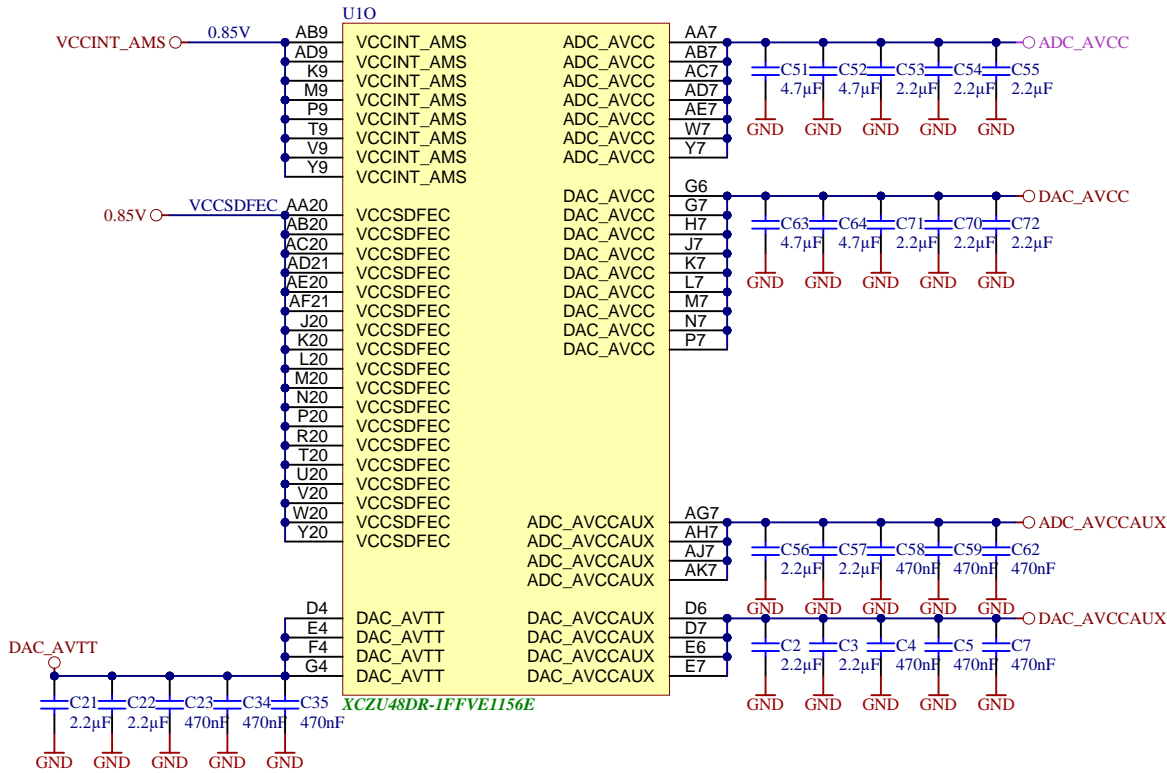
B

C

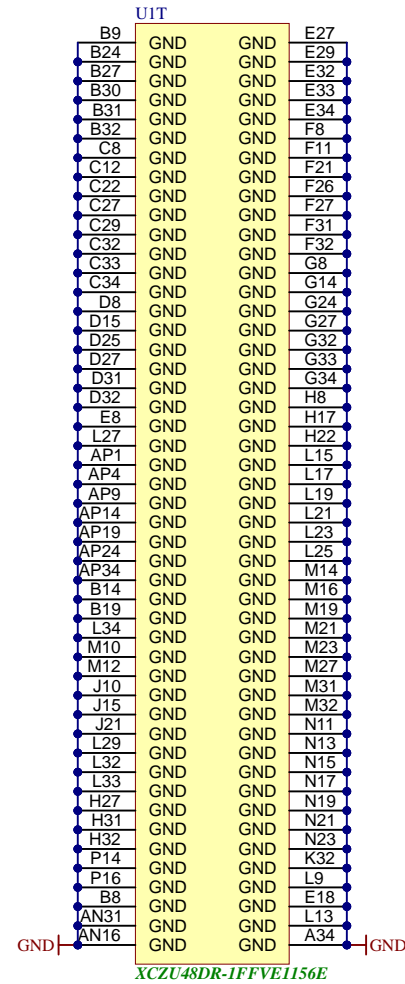
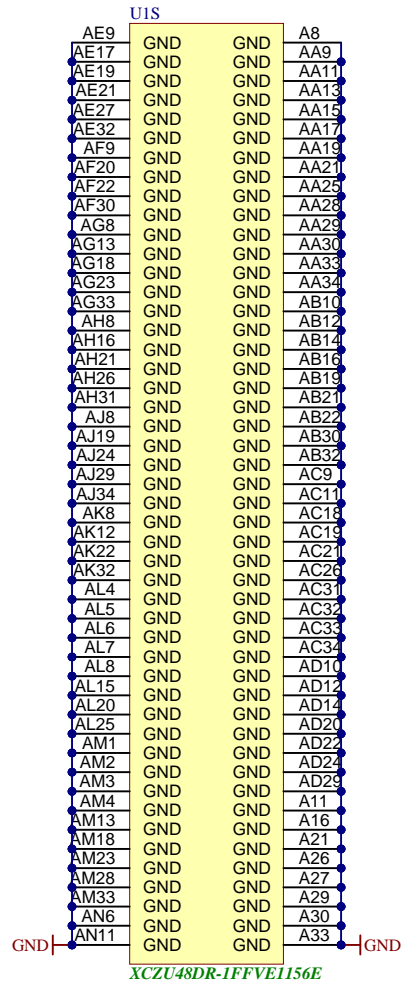
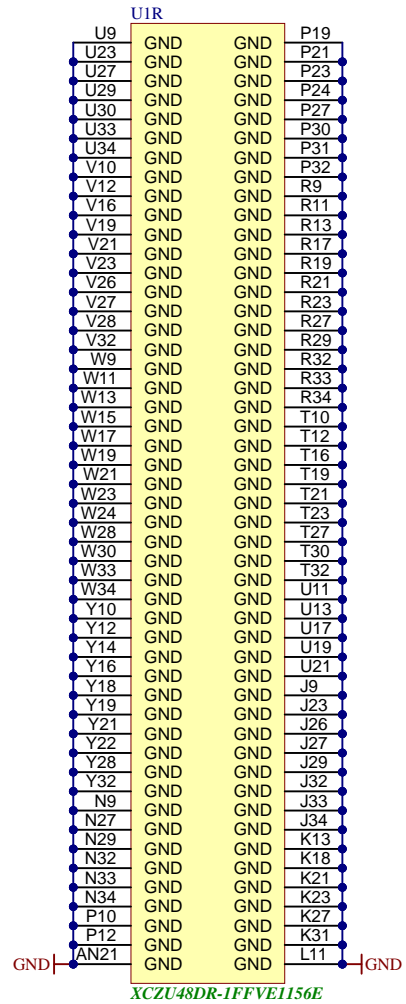
D



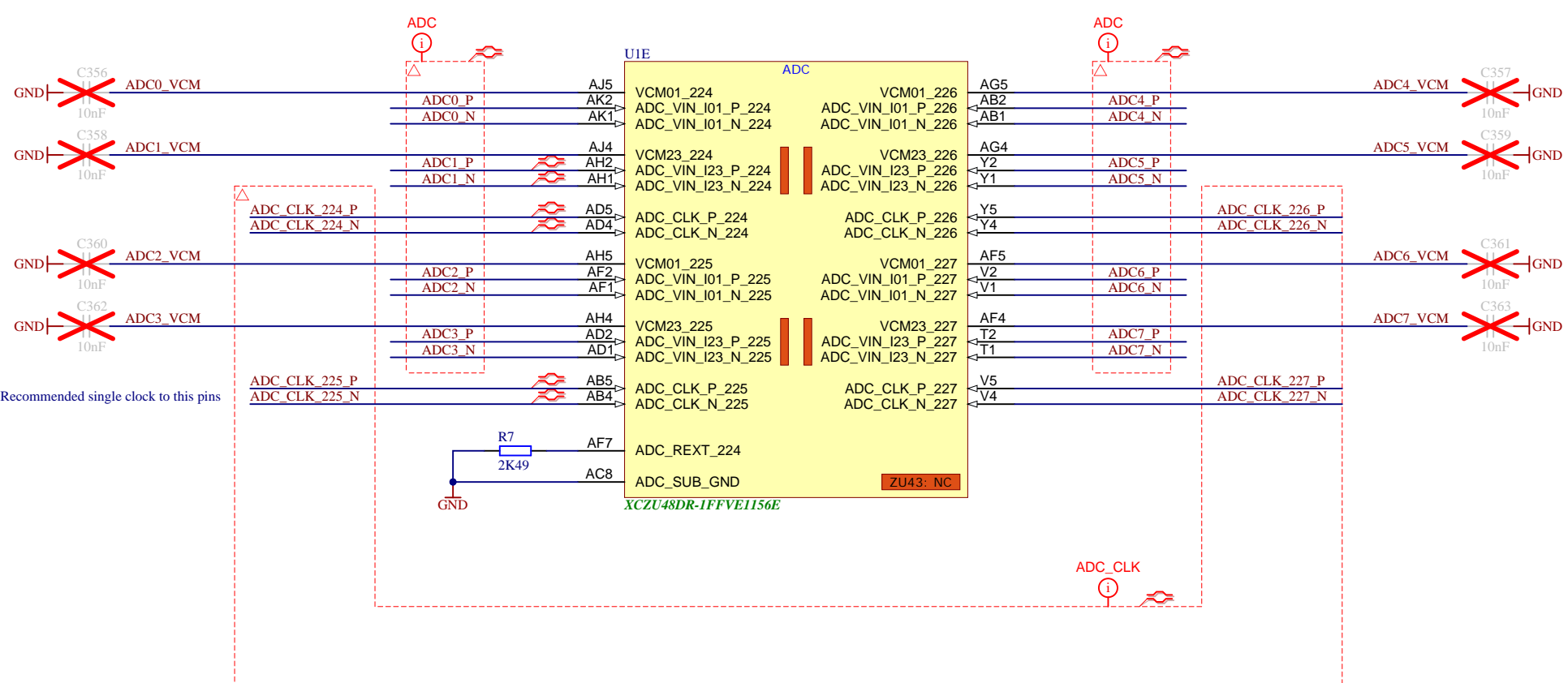
Title: ZU_PWR		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 10 of 34
Filename: ZU_PWR.SchDoc		




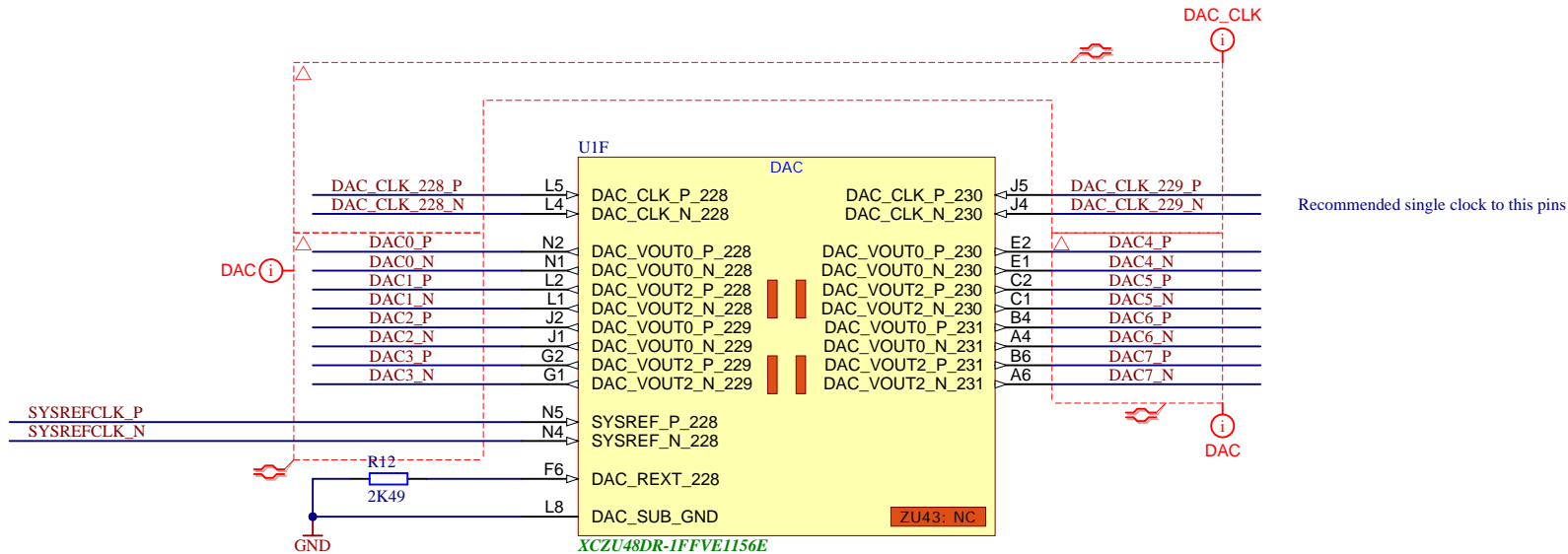
Title: ZU_PWR2		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 11 of 34
Filename: ZU_PWR2.SchDoc		



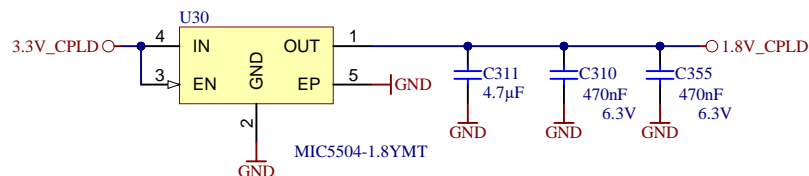
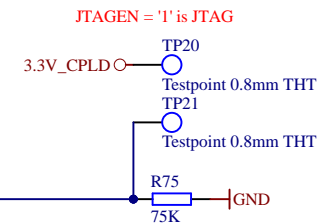
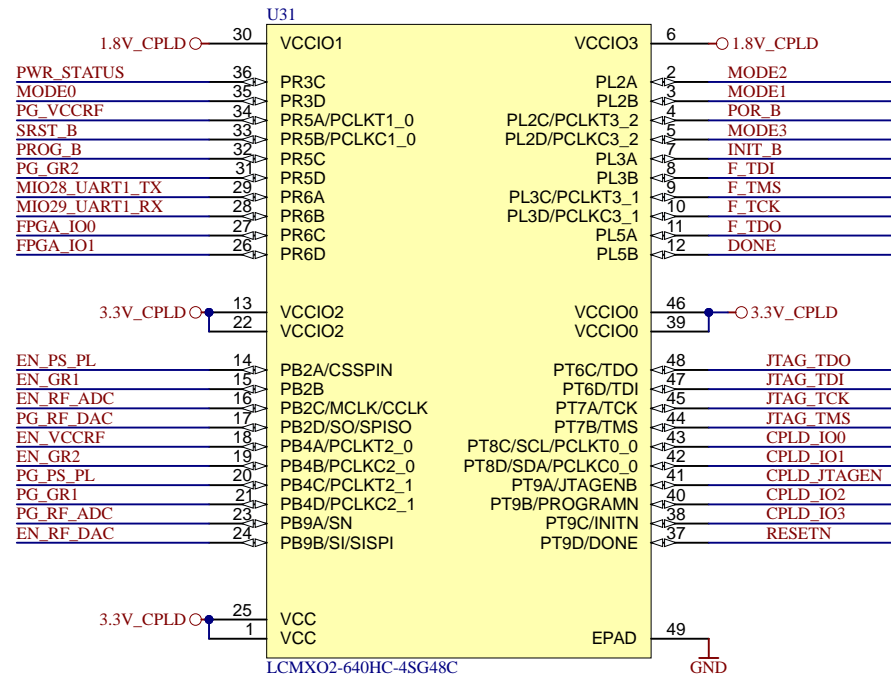
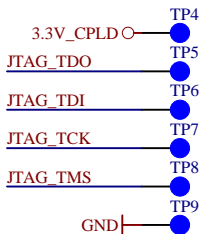
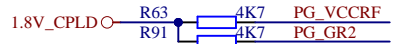
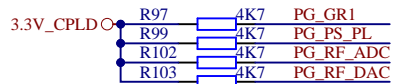
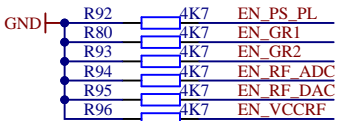
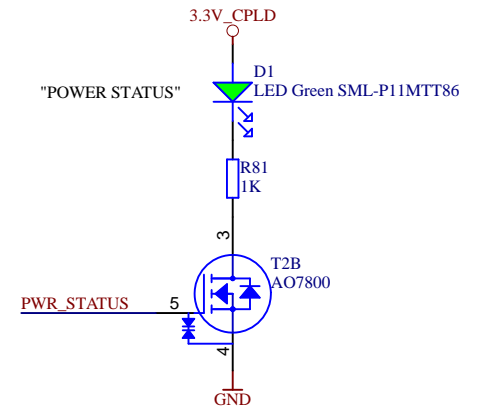
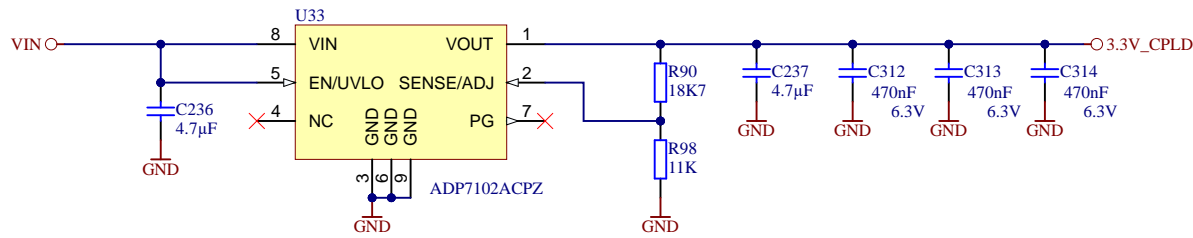
Title: ZU_PWR3		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 12 of 34
Filename: ZU_PWR3.SchDoc		



		Title: ZU_ADC	
		A4	Number: TE0835 UXE21-A
Date: 2020-06-10		Copyright: Trenz Electronic GmbH	
Filename: ZU_ADC.SchDoc		Page 13 of 34	

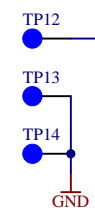


	Title: ZU_DAC		
	A4	Number: TE0835 UXE21-A	Rev. 02
	Date: 2020-06-10	Copyright: Trenz Electronic GmbH	
	Filename: ZU_DAC.SchDoc		Page 14 of 34

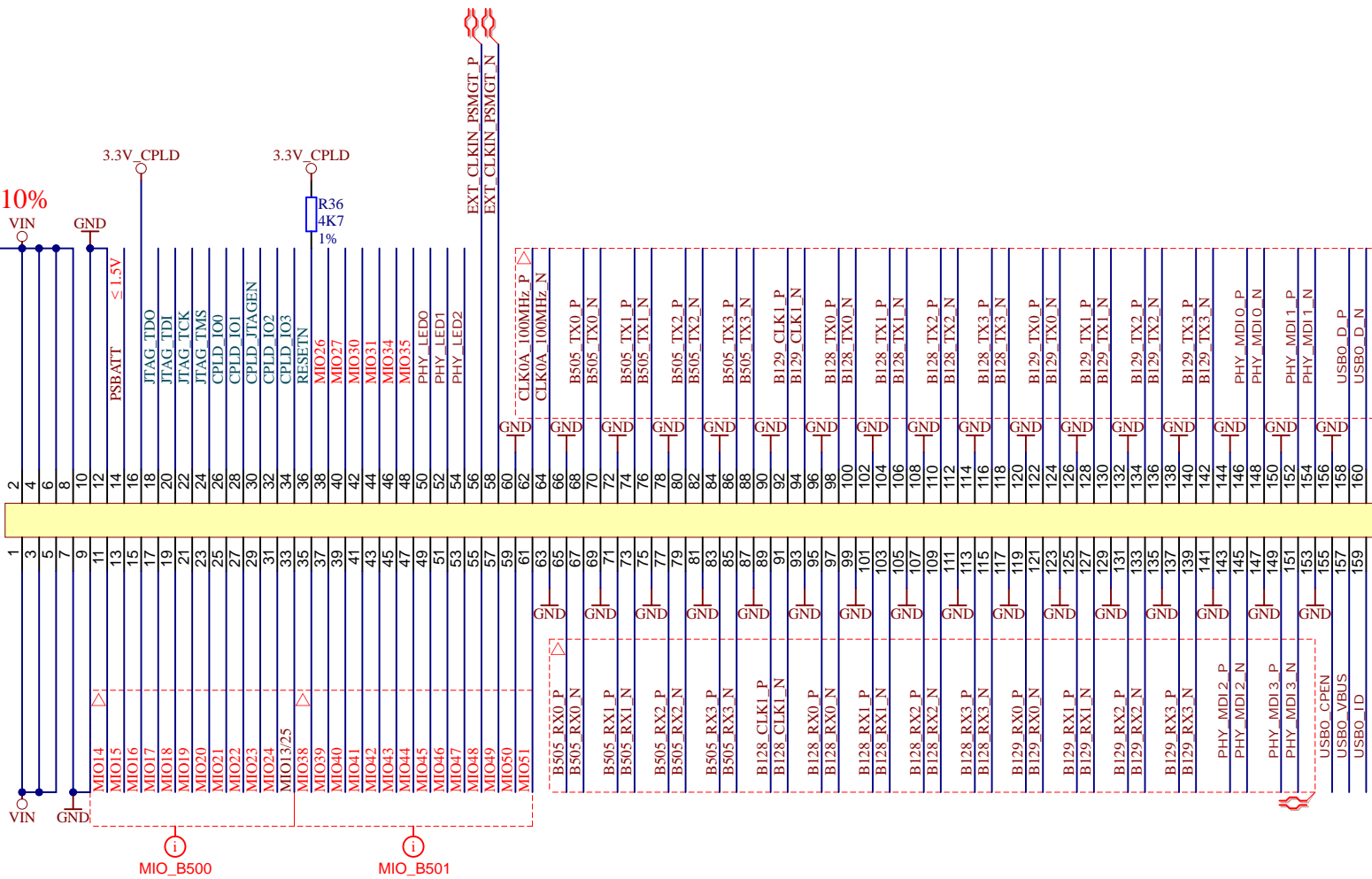


Title: CPLD		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 15 of 34
Filename: CPLD.SchDoc		

VIN=5V±10%



J1



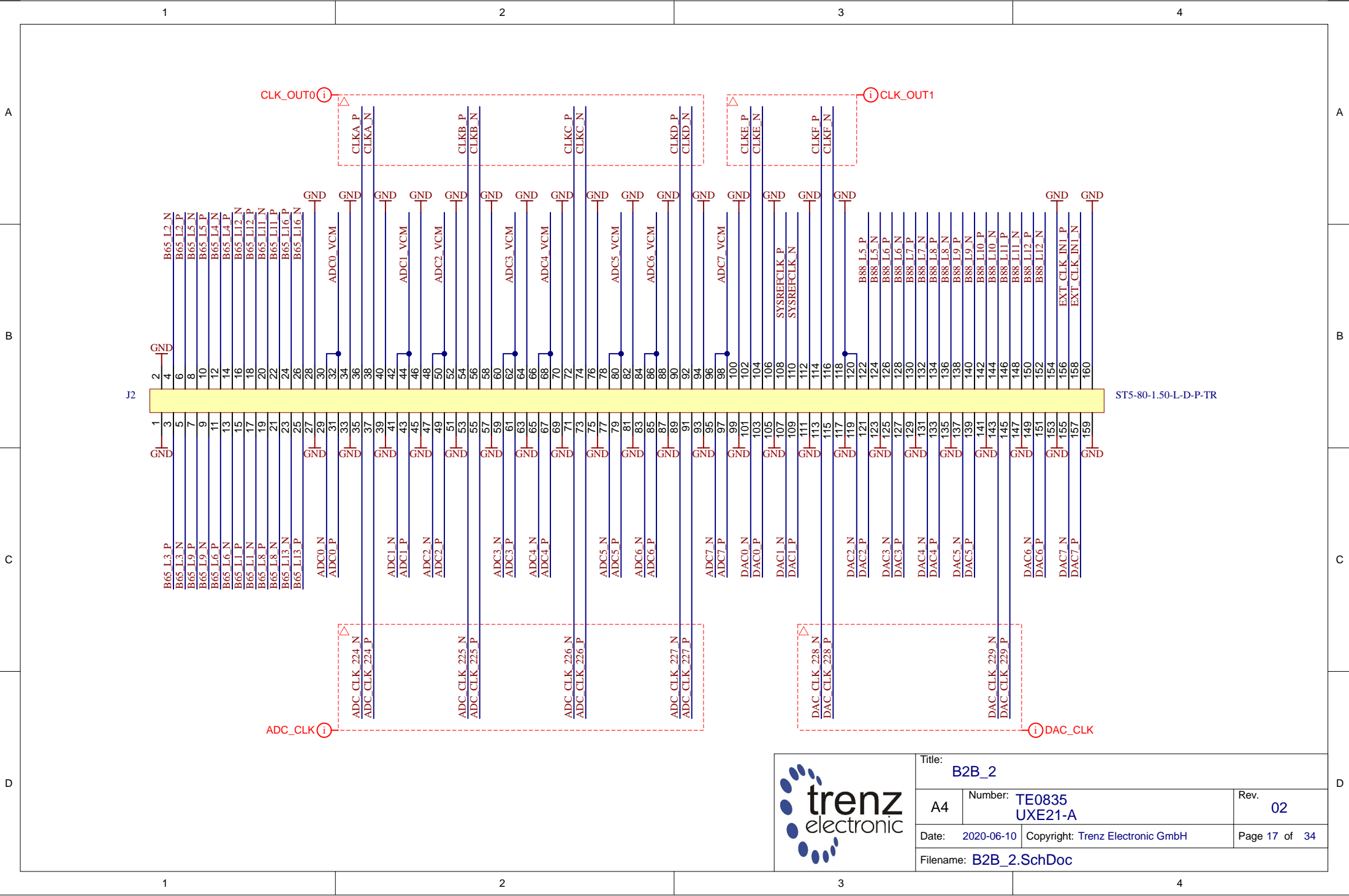
MIO_B500

MIO_B501


ST5-80-1.50-L-D-P-TR



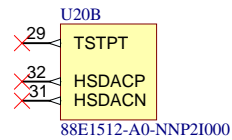
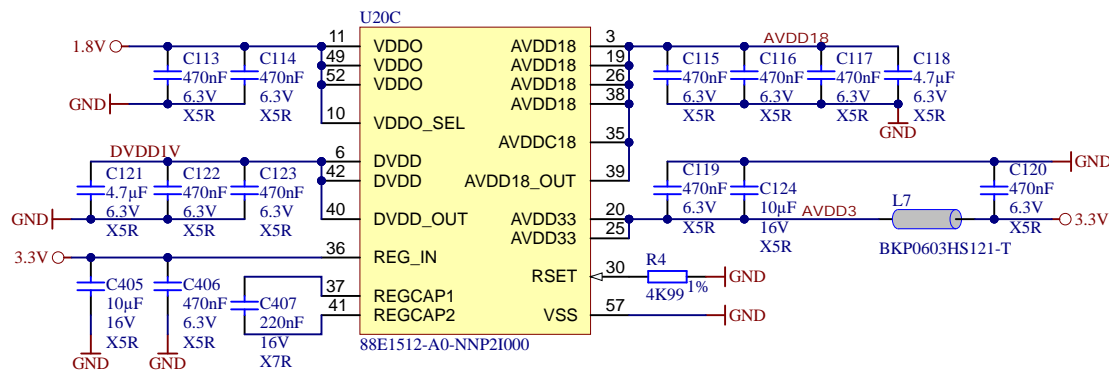
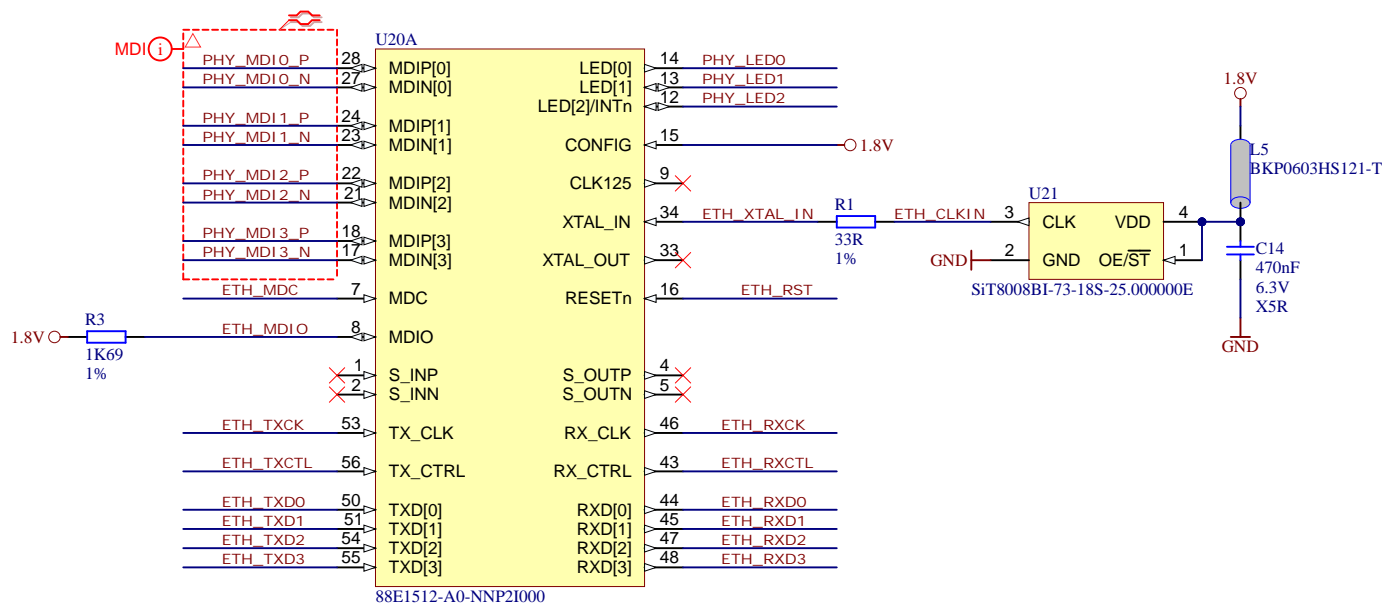
Title: B2B		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	
Filename: B2B.SchDoc		Page 16 of 34



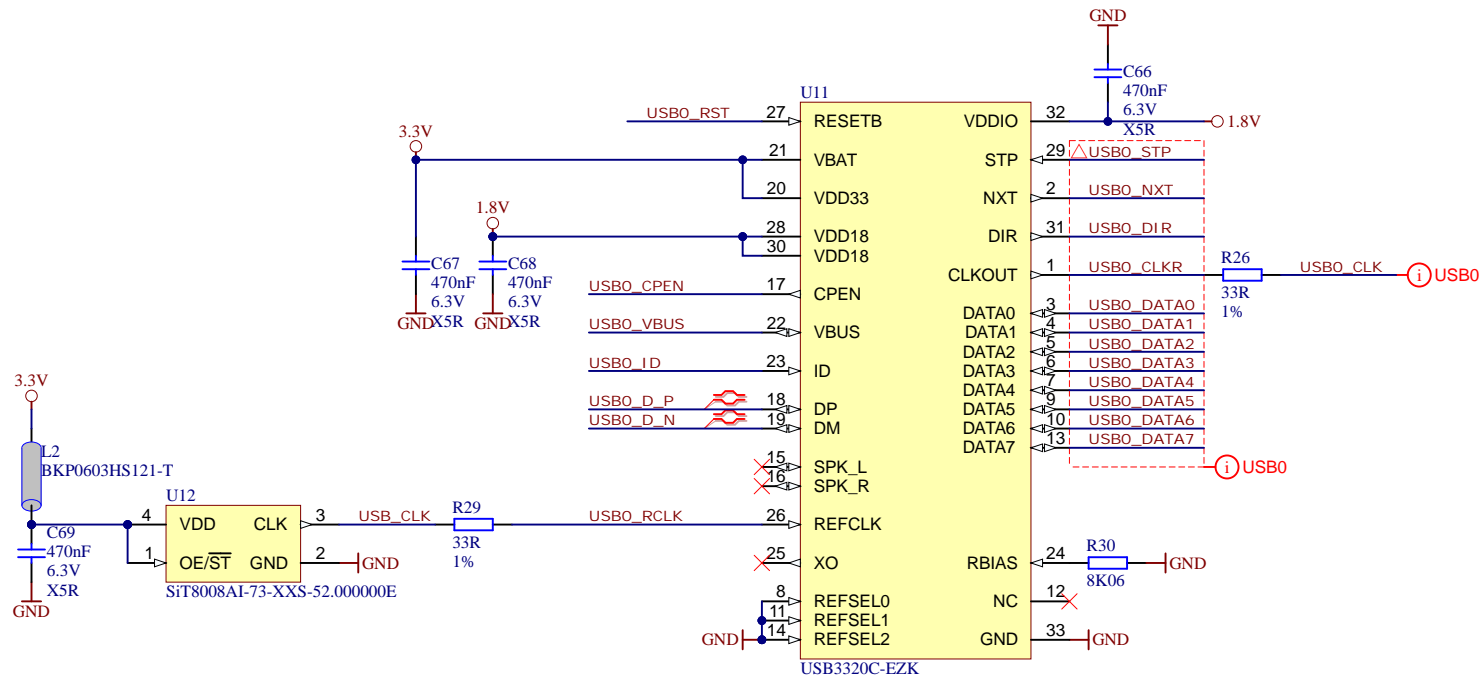
ST5-80-1.50-L-D-P-TR



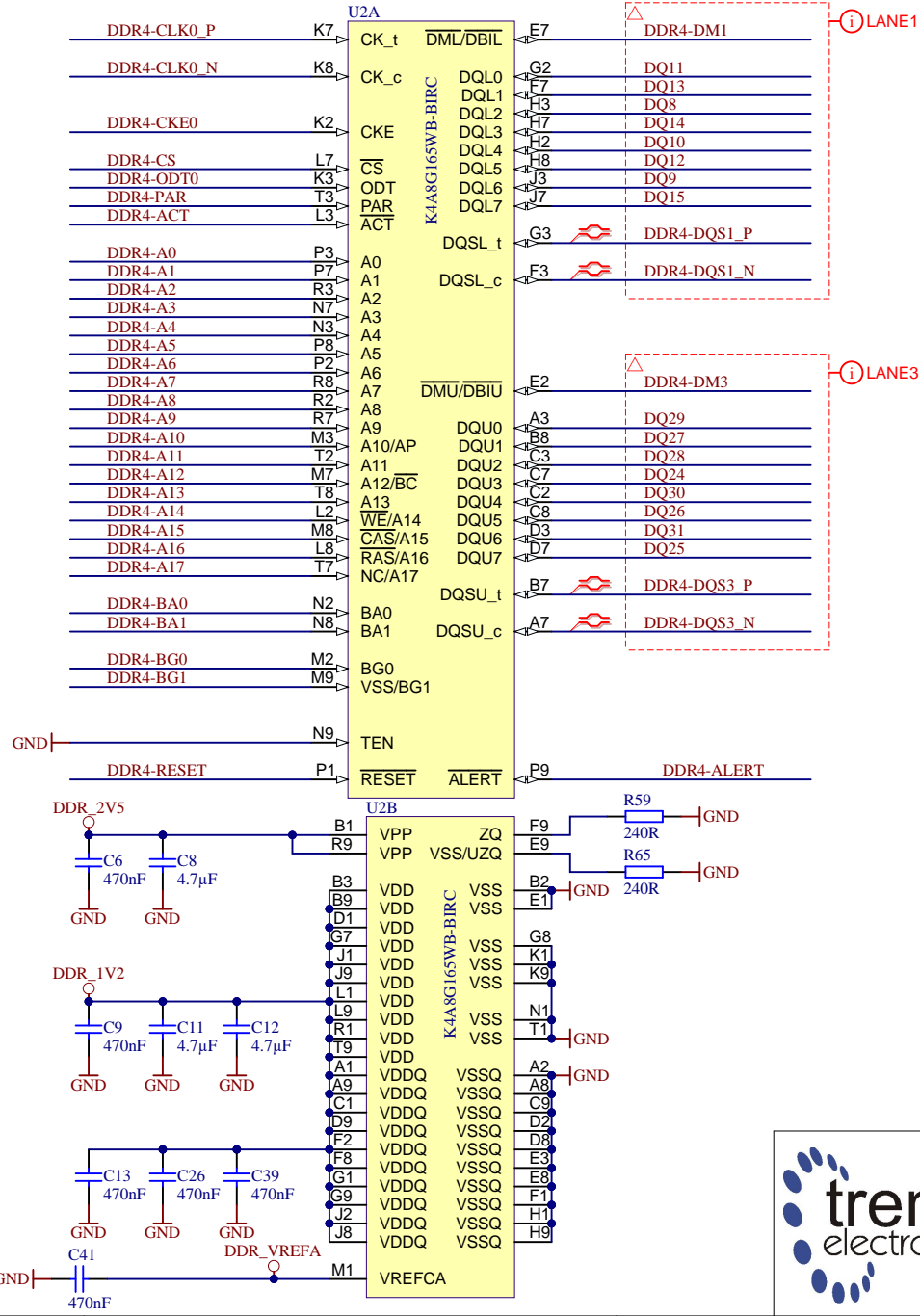
Title: B2B_2		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	
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Filename: B2B_2.SchDoc		



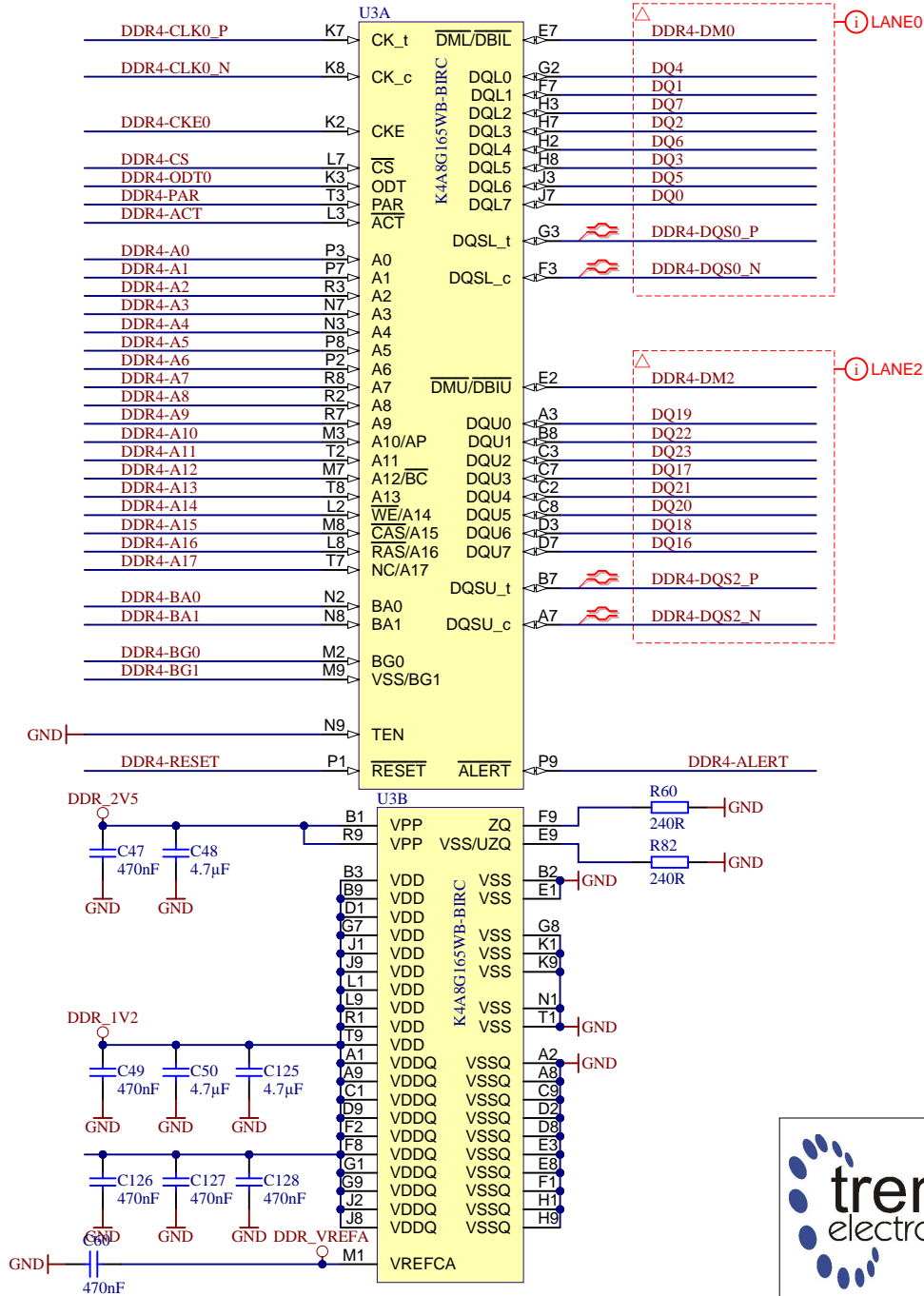
Title: Ethernet		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 18 of 34
Filename: Ethernet.SchDoc		



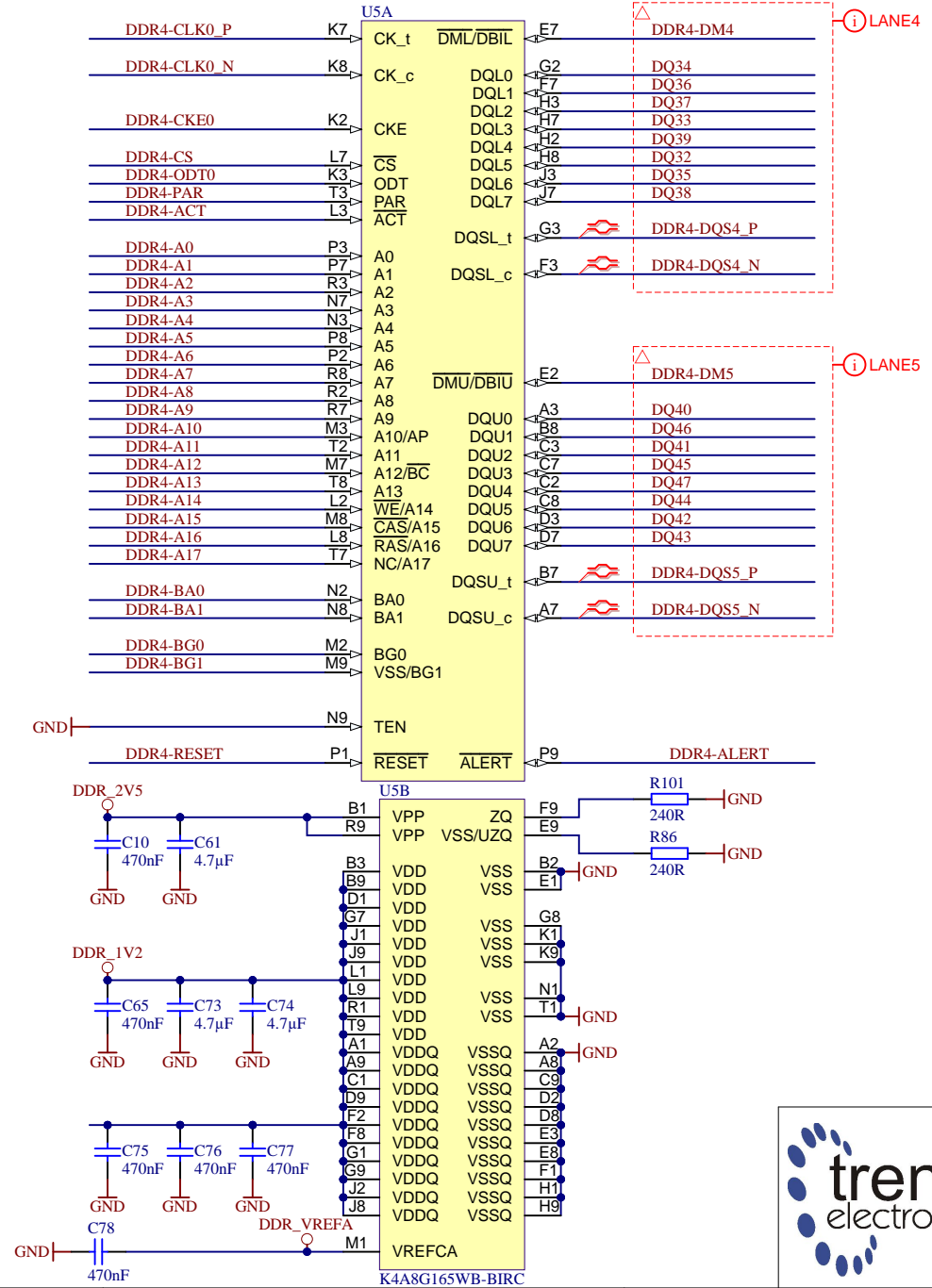
Title: USB-PHY		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 19 of 34
Filename: USB-PHY.SchDoc		



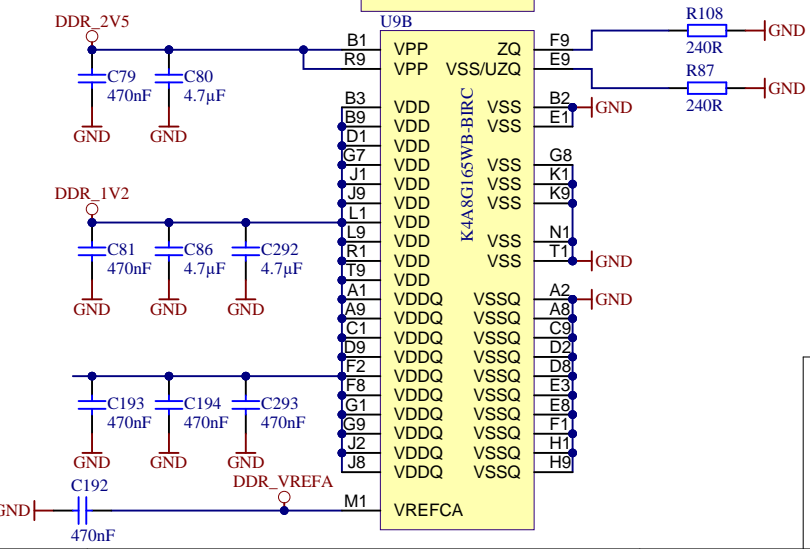
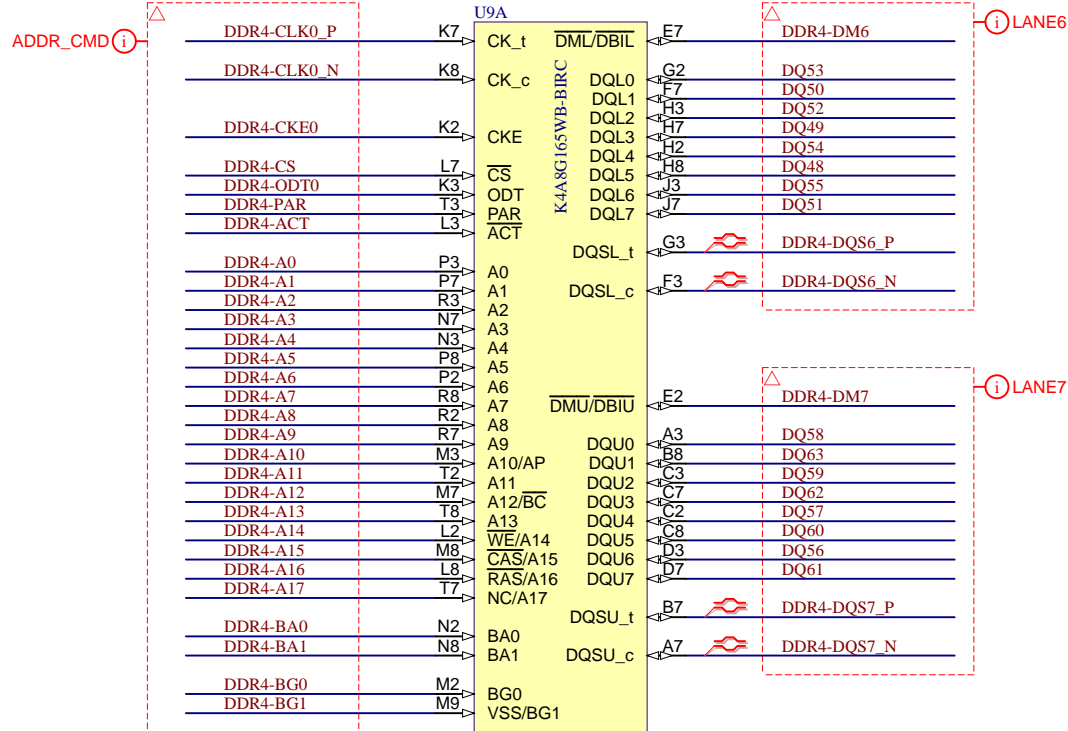
Title: DDR4-RAM		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 20 of 34
Filename: DDR4-RAM.SchDoc		



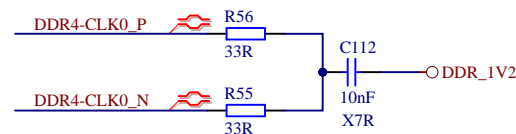
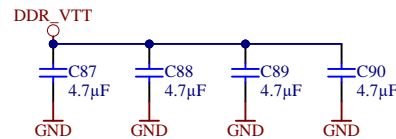
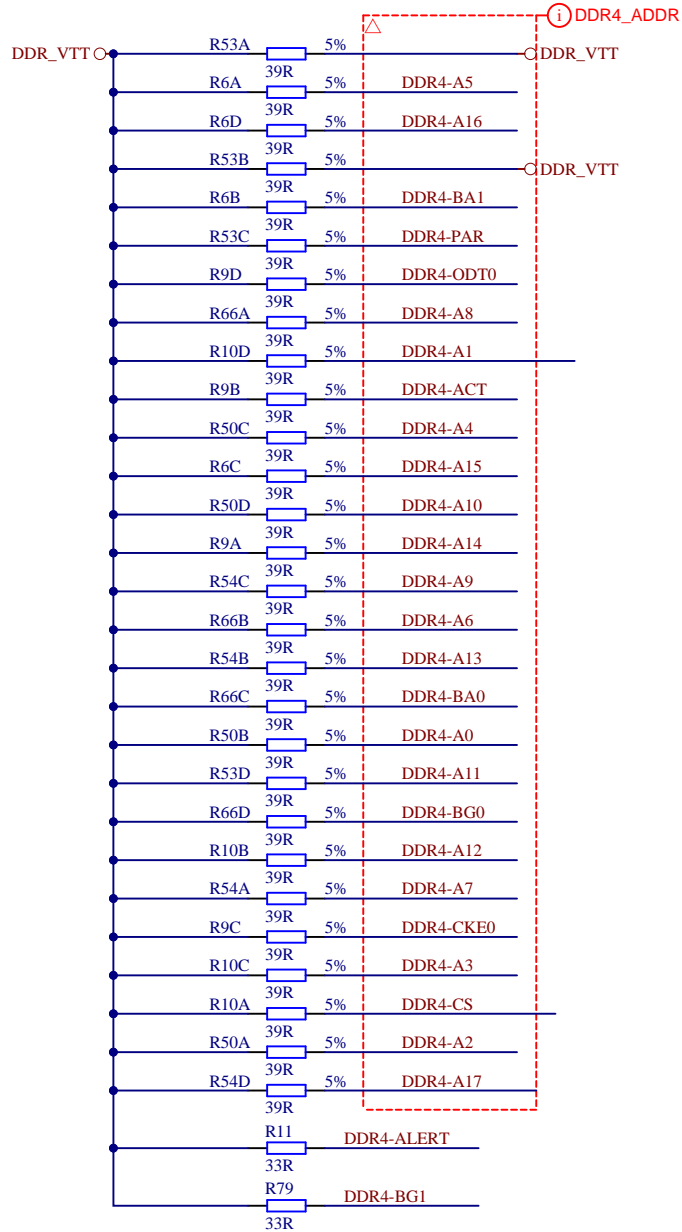
Title: DDR4-RAM_2		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 21 of 34
Filename: DDR4-RAM_2.SchDoc		



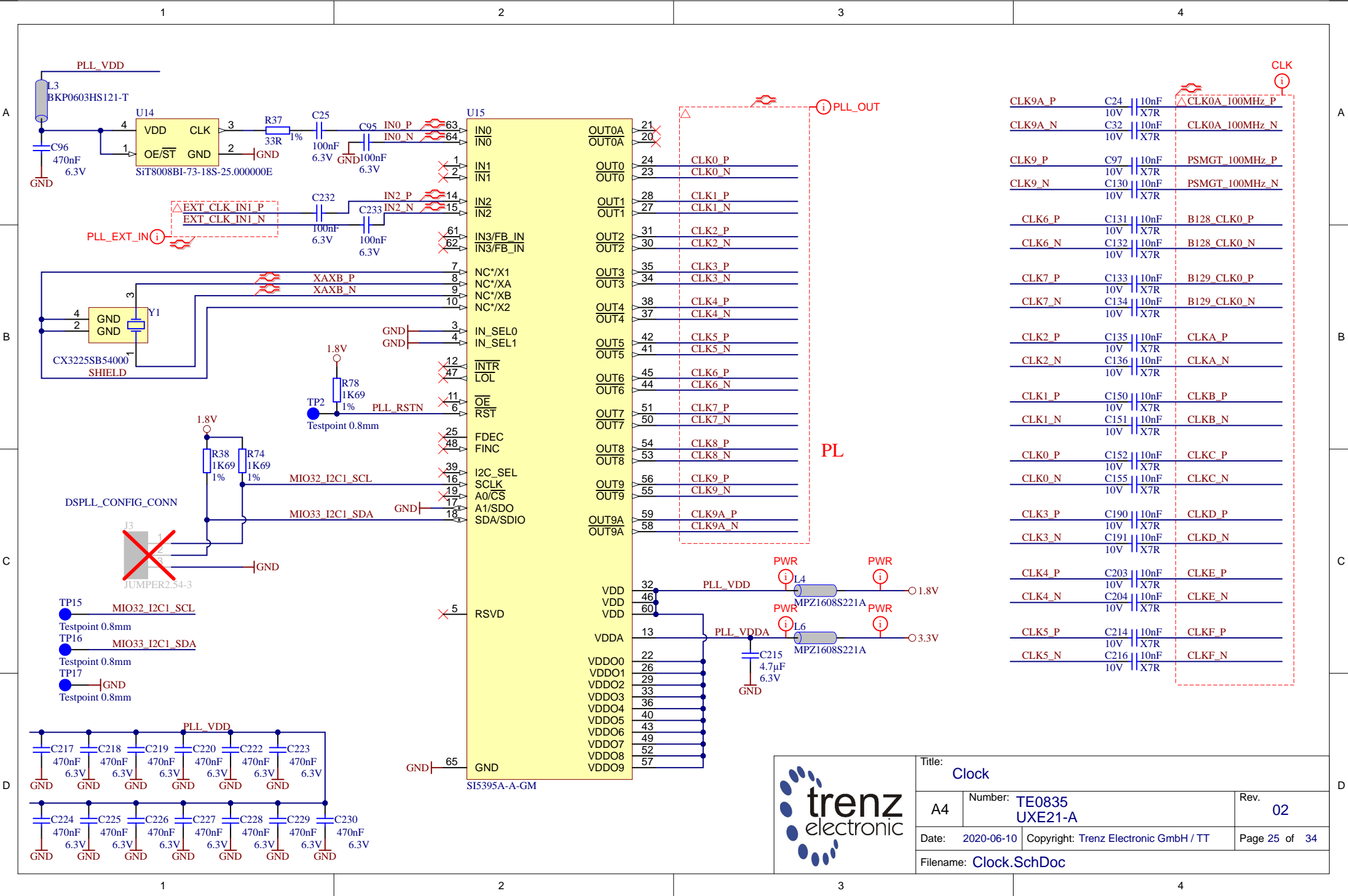
Title: DDR4-RAM_3		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 22 of 34
Filename: DDR4-RAM_3.SchDoc		



Title: DDR4-RAM_4		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 23 of 34
Filename: DDR4-RAM_4.SchDoc		



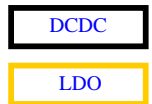
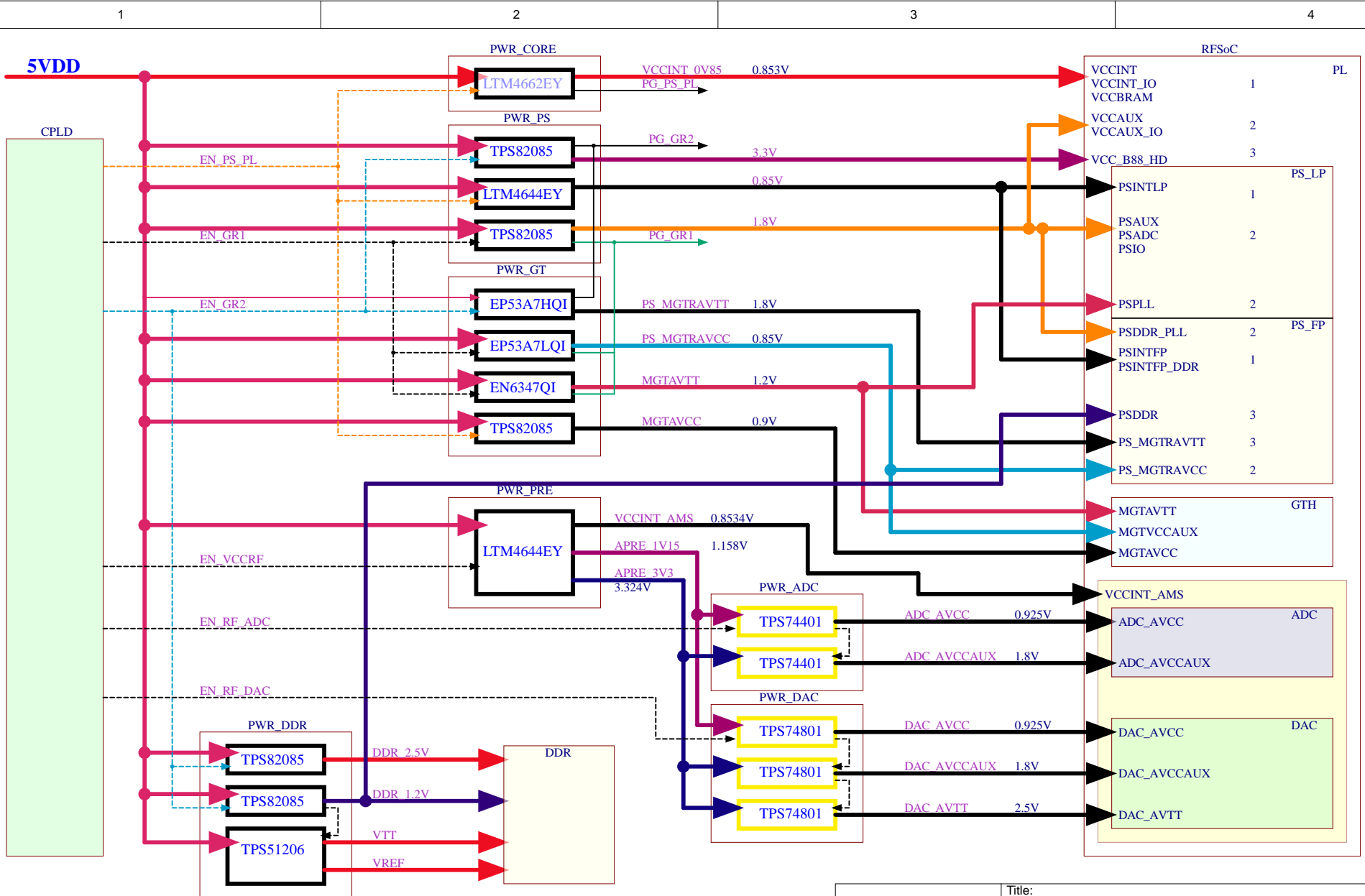
Title: DDR4-TERM		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 24 of 34
Filename: DDR4-TERM.SchDoc		



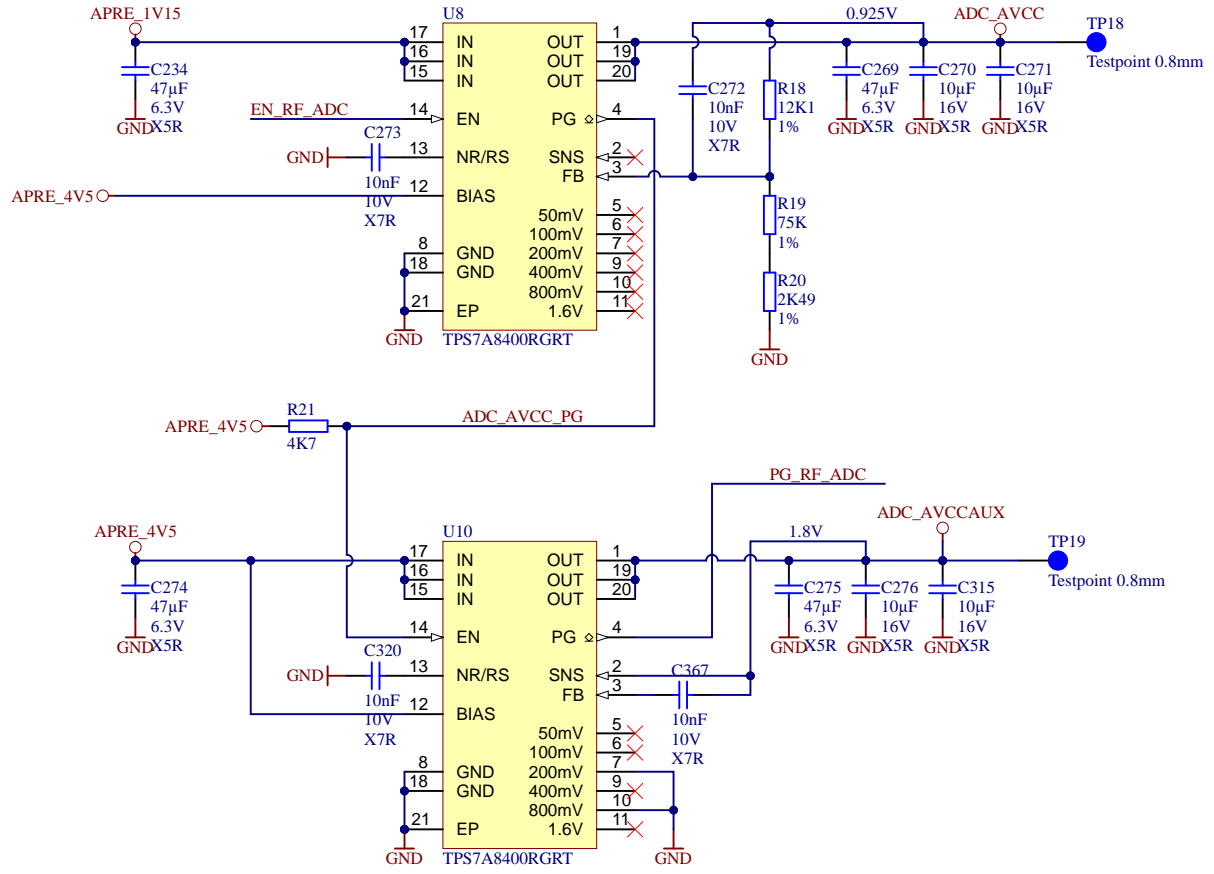
CLK9A_P	C24	10nF	CLK0A_100MHz_P
CLK9A_N	C32	10nF	CLK0A_100MHz_N
CLK9_P	C97	10nF	PSMGT_100MHz_P
CLK9_N	C130	10nF	PSMGT_100MHz_N
CLK6_P	C131	10nF	B128_CLK0_P
CLK6_N	C132	10nF	B128_CLK0_N
CLK7_P	C133	10nF	B129_CLK0_P
CLK7_N	C134	10nF	B129_CLK0_N
CLK2_P	C135	10nF	CLKA_P
CLK2_N	C136	10nF	CLKA_N
CLK1_P	C150	10nF	CLKB_P
CLK1_N	C151	10nF	CLKB_N
CLK0_P	C152	10nF	CLKC_P
CLK0_N	C155	10nF	CLKC_N
CLK3_P	C190	10nF	CLKD_P
CLK3_N	C191	10nF	CLKD_N
CLK4_P	C203	10nF	CLKE_P
CLK4_N	C204	10nF	CLKE_N
CLK5_P	C214	10nF	CLKF_P
CLK5_N	C216	10nF	CLKF_N




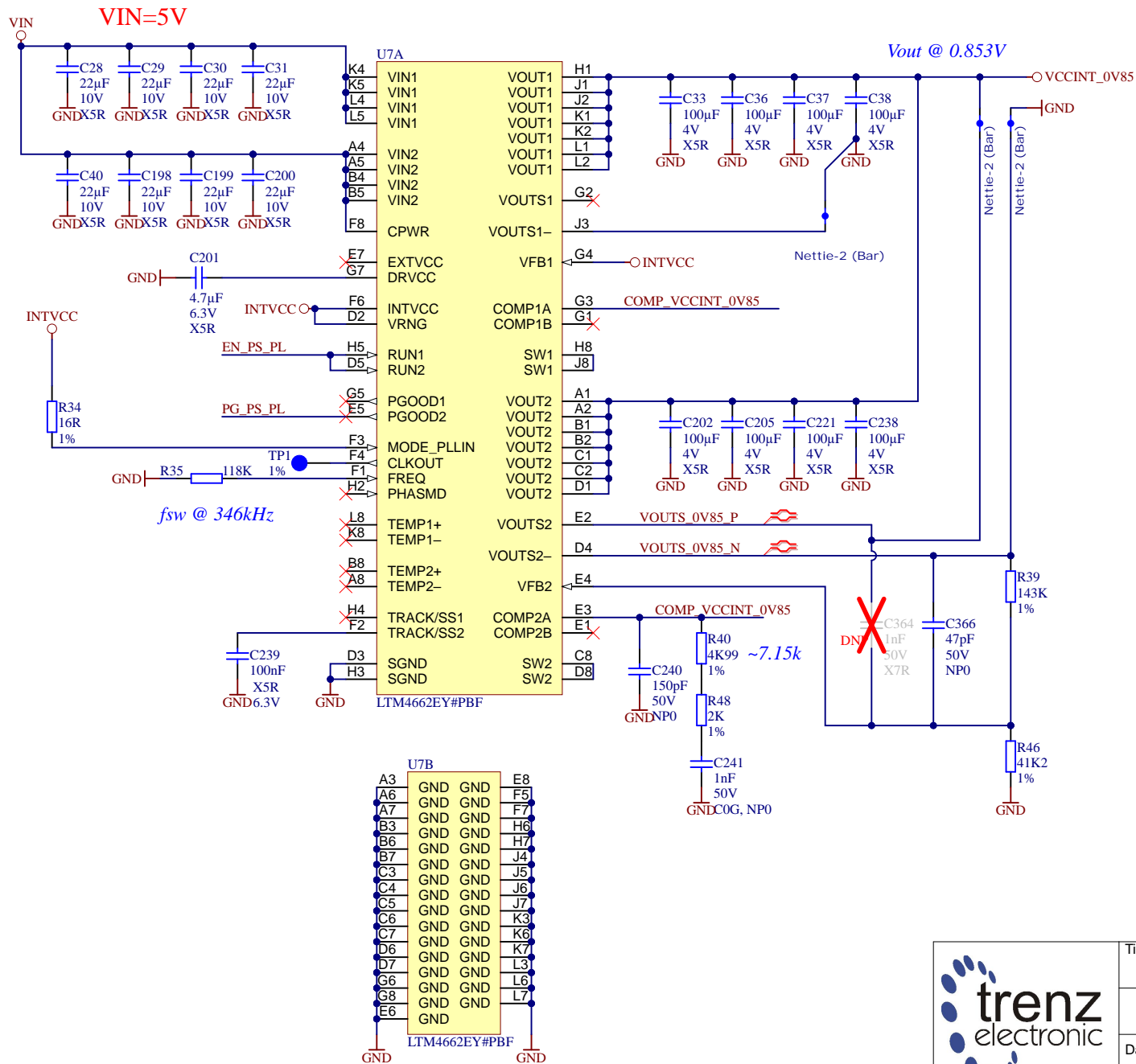
Title: Clock		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH / TT	Page 25 of 34
Filename: Clock.SchDoc		



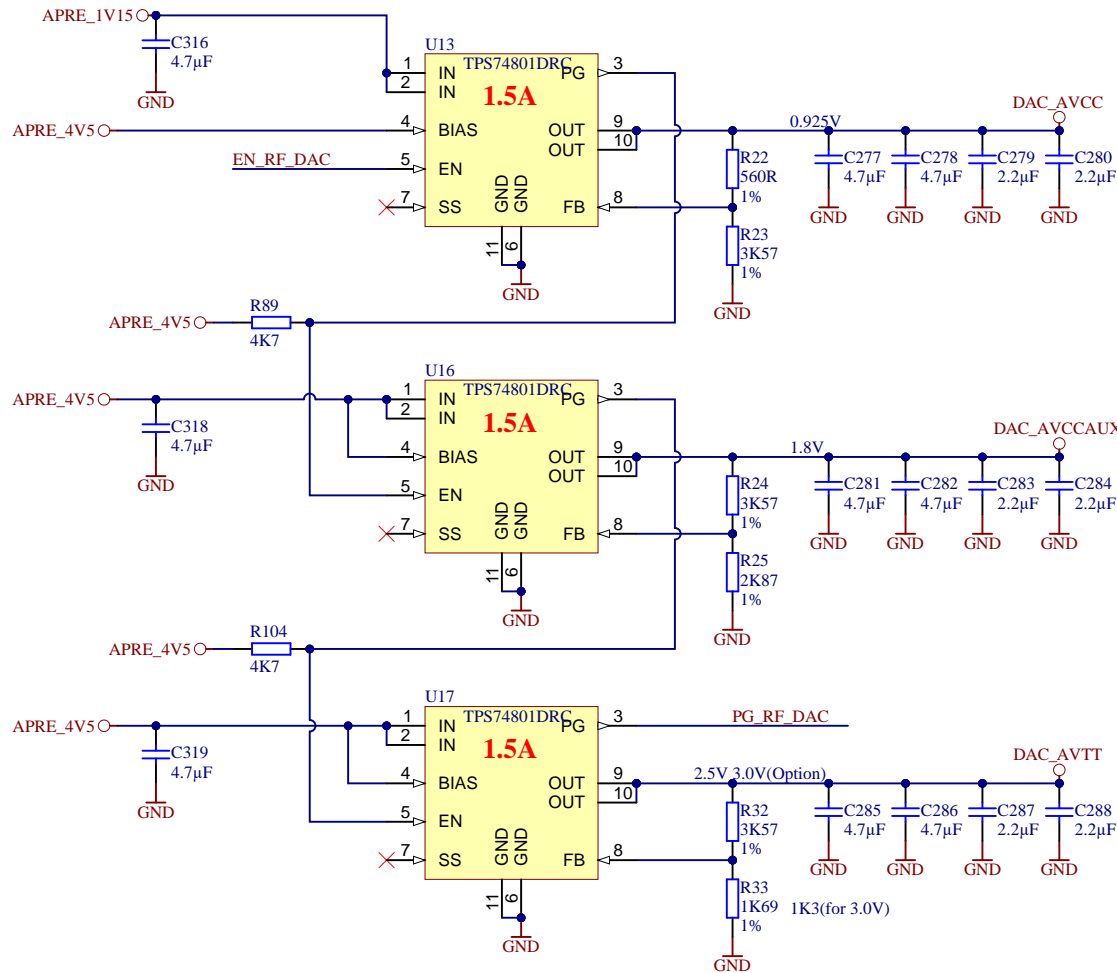
Title: PWR_Structure		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	
Filename: PWR_Structure.SchDoc		Page 26 of 34




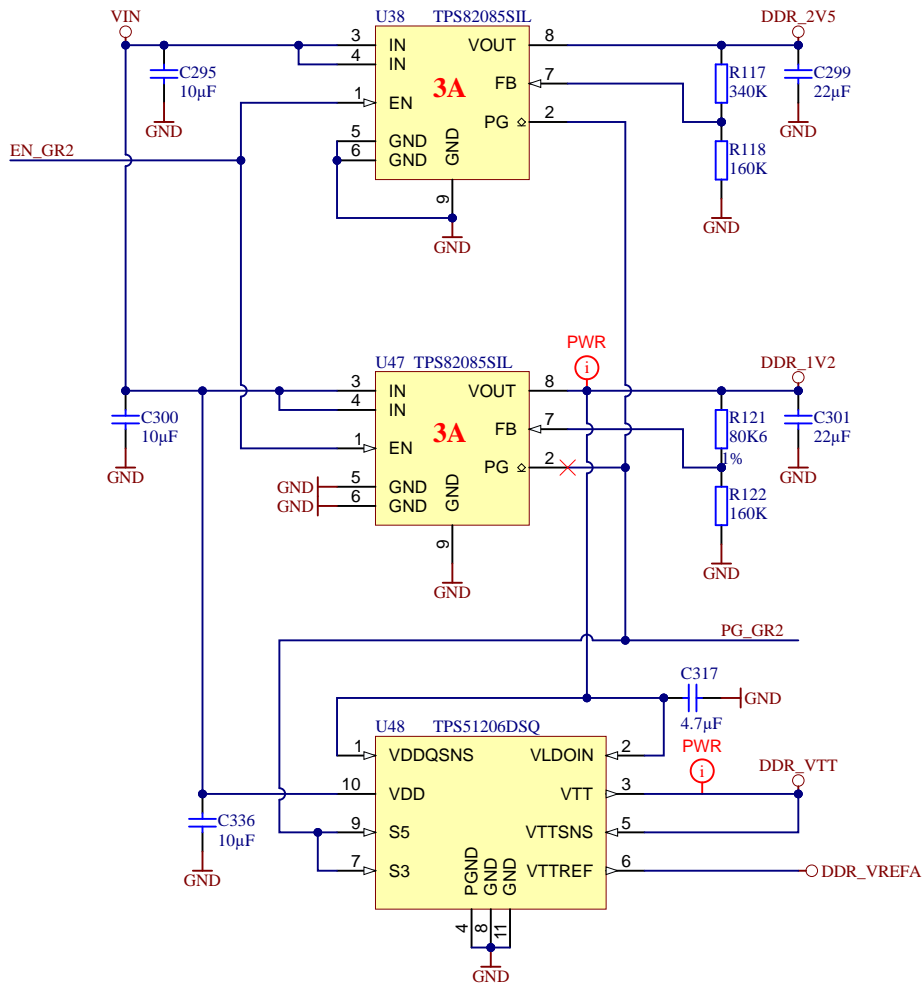
			Title: PWR_ADC	
			A4	Number: TE0835 UXE21-A
Date: 2020-06-10		Copyright: Trenz Electronic GmbH		Page 27 of 34
Filename: PWR_ADC.SchDoc				




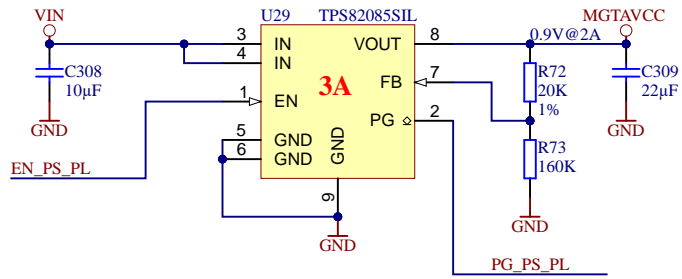
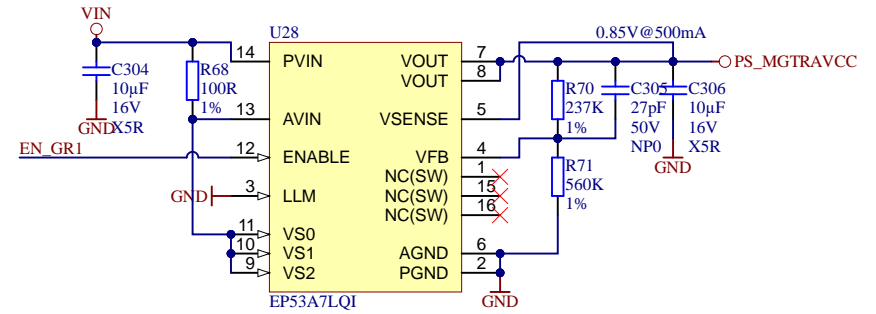
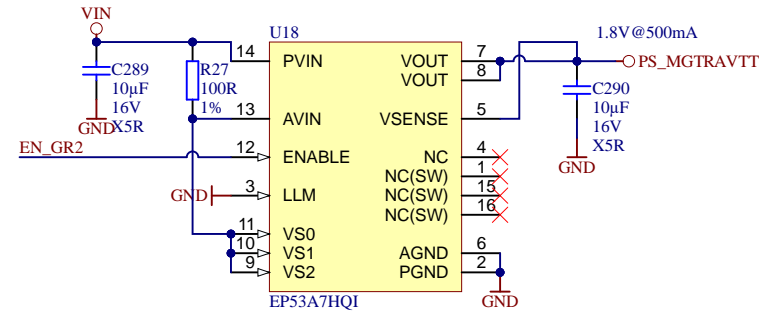
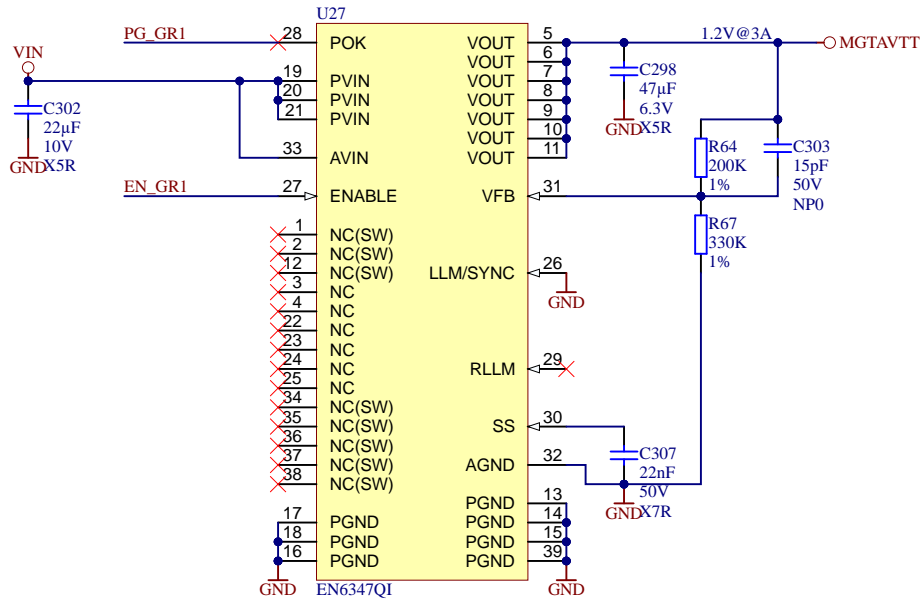
Title: PWR_CORE		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 28 of 34
Filename: PWR_CORE.SchDoc		



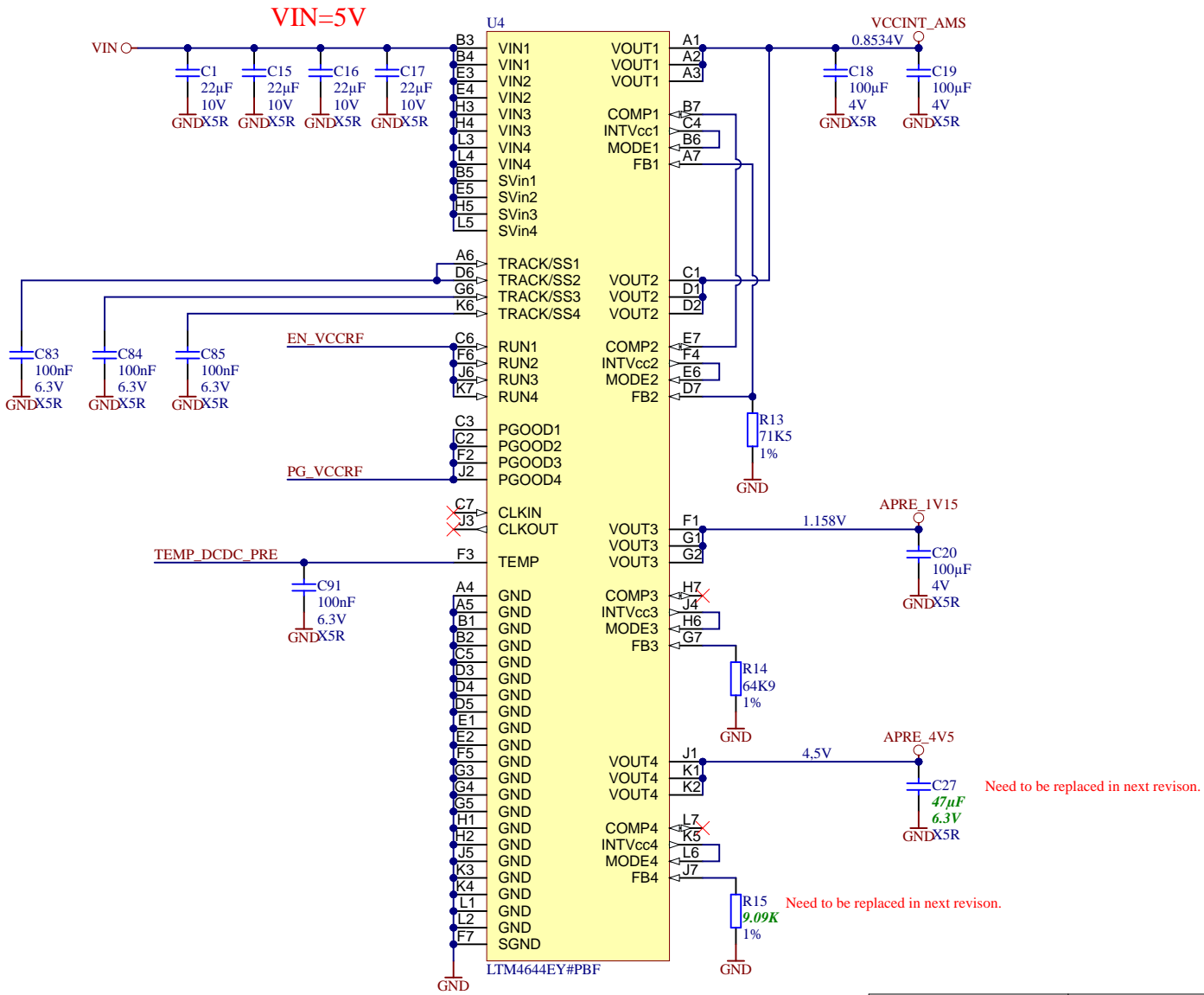
		Title: PWR_DAC	
		A4	Number: TE0835 UXE21-A
Date: 2020-06-10		Copyright: Trenz Electronic GmbH	
Filename: PWR_DAC.SchDoc		Page 29 of 34	




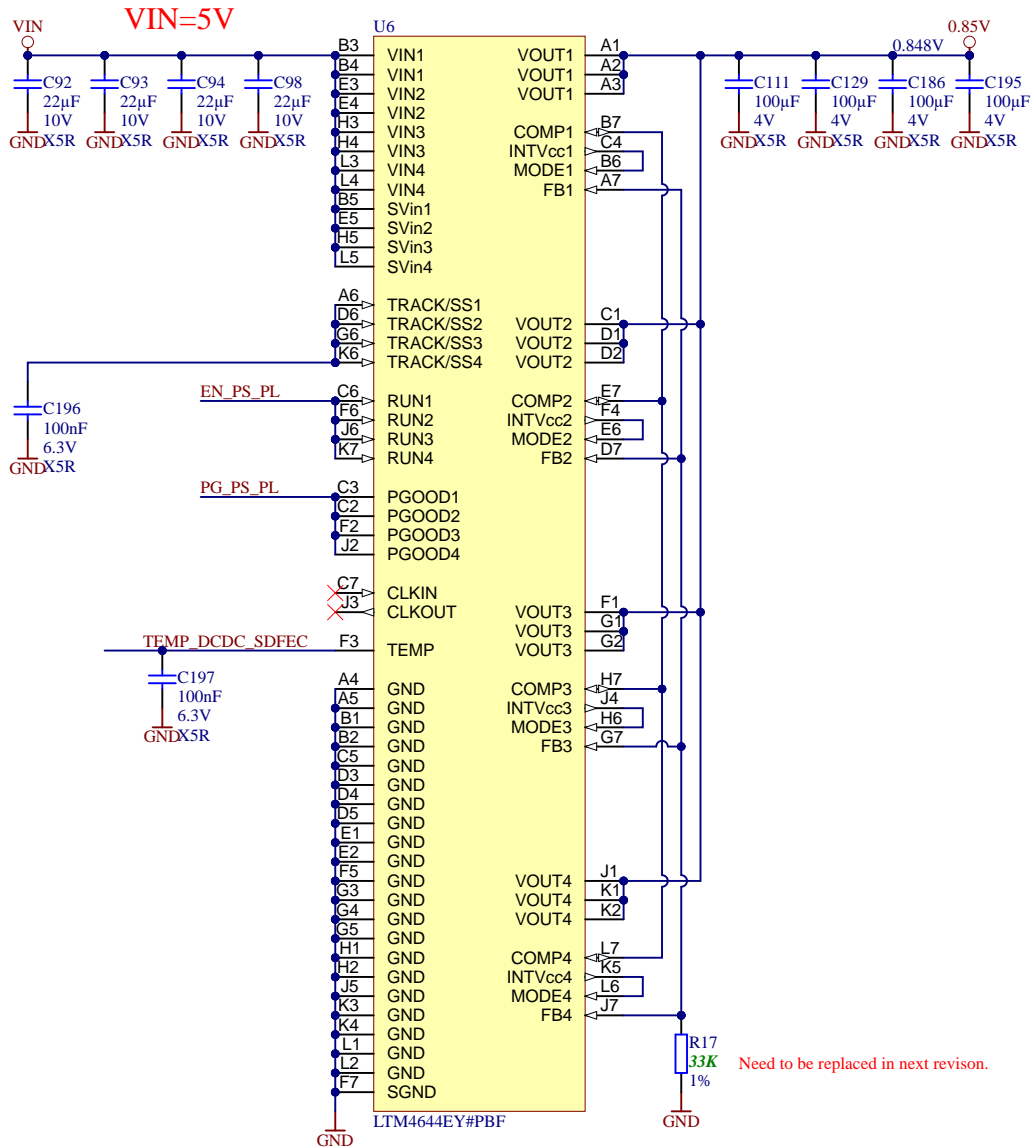
		Title: PWR_DDR	
		A4	Number: TE0835 UXE21-A
Date: 2020-06-10		Copyright: Trenz Electronic GmbH	
Date: 2020-06-10		Page 30 of 34	
Filename: PWR_DDR.SchDoc			



Title: PWR_GT		
A4	Number: TE0835 UXE21-A	Rev. 02
Date: 2020-06-10	Copyright: Trenz Electronic GmbH	Page 31 of 34
Filename: PWR_GT.SchDoc		

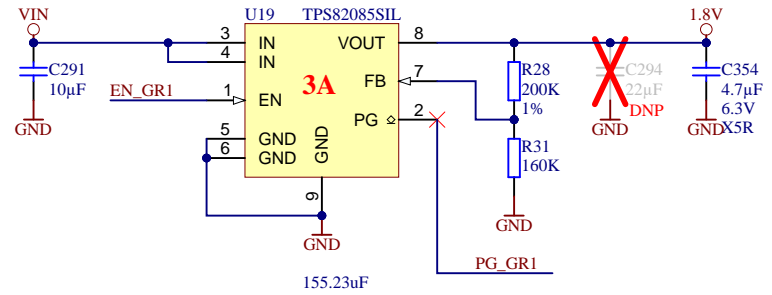


			Title: PWR_PRE	
			A4	Number: TE0835 UXE21-A
Date: 2020-06-10		Copyright: Trenz Electronic GmbH		Page 32 of 34
Filename: PWR_PRE.SchDoc				

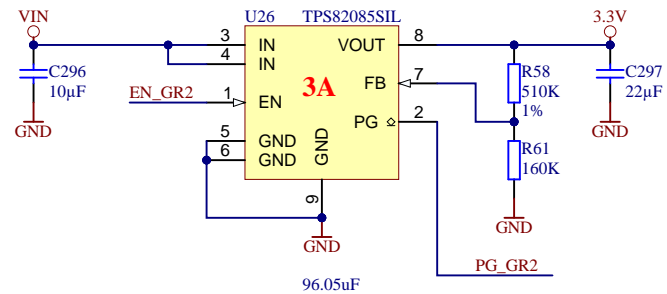


Need to be replaced in next revision.

Max C load < 150uF




Max C load < 150uF



Title: PWR_PS		
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REVISION HISTORY

REV	Description	
-01	Initial revision	IG
-02	<ol style="list-style-type: none"> 1. Added a VRP resistor on bank 65; 2. LDO U33 is changed on ADP7102ACPZ; 3. Signal FPGA IO0 is connected on AE18 pin of FPGA; 4. Signal DBG_LED3 is connected on AD18 pin of FPGA; 5. Signal MIO13_25 connected to J1 pin 33 instead MIO25. 6. Resistor R84 is removed; 7. LED D1 moved on edge of PCB; 8. Added THT testpoints J4 on CPLD_JTAGEN, R76 was removed; 9. Signals B49_XX_X are renamed in B88_XX_X; 10. C241 is changed on 1nF; 11. Length of CLK signals on RFADC and RFDAC are adjusted; 12. Wrong connection on U8 is fixed (PCB); 13. Wrong connection PGOOD1 pin of U7 is fixed; 14. R17 is changed from 35,5K to 33K for VCC_PL_PS correction. 	IG
	<ol style="list-style-type: none"> 15. APRE_3V3 renamed to APRE_4V5, voltage of the power rail increased from 3.3V to 4,58V. 16. Resistor R15 is changed from 13,3K to 9,09K. AN: 24671->25969 17. Capacitor C27 is changed from 100uF x 4V to 47uF x 6,3V. AN: 28940->24718 	IG

	Title: Revision_Changes		
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	Filename: Revision_Changes.SchDoc		