TE0835 TRM

Revision v.59

Exported on 2022-02-17

Online version of this document:

https://wiki.trenz-electronic.de/display/PD/TE0835+TRM

1 Table of Contents

2 Table of Figures

3 Table of Tables

$body

4 Overview

The Trenz Electronic TE0835 is an extended-grade module based on Xilinx Zynq UltraScale+ RFSoC. The module is equipped with 4x 8Gb DDR4 SDRAM Memory, 2x 512Mb SPI Flash Memory, USB2.0, Ethernet Transceiver and 2x Samtec Razor Beam Borard to Board (B2B) Connectors. The system controller CPLD is provided by Lattice MachXO2.

The Zynq UltraScale+ RFSoC family integrates key subsystems for multiband, multi-mode cellular radios and cable infrastructure (DOCSIS) into an SoC platform that contains a feature-rich 64-bitquad-core Arm Cortex-A53 and dual-core Arm Cortex-R5 based processing system.

Refer to http://trenz.org/te0835-info for the current online version of this manual and other available documentation.

4.1 Key Features

- **SoC/FPGA**
  - Package: FFVE1156, FSVE1156
  - Device: ZU25, ZU27, ZU28, ZU42, ZU43, ZU47, ZU48*
  - Engine: DR
  - Speed: -1, -L1, -2, -L2
  - Temperature: E, I*
- **RAM/Storage**
  - 4x 8Gb DDR4
  - 2x 512Mb SPI Flash
  - 2k I^2C EEPROM
- **On Board**
  - Lattice MachXO2 CPLD
  - Programmable Clock Generator
  - USB2.0 Transceiver
  - Gigabit Ethernet Transceiver
  - 3x Oscillators
  - 4x User LEDs
- **Interface**
  - 2x Samtec Razor Beam ST5 (2x80 pol) Board to Board Connectors
- **Power**
  - 5V Input Supply Voltage
- **Dimension**
  - 90 x 65 mm
- **Note**
  - * Different packages, speed and temperature range are available on assembly options

4.2 Block Diagram

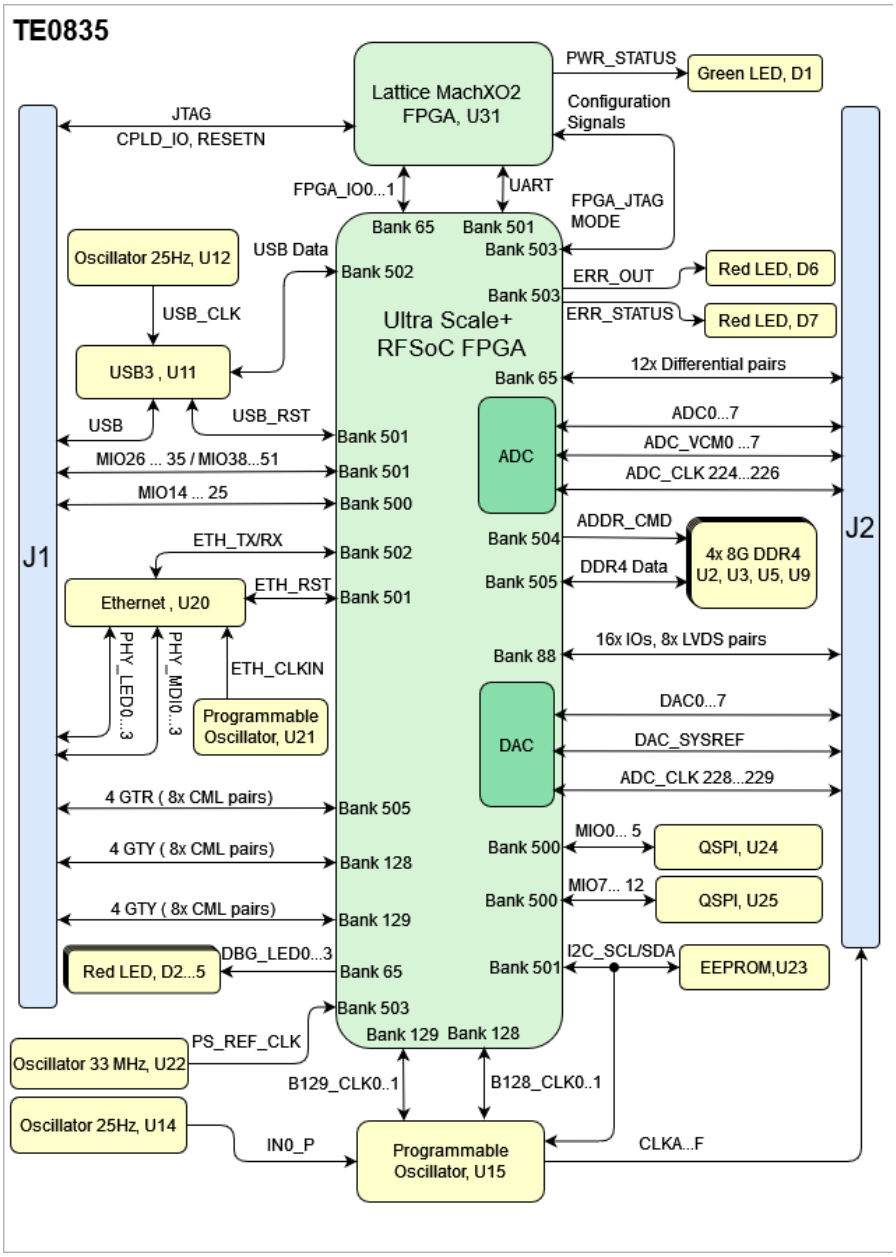

Figure 1: TE0835 block diagram

4.3 Main Components

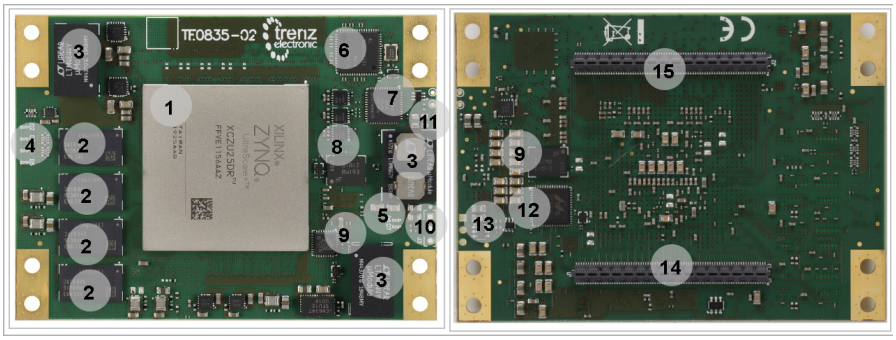

Figure 2: TE0835 main components

1. Xilinx UltraScale+ RFSoC, U1
2. 8Gb DDR4 SDRAM, U2,U3,U5,U9
3. Voltage Regulators, U4,U6,U7
4. User Red LEDs, D2...5
5. Error/Status Red LEDs, D6...7
6. Programmable Glock Generator, U15
7. Lattice MachXO2 CPLD, U31
8. Dual SPI Flash, U24-U25
9. USB2.0 Transceiver, U11
10. Pin Header 3x1, J3 (not Soldered)
11. Green LED, D1
12. Gigabit Ethernet Transceiver, U20
13. EEPROM, U23
14. B2B Connectors, J1
15. B2B Connectors, J2

4.4 Initial Delivery State

Storage device name	Content	Notes
2x SPI Flash	Not Programmed	
System Controller CPLD	Programmed	
EEPROM	Not Programmed	
4x DDR4 SDRAM	Not Programmed	
Programmable Clock Generator	Not Programmed	

Table 1: Initial delivery state of programmable devices on the module

4.5 Configuration Signals

Configuration must be set through CPLD,U31 by setting MODE0...3 signals.

MODE[3:0]	Boot Mode	Note
0000	PS_JTAG	Refer to CPLD Page
0001	Quad SPI Flash	Refer to CPLD Page
0101	SD Card	Refer to CPLD Page

Table 2: Boot process.
The reset pin is active low.

Signal	B2B	I/O	Note
RESETN	J1-36	Input	Pulled up to 3.3V_CPLD

Table 3: Reset process.

5 Signals, Interfaces and Pins

5.1 Board to Board (B2B) I/Os

FPGA bank number and number of I/O signals connected to the B2B connector:

FPGA Bank	B2B Connector	Number of I/Os	Voltage Level	Notes
Bank 500	J1	12x Single Ended	1.8V	MIO14...25
Bank 501	J1	20x Single Ended	1.8V	MIO26...51
Bank 505	J1	18x Single Ended, 9x Differential pairs	0.85V	EXT_CLKIN_PSMGT, RX/TX0...3
Bank 128	J1	2x Differnetial CLK Input, 8x Differential Transceiver	--	B128_CLK, RX/TX0...3
Bank 129	J1	2x Differnetial CLK Input 8x Differential Transceiver	--	B129_CLK, RX/TX0...3
Bank 65	J2	24x Single Ended, 12x Differential pairs	1.8V	HP Bank
Bank 88	J2	16x Single Ended, 8x Differential pairs	3.3V	HD Bank
ADC	J2	16x Single Ended,	Variable	

FPGA Bank	B2B Connector	Number of I/Os	Voltage Level	Notes
		8x Differential pairs 4x Differential Clocks		
DAC	J2	16x Single Ended, 8x Differential pairs 3x Differential Clocks	Variable	

Table 4: General PL I/O to B2B connectors information

5.2 JTAG Interface

JTAG access to the Xilinx UltraScale+ MPSoC is through B2B connector JM1. JTAG signals routed directly through the CPLD to FPGA. Access between CPLD and FPGA can be multiplexed via JTAGEN (logical one for CPLD, logical zero for FPGA) on B2B. When the CPLD_JTAGEN is 0 or off, it provides FPGA access and when it is 1 or ON, it provides CPLD access.

JTAG Signal	B2B Connector
JTAG_TMS	J1-24
JTAG_TDI	J1-20
JTAG_TDO	J1-18
JTAG_TCK	J1-22

Table 5: JTAG pins connection

5.3 MIO Pins

MIO Pin	Connected to	B2B	Notes
MIO0...12	SPI FLash, U24-U25	-	Dual SPI FLash
MIO13	LED Green, D1	-	3.3V_CPLD
MIO14...25	FPGA Bank 500,U1	J1	PSMIO
MIO26...27	FPGA Bank 501,U1	J1	PSMIO
MIO28...29	CPLD, U31	-	UART_TX, UART_RX
MIO30...31	FPGA Bank 501, U1	J1	PSMIO
MIO32...33	EEPROM,U23	-	I2C_SCL, I2C_SDA
MIO34...35	FPGA Bank 501,U1	J1	PSMIO
MIO36	Gigabit ETH, U20	-	ETH_RST
MIO37	USB2.0, U11	-	USB_RST
MIO38...51	FPGA Bank 501, U1	J1	PSMIO
MIO52...62	USB2.0, U11	-	USB
MIO63...77	Gigabit ETH, U20	-	ETH

Table 6: MIOs pins

5.4 Test Points

Test Point	Signal	Connected to	Notes
TP1	CLKOUT	Voltage Regulator, U7	
TP2	PLL_RSTN	Programmable Clock Generator, U15	
TP4	CPLD_JTAGEN	B2B, J1 CPLD, U31	
TP5	JTAG_TDO	B2B, J1 CPLD, U31	

Test Point	Signal	Connected to	Notes
TP6	JTAG_TDI	B2B, J1 CPLD, U31	
TP7	JTAG_TCK	B2B, J1 CPLD, U31	
TP8	JTAG_TMS	B2B, J1 CPLD, U31	
TP9	GND	GND	
TP10...11	IO_L1P_AD15P_88, O_L4N_AD12N_88	FPGA Bank 88, U1	
TP12	VIN	B2B, J1	
TP13...14	GND	GND	
TP15...16	MIO32-MIO33	EEPROM,U23 FPGA Bank 501, U1	
TP17	GND	GND	
TP18	ADC_AVCC	LDO Voltage Regulator, U8	
TP19	ADC_AVCCAUX	LDO Voltage Regulator, U10	
TP20	3.3V_CPLD	CPLD, U31 B2B, J1	
T21	CPLD_JTAGEN	B2B, J1 CPLD, U31	

Table 7: Test Points Information

6 On-board Peripherals

Chip/Interface	Designator	Notes
QSPI Flash(see page 15)	U24, U25	
DDR4 SDRAM(see page 21)	U2, U3, U5, U9	
CPLD(see page 16)	U31	
USB2.0(see page 18)	U11	
Gigabit Ethernet(see page 19)	U20	
Programmable Clock Generator(see page 21)	U15	
EEPROM(see page 20)	U22	
Oscillators(see page 21)	U14, U21, U12	
LEDs(see page 20)	D0...7	

Table 8: On board peripherals

6.1 Quad SPI Flash Memory

The TE0835 is a Dual SPI Flash module equipped with two SPI Flash U24, U25 connecfted to PSMIO FPGA bank 500.

MIO Pin	Schematic	U24 Pin	U25 Pin	Notes
MIO0	MIO0_QSPI	CLK	-	
MIO1	MIO1_QSPI	DO	-	
MIO2	MIO2_QSPI	nWP	-	
MIO3	MIO3_QSPI	nHOLD	-	
MIO4	MIO4_QSPI	DI	-	
MIO5	MIO5_QSPI	nCS	-	
MIO7	MIO5_QSPI	-	nCS	

MIO Pin	Schematic	U24 Pin	U25 Pin	Notes
MIO8	MIO5_QSPI	-	DI	
MIO9	MIO5_QSPI	-	DO	
MIO10	MIO5_QSPI	-	nWP	
MIO11	MIO5_QSPI	-	nHOLD	
MIO12	MIO5_QSPI	-	CLK	

Table 9: Quad SPI interface MIOs and pins

6.2 System Controller CPLD

The System Controller CPLD (U31) is provided by Lattice Semiconductor LCMXO2-460HC. The CPLD provides JTAG routing, boot mode, User IOs, LEDs, firmware and power management access. For more information please refer to the TE0835 CPLD[1] page.

Schematic /Pin	Connected to	Description	Note
MODE0...3	FPGA Bank 503, U1	Boot Mode	
POR_B	FPGA Bank 503, U1	Programming Status	Pulled up
PORG_B	FPGA Bank 503, U1	Programming Status	Pulled up
INIT_B	FPGA Bank 503, U1	Configuration initialization	Pulled up
DONE	FPGA Bank 503, U1	Configuration Done Status	Pulled up
F_TCK	FPGA Bank 503, U1	FPGA JTAG	
F_TDI	FPGA Bank 503, U1	FPGA JTAG	

1 https://wiki.trenz-electronic.de/display/PD/TE0835+CPLD

Schematic /Pin	Connected to	Description	Note
F_TMS	FPGA Bank 503, U1	FPGA JTAG	
F_TDO	FPGA Bank 503, U1	FPGA JTAG	
JTAG_TDO	B2B, J1	CPLD JTAG	
JTAG_TMS	B2B, J1	CPLD JTAG	
JTAG_TDI	B2B, J1	CPLD JTAG	
JTAG_TCK	B2B, J1	CPLD JTAG	
CPLD_JTAG EN	B2B, J1	CPLD JTAG Enable	
CPLDIO0...3	B2B, J1	CPLD IOs	
RESETN	B2B, J1	Reset	
MIO13	LED Green, D1	3.3V_CPLD	
MIO28	FPGA Bank 501, U1	UART_TX	
MIO29	FPGA Bank 501, U1	UART_RX	
FPGA_IO0... 1	FPGA Bank 65, U1	IOs	
EN_PS_PL	Voltage Regulators, U6, U7, U29	PS/PL Enable Signals	Pulled Down
EN_GR1	Voltage Regulators, U19, U27, U28	MGTAVTT, PSLL	Pulled Down
EN_GR2	Voltage Regulators, U38, U18, U38	PS_MGTRAVTT, 3.3, DDR2.5V	Pulled Down

Schematic /Pin	Connected to	Description	Note
EN_RF_ADC	Voltage Regulators, U8	Enable ADC	Pulled Down
PG_RF_DAC	Voltage Regulators, U17	ADC Power Good Status	Pulled Down
PG_PS_PL	Voltage Regulators, U6, U7, U29	PS/PL Power Good Status	Pulled Down
EN_RF_DAC	Voltage Regulators, U13	Enable DAC	Pulled Down
PG_RF_DAC	Voltage Regulators, U10	DAC Power Good Status	Pulled Down

Table 10: USB2.0 interface connections and pins

6.3 USB2.0

The TE0835 is equipped with a USB2.0, U11.

U11 Pin	Schematic	Connected to	Notes
RESETB	USB0_RST	FPGA Bank 501, U1	
VDDIO	1.8V	1.8V	
CPEN	USB0_CPE	B2B, J1	
VBUS	USB0_VBUS	B2B, J1	
ID	USB0_ID	B2B, J1	
DP	USB0_D_P	B2B, J1	
DM	USB0_D_N	B2B, J1	
REFCLK	USB_CLK	Oschillator, U12	
STP	USB0_STP	FPGA Bank 502, U1	
NXT	USB0_NXT	FPGA Bank 502, U1	
DIR	USB0_DIR	FPGA Bank 502, U1	

U11 Pin	Schematic	Connected to	Notes
CLKOUT	USB_CLK	Oschillator, U12	
DATA0...7	USB0_DATA0...8	FPGA Bank 502, U1	

Table 11: USB2.0 interface connections and pins

6.4 Ethernet

The module TE0835 is equipped with a Gigabit Ethernet Transceiver, U20.

U20 Pin	Signal Name	Connected to	Signal Description	Note
MDIO	ETH_MDIO	FPGA Bank 502, U1	Data Management	
MDC	ETH_MDC	FPGA Bank 502, U1	Data Management clock reference for the serial interface	
TX_CLK	ETH_TXCK	FPGA Bank 502, U1	Transmit Clock	
TX_CTRL	ETH_TXCTL	FPGA Bank 502, U1	Transmit Control	
TXD0...3	ETH_TXD0...3	FPGA Bank 502, U1	Transmit Data	
RX_CLK	ETH_RXCK	FPGA Bank 502, U1	Receive Clock	
RX_CTRL	ETH_RXCTL	FPGA Bank 502, U1	Receive Control	
RXD0...3	ETH_RXD0...3	FPGA Bank 502, U1	Receive Data	

U20 Pin	Signal Name	Connected to	Signal Description	Note
RESETn	ETH_RST	FPGA Bank 501, U1	Ethernet reset, Active low.	
XTAL_IN	ETH_XTAL_IN	Oscillator, U21	Reference Clock	
MDI0...3	PHY_MDI0...3	B2B, J1	Media Dependent Interface 0...3	
LED0...1	PHY_LED0...1	B2B, J1	LED output	
LED/INT	PHY_LED2	B2B, J1	LED interrupt	

Table 12: Ethernet connections

6.5 EEPROM

The module TE0835 has an EEPROM IC (U23) connected to PSMIO FPGA Bank 501.

MIO Pin	Schematic	U23 Pin	Notes
MIO32	MIO32_I2C1_SCL	SCL	
MIO33	MIO33_I2C1_SDA	SDA	

Table 13: I2C EEPROM interface MIOs and pins

MIO Pin	I2C Address	Designator	Notes
MIO32...33	0xA1	U23	

Table 14: I2C address for EEPROM

6.6 LEDs

Designator	Color	Connected to	Active Level	Note
D1	Green	MIO13	Active High	3.3V CPLD

Designator	Color	Connected to	Active Level	Note
D2...5	Red	DBG_LED0...3	Active Low	User LED
D6	Red	ERR_OUT	Active High	
D7	Red	ERR_STATUS	Active High	

Table 15: On-board LEDs

6.7 DDR4 SDRAM

The TE0835 SoM has 4x 1 Gigabyte volatile DDR4 SDRAM IC for storing user application code and data.

- Part number: K4A8G165WB
- Supply voltage: 1.2 V
- Speed: 2400 Mbps
- Temperature: -40 ~ 95 °C

6.8 Clock Sources

Designator	Description	Frequency	Note
U14, U21	MEMS Oscillator	25MHz	
U22	MEMS Oscillator	33.33 MHz	
Y1	Crystal Oscillator	54 MHz	
U12	MEMS Oscillator	52MHz	
U15	Programmable Clock Generator	Variable	

Table 16: Oscillators

6.9 Programmable Clock Generator

There is a Silicon Labs I^2C programmable clock generator on-board (U10) in order to generate reference clocks for the module. Programming can be done using I^2C via PIN header J3. The I^2C Address is 0x69.

U15 Pin	Signal	Connected to	Direction	Note
IN0	IN0_P	Oscillator, U14	Input	
IN1	-	N.C	-	
IN2	EXT_CLK_IN1	B2B,J2	Input	
IN3	-	N.C		
nRST	PLL_RSTN	FPGA Bank 65,U1	Input	
SCL	MIO32_I2C1_SCL	Pin Header, J3	Input	I2C
SDA	MIO33_I2C1_SDA	Pin Header, J3	Input	I2C
OUT0	CLKC	B2B,J2	Output	Differential Clock
OUT1	CLKB	B2B,J2	Output	Differential Clock
OUT2	CLKA	B2B,J2	Output	Differential Clock
OUT3	CLKD	B2B,J2	Output	Differential Clock
OUT4	CLKE	B2B,J2	Output	Differential Clock
OUT5	CLKF	B2B,J2	Output	Differential Clock
OUT6	B128_CLK0	FPGA Bank 128,U1	Output	
OUT7	B129_CLK0	FPGA Bank 129,U1	Output	

U15 Pin	Signal	Connected to	Direction	Note
OUT8	CLK8	FPGA Bank 65,U1	Output	
OUT9	PSMGT_100MHZ	FPGA Bank 505,U1	Output	
OUT9A	CLK0A_100MHZ	B2B, J1	Output	

Table 17: Programmable Clock Generator Inputs and Outputs

7 Power and Power-On Sequence

7.1 Power Supply

Power supply with minimum current capability of 2.5A for system startup is recommended.

7.2 Power Consumption

Power Input Pin	Typical Current
VIN (5V)	TBD*

Table 18: Power Consumption
* TBD - To Be Determined

7.3 Power Distribution Dependencies

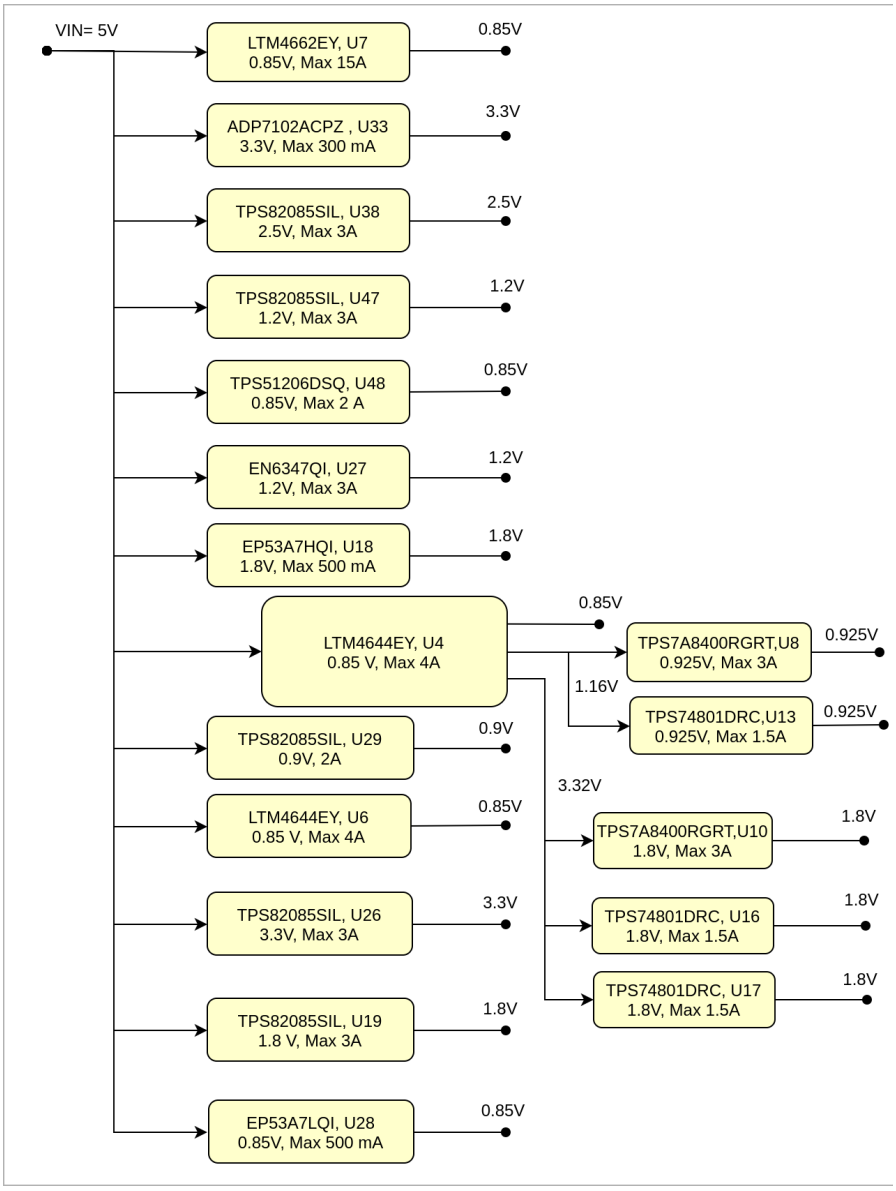

Figure 3: Power Distribution

7.4 Power-On Sequence

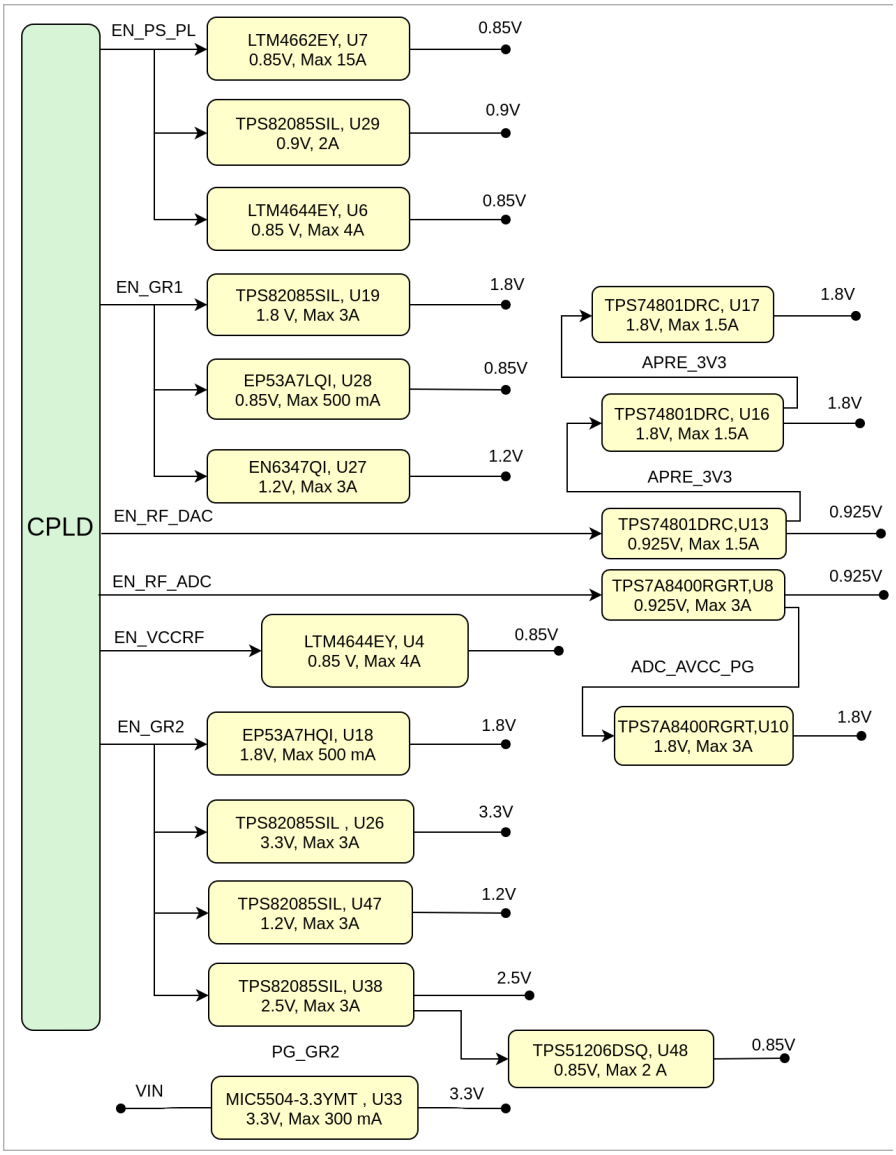

Figure 4: Power Sequency

7.5 Power Rails

Power Rail Name	B2B J1 Pin	B2B J2 Pin	Direction	Notes
VIN	1,2,3,4,5,6,8	-	Input	
PSBATT	14	-	Input	
3.3V_CPLD	16	-	Output	

Table 19: Module power rails.

7.6 Bank Voltages

Bank	Schematic Name	Voltage	Notes
Bank 65 HP	VCCO_65	1.8V	
Bank 503 PSCONFIG	VCCO_PSIO3_503	1.8V	
Bank 88 HD	VCCO_88	3.3V	
Bank 128 GTY	MGTAVCC	0.9V	
Bank 129 GTY	MGTAVCC	0.9V	
Bank 500 PSMIO	VCCO_PSIO0_500	1.8V	
Bank 501 PSMIO	VCCO_PSIO0_501	1.8V	
Bank 502	VCCO_PSIO0_502	1.8V	
Bank 504 PSDDR	VCCO_PSDDR_504	1.2V	
Bank 505 PSGTR	PS_MGTRAVCC	0.85V	

Table 20: Zynq SoC bank voltages.

8 Board to Board Connectors

Unable to render include or excerpt-include. Could not retrieve page.

9 Technical Specifications

9.1 Absolute Maximum Ratings

Symbols	Description	Min	Max	Unit
VIN	Input Supply Voltage	0	5	V
T_STG	Storage Temperature	-40	95	°C

Table 21: PS absolute maximum ratings

9.2 Recommended Operating Conditions

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

Parameter	Min	Max	Units	Reference Document
VIN	4.5	5.5	V	See Schematic
T_OPR	-40	85	°C	See USB2.0 Datasheet

Table 22: Recommended operating conditions.

9.3 Physical Dimensions

- Module size: 90 mm × 65 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 7 mm.

PCB thickness: 1.65 mm.

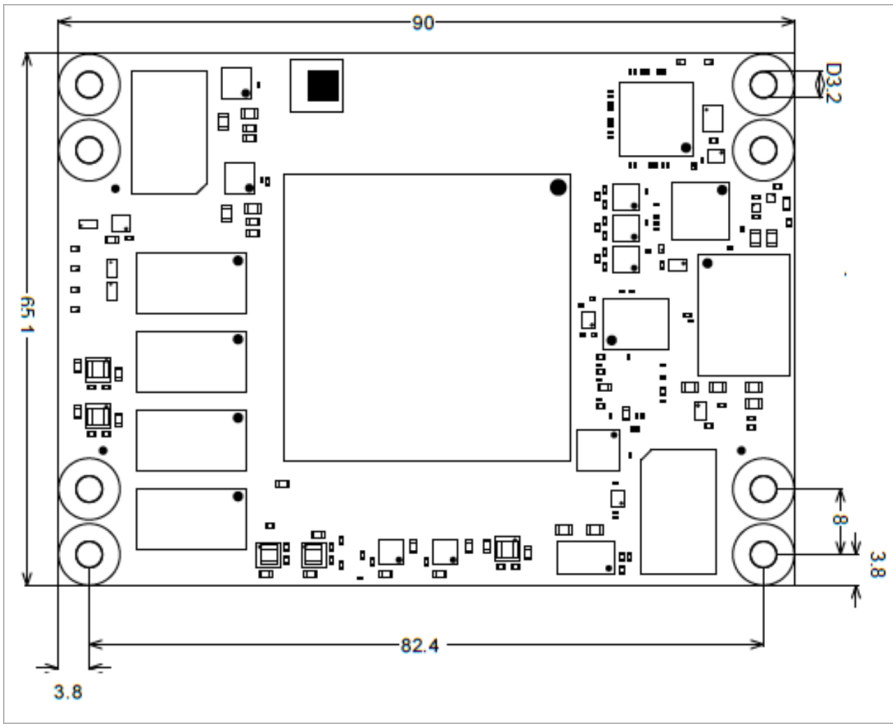

Figure 5: Physical Dimension

10 Currently Offered Variants

Trenz shop TE0835 overview page	
English page[2]	German page[3]

Table 23: Trenz Electronic Shop Overview

2 https://shop.trenz-electronic.de/en/search?sSearch=TE0835
3 https://shop.trenz-electronic.de/de/search?sSearch=TE0835

11 Revision History

11.1 Hardware Revision History

Date	Revision	Changes	Documentation Link
2019-11-05	REV01	Initial Release	REV01[4]

4 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/6.5x9/TE0835/REV01

Date	Revision	Changes	Documentation Link
2020-06-17	REV02	1. Added a VRP resistor on bank 65; 2. LDO U33 is changed on ADP7102ACPZ; 3. Signal FPGA IO0 is connected on AE18 pin of FPGA; 4. Signal DBG_LED3 is connected on AD18 pin of FPGA; 5. Signal MIO13_25 connected to J1 pin 33 instead MIO25. 6. Resistor R84 is removed; 7. LED D1 moved on edge of PCB; 8. Added THT testpoints J4 on CPLD_JTAGEN, R76 was removed; 9. Signals B49_XX_X are renamed in B88_XX_X; 10. C241 is changed on 1nF; 11. Length of CLK signals on RFADC and RFDAC are adjusted; 12. Wrong connection on U8 is fixed (PCB); 13. Wrong connection PGOOD1 pin of U7 is fixed;	REV02[5]

5 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/6.5x9/TE0835/REV02

Date	Revision	Changes	Documentation Link
		14. R17 is changed from 35,5K to 33K for VCC_PL_PS correction.	

Table 24: Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

Figure 6: Board hardware revision number.

11.2 Document Change History

Date	Revision	Contributor	Description
2022-02-17	v.59(see page 6)	John Hartfiel[6]	• Bugfix Overview Picture
2021-12-21	v.58	John Hartfiel	• Bugfix B2B section • Replace GTH with GTY
2021-05-28	v.55	John Hartfiel	• Style update • Bugfix PDF Link • Key features update
2020-11-23	v.51	Pedram Babakhani	• Update to REV02

6 https://wiki.trenz-electronic.de/display/~j.hartfiel

Date	Revision	Contributor	Description
--	all	Pedram Babakhani[7] , John Hartfiel[8] , Martin Rohrmüller[9]	• --

Table 25: Document change history.

7 https://wiki.trenz-electronic.de/display/~P.Babakhani
8 https://wiki.trenz-electronic.de/display/~j.hartfiel
9 https://wiki.trenz-electronic.de/display/~m.rohrmueller

12 Disclaimer

12.1 Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

12.2 Document Warranty

The material contained in this document is provided “as is” and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

12.3 Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

12.4 Copyright Notice

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Trenz Electronic.

12.5 Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used /modified / copied only in accordance with the terms of such license.

12.6 Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

12.7 REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH[10]. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List[11] are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA)[12].

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

10 http://guidance.echa.europa.eu/
11 https://echa.europa.eu/candidate-list-table
12 http://www.echa.europa.eu/

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

2019-06-07