


Regarding the usage of our schematics and alike documentation for Trenz module TE0835 .


Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0835 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

	Title: Legal Notices Modules		
	A4	Number: TE0835 MXE81-A	Rev. 03
	Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 1 of 39
	Filename: Legal Notices Modules.SchDoc		

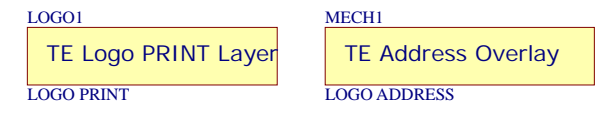
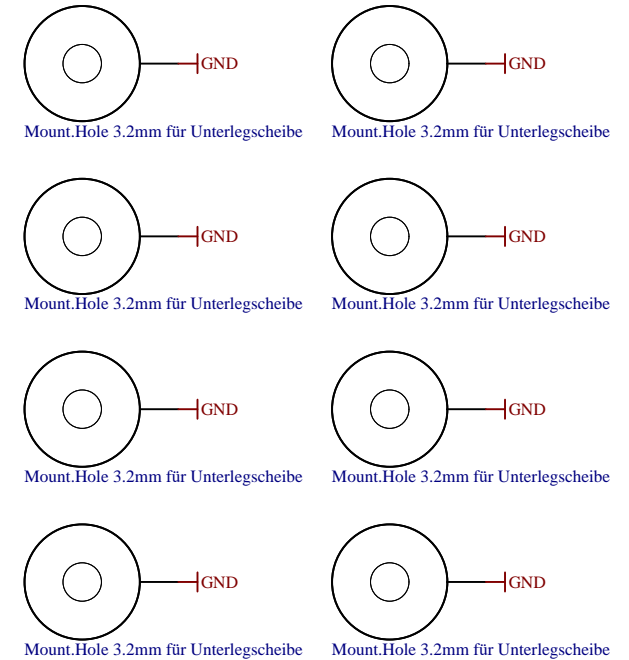
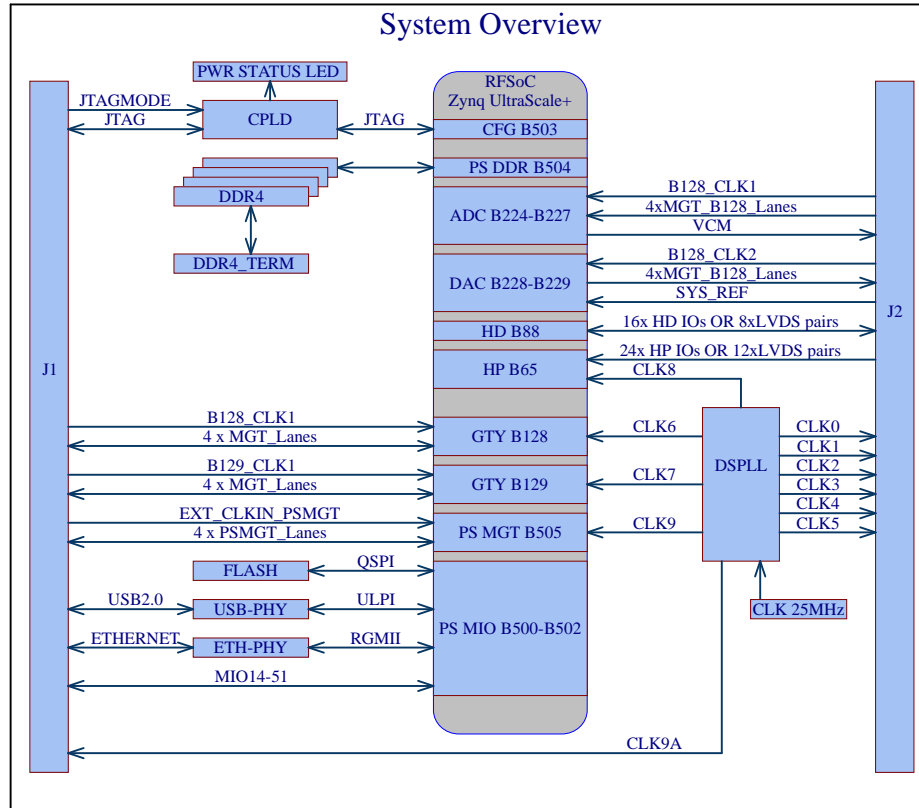
REVISION HISTORY

REV	Description	
-01	Initial revision	IG
-02	<ol style="list-style-type: none"> Added a VRP resistor on bank 65; LDO U33 is changed on ADP7102ACPZ; Signal FPGA IO0 is connected on AE18 pin of FPGA; Signal DBG_LED3 is connected on AD18 pin of FPGA; Signal MIO13_25 connected to J1 pin 33 instead MIO25. Resistor R84 is removed; LED D1 moved on edge of PCB; Added THT testpoints J4 on CPLD_JTAGEN, R76 was removed; Signals B49_XX_X are renamed in B88_XX_X; C241 is changed on 1nF; Length of CLK signals on RFADC and RFDAC are adjusted; Wrong connection on U8 is fixed (PCB); Wrong connection PGOOD1 pin of U7 is fixed; R17 is changed from 35,5K to 33K for VCC_PL_PS correction. 	IG
-02	<ol style="list-style-type: none"> APRE_3V3 renamed to APRE_4V5, voltage of the power rail increased from 3.3V to 4,58V. Resistor R15 is changed from 13,3K to 9,09K. AN: 24671->25969 Capacitor C27 is changed from 100uF x 4V to 47uF x 6,3V. AN: 28940->24718 	IG
-03	<ol style="list-style-type: none"> Added Legal Notices. Added Power Diagram. Added a DC-DCs synchronization circuit to spread spectrum. Changed the core power supply schematic to 4 phases to increase current and reduce noise. The power supply circuit of the module supports input voltage 5...12V. EOL components are replaced: <ol style="list-style-type: none"> L10, L12, L13, L14, L16 Ferrit beads BKP0603HS121-T replaced with MPZ0603S121HT000. Updated layerstack to enhance power supply circuits and improve signal impedance matching. Added POR_OVERRIDE configuration. U25 (Pin 33) PS_SRST_B signal was removed. POR_OVERRIDE_N connected. Added transistor T2A. C180 is removed from schematic. Networks to power the banks have been renamed. Added Level shifter U19. LEDs renamed: D1 --> LED0; D2 --> LED1; D3 --> LED2; D4 --> LED3 and connected to V_3V3_IO. Resistors R77A, R77B, R77C, R77D (39 R) replaced with R77, R130, R132, R134 (1K) respectively according to new schematic. Added pull-up resistors R157, R158, R159, R161, R162, R163 to synchronise the power supplies. Added resistors R142-R145. U23 connected to V_3V3_IO (was 1.8V). ZU_PWR: L9 removed from schematic. Added resistors R46, R90, R98, R146, R149. Added U44. U33 (ADP7102ACPZ) replaced with MIC5504-3.3YMT. Added two capacitors 4.7uF C355 and C488 on DDR_VTT. Added signal SEL_2V5_DAC to Bank 65HP. Pin AD16. Capacitors C24, C32, C97, C130-136, 150-152, 155, 190,191, C203, C204, C214, C216 are replaced with 100 nF. Y1 CX3225SB54000 is EOL, it is replaced with ECS-540-8-33-JTN-TR Added a VIN voltage sensor R121, R124, R150, R122, R153, C489. Added R154, R155 to implement I2C interface between SC and RFSoc. Clock CLK0A_100MHz renamed to PLL_CLKOUT 	IG 27.03.2024

		Title: Revision_Changes	
		A4	Number: TE0835 MXE81-A
Date: 2023-10-26		Copyright: Trenz Electronic GmbH	
Date: 2023-10-26		Page 2 of 39	
Filename: Revision_Changes.SchDoc			

Special notes:

- U_PWR-DIAGRAM
- U_FPGA-PWR
- U_FPGA-PWR_RF
- U_FPGA-GND
- POWER_STDBY_BIAS
- POWER_VCCINT_PH1
- POWER_VCCINT_PH2
- POWER_VCCINT_PH3
- POWER_VCCINT_PH4
- POWER_IV2
- POWER_IO_1V8
- POWER_IO_3V3
- POWER_MGT
- POWER_RF
- POWER_RF_1V8
- POWER_DDR



S/N
Serial
Serialnumber 6,3 x 6.3mm

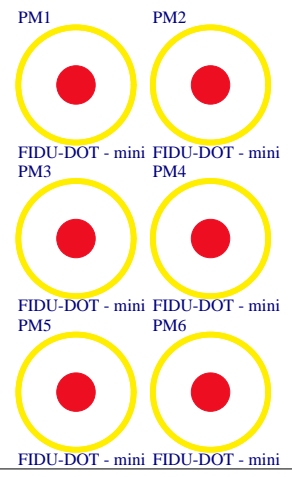


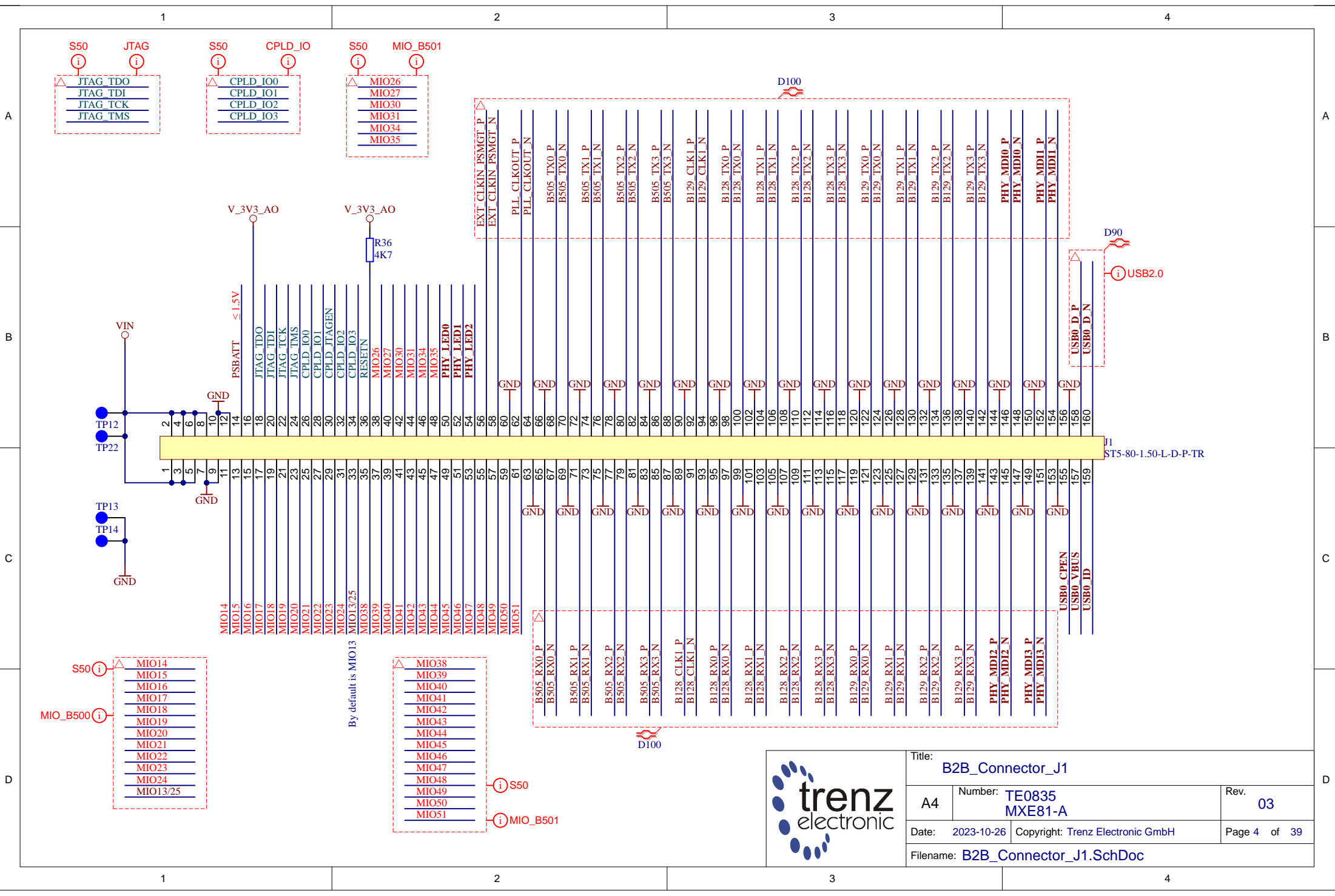
Table of I2C devices and addresses

Designator	I2C Address	Description
U23	0x50	I2C MAC EEPROM
U27	0x60	Security Chip
U15	0x69	DSPLL

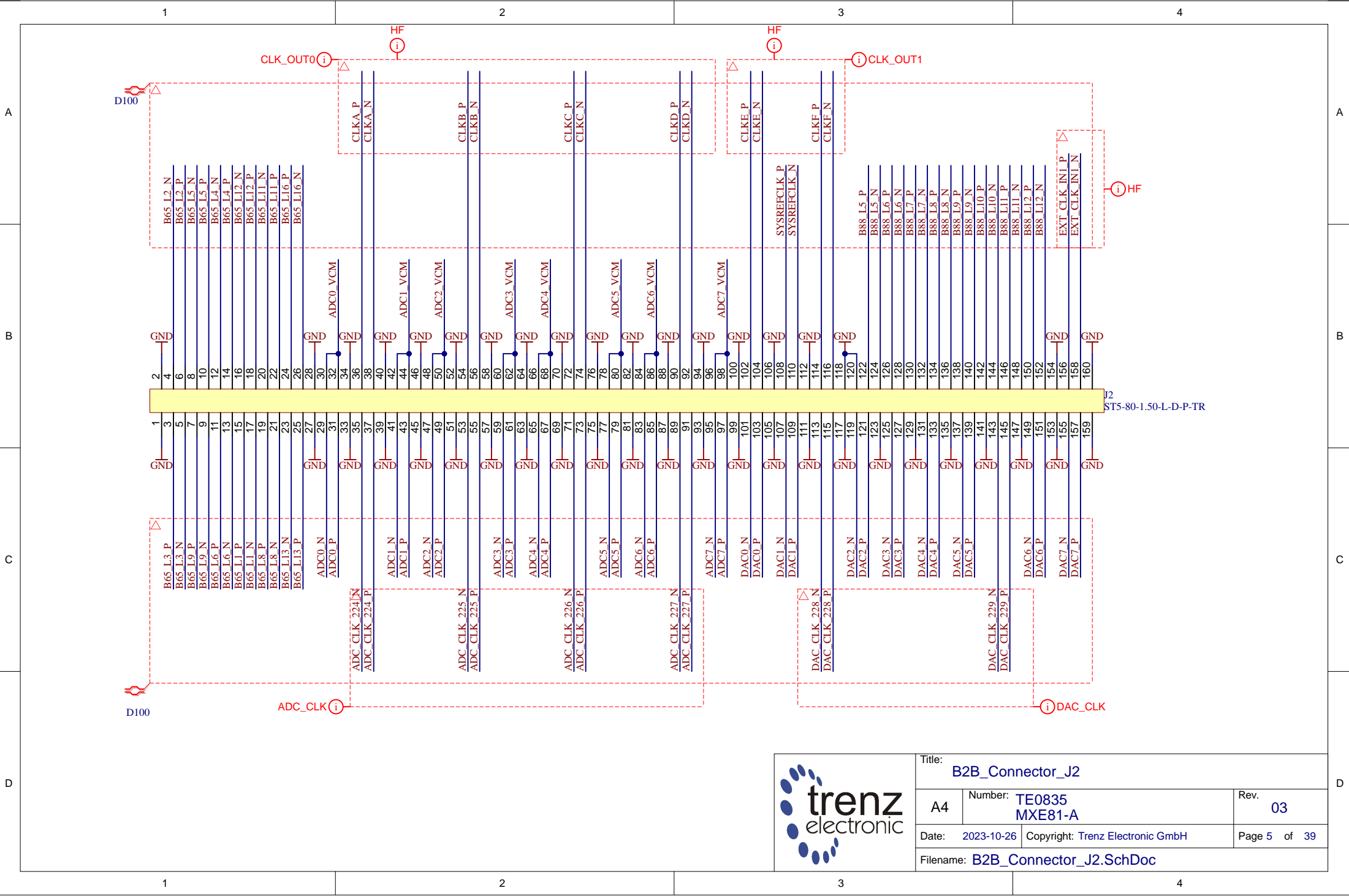
Design drawn by: IG
 Checked by: MR
 Assembly variant: MXE81-A
 Created by: IG
 Modified by: IG
 Modified at: 2024-02-19



Title: TE0835		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 3 of 39
Filename: TE0835-Overview.SchDoc		

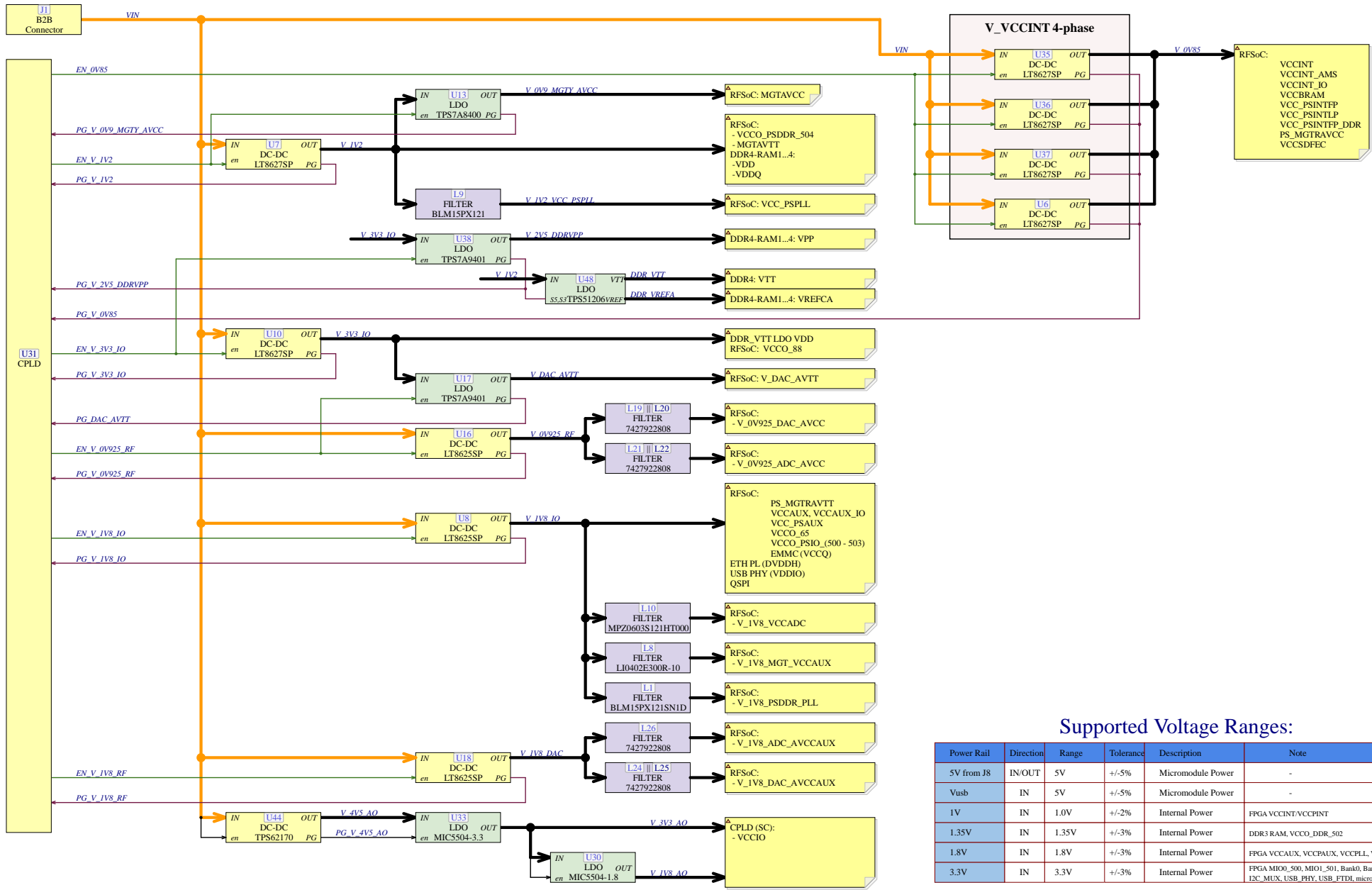


Title: B2B_Connector_J1		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	
Filename: B2B_Connector_J1.SchDoc		Page 4 of 39



Title: B2B_Connector_J2		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	
Filename: B2B_Connector_J2.SchDoc		Page 5 of 39

Power-on sequencing:



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
5V from J8	IN/OUT	5V	+/-5%	Micromodule Power	-
Vusb	IN	5V	+/-5%	Micromodule Power	-
1V	IN	1.0V	+/-2%	Internal Power	FPGA VCCINT/VCCPINT
1.35V	IN	1.35V	+/-3%	Internal Power	DDR3 RAM, VCCO_DDR_502
1.8V	IN	1.8V	+/-3%	Internal Power	FPGA VCCAUX, VCCPLL, VCCPLL, VCCBATT, AVCC, SC
3.3V	IN	3.3V	+/-3%	Internal Power	FPGA MIO0_500, MIO1_501, Bank0, Bank34, Bank35 I2C_MUX, USB, PHY, USB, FTDI, micro SD, USB Hub, SC



Title: **Power_Diagram**

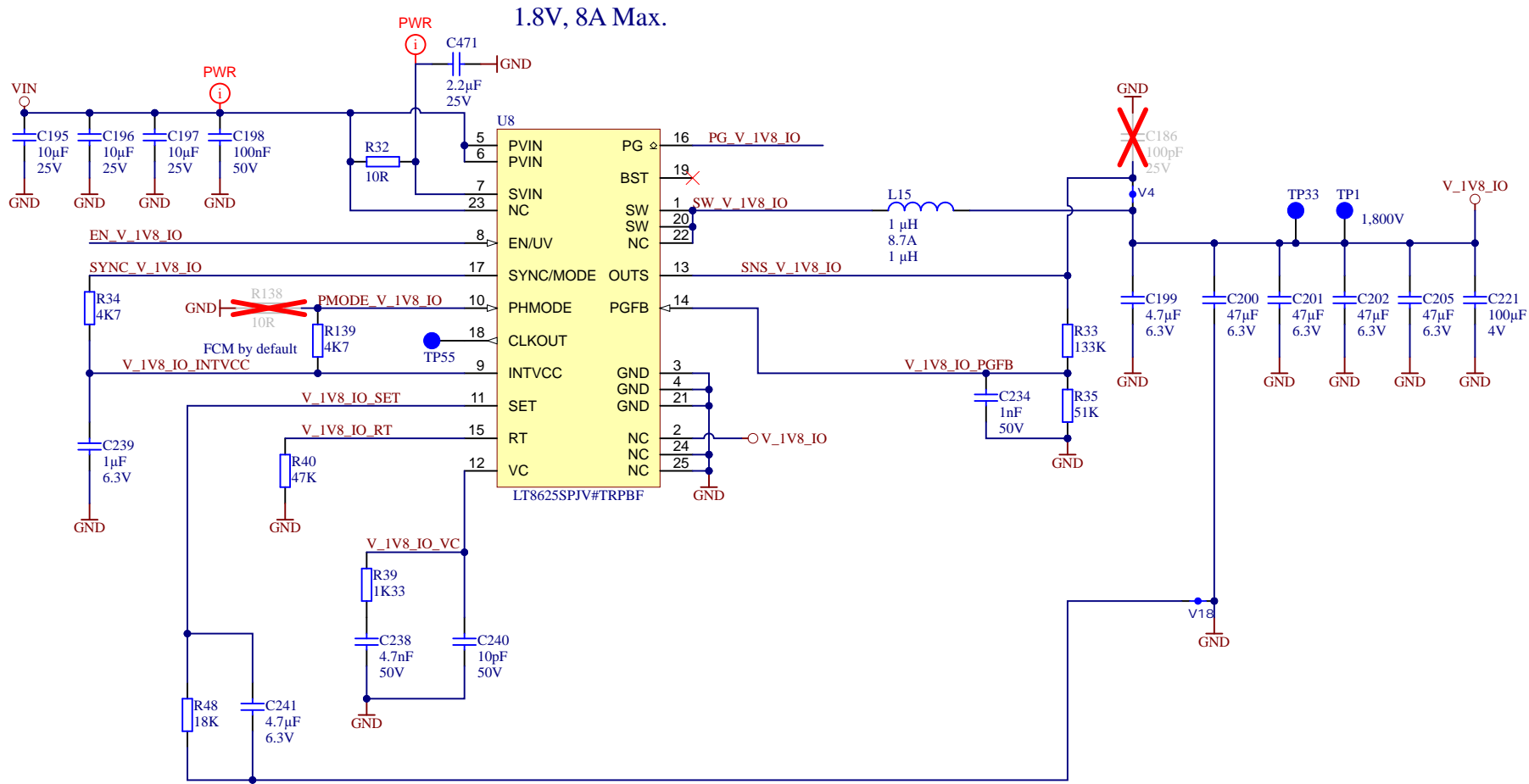
A3	Number: TE0835 MXE81-A	Rev. 03
Datum: 2024-07-16		Page 6 of 39
Filename: Power Diagram.SchDoc		

1

2

3

4



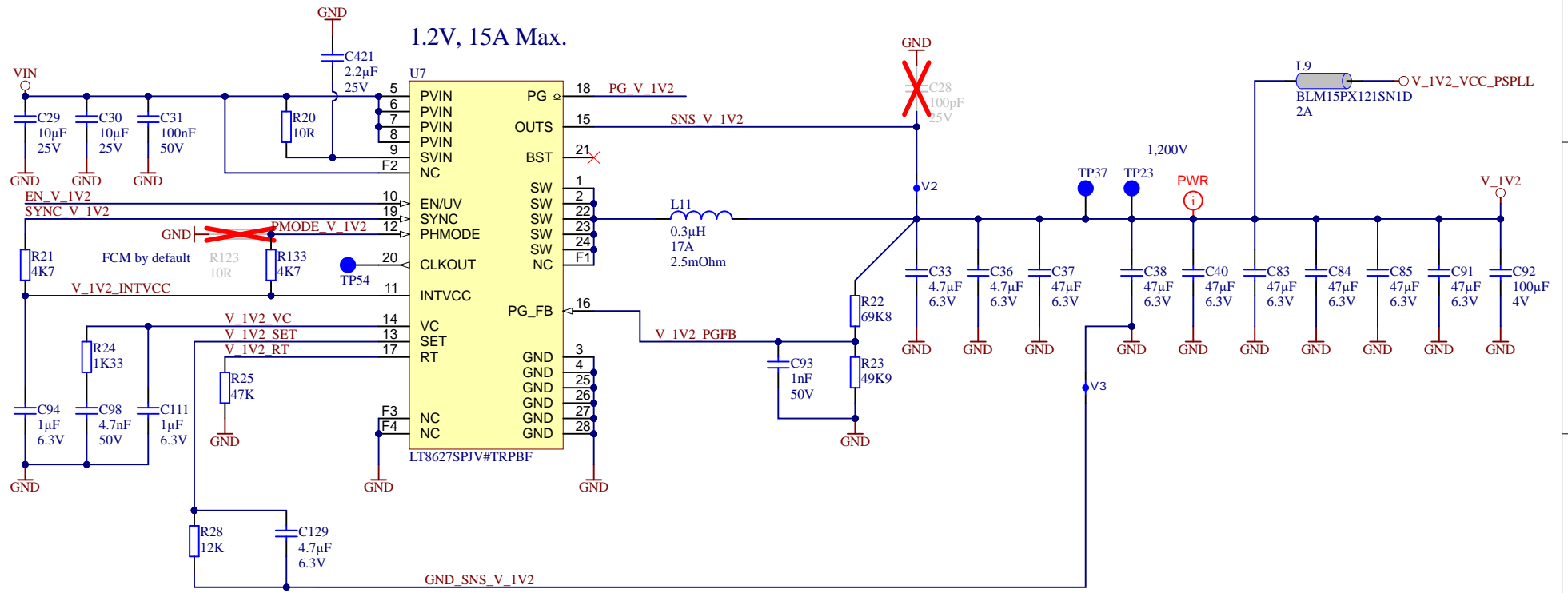
	Title: POWER_IO_1V8		
	A4	Number: TE0835 MXE81-A	Rev. 03
	Date: 2024-07-17	Copyright: Trenz Electronic GmbH	
	Filename: POWER_IO_1V8.SchDoc		Page 7 of 39


1

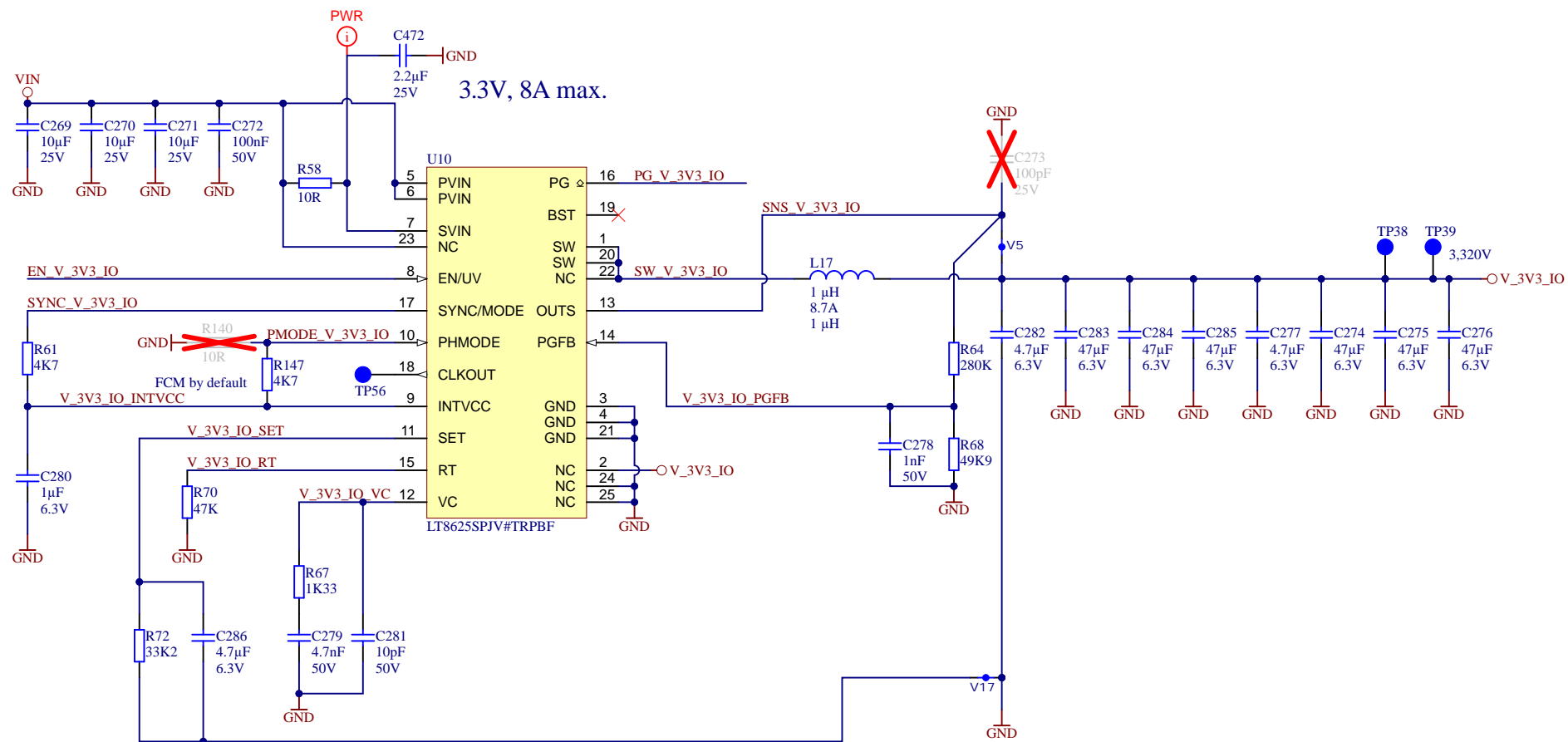
2


3

4

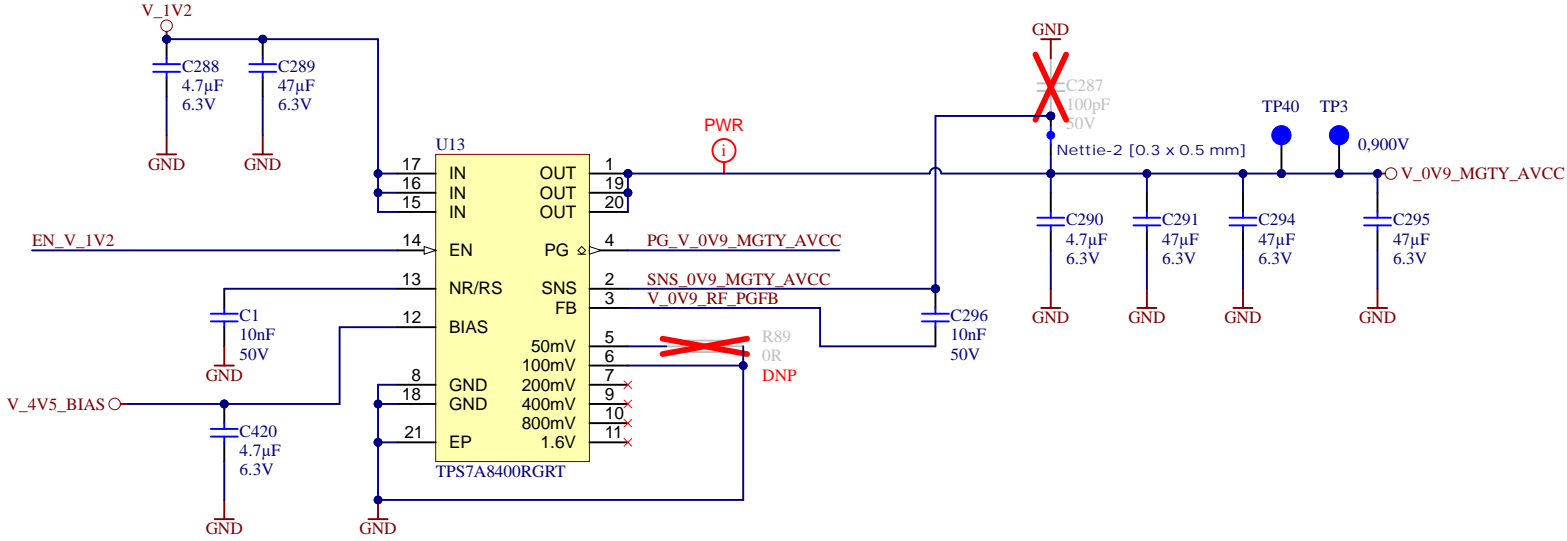



		Title: POWER_1V2	
		A4	Number: TE0835 MXE81-A
Date: 2024-07-17		Copyright: Trenz Electronic GmbH	
Filename: POWER_1V2.SchDoc		Page 8 of 39	



		Title: POWER_IO_3V3	
		A4	Number: TE0835 MXE81-A
Date: 2024-07-17		Copyright: Trenz Electronic GmbH	
Date: 2024-07-17		Page 9 of 39	
Filename: POWER_IO_3V3.SchDoc			

V_0V9_MGTAVCC, 2.5A Max



		Title: POWER_MGT	
		A4	Number: TE0835 MXE81-A
Date: 2024-07-16		Copyright: Trenz Electronic GmbH	
Filename: POWER_MGT.SchDoc		Page 10 of 39	

V_0V925_DAC_AVCC, (0.12 - 4.6A) + V_0V925_ADC_AVCC, (1.2 - 2.3A) ==> 1.32 - 6.9 A

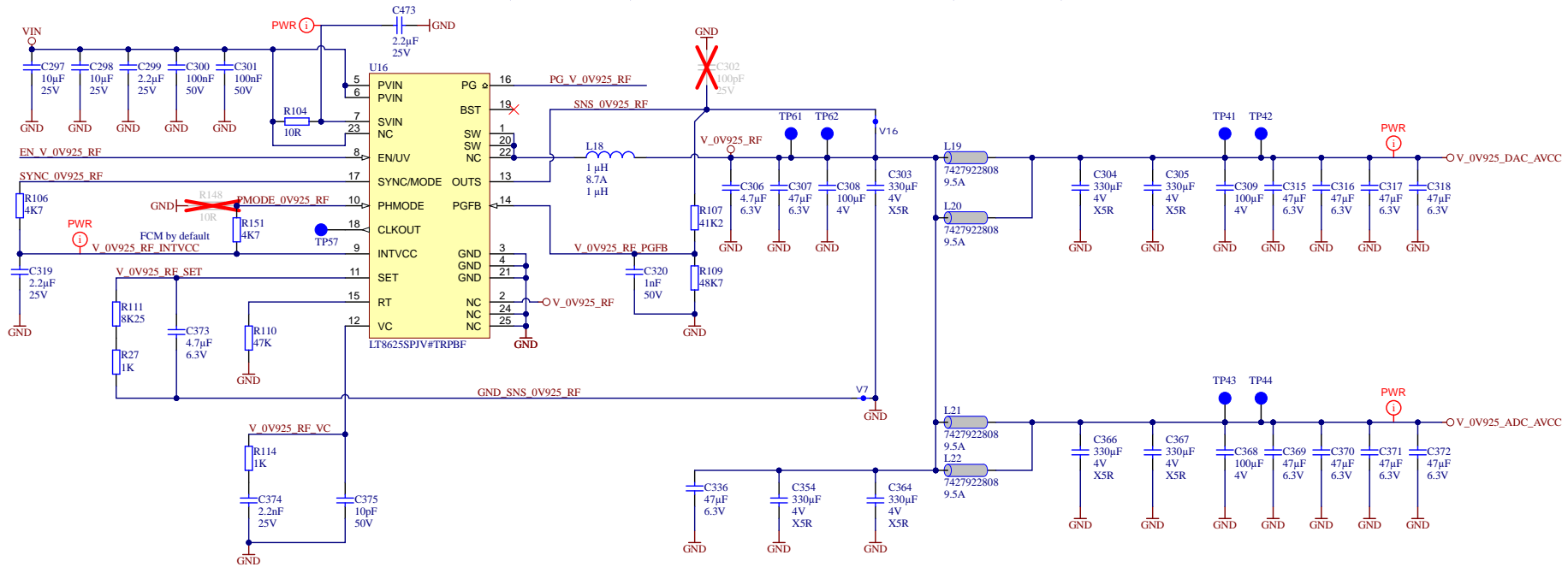
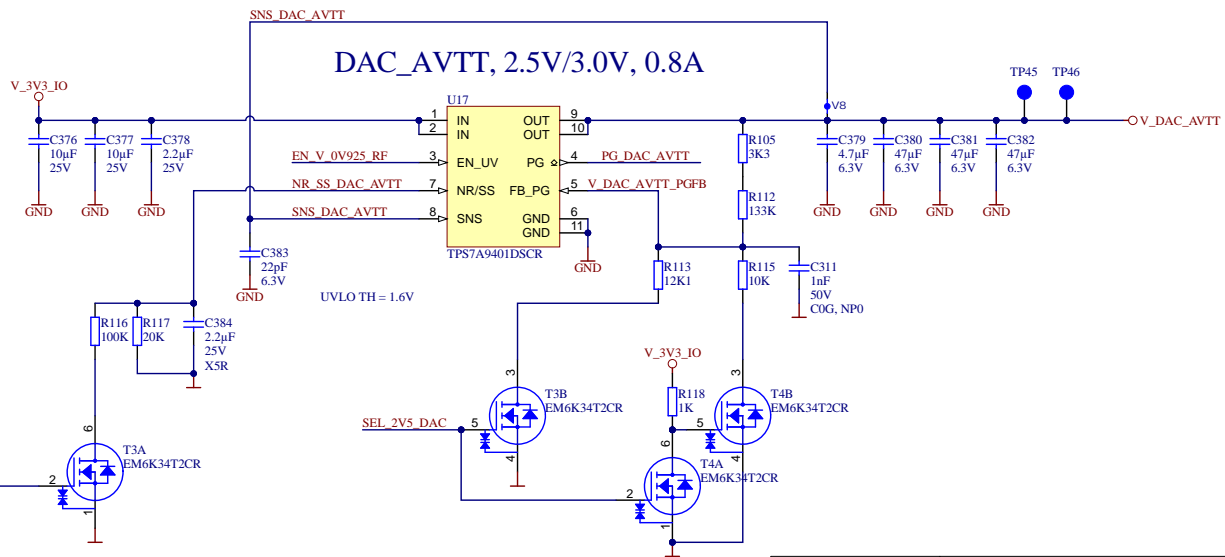


Table 3-22: ADC and DAC Voltage Supply Specifications for Gen 3 Devices⁽¹⁾

Supply	Nominal Voltage (V)	Tolerance (%) ⁽²⁾	Frequency Range (MHz)	Maximum Supply Ripple (mVpp) ⁽³⁾
ADC_AVCC	0.925	±3	0.1-15	0.25
ADC_AVCCAUX	1.8	±3	0.1-15	1.2
DAC_AVCC	0.925	±3	0.1-15	0.32
DAC_AVCCAUX	1.8	±3	0.1-15	1.0
DAC_AVTT	2.5/3.0 ⁽⁴⁾	±3	0.1-15	2.0
VCCINT_AMS	0.85	±3	0.1-15	20.0

- Notes:
- For the maximum current, refer to the *30mV Power Estimator (SPE)* tool.
 - The tolerance percentage is for the switching regulator that feeds the VMS.
 - Output of the VMS.
 - DAC_AVTT should be set to 2.5V if used in 20 mA mode, and 3.0V if used in 32 mA mode in Gen 1 and Gen 2. *30mV* recommends DAC_AVTT be set to 3.0V in Gen 3 to enable the VMS function. Refer to *30mV Estimator - 450C or Data Converter Logic/IC Product Guide (PG289) (Rev 1)* for details and compatibility mode.



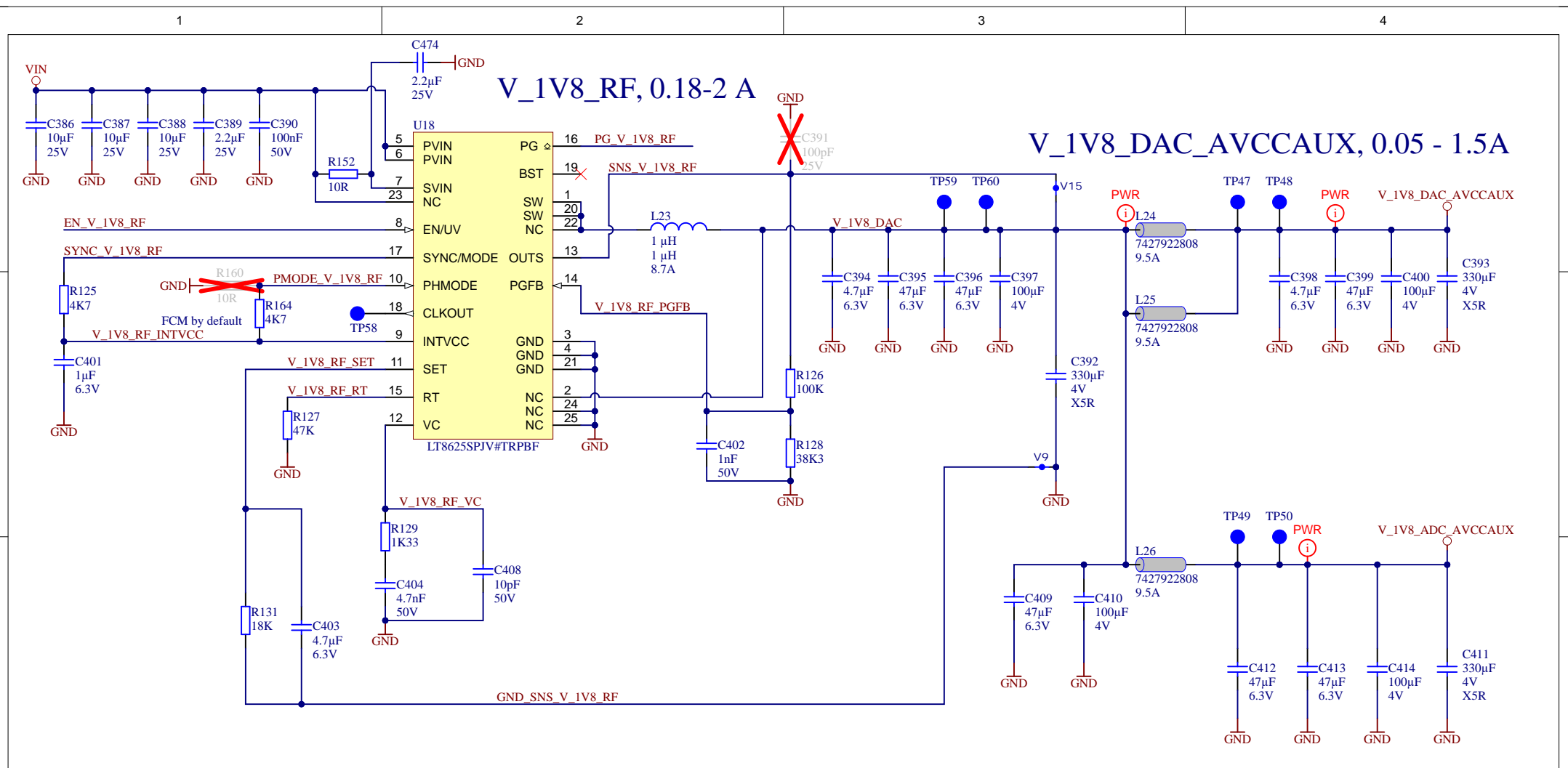
OUTPUT VOLTAGE 2.5V, R_{nr} = 16.5 kOhms (default)
 OUTPUT VOLTAGE 3.0V, R_{nr} = 20.0 kOhms

trenz electronic

Title: POWER_RF

A3	Number: TE0835 MXE81-A	Rev. 03
Datum: 2021-02-01		Copyright: Trenz Electronic GmbH
Page 11 of 39		

Filename: POWER_RF.SchDoc



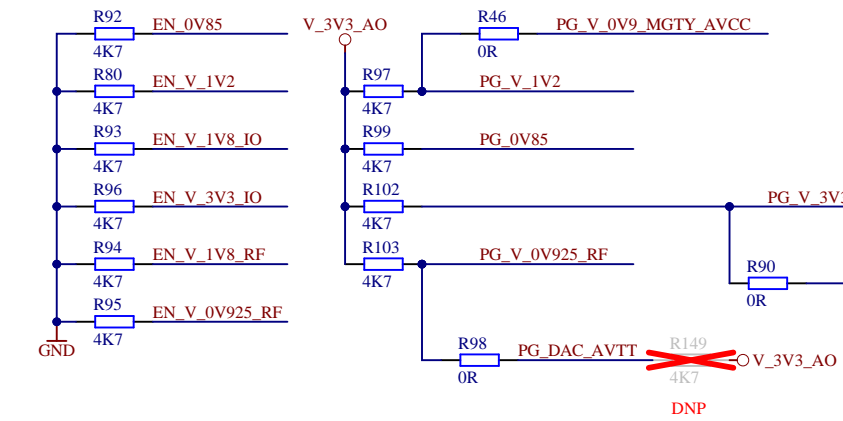
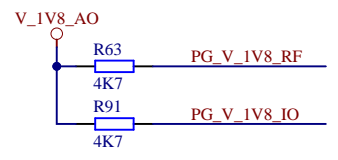
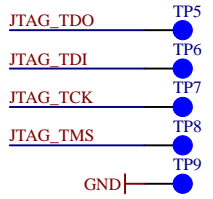
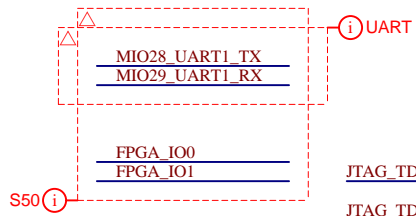
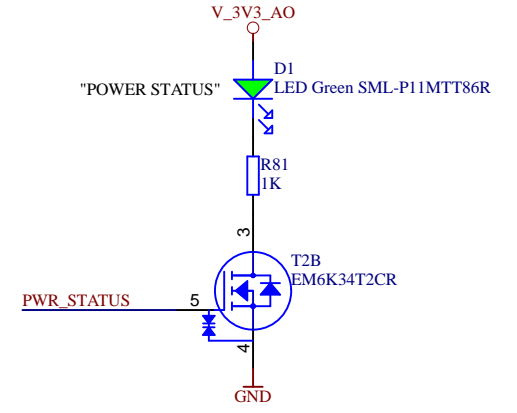
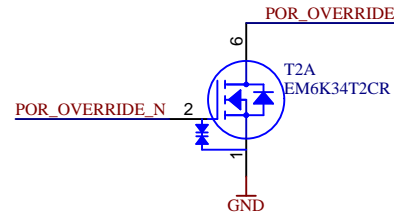
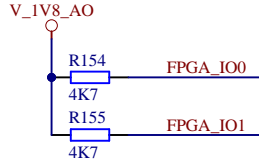
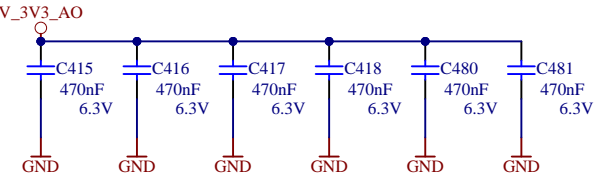
V_1V8_RF, 0.18-2 A

V_1V8_DAC_AVCCAUX, 0.05 - 1.5A

V_1V8_ADC_AVCCAUX, 0.13-0.5A

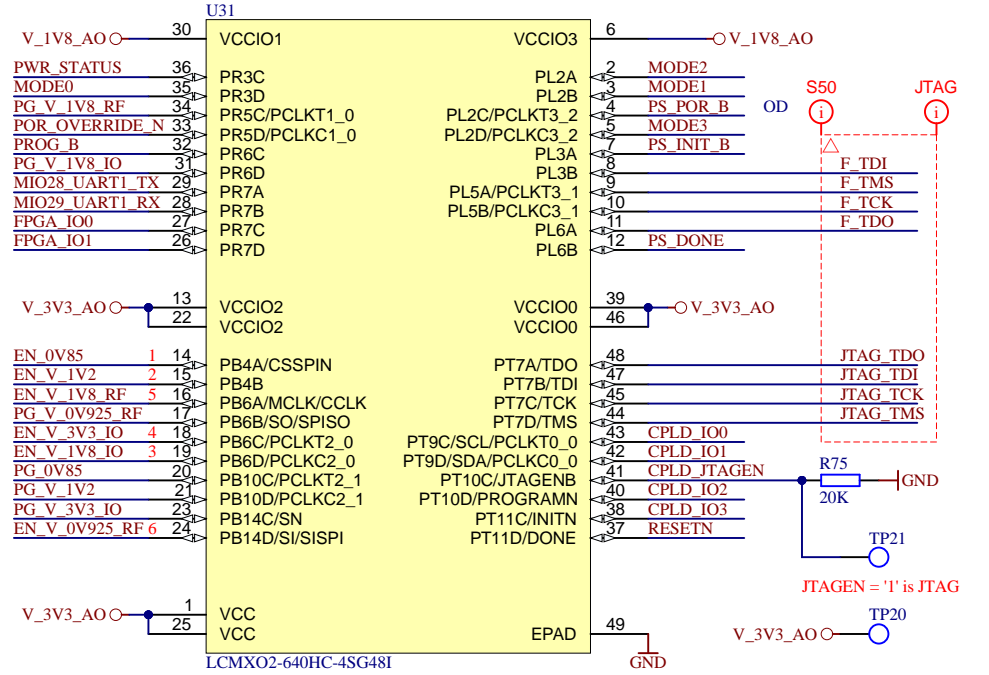
	Title: POWER_RF_1V8	
	A4	Number: TE0835 MXE81-A
	Date: 2024-07-17	Copyright: Trenz Electronic GmbH
	Filename: POWER_RF_1V8.SchDoc	
	Rev. 03	Page 12 of 39

System Controller (SC)

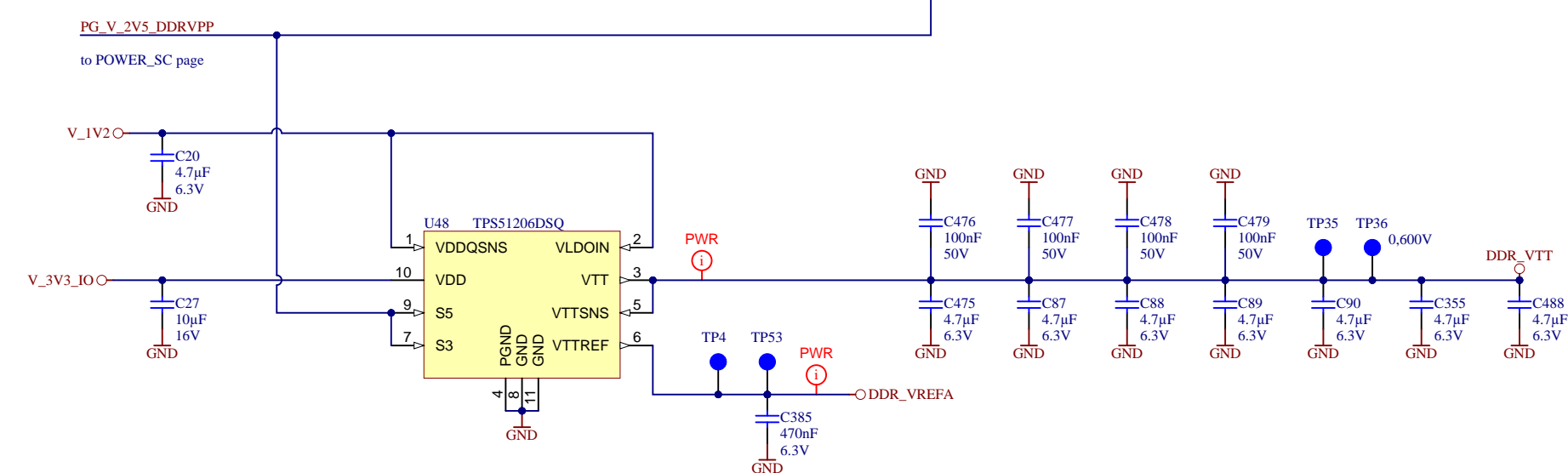
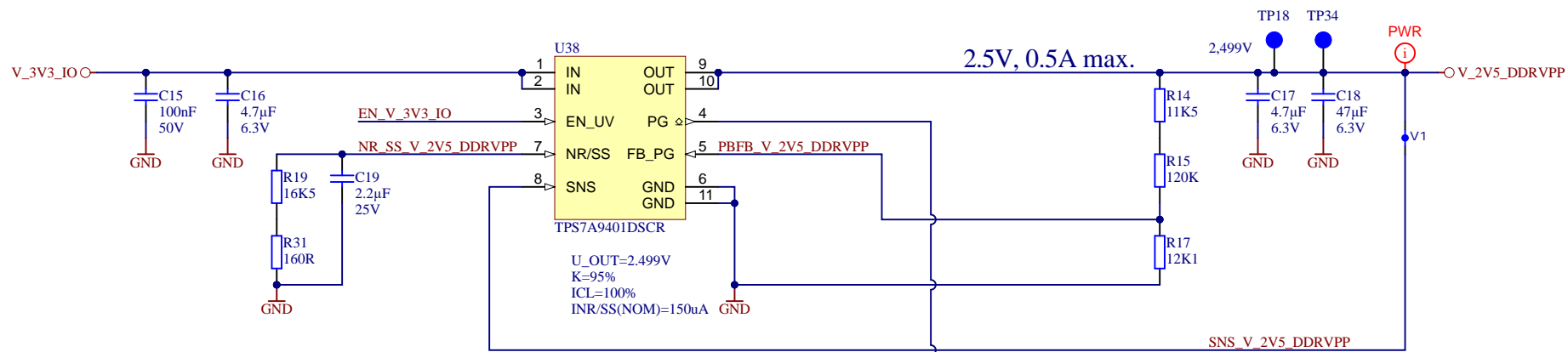



REV02
Net names:
PG_VCCRF
SRST_B
PG_GR2

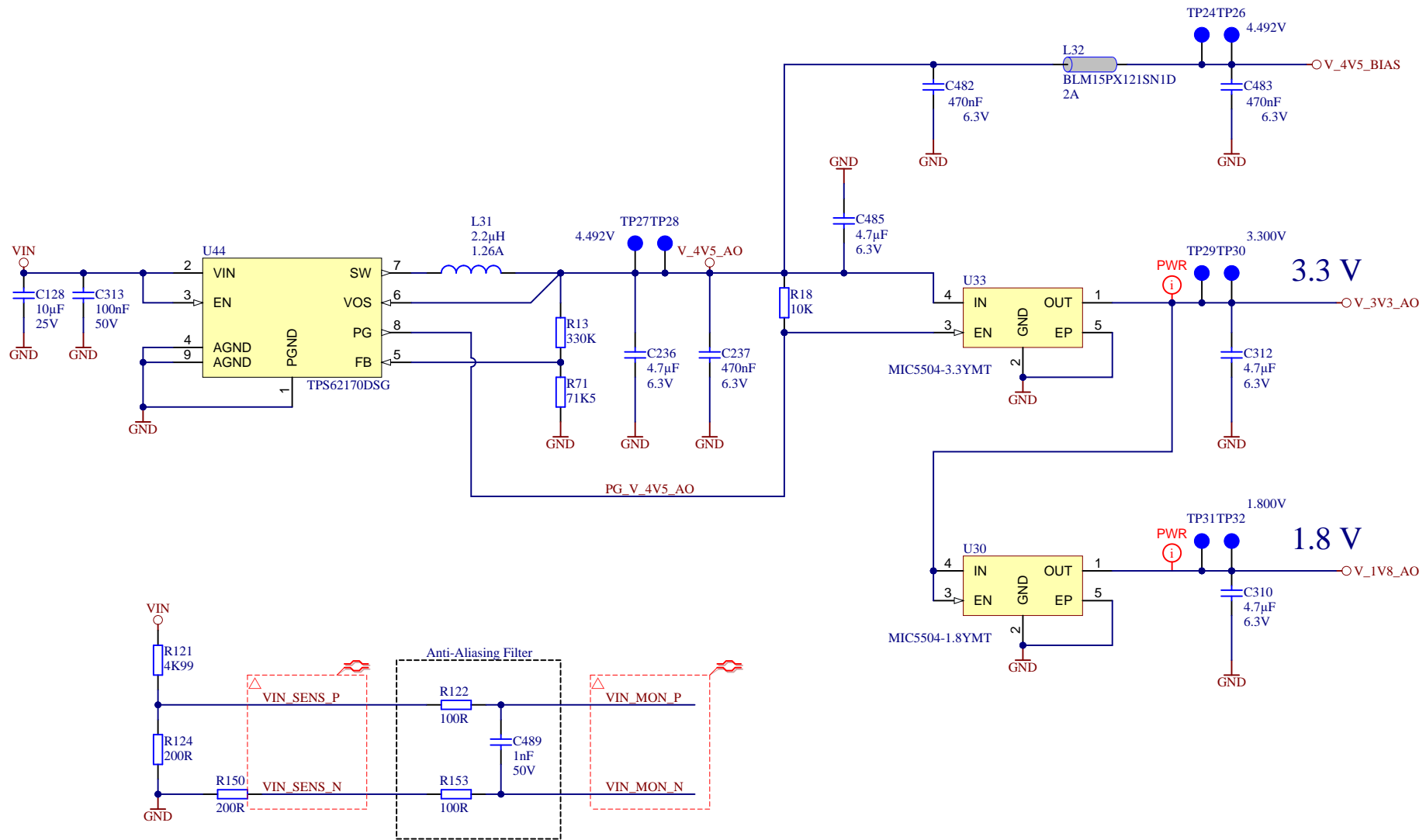
EN_PS_PL
EN_GR1
EN_RF_ADC
PG_RF_DAC
EN_VCCRF
EN_GR2
PG_PS_PL
PG_GR1
PG_RF_ADC
EN_RF_DAC




Title: POWER_SEQ		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2024-07-16	Copyright: Trenz Electronic GmbH	Page 13 of 39
Filename: SC.SchDoc		

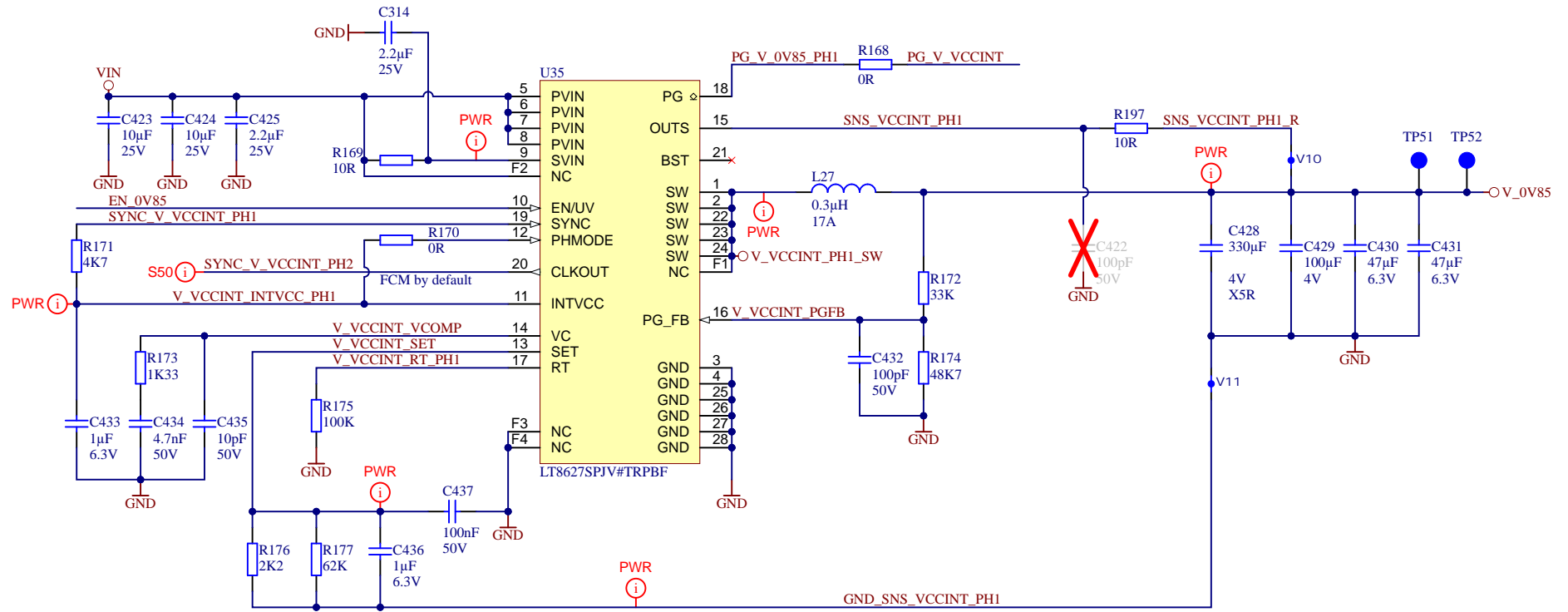



			Title: PWR_DDR	
			A4	Number: TE0835 MXE81-A
Date: 2023-10-26		Copyright: Trenz Electronic GmbH		Page 14 of 39
Filename: POWER_DDR.SchDoc				



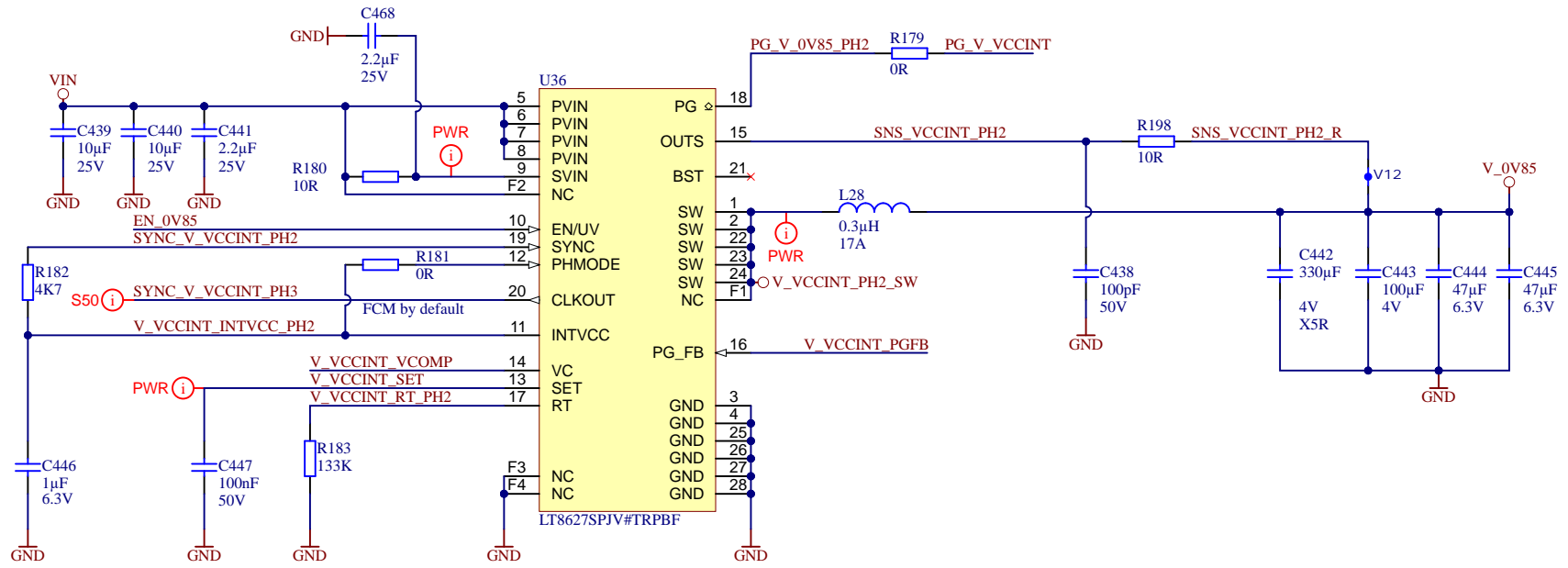
	Title: POWER_STDBY_BIAS		
	A4	Number: TE0835 MXE81-A	Rev. 03
	Date: 2024-07-17	Copyright: Trenz Electronic GmbH	
	Page 15 of 39		
Filename: POWER_STDBY_BIAS.SchDoc			


VCCINT Phase 1/4, 0.85V, 45A, 15A per Phase



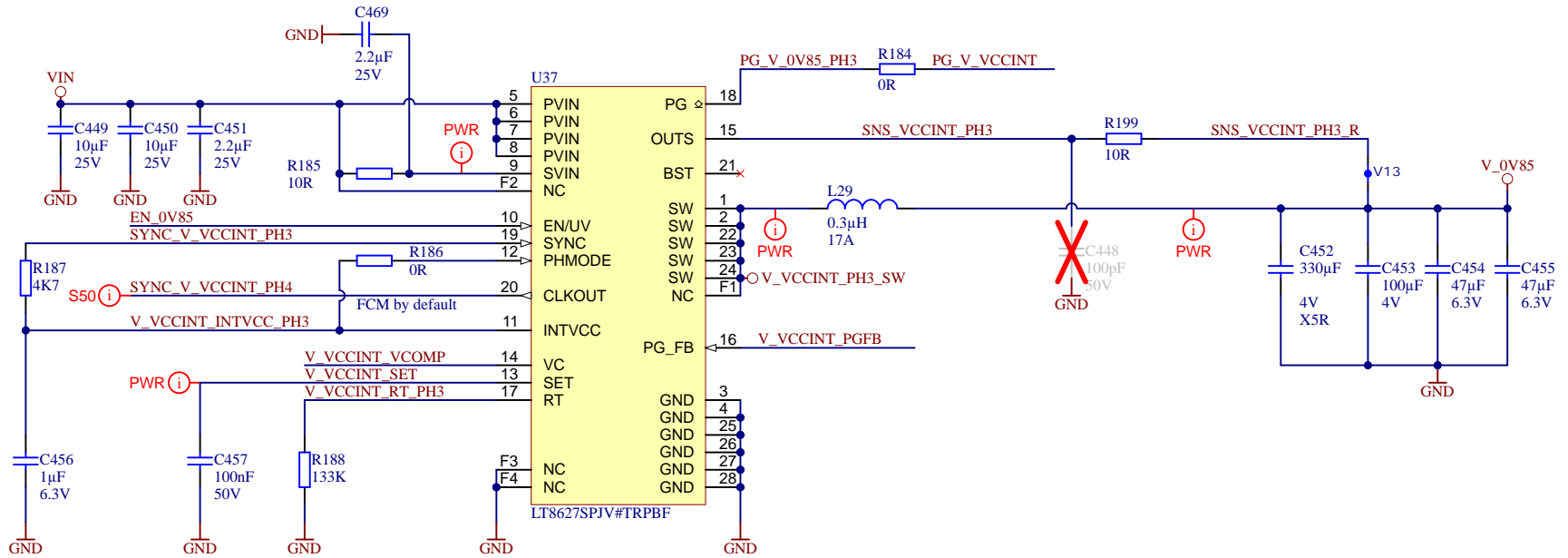
	Title: POWER_VCCINT_PH1		
	A4	Number: TE0835 MXE81-A	Rev. 03
	Date: 2024-07-17	Copyright: Trenz Electronic GmbH	Page 16 of 39
	Filename: POWER_VCCINT_PH1.SchDoc		


VCCINT Phase 2/4, 0.85V, 45A, 15A per Phase



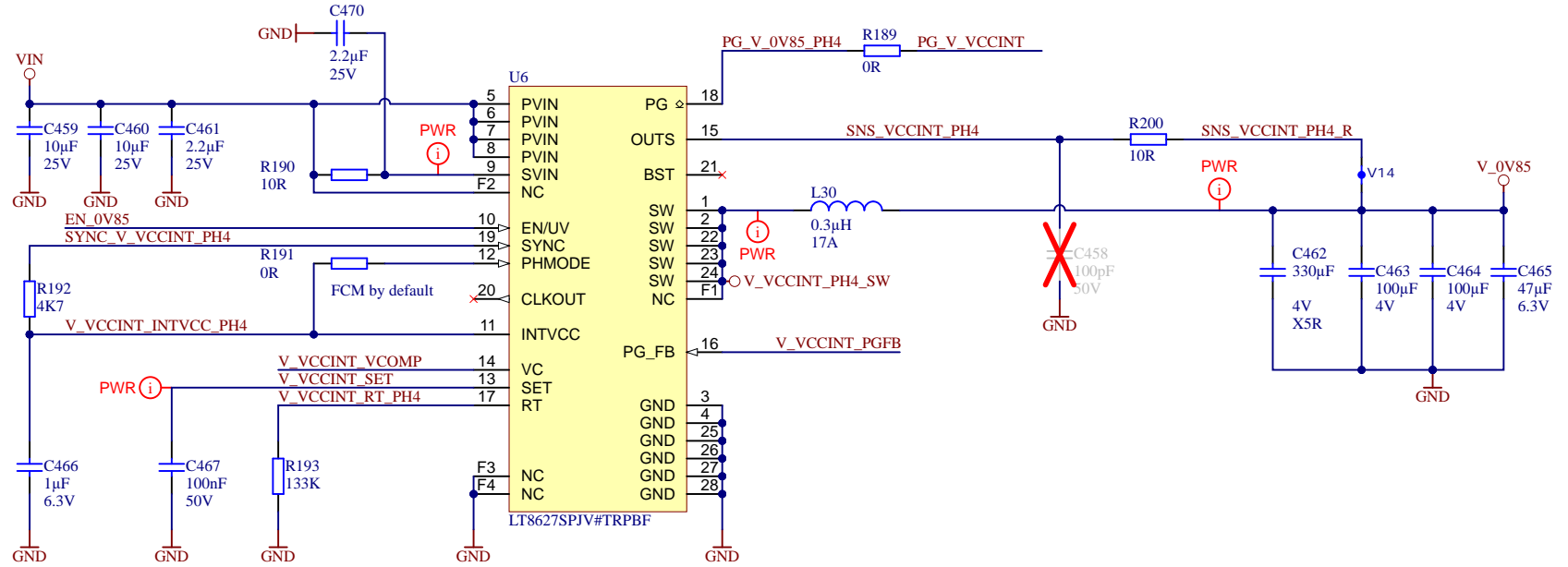
	Title: POWER_VCCINT_PH2		
	A4	Number: TE0835 MXE81-A	Rev. 03
	Date: 2024-07-17	Copyright: Trenz Electronic GmbH	
	Page 17 of 39		
Filename: POWER_VCCINT_PH2.SchDoc			


VCCINT Phase 3/4, 0.85V, 45A, 15A per Phase



			Title: POWER_VCCINT_PH3	
			A4	Number: TE0835 MXE81-A
Date: 2024-07-17		Copyright: Trenz Electronic GmbH		Page 18 of 39
Filename: POWER_VCCINT_PH3.SchDoc				

VCCINT Phase 4/4, 0.85V, 45A, 15A per Phase



			Title: POWER_VCCINT_PH4	
			A4	Number: TE0835 MXE81-A
Date: 2024-07-17		Copyright: Trenz Electronic GmbH		Page 19 of 39
Filename: POWER_VCCINT_PH4.SchDoc				

A

B

C

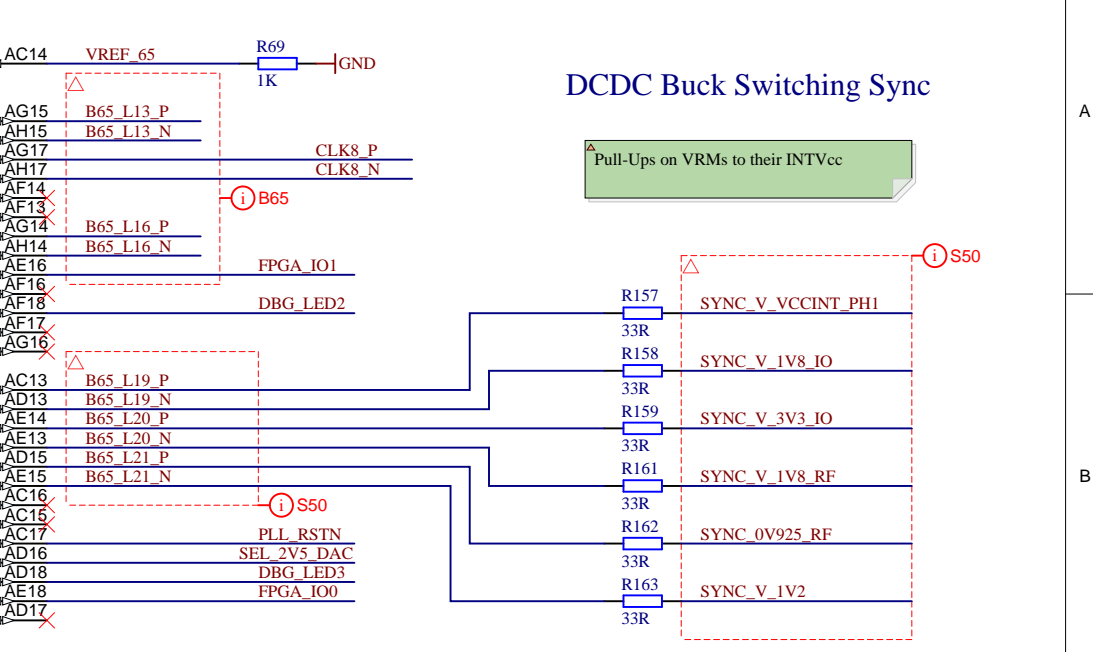
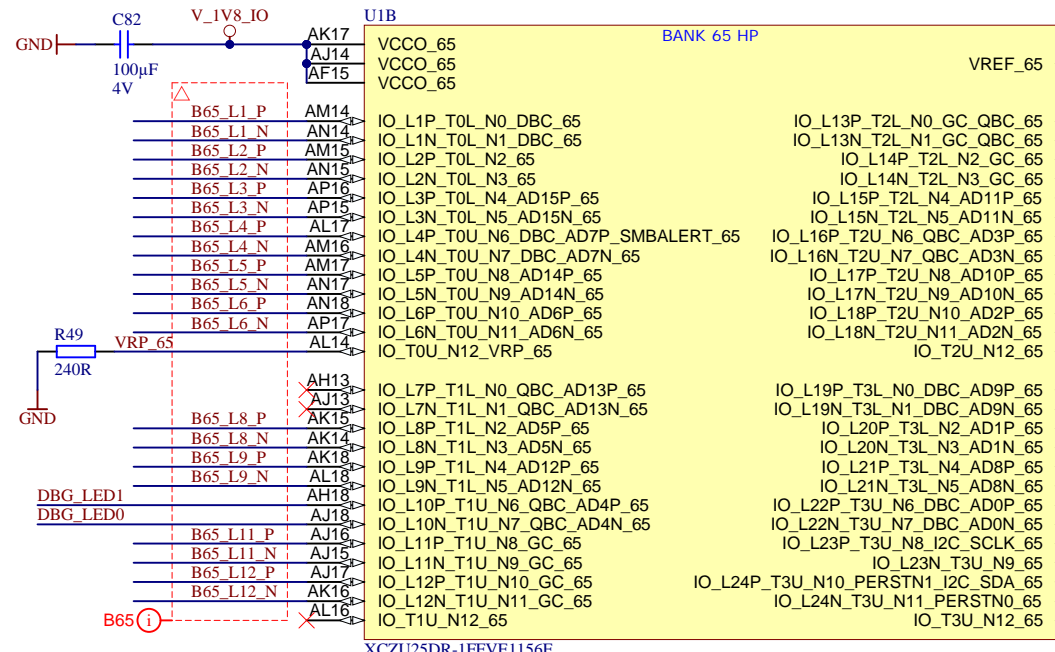
D

A

B

C

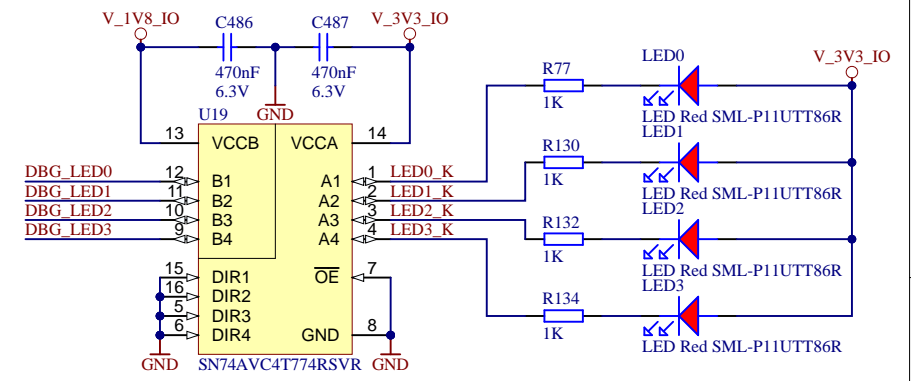
D



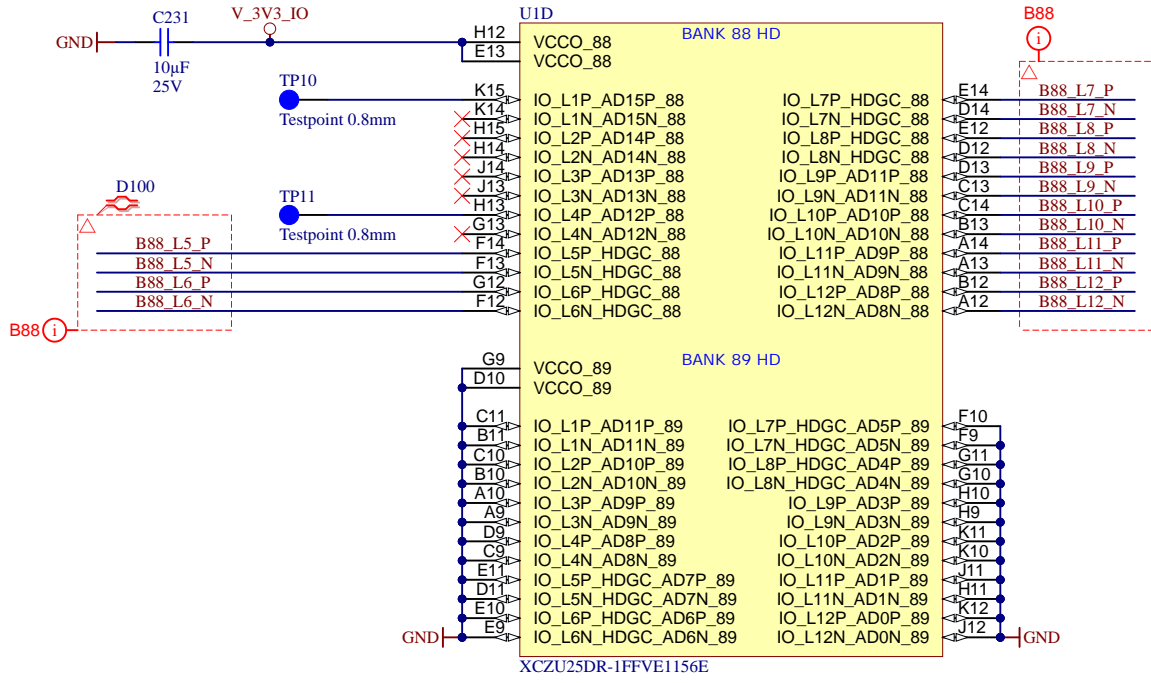
DCDC Buck Switching Sync

Pull-Ups on VRMs to their INTVcc

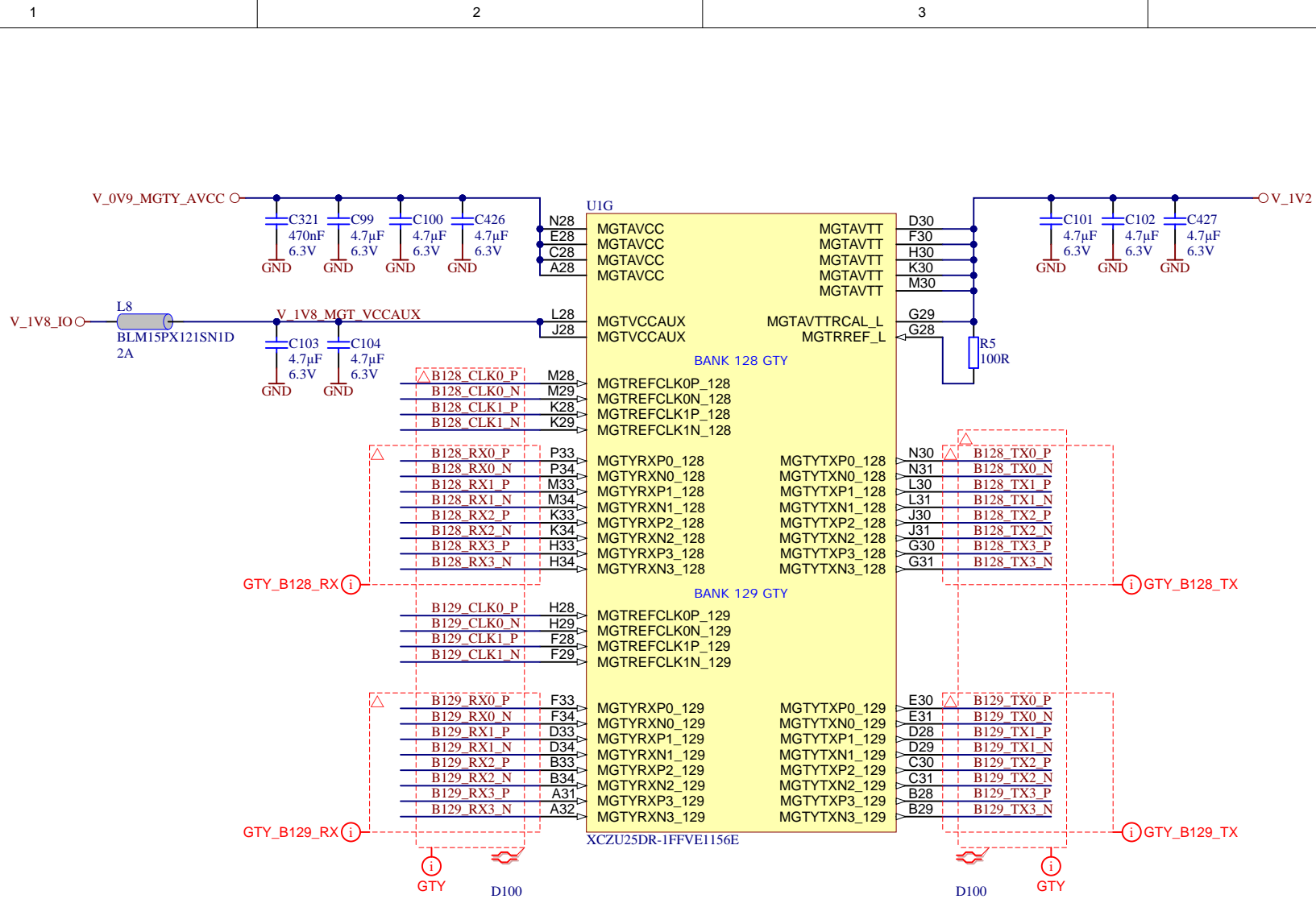
SYNC Threshold	SYNC DC and Clock Low Level Voltage	0.7	1.5	V
	SYNC DC and Clock High Level Voltage			



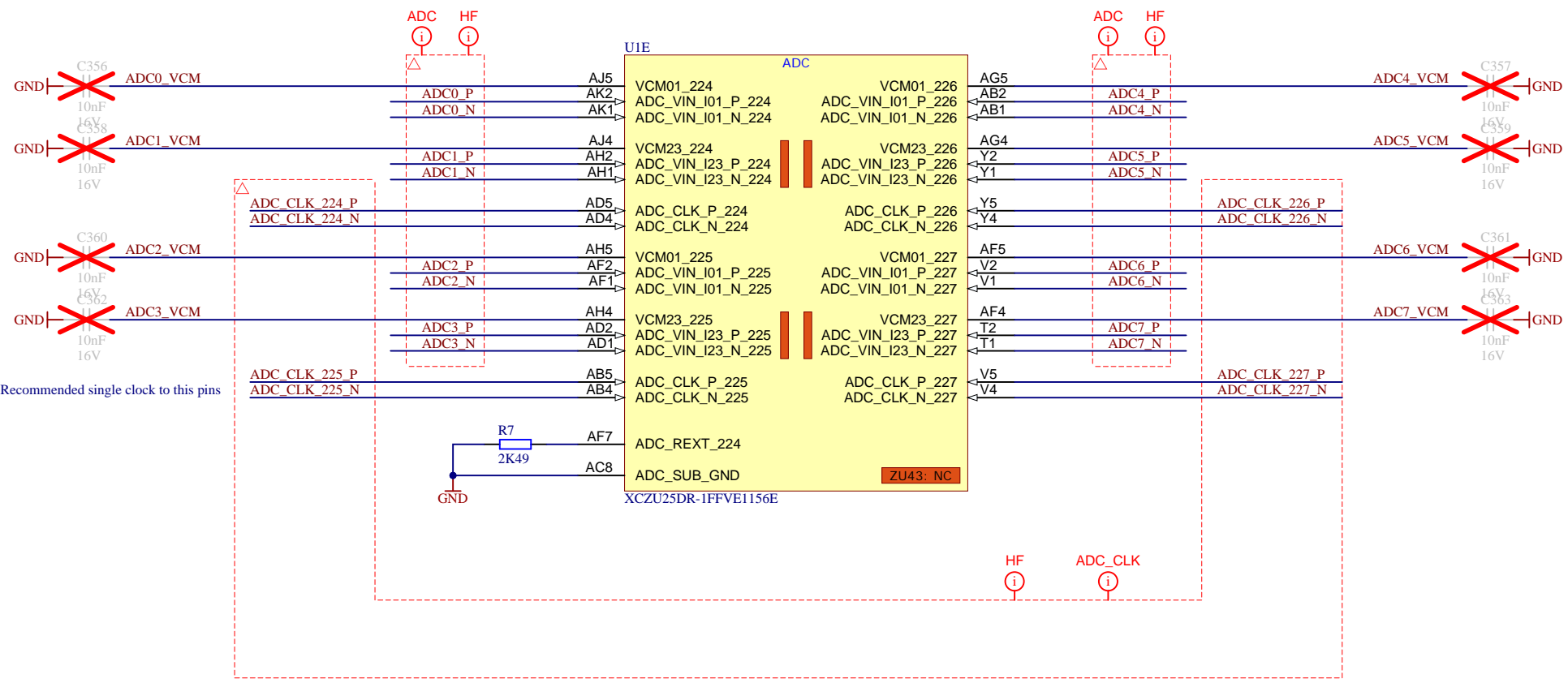
Title: ZU_B65_B66		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 20 of 39
Filename: ZU_HP_B65_B66.SchDoc		




Title: ZU_HD		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	
Page 21 of 39		Filename: ZU_HD_B88_B89.SchDoc

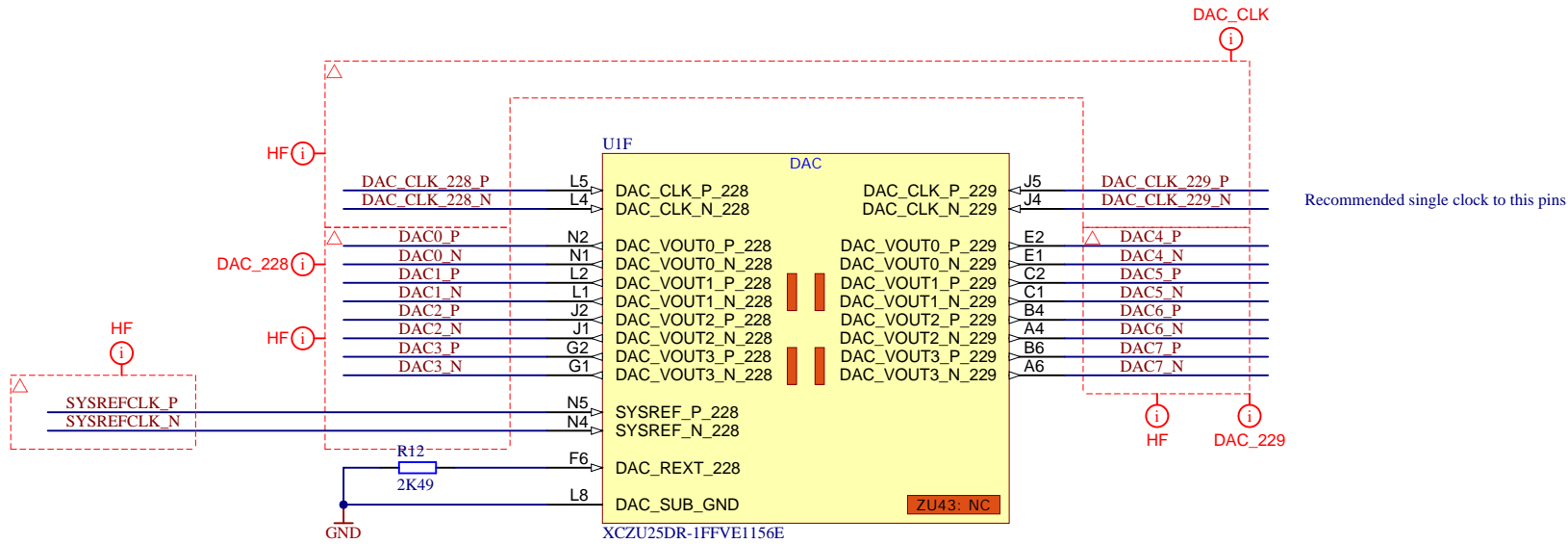


Title: ZU_MGT_L		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 22 of 39
Filename: ZU_MGT_B128_B129.SchDoc		

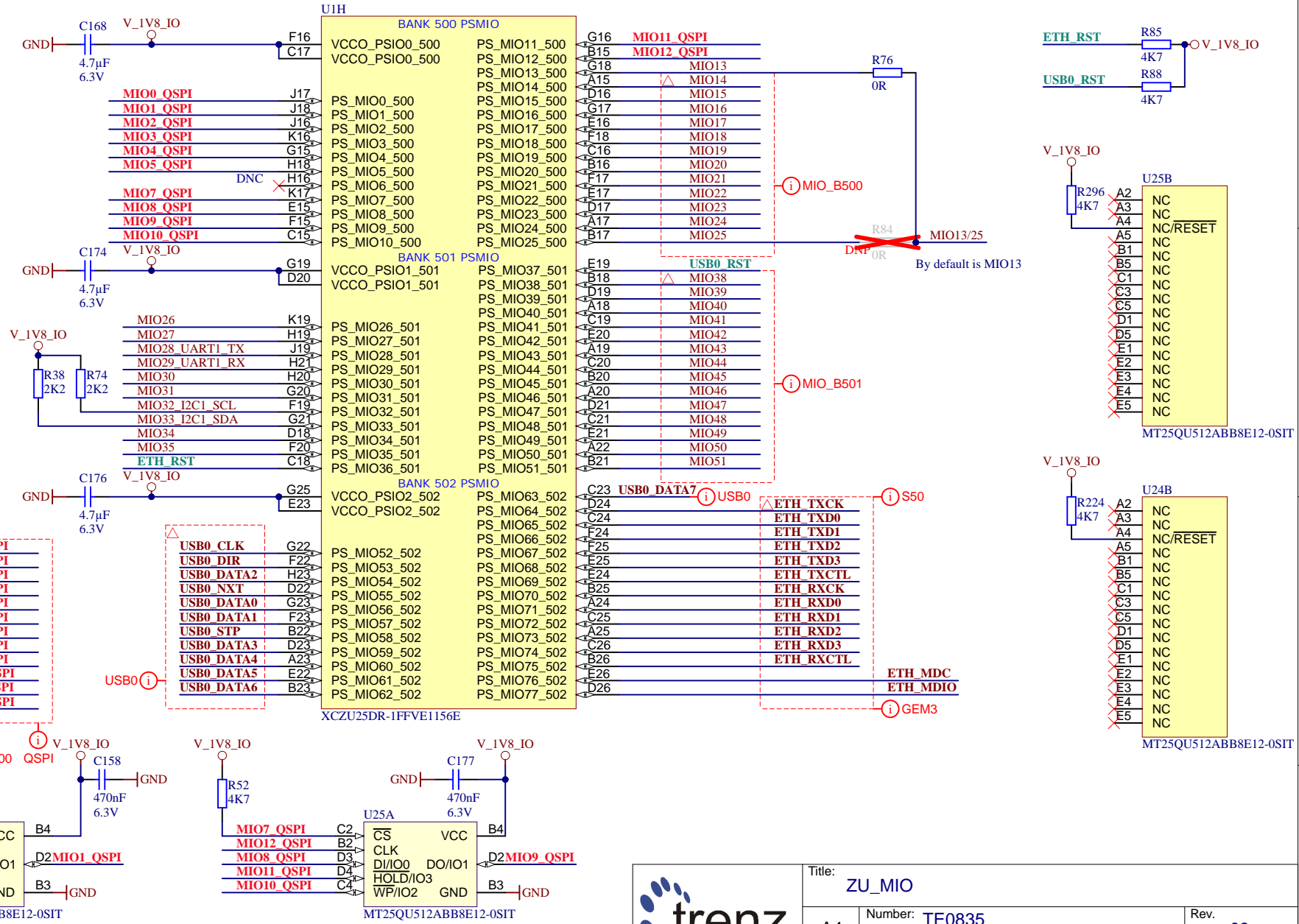
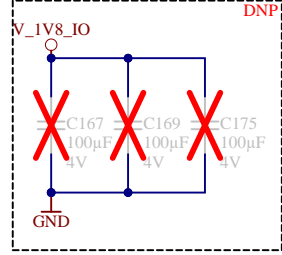


Recommended single clock to this pins

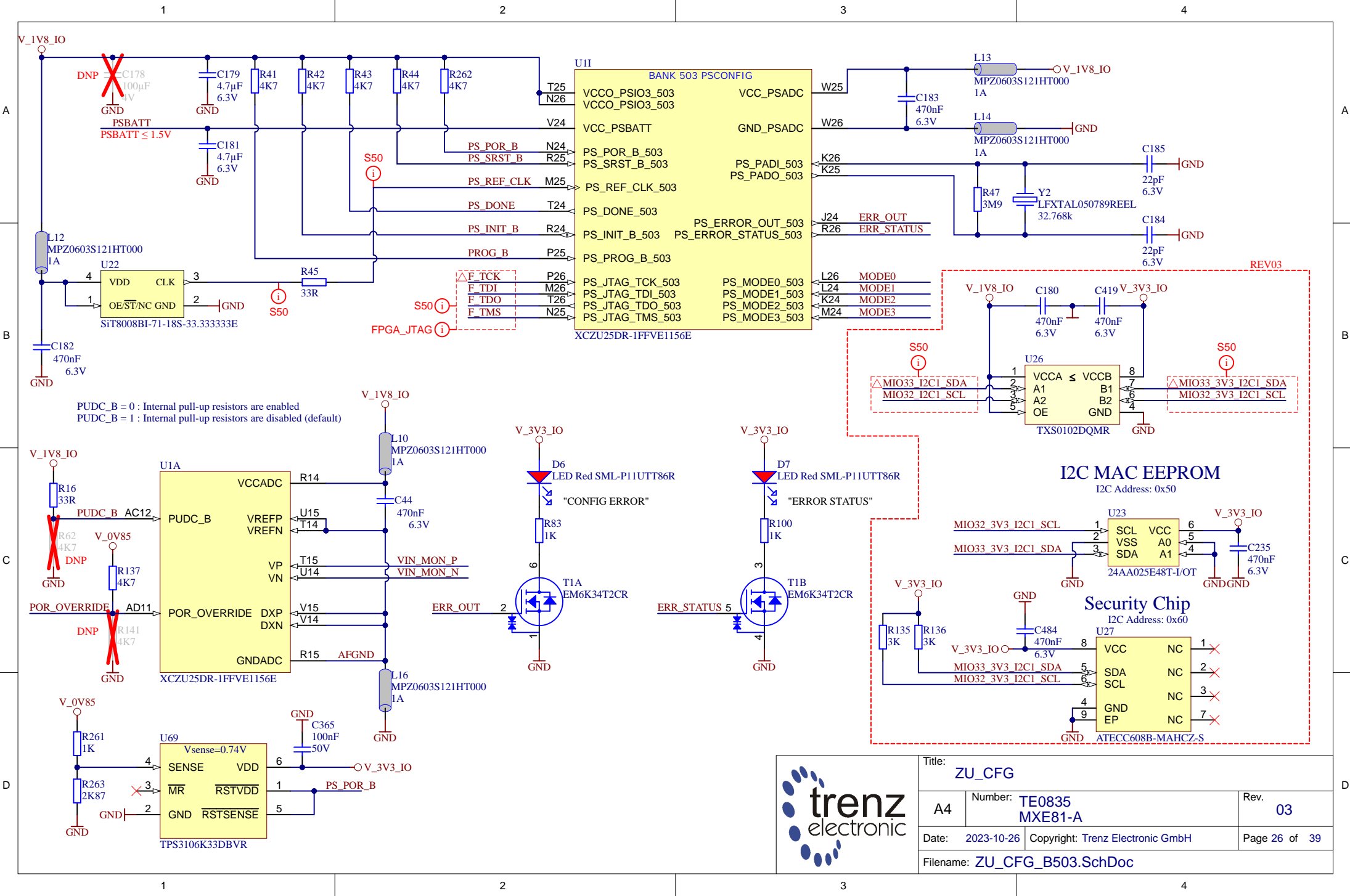
	Title: ZU_ADC	
	A4	Number: TE0835 MXE81-A
	Date: 2023-10-26	Copyright: Trenz Electronic GmbH
	Filename: ZU_ADC_B224_B225_B226_B227.SchDoc	
	Rev. 03	Page 23 of 39



	Title: ZU_DAC		
	A4	Number: TE0835 MXE81-A	Rev. 03
	Date: 2023-10-26	Copyright: Trenz Electronic GmbH	
	Page 24 of 39		
Filename: ZU_DAC_B228_B229.SchDoc			



Title: ZU_MIO		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 25 of 39
Filename: ZU_MIO_B500_B501_B502.SchDoc		



Title: ZU_CFG		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	
Filename: ZU_CFG_B503.SchDoc		Page 26 of 39



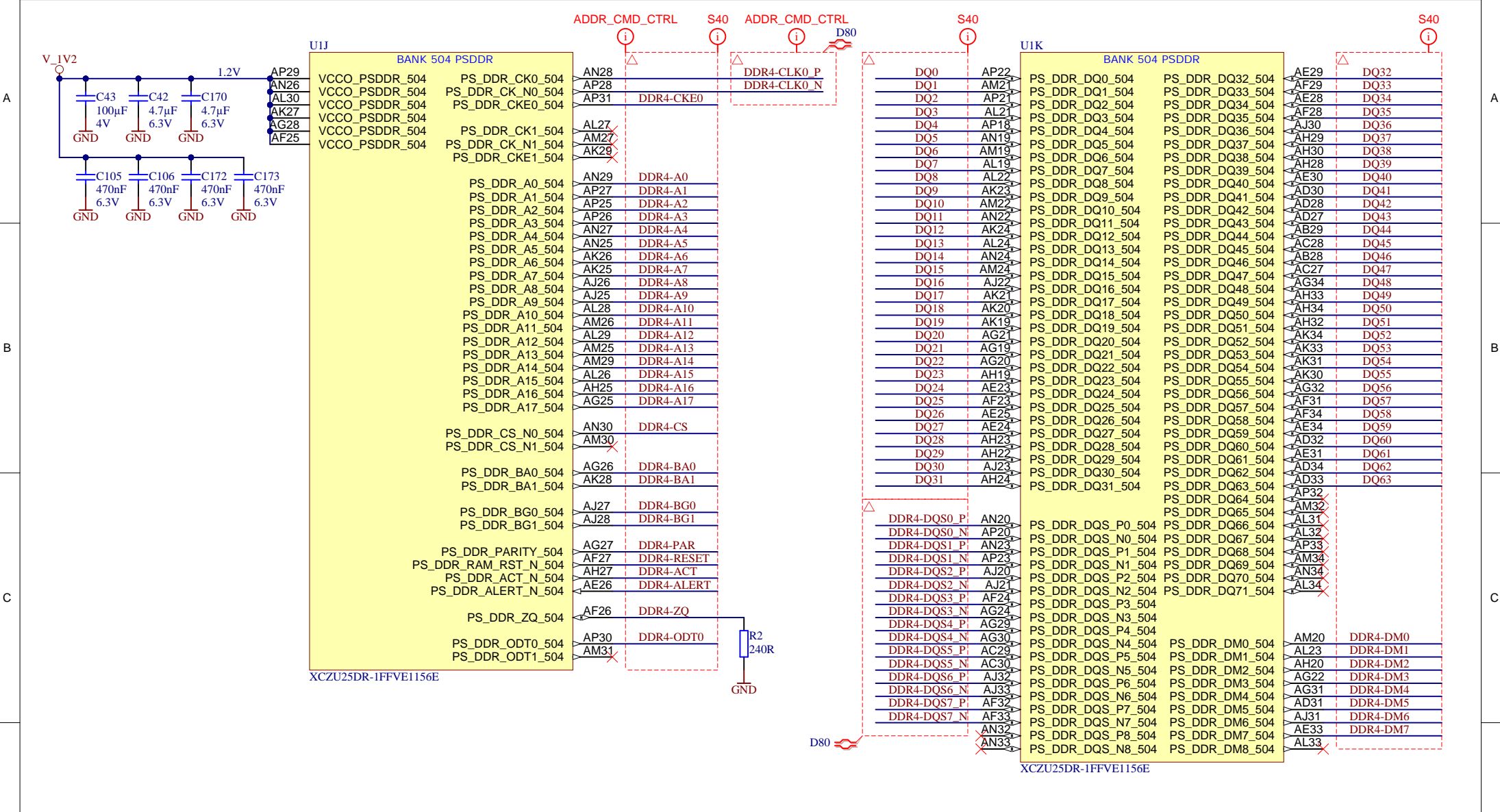
PUDC_B = 0 : Internal pull-up resistors are enabled
PUDC_B = 1 : Internal pull-up resistors are disabled (default)

I2C MAC EEPROM

I2C Address: 0x50

Security Chip

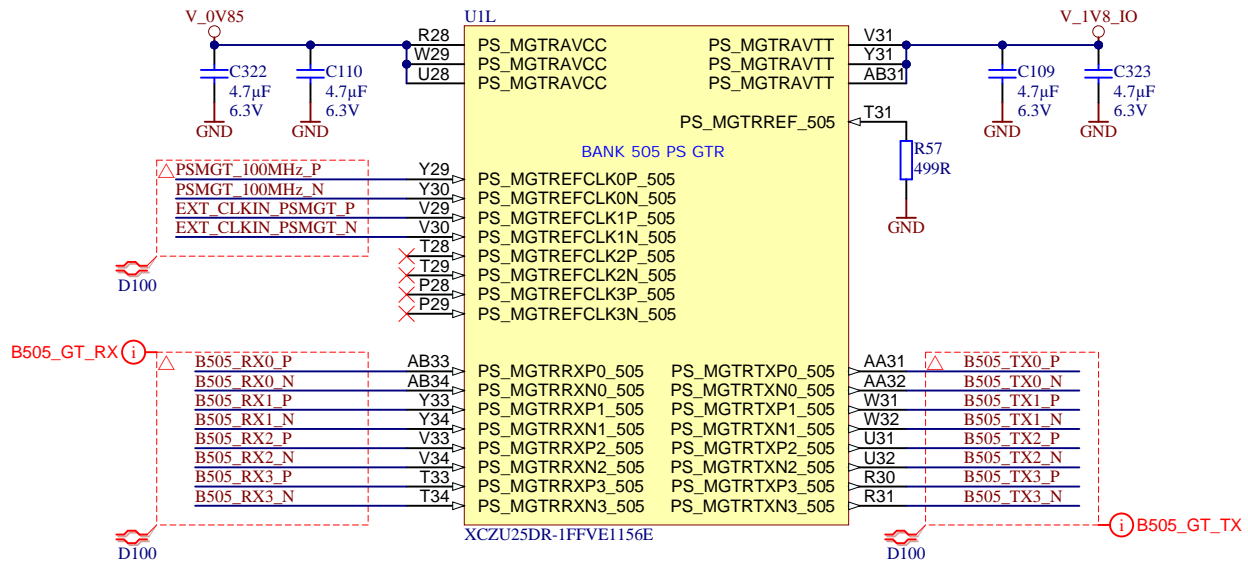
I2C Address: 0x60



Title: **ZU_PSDDR**

A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	
Page 27 of 39		

Filename: **ZU_PSDDR_B504.SchDoc**



Title: ZU_PSMGT		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 28 of 39
Filename: ZU_PSMGT_B505.SchDoc		

A

A

B

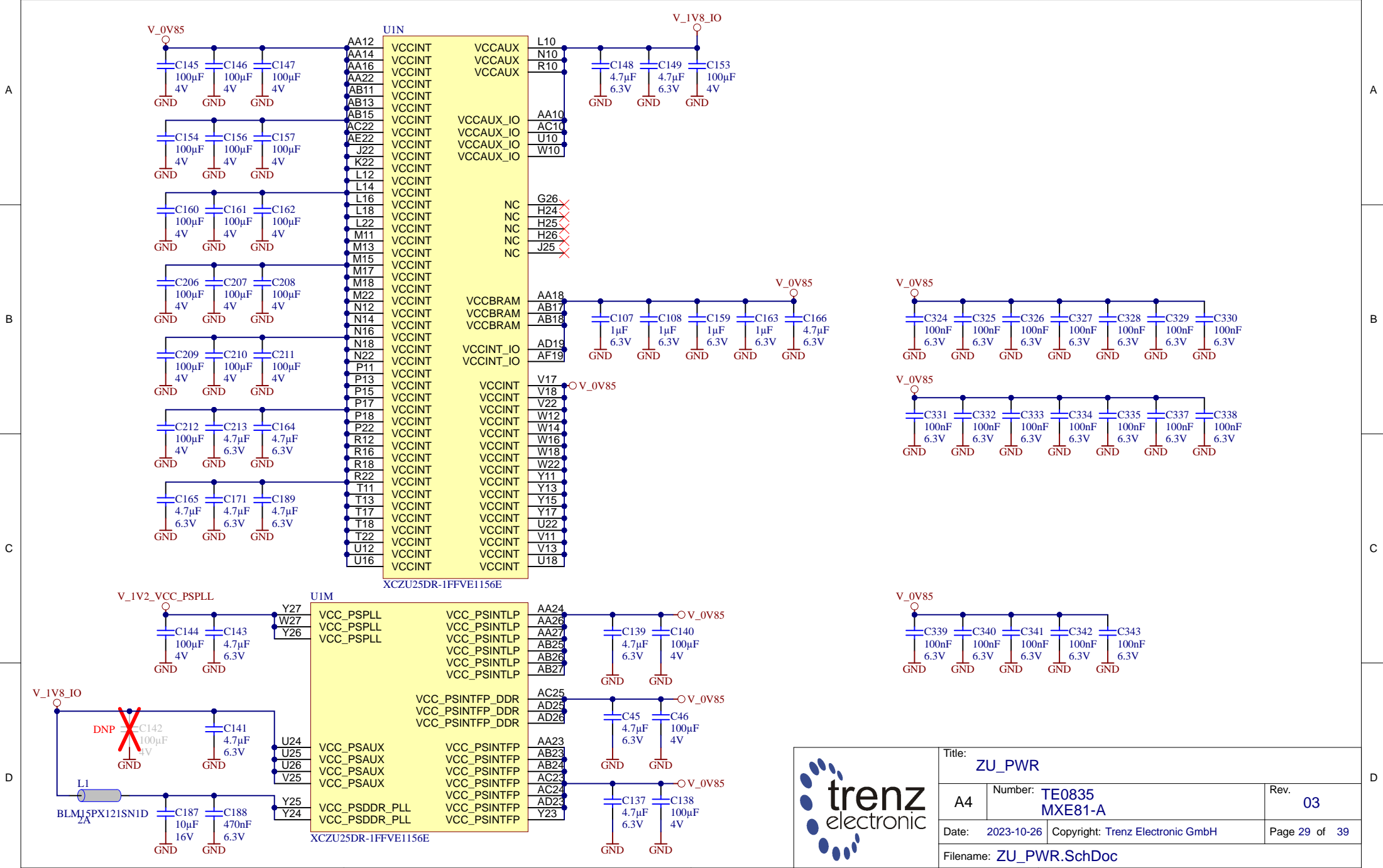
B

C

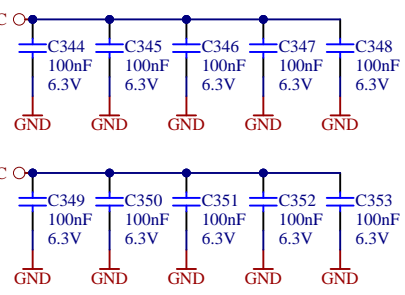
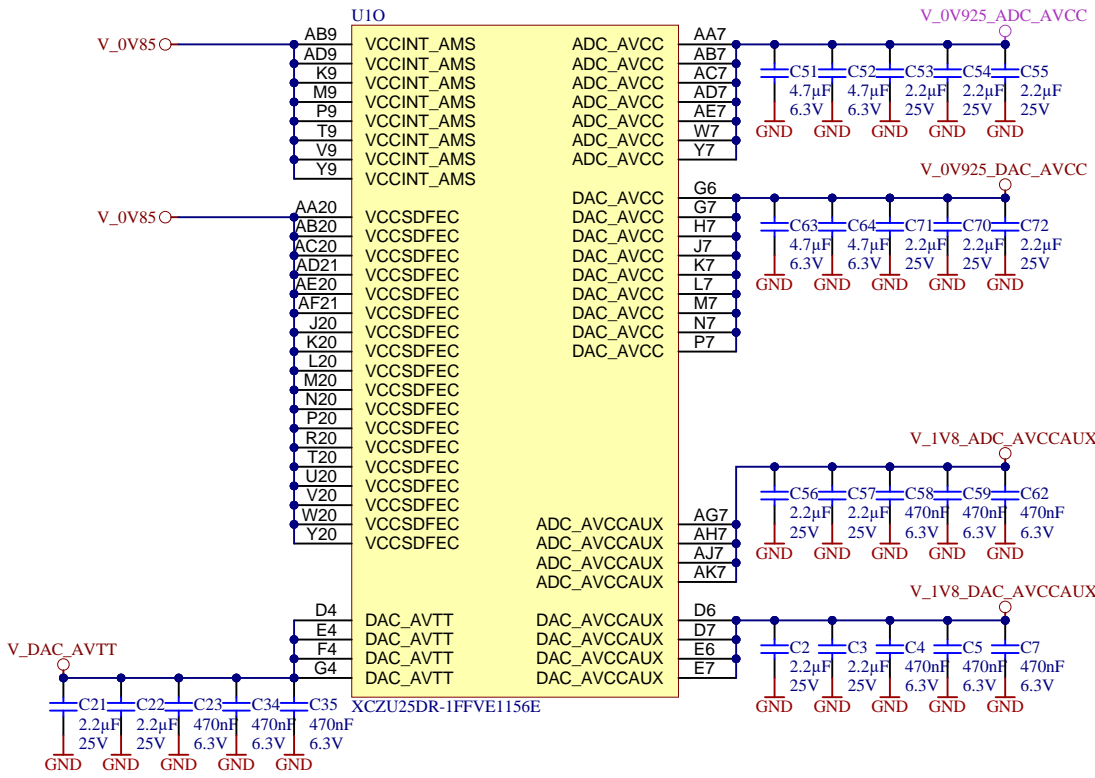
C

D

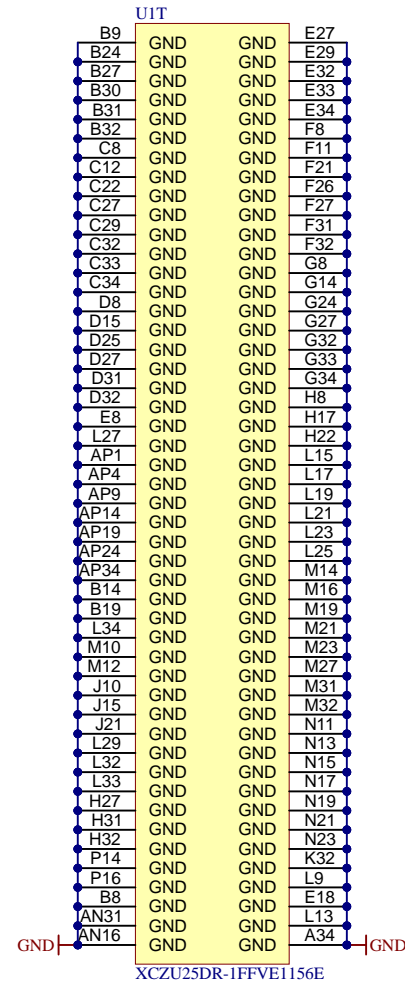
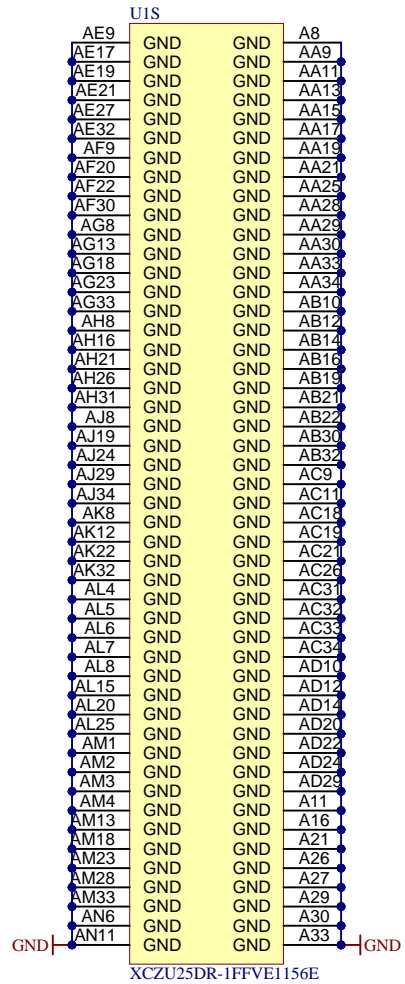
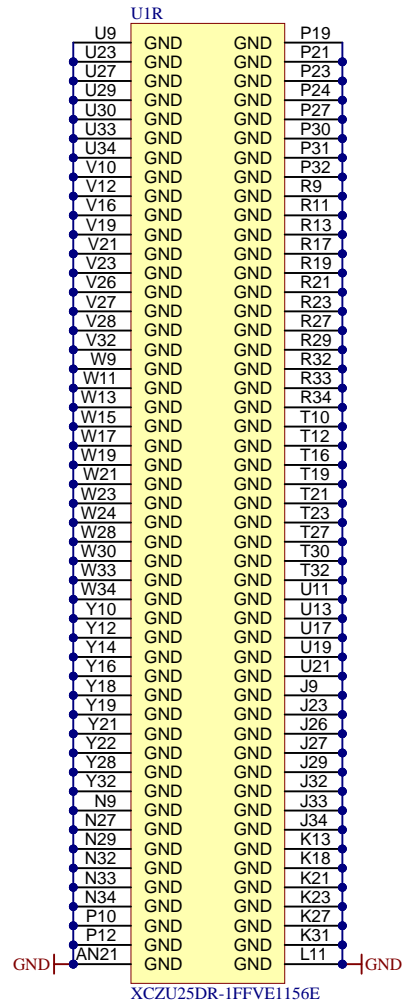
D



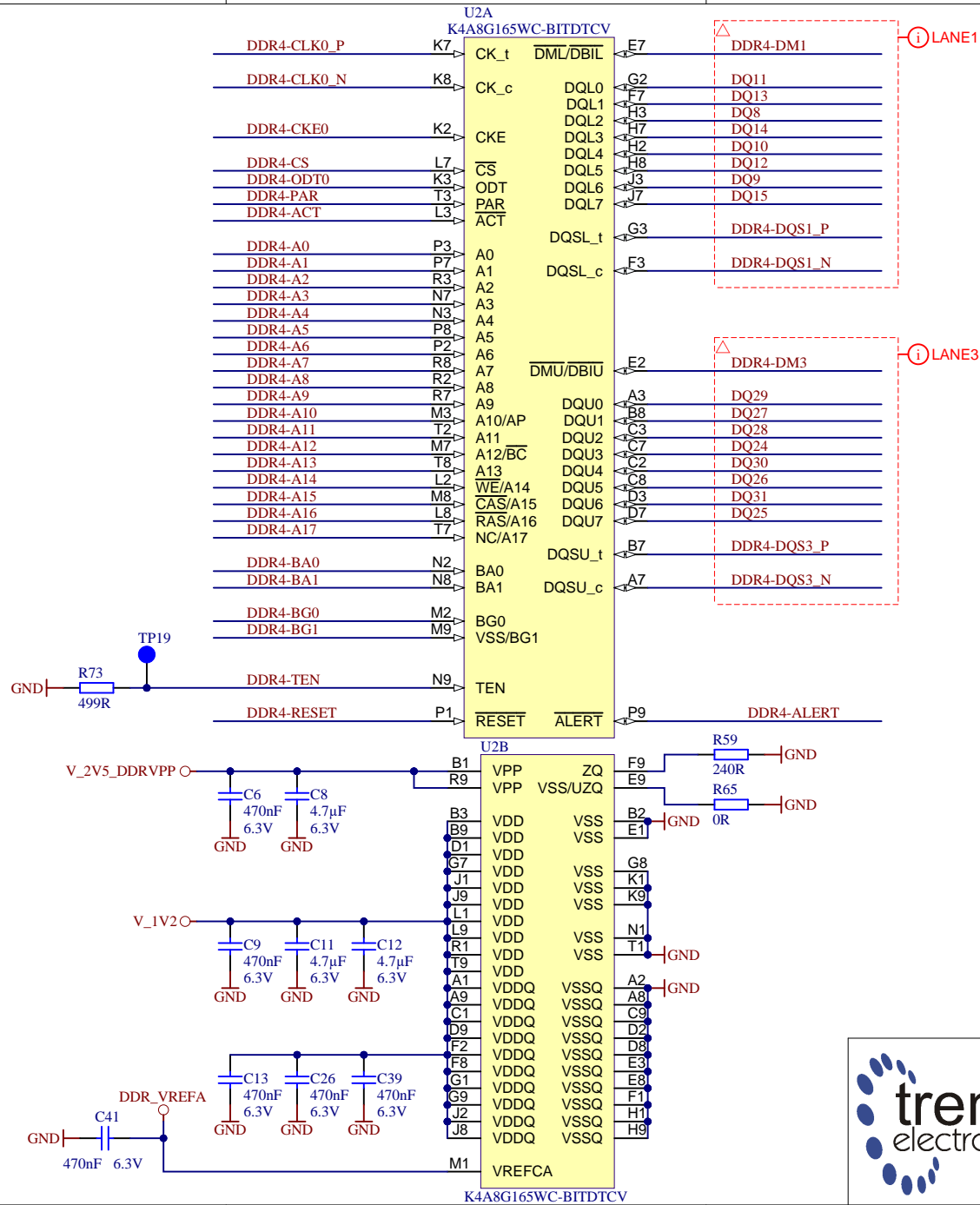
Title: ZU_PWR		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	
Page 29 of 39		
Filename: ZU_PWR.SchDoc		



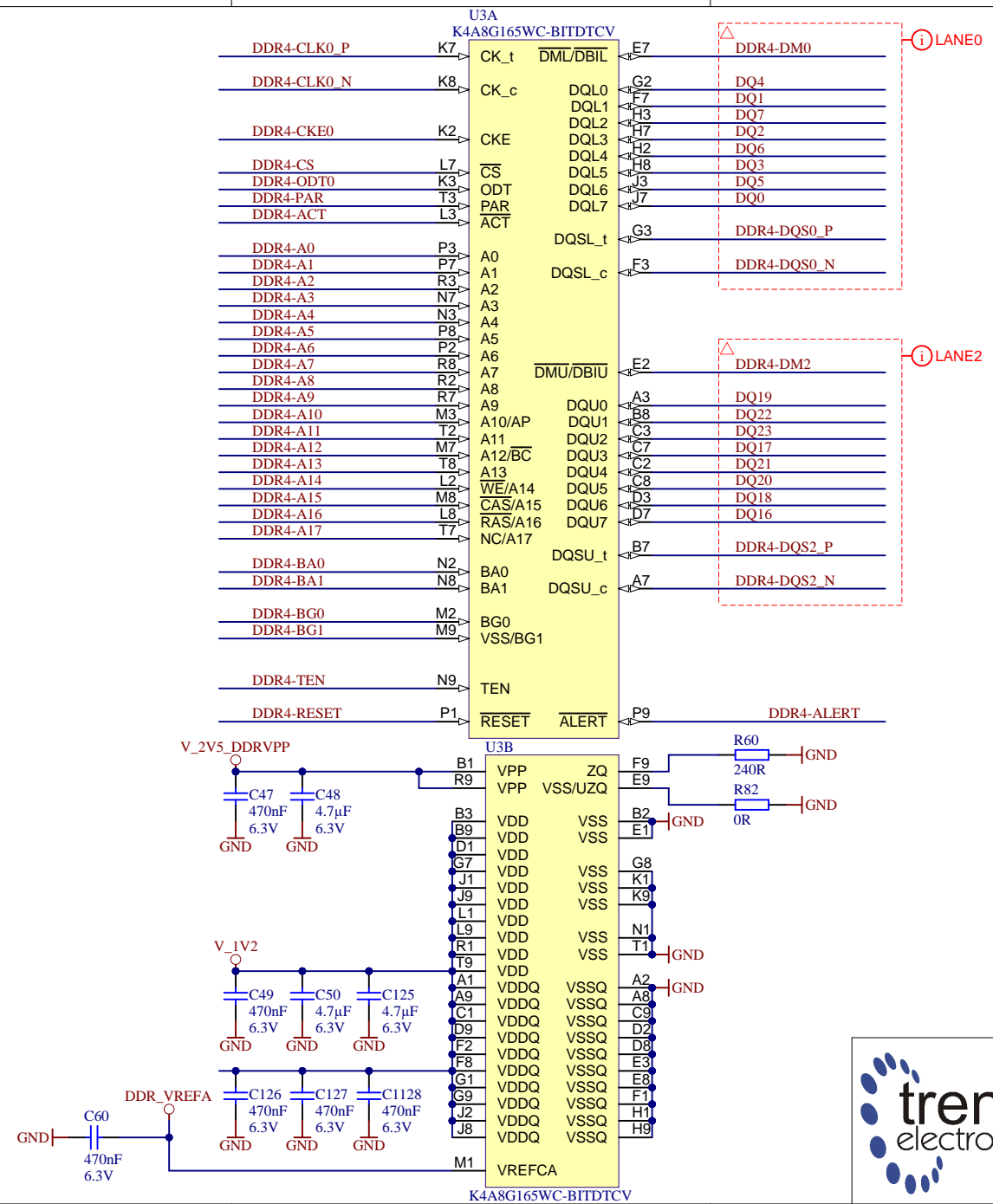
Title: ZU_PWR2		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 30 of 39
Filename: ZU_PWR_RF.SchDoc		



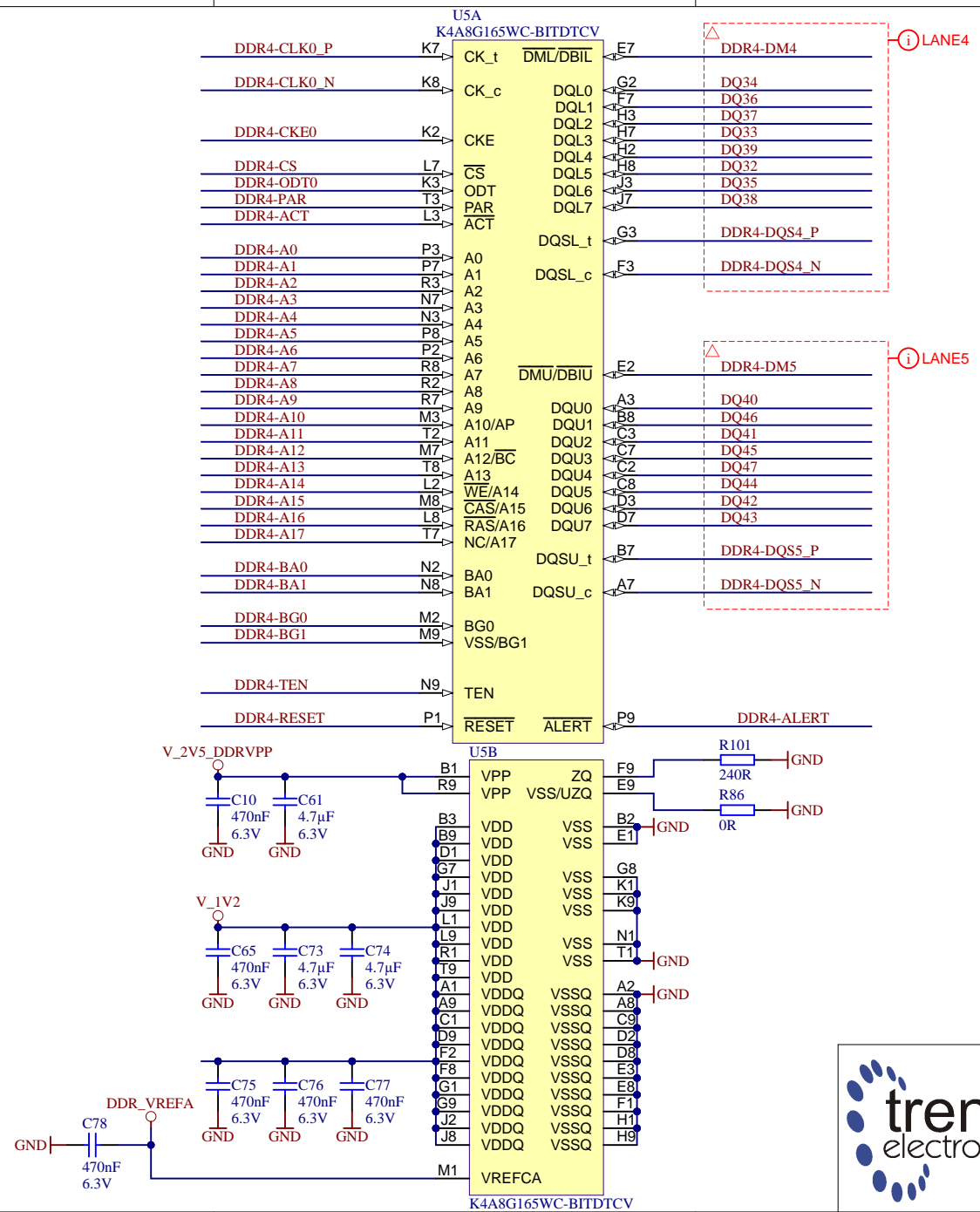
Title: ZU_PWR3		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 31 of 39
Filename: ZU_GND.SchDoc		



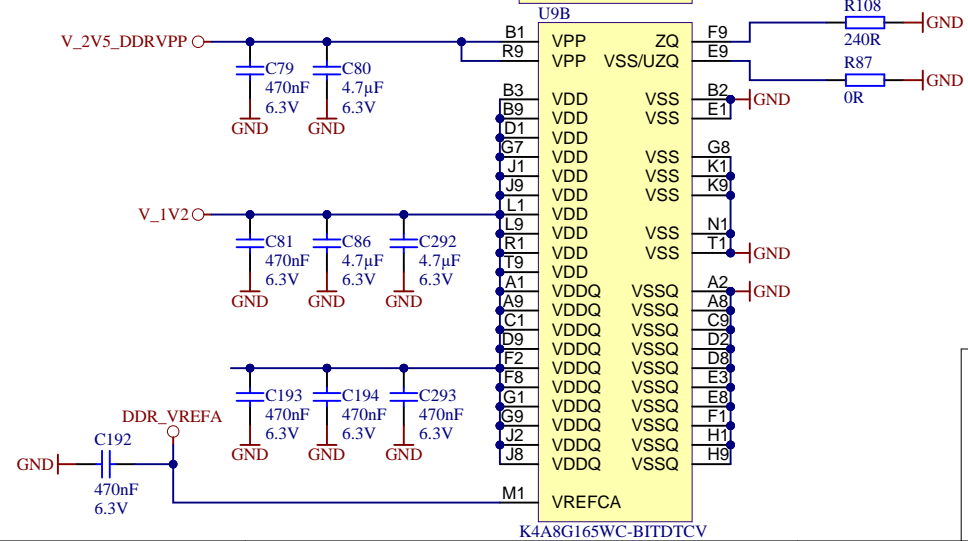
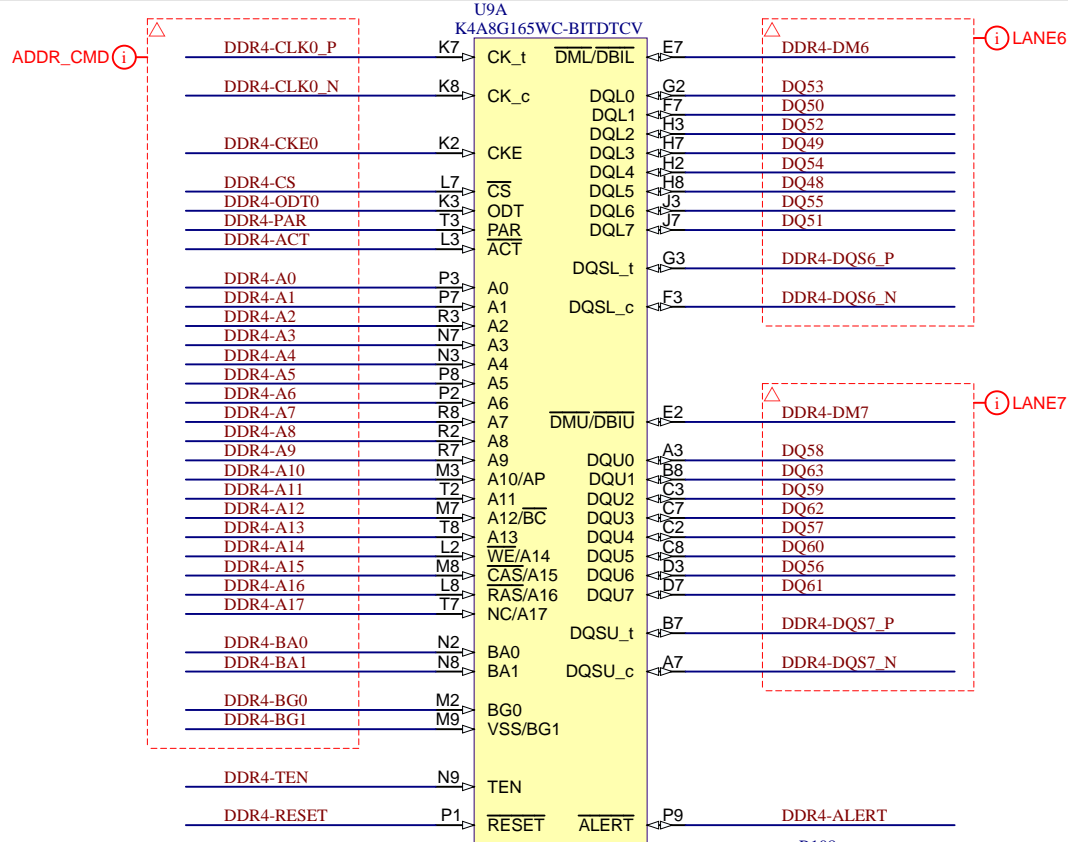
Title: DDR4-RAM_1		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 32 of 39
Filename: DDR4-RAM_1.SchDoc		



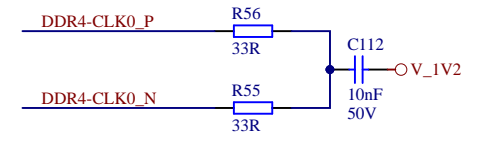
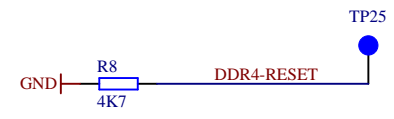
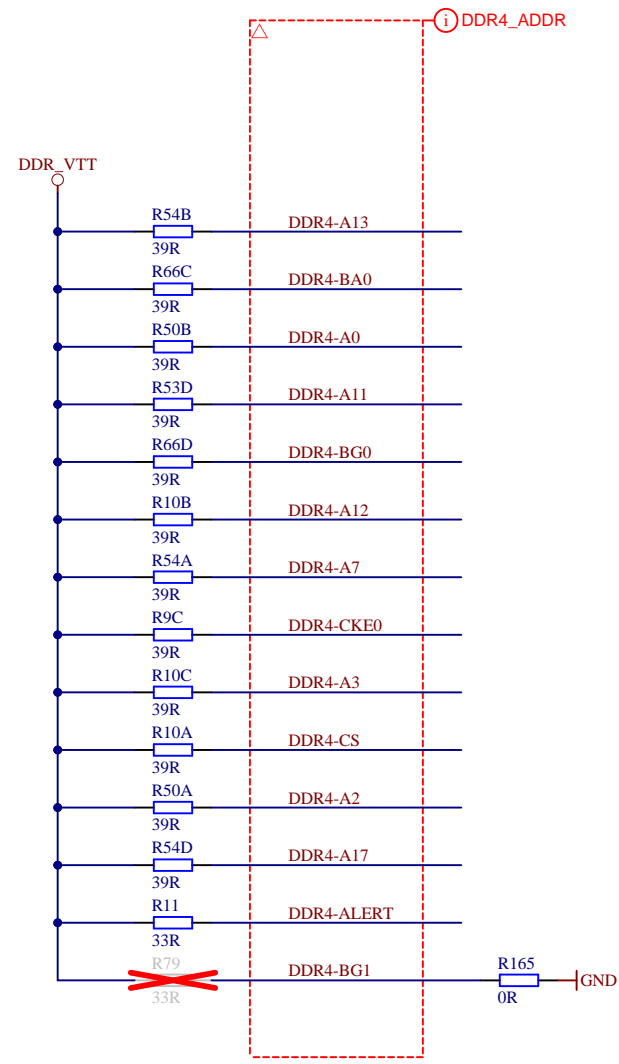
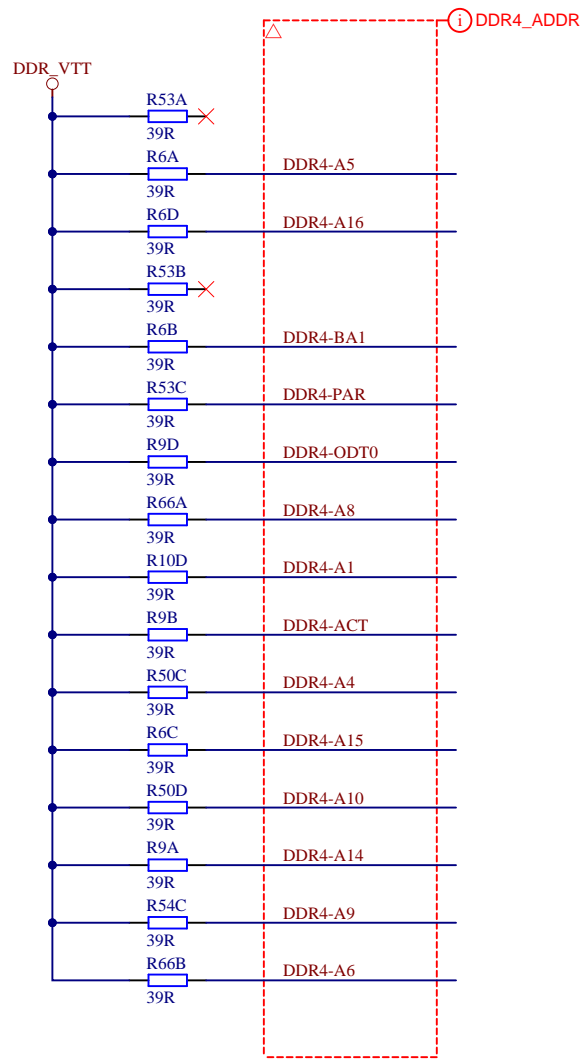
Title: DDR4-RAM_2		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	
Page 33 of 39		
Filename: DDR4-RAM_2.SchDoc		




Title: DDR4-RAM_3		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 34 of 39
Filename: DDR4-RAM_3.SchDoc		



Title: DDR4-RAM_4		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 35 of 39
Filename: DDR4-RAM_4.SchDoc		



		Title: DDR4-TERM	
		A4	Number: TE0835 MXE81-A
Date: 2023-10-26		Copyright: Trenz Electronic GmbH	
Filename: DDR4-TERM.SchDoc		Page 36 of 39	

A

B

C

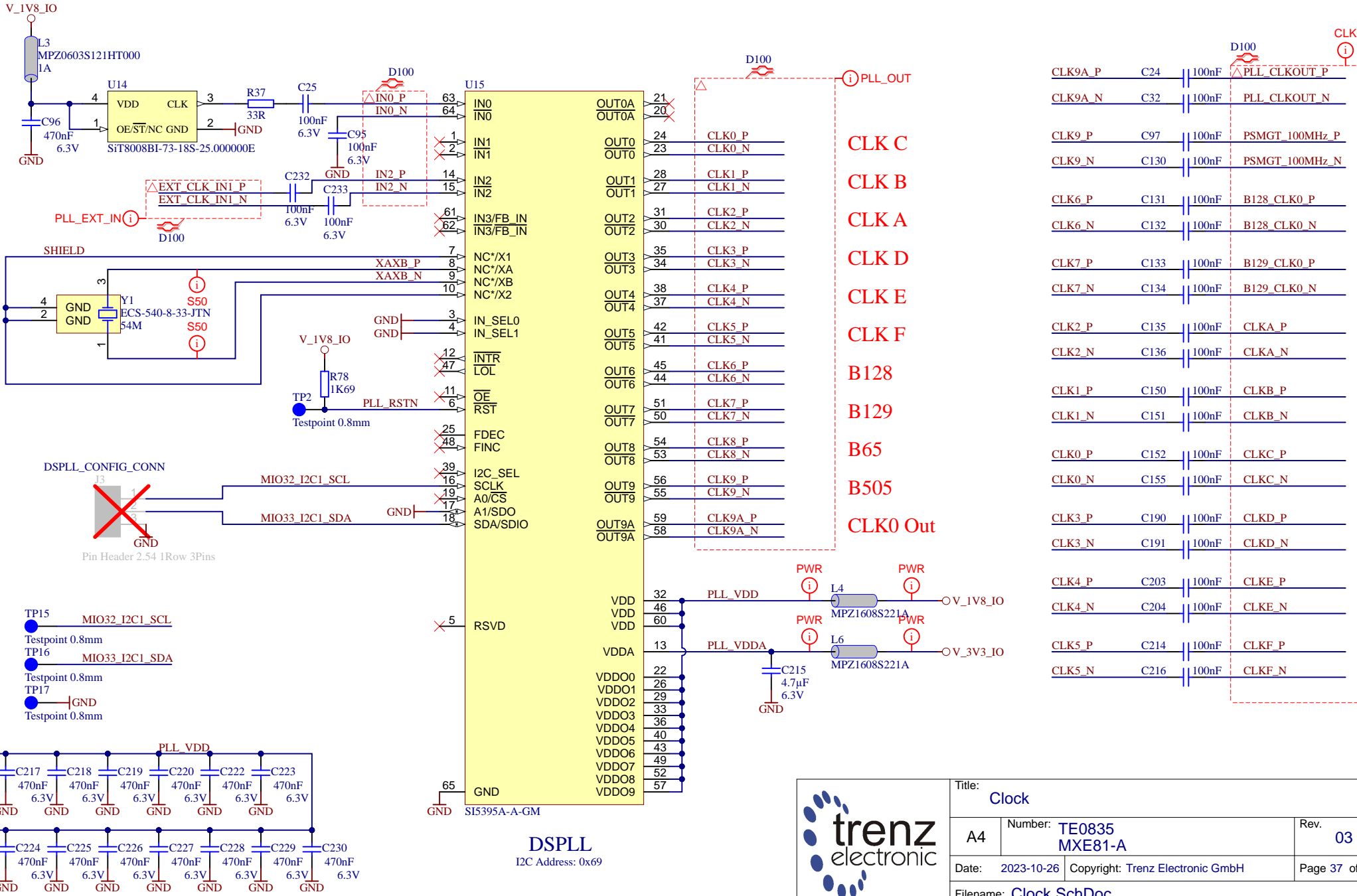
D

A

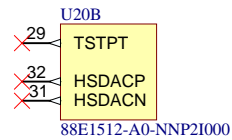
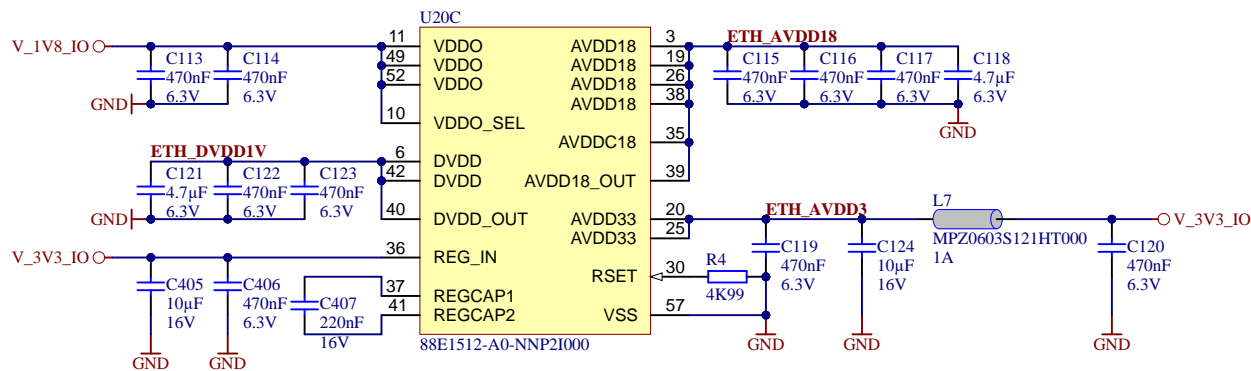
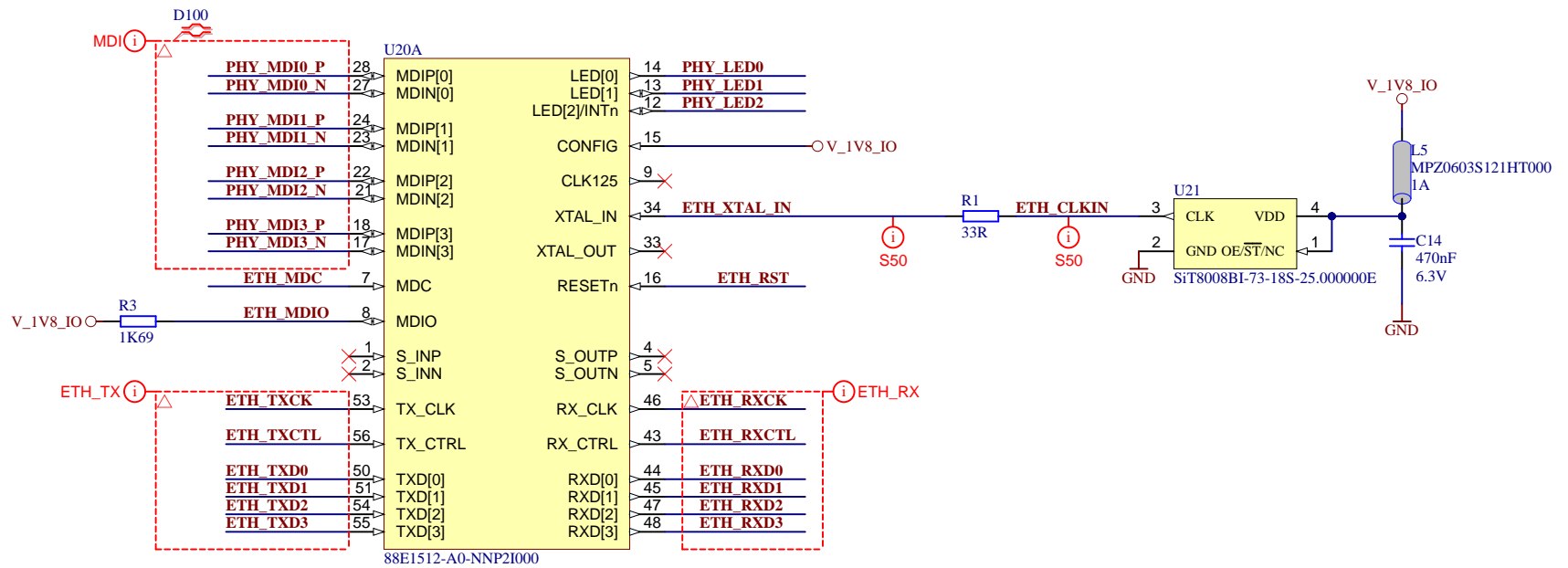
B

C

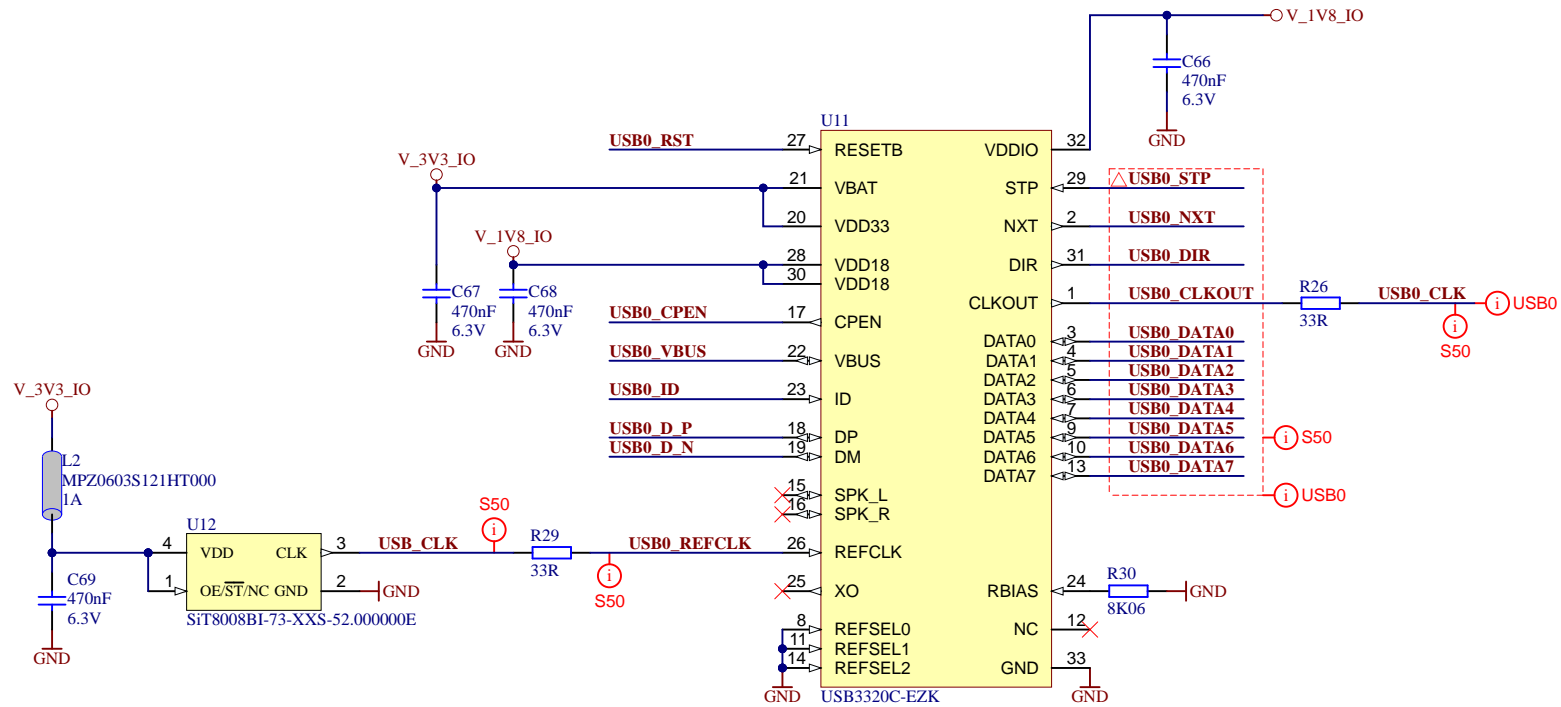
D




Title: Clock		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 37 of 39
Filename: Clock.SchDoc		



Title: Ethernet		
A4	Number: TE0835 MXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 38 of 39
Filename: Ethernet.SchDoc		



	Title: USB-PHY		
	A4	Number: TE0835 MXE81-A	Rev. 03
	Date: 2023-10-26	Copyright: Trenz Electronic GmbH	
	Filename: USB-PHY.SchDoc		Page 39 of 39