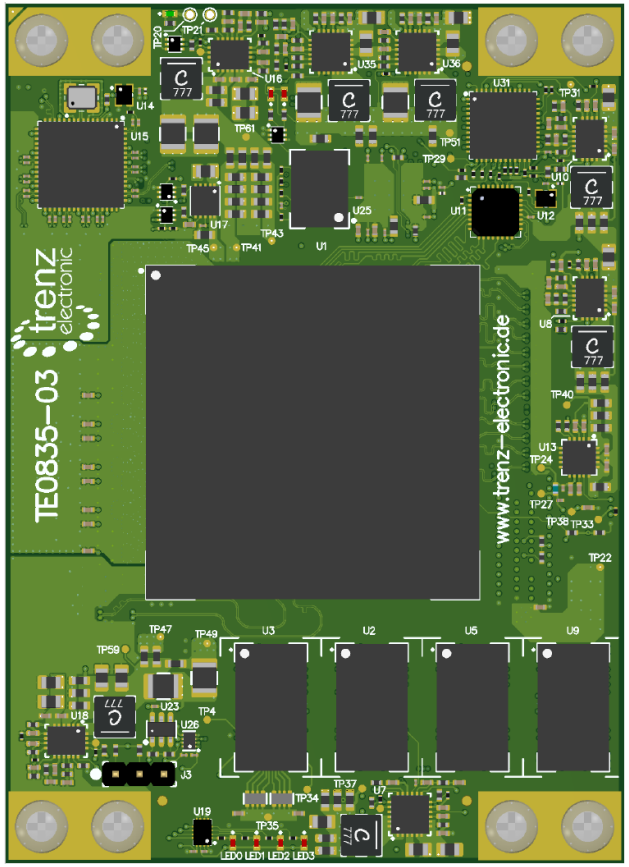

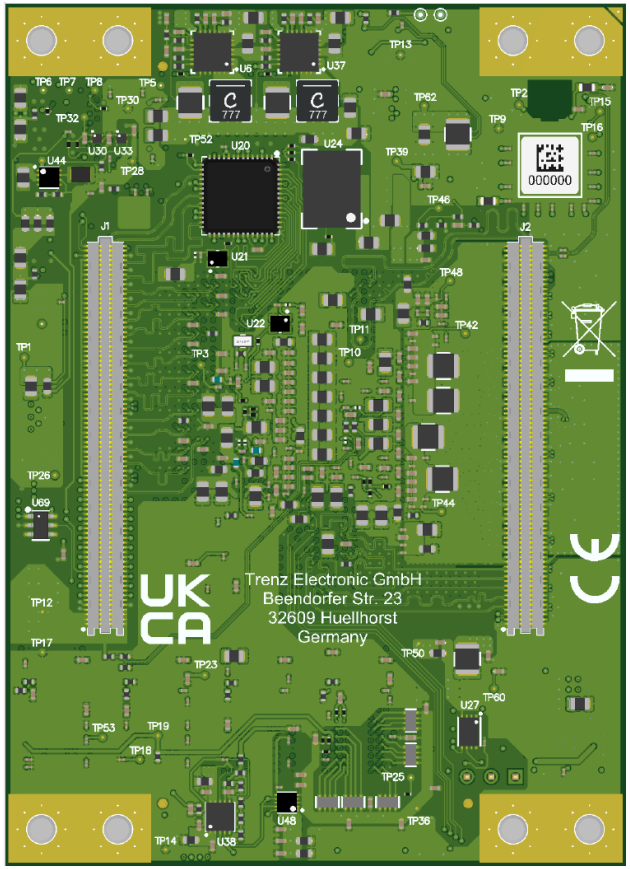

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Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: Legal Notices Modules		
	A4	Number: TE0835 TXE81-A	Rev. 03
	Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 1 of 39
	Filename: Legal Notices Modules.SchDoc		

REVISION HISTORY

REV	Description	
-01	Initial revision	IG
-02	1. Added a VRP resistor on bank 65; 2. LDO U33 is changed on ADP7102ACPZ; 3. Signal FPGA IO0 is connected on AE18 pin of FPGA; 4. Signal DBG_LED3 is connected on AD18 pin of FPGA; 5. Signal MIO13_25 connected to J1 pin 33 instead MIO25. 6. Resistor R84 is removed; 7. LED D1 moved on edge of PCB; 8. Added THT testpoints J4 on CPLD_JTAGEN, R76 was removed; 9. Signals B49_XX_X are renamed in B88_XX_X; 10. C241 is changed on 1nF; 11. Length of CLK signals on RFADC and RFDAC are adjusted; 12. Wrong connection on U8 is fixed (PCB); 13. Wrong connection PGOOD1 pin of U7 is fixed; 14. R17 is changed from 35,5K to 33K for VCC_PL_PS correction.	IG
-02	15. APRE_3V3 ranamed to APRE_4V5, voltage of the power rail incrised from 3.3V to 4,58V. 16. Resistor R15 is changed from 13,3K to 9,09K. AN: 24671->25969 17. Capasitor C27 is changed from 100uF x 4V to 47uF x 6,3V. AN: 28940->24718	IG
-03	1. Added Legal Notices. 2. Added Power Diagram. 3. Added a DC-DCs synchronization circuit to spread spectrum. 4. Changed the core power supply schematic to 4 phases to increase current and reduce noise. 5. The power supply circuit of the module supports input voltage 5...12V. 6. EOL components are replaced: 6.1. L10, L12, L13, L14, L16 Ferrit beads BKP0603HS121-T replaced with MPZ0603S121HT000. 7. Updated layerstack to enhance power supply circuits and improve signal impedance matching. 8. Added POR_OVERRIDE configuration. 9. U25 (Pin 33) PS_SRST_B signal was removed. POR_OVERRIDE_N connected. 10. Added transistor T2A. 11. C180 is removed from schematic. 12. Networks to power the banks have been renamed. 13. Added Level shifter U19. 14. LEDs renamed: D1 --> LED0; D2 --> LED1; D3 --> LED2; D4 --> LED3 and connected to V_3V3_IO. Resistors R77A, R77B, R77C, R77D (39 R) replaced with R77, R130, R132, R134 (1K) respectively according to new shematic. 15. Added pull-up resistors R157, R158, R159, R161, R162, R163 to synchronise the power supplies. 16. Added resistors R142-R145. 17. U23 connected to V_3V3_IO (was 1.8V). 18. ZU_PWR: L9 removed from shematic. 19. Added resistors R46, R90, R98, R146, R149. 20. Added U44. 21. U33 (ADP7102ACPZ) replaced with MIC5504-3.3YMT. 22. Added two capasitors 4.7uF C355 and C488 on DDR_VTT. 23. Added signal SEL_2V5_DAC to Bank 65HP. Pin AD16. 24. Capasitors C24, C32, C97, C130-136, 150-152, 155, 190,191, C203, C204, C214, C216 are replaced with 100 nF. 25. Y1 CX3225SB54000 is EOL, it is replaced with ECS-540-8-33-JTN-TR 26. Added a VIN voltage sensor R121, R124, R150, R122, R153, C489. 27. Added R154, R155 to implement I2C interface between SC and RFSoC. 28. Clock CLK0A_100MHz renamed to PLL_CLKOUT	IG 27.03.2024

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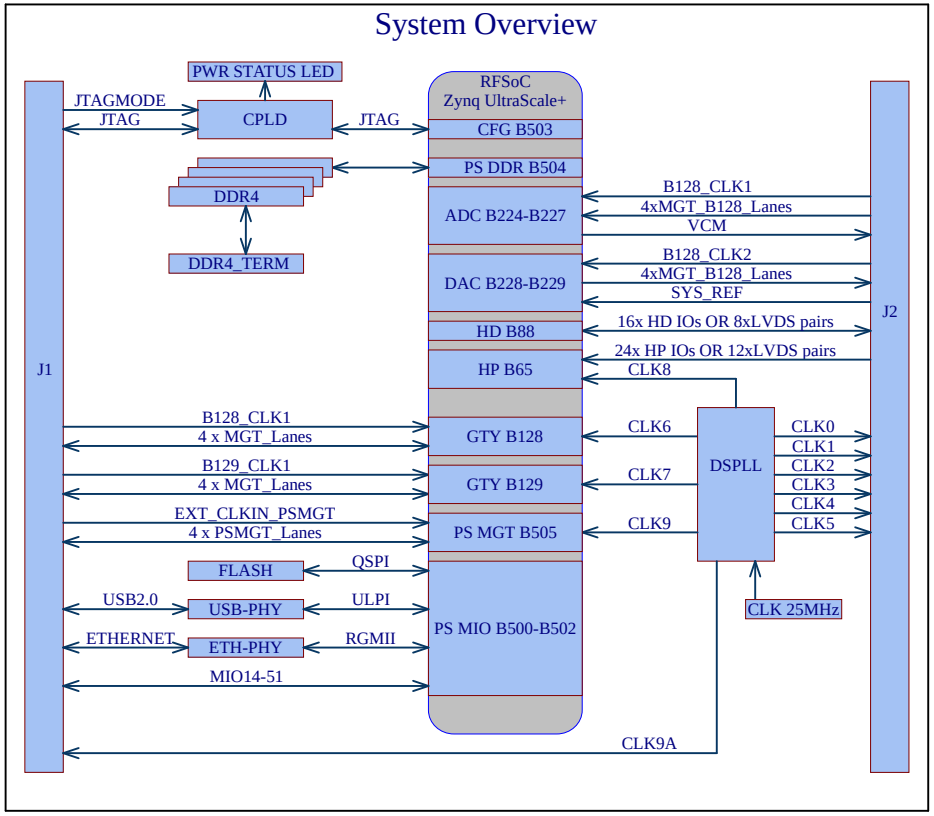
Special notes:

U_PWR-DIAGRAM
U_FPGA-PWR
U_FPGA-PWR_RF
U_FPGA-GND
POWER_STDBY_BIAS
POWER_VCCINT_PH1
POWER_VCCINT_PH2
POWER_VCCINT_PH3
POWER_VCCINT_PH4
POWER_1V2
POWER_IO_1V8
POWER_IO_3V3
POWER_MGT
POWER_RF
POWER_RF_1V8
POWER_DDR

System Overview



PM1 FIDU-DOT - mini
PM2 FIDU-DOT - mini
PM3 FIDU-DOT - mini
PM4 FIDU-DOT - mini
PM5 FIDU-DOT - mini
PM6 FIDU-DOT - mini

Table of I2C devices and addresses

Designator	I2C Address	Description
U23	0x50	I2C MAC EEPROM
U27	0x60	Security Chip
U15	0x69	DSPLL

LOGO1
TE Logo PRINT Layer
LOGO PRINT

MECH1
TE Address Overlay
LOGO ADDRESS

S/N
Serial
Serialnumber 6,3 x 6.3mm

UKCA
UKCA Logo on Top Overlay
UKCA-TOPOVERLAY

Design drawn by:	IG
Checked by:	MR
Assembly variant:	TXE81-A
Created by:	OT
Modified by:	IG
Modified at:	2024-02-19

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Title: TE0835

A4	Number: TE0835 TXE81-A	Rev. 03
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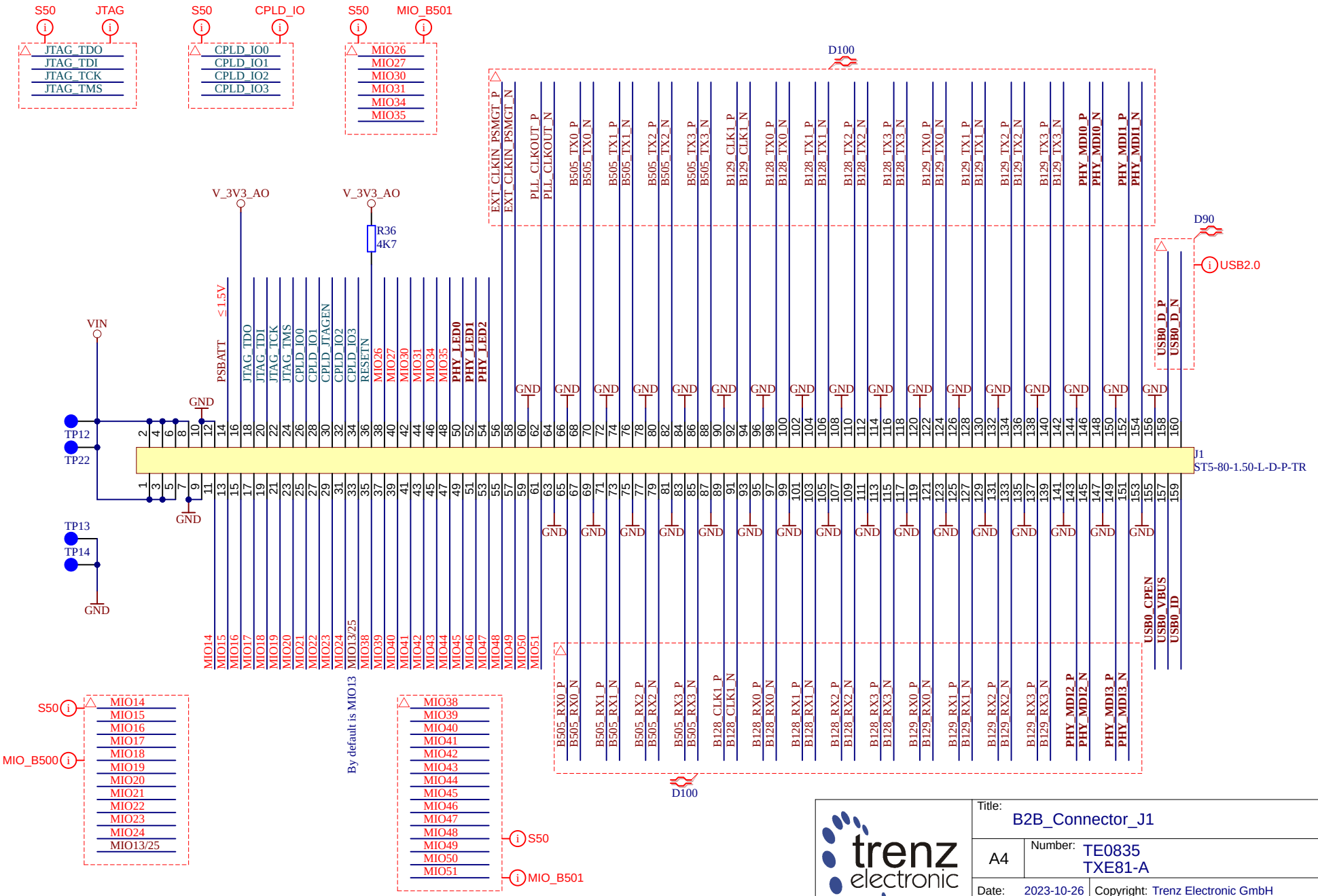
Filename: TE0835-Overview.SchDoc		


S50
JTAG
JTAG_TDO
JTAG_TDI
JTAG_TCK
JTAG_TMS
S50
CPLD_IO
CPLD_IO0
CPLD_IO1
CPLD_IO2
CPLD_IO3
S50
MIO_B501
MIO26
MIO27
MIO30
MIO31
MIO34
MIO35
D100
V_3V3_AO
V_3V3_AO
R36
4K7
D90
USB2.0
USB0_D_P
USB0_D_N
VIN
PSBATT
≤1.5V
JTAG_TDO
JTAG_TDI
JTAG_TCK
JTAG_TMS
CPLD_IO0
CPLD_IO1
CPLD_JTAGEN
CPLD_IO2
CPLD_IO3
RESETN
MIO26
MIO27
MIO30
MIO31
MIO34
MIO35
PHY_LED0
PHY_LED1
PHY_LED2
GND
TP12
TP22
TP13
TP14
J1
ST5-80-1.50-L-D-P-TR
EXT_CLKIN_PSMGT_P
EXT_CLKIN_PSMGT_N
PLL_CLKOUT_P
PLL_CLKOUT_N
B505_TX0_P
B505_TX0_N
B505_TX1_P
B505_TX1_N
B505_TX2_P
B505_TX2_N
B505_TX3_P
B505_TX3_N
B129_CLK1_P
B129_CLK1_N
B128_TX0_P
B128_TX0_N
B128_TX1_P
B128_TX1_N
B128_TX2_P
B128_TX2_N
B128_TX3_P
B128_TX3_N
B129_TX0_P
B129_TX0_N
B129_TX1_P
B129_TX1_N
B129_TX2_P
B129_TX2_N
B129_TX3_P
B129_TX3_N
PHY_MDI0_P
PHY_MDI0_N
PHY_MDI1_P
PHY_MDI1_N
USB0_CPEN
USB0_VBUS
USB0_ID
MIO14
MIO15
MIO16
MIO17
MIO18
MIO19
MIO20
MIO21
MIO22
MIO23
MIO24
MIO13/25
MIO38
MIO39
MIO40
MIO41
MIO42
MIO43
MIO44
MIO45
MIO46
MIO47
MIO48
MIO49
MIO50
MIO51
B505_RX0_P
B505_RX0_N
B505_RX1_P
B505_RX1_N
B505_RX2_P
B505_RX2_N
B505_RX3_P
B505_RX3_N
B128_CLK1_P
B128_CLK1_N
B128_RX0_P
B128_RX0_N
B128_RX1_P
B128_RX1_N
B128_RX2_P
B128_RX2_N
B128_RX3_P
B128_RX3_N
B129_RX0_P
B129_RX0_N
B129_RX1_P
B129_RX1_N
B129_RX2_P
B129_RX2_N
B129_RX3_P
B129_RX3_N
PHY_MDI2_P
PHY_MDI2_N
PHY_MDI3_P
PHY_MDI3_N
By default is MIO13
S50
MIO_B500
MIO14
MIO15
MIO16
MIO17
MIO18
MIO19
MIO20
MIO21
MIO22
MIO23
MIO24
MIO13/25
MIO38
MIO39
MIO40
MIO41
MIO42
MIO43
MIO44
MIO45
MIO46
MIO47
MIO48
MIO49
MIO50
MIO51
S50
MIO_B501
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Title: B2B_Connector_J1
A4
Number: TE0835 TXE81-A
Rev. 03
Date: 2023-10-26
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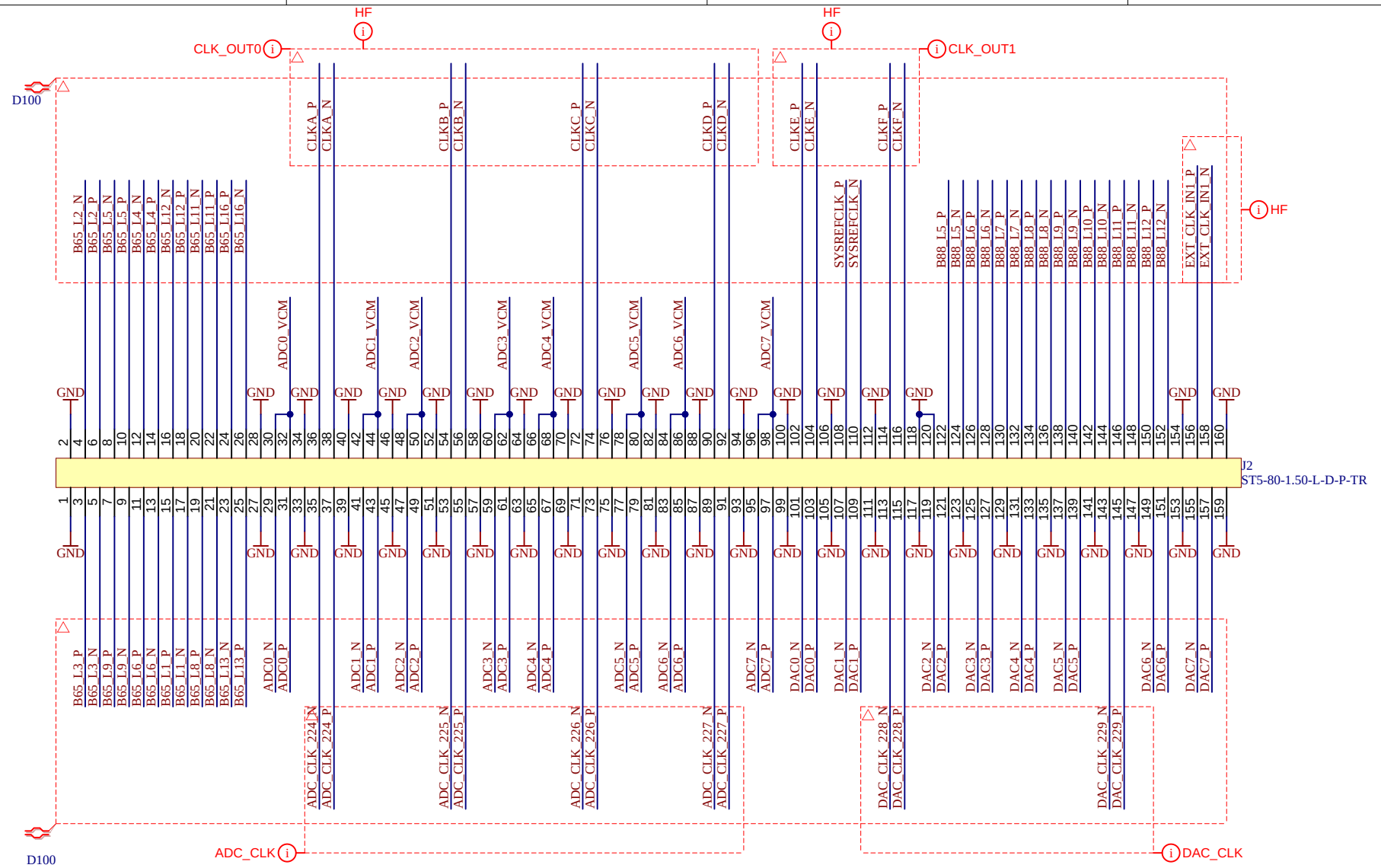
Filename: B2B_Connector_J1.SchDoc



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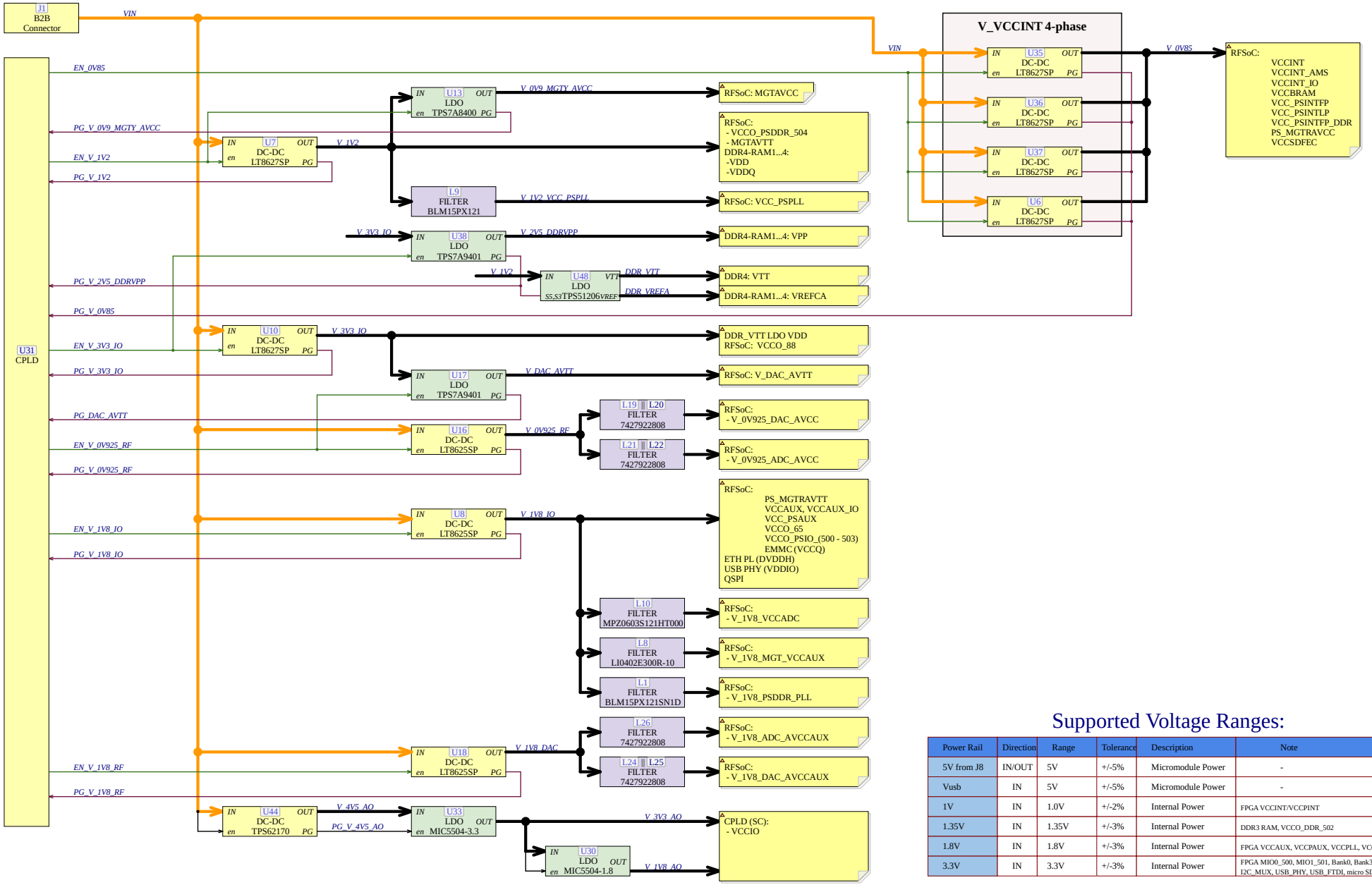
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 5 of 39
Filename: B2B_Connector_J2.SchDoc			

Power-on sequencing:



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
5V from J8	IN/OUT	5V	+/-5%	Micromodule Power	-
Vusb	IN	5V	+/-5%	Micromodule Power	-
1V	IN	1.0V	+/-2%	Internal Power	FPGA VCCINT/VCCPINT
1.35V	IN	1.35V	+/-3%	Internal Power	DDR3 RAM, VCCO_DDR_502
1.8V	IN	1.8V	+/-3%	Internal Power	FPGA VCCAUX, VCCPAUX, VCCPLL, VCCBATT, AVCC; SC
3.3V	IN	3.3V	+/-3%	Internal Power	FPGA MIO0_500, MIO1_501, Bank0, Bank34, Bank35 I2C_MUX, USB_PHY, USB_FTDI, micro SD, USB Hub, SC

Net name — Power bus

U4 DC-DC TPS62170 — Power converter

en — Control signals

PG — Power Good signals

LDOs

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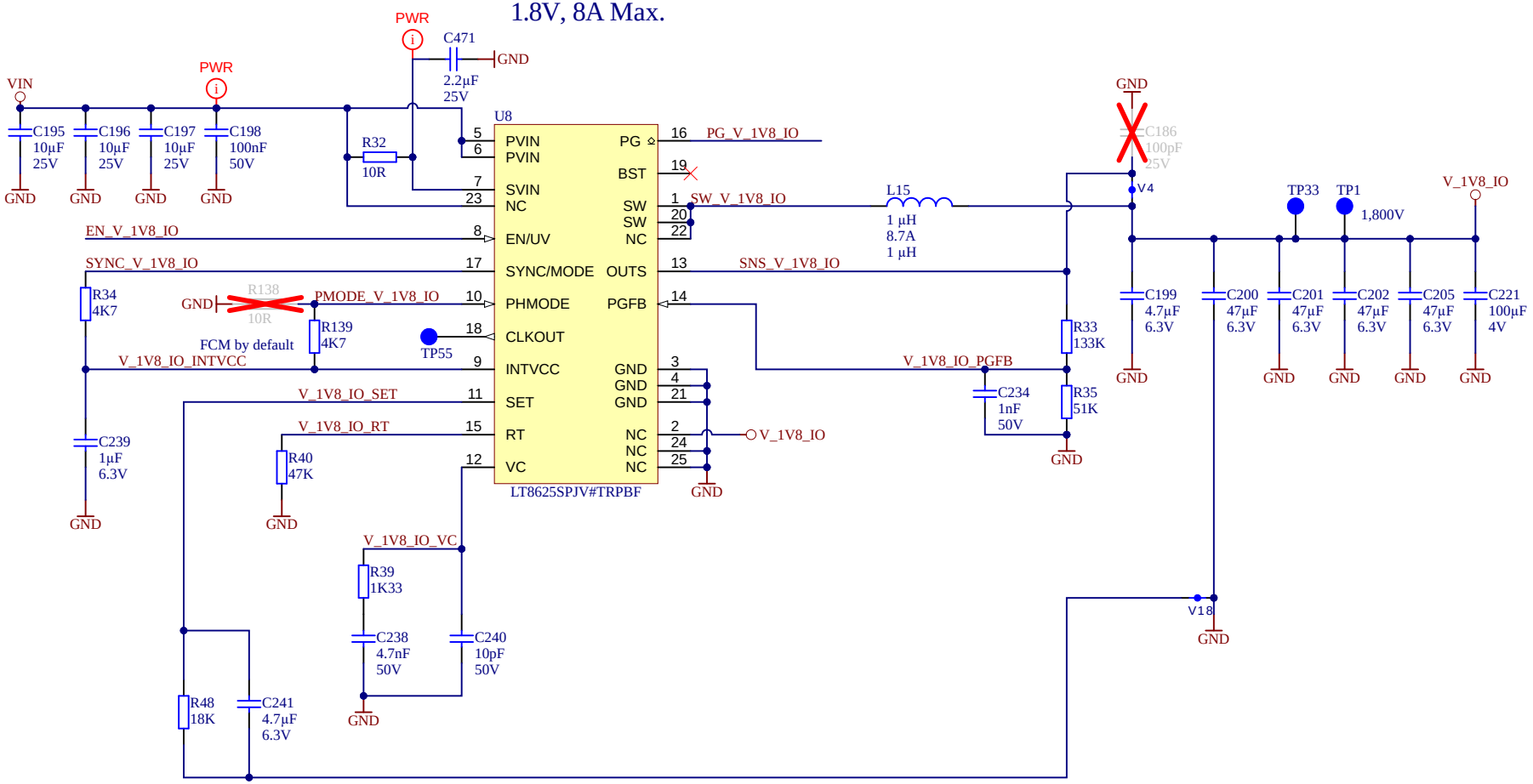
Title: Power_Diagram		
A3	Nummer: TE0835 TXE81-A	Rev. 03
Datum: 2024-07-16	Copyright:Trenz Electronic GmbH	Page 6 of 39
Filename: Power Diagram.SchDoc		



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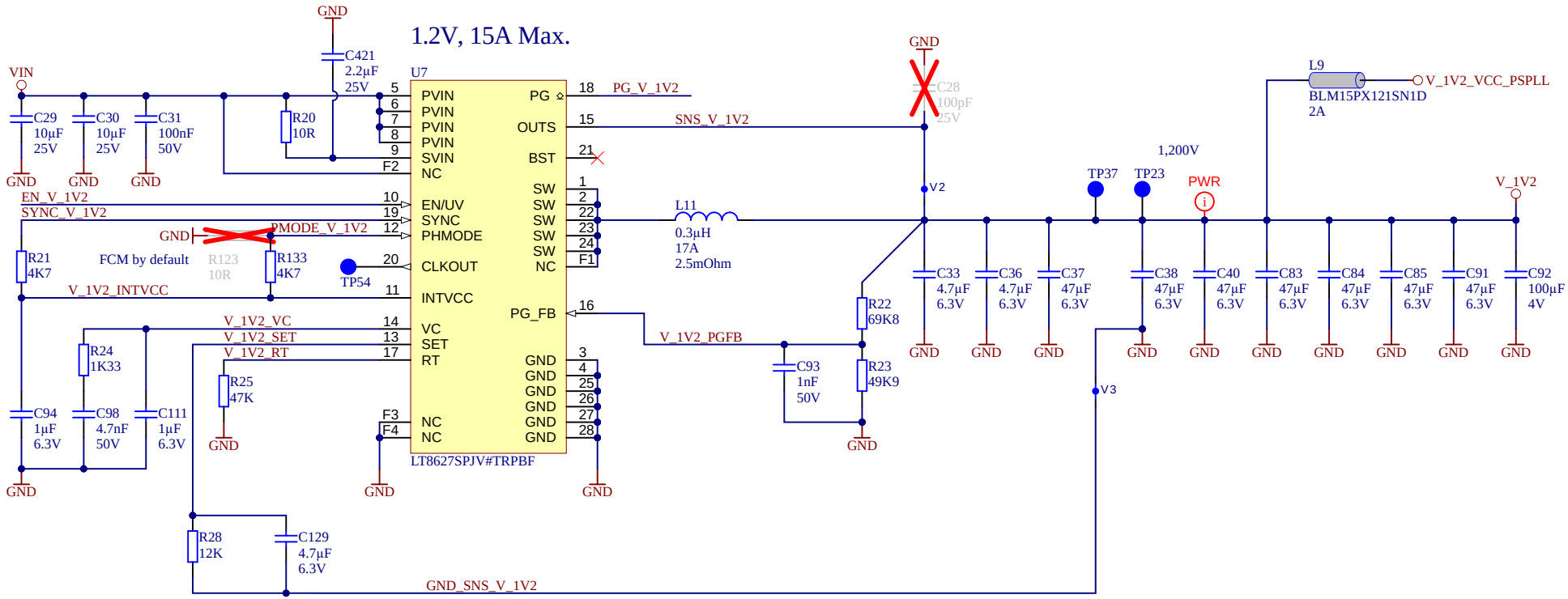
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2024-07-17	Copyright: Trenz Electronic GmbH		Page 7 of 39
Filename: POWER_IO_1V8.SchDoc			



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	A4	Number: TE0835 TXE81-A	Rev. 03
	Date: 2024-07-17	Copyright: Trenz Electronic GmbH	Page 8 of 39
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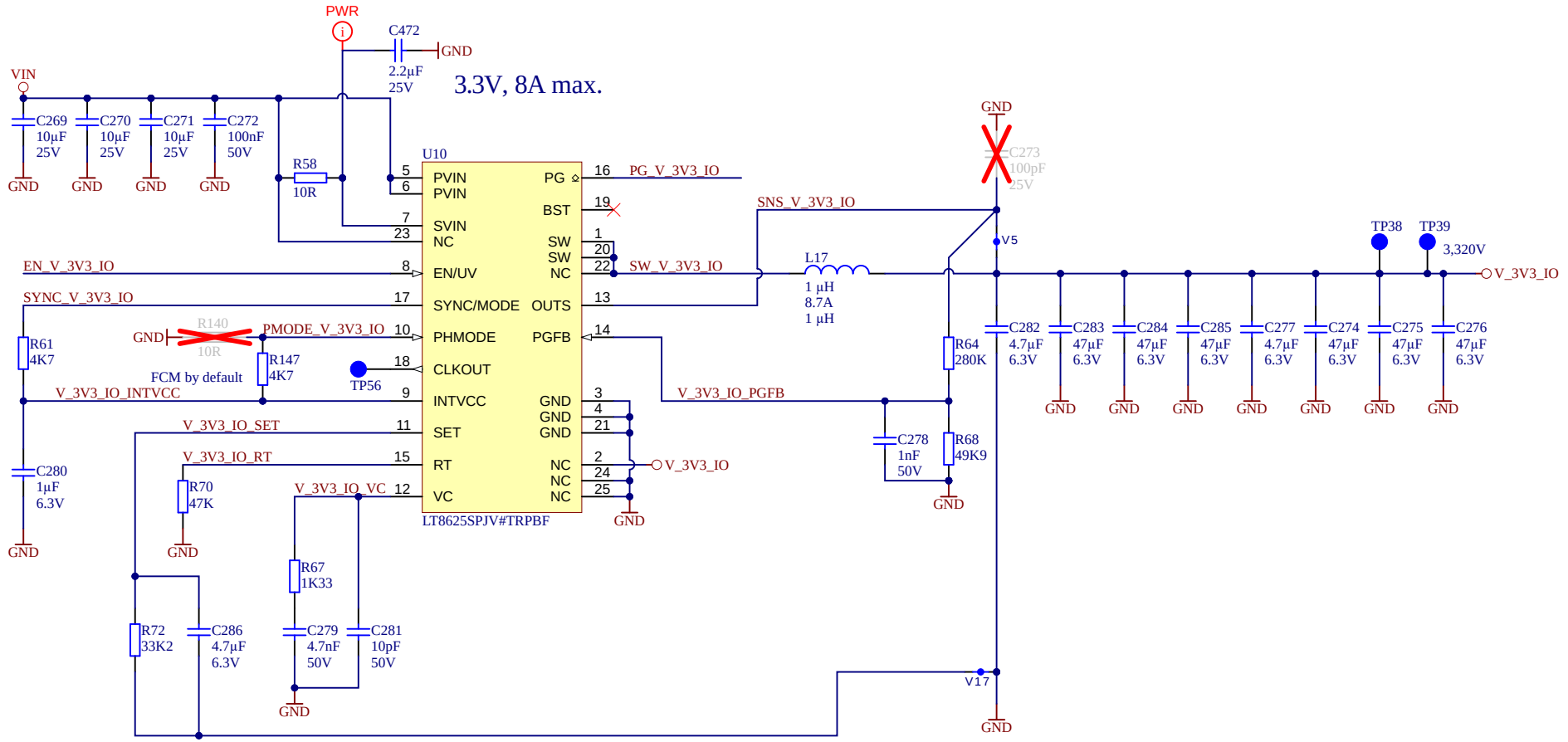

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A4	Number: TE0835 TXE81-A		Rev. 03
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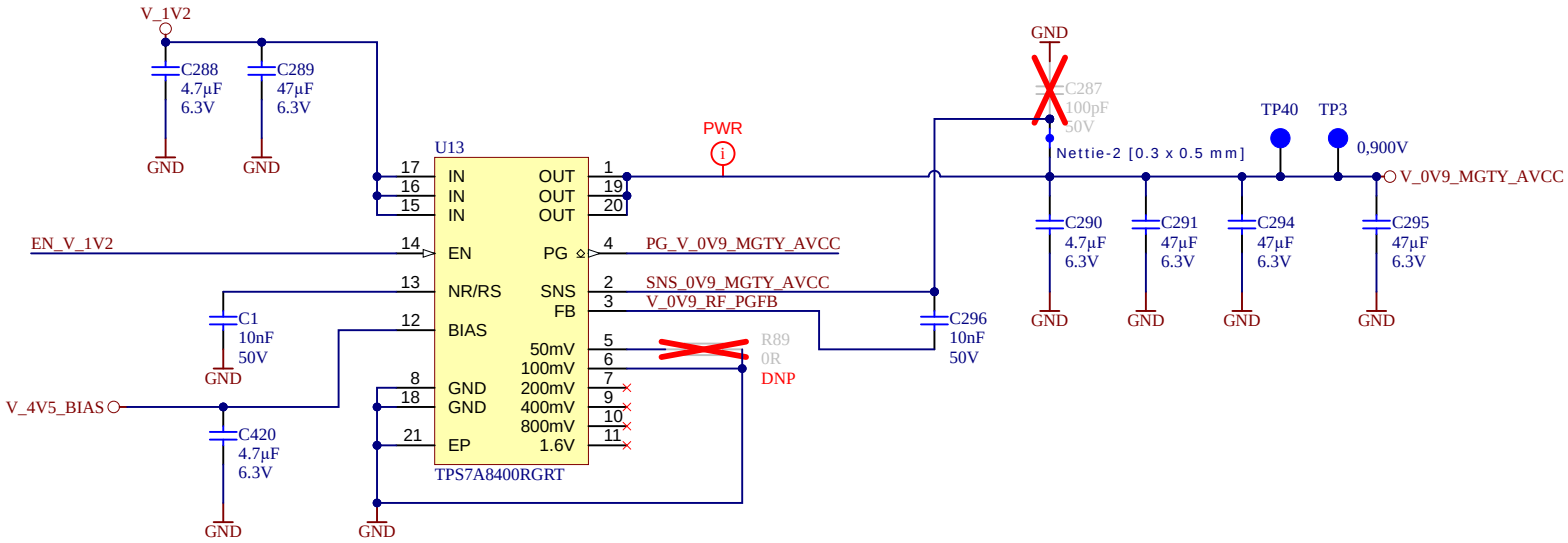
Filename: POWER_IO_3V3.SchDoc			

V_0V9_MGTAVCC, 2.5A Max



Title: POWER_MGT			
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2024-07-16	Copyright: Trenz Electronic GmbH		Page 10 of 39
Filename: POWER_MGT.SchDoc			

V_0V925_DAC_AVCC, (0.12 - 4.6A) + V_0V925_ADC_AVCC, (1.2 - 2.3A) ==> 1.32 - 6.9 A

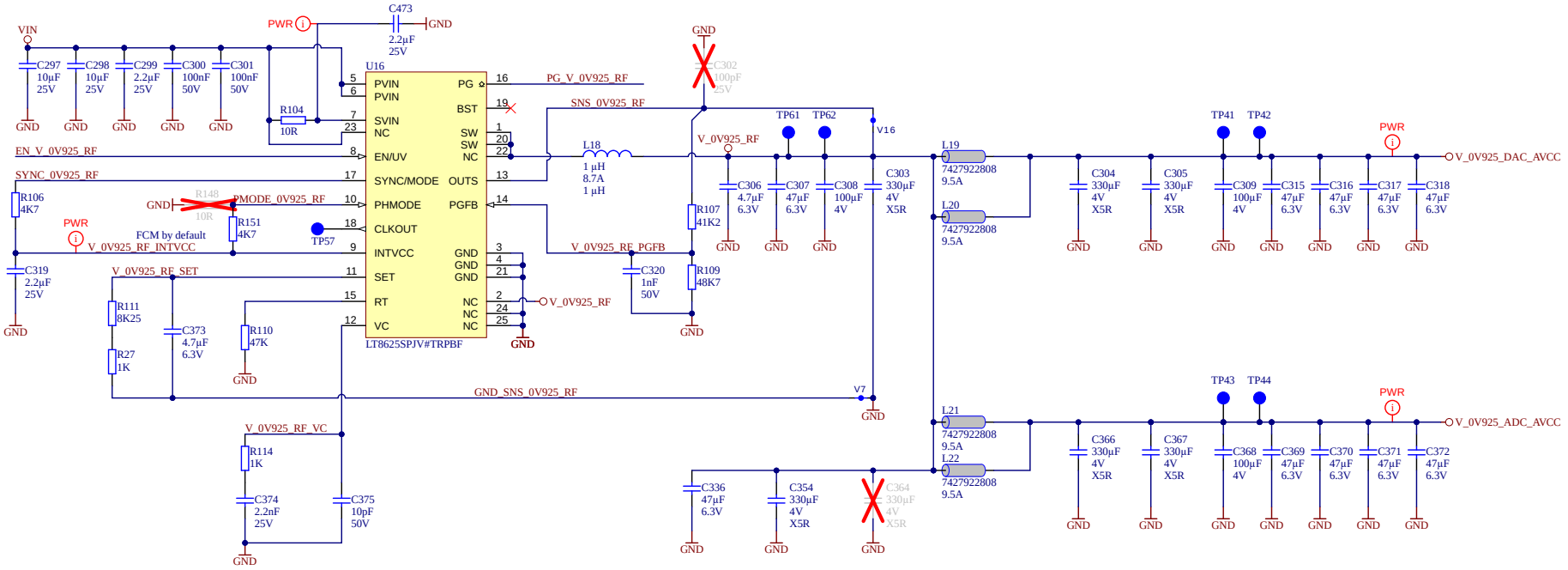
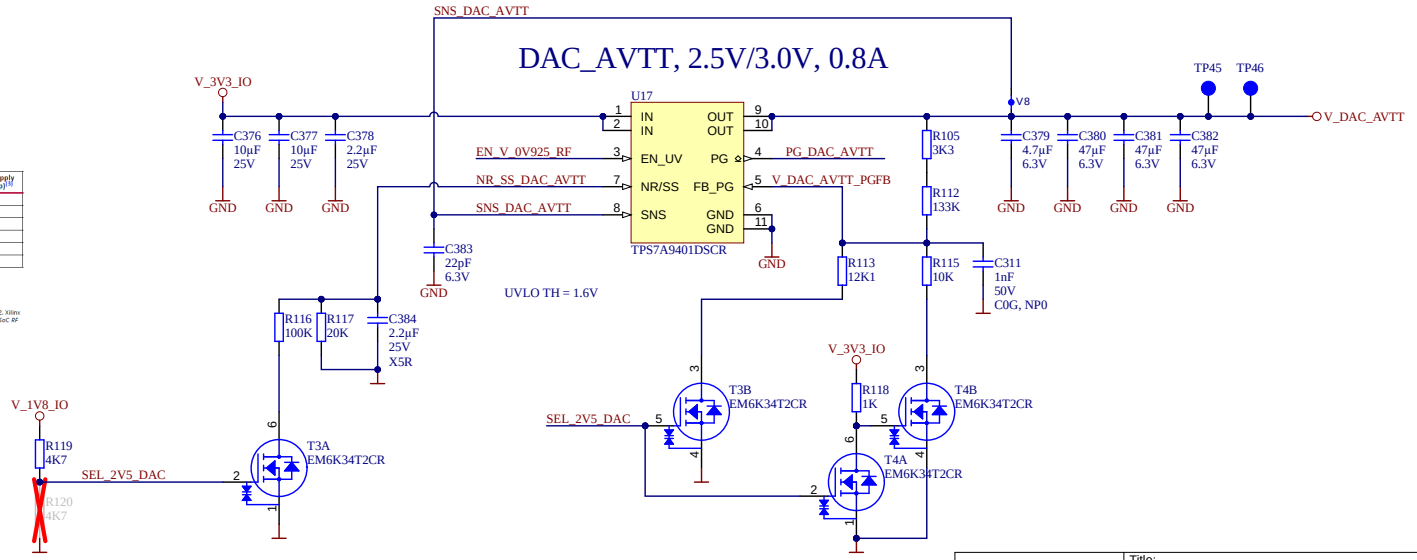


Table 3-11: ADC and DAC Voltage Supply Specifications for Gen 3 Devices[1]

Supply	Nominal Voltage (V)	Tolerance (%)[2]	Frequency Range (MHz)	Maximum Supply Ripple (mVpp)[3]
ADC_AVCC	0.925	±3	0.1–15	0.25
ADC_AVCCAUX	1.8	±3	0.1–15	1.2
DAC_AVCC	0.925	±3	0.1–15	0.32
DAC_AVCCAUX	1.8	±3	0.1–15	1.0
DAC_AVTT	2.5/3.0[4]	±3	0.1–15	2.0
VCCINT_AMS	0.85	±3	0.1–15	20.0

Notes:
1. For the maximum current, refer to the Xilinx Power Estimator (XPE) tool.
2. The tolerance percentage is for the switching regulator that feeds the VRM.
3. Output of the VRM.
4. DAC_AVTT should be set to 2.5V if used in 20 mA mode, and 3.0V if used in 32 mA mode in Gen 1 and Gen 2. Xilinx recommends DAC_AVTT be set to 5.0V in Gen 3 to enable the VOP function. Refer to *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide (PG269)* [Ref 17] for details and compatibility mode.

DAC_AVTT, 2.5V/3.0V, 0.8A



OUTPUT VOLTAGE 2.5V, Rnr =16.5 kOhms (default)
OUTPUT VOLTAGE 3.0V, Rnr =20.0 kOhms

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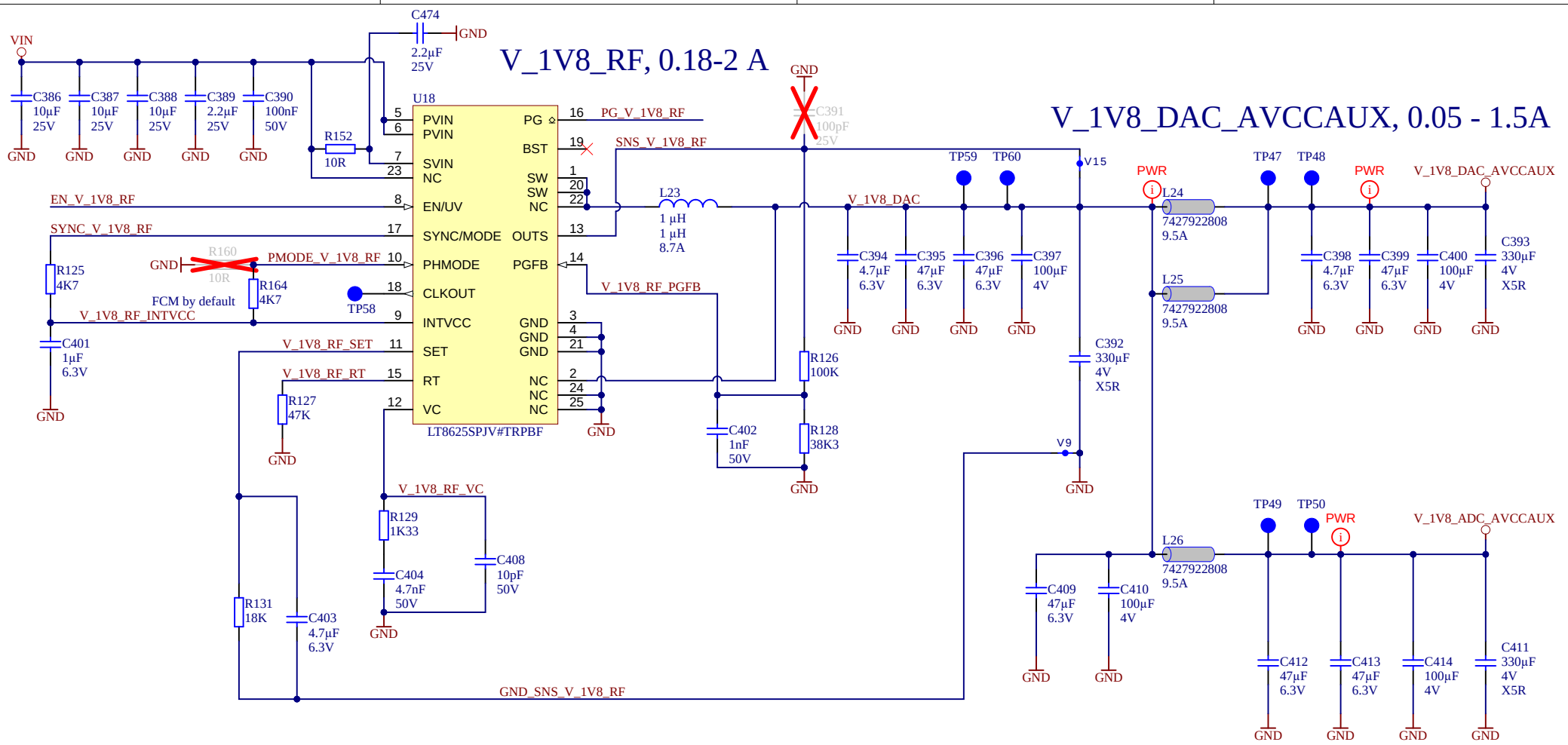
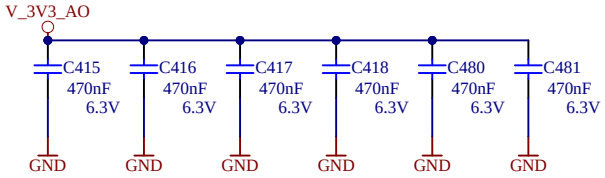
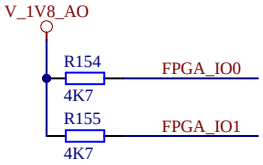
Title: POWER_RF		
A3	Nummer: TE0835 TXE81-A	Rev. 03
Datum: 2021-02-01	Copyright:Trenz Electronic GmbH	Page 11 of 39
Filename: POWER_RF.SchDoc		

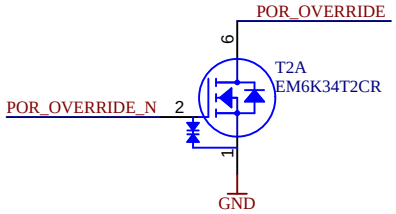


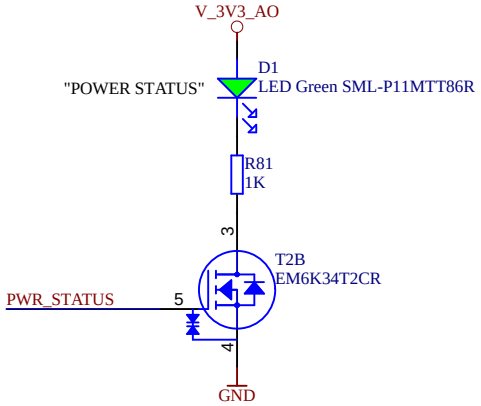
trenz electronic	Title: POWER_RF_1V8		
	A4	Number: TE0835 TXE81-A	Rev. 03
	Date: 2024-07-17	Copyright: Trenz Electronic GmbH	Page 12 of 39
	Filename: POWER_RF_1V8.SchDoc		

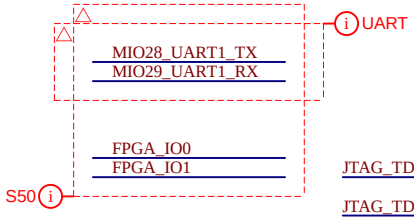
System Controller (SC)

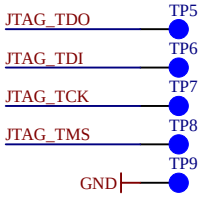


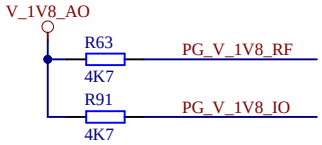


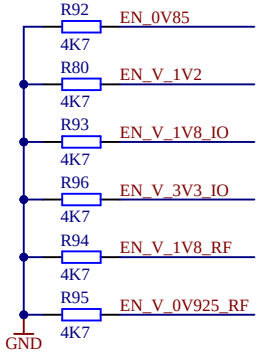


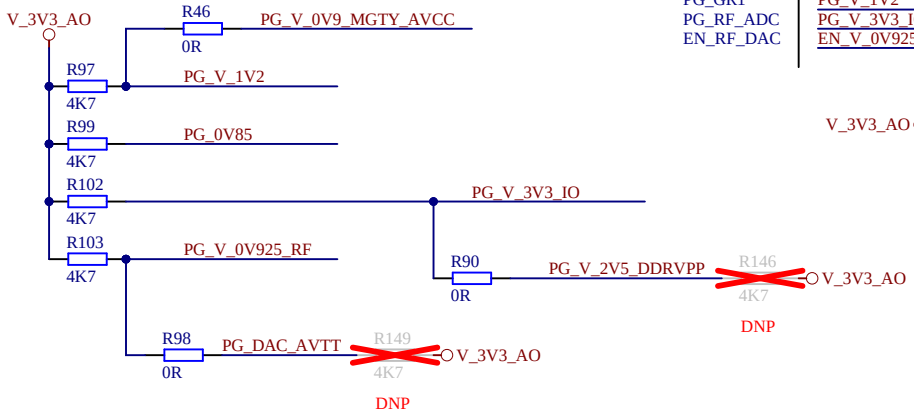










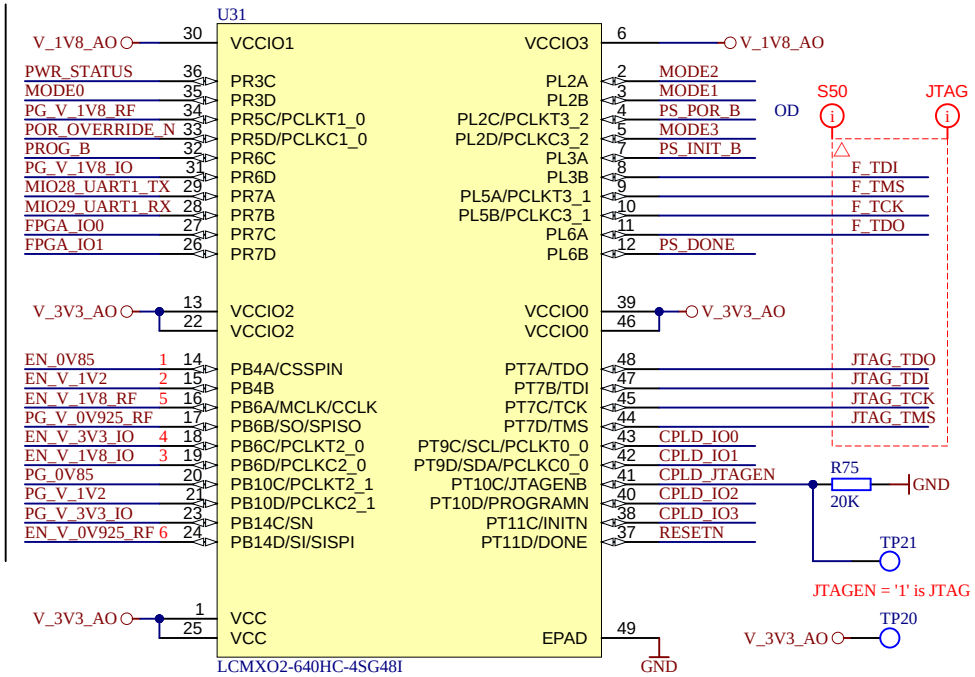


REV02
Net names:

PG_VCCRF
SRST_B

PG_GR2

EN_PS_PL
EN_GR1
EN_RF_ADC
PG_RF_DAC
EN_VCCRF
EN_GR2
PG_PS_PL
PG_GR1
PG_RF_ADC
EN_RF_DAC



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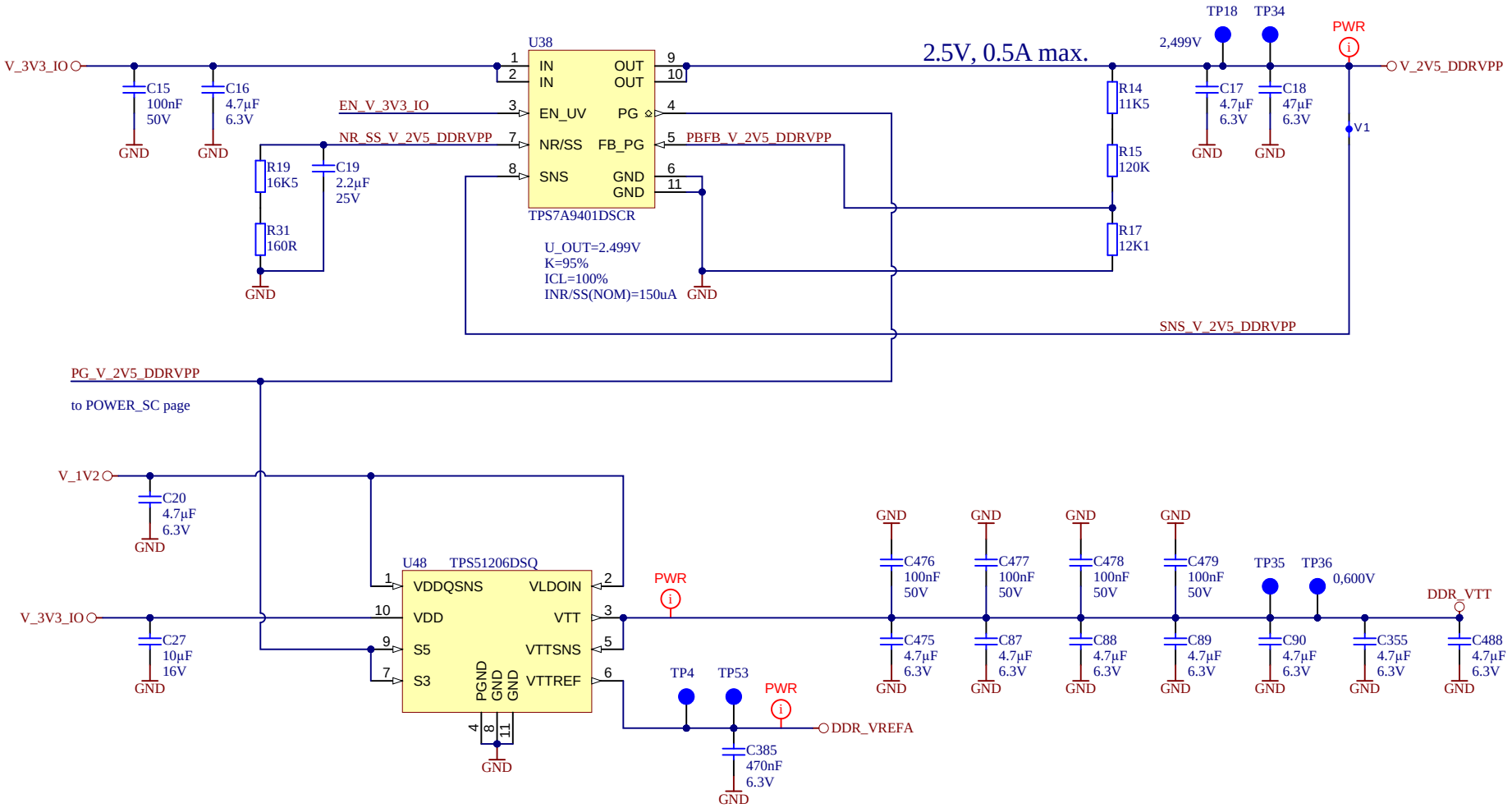
	Date: 2024-07-16	Copyright: Trenz Electronic GmbH	Page 13 of 39
	Filename: SC.SchDoc		



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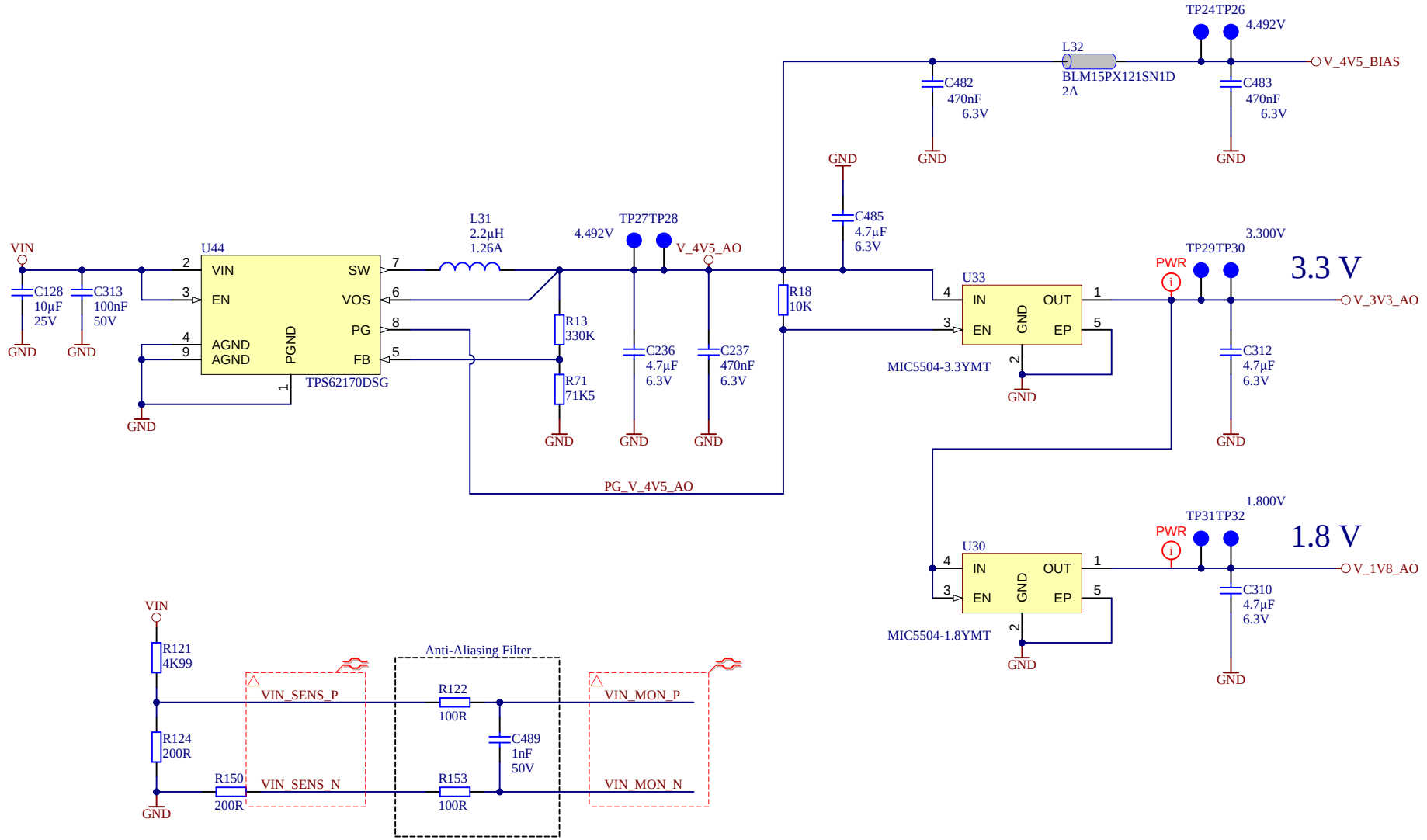
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 14 of 39
Filename: POWER_DDR.SchDoc			



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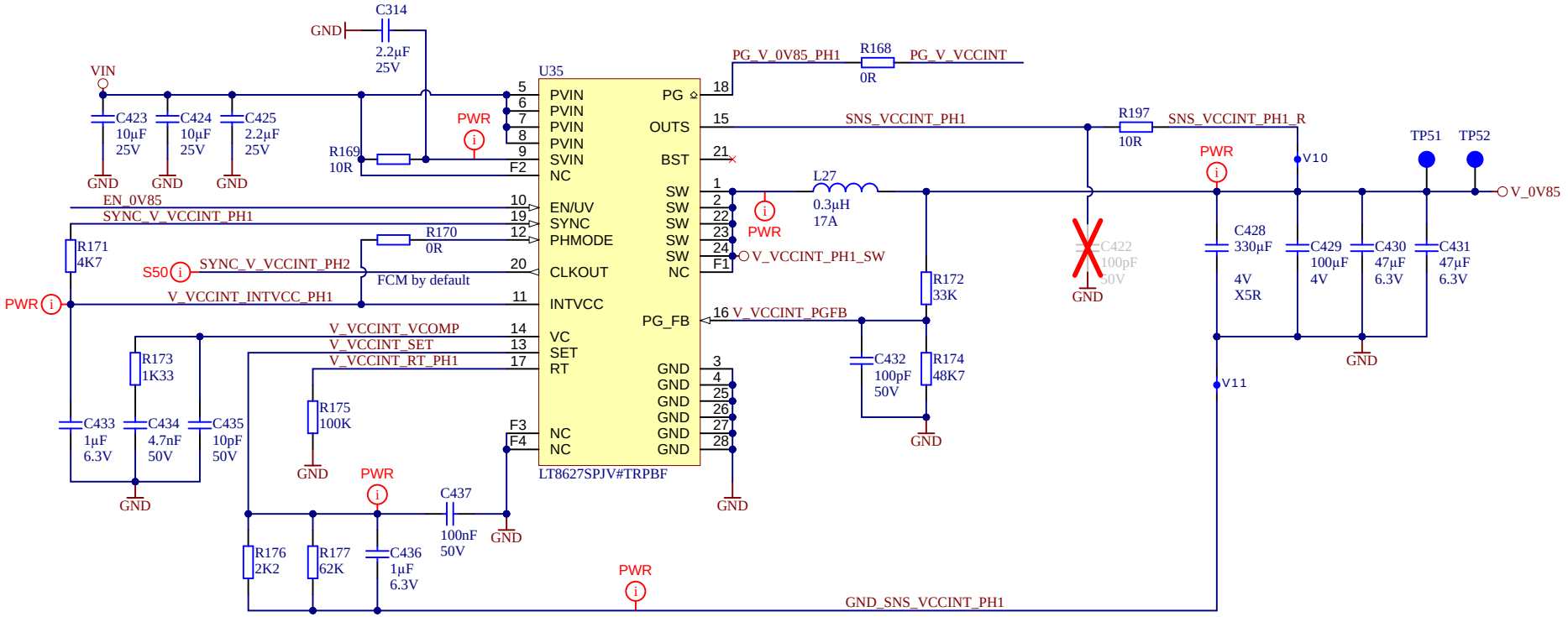
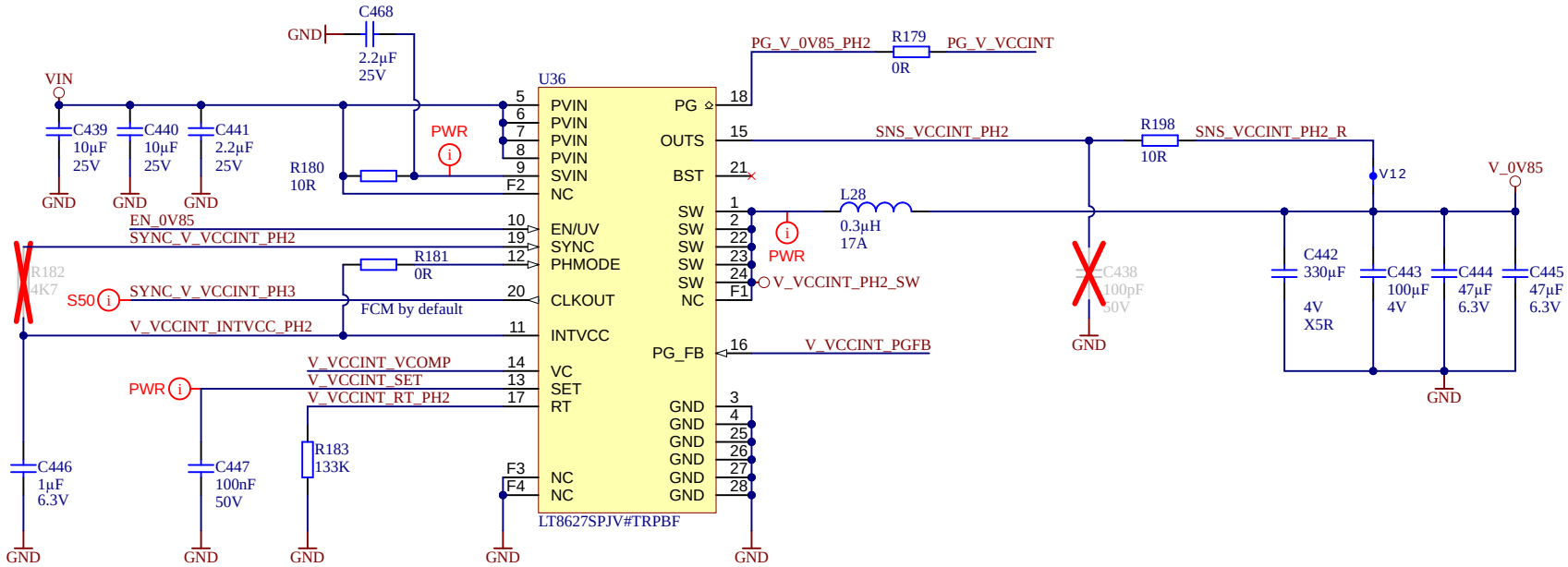
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2024-07-17	Copyright: Trenz Electronic GmbH		Page 15 of 39
Filename: POWER_STDBY_BIAS.SchDoc			

VCCINT Phase 1/4, 0.85V, 45A, 15A per Phase



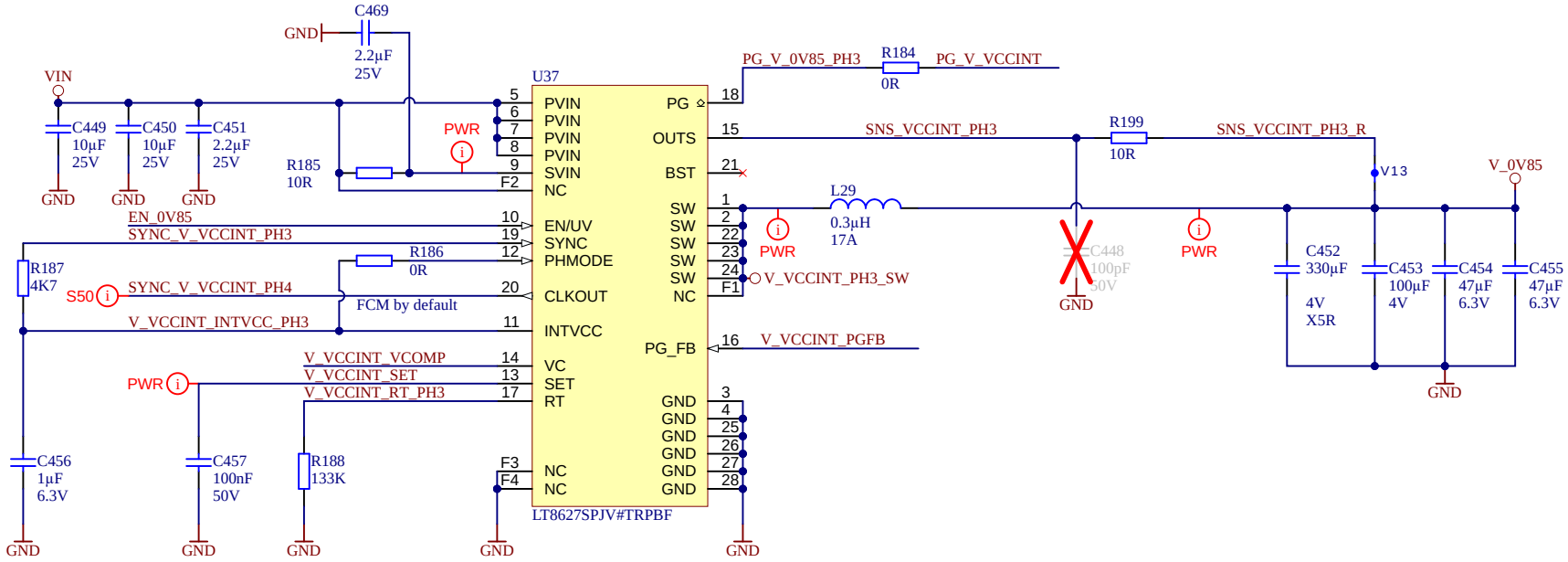
Title: POWER_VCCINT_PH1			
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2024-07-17	Copyright: Trenz Electronic GmbH		Page 16 of 39
Filename: POWER_VCCINT_PH1.SchDoc			

VCCINT Phase 2/4, 0.85V, 45A, 15A per Phase



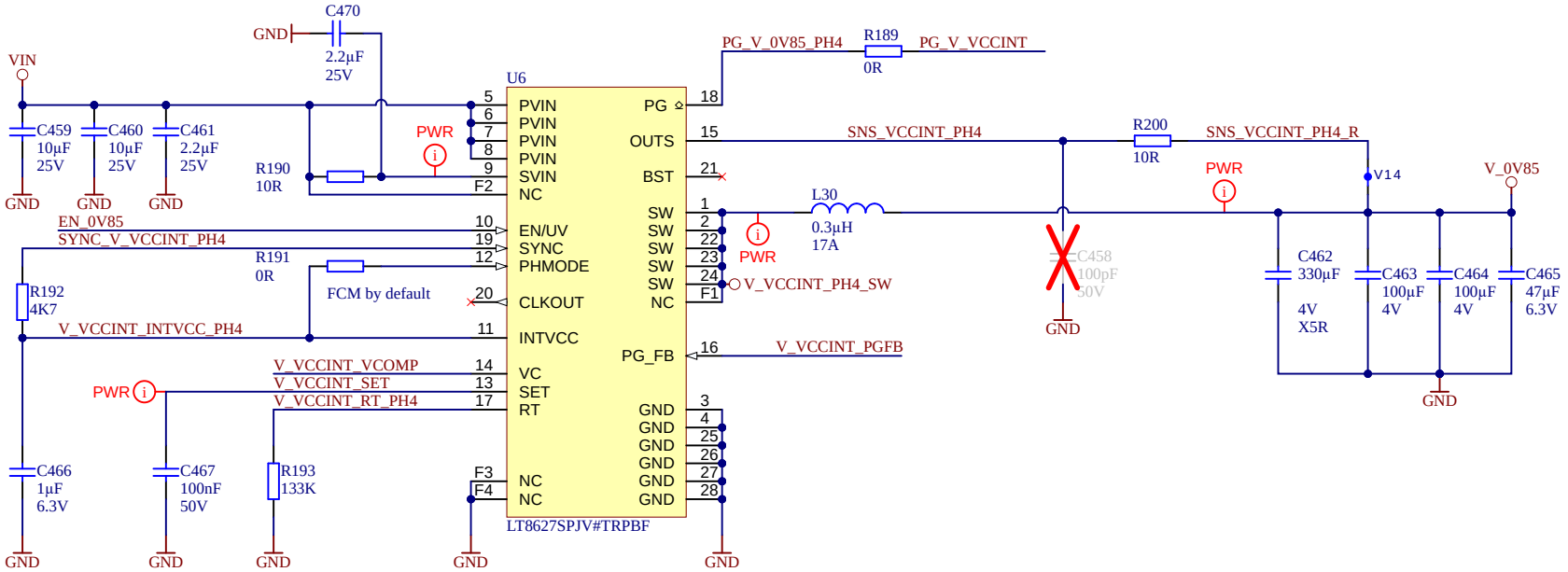
trenz electronic	Title: POWER_VCCINT_PH2		
	A4	Number: TE0835 TXE81-A	Rev. 03
	Date: 2024-07-17	Copyright: Trenz Electronic GmbH	Page 17 of 39
	Filename: POWER_VCCINT_PH2.SchDoc		

VCCINT Phase 3/4, 0.85V, 45A, 15A per Phase

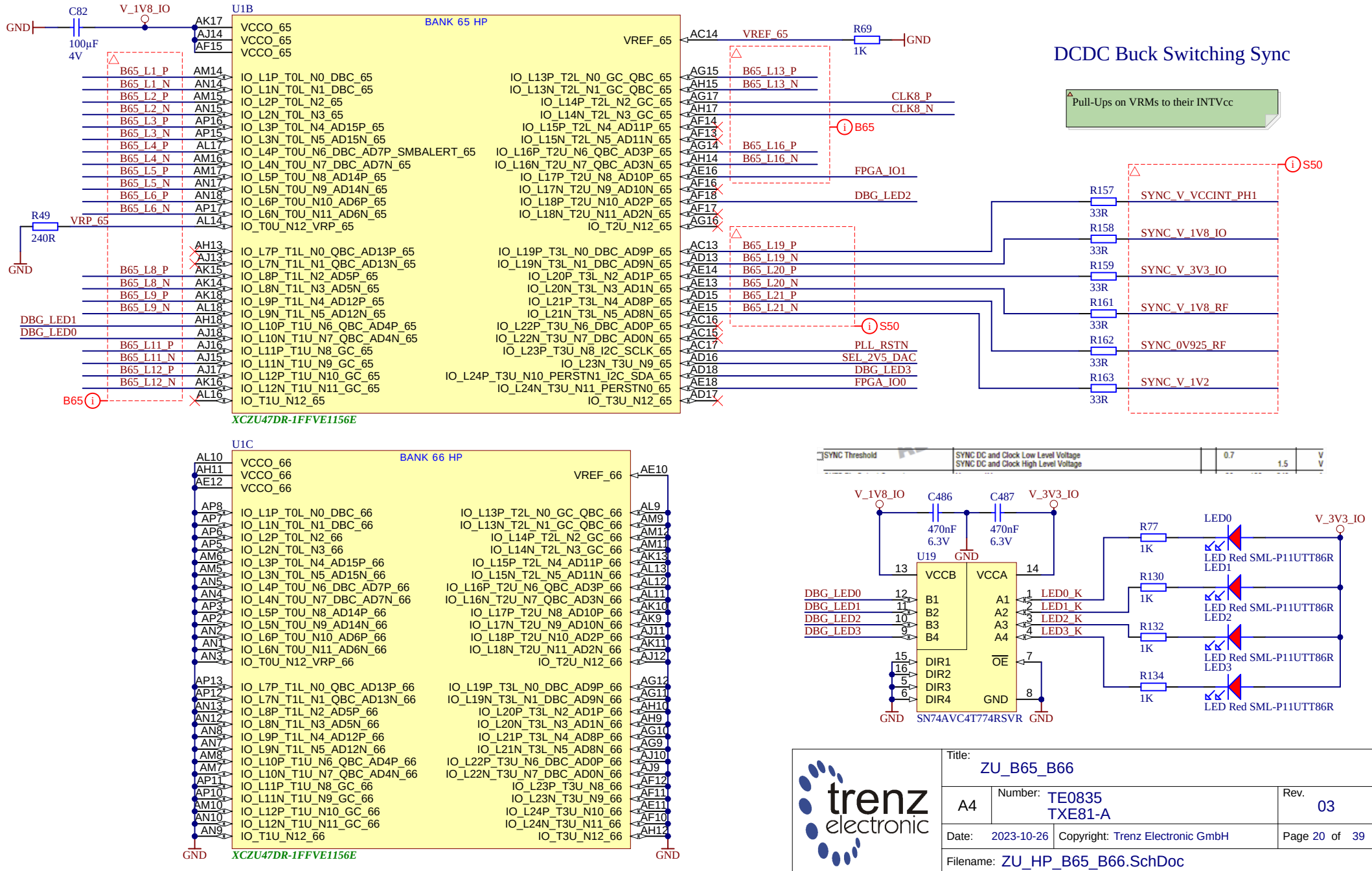


trenz electronic	Title: POWER_VCCINT_PH3		
	A4	Number: TE0835 TXE81-A	Rev. 03
	Date: 2024-07-17	Copyright: Trenz Electronic GmbH	Page 18 of 39
	Filename: POWER_VCCINT_PH3.SchDoc		

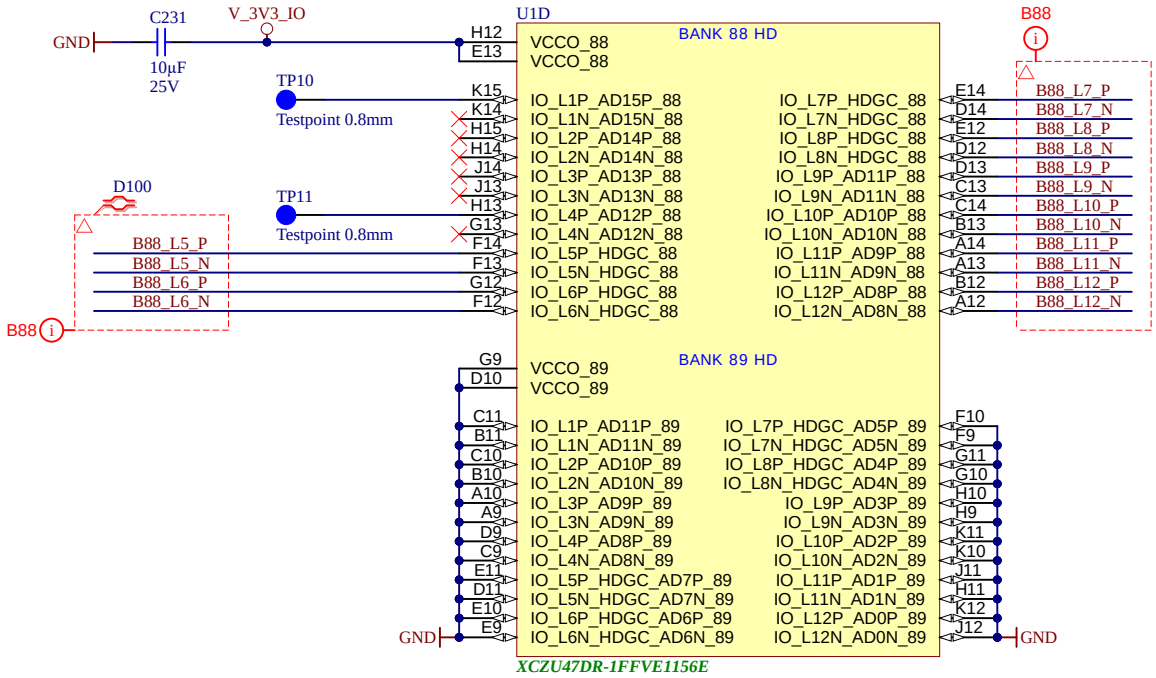
VCCINT Phase 4/4, 0.85V, 45A, 15A per Phase



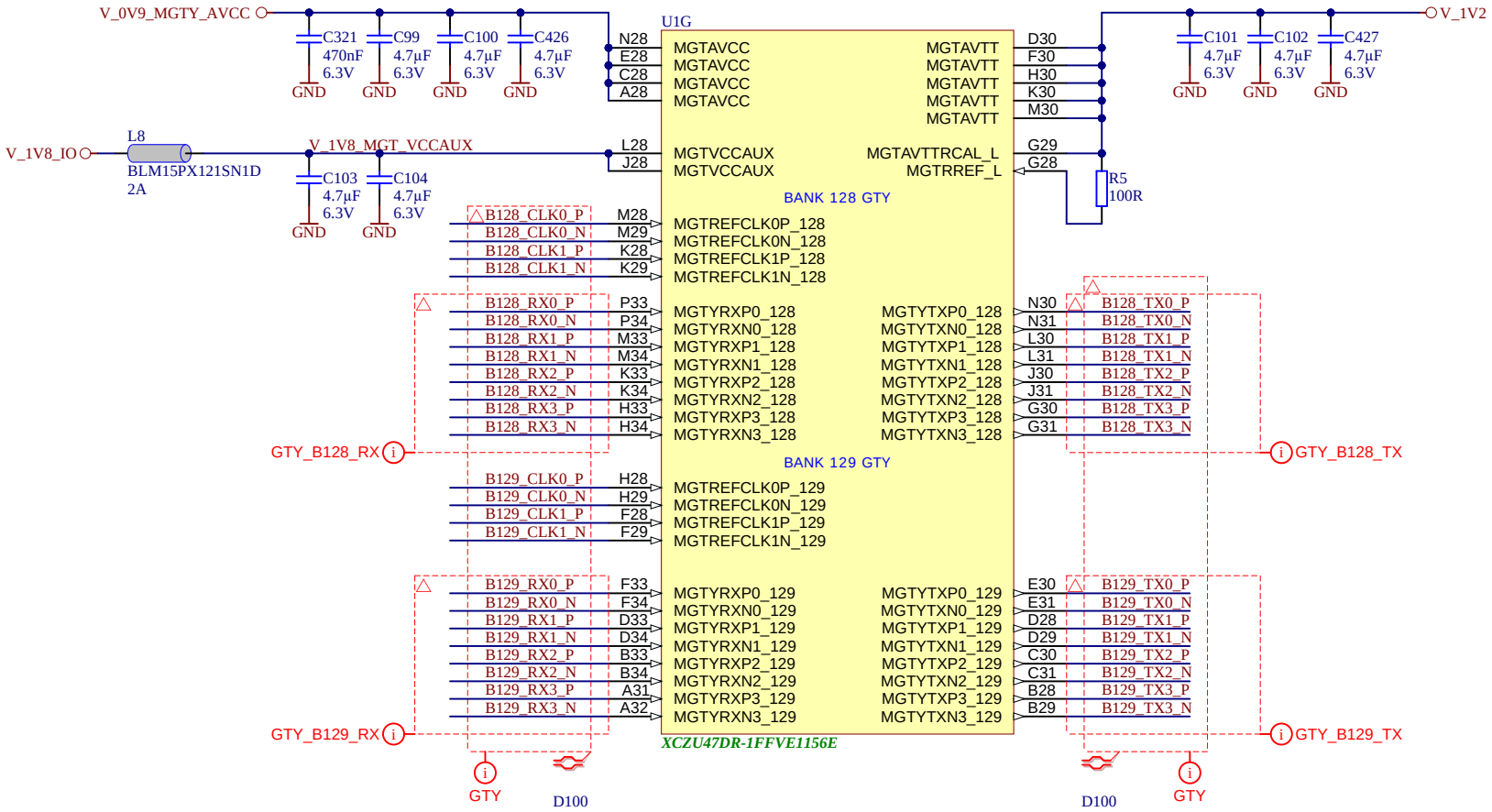
trenz electronic	Title: POWER_VCCINT_PH4		
	A4	Number: TE0835 TXE81-A	Rev. 03
	Date: 2024-07-17	Copyright: Trenz Electronic GmbH	Page 19 of 39
	Filename: POWER_VCCINT_PH4.SchDoc		



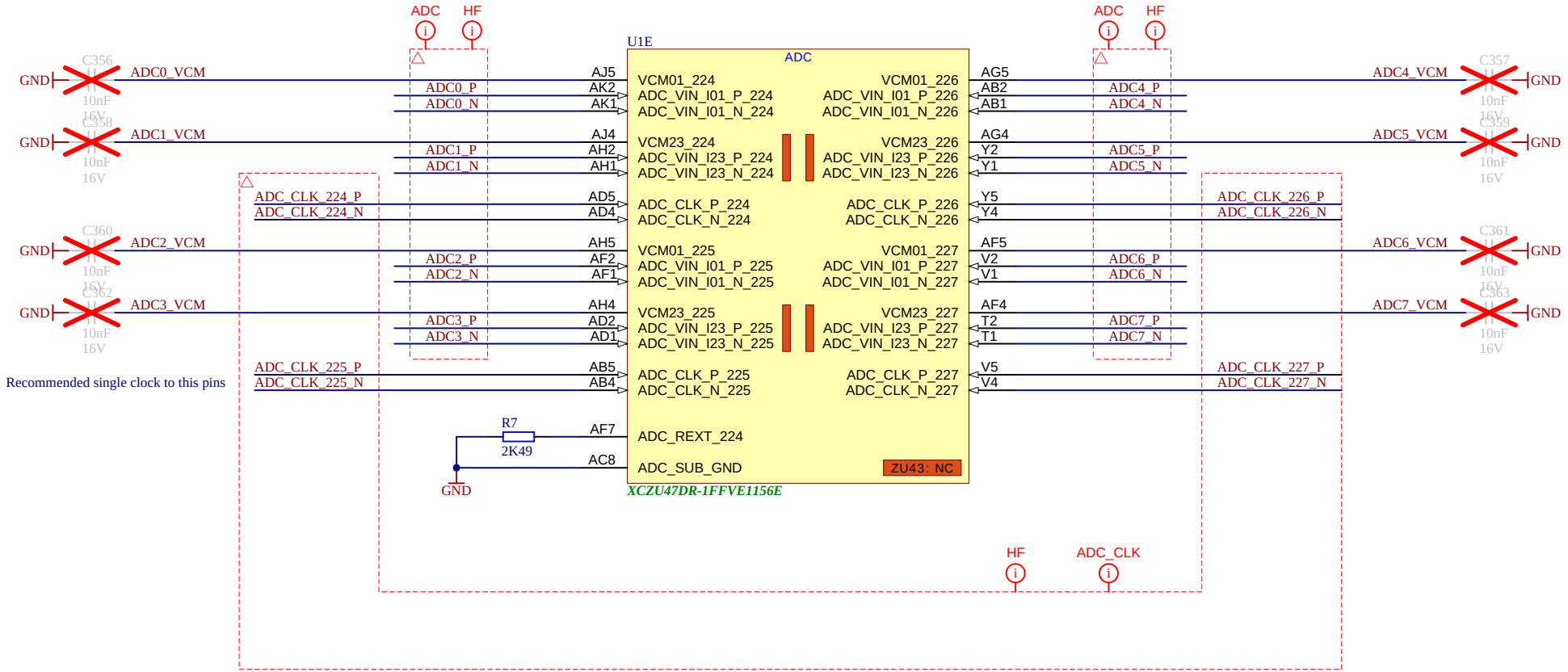
Title: ZU_B65_B66			
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 20 of 39
Filename: ZU_HP_B65_B66.SchDoc			



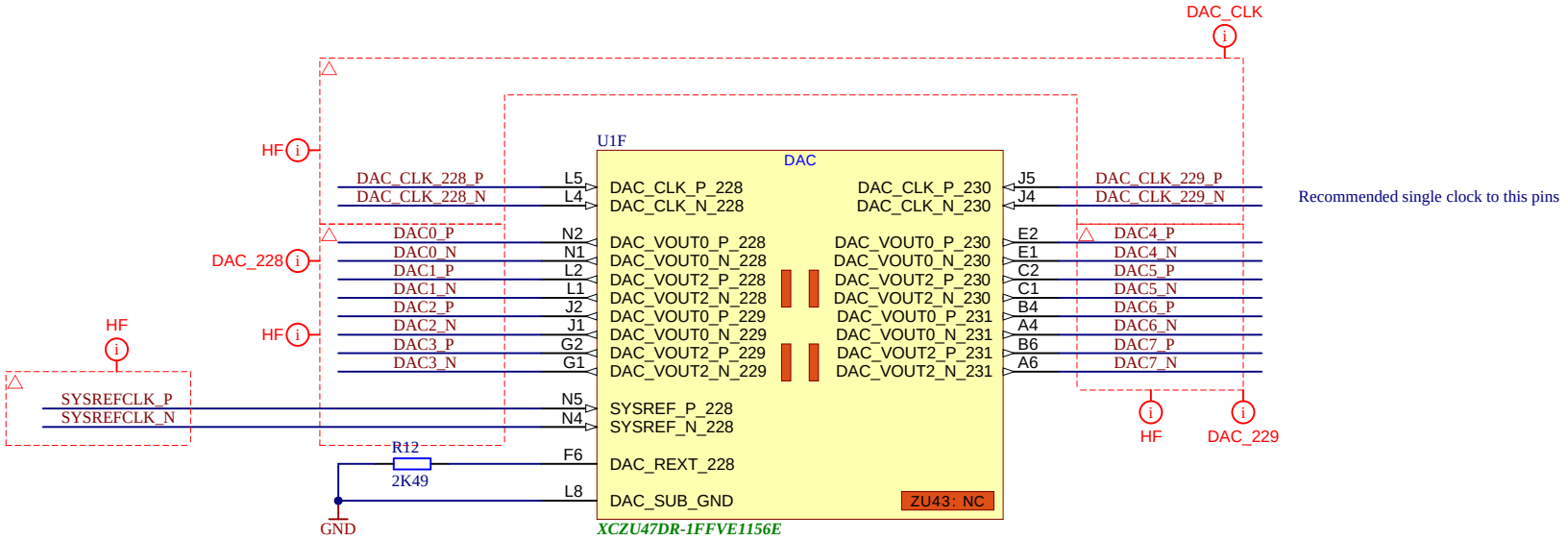
Title: ZU_HD			
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 21 of 39
Filename: ZU_HD_B88_B89.SchDoc			



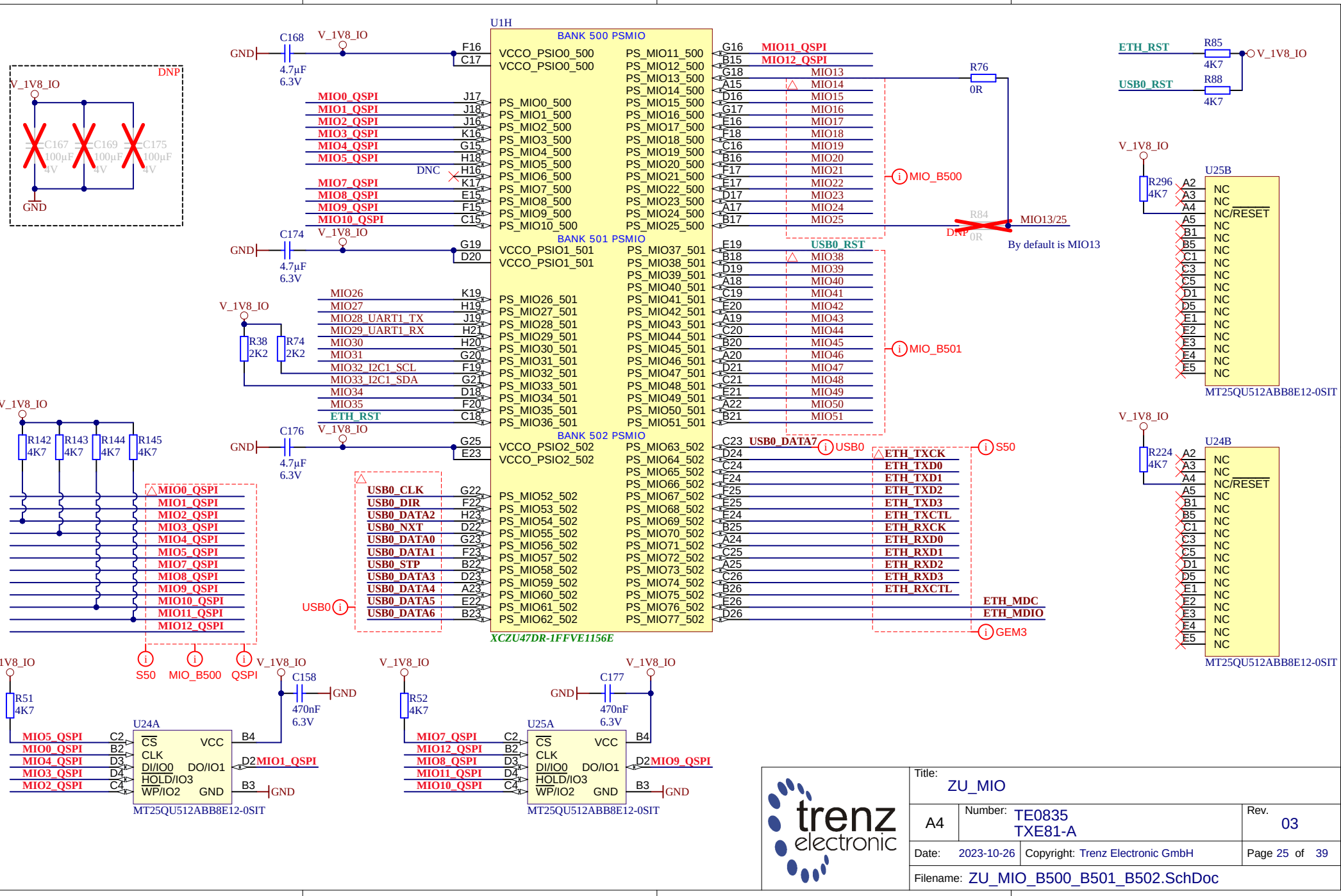
trenz electronic	Title: ZU_MGT_L		
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 22 of 39
Filename: ZU_MGT_B128_B129.SchDoc			

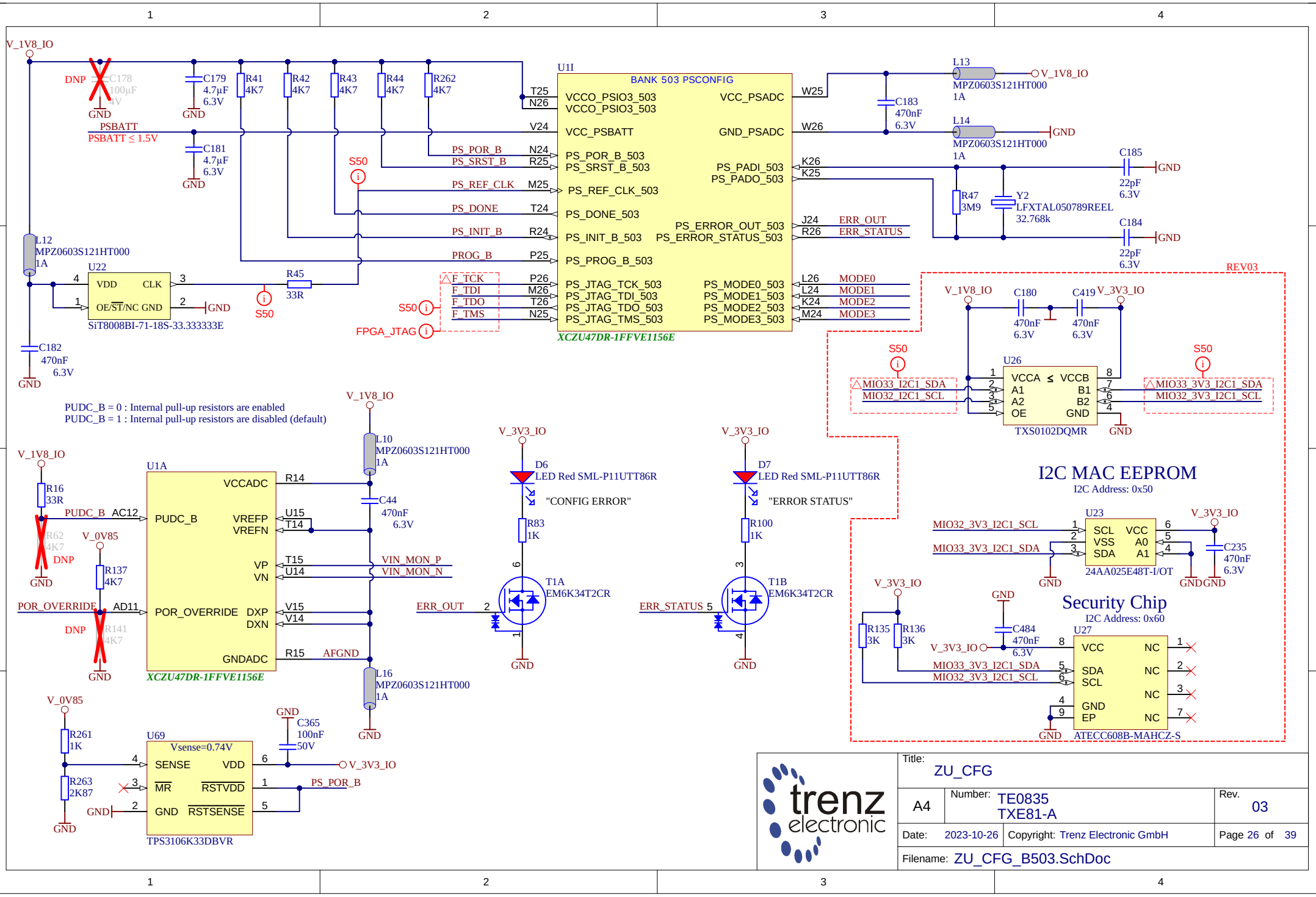


Title: ZU_ADC			
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 23 of 39
Filename: ZU_ADC_B224_B225_B226_B227.SchDoc			

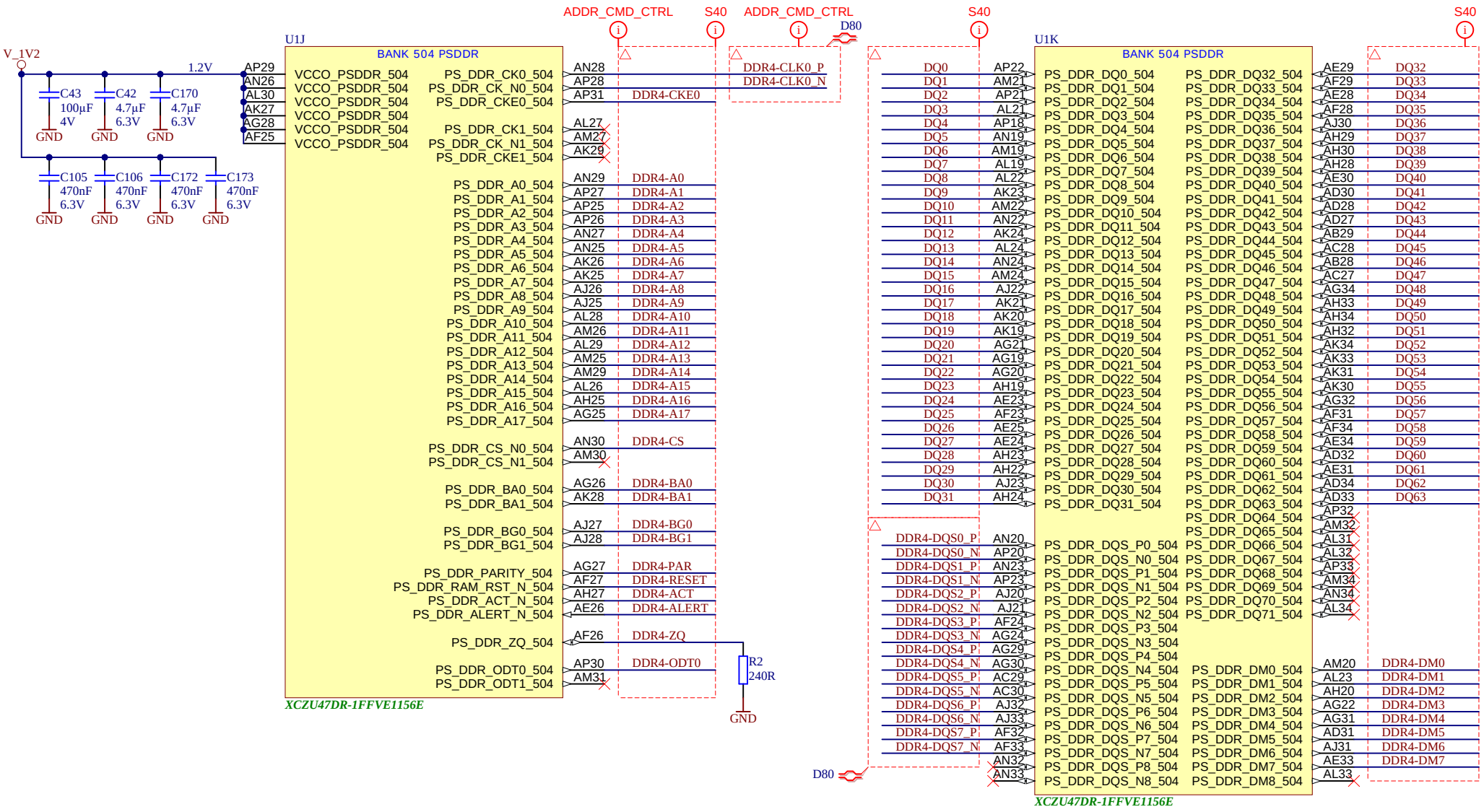


Title: ZU_DAC			
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 24 of 39
Filename: ZU_DAC_B228_B229.SchDoc			


U1H
BANK 500 PSMIO
BANK 501 PSMIO
BANK 502 PSMIO
XCZU47DR-1FFVE1156E
C168
C174
C176
C158
C177
R76
0R
R84
DNP
MIO13/25
By default is MIO13
MIO_B500
MIO_B501
USB0_RST
ETH_RST
R85
R88
4K7
R38
R74
2K2
R142
R143
R144
R145
R51
R52
R296
R224
U24A
U25A
U25B
U24B
MT25QU512ABB8E12-0SIT
S50
QSPI
USB0
GEM3
ETH_MDC
ETH_MDIO
Title:
ZU_MIO
A4
Number:
TE0835
TXE81-A
Rev.
03
Date:
2023-10-26
Copyright:
Trenz Electronic GmbH
Page 25 of 39
Filename:
ZU_MIO_B500_B501_B502.SchDoc



Title: ZU_CFG			
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 26 of 39
Filename: ZU_CFG_B503.SchDoc			


V_1V2
1.2V
C43 100µF 4V
C42 4.7µF 6.3V
C170 4.7µF 6.3V
C105 470nF 6.3V
C106 470nF 6.3V
C172 470nF 6.3V
C173 470nF 6.3V
GND
U1J
BANK 504 PSDDR
VCCO_PSDDR_504
AP29
AN26
AL30
AK27
AG28
AF25
PS_DDR_CK0_504
PS_DDR_CK_N0_504
PS_DDR_CKE0_504
PS_DDR_CK1_504
PS_DDR_CK_N1_504
PS_DDR_CKE1_504
PS_DDR_A0_504
PS_DDR_A1_504
PS_DDR_A2_504
PS_DDR_A3_504
PS_DDR_A4_504
PS_DDR_A5_504
PS_DDR_A6_504
PS_DDR_A7_504
PS_DDR_A8_504
PS_DDR_A9_504
PS_DDR_A10_504
PS_DDR_A11_504
PS_DDR_A12_504
PS_DDR_A13_504
PS_DDR_A14_504
PS_DDR_A15_504
PS_DDR_A16_504
PS_DDR_A17_504
PS_DDR_CS_N0_504
PS_DDR_CS_N1_504
PS_DDR_BA0_504
PS_DDR_BA1_504
PS_DDR_BG0_504
PS_DDR_BG1_504
PS_DDR_PARITY_504
PS_DDR_RAM_RST_N_504
PS_DDR_ACT_N_504
PS_DDR_ALERT_N_504
PS_DDR_ZQ_504
PS_DDR_ODT0_504
PS_DDR_ODT1_504
AN28
AP28
AP31 DDR4-CKE0
AL27
AM27
AK29
AN29 DDR4-A0
AP27 DDR4-A1
AP25 DDR4-A2
AP26 DDR4-A3
AN27 DDR4-A4
AN25 DDR4-A5
AK26 DDR4-A6
AK25 DDR4-A7
AJ26 DDR4-A8
AJ25 DDR4-A9
AL28 DDR4-A10
AM26 DDR4-A11
AL29 DDR4-A12
AM25 DDR4-A13
AM29 DDR4-A14
AL26 DDR4-A15
AH25 DDR4-A16
AG25 DDR4-A17
AN30 DDR4-CS
AM30
AG26 DDR4-BA0
AK28 DDR4-BA1
AJ27 DDR4-BG0
AJ28 DDR4-BG1
AG27 DDR4-PAR
AF27 DDR4-RESET
AH27 DDR4-ACT
AE26 DDR4-ALERT
AF26 DDR4-ZQ
AP30 DDR4-ODT0
AM31
XCZU47DR-1FFVE1156E
ADDR_CMD_CTRL
S40
DDR4-CLK0_P
DDR4-CLK0_N
D80
R2 240R
GND
U1K
BANK 504 PSDDR
DQ0 AP22
DQ1 AM21
DQ2 AP21
DQ3 AL21
DQ4 AP18
DQ5 AN19
DQ6 AM19
DQ7 AL19
DQ8 AL22
DQ9 AK23
DQ10 AM22
DQ11 AN22
DQ12 AK24
DQ13 AL24
DQ14 AN24
DQ15 AM24
DQ16 AJ22
DQ17 AK21
DQ18 AK20
DQ19 AK19
DQ20 AG21
DQ21 AG19
DQ22 AG20
DQ23 AH19
DQ24 AE23
DQ25 AF23
DQ26 AE25
DQ27 AE24
DQ28 AH23
DQ29 AH22
DQ30 AJ23
DQ31 AH24
DDR4-DQS0_P AN20
DDR4-DQS0_N AP20
DDR4-DQS1_P AN23
DDR4-DQS1_N AP23
DDR4-DQS2_P AJ20
DDR4-DQS2_N AJ21
DDR4-DQS3_P AF24
DDR4-DQS3_N AG24
DDR4-DQS4_P AG29
DDR4-DQS4_N AG30
DDR4-DQS5_P AC29
DDR4-DQS5_N AC30
DDR4-DQS6_P AJ32
DDR4-DQS6_N AJ33
DDR4-DQS7_P AF32
DDR4-DQS7_N AF33
AN32
AN33
PS_DDR_DQ0_504
PS_DDR_DQ1_504
PS_DDR_DQ2_504
PS_DDR_DQ3_504
PS_DDR_DQ4_504
PS_DDR_DQ5_504
PS_DDR_DQ6_504
PS_DDR_DQ7_504
PS_DDR_DQ8_504
PS_DDR_DQ9_504
PS_DDR_DQ10_504
PS_DDR_DQ11_504
PS_DDR_DQ12_504
PS_DDR_DQ13_504
PS_DDR_DQ14_504
PS_DDR_DQ15_504
PS_DDR_DQ16_504
PS_DDR_DQ17_504
PS_DDR_DQ18_504
PS_DDR_DQ19_504
PS_DDR_DQ20_504
PS_DDR_DQ21_504
PS_DDR_DQ22_504
PS_DDR_DQ23_504
PS_DDR_DQ24_504
PS_DDR_DQ25_504
PS_DDR_DQ26_504
PS_DDR_DQ27_504
PS_DDR_DQ28_504
PS_DDR_DQ29_504
PS_DDR_DQ30_504
PS_DDR_DQ31_504
PS_DDR_DQS_P0_504
PS_DDR_DQS_N0_504
PS_DDR_DQS_P1_504
PS_DDR_DQS_N1_504
PS_DDR_DQS_P2_504
PS_DDR_DQS_N2_504
PS_DDR_DQS_P3_504
PS_DDR_DQS_N3_504
PS_DDR_DQS_P4_504
PS_DDR_DQS_N4_504
PS_DDR_DQS_P5_504
PS_DDR_DQS_N5_504
PS_DDR_DQS_P6_504
PS_DDR_DQS_N6_504
PS_DDR_DQS_P7_504
PS_DDR_DQS_N7_504
PS_DDR_DQS_P8_504
PS_DDR_DQS_N8_504
PS_DDR_DQ32_504
PS_DDR_DQ33_504
PS_DDR_DQ34_504
PS_DDR_DQ35_504
PS_DDR_DQ36_504
PS_DDR_DQ37_504
PS_DDR_DQ38_504
PS_DDR_DQ39_504
PS_DDR_DQ40_504
PS_DDR_DQ41_504
PS_DDR_DQ42_504
PS_DDR_DQ43_504
PS_DDR_DQ44_504
PS_DDR_DQ45_504
PS_DDR_DQ46_504
PS_DDR_DQ47_504
PS_DDR_DQ48_504
PS_DDR_DQ49_504
PS_DDR_DQ50_504
PS_DDR_DQ51_504
PS_DDR_DQ52_504
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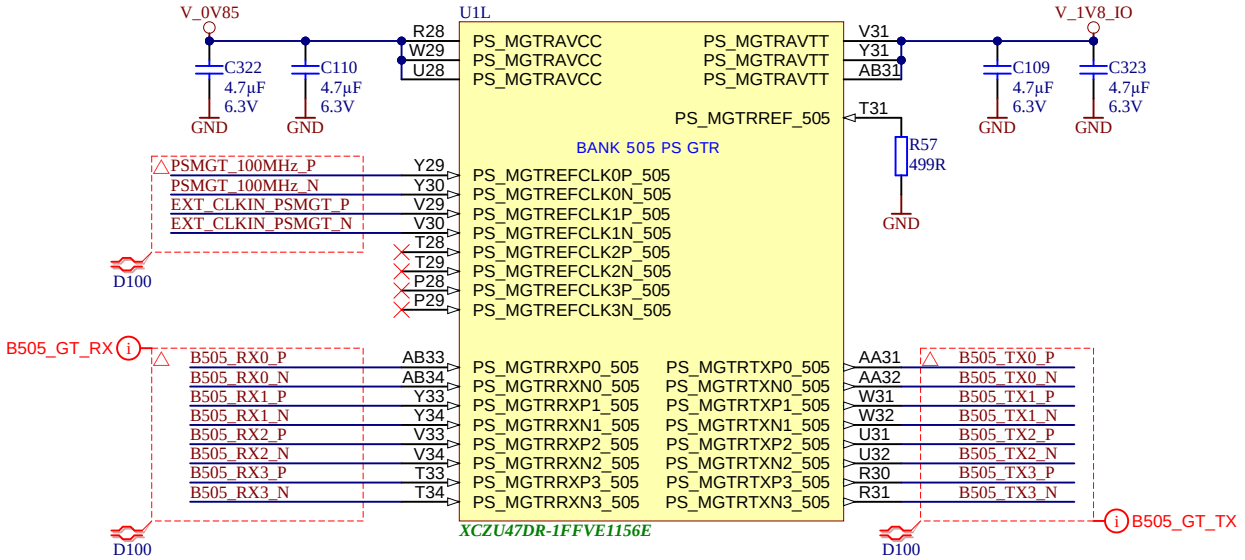
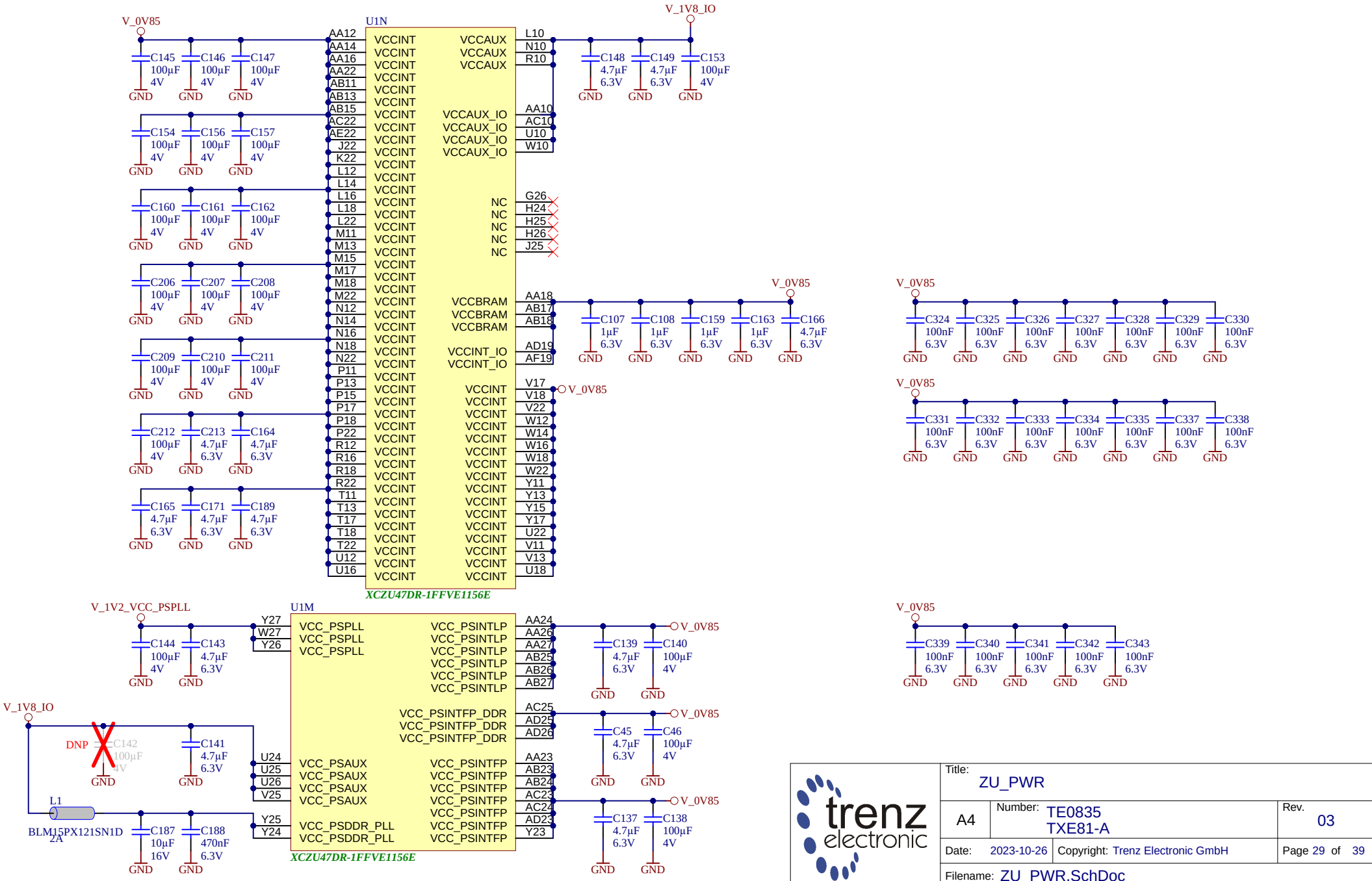
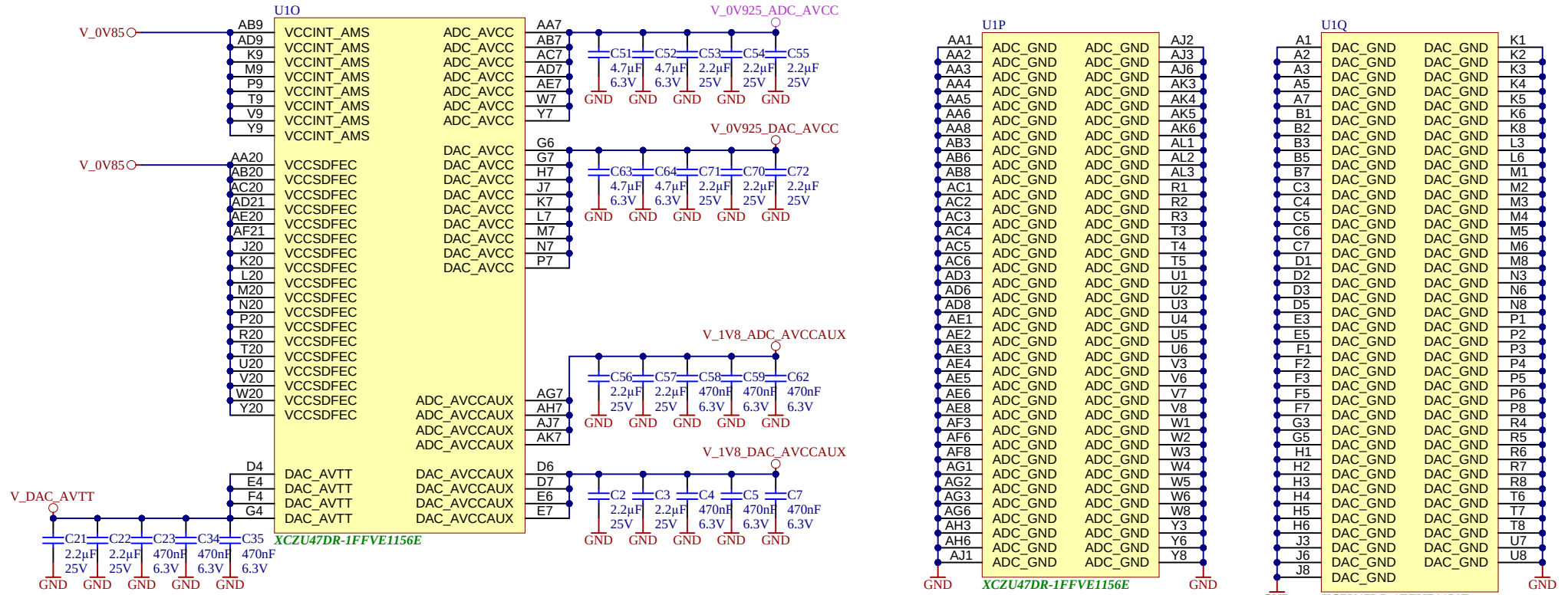
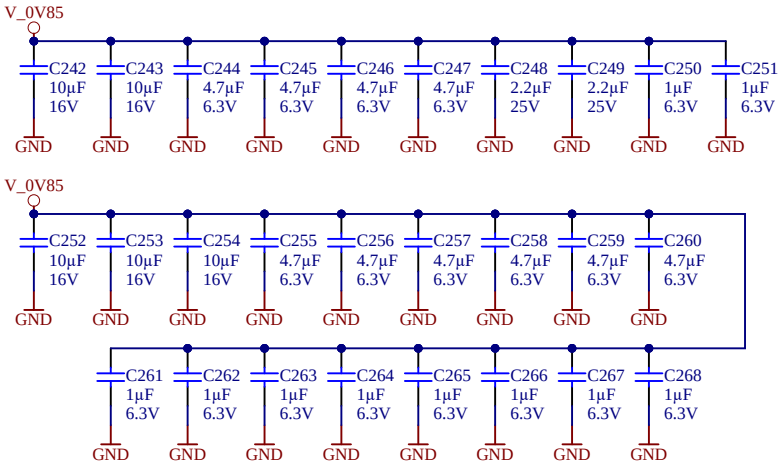
PS_DDR_DQ55_504
PS_DDR_DQ56_504
PS_DDR_DQ57_504
PS_DDR_DQ58_504
PS_DDR_DQ59_504
PS_DDR_DQ60_504
PS_DDR_DQ61_504
PS_DDR_DQ62_504
PS_DDR_DQ63_504
PS_DDR_DQ64_504
PS_DDR_DQ65_504
PS_DDR_DQ66_504
PS_DDR_DQ67_504
PS_DDR_DQ68_504
PS_DDR_DQ69_504
PS_DDR_DQ70_504
PS_DDR_DQ71_504
PS_DDR_DM0_504
PS_DDR_DM1_504
PS_DDR_DM2_504
PS_DDR_DM3_504
PS_DDR_DM4_504
PS_DDR_DM5_504
PS_DDR_DM6_504
PS_DDR_DM7_504
PS_DDR_DM8_504
AE29 DQ32
AF29 DQ33
AE28 DQ34
AF28 DQ35
AJ30 DQ36
AH29 DQ37
AH30 DQ38
AH28 DQ39
AE30 DQ40
AD30 DQ41
AD28 DQ42
AD27 DQ43
AB29 DQ44
AC28 DQ45
AB28 DQ46
AC27 DQ47
AG34 DQ48
AH33 DQ49
AH34 DQ50
AH32 DQ51
AK34 DQ52
AK33 DQ53
AK31 DQ54
AK30 DQ55
AG32 DQ56
AF31 DQ57
AF34 DQ58
AE34 DQ59
AD32 DQ60
AE31 DQ61
AD34 DQ62
AD33 DQ63
AP32
AM32
AL31
AL32
AP33
AM34
AN34
AL34
AM20 DDR4-DM0
AL23 DDR4-DM1
AH20 DDR4-DM2
AG22 DDR4-DM3
AG31 DDR4-DM4
AD31 DDR4-DM5
AJ31 DDR4-DM6
AE33 DDR4-DM7
AL33
XCZU47DR-1FFVE1156E
trenz electronic
Title: ZU_PSDDR
A4
Number: TE0835 TXE81-A
Rev. 03
Date: 2023-10-26
Copyright: Trenz Electronic GmbH
Page 27 of 39
Filename: ZU_PSDDR_B504.SchDoc

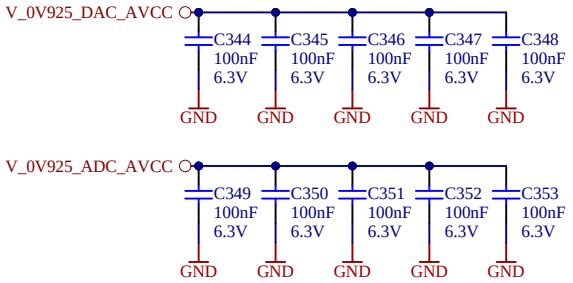


trenz electronic	Title: ZU_PSMGT		
	A4	Number: TE0835 TXE81-A	Rev. 03
	Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 28 of 39
	Filename: ZU_PSMGT_B505.SchDoc		


U1N
V_0V85
V_1V8_IO
VCCINT
VCCAUX
VCCAUX_IO
VCCBRAM
VCCINT_IO
NC
XCZU47DR-1FFVE1156E
U1M
V_1V2_VCC_PSPLL
VCC_PSPLL
VCC_PSINTLP
VCC_PSINTFP_DDR
VCC_PSAUX
VCC_PSINTFP
VCC_PSDDR_PLL
DNP
L1
BLM15PX121SN1D
2A
GND
ZU_PWR
A4
Number: TE0835 TXE81-A
Rev. 03
Date: 2023-10-26
Copyright: Trenz Electronic GmbH
Page 29 of 39
Filename: ZU_PWR.SchDoc







Title: ZU_PWR2			
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 30 of 39
Filename: ZU_PWR_RF.SchDoc			

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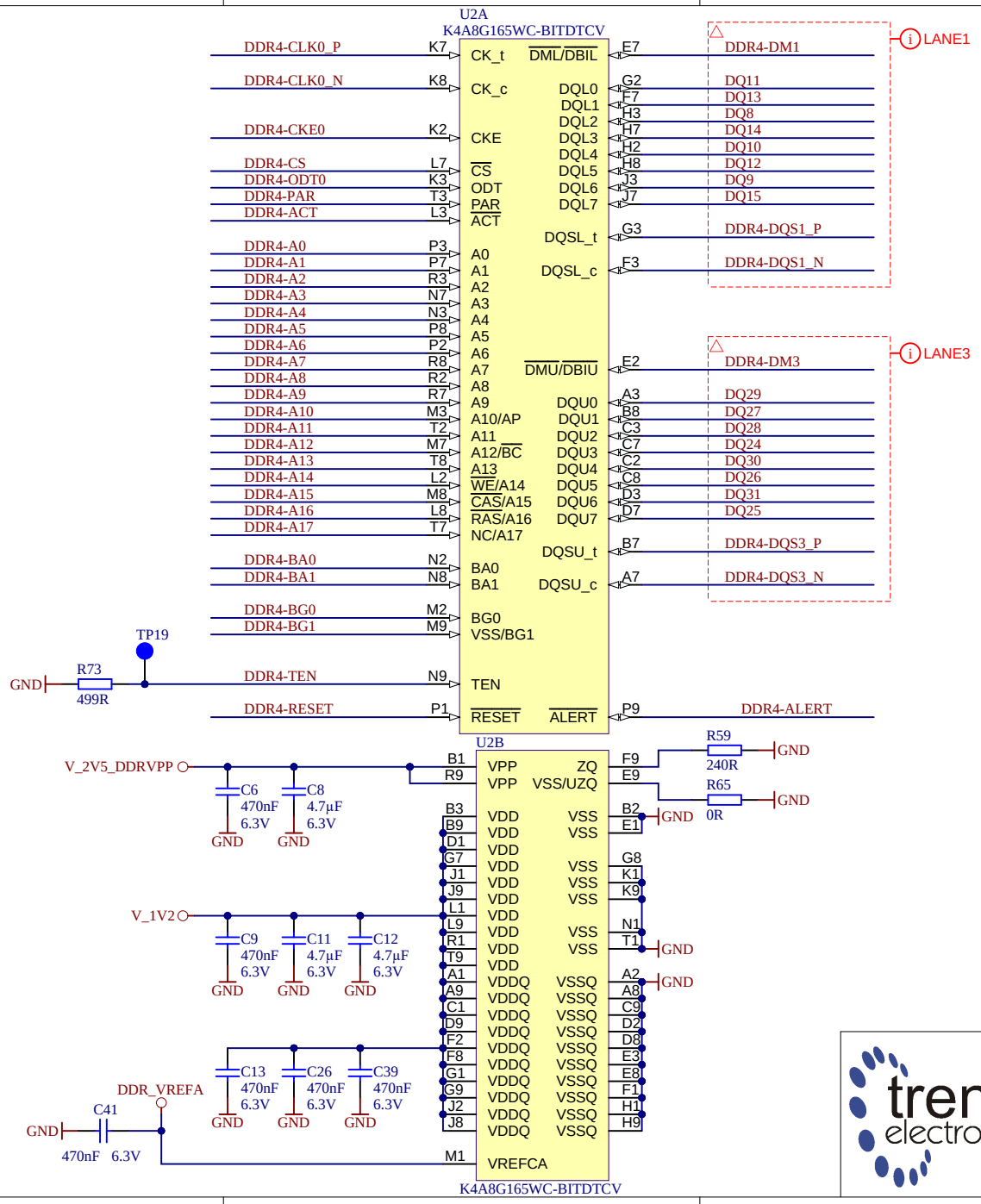
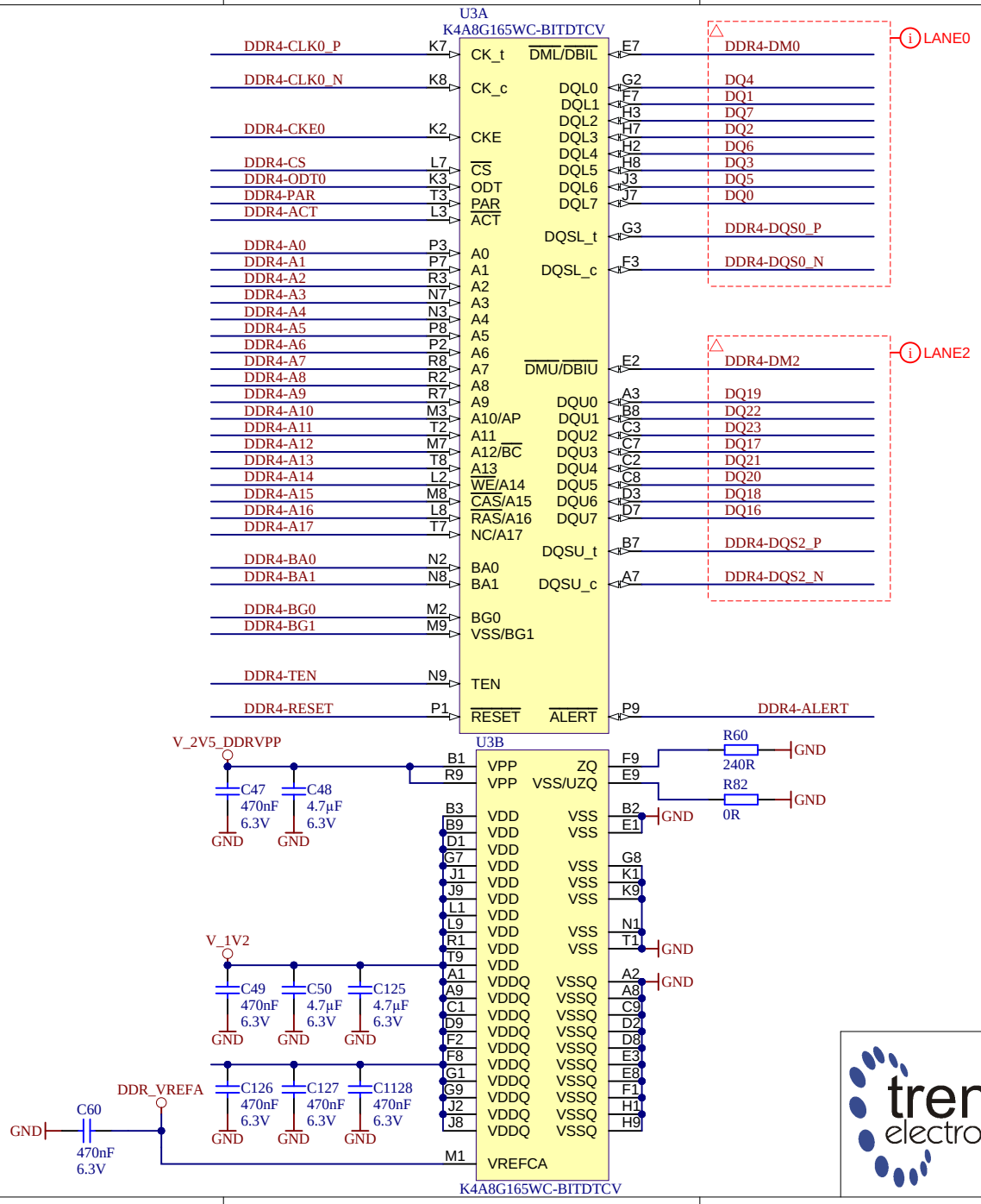
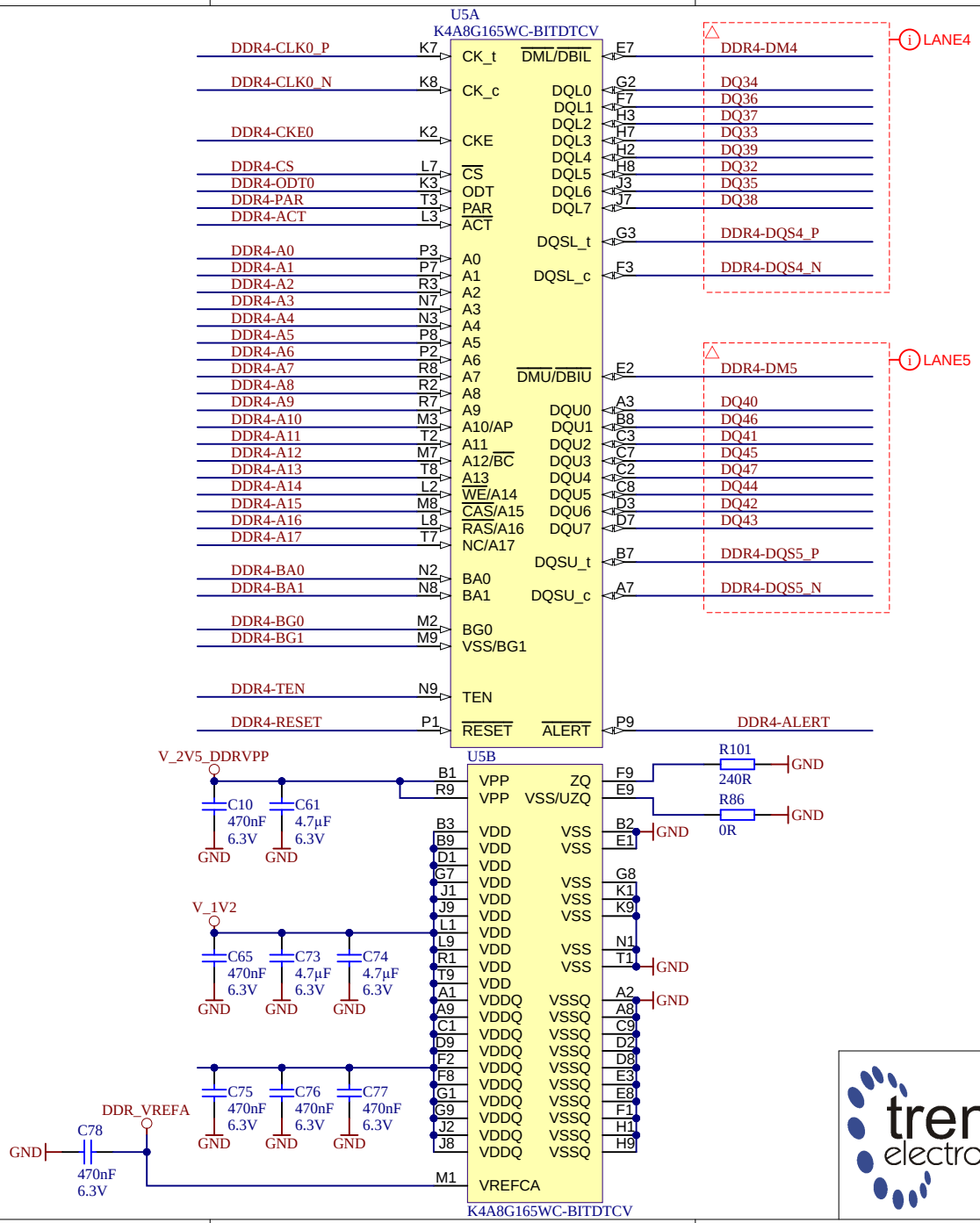
Title: ZU_PWR3		
A4	Number: TE0835 TXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 31 of 39
Filename: ZU_GND.SchDoc		



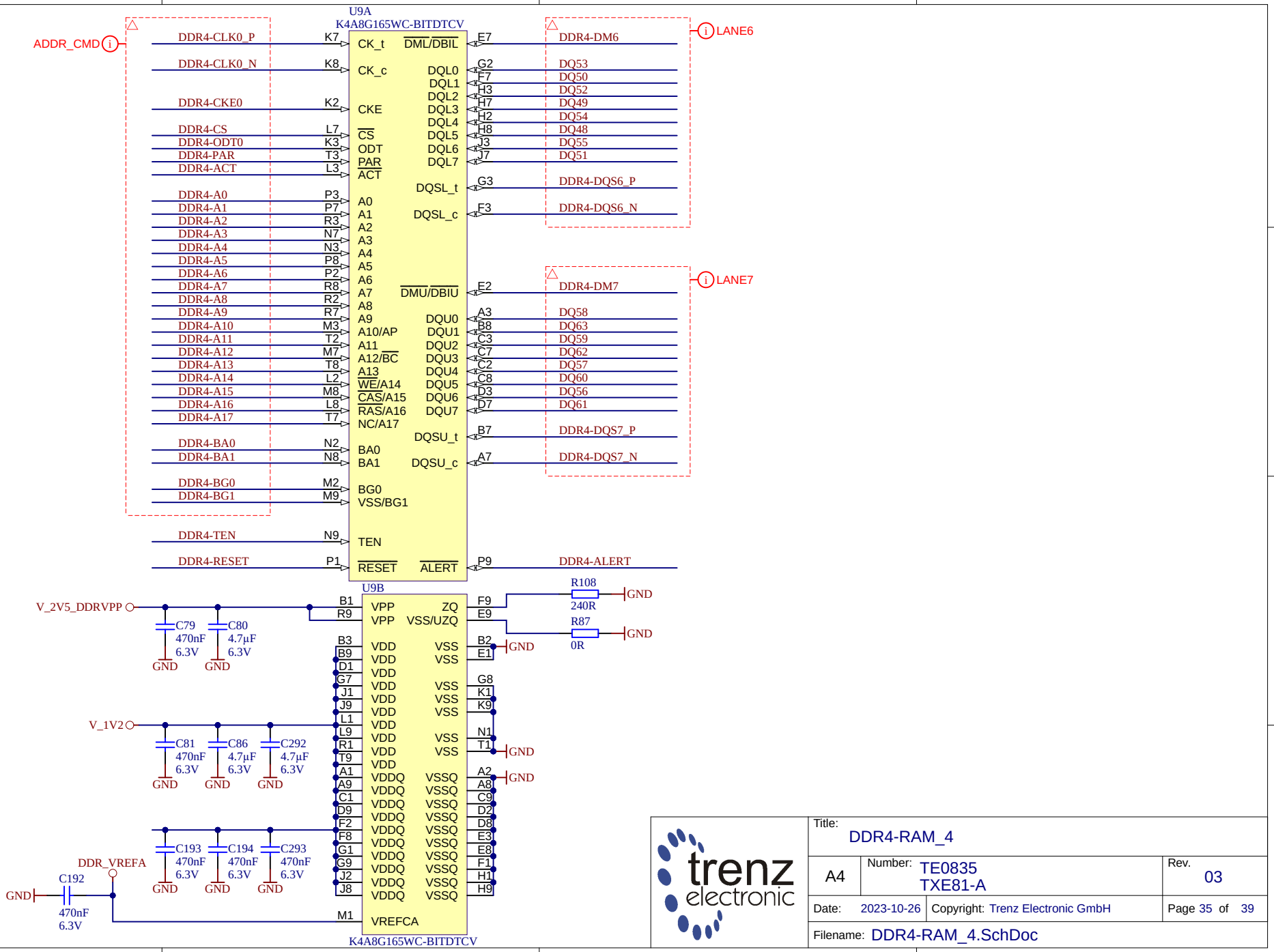
Title: DDR4-RAM_1			
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 32 of 39
Filename: DDR4-RAM_1.SchDoc			



trenz electronic	Title: DDR4-RAM_2		
	A4	Number: TE0835 TXE81-A	Rev. 03
	Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 33 of 39
	Filename: DDR4-RAM_2.SchDoc		

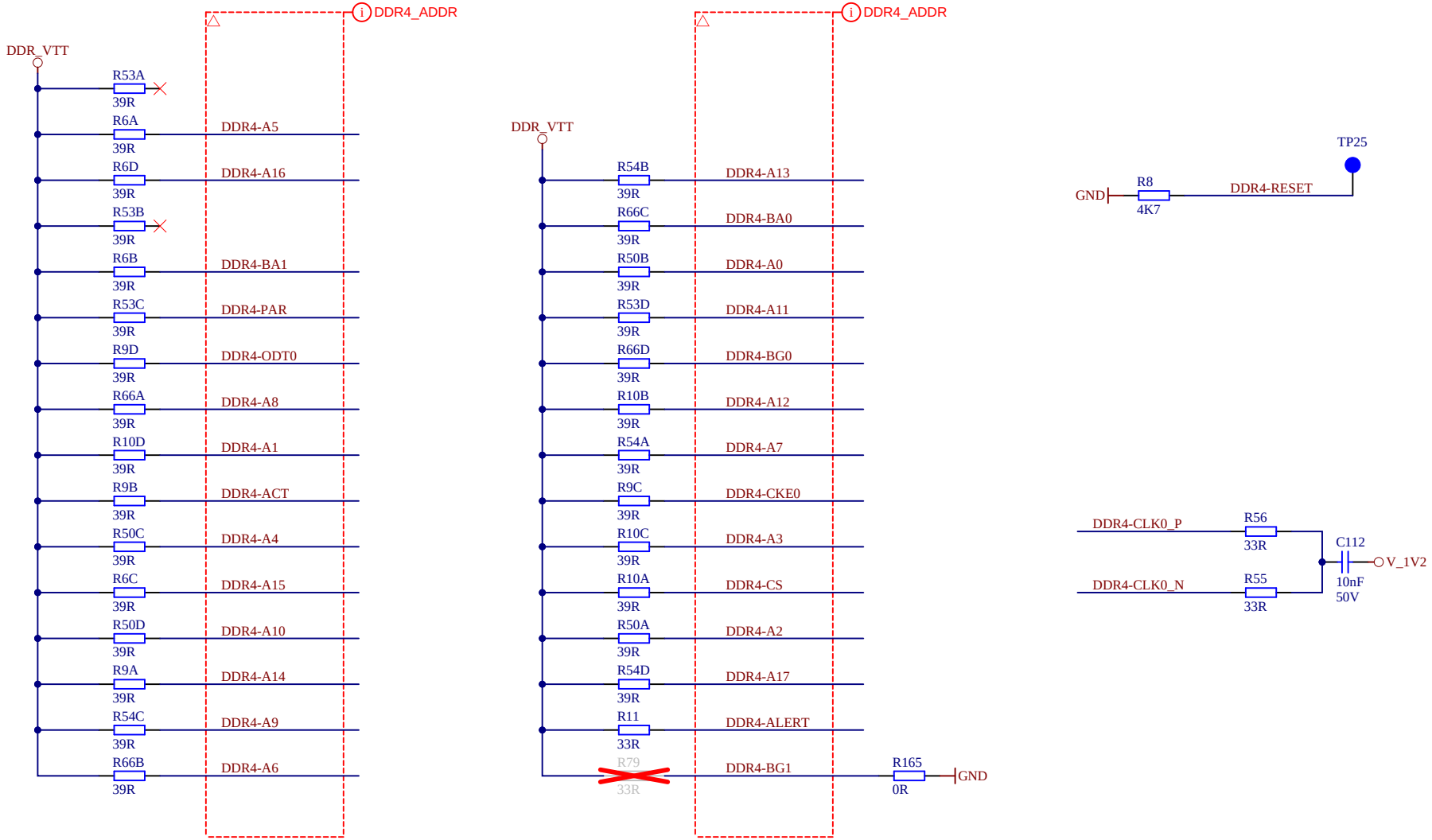


trenz electronic	Title: DDR4-RAM_3		
	A4	Number: TE0835 TXE81-A	Rev. 03
	Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 34 of 39
	Filename: DDR4-RAM_3.SchDoc		

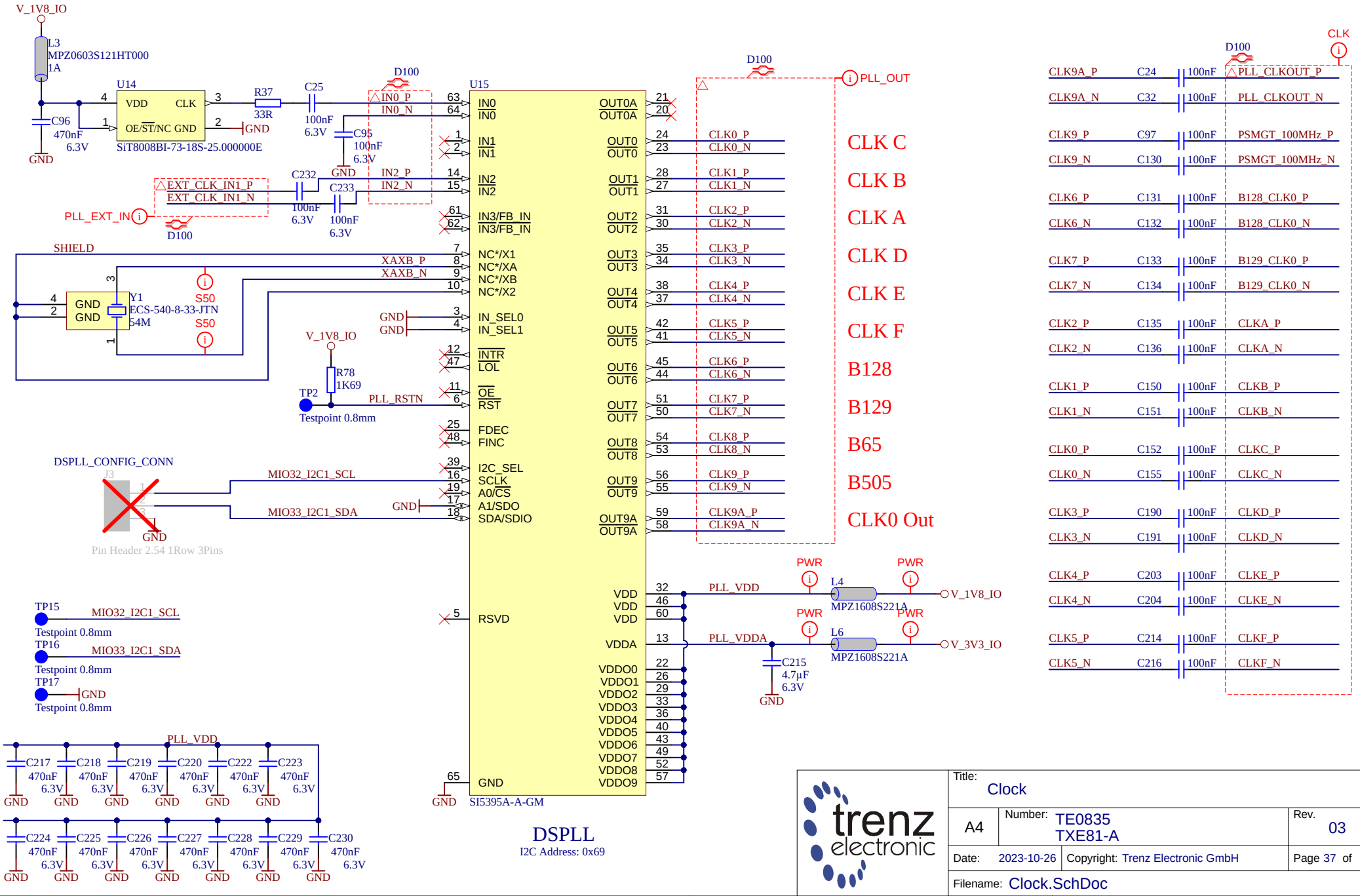


trenz electronic

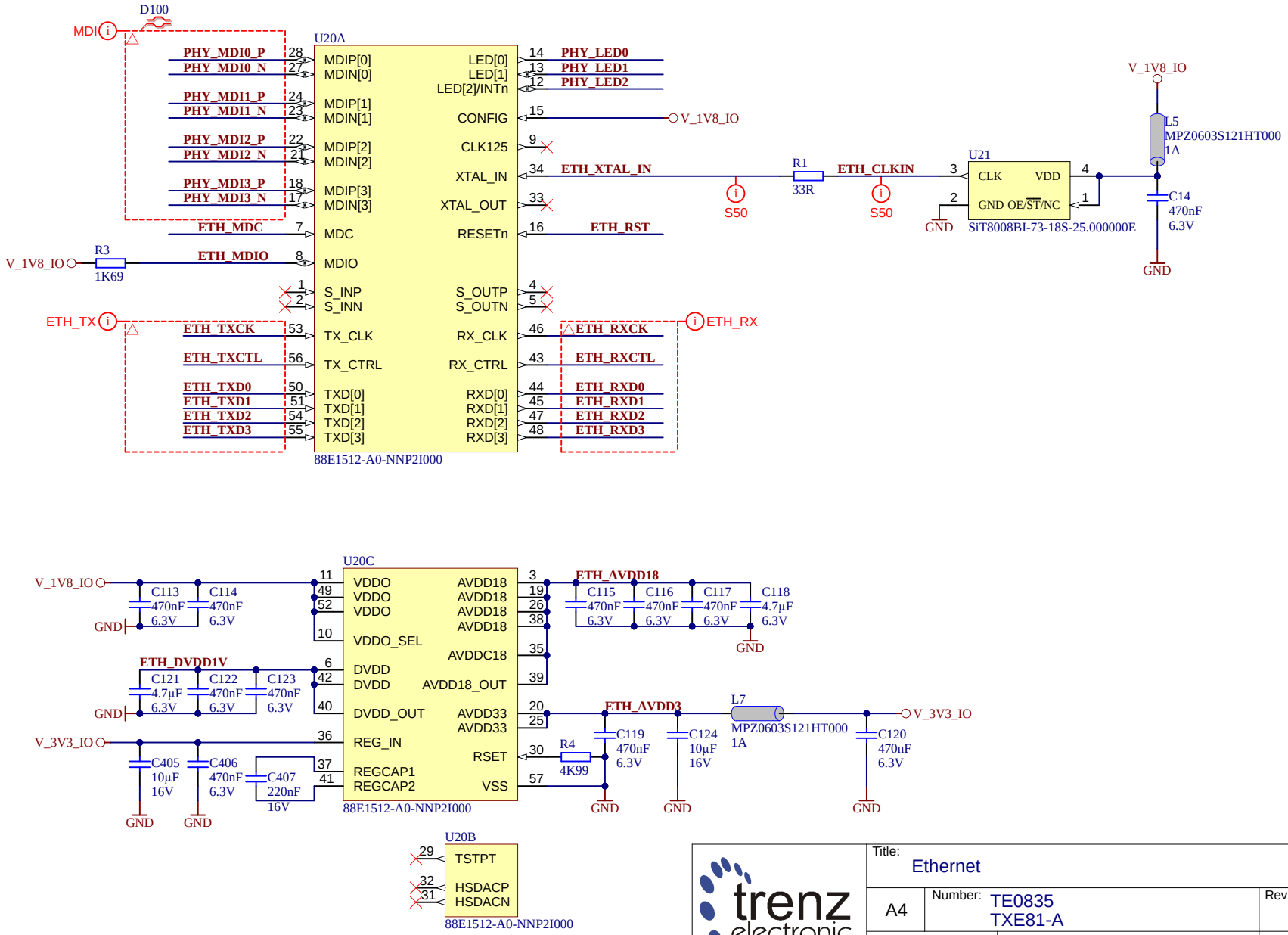
Title: DDR4-RAM_4			
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 35 of 39
Filename: DDR4-RAM_4.SchDoc			



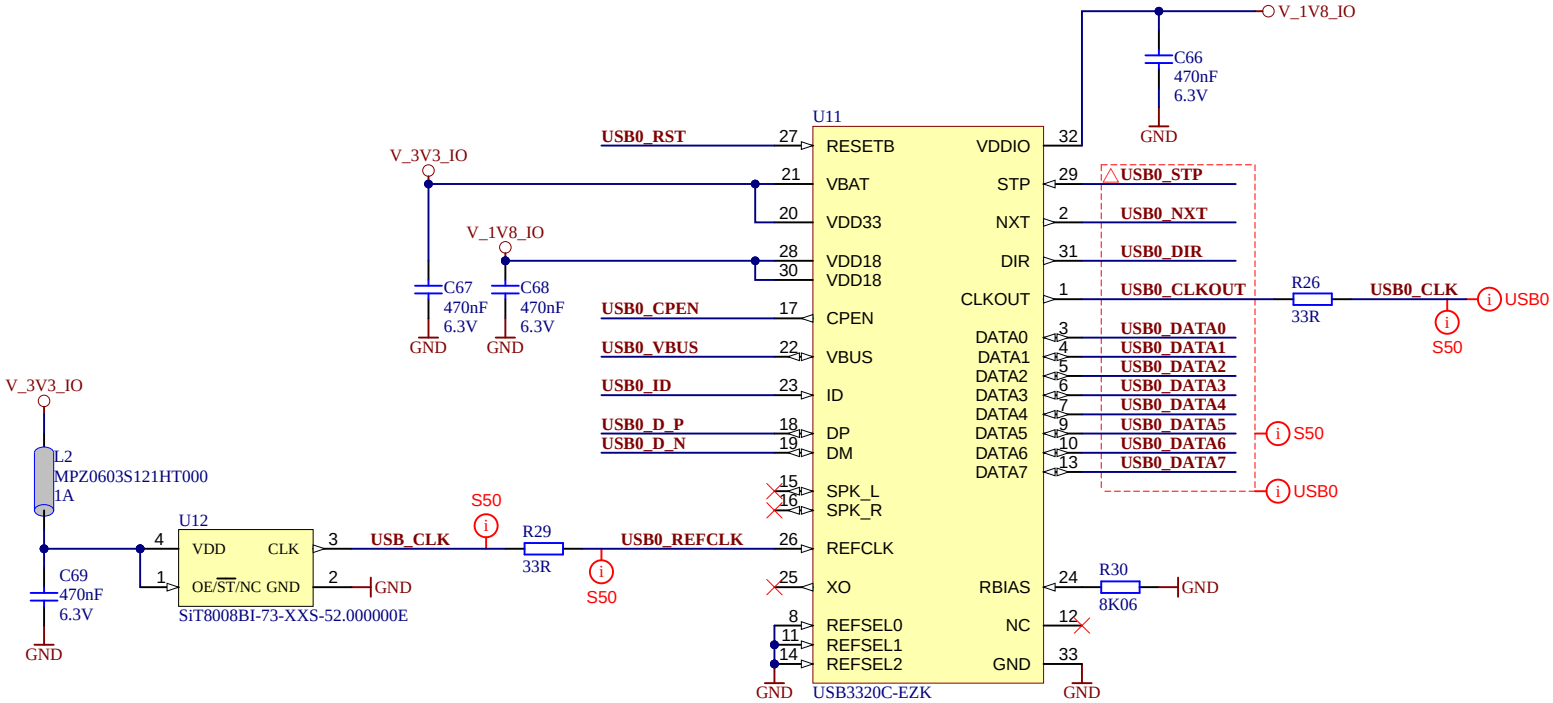
trenz electronic	Title: DDR4-TERM		
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 36 of 39
Filename: DDR4-TERM.SchDoc			



Title: Clock			
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 37 of 39
Filename: Clock.SchDoc			



	Title: Ethernet		
A4	Number: TE0835 TXE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 38 of 39
Filename: Ethernet.SchDoc			



trenz electronic	Title: USB-PHY		
	A4	Number: TE0835 TXE81-A	Rev. 03
	Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 39 of 39
	Filename: USB-PHY.SchDoc		