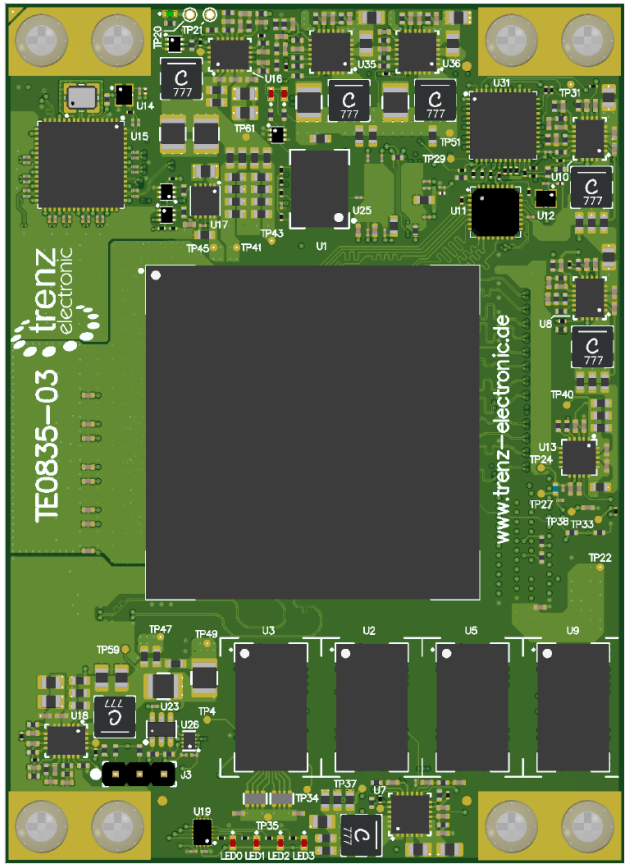

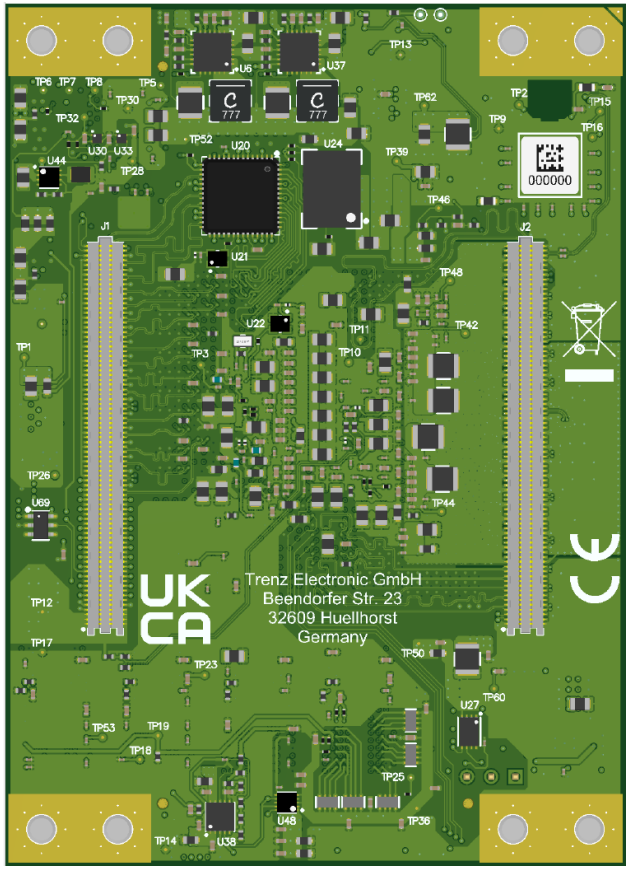

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Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0835 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: Legal Notices Modules		
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	Filename: Legal Notices Modules.SchDoc		

REVISION HISTORY

REV	Description	
-01	Initial revision	IG
-02	1. Added a VRP resistor on bank 65; 2. LDO U33 is changed on ADP7102ACPZ; 3. Signal FPGA IO0 is connected on AE18 pin of FPGA; 4. Signal DBG_LED3 is connected on AD18 pin of FPGA; 5. Signal MIO13_25 connected to J1 pin 33 instead MIO25. 6. Resistor R84 is removed; 7. LED D1 moved on edge of PCB; 8. Added THT testpoints J4 on CPLD_JTAGEN, R76 was removed; 9. Signals B49_XX_X are renamed in B88_XX_X; 10. C241 is changed on 1nF; 11. Length of CLK signals on RFADC and RFDAC are adjusted; 12. Wrong connection on U8 is fixed (PCB); 13. Wrong connection PGOOD1 pin of U7 is fixed; 14. R17 is changed from 35,5K to 33K for VCC_PL_PS correction.	IG
-02	15. APRE_3V3 ranamed to APRE_4V5, voltage of the power rail incrised from 3.3V to 4,58V. 16. Resistor R15 is changed from 13,3K to 9,09K. AN: 24671->25969 17. Capasitor C27 is changed from 100uF x 4V to 47uF x 6,3V. AN: 28940->24718	IG
-03	1. Added Legal Notices. 2. Added Power Diagram. 3. Added a DC-DCs synchronization circuit to spread spectrum. 4. Changed the core power supply schematic to 4 phases to increase current and reduce noise. 5. The power supply circuit of the module supports input voltage 5...12V. 6. EOL components are replaced: 6.1. L10, L12, L13, L14, L16 Ferrit beads BKP0603HS121-T replaced with MPZ0603S121HT000. 7. Updated layerstack to enhance power supply circuits and improve signal impedance matching. 8. Added POR_OVERRIDE configuration. 9. U25 (Pin 33) PS_SRST_B signal was removed. POR_OVERRIDE_N connected. 10. Added transistor T2A. 11. C180 is removed from schematic. 12. Networks to power the banks have been renamed. 13. Added Level shifter U19. 14. LEDs renamed: D1 --> LED0; D2 --> LED1; D3 --> LED2; D4 --> LED3 and connected to V_3V3_IO. Resistors R77A, R77B, R77C, R77D (39 R) replaced with R77, R130, R132, R134 (1K) respectively according to new shematic. 15. Added pull-up resistors R157, R158, R159, R161, R162, R163 to synchronise the power supplies. 16. Added resistors R142-R145. 17. U23 connected to V_3V3_IO (was 1.8V). 18. ZU_PWR: L9 removed from shematic. 19. Added resistors R46, R90, R98, R146, R149. 20. Added U44. 21. U33 (ADP7102ACPZ) replaced with MIC5504-3.3YMT. 22. Added two capasitors 4.7uF C355 and C488 on DDR_VTT. 23. Added signal SEL_2V5_DAC to Bank 65HP. Pin AD16. 24. Capasitors C24, C32, C97, C130-136, 150-152, 155, 190,191, C203, C204, C214, C216 are replaced with 100 nF. 25. Y1 CX3225SB54000 is EOL, it is replaced with ECS-540-8-33-JTN-TR 26. Added a VIN voltage sensor R121, R124, R150, R122, R153, C489. 27. Added R154, R155 to implement I2C interface between SC and RFSoC. 28. Clock CLK0A_100MHz renamed to PLL_CLKOUT	IG 27.03.2024

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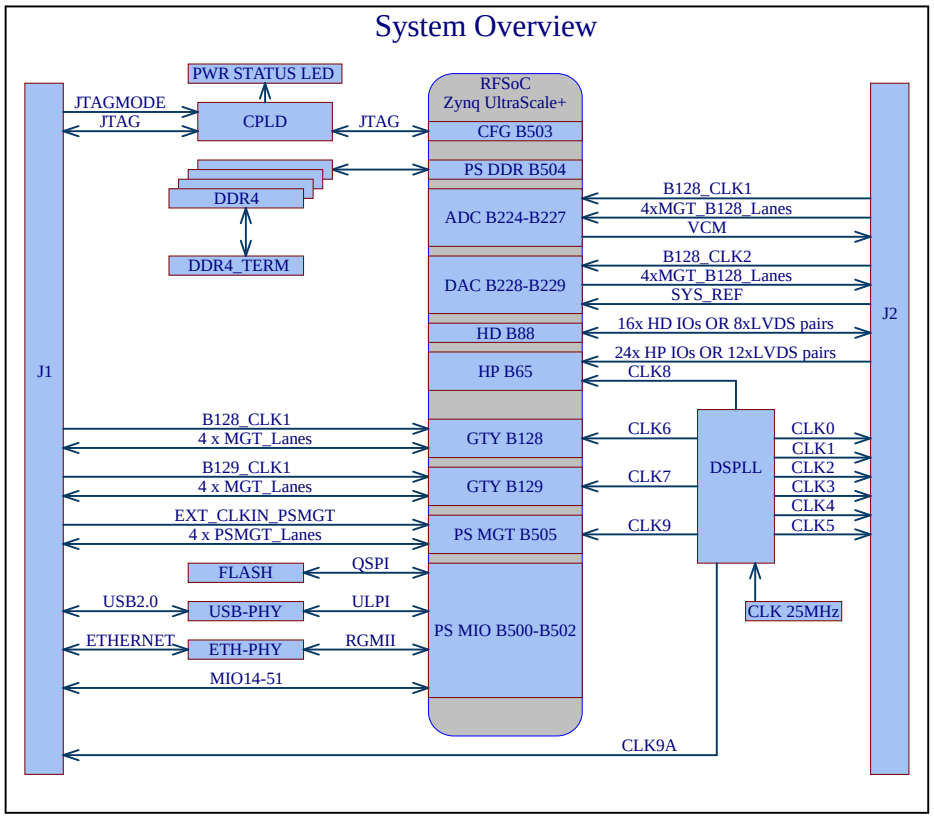
Special notes:

U_PWR-DIAGRAM
U_FPGA-PWR
U_FPGA-PWR_RF
U_FPGA-GND
POWER_STDBY_BIAS
POWER_VCCINT_PH1
POWER_VCCINT_PH2
POWER_VCCINT_PH3
POWER_VCCINT_PH4
POWER_1V2
POWER_IO_1V8
POWER_IO_3V3
POWER_MGT
POWER_RF
POWER_RF_1V8
POWER_DDR

System Overview



GND — Mount.Hole 3.2mm für Unterlegscheibe
GND — Mount.Hole 3.2mm für Unterlegscheibe
GND — Mount.Hole 3.2mm für Unterlegscheibe
GND — Mount.Hole 3.2mm für Unterlegscheibe
GND — Mount.Hole 3.2mm für Unterlegscheibe
GND — Mount.Hole 3.2mm für Unterlegscheibe
GND — Mount.Hole 3.2mm für Unterlegscheibe
GND — Mount.Hole 3.2mm für Unterlegscheibe

PM1 FIDU-DOT - mini
PM2 FIDU-DOT - mini
PM3 FIDU-DOT - mini
PM4 FIDU-DOT - mini
PM5 FIDU-DOT - mini
PM6 FIDU-DOT - mini

LOGO1
TE Logo PRINT Layer
LOGO PRINT

MECH1
TE Address Overlay
LOGO ADDRESS

S/N
Serial
Serialnumber 6,3 x 6.3mm

UKCA
UKCA Logo on Top Overlay
UKCA-TOPOVERLAY

Table of I2C devices and addresses

Designator	I2C Address	Description
U23	0x50	I2C MAC EEPROM
U27	0x60	Security Chip
U15	0x69	DSPLL

Design drawn by:	IG
Checked by:	MR
Assembly variant:	TYE81-A
Created by:	IG
Modified by:	IG
Modified at:	2024-07-17

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Title: TE0835

A4	Number: TE0835 TYE81-A	Rev. 03
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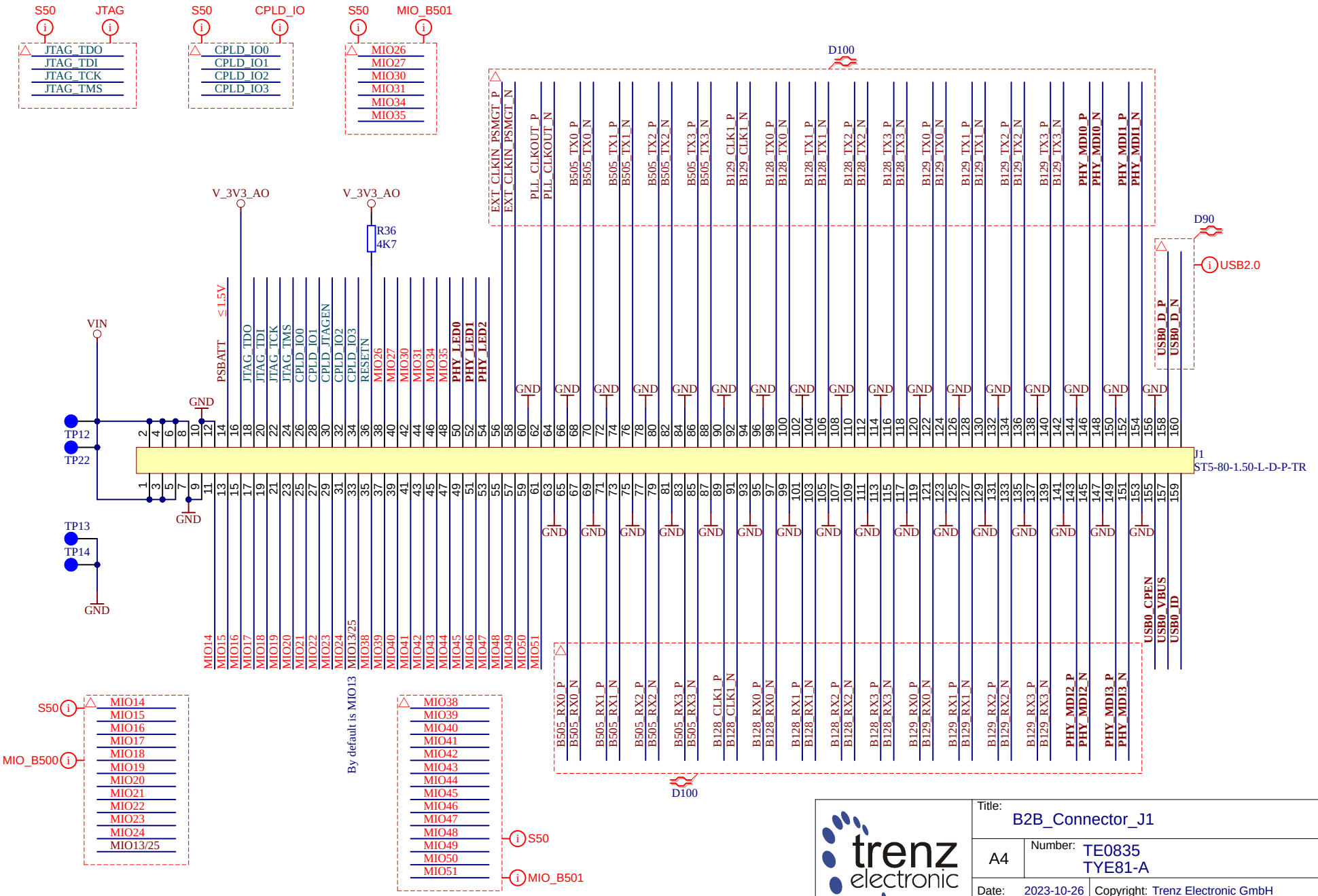
Filename: TE0835-Overview.SchDoc		



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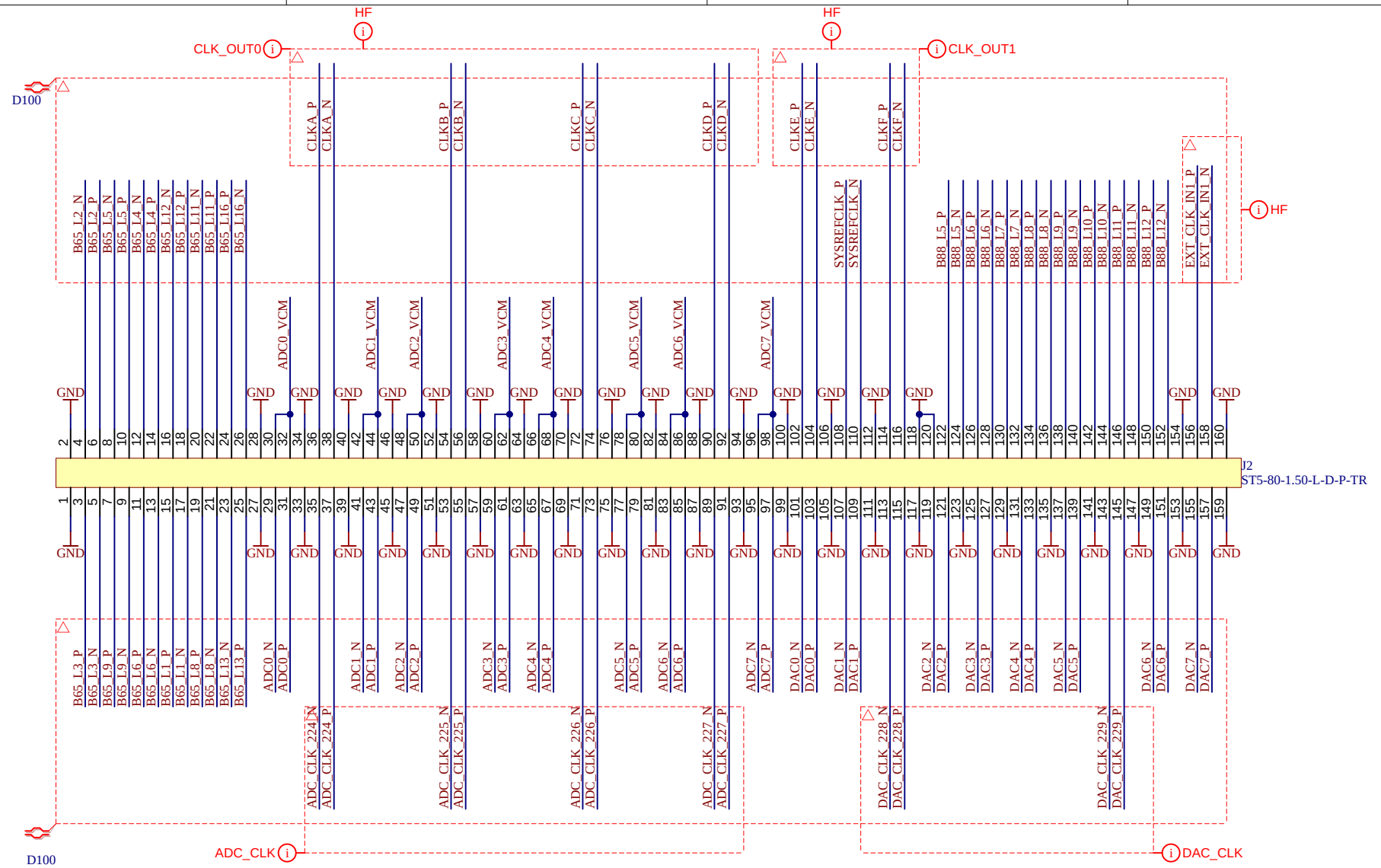
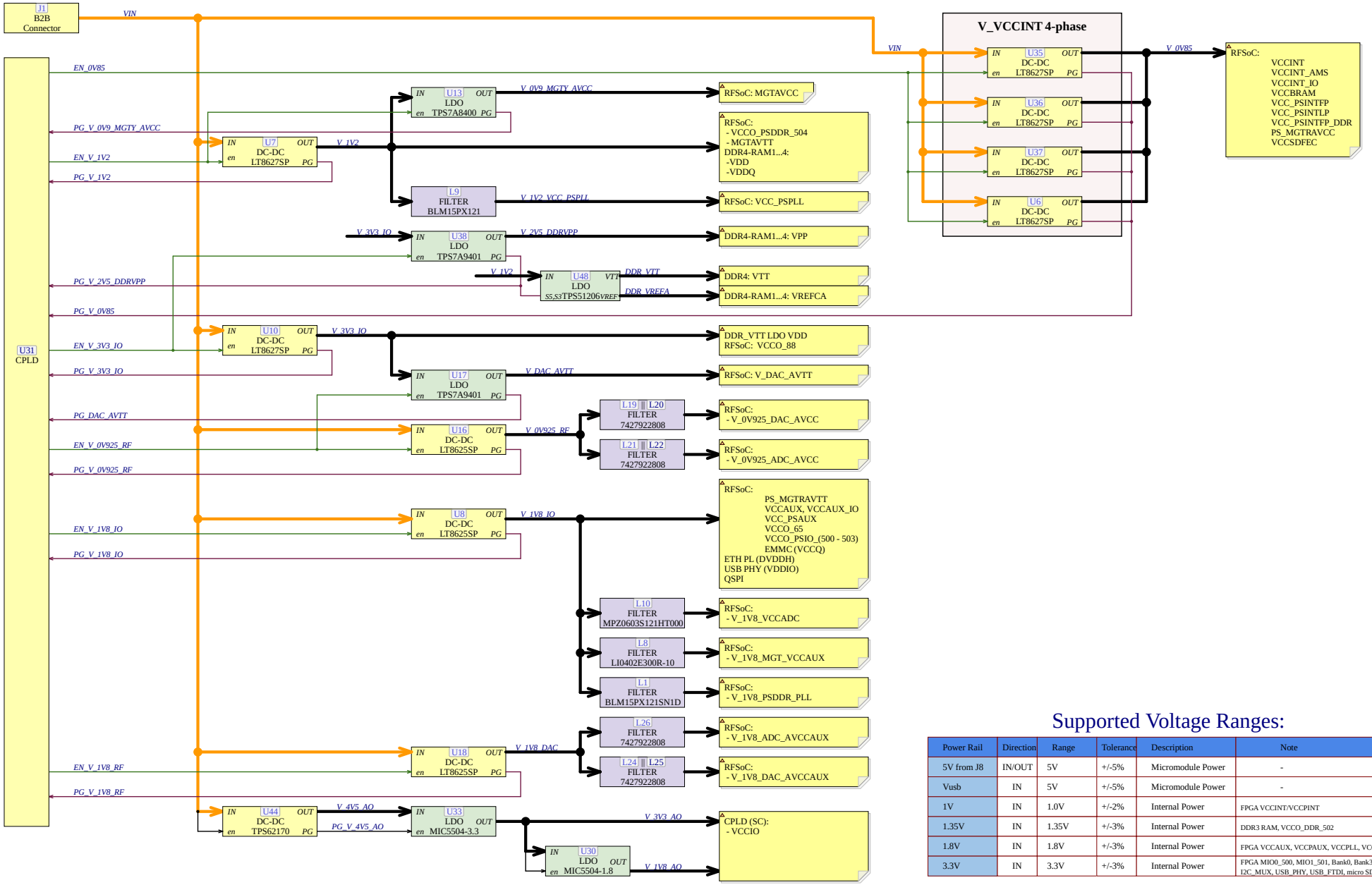
A4	Number: TE0835 TYE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 4 of 39
Filename: B2B_Connector_J1.SchDoc			



trenz electronic	Title: B2B_Connector_J2		
A4	Number: TE0835 TYE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 5 of 39
Filename: B2B_Connector_J2.SchDoc			

Power-on sequencing:



Net name — Power bus

U4 DC-DC TPS62170 — Power converter

en — Control signals

PG — Power Good signals

LDOs

Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
5V from J8	IN/OUT	5V	+/-5%	Micromodule Power	-
Vusb	IN	5V	+/-5%	Micromodule Power	-
1V	IN	1.0V	+/-2%	Internal Power	FPGA VCCINT/VCCPINT
1.35V	IN	1.35V	+/-3%	Internal Power	DDR3 RAM, VCCO_DDR_502
1.8V	IN	1.8V	+/-3%	Internal Power	FPGA VCCAUX, VCCPAUX, VCCPLL, VCCBATT, AVCC; SC
3.3V	IN	3.3V	+/-3%	Internal Power	FPGA MIO0_500, MIO1_501, Bank0, Bank34, Bank35 I2C_MUX, USB_PHY, USB_FTDI, micro SD, USB Hub, SC

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Title: Power_Diagram		
A3	Nummer: TE0835 TYE81-A	Rev. 03
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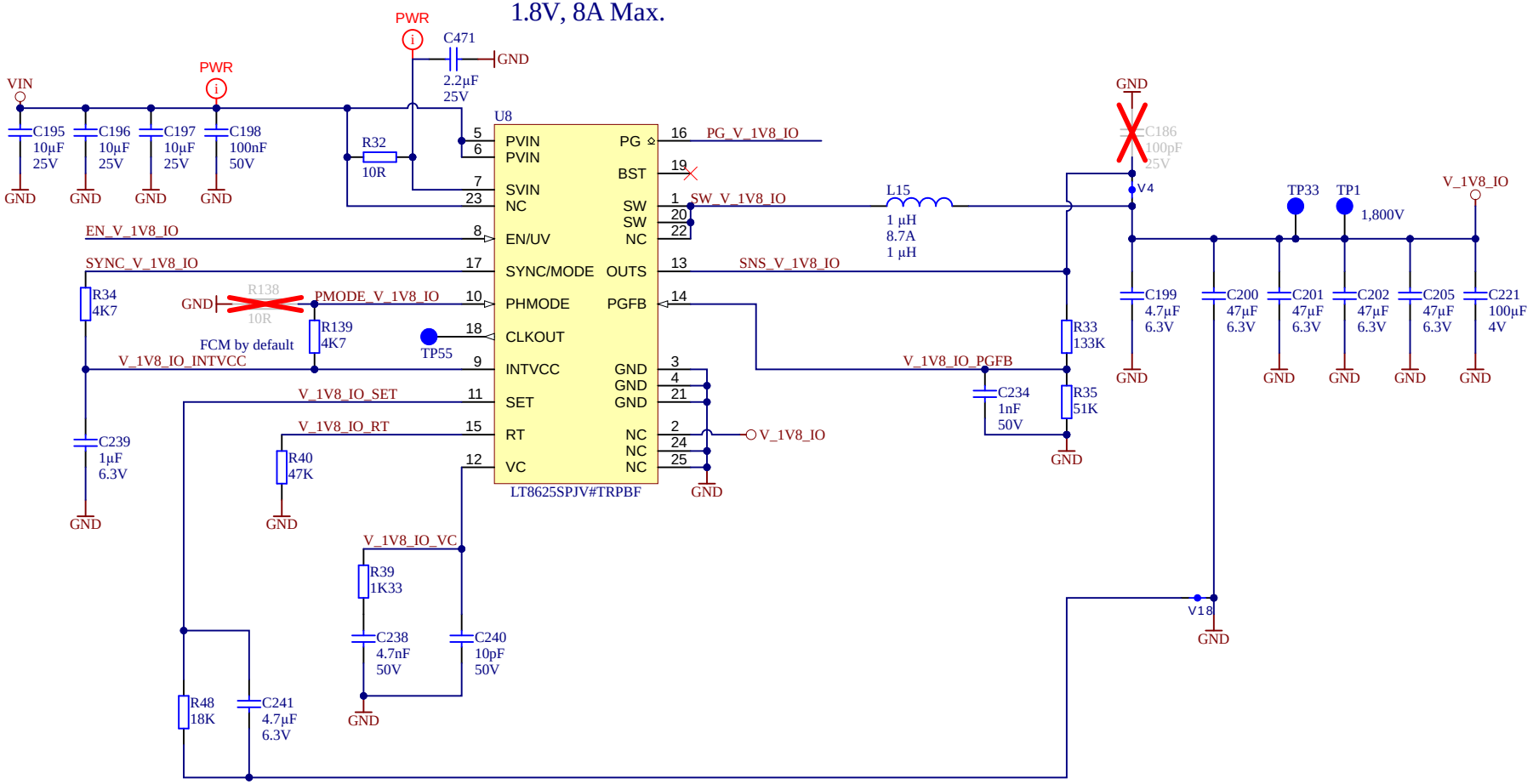
Filename: Power Diagram.SchDoc		



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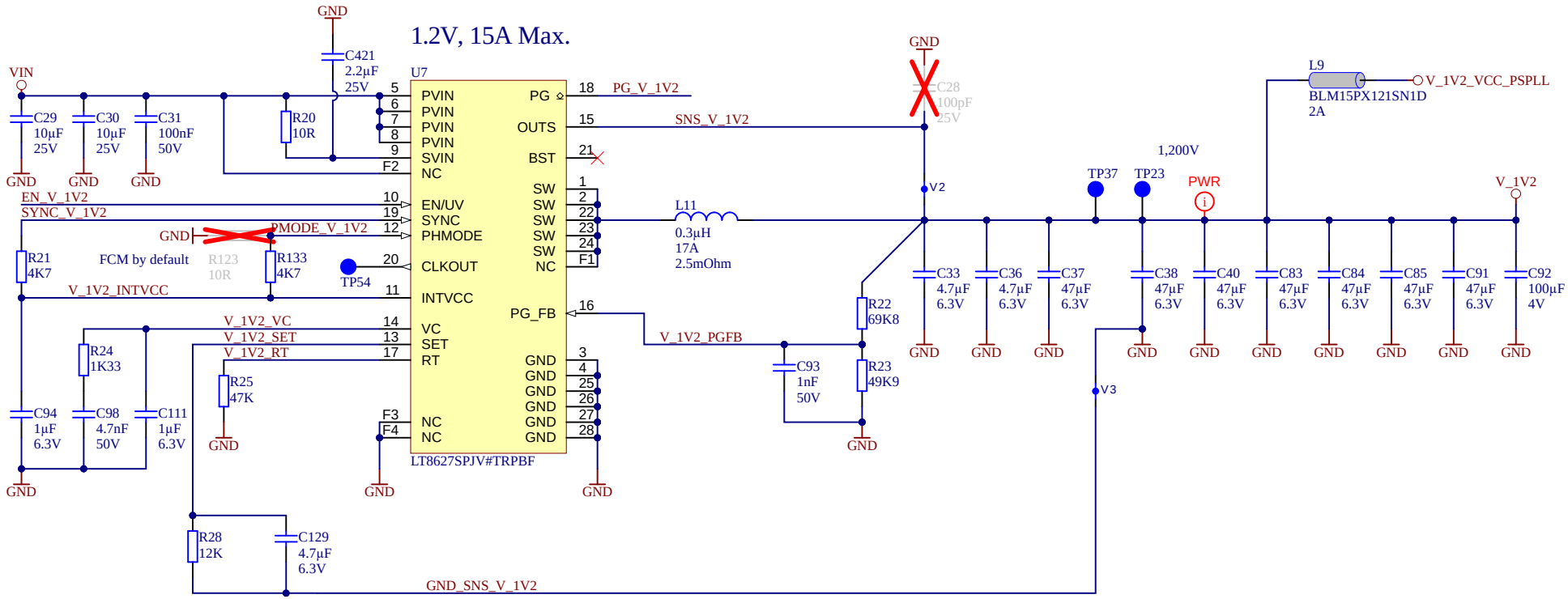
Date: 2024-07-17	Copyright: Trenz Electronic GmbH		Page 7 of 39
Filename: POWER_IO_1V8.SchDoc			



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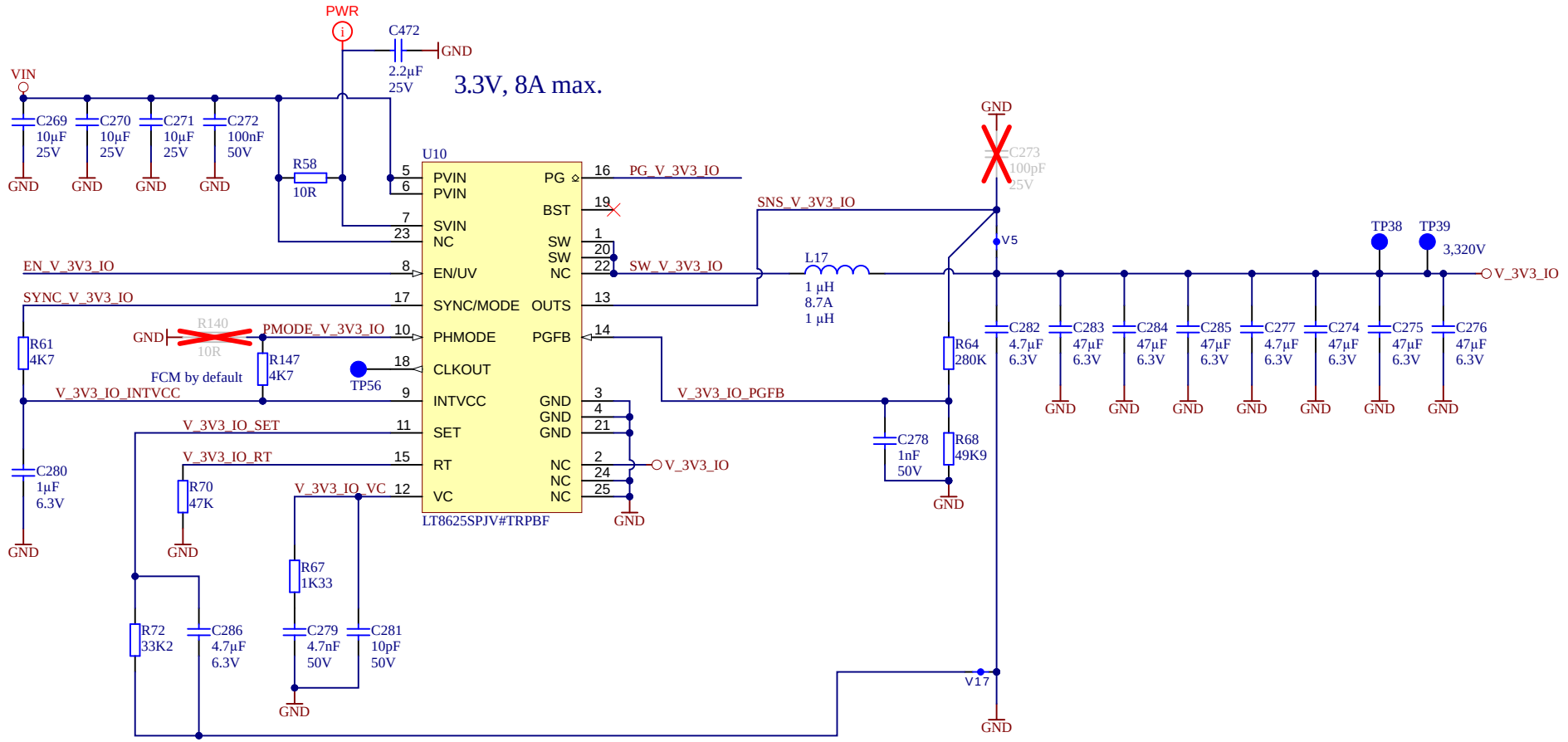
	Date: 2024-07-17	Copyright: Trenz Electronic GmbH	Page 8 of 39
	Filename: POWER_1V2.SchDoc		



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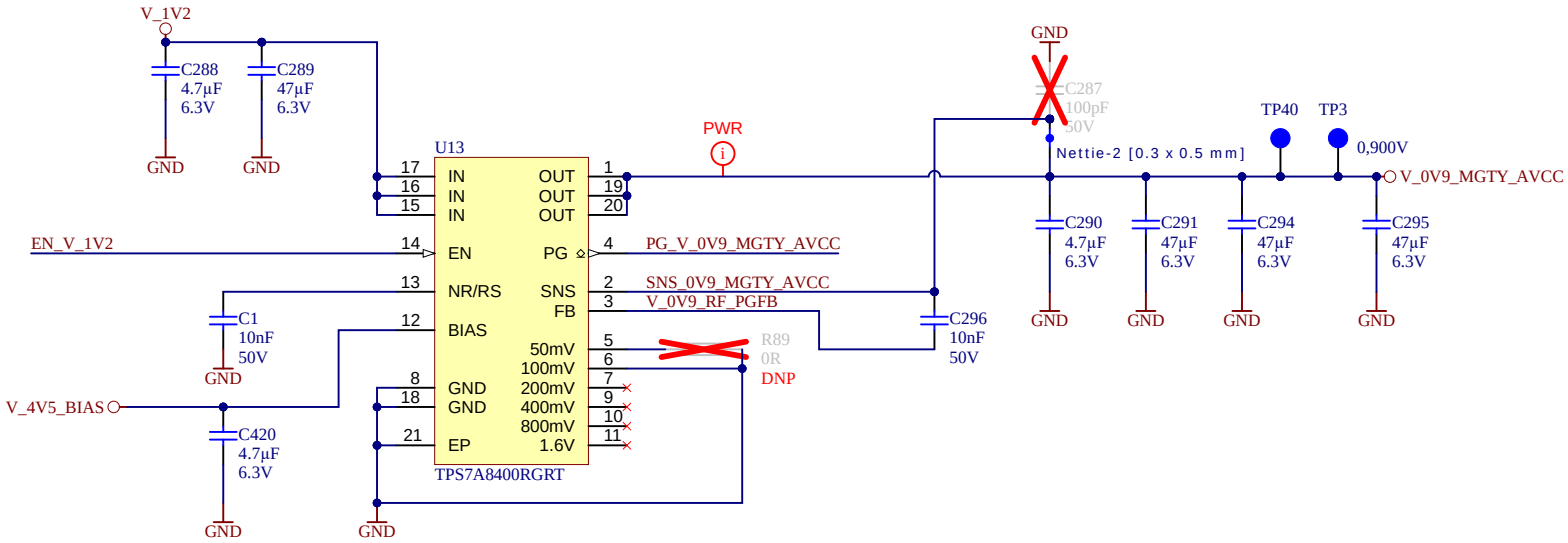
A4	Number: TE0835 TYE81-A		Rev. 03
Date: 2024-07-17	Copyright: Trenz Electronic GmbH		Page 9 of 39
Filename: POWER_IO_3V3.SchDoc			

V_0V9_MGTAVCC, 2.5A Max



trenz electronic	Title: POWER_MGT		
	A4	Number: TE0835 TYE81-A	Rev. 03
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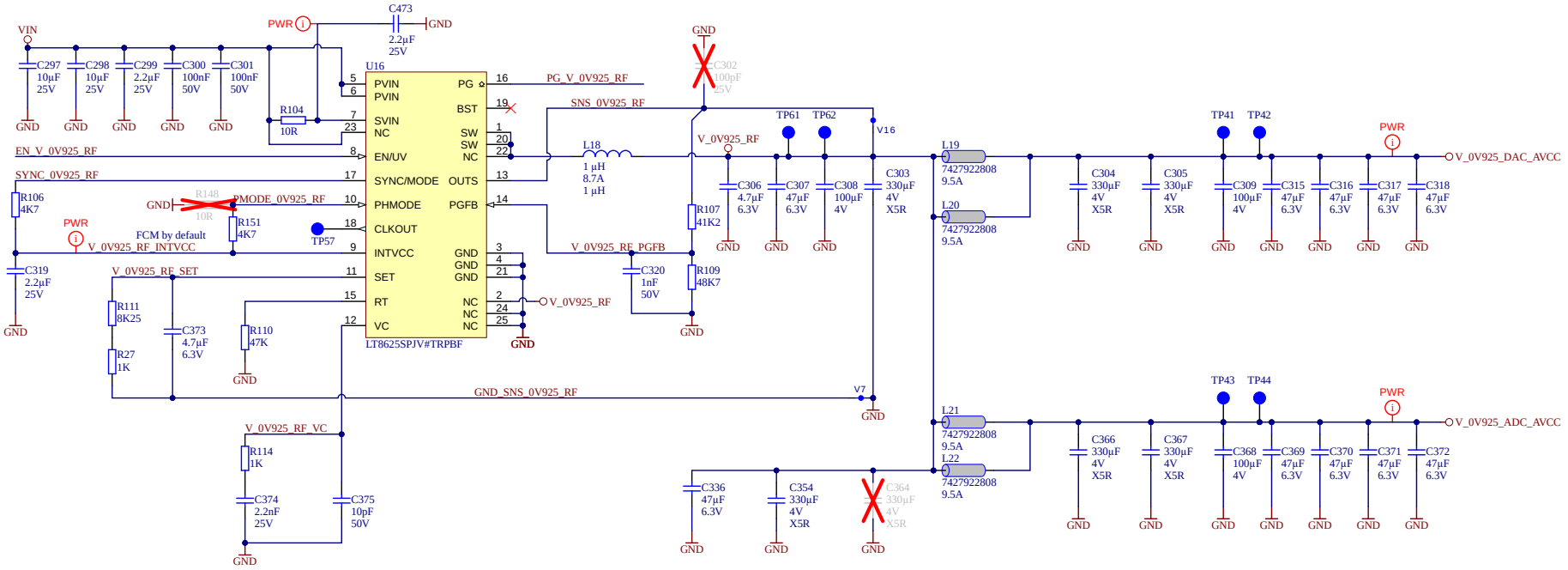
V_0V925_DAC_AVCC, (0.12 - 4.6A) + V_0V925_ADC_AVCC, (1.2 - 2.3A) ==> 1.32 - 6.9 A



DAC_AVTT, 2.5V/3.0V, 0.8A

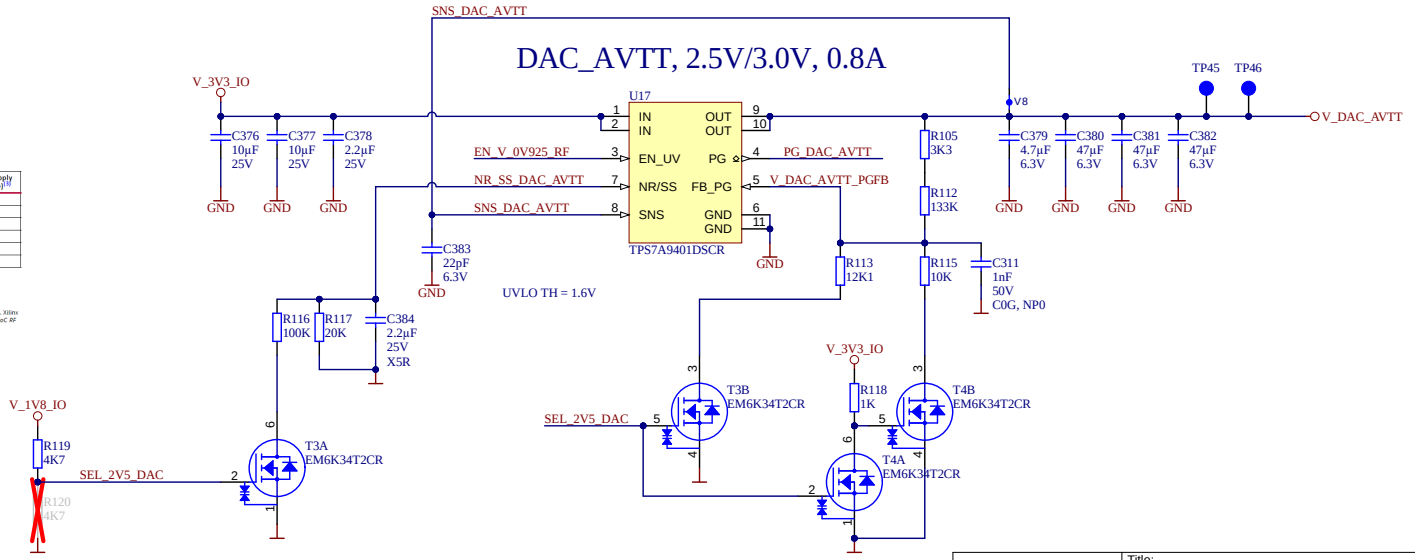


Table 3-11: ADC and DAC Voltage Supply Specifications for Gen 3 Devices[1]

Supply	Nominal Voltage (V)	Tolerance (%)[2]	Frequency Range (MHz)	Maximum Supply Ripple (mVpp)[3]
ADC_AVCC	0.925	±3	0.1–15	0.25
ADC_AVCCAUX	1.8	±3	0.1–15	1.2
DAC_AVCC	0.925	±3	0.1–15	0.32
DAC_AVCCAUX	1.8	±3	0.1–15	1.0
DAC_AVTT	2.5/3.0[4]	±3	0.1–15	2.0
VCCINT_AMS	0.85	±3	0.1–15	20.0

Notes:
1. For the maximum current, refer to the Xilinx Power Estimator (XPE) tool.
2. The tolerance percentage is for the switching regulator that feeds the VRM.
3. Output of the VRM.
4. DAC_AVTT should be set to 2.5V if used in 20 mA mode, and 3.0V if used in 32 mA mode in Gen 1 and Gen 2. Xilinx recommends DAC_AVTT be set to 3.0V in Gen 3 to enable the VOP function. Refer to *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide (PG269)* [Ref 17] for details and compatibility mode.

OUTPUT VOLTAGE 2.5V, Rnr =16.5 kOhms (default)
OUTPUT VOLTAGE 3.0V, Rnr =20.0 kOhms

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Title: POWER_RF		
A3	Nummer: TE0835 TYE81-A	Rev. 03
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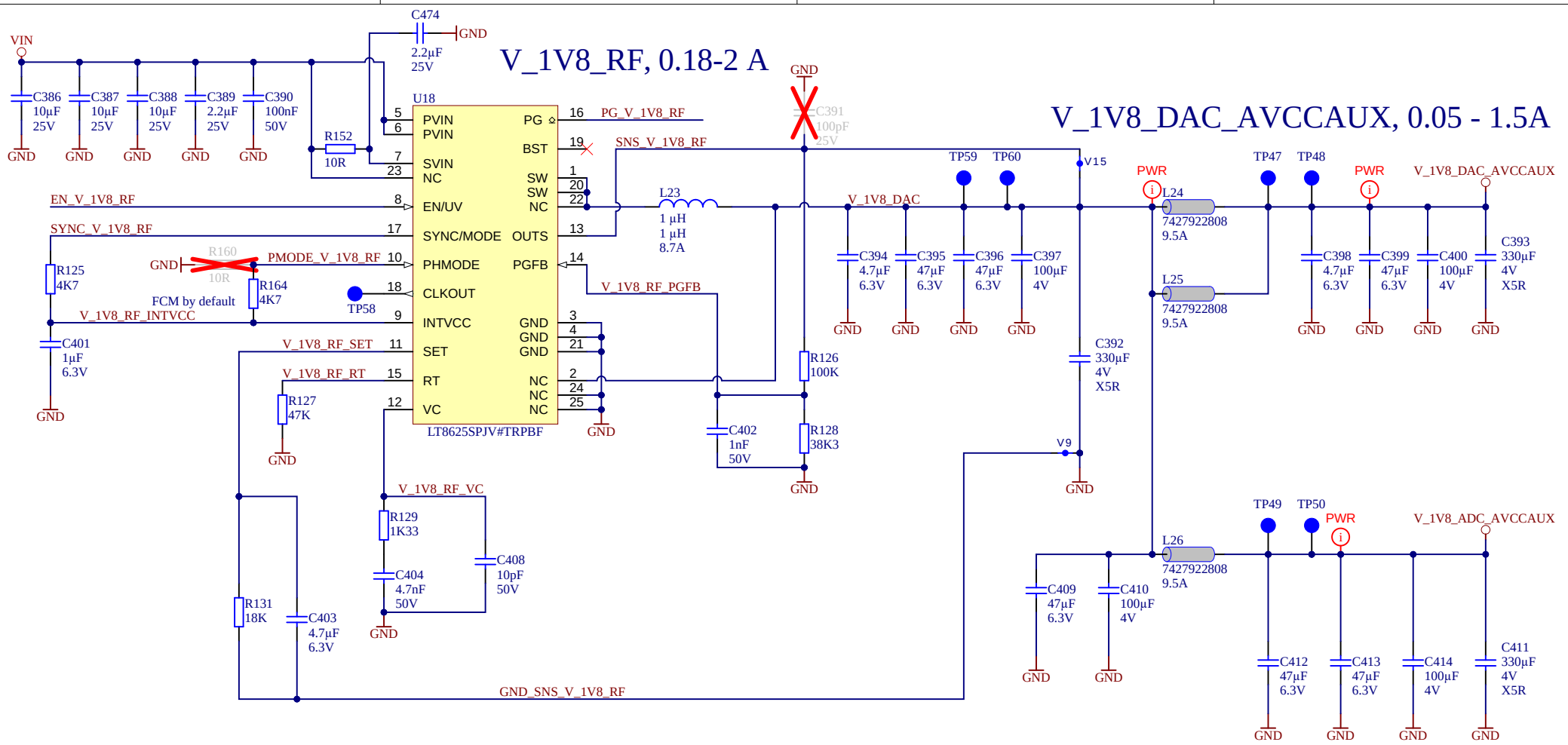

trenz electronic	Title: POWER_RF_1V8		
	A4	Number: TE0835 TYE81-A	Rev. 03
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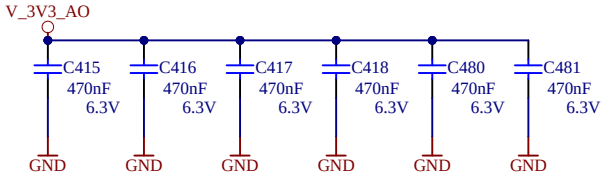
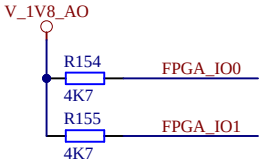
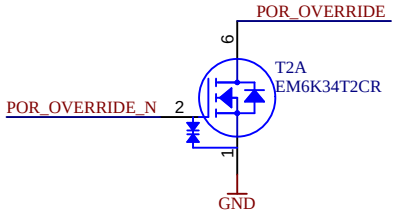
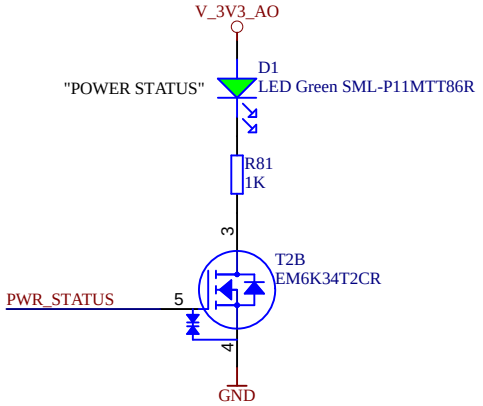
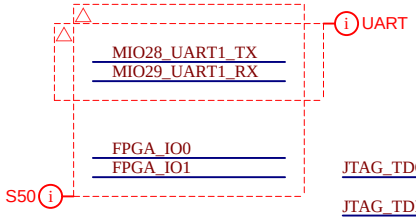
System Controller (SC)

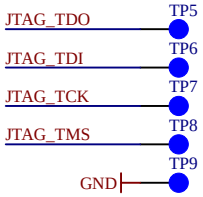


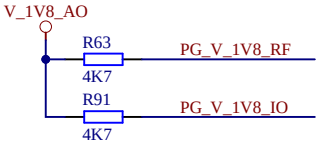


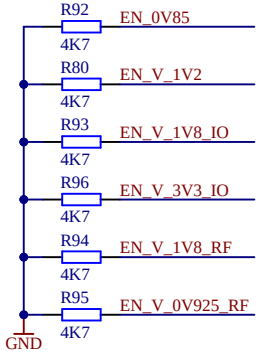


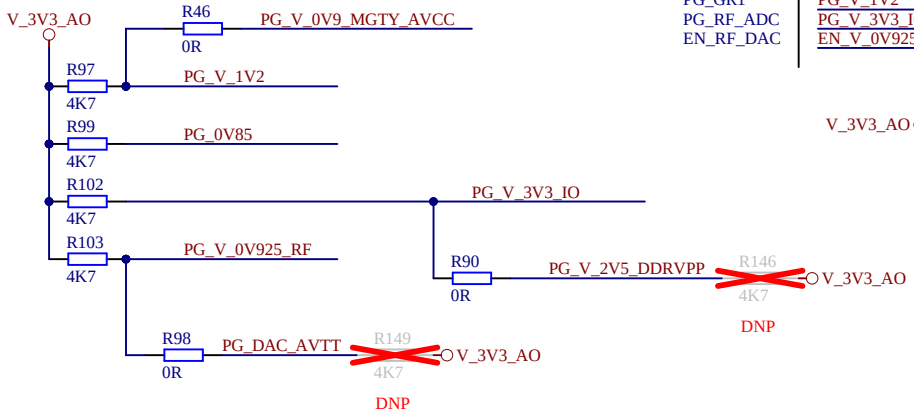










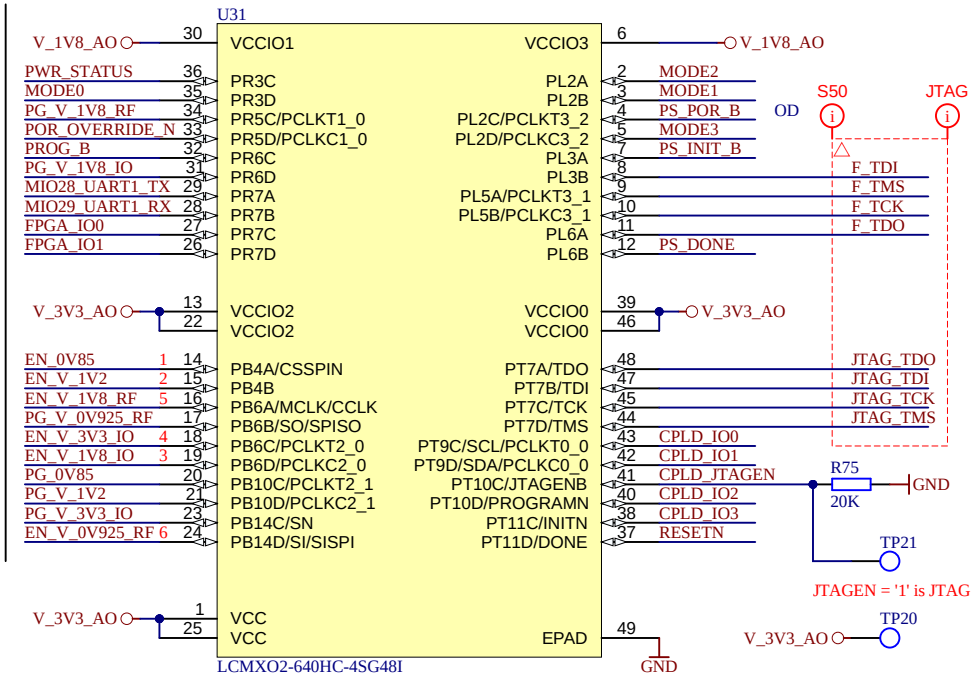


REV02
Net names:

PG_VCCRF
SRST_B

PG_GR2

EN_PS_PL
EN_GR1
EN_RF_ADC
PG_RF_DAC
EN_VCCRF
EN_GR2
PG_PS_PL
PG_GR1
PG_RF_ADC
EN_RF_DAC



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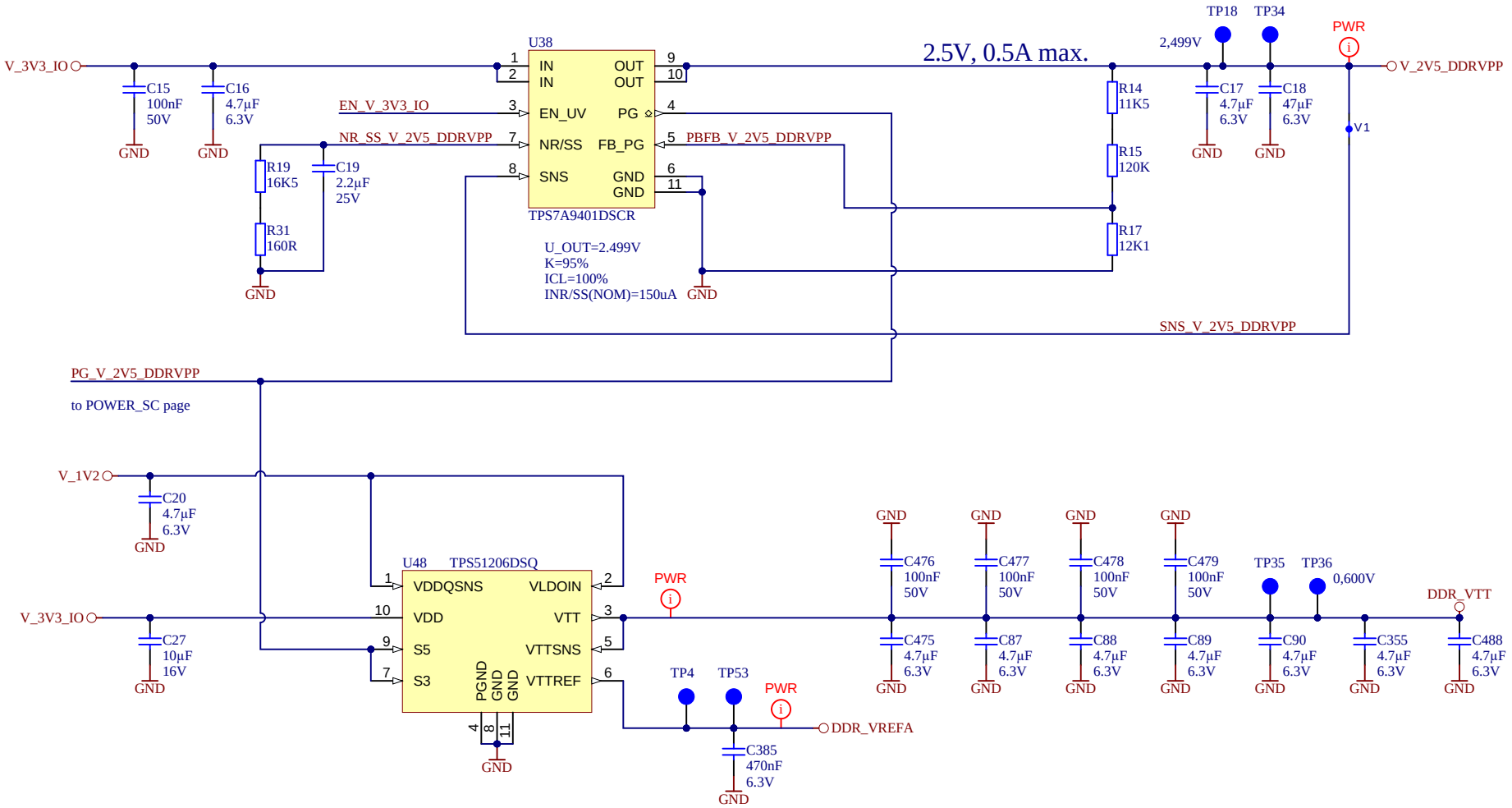

trenz electronic	Title: PWR_DDR		
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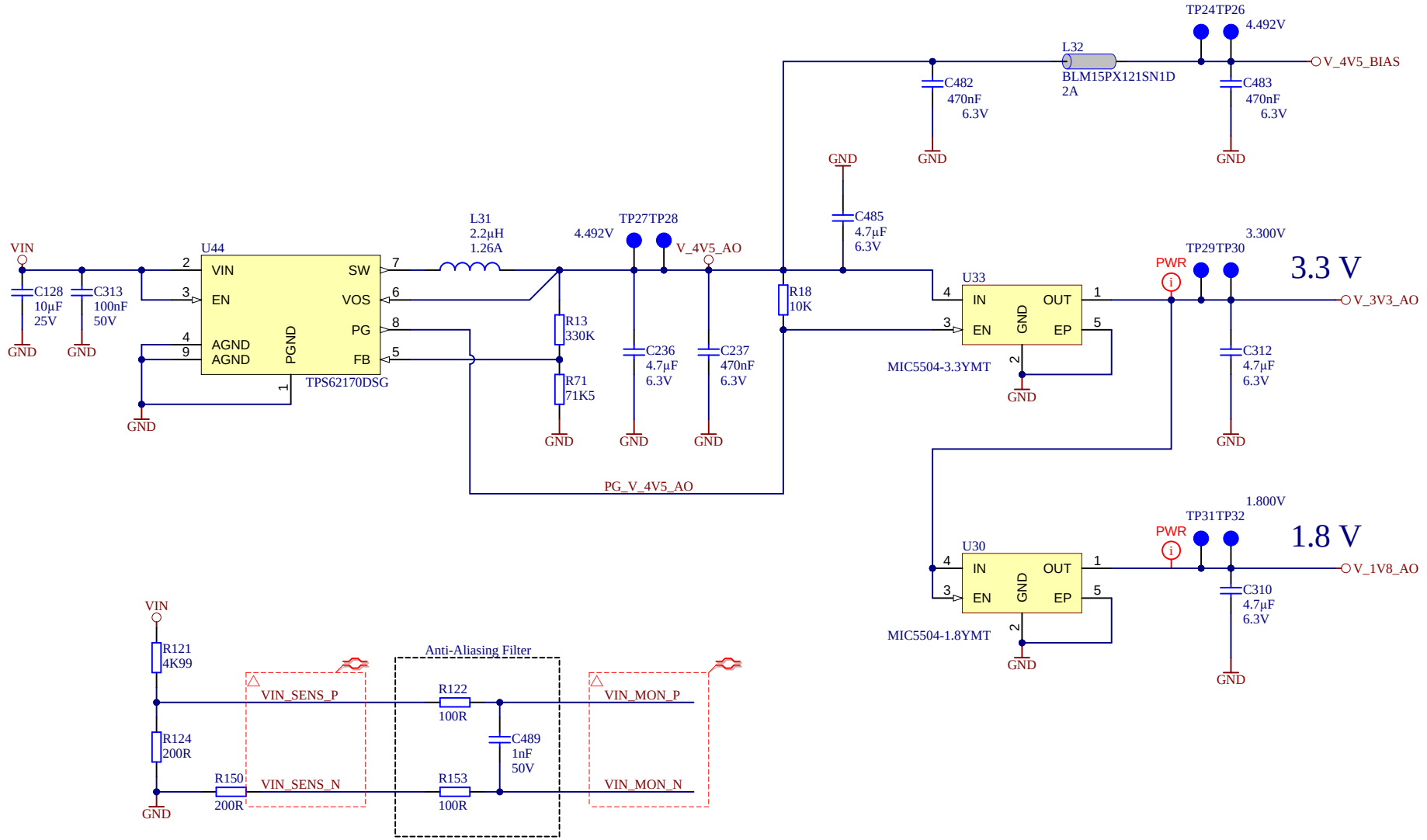
Filename: POWER_DDR.SchDoc			



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A4	Number: TE0835 TYE81-A		Rev. 03
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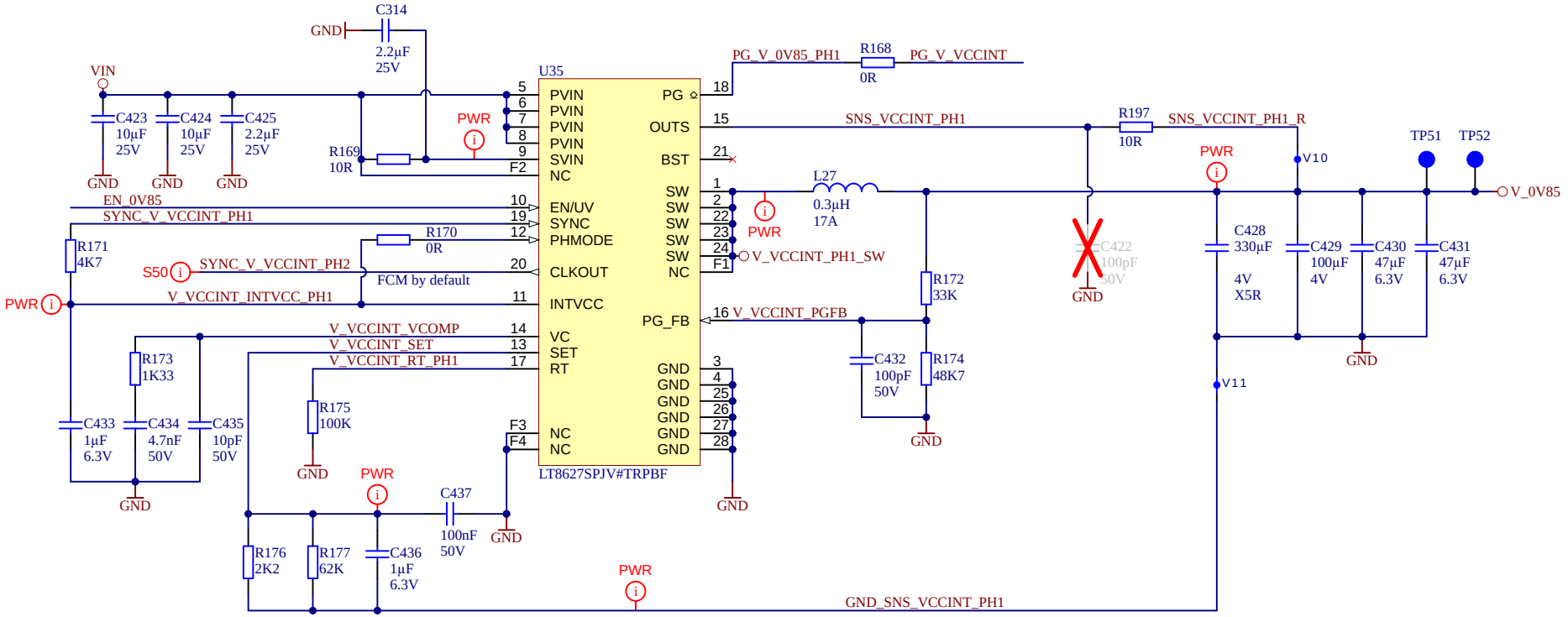
Filename: POWER_STDBY_BIAS.SchDoc			

VCCINT Phase 1/4, 0.85V, 45A, 15A per Phase



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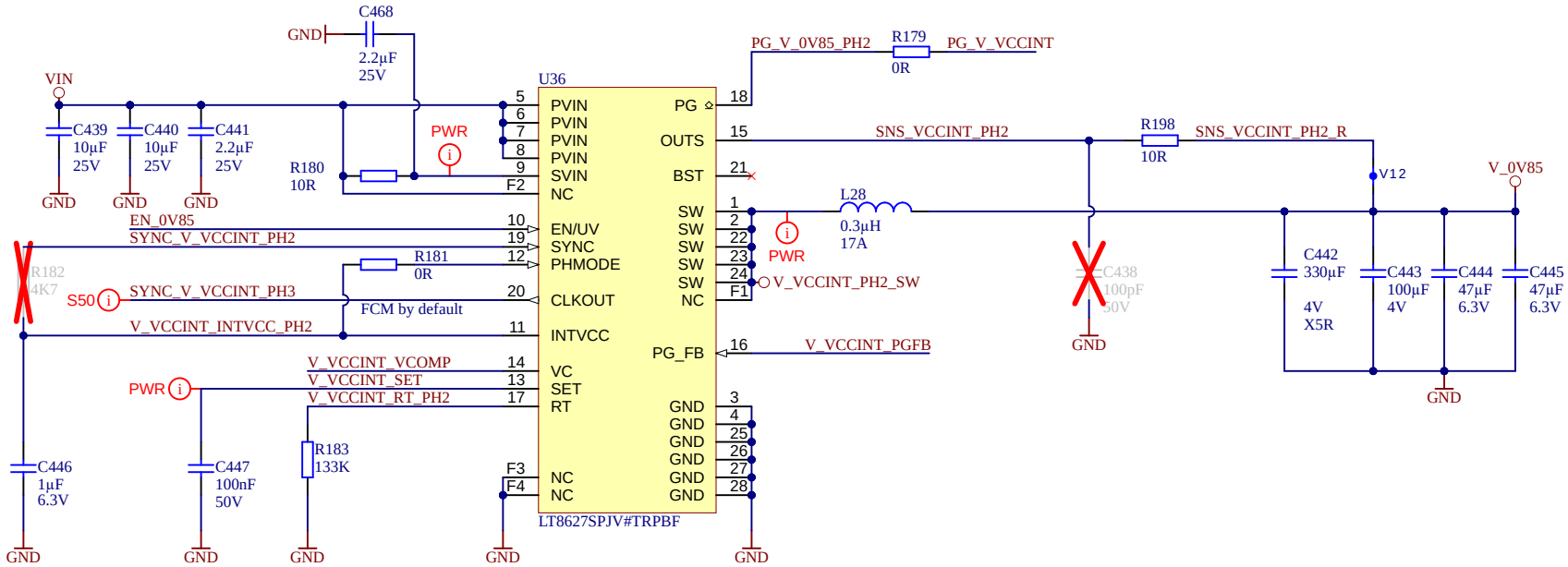
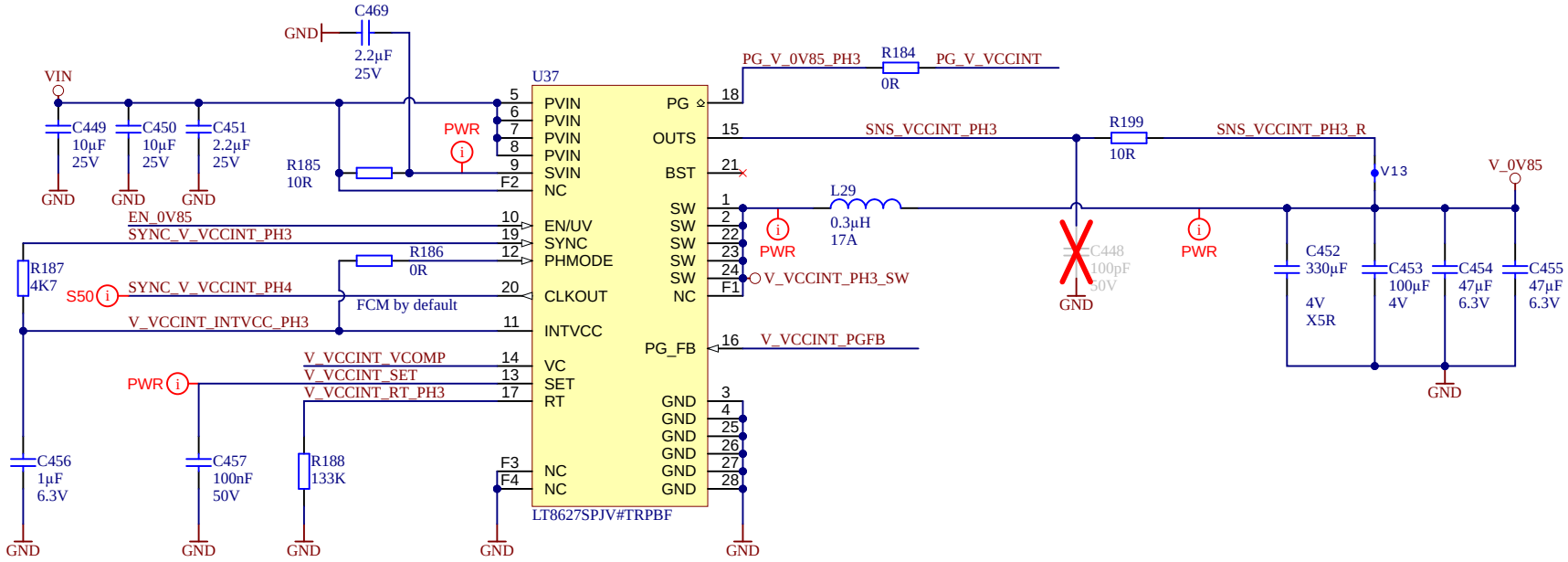
	Date: 2024-07-17	Copyright: Trenz Electronic GmbH	Page 16 of 39
	Filename: POWER_VCCINT_PH1.SchDoc		

VCCINT Phase 2/4, 0.85V, 45A, 15A per Phase



trenz electronic	Title: POWER_VCCINT_PH2		
	A4	Number: TE0835 TYE81-A	Rev. 03
	Date: 2024-07-17	Copyright: Trenz Electronic GmbH	Page 17 of 39
	Filename: POWER_VCCINT_PH2.SchDoc		

VCCINT Phase 3/4, 0.85V, 45A, 15A per Phase



trenz electronic	Title: POWER_VCCINT_PH3		
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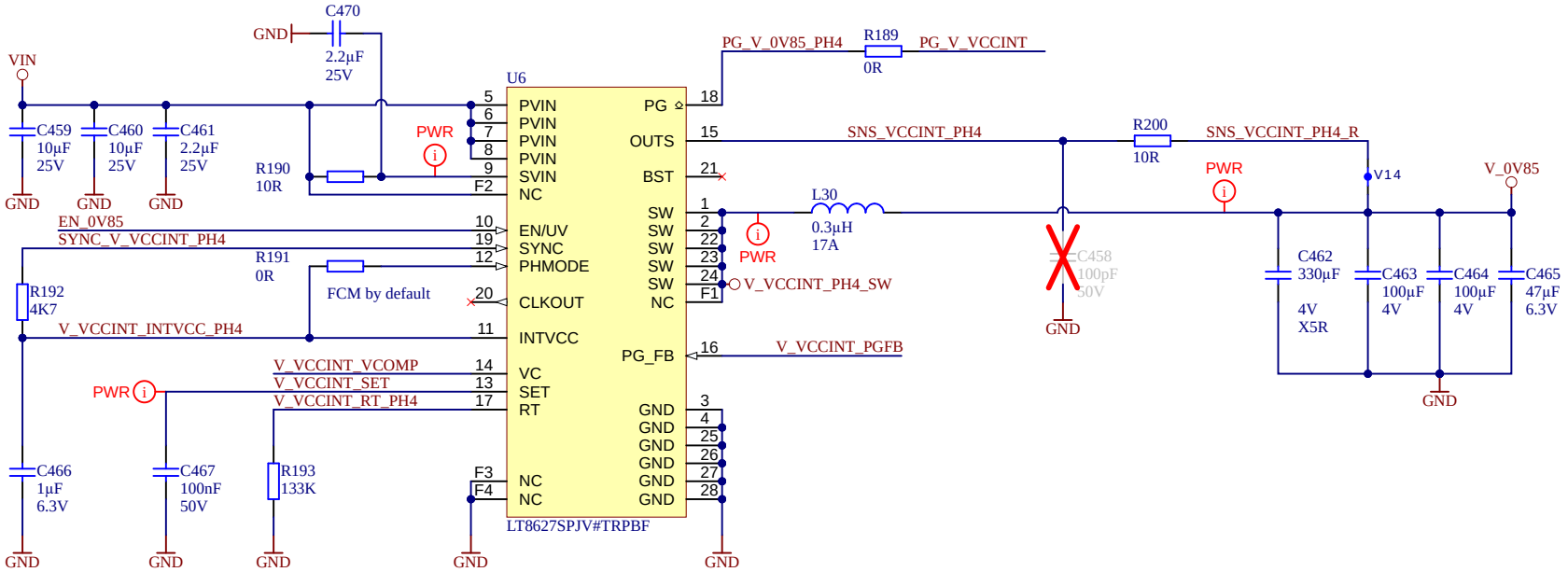
	Date: 2024-07-17	Copyright: Trenz Electronic GmbH	Page 18 of 39
	Filename: POWER_VCCINT_PH3.SchDoc		

VCCINT Phase 4/4, 0.85V, 45A, 15A per Phase



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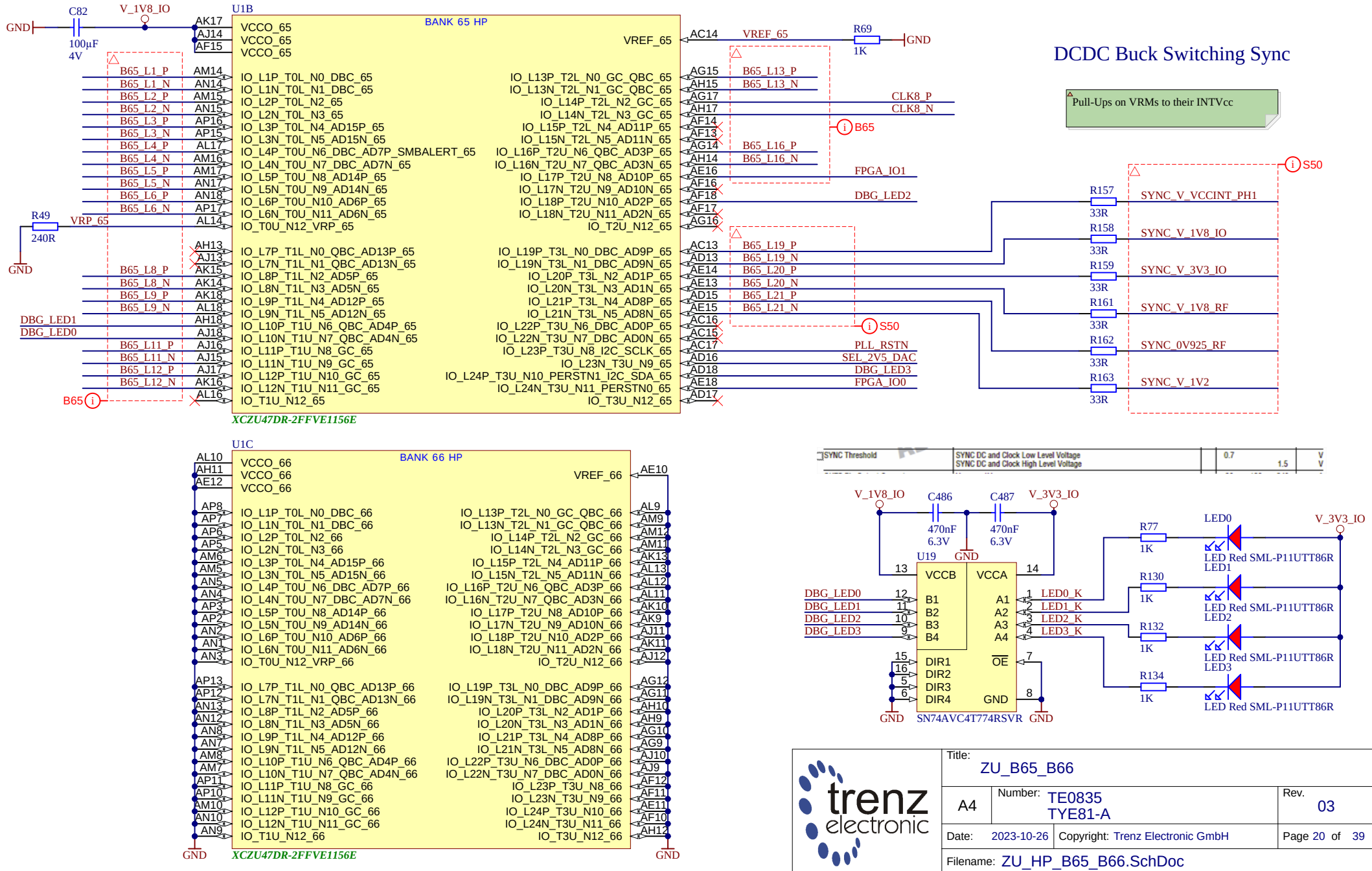
	Date: 2024-07-17	Copyright: Trenz Electronic GmbH	Page 19 of 39
	Filename: POWER_VCCINT_PH4.SchDoc		


DCDC Buck Switching Sync
Pull-Ups on VRMs to their INTVcc
U1B
BANK 65 HP
XCZU47DR-2FFVE1156E
U1C
BANK 66 HP
XCZU47DR-2FFVE1156E
U19
SN74AVC4T774RSVR
Title: ZU_B65_B66
A4
Number: TE0835 TYE81-A
Rev. 03
Date: 2023-10-26
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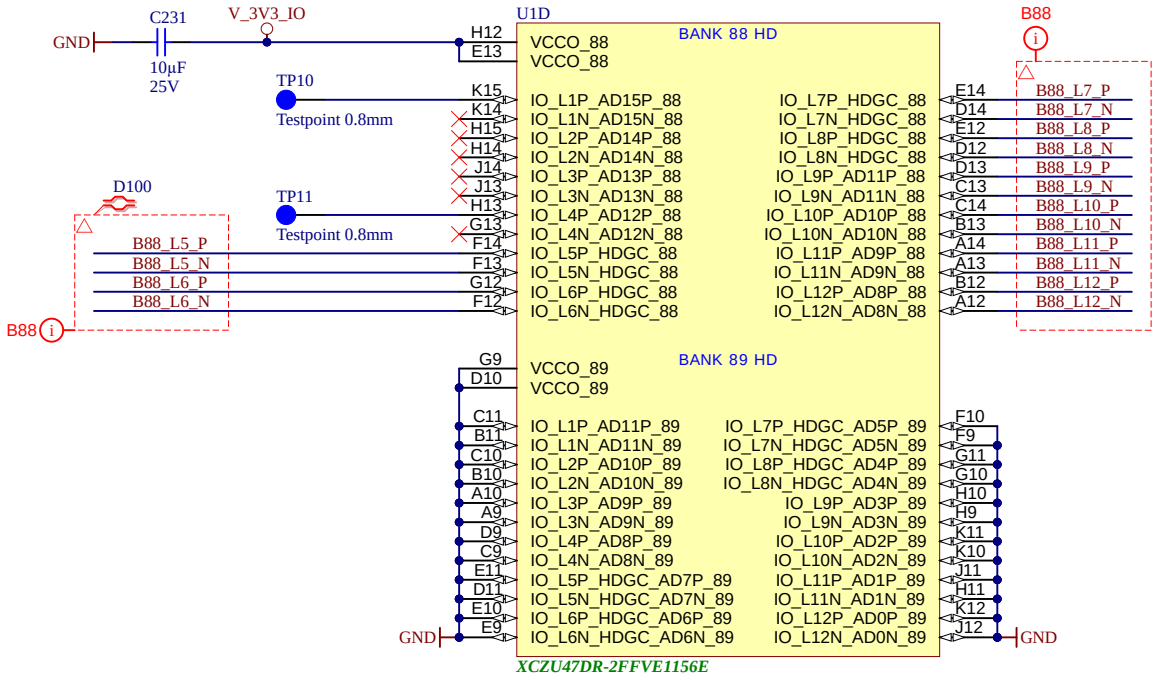
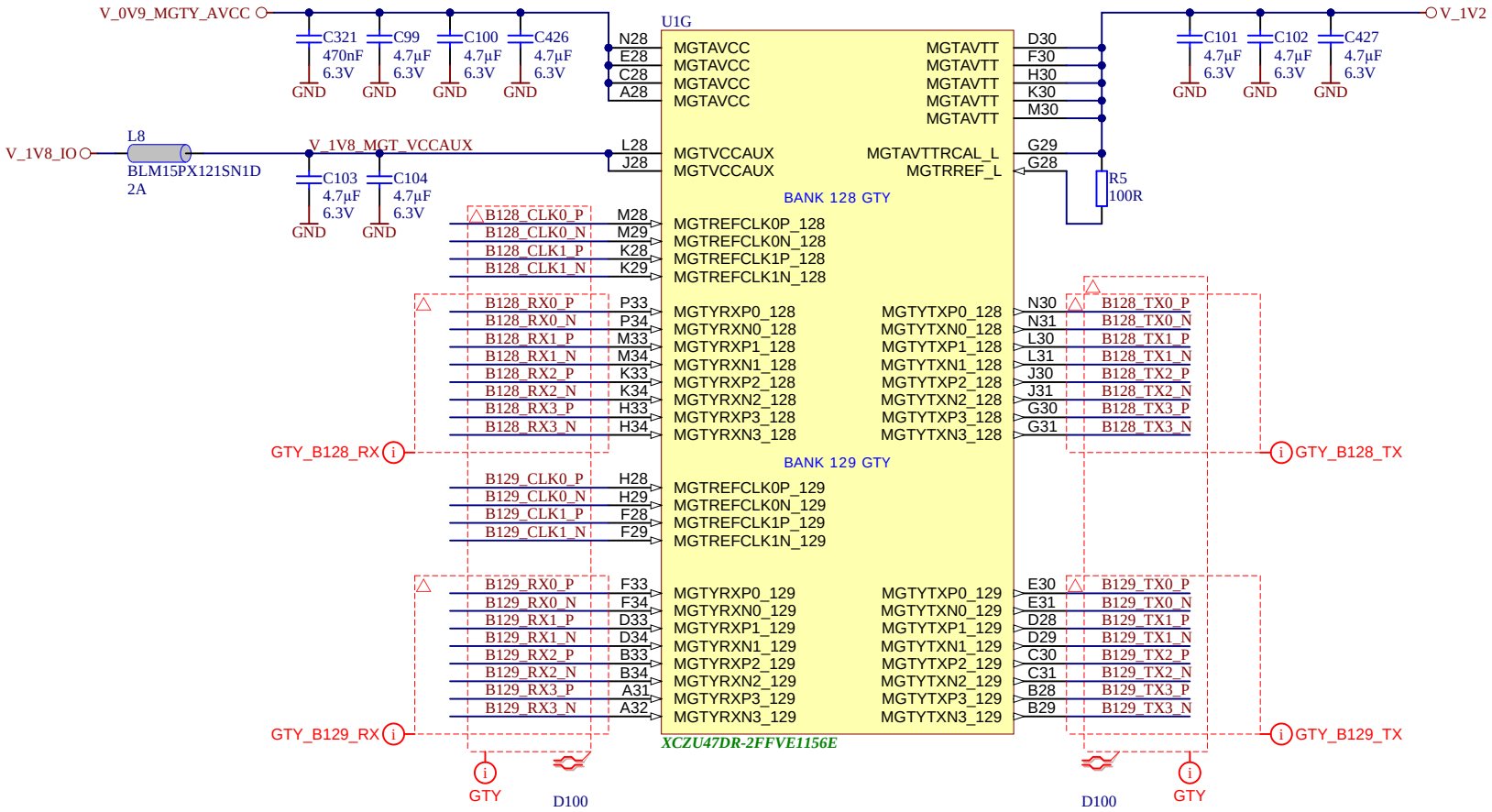
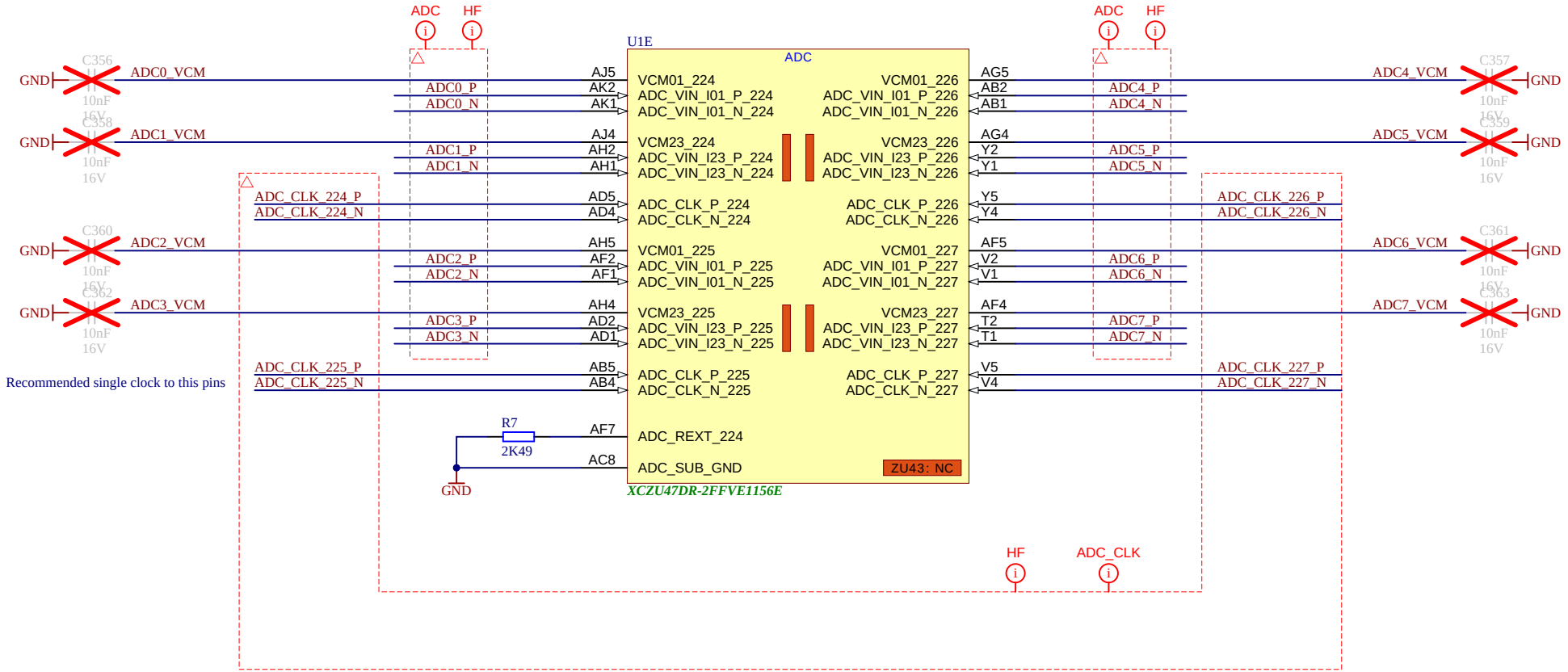
Page 20 of 39
Filename: ZU_HP_B65_B66.SchDoc



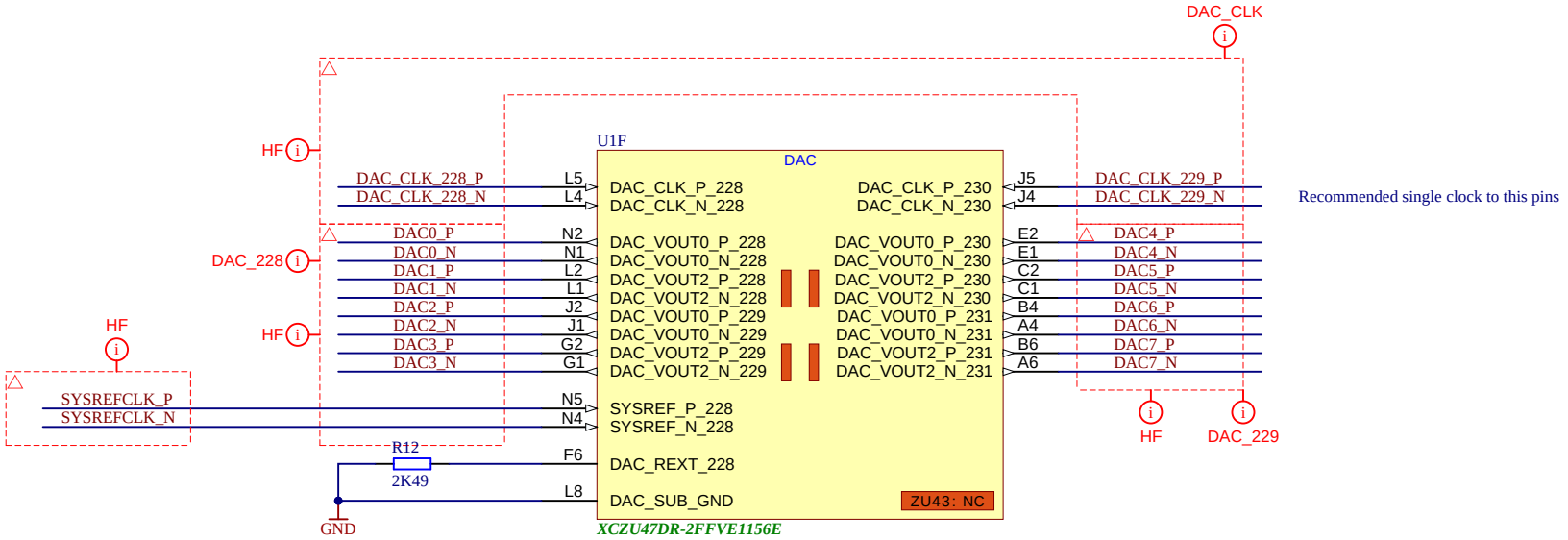
Title: ZU_HD			
A4	Number: TE0835 TYE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 21 of 39
Filename: ZU_HD_B88_B89.SchDoc			



trenz electronic	Title: ZU_MGT_L		
A4	Number: TE0835 TYE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 22 of 39
Filename: ZU_MGT_B128_B129.SchDoc			



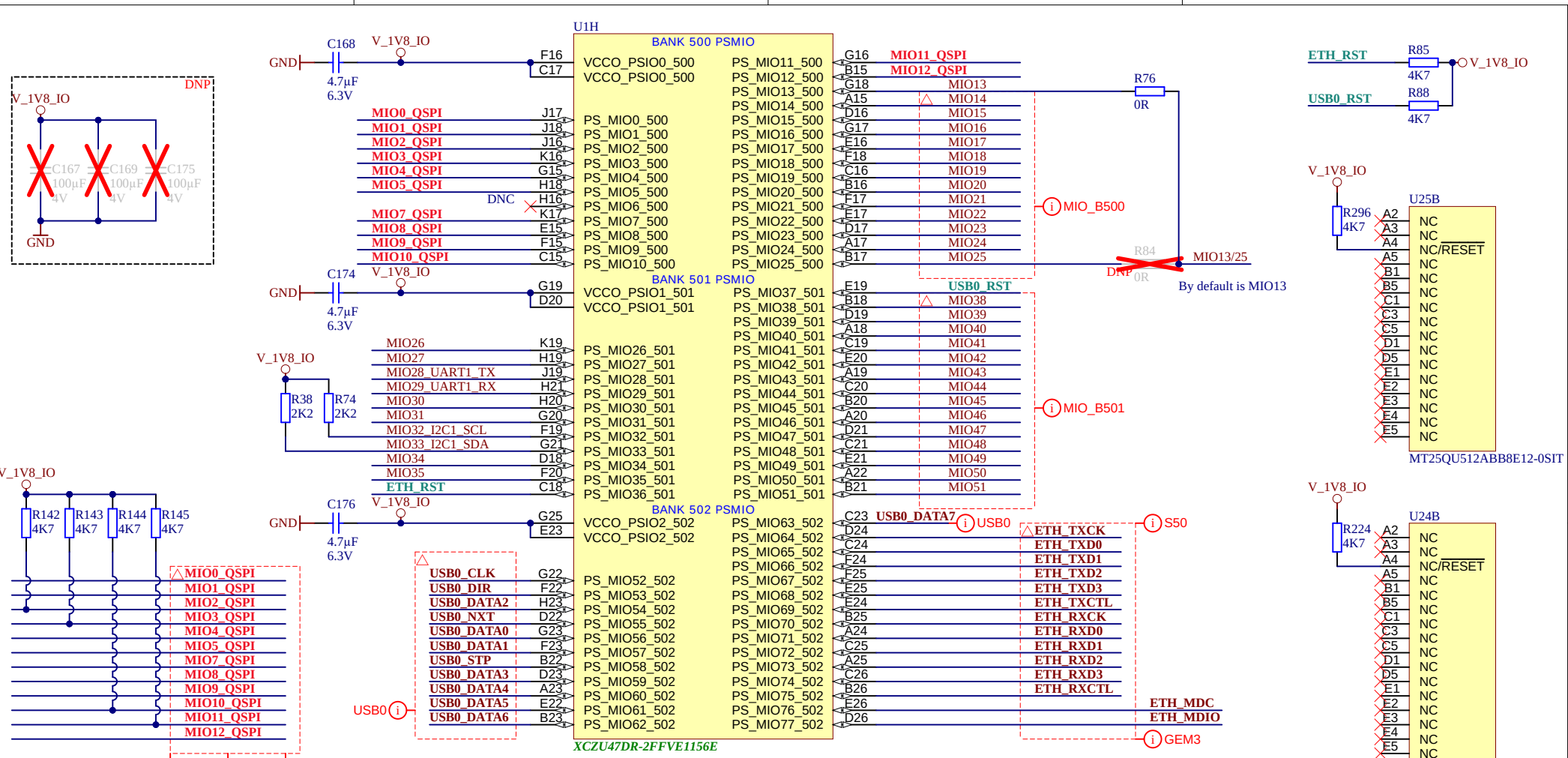
trenz electronic	Title: ZU_ADC		
	A4	Number: TE0835 TYE81-A	Rev. 03
	Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 23 of 39
	Filename: ZU_ADC_B224_B225_B226_B227.SchDoc		



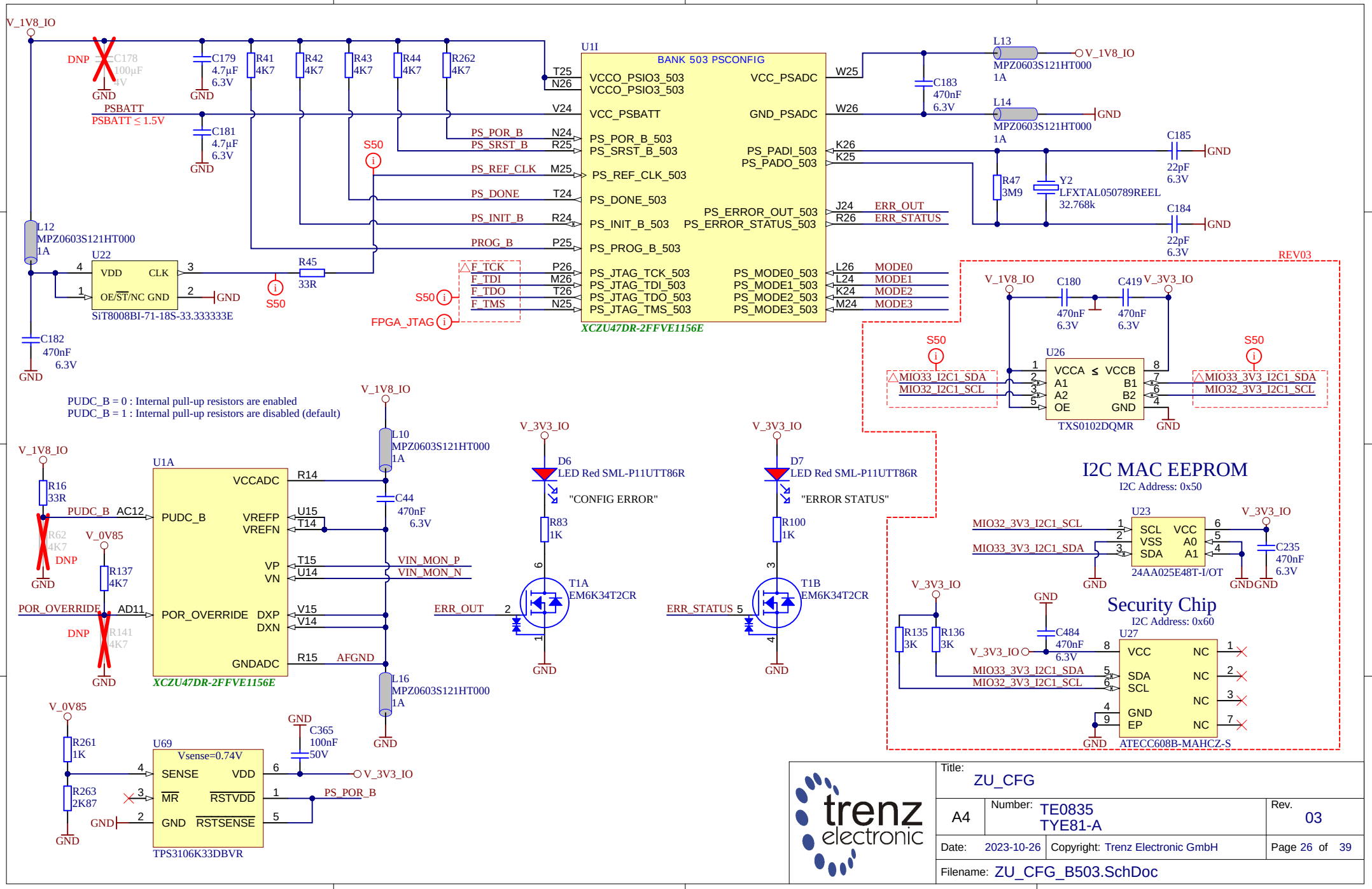
Recommended single clock to this pins

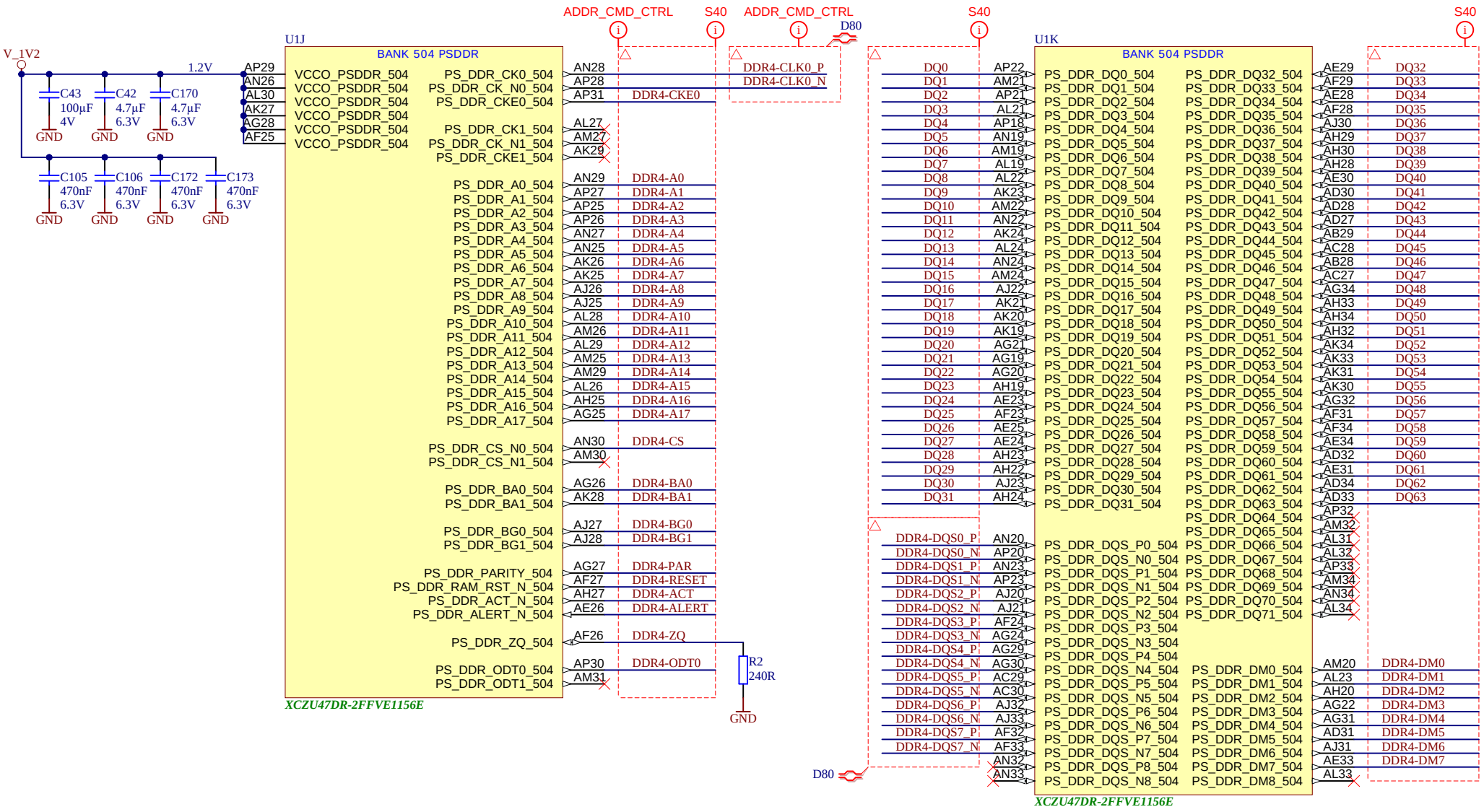
trenz electronic

Title: ZU_DAC		
A4	Number: TE0835 TYE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 24 of 39
Filename: ZU_DAC_B228_B229.SchDoc		

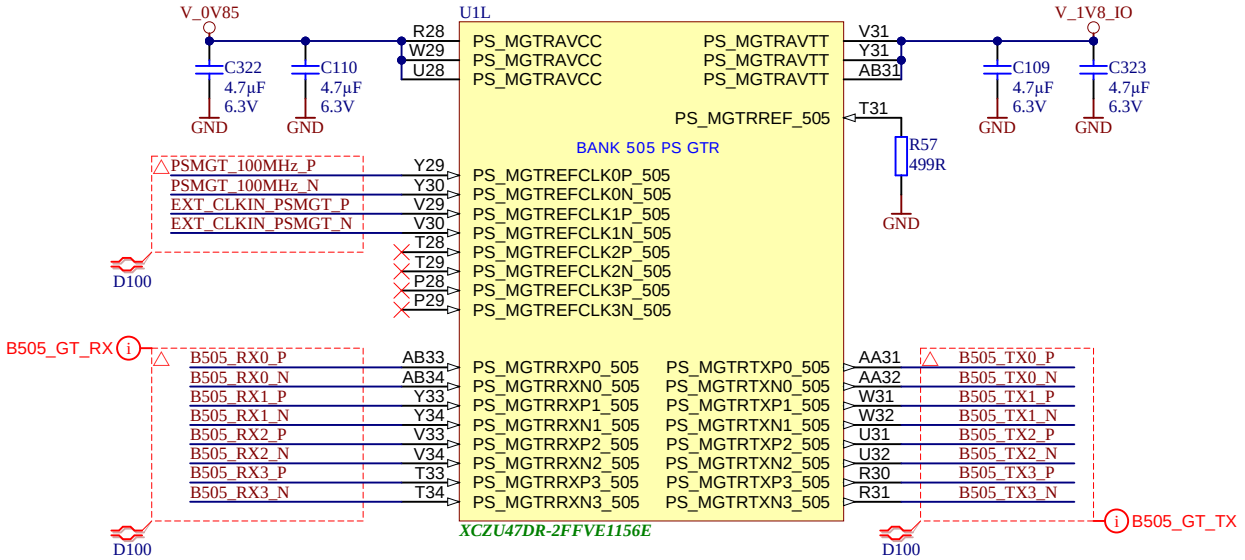


Title: ZU_MIO			
A4	Number: TE0835 TYE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 25 of 39
Filename: ZU_MIO_B500_B501_B502.SchDoc			

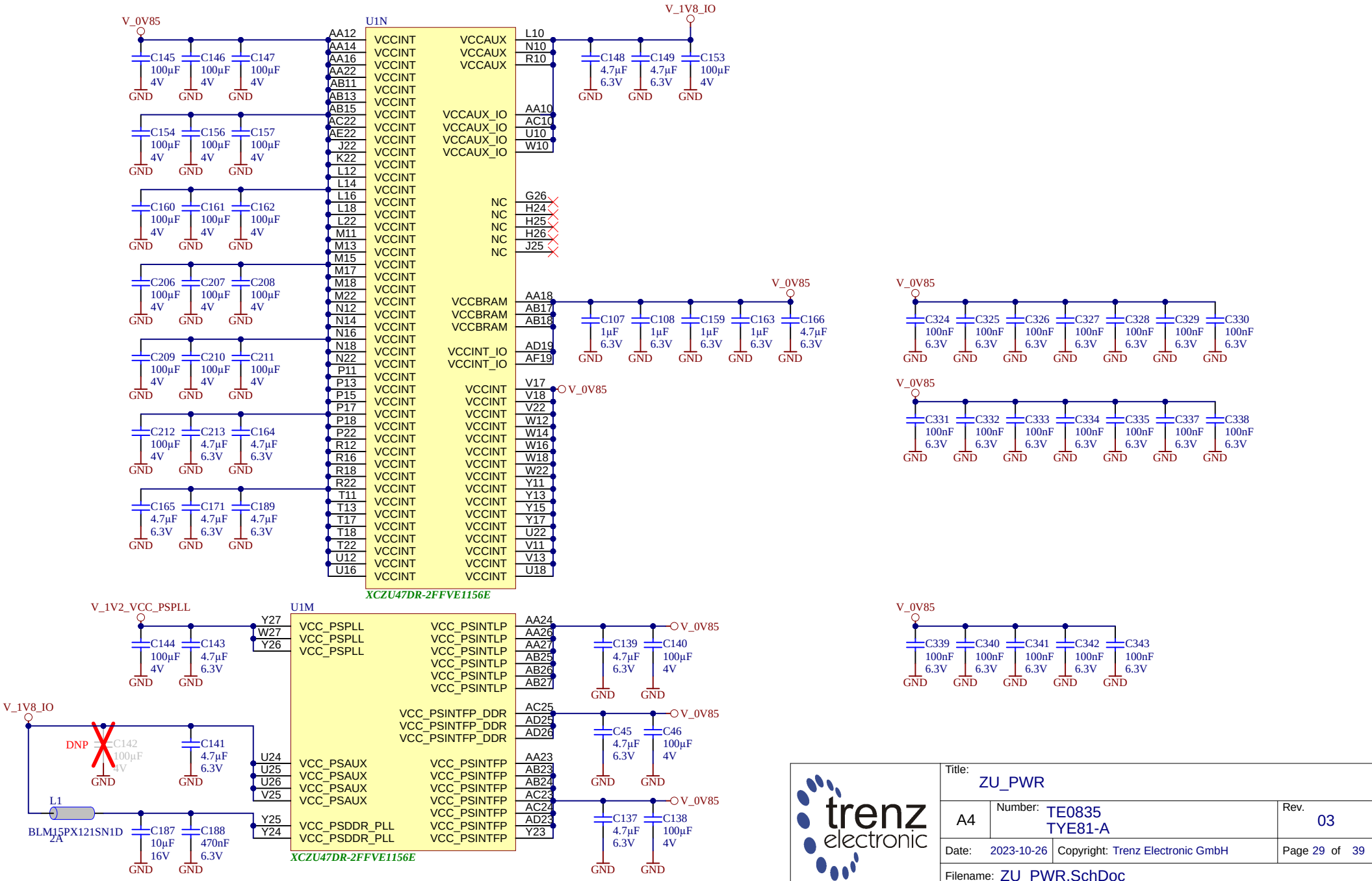

V_1V8_IO
DNP C178 100µF 4V
C179 4.7µF 6.3V
R41 4K7
R42 4K7
R43 4K7
R44 4K7
R262 4K7
GND
PSBATT
PSBATT ≤ 1.5V
C181 4.7µF 6.3V
U1I
BANK 503 PSCONFIG
VCCO_PSIO3_503
VCCO_PSIO3_503
VCC_PSBATT
PS_POR_B_503
PS_SRST_B_503
PS_REF_CLK_503
PS_DONE_503
PS_INIT_B_503
PS_PROG_B_503
PS_JTAG_TCK_503
PS_JTAG_TDI_503
PS_JTAG_TDO_503
PS_JTAG_TMS_503
VCC_PSADC
GND_PSADC
PS_PADI_503
PS_PADO_503
PS_ERROR_OUT_503
PS_ERROR_STATUS_503
PS_MODE0_503
PS_MODE1_503
PS_MODE2_503
PS_MODE3_503
T25
N26
V24
N24
R25
M25
T24
R24
P25
P26
M26
T26
N25
W25
W26
K26
K25
J24
R26
L26
L24
K24
M24
PS_POR_B
PS_SRST_B
PS_REF_CLK
PS_DONE
PS_INIT_B
PS_PROG_B
F_TCK
F_TDI
F_TDO
F_TMS
ERR_OUT
ERR_STATUS
MODE0
MODE1
MODE2
MODE3
XCZU47DR-2FFVE1156E
S50
FPGA_JTAG
L13 MPZ0603S121HT000 1A
L14 MPZ0603S121HT000 1A
C183 470nF 6.3V
C185 22pF 6.3V
C184 22pF 6.3V
R47 3M9
Y2 LFXTAL050789REEL 32.768k
L12 MPZ0603S121HT000 1A
U22
VDD CLK OE/ST/NC GND
SiT8008BI-71-18S-33.333333E
R45 33R
C182 470nF 6.3V
REV03
V_3V3_IO
C180 470nF 6.3V
C419 470nF 6.3V
U26
VCCA VCCB A1 A2 OE B1 B2 GND
TXS0102DQMR
MIO33_I2C1_SDA
MIO32_I2C1_SCL
MIO33_3V3_I2C1_SDA
MIO32_3V3_I2C1_SCL
PUDC_B = 0 : Internal pull-up resistors are enabled
PUDC_B = 1 : Internal pull-up resistors are disabled (default)
U1A
VCCADC PUDC_B VREFP VREFN VP VN POR_OVERRIDE DXP DXN GNDADC
R16 33R
R62 4K7 DNP
R137 4K7
R141 4K7 DNP
PUDC_B AC12
POR_OVERRIDE AD11
V_0V85
R14 R15 AFGND
U15 T14 T15 U14 V15 V14
VIN_MON_P VIN_MON_N
L10 MPZ0603S121HT000 1A
C44 470nF 6.3V
L16 MPZ0603S121HT000 1A
XCZU47DR-2FFVE1156E
D6 LED Red SML-P11UTT86R "CONFIG ERROR"
D7 LED Red SML-P11UTT86R "ERROR STATUS"
R83 1K
R100 1K
T1A EM6K34T2CR
T1B EM6K34T2CR
ERR_OUT
ERR_STATUS
I2C MAC EEPROM
I2C Address: 0x50
U23
SCL SDA VCC VSS A0 A1
24AA025E48T-I/OT
C235 470nF 6.3V
Security Chip
I2C Address: 0x60
U27
VCC SDA SCL GND EP NC
ATECC608B-MAHCZ-S
C484 470nF 6.3V
R135 3K
R136 3K
U69
Vsense=0.74V
SENSE VDD MR RSTVDD GND RSTSENSE
TPS3106K33DBVR
R261 1K
R263 2K87
C365 100nF 50V
PS_POR_B
trenz electronic
Title: ZU_CFG
A4
Number: TE0835 TYE81-A
Rev. 03
Date: 2023-10-26
Copyright: Trenz Electronic GmbH
Page 26 of 39
Filename: ZU_CFG_B503.SchDoc

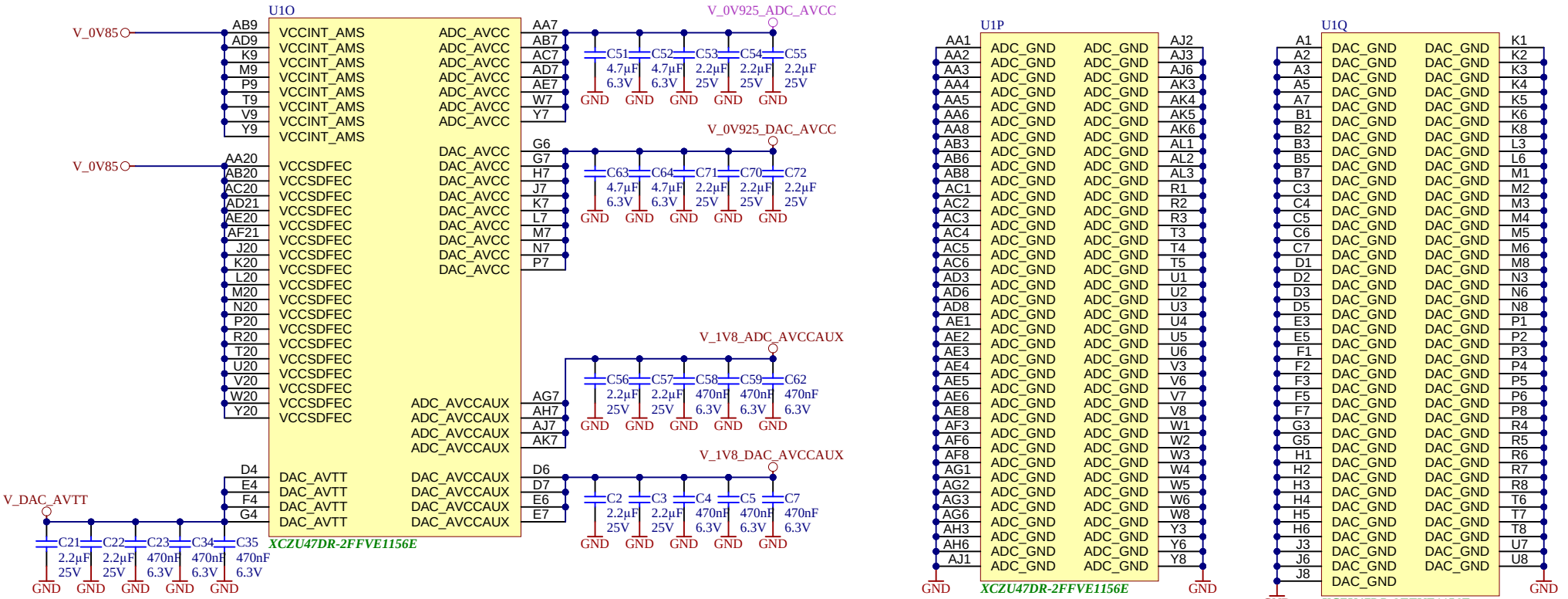


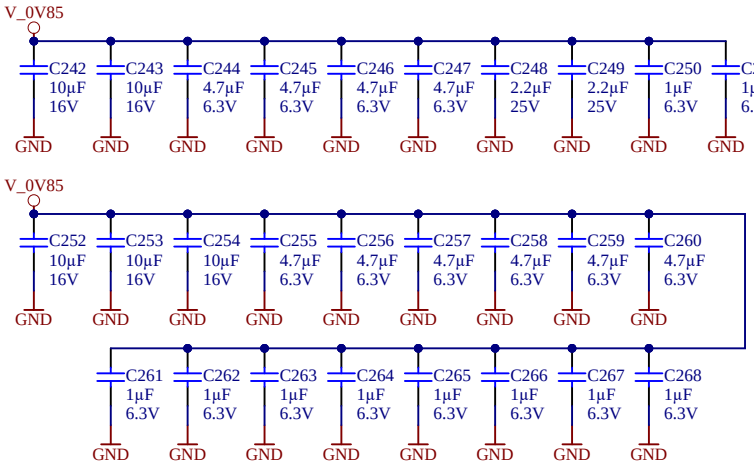
trenz electronic	Title: ZU_PSDDR		
A4	Number: TE0835 TYE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 27 of 39
Filename: ZU_PSDDR_B504.SchDoc			

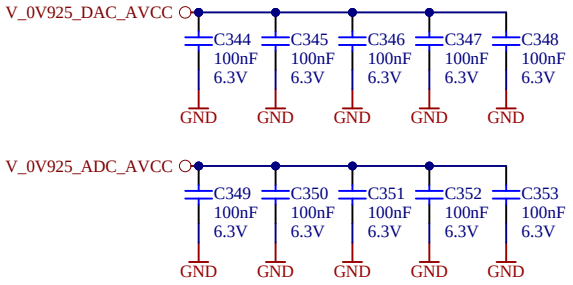


trenz electronic	Title: ZU_PSMGT		
	A4	Number: TE0835 TYE81-A	Rev. 03
	Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 28 of 39
	Filename: ZU_PSMGT_B505.SchDoc		


U1N
V_0V85
V_1V8_IO
XCZU47DR-2FFVE1156E
U1M
V_1V2_VCC_PSPLL
V_1V8_IO
DNP
L1
BLM15PX121SN1D
2A
XCZU47DR-2FFVE1156E
trenz electronic
Title: ZU_PWR
A4
Number: TE0835 TYE81-A
Rev. 03
Date: 2023-10-26
Copyright: Trenz Electronic GmbH
Page 29 of 39
Filename: ZU_PWR.SchDoc







Title: ZU_PWR2			
A4	Number: TE0835 TYE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 30 of 39
Filename: ZU_PWR_RF.SchDoc			

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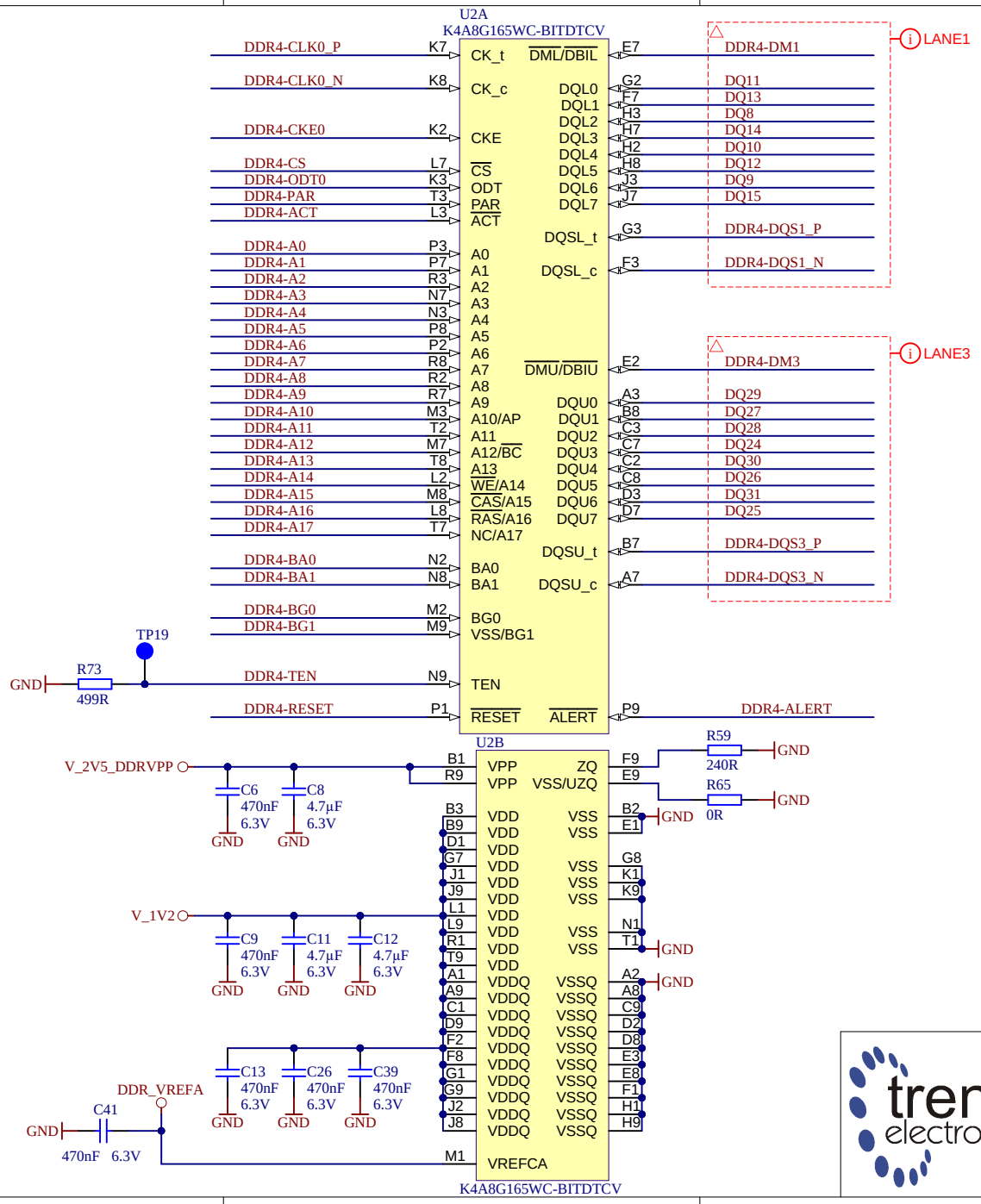
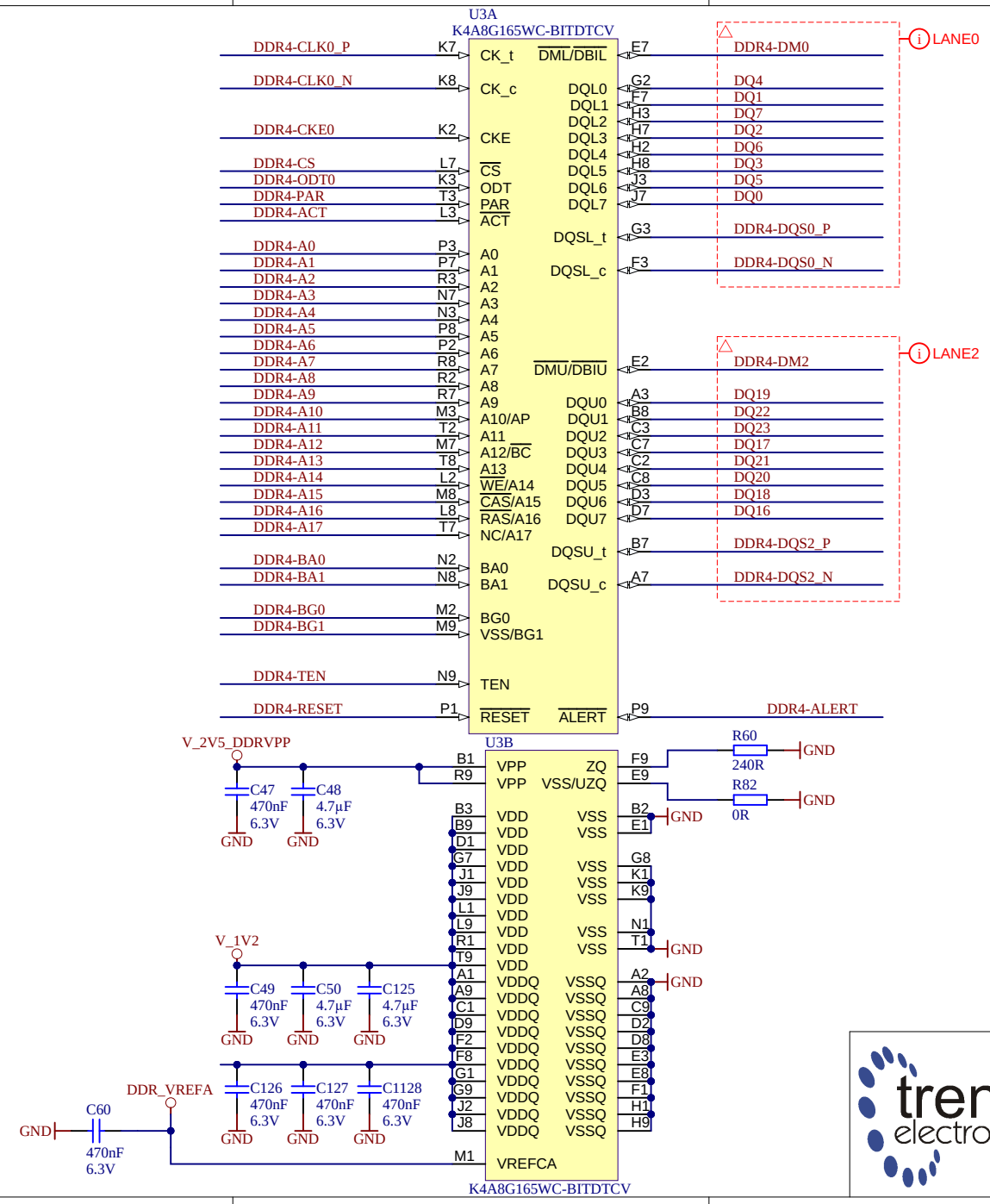
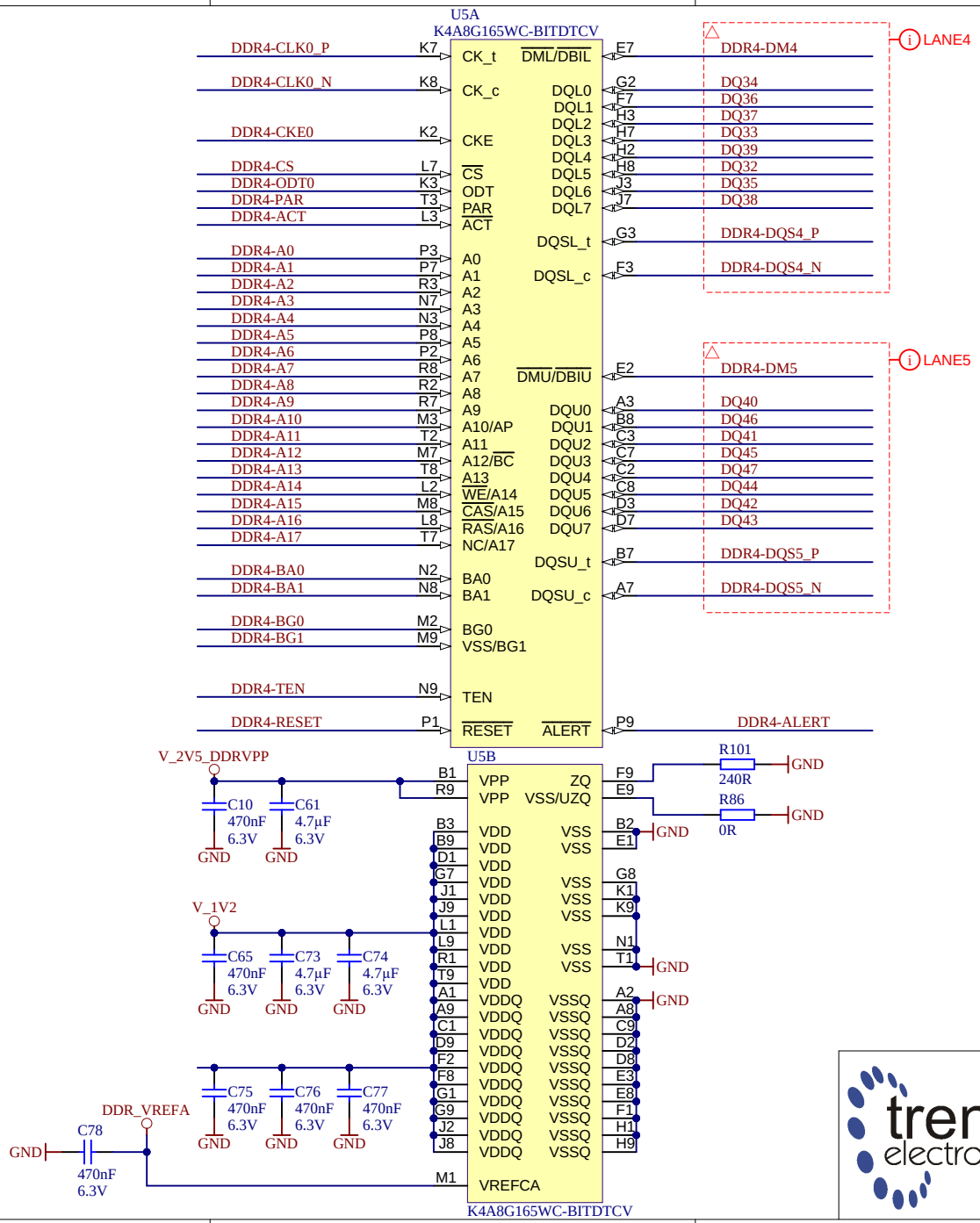
Title: ZU_PWR3		
A4	Number: TE0835 TYE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 31 of 39
Filename: ZU_GND.SchDoc		



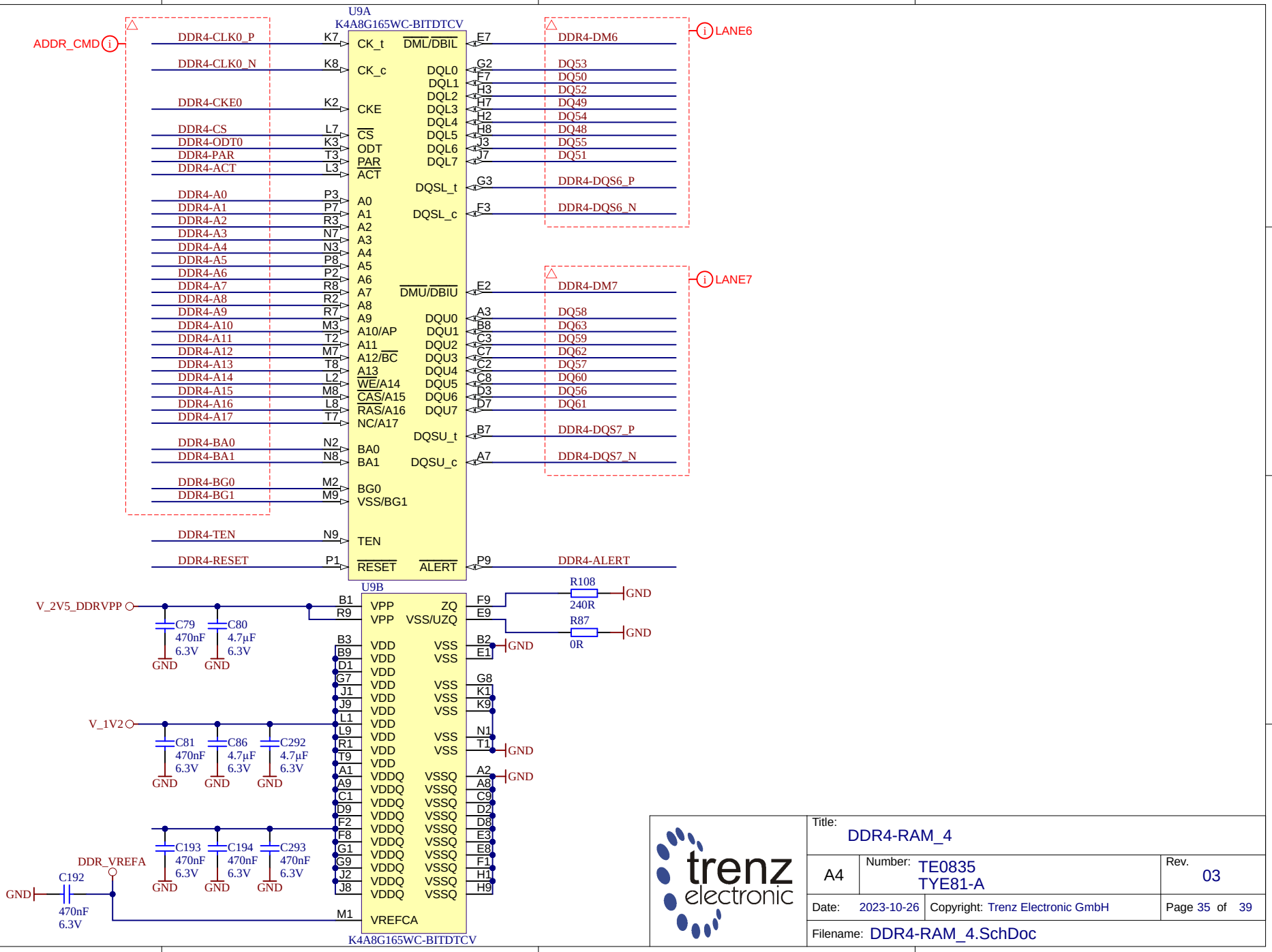
Title: DDR4-RAM_1			
A4	Number: TE0835 TYE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 32 of 39
Filename: DDR4-RAM_1.SchDoc			



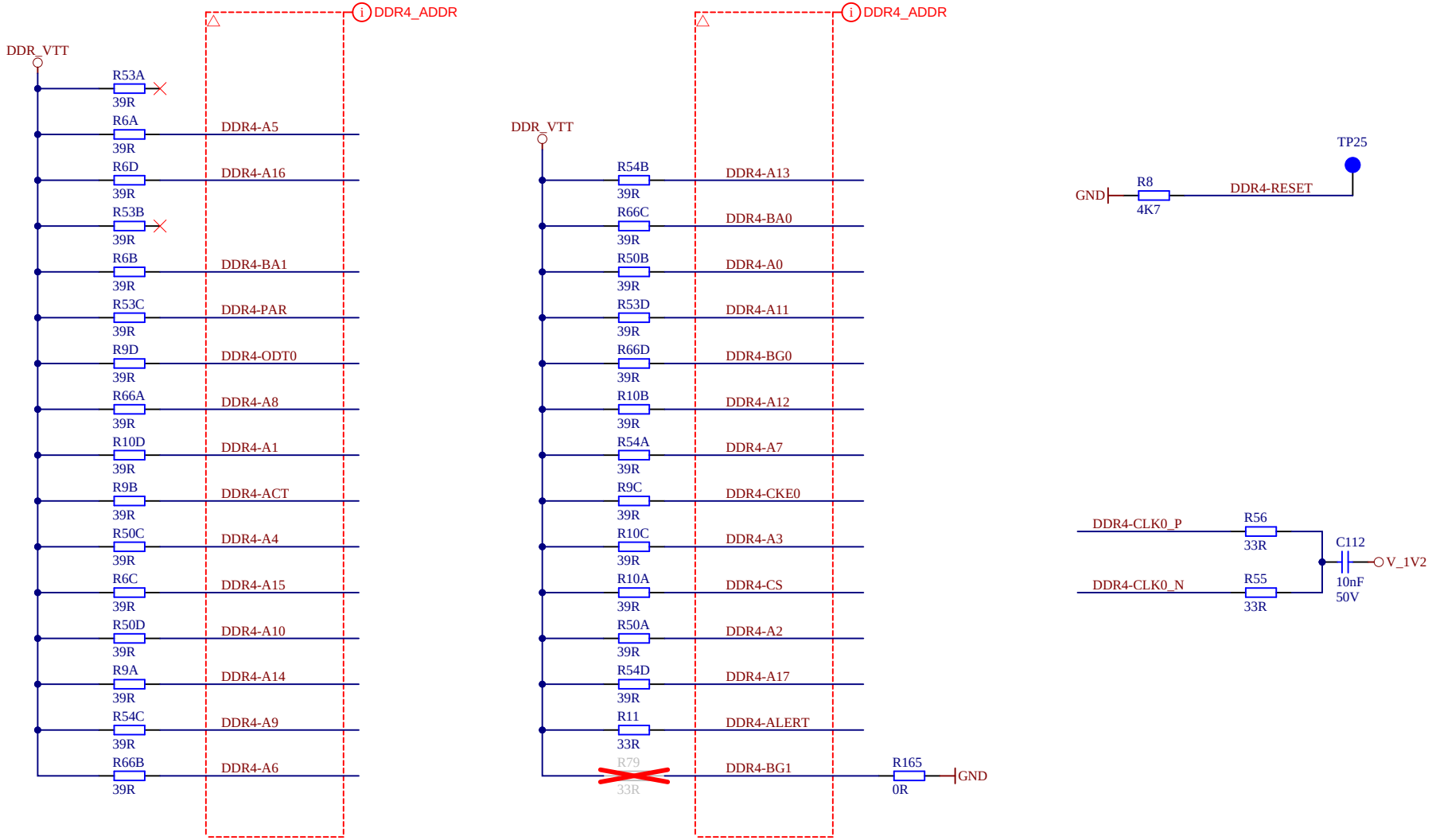
Title: DDR4-RAM_2			
A4	Number: TE0835 TYE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 33 of 39
Filename: DDR4-RAM_2.SchDoc			



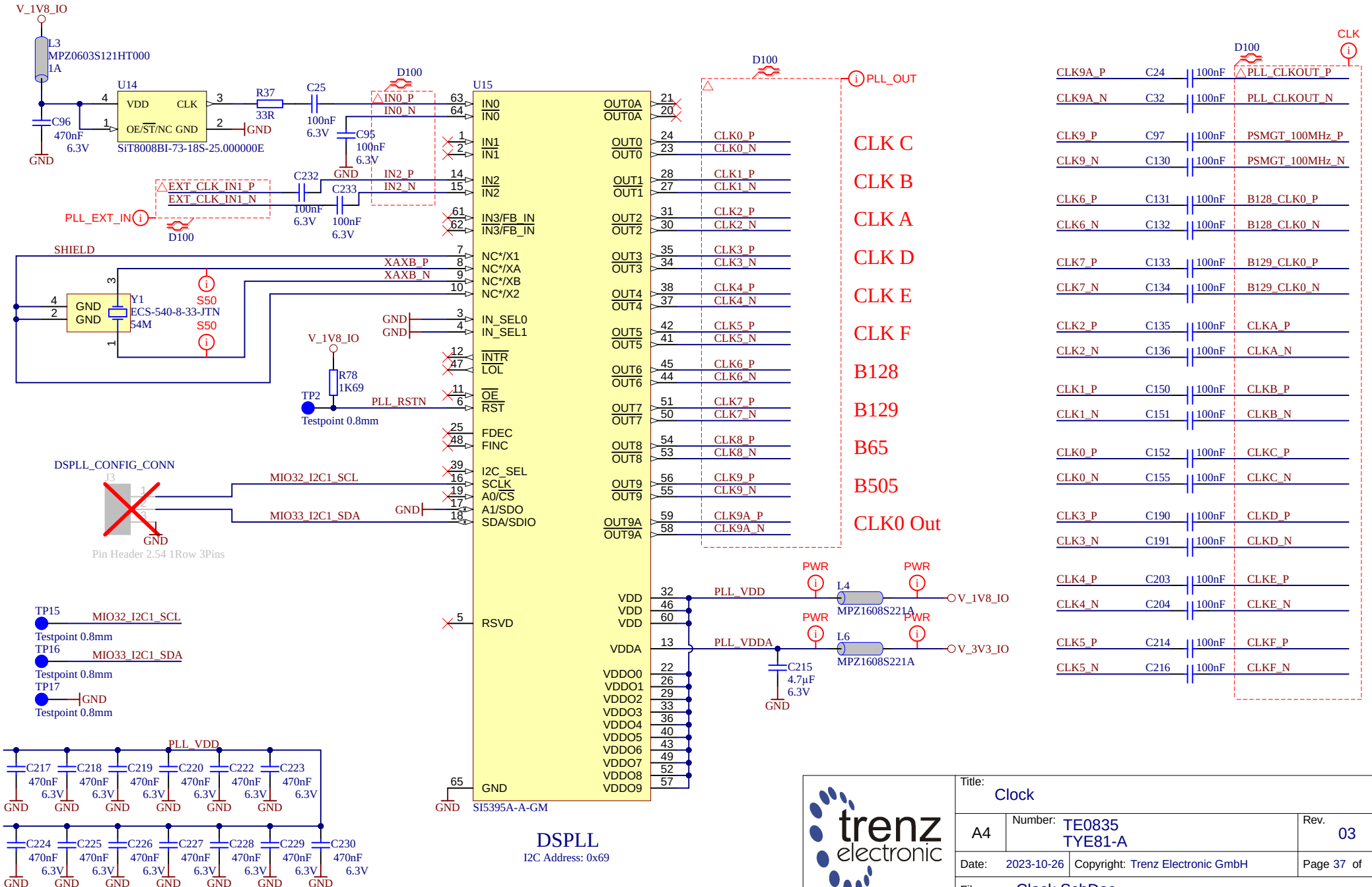
trenz electronic	Title: DDR4-RAM_3		
	A4	Number: TE0835 TYE81-A	Rev. 03
	Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 34 of 39
	Filename: DDR4-RAM_3.SchDoc		



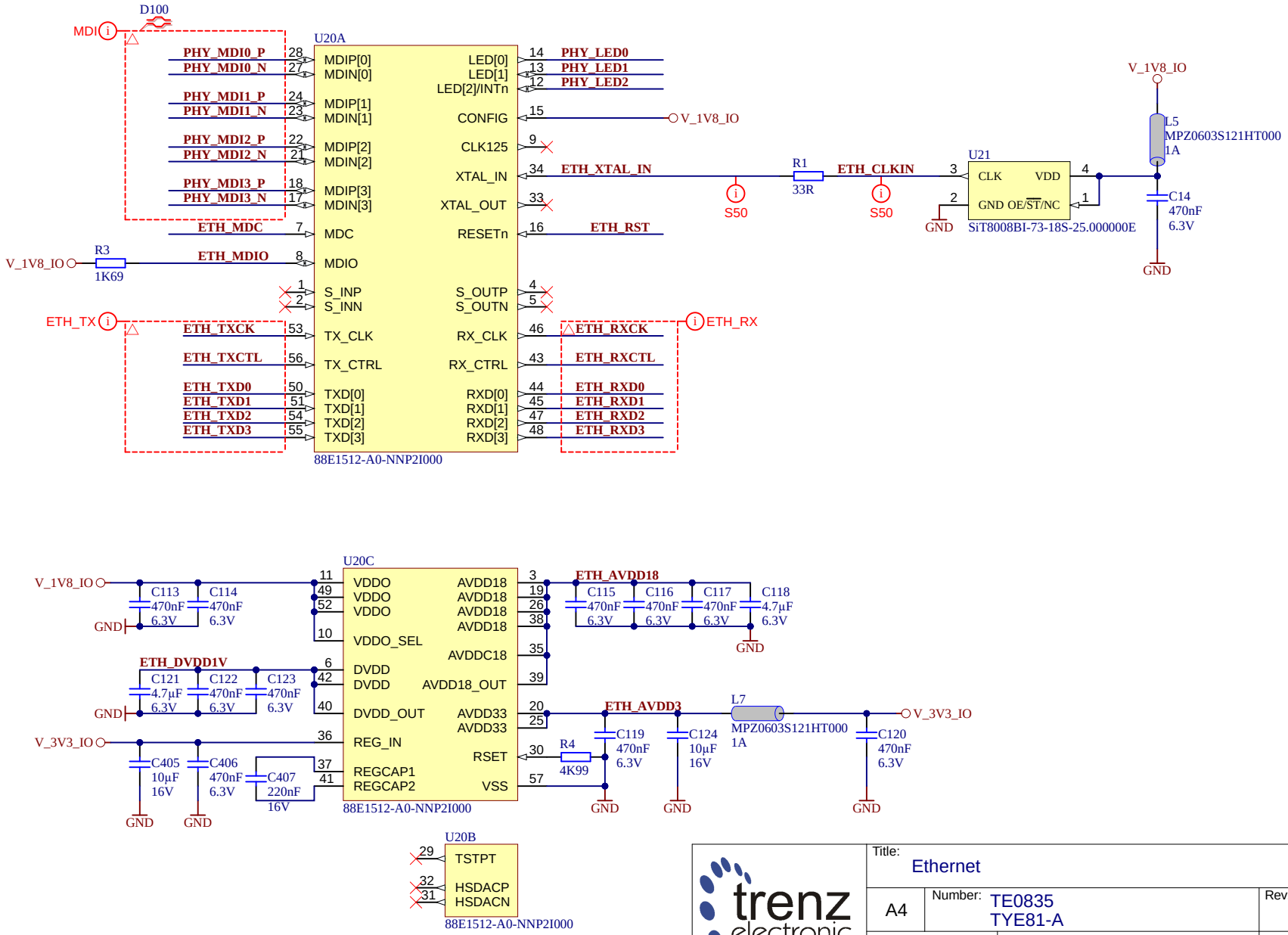
	Title: DDR4-RAM_4		
A4	Number: TE0835 TYE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 35 of 39
Filename: DDR4-RAM_4.SchDoc			



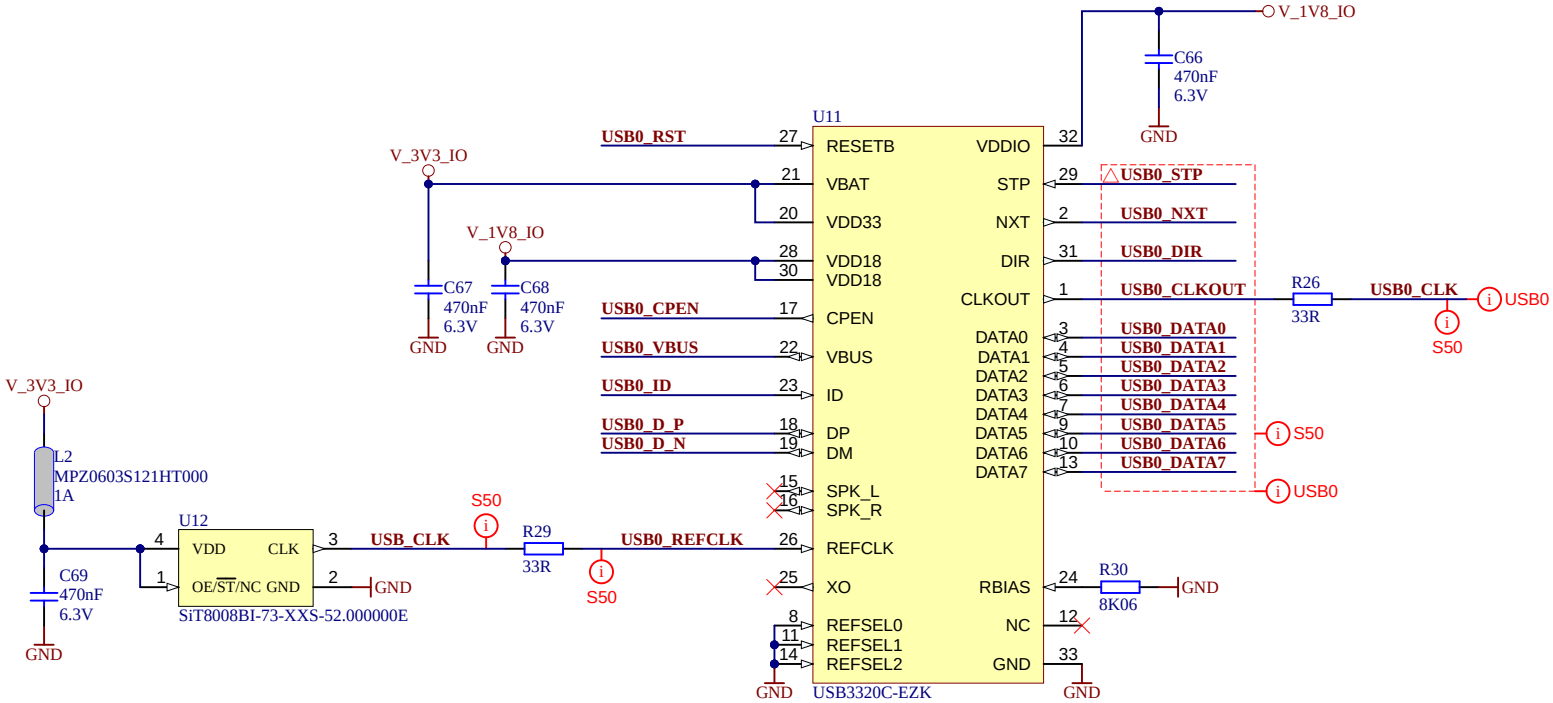
trenz electronic	Title: DDR4-TERM		
A4	Number: TE0835 TYE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 36 of 39
Filename: DDR4-TERM.SchDoc			



Title: Clock			
A4	Number: TE0835 TYE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 37 of 39
Filename: Clock.SchDoc			



Title: Ethernet			
A4	Number: TE0835 TYE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 38 of 39
Filename: Ethernet.SchDoc			



trenz electronic	Title: USB-PHY		
A4	Number: TE0835 TYE81-A		Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH		Page 39 of 39
Filename: USB-PHY.SchDoc			