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Schematics and other handouts serve for informational purposes only!

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REVISION HISTORY

REV	Description	
-01	Initial revision	IG
-02	<ol style="list-style-type: none"> Added a VRP resistor on bank 65; LDO U33 is changed on ADP7102ACPZ; Signal FPGA IO0 is connected on AE18 pin of FPGA; Signal DBG_LED3 is connected on AD18 pin of FPGA; Signal MIO13_25 connected to J1 pin 33 instead MIO25. Resistor R84 is removed; LED D1 moved on edge of PCB; Added THT testpoints J4 on CPLD_JTAGEN, R76 was removed; Signals B49_XX_X are renamed in B88_XX_X; C241 is changed on 1nF; Length of CLK signals on RFADC and RFDAC are adjusted; Wrong connection on U8 is fixed (PCB); Wrong connection PGOOD1 pin of U7 is fixed; R17 is changed from 35,5K to 33K for VCC_PL_PS correction. 	IG
-02	<ol style="list-style-type: none"> APRE_3V3 renamed to APRE_4V5, voltage of the power rail increased from 3.3V to 4,58V. Resistor R15 is changed from 13,3K to 9,09K. AN: 24671->25969 Capacitor C27 is changed from 100uF x 4V to 47uF x 6,3V. AN: 28940->24718 	IG
-03	<ol style="list-style-type: none"> Added Legal Notices. Added Power Diagram. Added a DC-DCs synchronization circuit to spread spectrum. Changed the core power supply schematic to 4 phases to increase current and reduce noise. The power supply circuit of the module supports input voltage 5...12V. EOL components are replaced: <ol style="list-style-type: none"> L10, L12, L13, L14, L16 Ferrit beads BKP0603HS121-T replaced with MPZ0603S121HT000. Updated layerstack to enhance power supply circuits and improve signal impedance matching. Added POR_OVERRIDE configuration. U25 (Pin 33) PS_SRST_B signal was removed. POR_OVERRIDE_N connected. Added transistor T2A. C180 is removed from schematic. Networks to power the banks have been renamed. Added Level shifter U19. LEDs renamed: D1 --> LED0; D2 --> LED1; D3 --> LED2; D4 --> LED3 and connected to V_3V3_IO. Resistors R77A, R77B, R77C, R77D (39 R) replaced with R77, R130, R132, R134 (1K) respectively according to new schematic. Added pull-up resistors R157, R158, R159, R161, R162, R163 to synchronise the power supplies. Added resistors R142-R145. U23 connected to V_3V3_IO (was 1.8V). ZU_PWR: L9 removed from schematic. Added resistors R46, R90, R98, R146, R149. Added U44. U33 (ADP7102ACPZ) replaced with MIC5504-3.3YMT. Added two capacitors 4.7uF C355 and C488 on DDR_VTT. Added signal SEL_2V5_DAC to Bank 65HP. Pin AD16. Capacitors C24, C32, C97, C130-136, 150-152, 155, 190,191, C203, C204, C214, C216 are replaced with 100 nF. Y1 CX3225SB54000 is EOL, it is replaced with ECS-540-8-33-JTN-TR Added a VIN voltage sensor R121, R124, R150, R122, R153, C489. Added R154, R155 to implement I2C interface between SC and RFSoc. Clock CLK0A_100MHz renamed to PLL_CLKOUT 	IG 27.03.2024

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Special notes:

- U_PWR-DIAGRAM
- U_FPGA-PWR
- U_FPGA-PWR_RF
- U_FPGA-GND
- POWER_STDBY_BIAS
- POWER_VCCINT_PH1
- POWER_VCCINT_PH2
- POWER_VCCINT_PH3
- POWER_VCCINT_PH4
- POWER_IV2
- POWER_IO_1V8
- POWER_IO_3V3
- POWER_MGT
- POWER_RF
- POWER_RF_1V8
- POWER_DDR

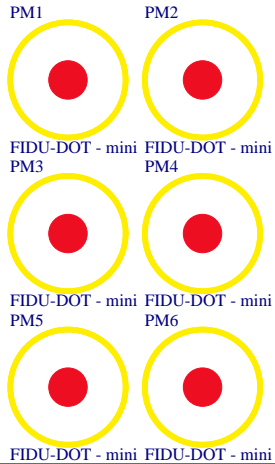
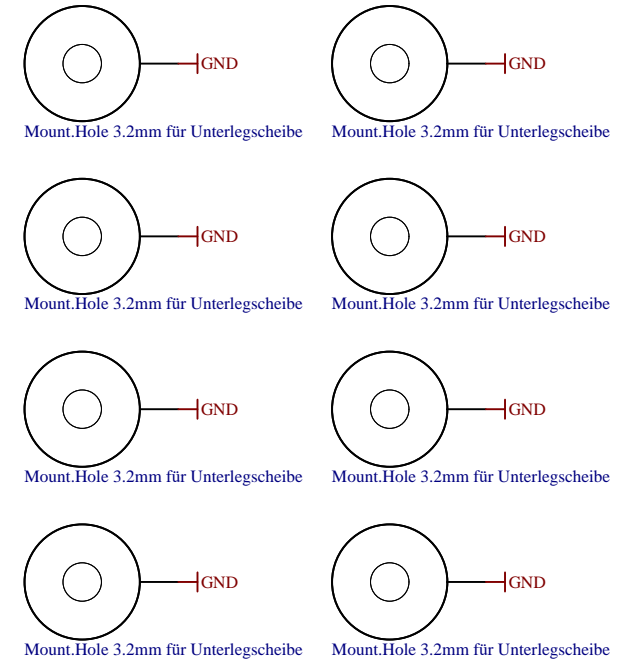
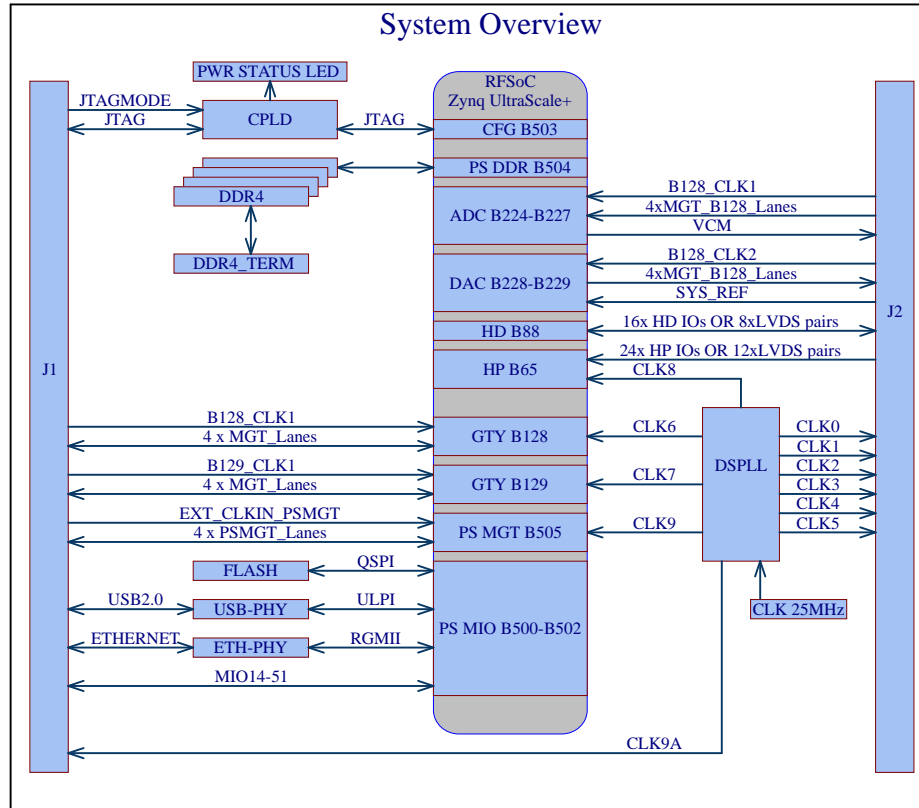


Table of I2C devices and addresses

Designator	I2C Address	Description
U23	0x50	I2C MAC EEPROM
U27	0x60	Security Chip
U15	0x69	DSPLL

LOGO1
TE Logo PRINT Layer
LOGO PRINT

MECH1
TE Address Overlay
LOGO ADDRESS

S/N
Serial
Serialnumber 6,3 x 6.3mm

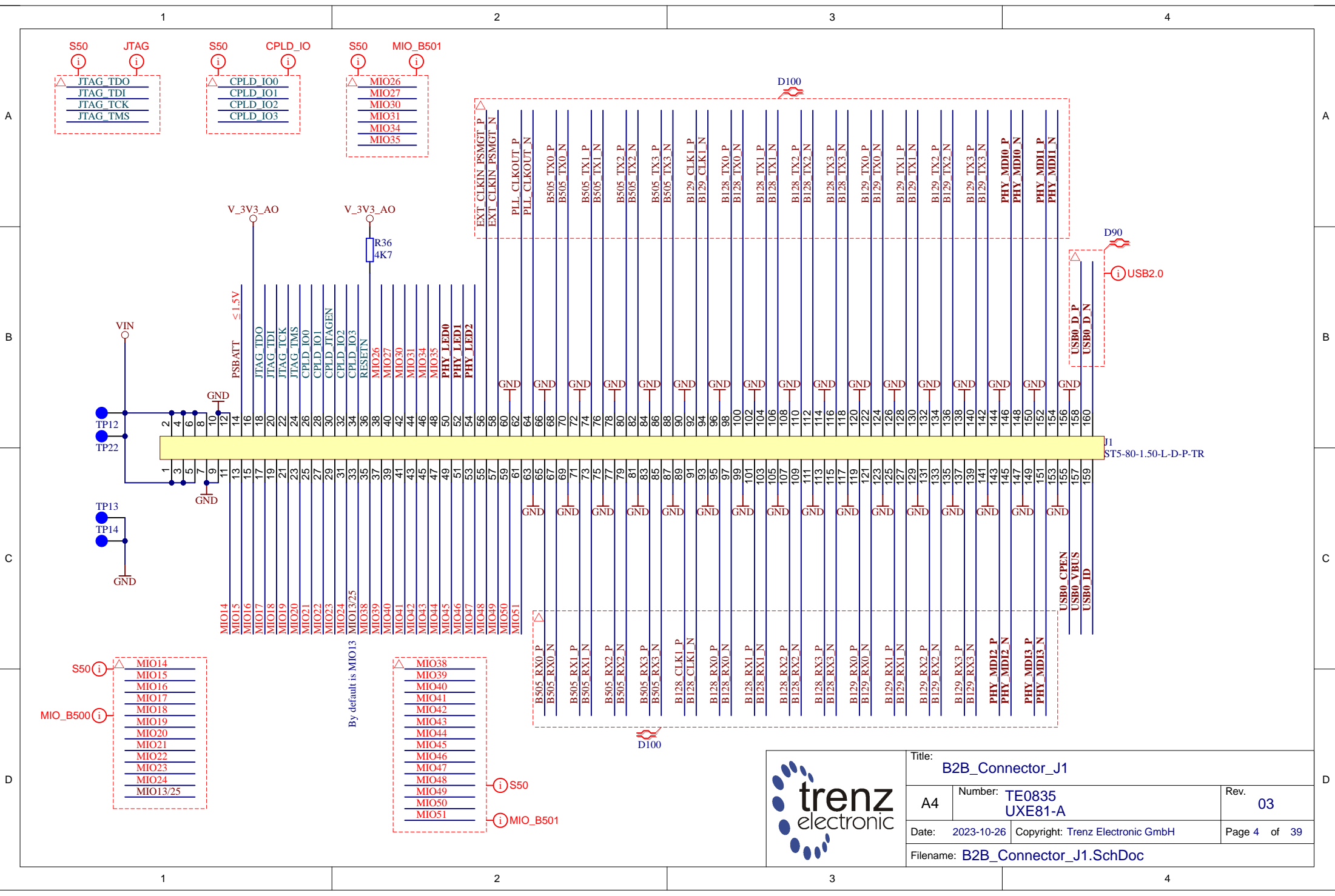
UKCA
UKCA Logo on Top Overlay
UKCA-TOPOVERLAY

Design drawn by: IG
Checked by: MR
Assembly variant: UXE81-A
Created by: IG
Modified by: IG
Modified at: 2024-02-19

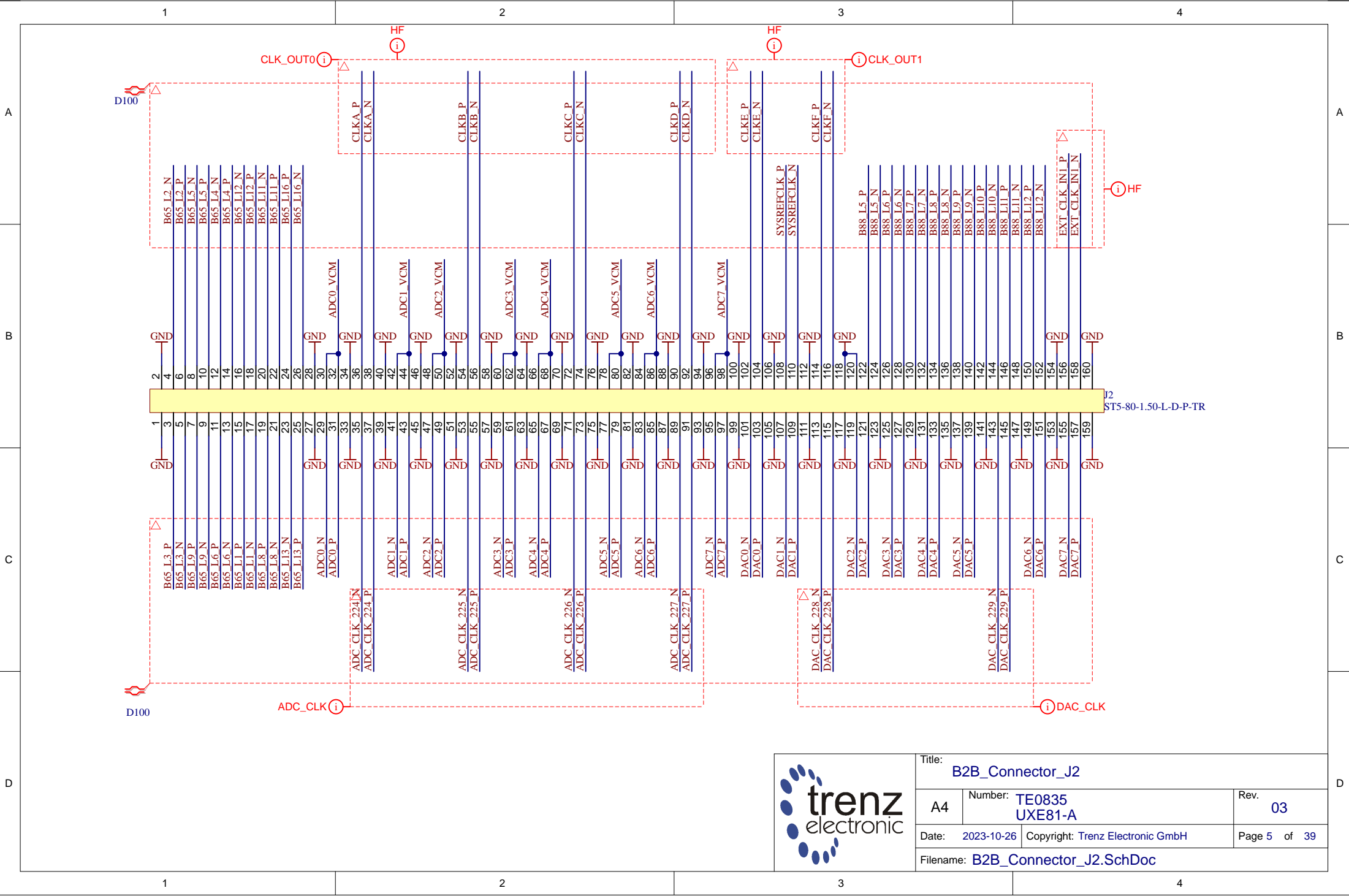


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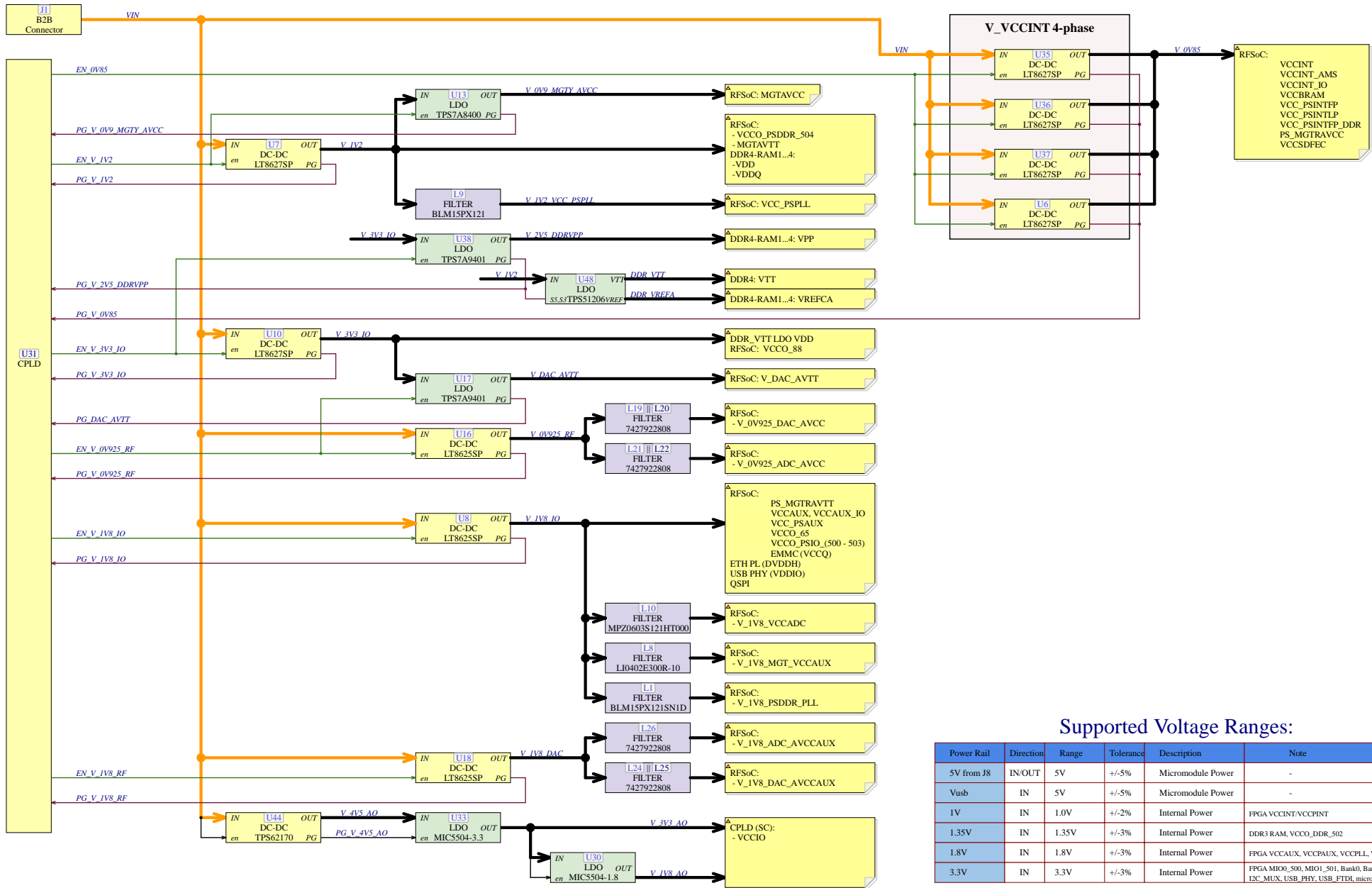


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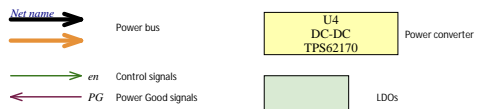
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Filename: B2B_Connector_J2.SchDoc		Page 5 of 39

Power-on sequencing:



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
5V from J8	IN/OUT	5V	+/-5%	Micromodule Power	-
Vusb	IN	5V	+/-5%	Micromodule Power	-
1V	IN	1.0V	+/-2%	Internal Power	FPGA VCCINT/VCCPINT
1.35V	IN	1.35V	+/-3%	Internal Power	DDR3 RAM, VCCO_DDR_502
1.8V	IN	1.8V	+/-3%	Internal Power	FPGA VCCAUX, VCCPACC, VCCPLL, VCCBATT, AVCC, SC
3.3V	IN	3.3V	+/-3%	Internal Power	FPGA MIO0_500, MIO1_501, Bank0, Bank34, Bank35 I2C_MUX, USB_PHY, USB_FTDI, micro SD, USB Hub, SC



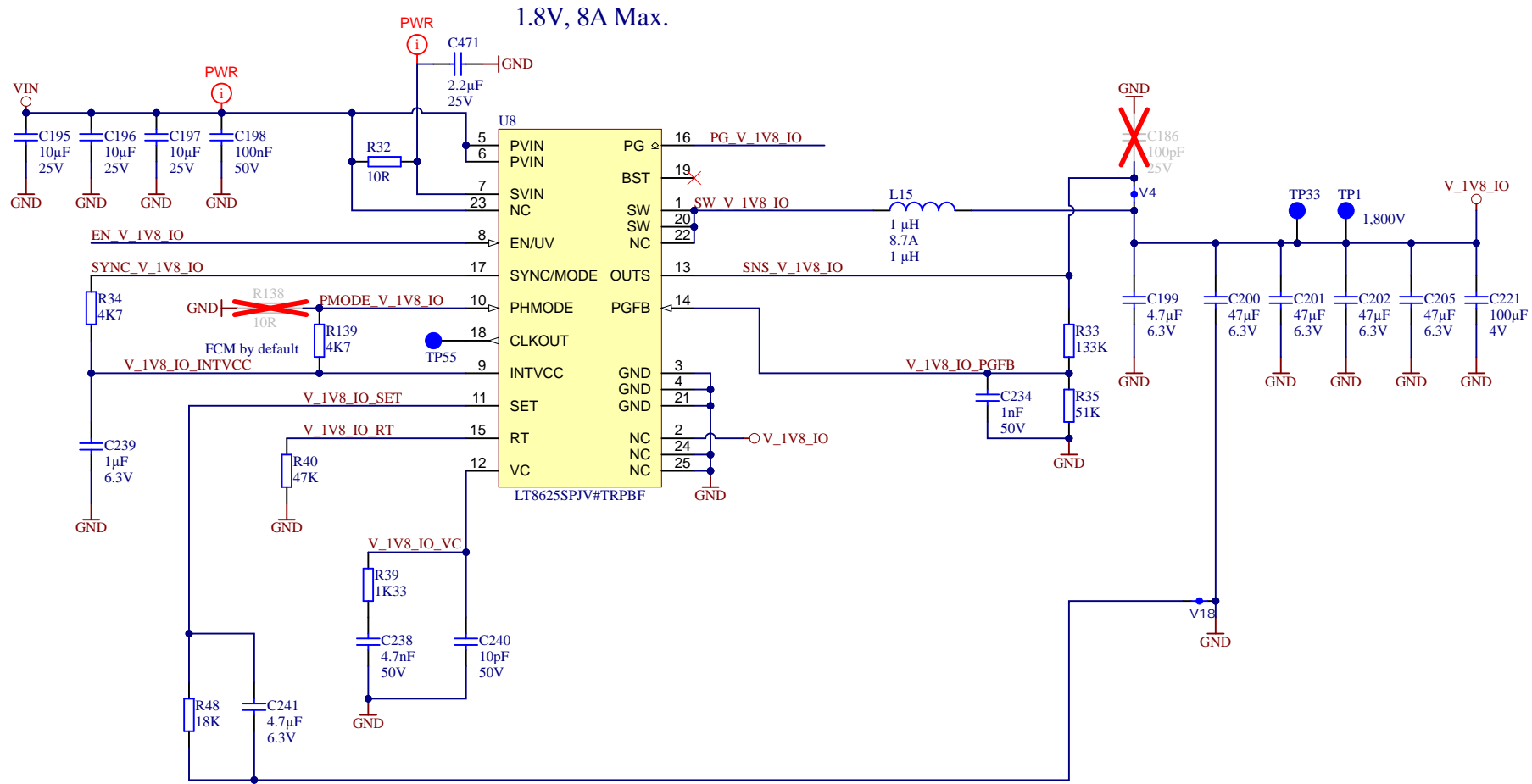
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Filename: Power Diagram.SchDoc		

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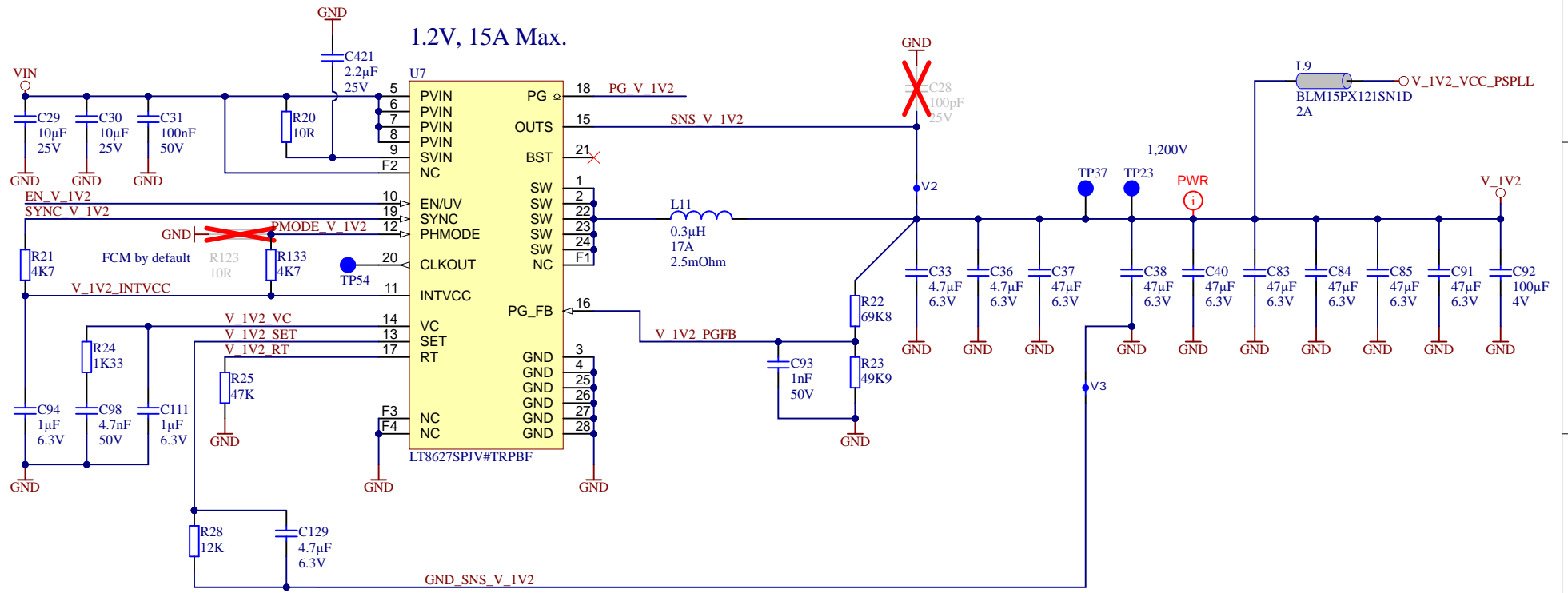
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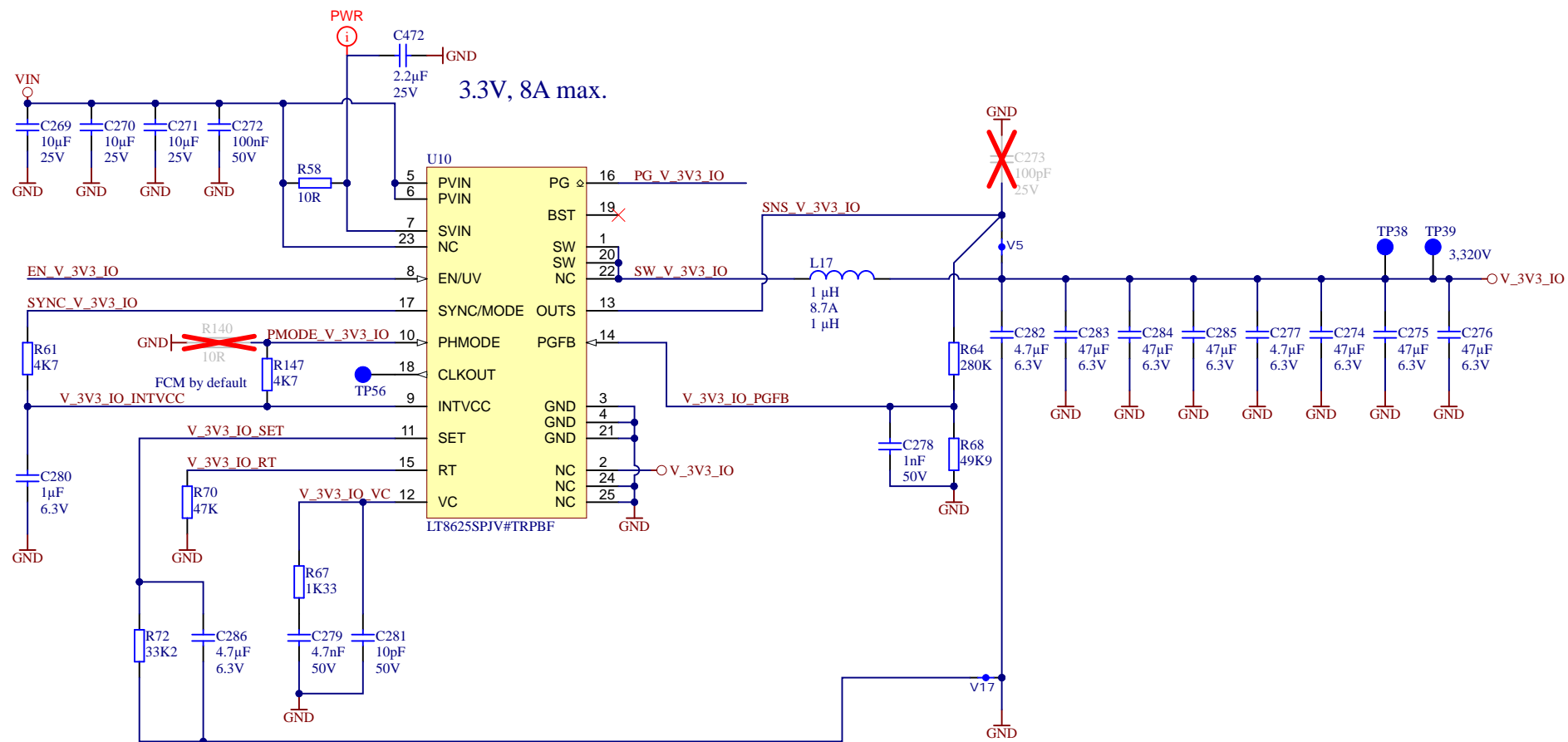
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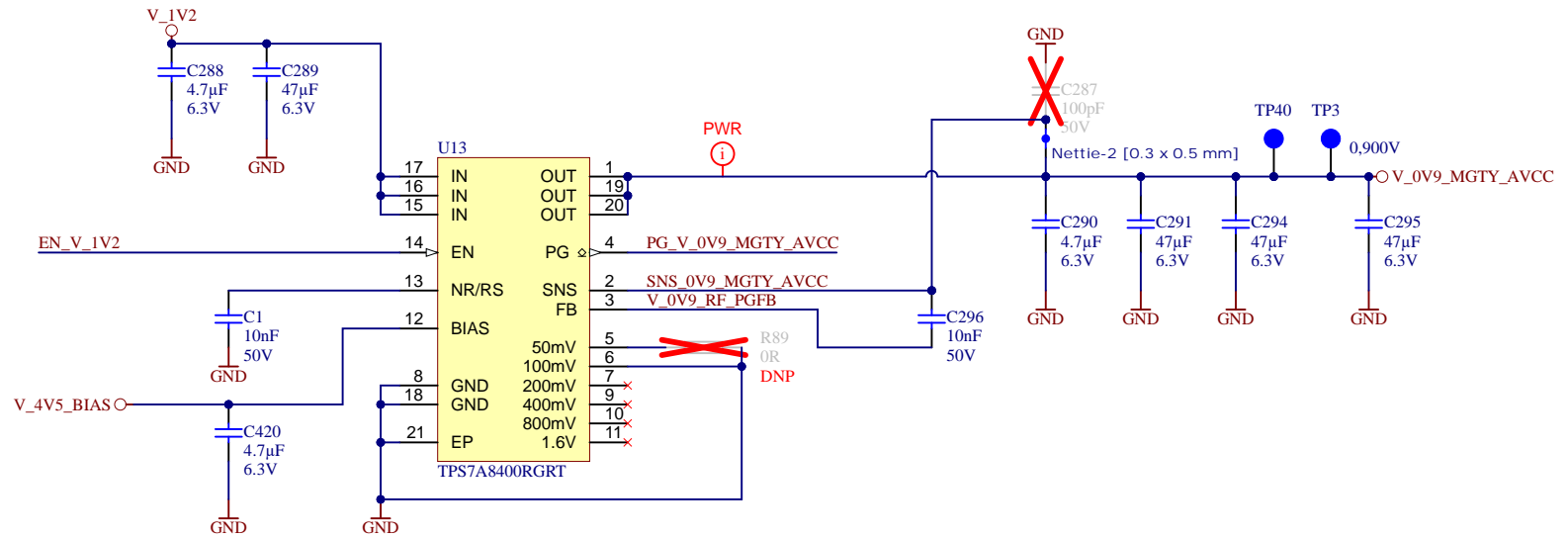



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V_0V9_MGTAVCC, 2.5A Max



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V_0V925_DAC_AVCC, (0.12 - 4.6A) + V_0V925_ADC_AVCC, (1.2 - 2.3A) ==> 1.32 - 6.9 A

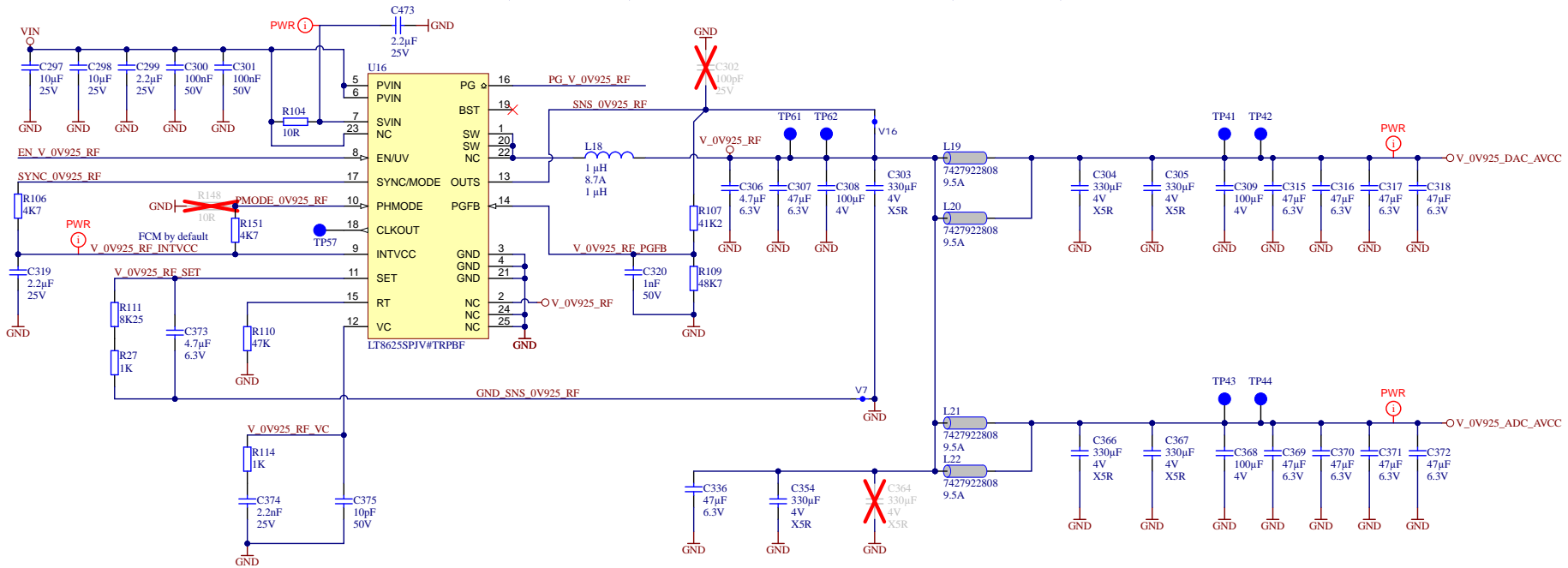
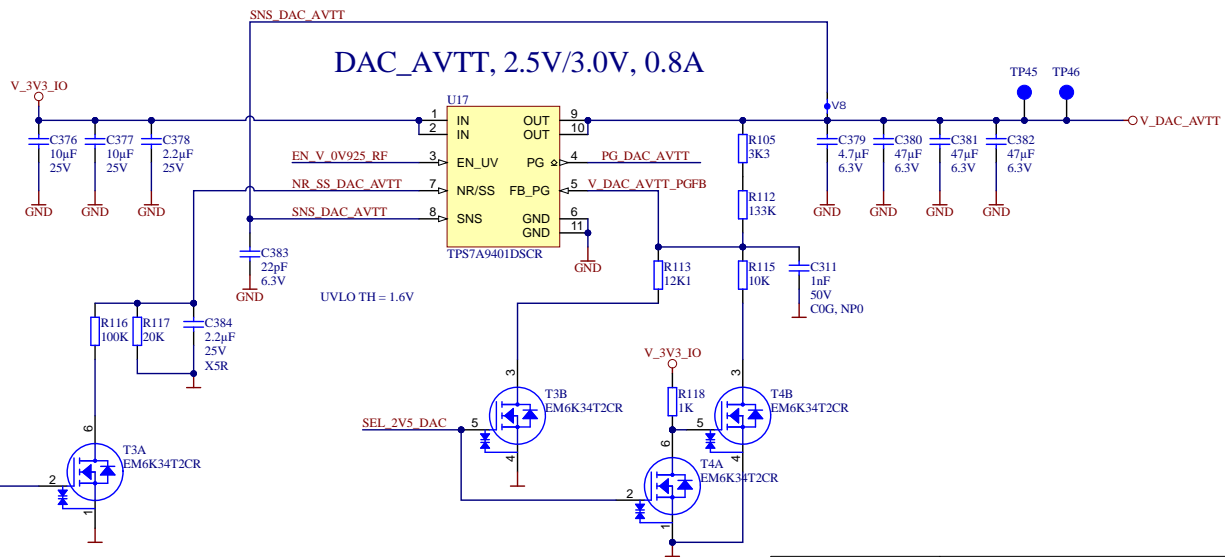


Table 9-22: ADC and DAC Voltage Supply Specifications for Gen 3 Devices⁽¹⁾

Supply	Nominal Voltage (V)	Tolerance (%) ⁽²⁾	Frequency Range (MHz)	Maximum Supply Ripple (mVpp) ⁽³⁾
ADC_AVCC	0.925	±3	0.1-15	0.25
ADC_AVCCCAUX	1.8	±3	0.1-15	1.2
DAC_AVCC	0.925	±3	0.1-15	0.32
DAC_AVCCCAUX	1.8	±3	0.1-15	1.0
DAC_AVTT	2.5/3.0 ⁽⁴⁾	±3	0.1-15	2.0
VCCINT_AMS	0.85	±3	0.1-15	20.0

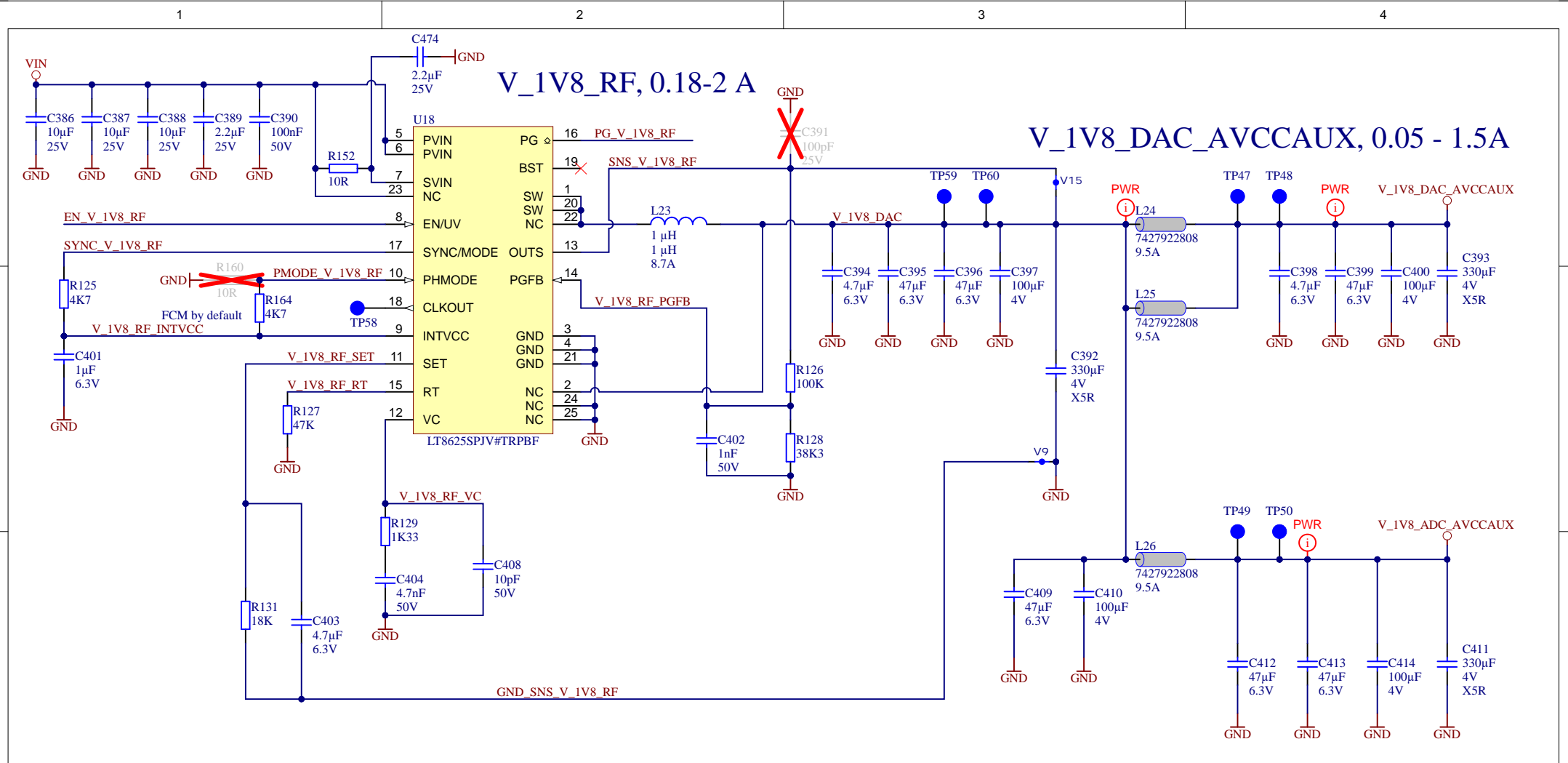
Notes:
 1. For the maximum current, refer to the *Mini Power Estimator (SPE)* tool.
 2. The tolerance percentage is for the switching regulator that feeds the VIMS.
 3. Output of the VIMS.
 4. DAC_AVTT should be set to 2.5V if used in 20 mA mode, and 3.0V if used in 32 mA mode in Gen 1 and Gen 2. *Mini Power Estimator (SPE)* tool should be used to enable the VIMS. Refer to *Gen 3 Selection - AVCC of Data Converter Logic/CP Product Guide (PG289) (Rev 1)* for details and compatibility mode.



OUTPUT VOLTAGE 2.5V, R_{nr} = 16.5 kOhms (default)
 OUTPUT VOLTAGE 3.0V, R_{nr} = 20.0 kOhms

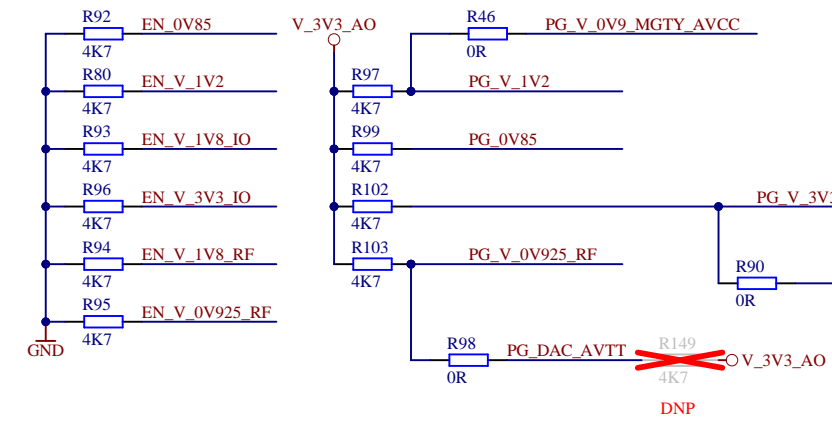
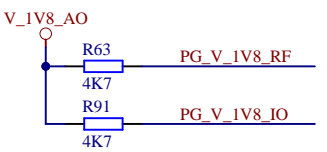
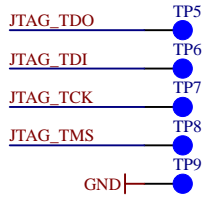
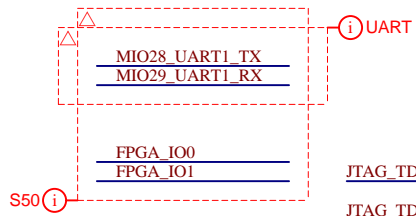
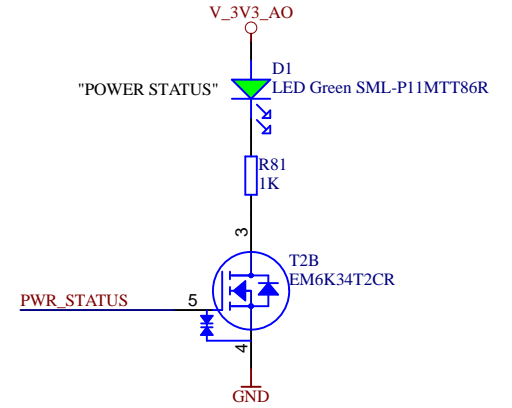
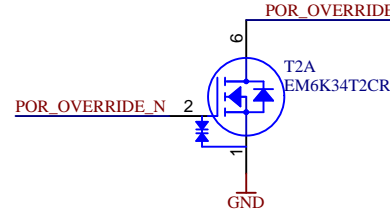
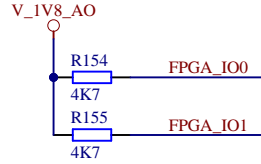
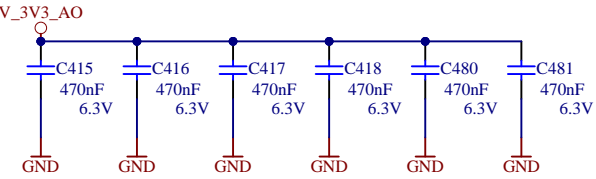


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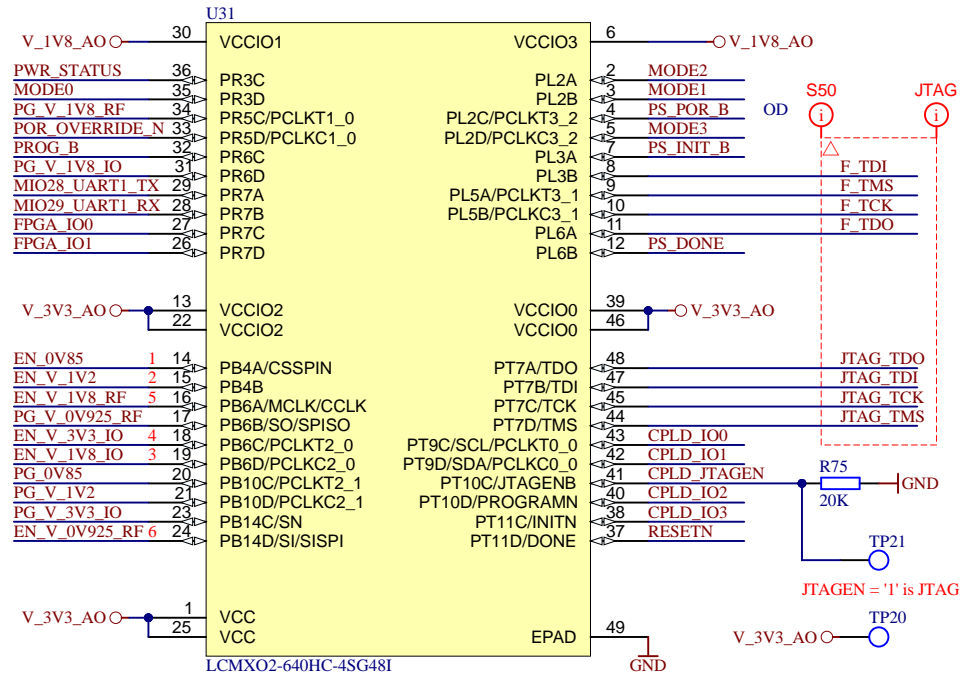
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System Controller (SC)

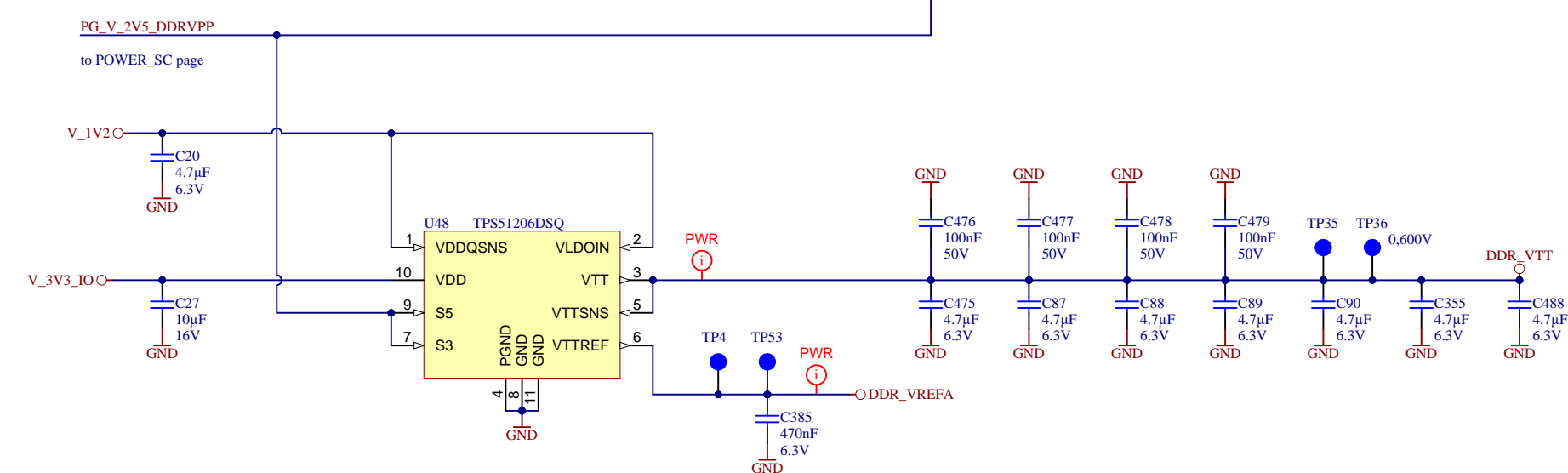
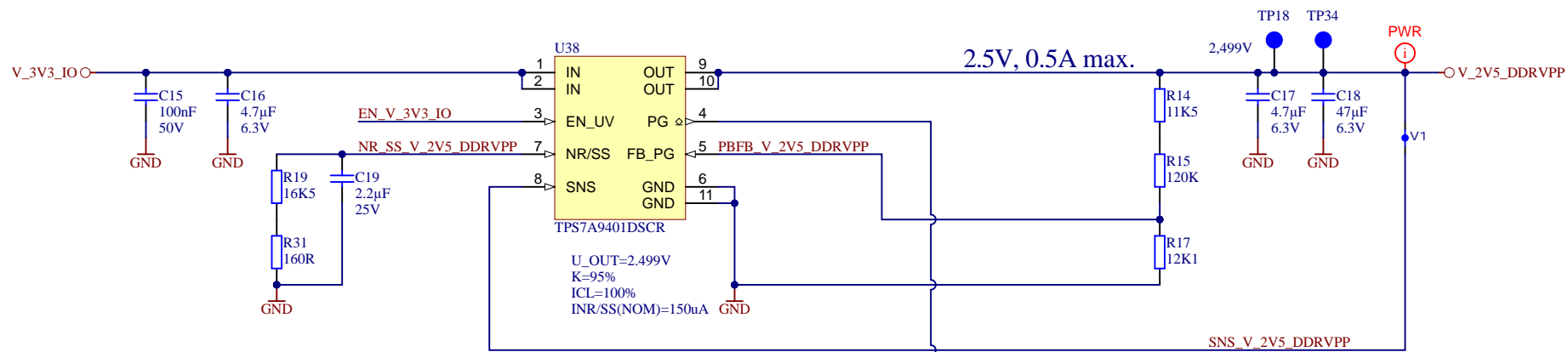



REV02
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SRST_B
PG_GR2

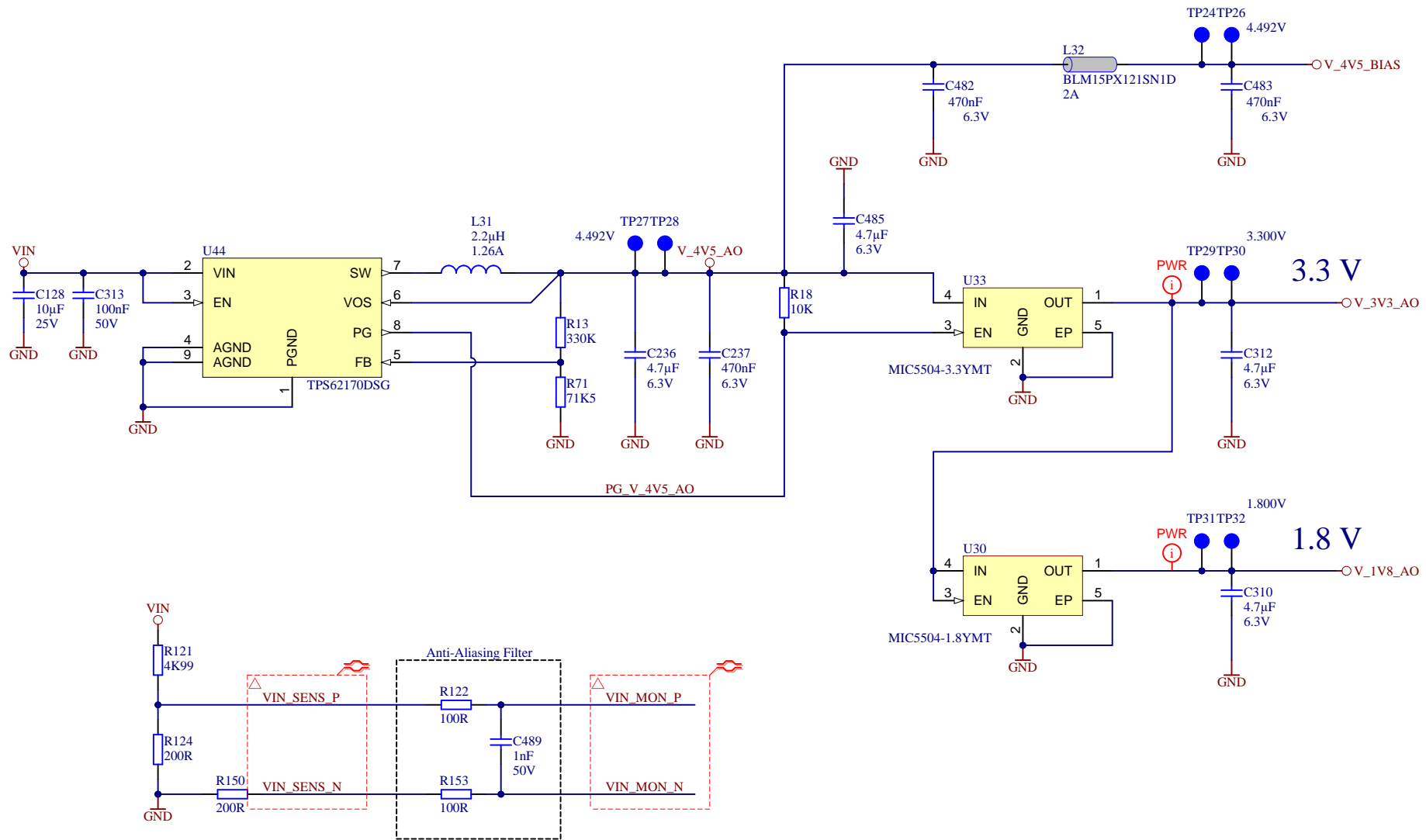
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PG_RF_DAC
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EN_RF_DAC




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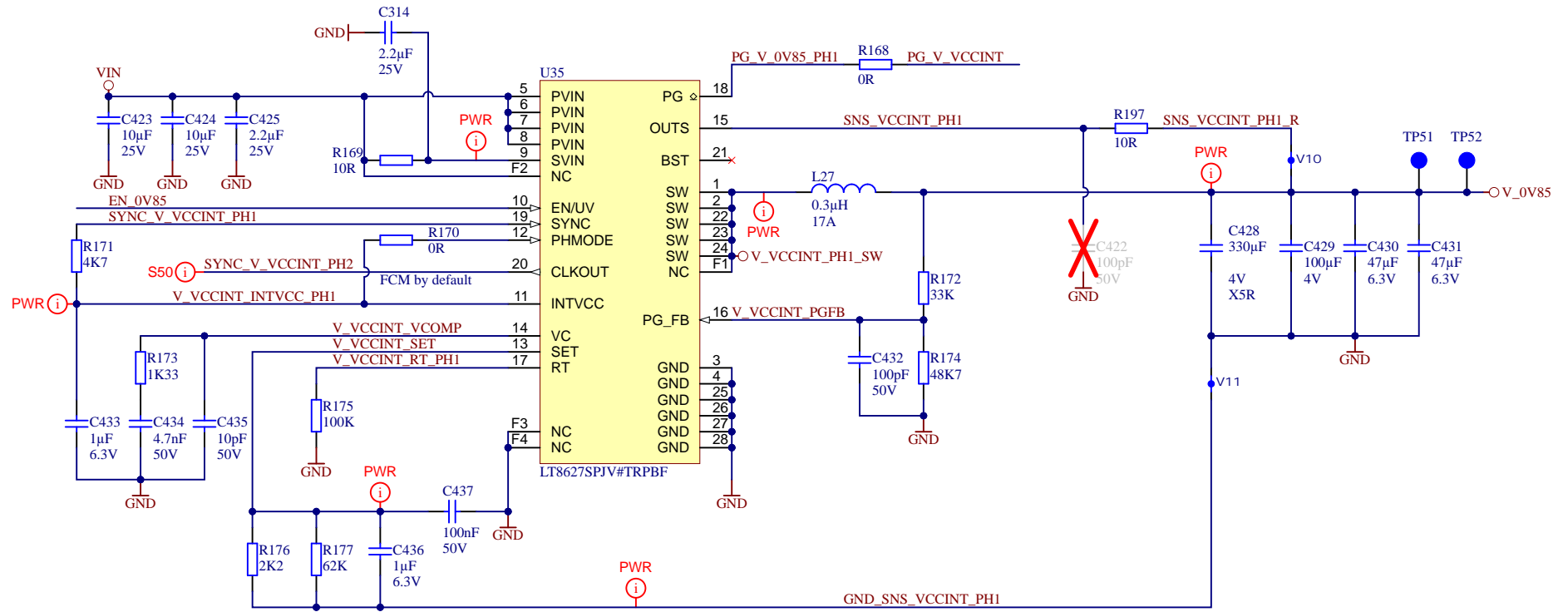



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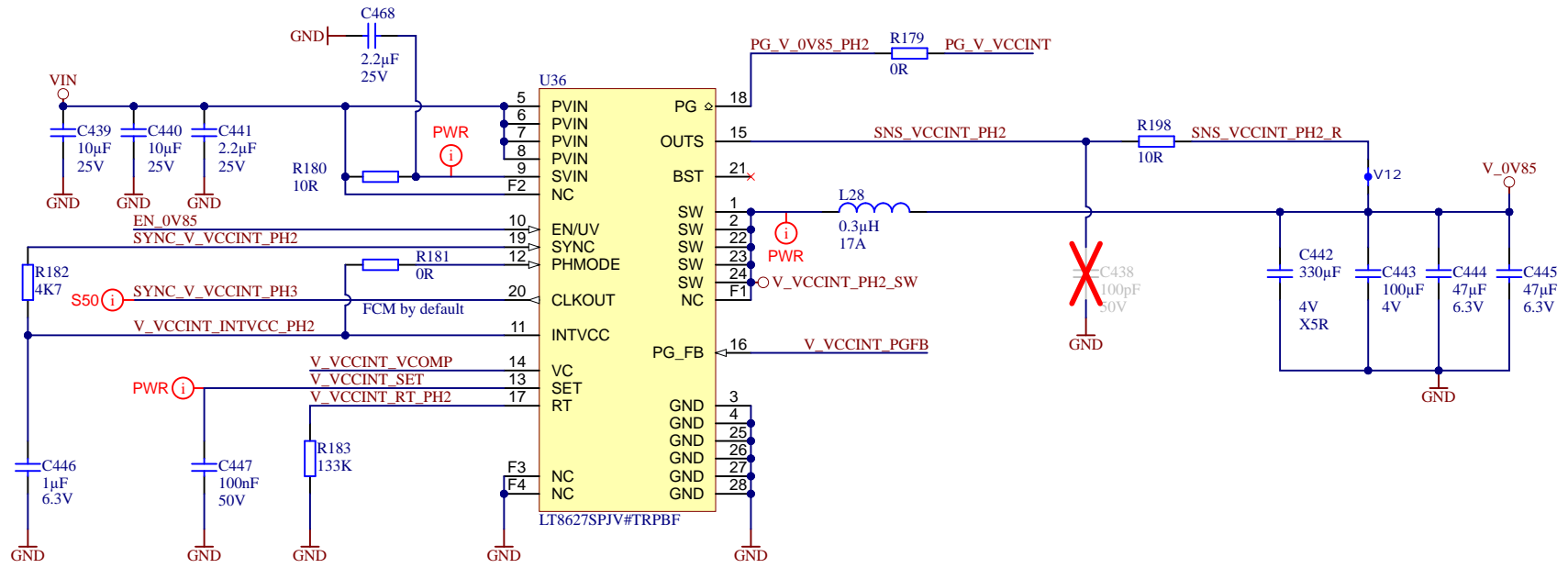
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VCCINT Phase 1/4, 0.85V, 45A, 15A per Phase



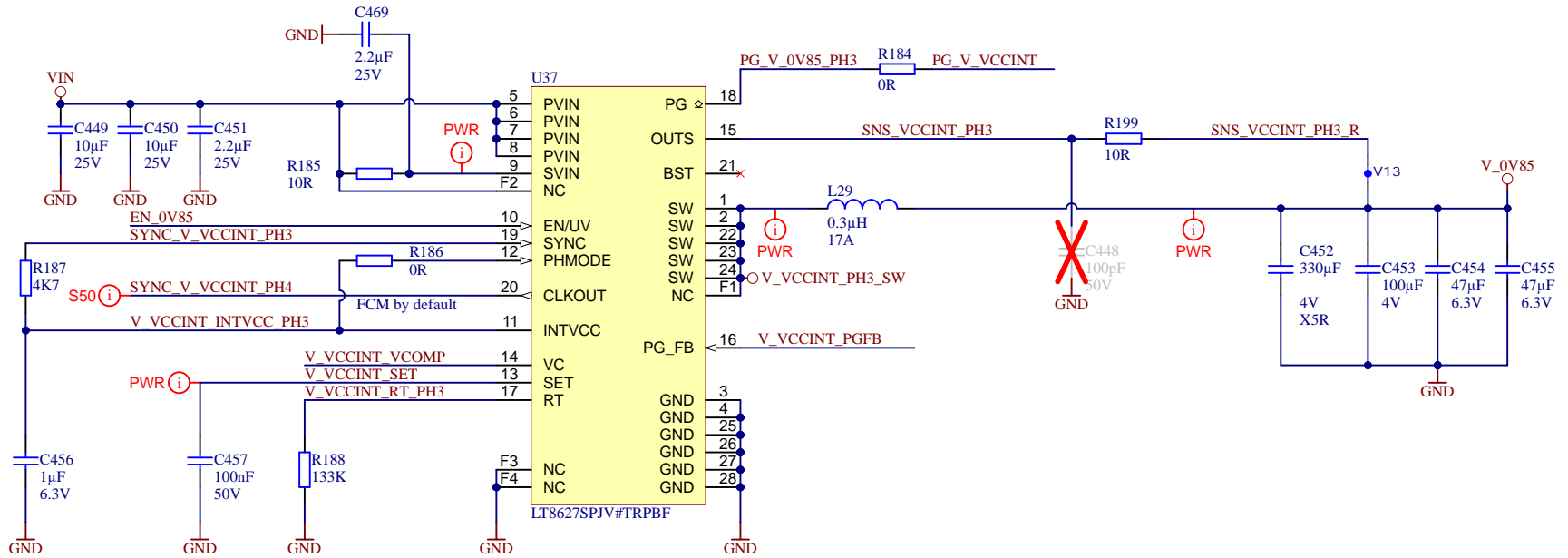
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VCCINT Phase 2/4, 0.85V, 45A, 15A per Phase



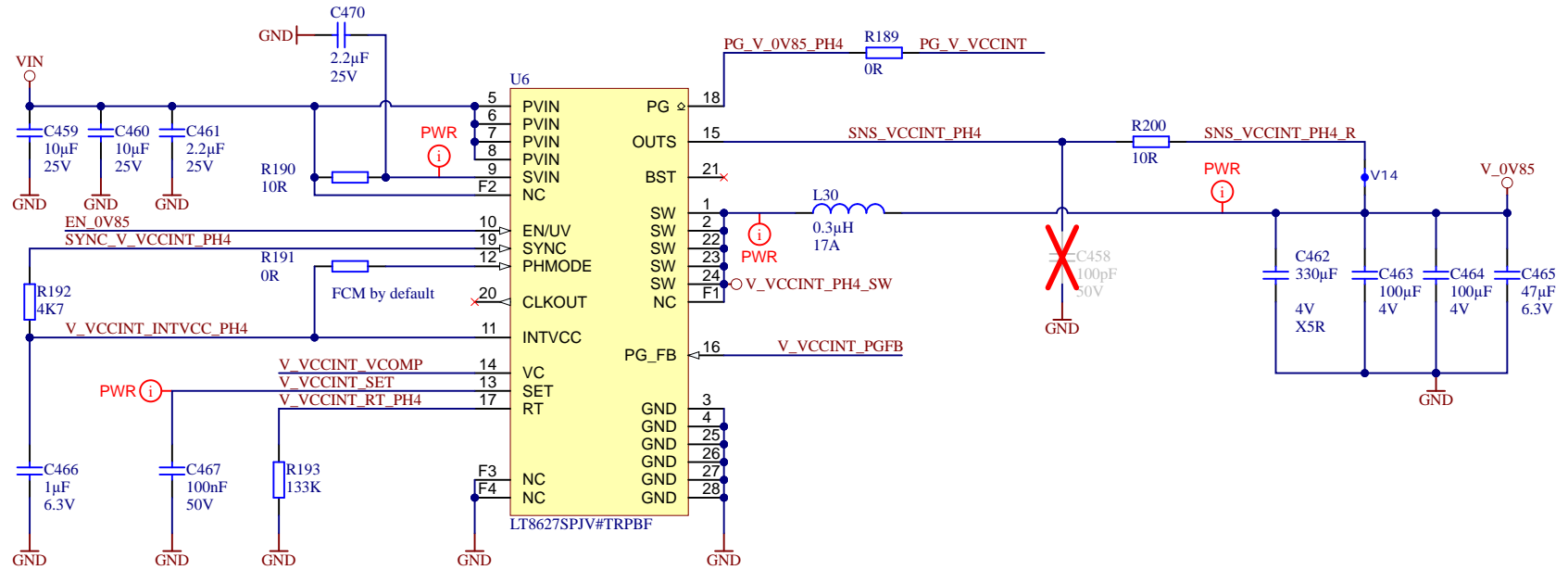
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VCCINT Phase 3/4, 0.85V, 45A, 15A per Phase

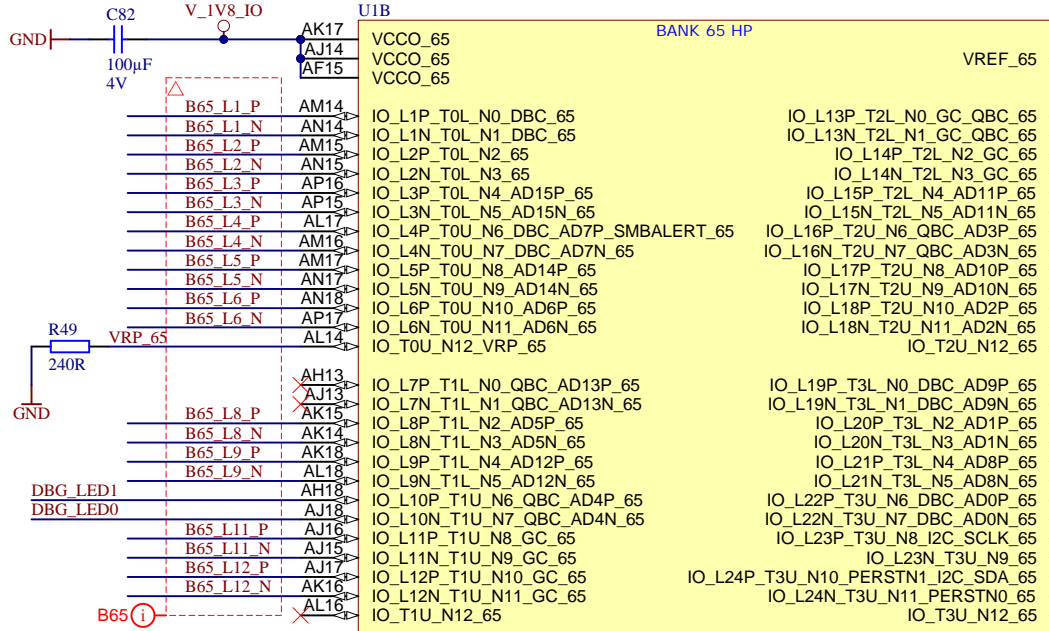


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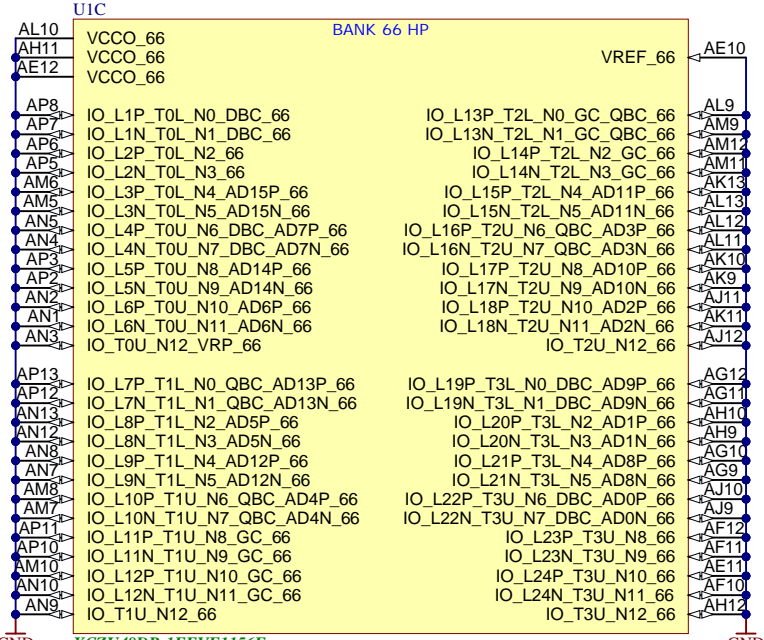
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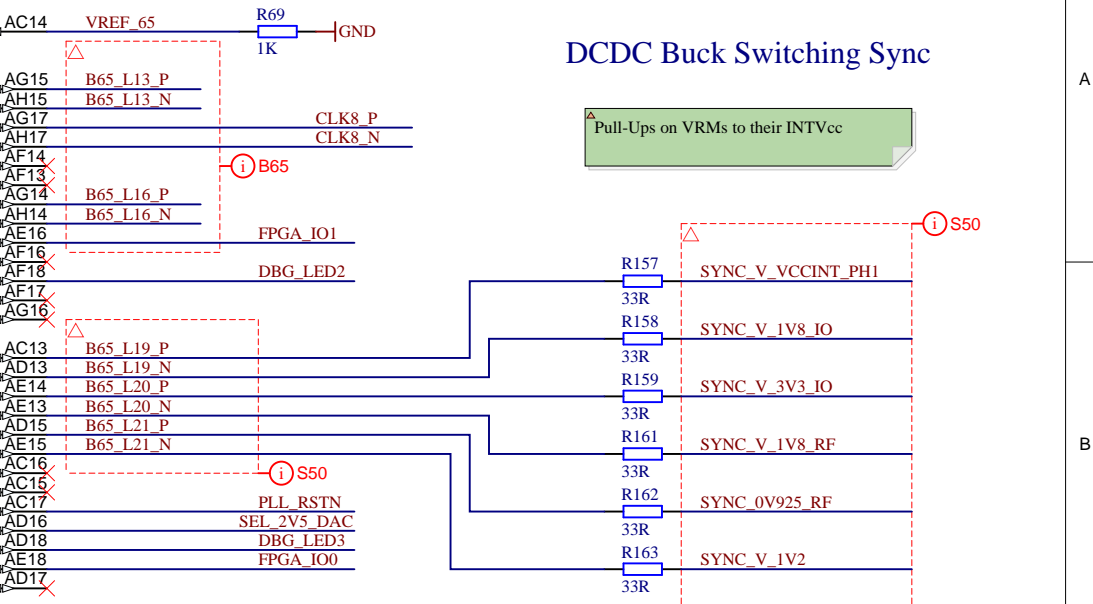
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XCZU48DR-1FFVE1156E

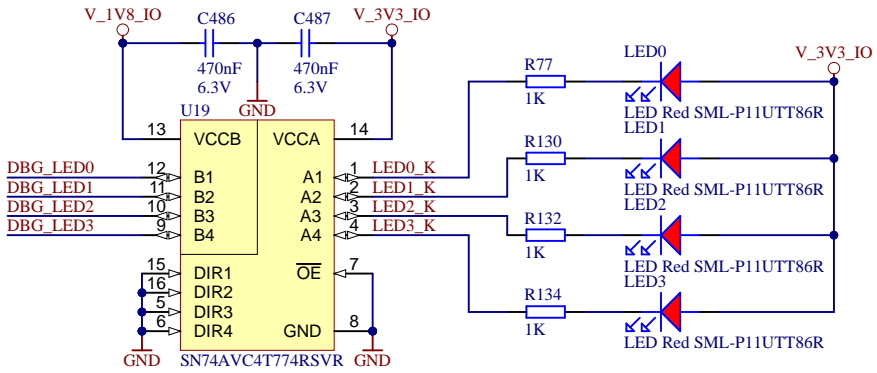


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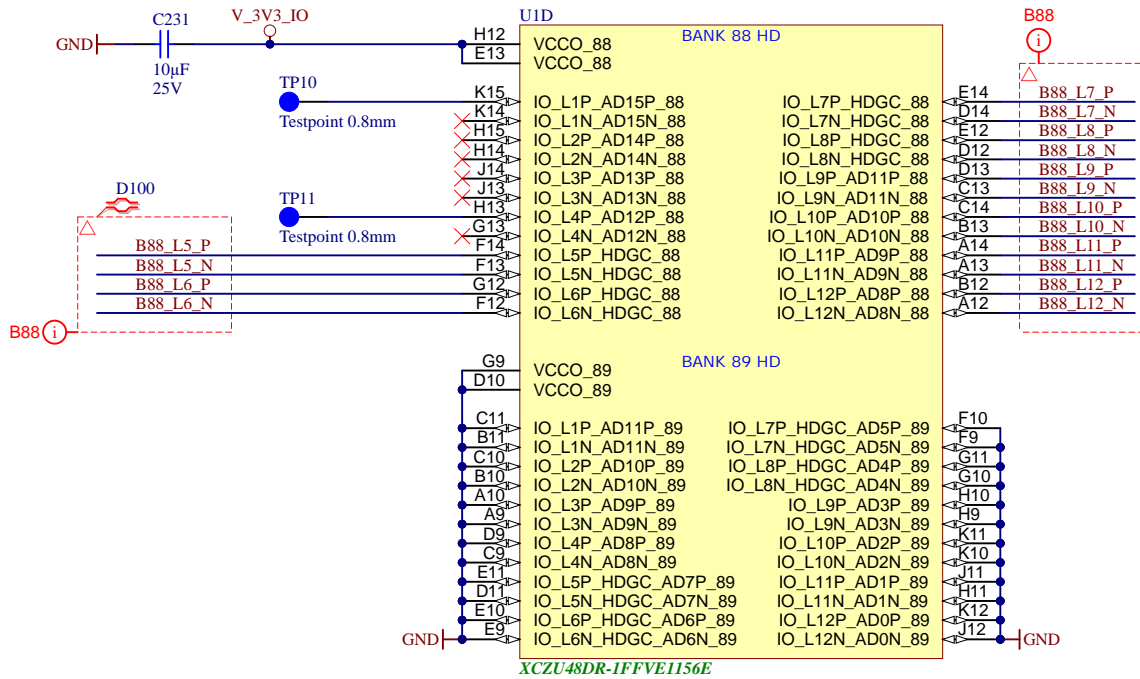
Pull-Ups on VRMs to their INTVcc

SYNC Threshold	SYNC DC and Clock Low Level Voltage	0.7	1.5	V
	SYNC DC and Clock High Level Voltage			

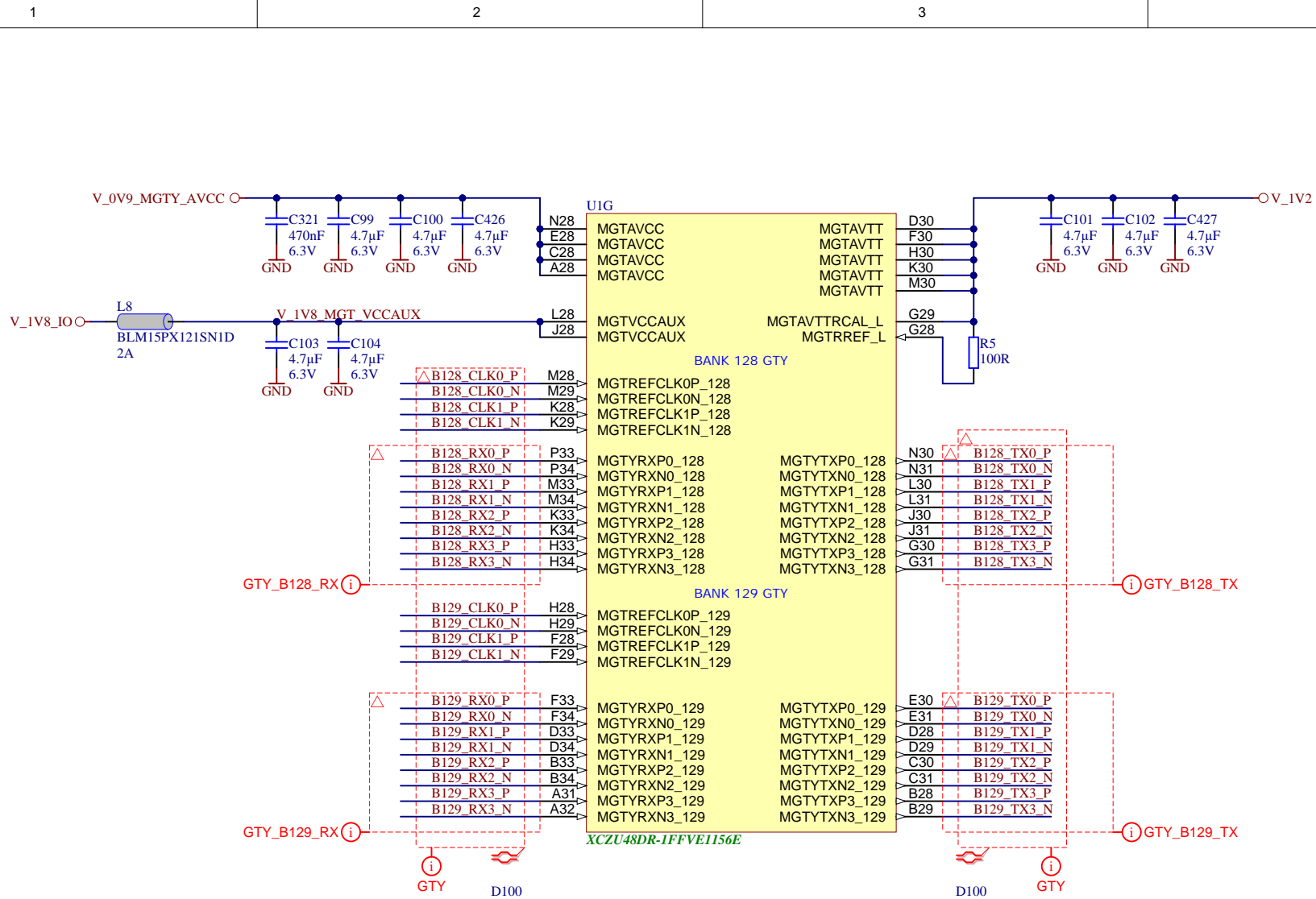


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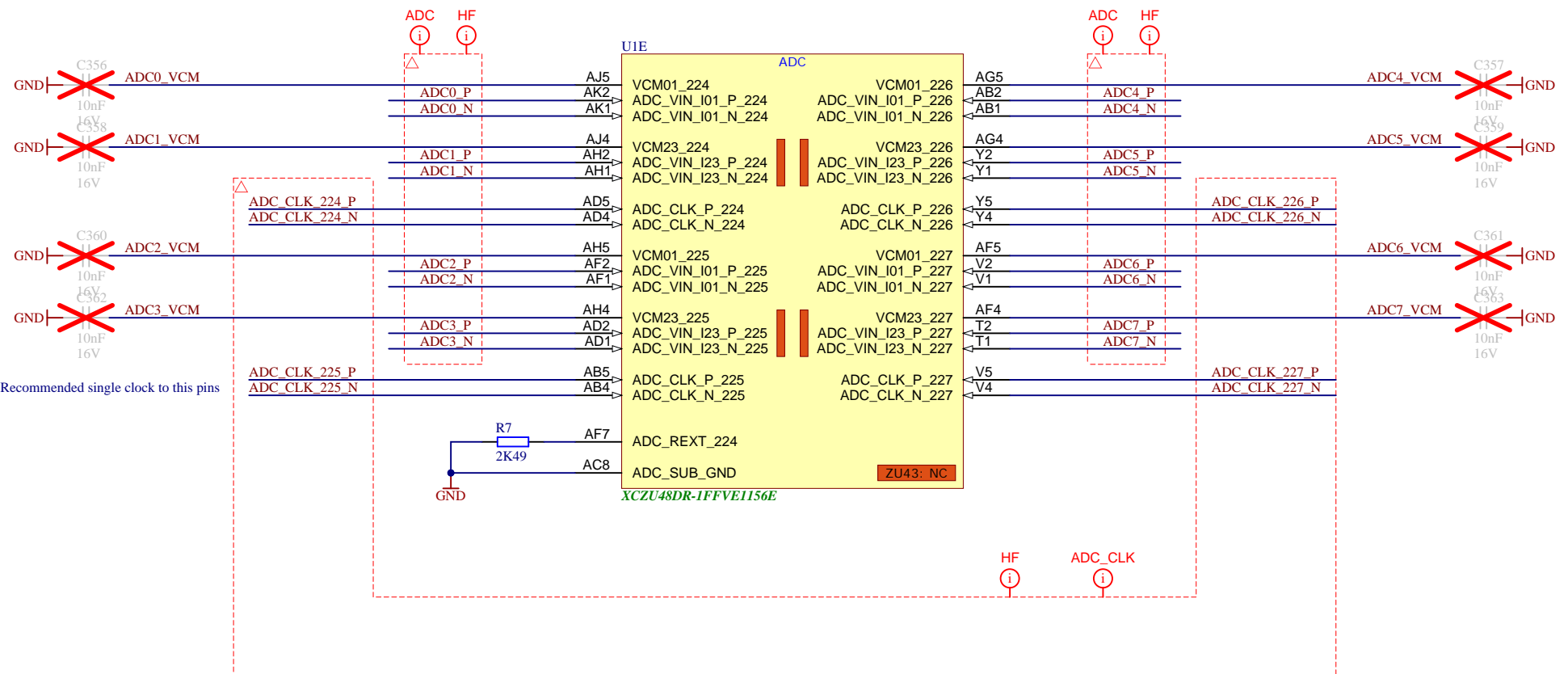
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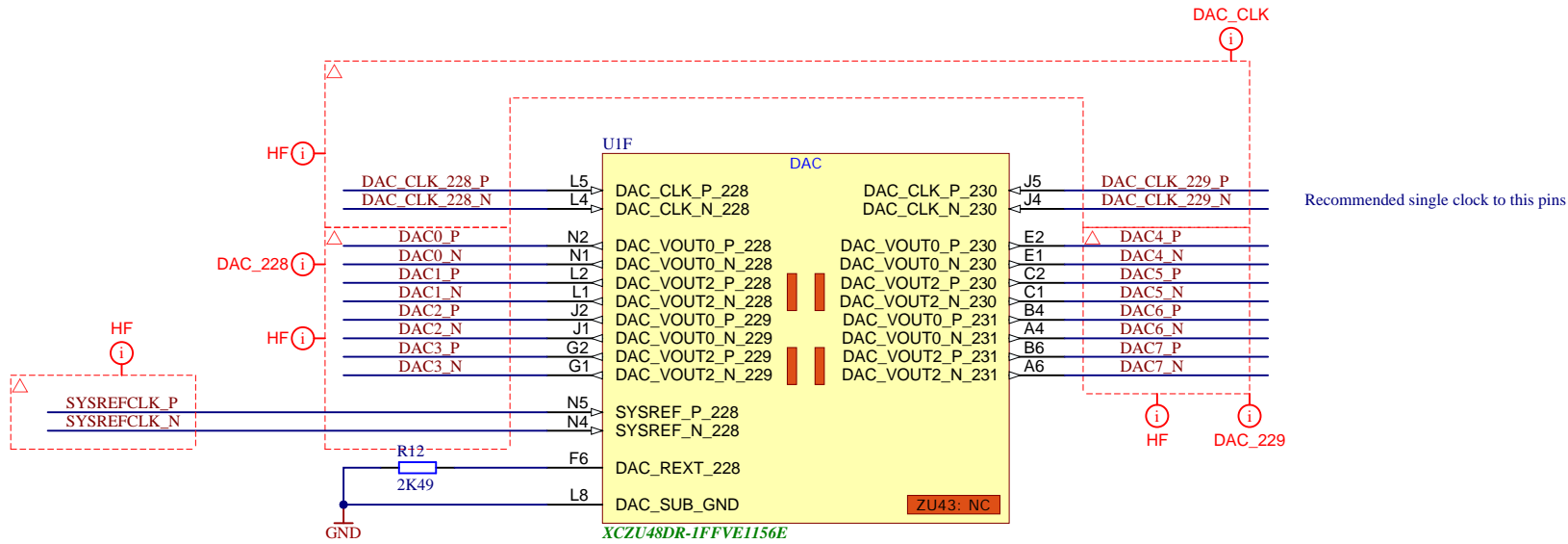



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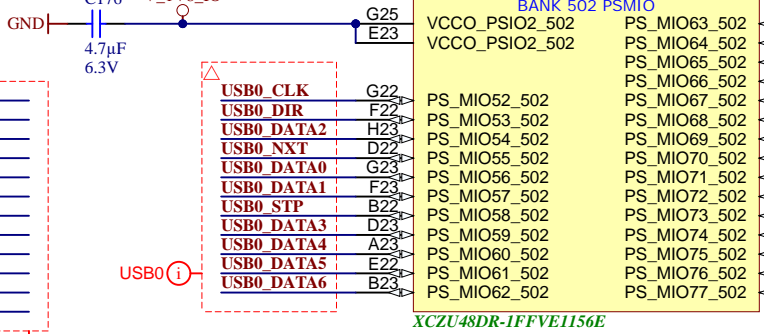
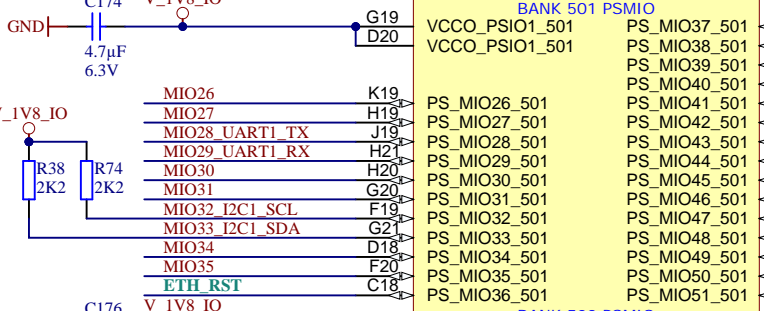
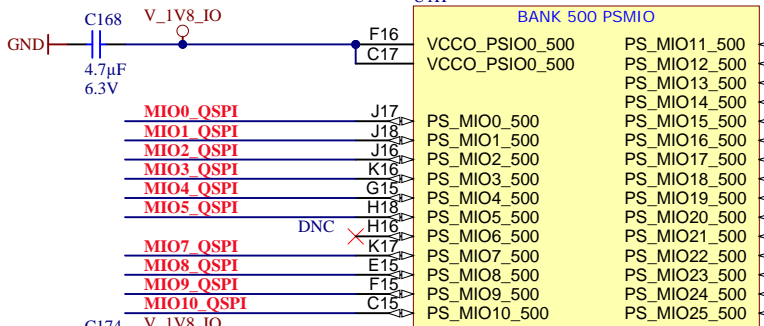
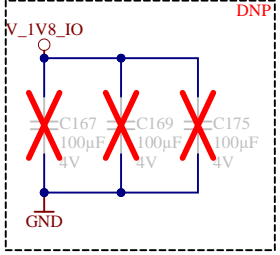


Recommended single clock to this pins

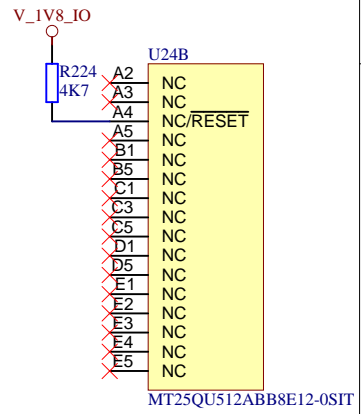
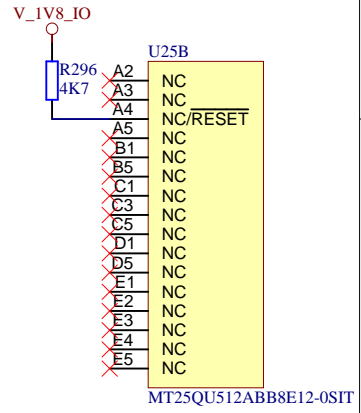
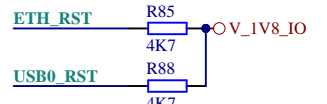
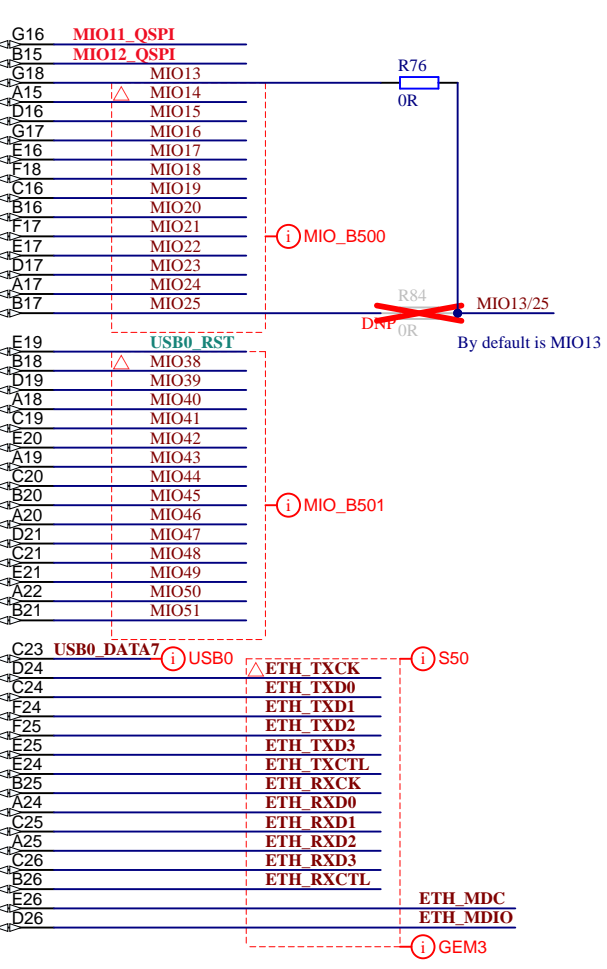
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XCZU48DR-1FFVE1156E



A

A

B

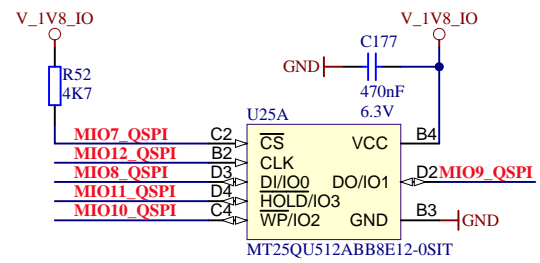
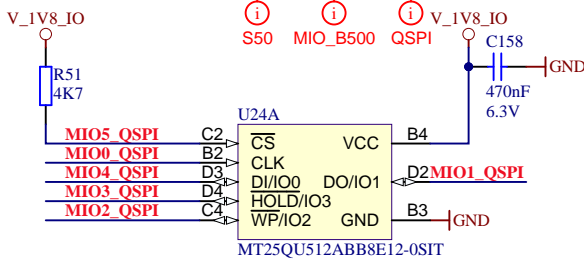
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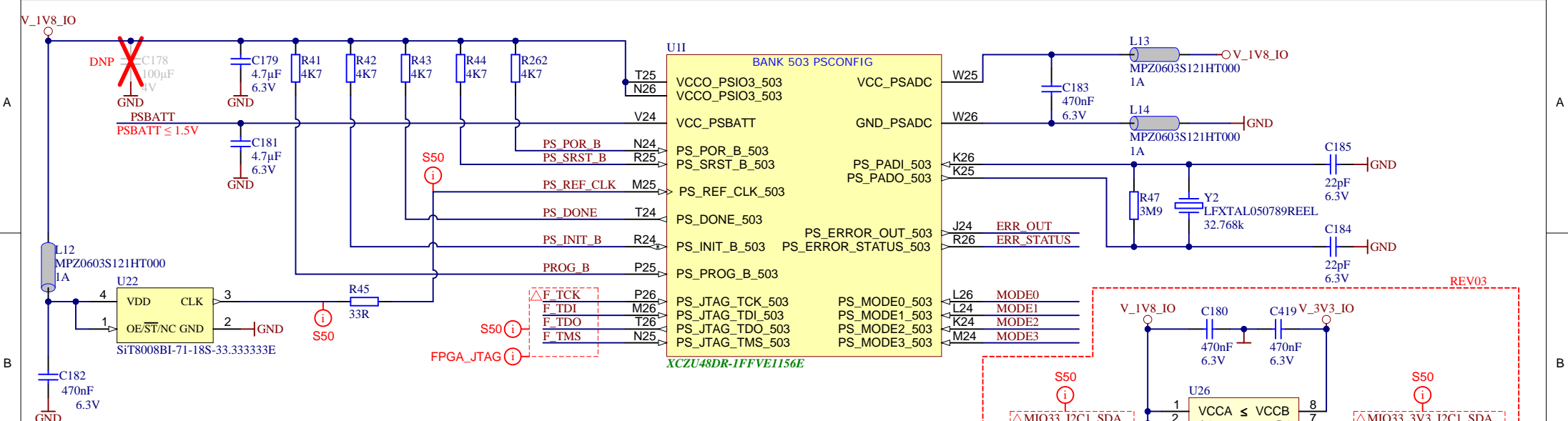
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D

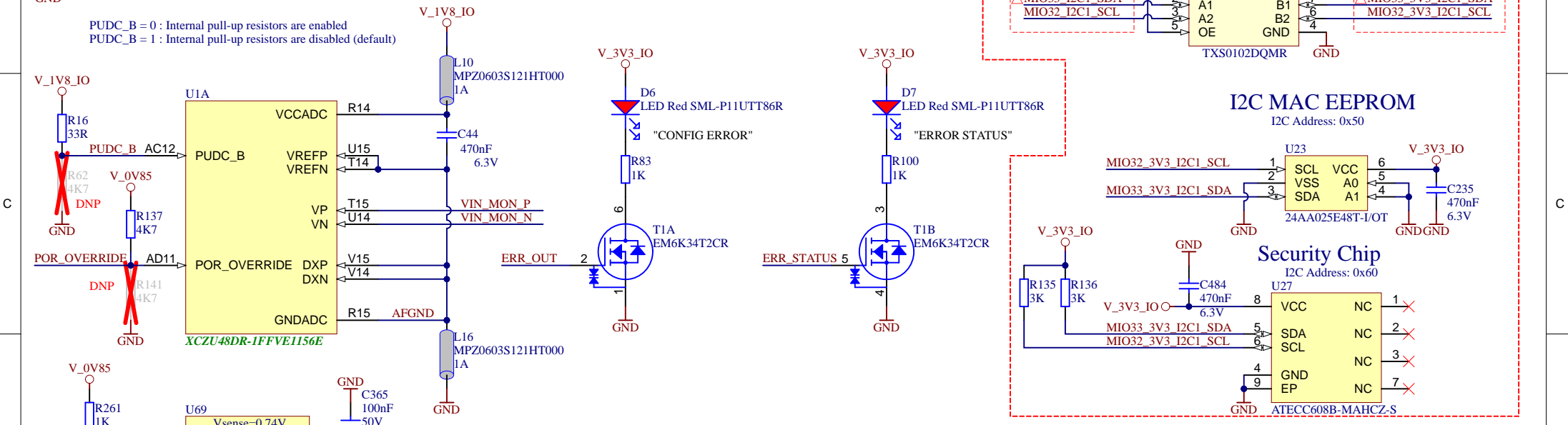
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Title: ZU_MIO		
A4	Number: TE0835 UXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 25 of 39
Filename: ZU_MIO_B500_B501_B502.SchDoc		



PUDC_B = 0 : Internal pull-up resistors are enabled
 PUDC_B = 1 : Internal pull-up resistors are disabled (default)



Title: ZU_CFG		
A4	Number: TE0835 UXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 26 of 39
Filename: ZU_CFG_B503.SchDoc		

A

B

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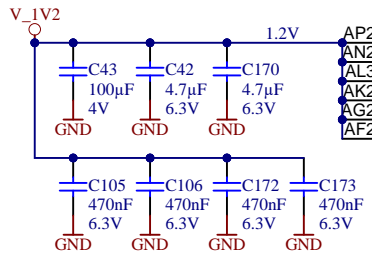
D

A

B

C

D



UIJ BANK 504 PSDDR

VCCO_PSDDR_504	PS_DDR_CK0_504	AN28
VCCO_PSDDR_504	PS_DDR_CK_NO_504	AP28
VCCO_PSDDR_504	PS_DDR_CKE0_504	AP31
VCCO_PSDDR_504	PS_DDR_CK1_504	AL27
VCCO_PSDDR_504	PS_DDR_CK_N1_504	AM2
VCCO_PSDDR_504	PS_DDR_CKE1_504	AK28
PS_DDR_A0_504	DDR4-A0	AN29
PS_DDR_A1_504	DDR4-A1	AP27
PS_DDR_A2_504	DDR4-A2	AP25
PS_DDR_A3_504	DDR4-A3	AP26
PS_DDR_A4_504	DDR4-A4	AN27
PS_DDR_A5_504	DDR4-A5	AN25
PS_DDR_A6_504	DDR4-A6	AK26
PS_DDR_A7_504	DDR4-A7	AK25
PS_DDR_A8_504	DDR4-A8	AJ26
PS_DDR_A9_504	DDR4-A9	AJ25
PS_DDR_A10_504	DDR4-A10	AL28
PS_DDR_A11_504	DDR4-A11	AM26
PS_DDR_A12_504	DDR4-A12	AL29
PS_DDR_A13_504	DDR4-A13	AM25
PS_DDR_A14_504	DDR4-A14	AM29
PS_DDR_A15_504	DDR4-A15	AL26
PS_DDR_A16_504	DDR4-A16	AH25
PS_DDR_A17_504	DDR4-A17	AG25
PS_DDR_CS_N0_504	DDR4-CS	AN30
PS_DDR_CS_N1_504	DDR4-CS	AM30
PS_DDR_BA0_504	DDR4-BA0	AG26
PS_DDR_BA1_504	DDR4-BA1	AK28
PS_DDR_BG0_504	DDR4-BG0	AJ27
PS_DDR_BG1_504	DDR4-BG1	AJ28
PS_DDR_PARITY_504	DDR4-PAR	AG27
PS_DDR_RAM_RST_N_504	DDR4-RESET	AF27
PS_DDR_ACT_N_504	DDR4-ACT	AH27
PS_DDR_ALERT_N_504	DDR4-ALERT	AE26
PS_DDR_ZQ_504	DDR4-ZQ	AF26
PS_DDR_ODT0_504	DDR4-ODT0	AP30
PS_DDR_ODT1_504	DDR4-ODT0	AM31

XCZU48DR-1FFVE1156E

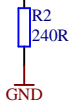
ADDR_CMD_CTRL S40

ADDR_CMD_CTRL S40

UIK BANK 504 PSDDR

DQ0	AP22	PS_DDR_DQ0_504	PS_DDR_DQ32_504	AE29	DQ32
DQ1	AM2	PS_DDR_DQ1_504	PS_DDR_DQ33_504	AF29	DQ33
DQ2	AP21	PS_DDR_DQ2_504	PS_DDR_DQ34_504	AE28	DQ34
DQ3	AL21	PS_DDR_DQ3_504	PS_DDR_DQ35_504	AF28	DQ35
DQ4	AP18	PS_DDR_DQ4_504	PS_DDR_DQ36_504	AJ30	DQ36
DQ5	AN19	PS_DDR_DQ5_504	PS_DDR_DQ37_504	AH29	DQ37
DQ6	AM19	PS_DDR_DQ6_504	PS_DDR_DQ38_504	AH30	DQ38
DQ7	AL19	PS_DDR_DQ7_504	PS_DDR_DQ39_504	AH28	DQ39
DQ8	AL27	PS_DDR_DQ8_504	PS_DDR_DQ40_504	AE30	DQ40
DQ9	AK23	PS_DDR_DQ9_504	PS_DDR_DQ41_504	AD30	DQ41
DQ10	AM2	PS_DDR_DQ10_504	PS_DDR_DQ42_504	AD28	DQ42
DQ11	AN2	PS_DDR_DQ11_504	PS_DDR_DQ43_504	AD27	DQ43
DQ12	AK24	PS_DDR_DQ12_504	PS_DDR_DQ44_504	AB29	DQ44
DQ13	AL24	PS_DDR_DQ13_504	PS_DDR_DQ45_504	AC28	DQ45
DQ14	AN2	PS_DDR_DQ14_504	PS_DDR_DQ46_504	AB28	DQ46
DQ15	AM2	PS_DDR_DQ15_504	PS_DDR_DQ47_504	AC27	DQ47
DQ16	AJ22	PS_DDR_DQ16_504	PS_DDR_DQ48_504	AG34	DQ48
DQ17	AK21	PS_DDR_DQ17_504	PS_DDR_DQ49_504	AH33	DQ49
DQ18	AK20	PS_DDR_DQ18_504	PS_DDR_DQ50_504	AH34	DQ50
DQ19	AK19	PS_DDR_DQ19_504	PS_DDR_DQ51_504	AH32	DQ51
DQ20	AG2	PS_DDR_DQ20_504	PS_DDR_DQ52_504	AK34	DQ52
DQ21	AG19	PS_DDR_DQ21_504	PS_DDR_DQ53_504	AK33	DQ53
DQ22	AG20	PS_DDR_DQ22_504	PS_DDR_DQ54_504	AK31	DQ54
DQ23	AH19	PS_DDR_DQ23_504	PS_DDR_DQ55_504	AK30	DQ55
DQ24	AE23	PS_DDR_DQ24_504	PS_DDR_DQ56_504	AG32	DQ56
DQ25	AF23	PS_DDR_DQ25_504	PS_DDR_DQ57_504	AF31	DQ57
DQ26	AE25	PS_DDR_DQ26_504	PS_DDR_DQ58_504	AF34	DQ58
DQ27	AE24	PS_DDR_DQ27_504	PS_DDR_DQ59_504	AE34	DQ59
DQ28	AH23	PS_DDR_DQ28_504	PS_DDR_DQ60_504	AD32	DQ60
DQ29	AH2	PS_DDR_DQ29_504	PS_DDR_DQ61_504	AE31	DQ61
DQ30	AJ23	PS_DDR_DQ30_504	PS_DDR_DQ62_504	AD34	DQ62
DQ31	AH24	PS_DDR_DQ31_504	PS_DDR_DQ63_504	AD33	DQ63
DDR4-DQS0_P	AN20	PS_DDR_DQS_P0_504	PS_DDR_DQ64_504	AP32	
DDR4-DQS0_N	AP20	PS_DDR_DQS_N0_504	PS_DDR_DQ65_504	AM32	
DDR4-DQS1_P	AN23	PS_DDR_DQS_P1_504	PS_DDR_DQ66_504	AL31	
DDR4-DQS1_N	AP23	PS_DDR_DQS_N1_504	PS_DDR_DQ67_504	AL32	
DDR4-DQS2_P	AJ20	PS_DDR_DQS_P2_504	PS_DDR_DQ68_504	AP33	
DDR4-DQS2_N	AJ21	PS_DDR_DQS_N2_504	PS_DDR_DQ69_504	AM34	
DDR4-DQS3_P	AF24	PS_DDR_DQS_P3_504	PS_DDR_DQ70_504	AN34	
DDR4-DQS3_N	AG24	PS_DDR_DQS_N3_504	PS_DDR_DQ71_504	AL34	
DDR4-DQS4_P	AG29	PS_DDR_DQS_P4_504	PS_DDR_DM0_504	AM20	DDR4-DM0
DDR4-DQS4_N	AG30	PS_DDR_DQS_N4_504	PS_DDR_DM1_504	AL23	DDR4-DM1
DDR4-DQS5_P	AC29	PS_DDR_DQS_P5_504	PS_DDR_DM2_504	AH20	DDR4-DM2
DDR4-DQS5_N	AC30	PS_DDR_DQS_N5_504	PS_DDR_DM3_504	AG22	DDR4-DM3
DDR4-DQS6_P	AJ32	PS_DDR_DQS_P6_504	PS_DDR_DM4_504	AG31	DDR4-DM4
DDR4-DQS6_N	AJ33	PS_DDR_DQS_N6_504	PS_DDR_DM5_504	AD31	DDR4-DM5
DDR4-DQS7_P	AF32	PS_DDR_DQS_P7_504	PS_DDR_DM6_504	AJ31	DDR4-DM6
DDR4-DQS7_N	AF33	PS_DDR_DQS_N7_504	PS_DDR_DM7_504	AE33	DDR4-DM7
DDR4-DQS8_P	AN32	PS_DDR_DQS_P8_504	PS_DDR_DM8_504	AL33	
DDR4-DQS8_N	AN33	PS_DDR_DQS_N8_504			

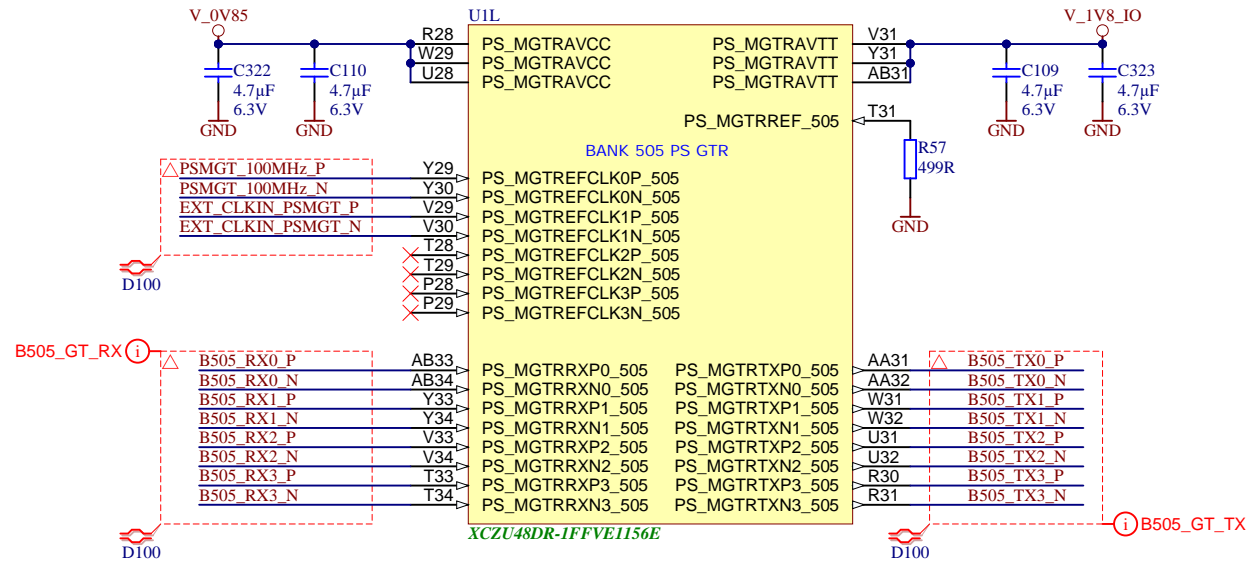
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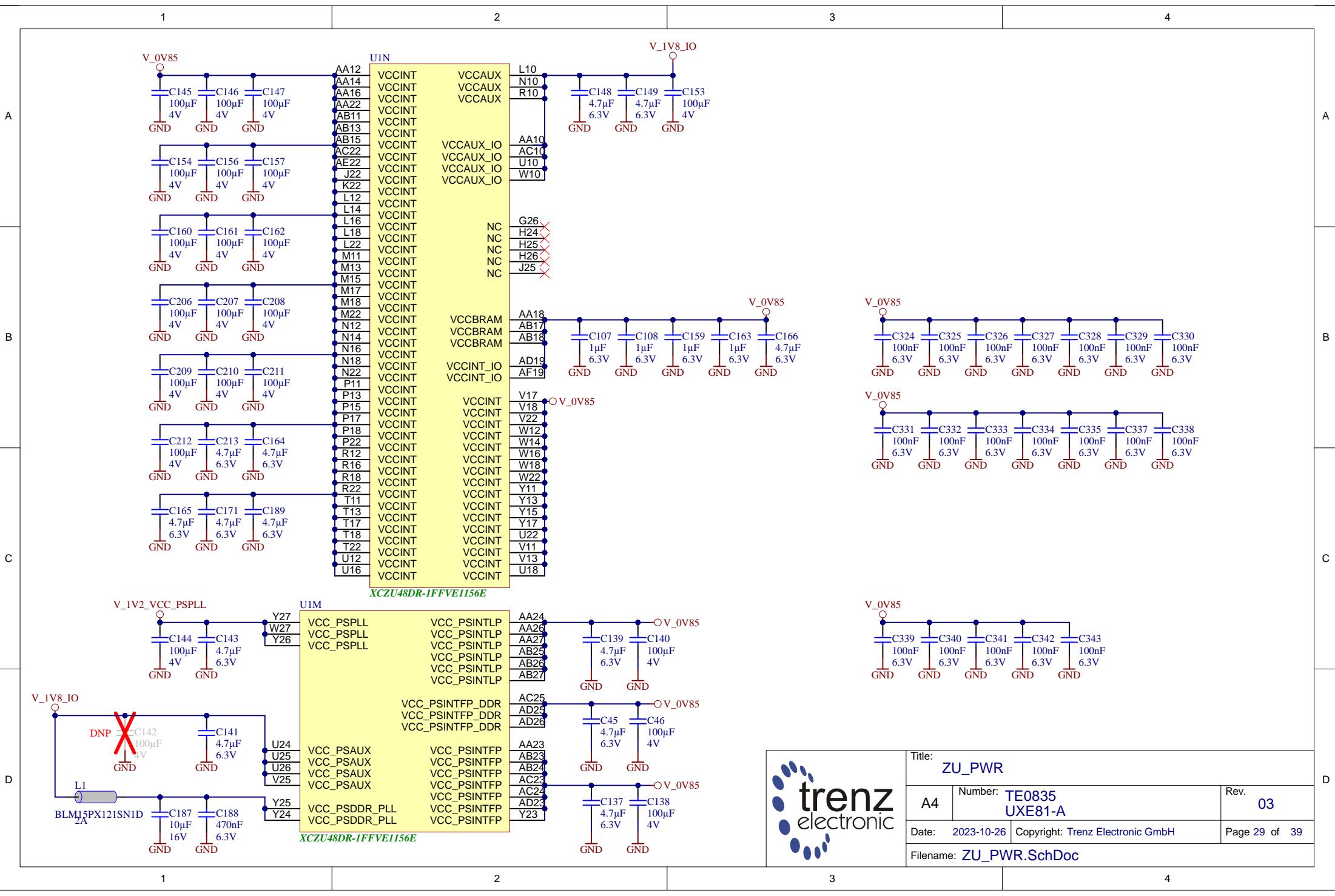
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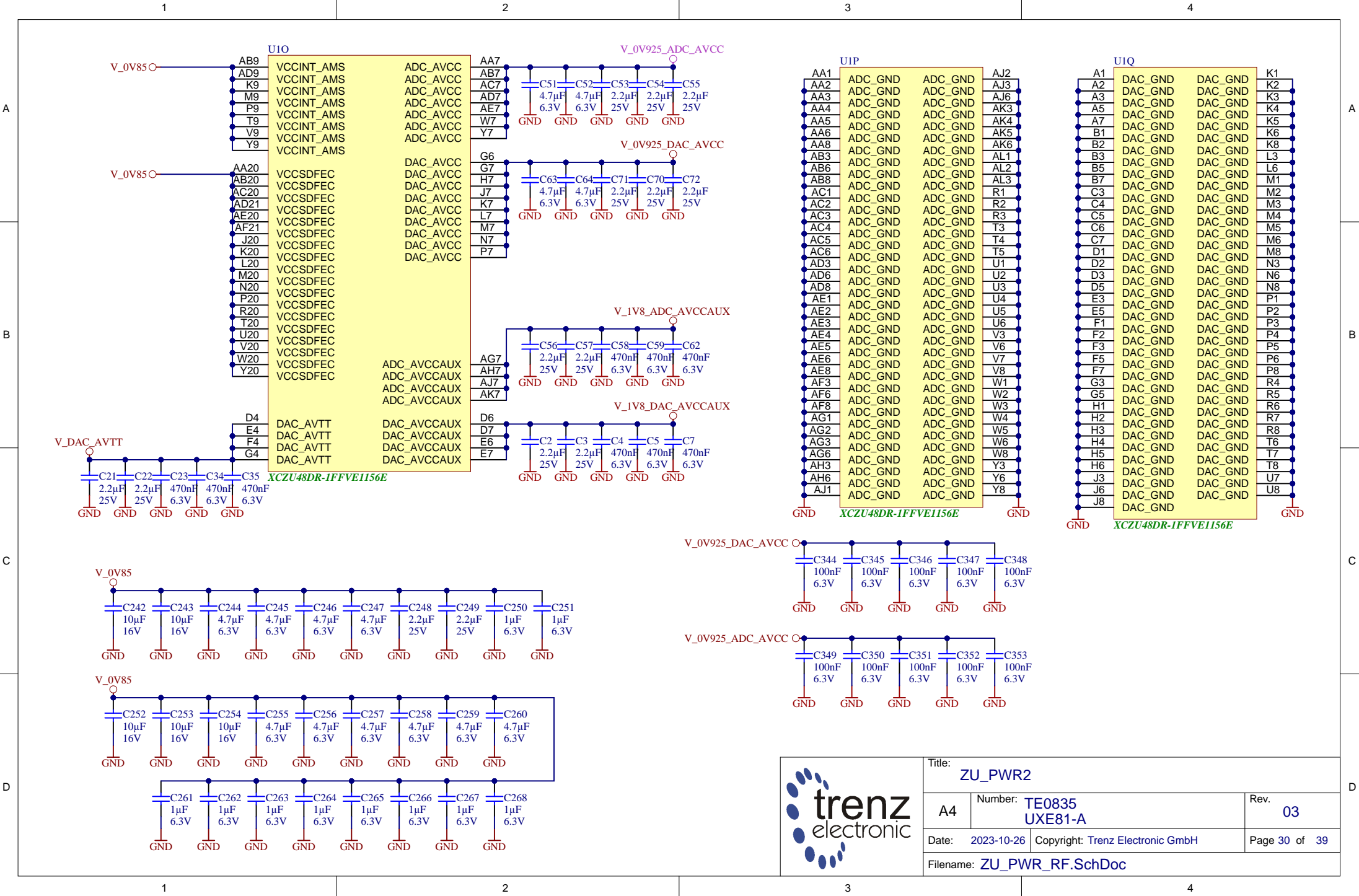
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A4	Number: TE0835 UXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 27 of 39
Filename: ZU_PSDDR_B504.SchDoc		



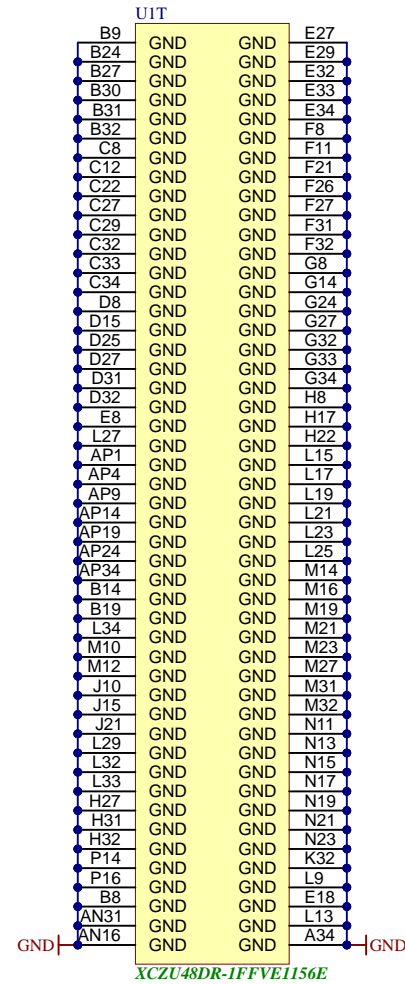
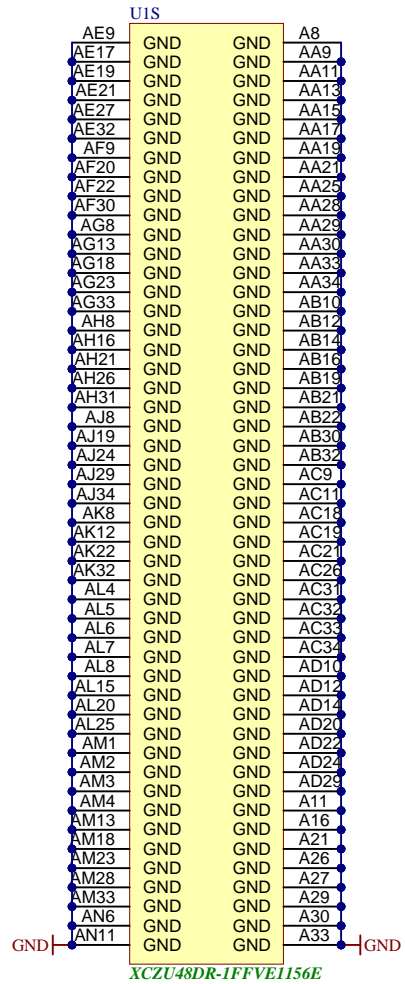
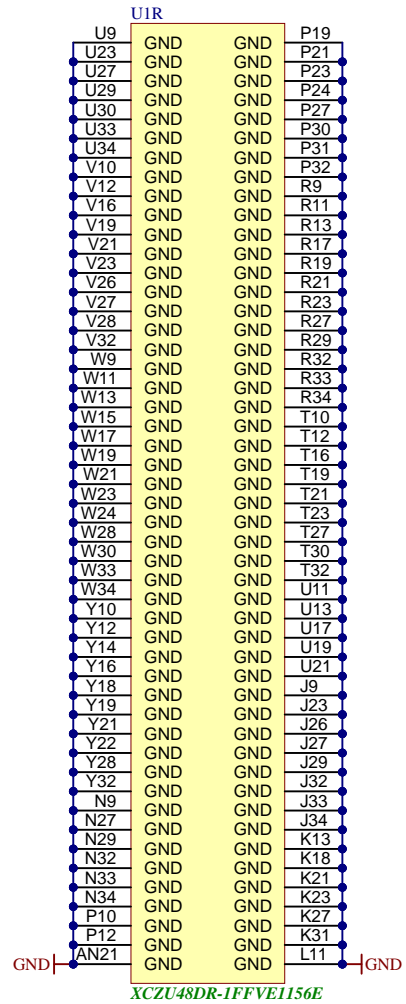
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	A4	Number: TE0835 UXE81-A
	Date: 2023-10-26	Copyright: Trenz Electronic GmbH
	Filename: ZU_PSMGT_B505.SchDoc	
	Rev. 03	Page 28 of 39



Title: ZU_PWR		
A4	Number: TE0835 UXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 29 of 39
Filename: ZU_PWR.SchDoc		



Title: ZU_PWR2		
A4	Number: TE0835 UXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 30 of 39
Filename: ZU_PWR_RF.SchDoc		



Title: ZU_PWR3		
A4	Number: TE0835 UXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 31 of 39
Filename: ZU_GND.SchDoc		

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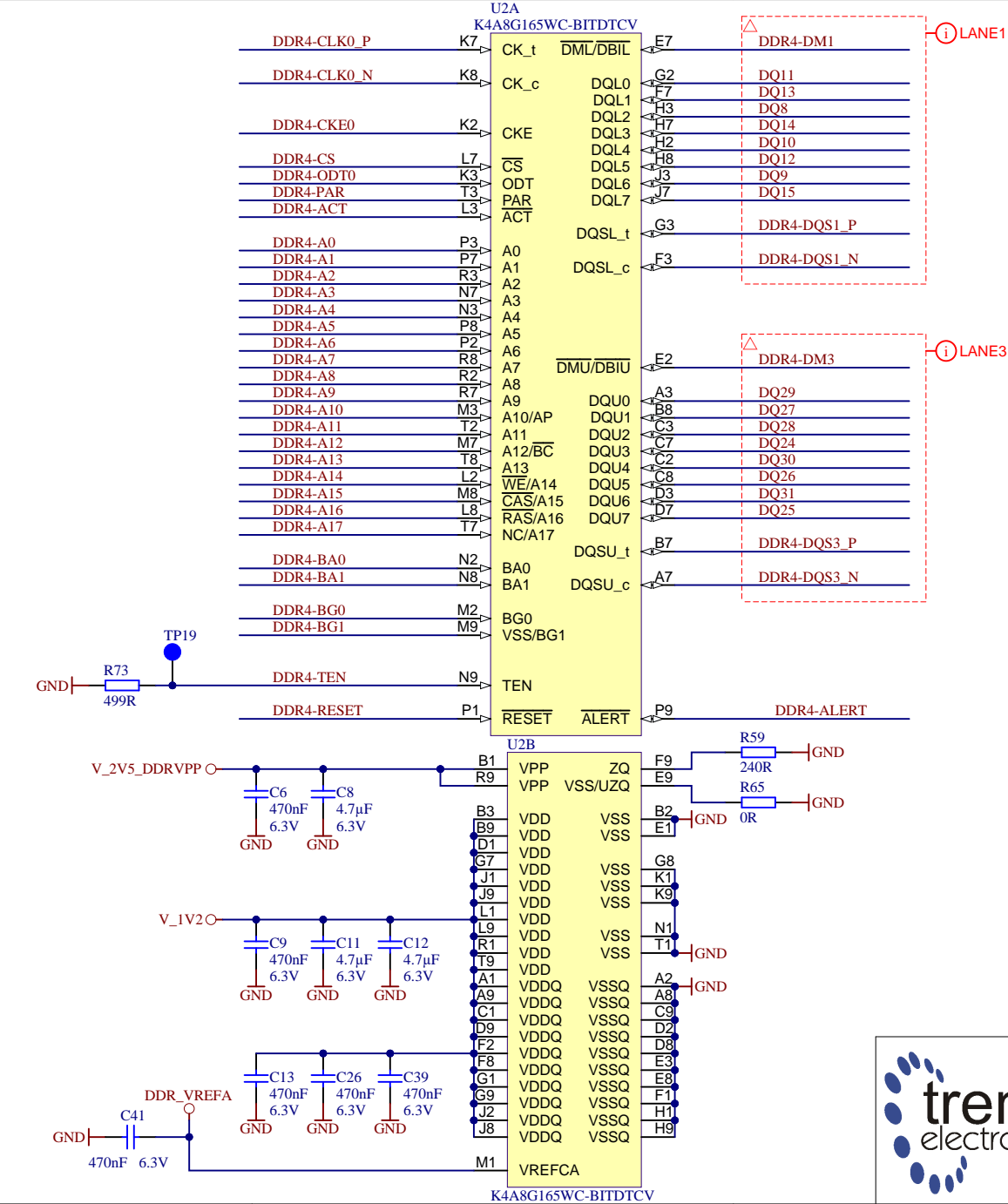
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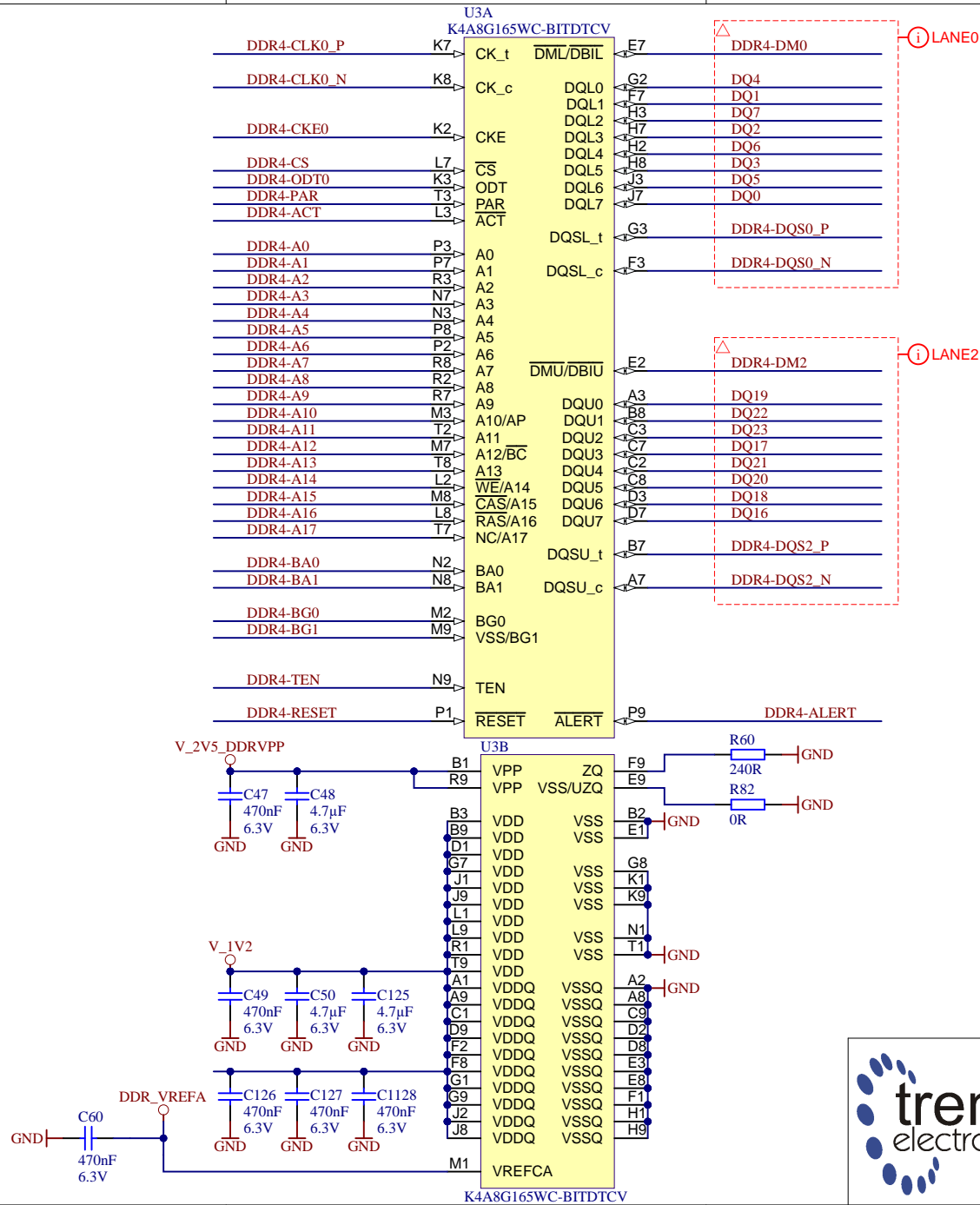
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A4	Number: TE0835 UXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 32 of 39
Filename: DDR4-RAM_1.SchDoc		

1

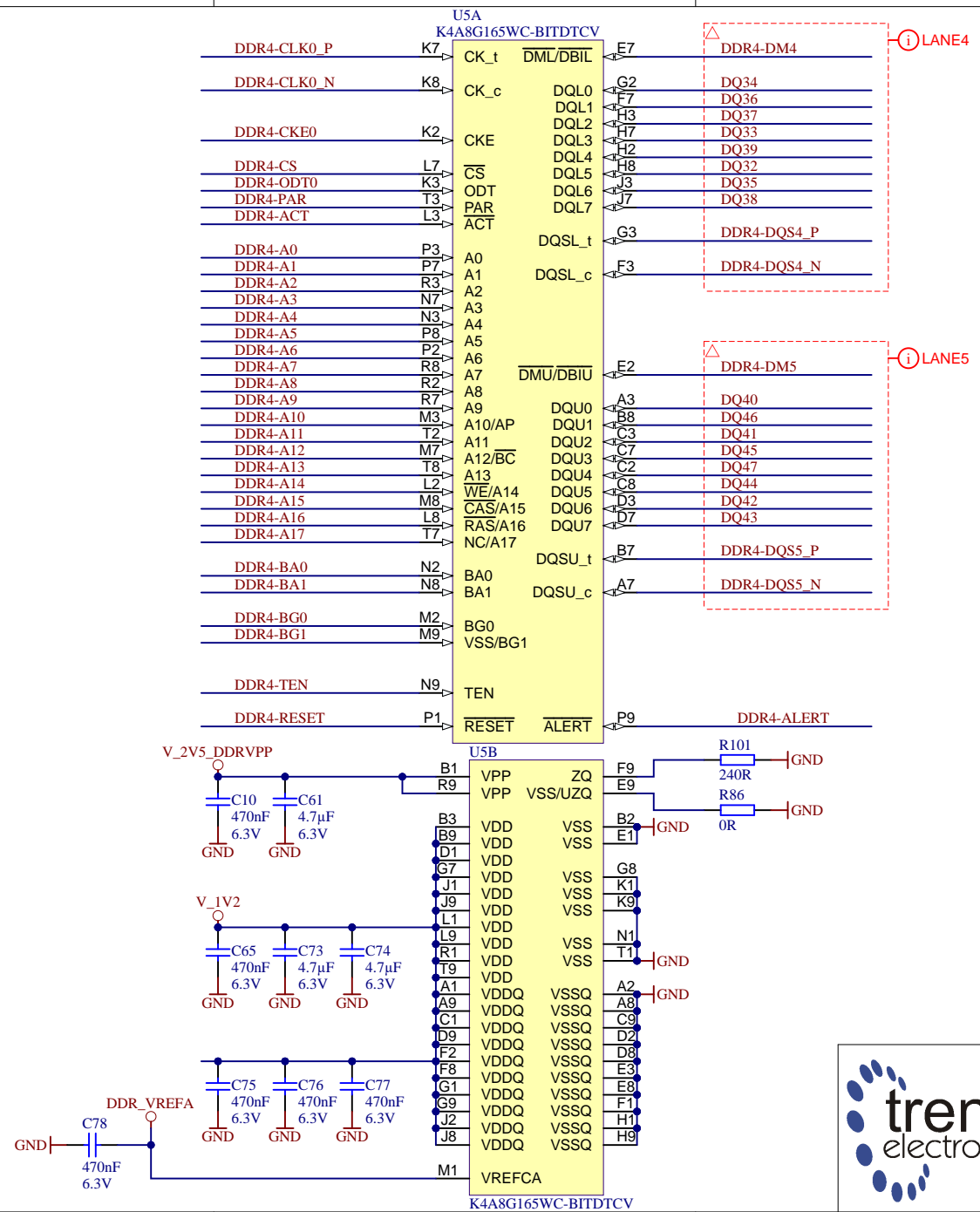
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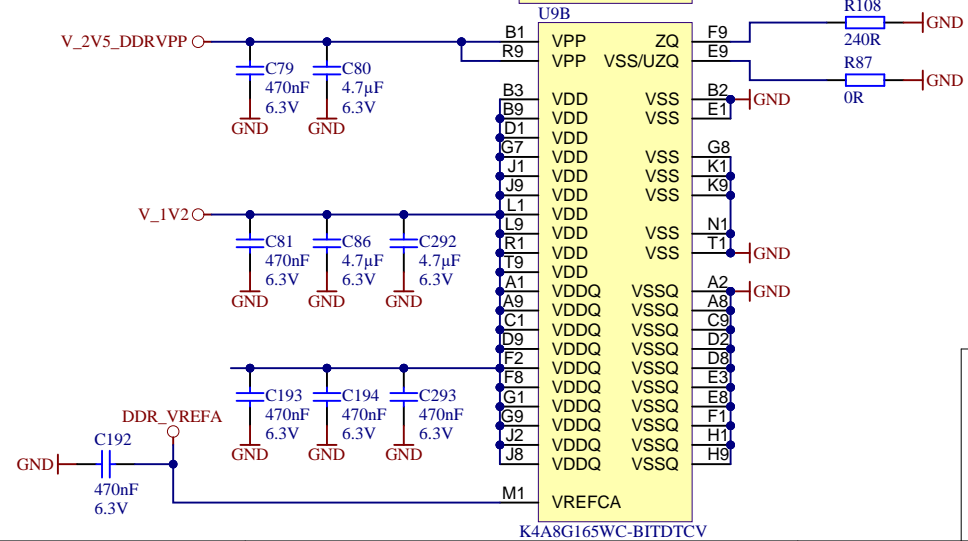
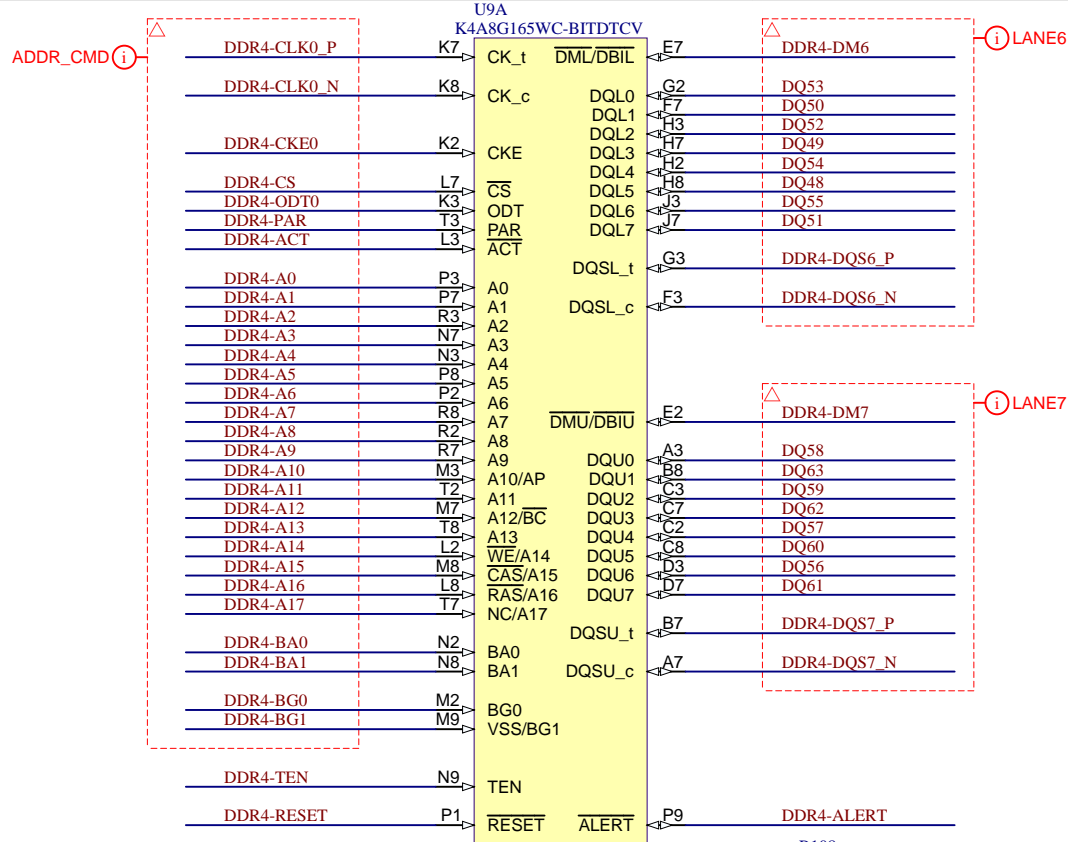
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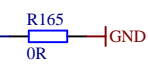
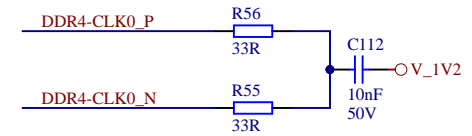
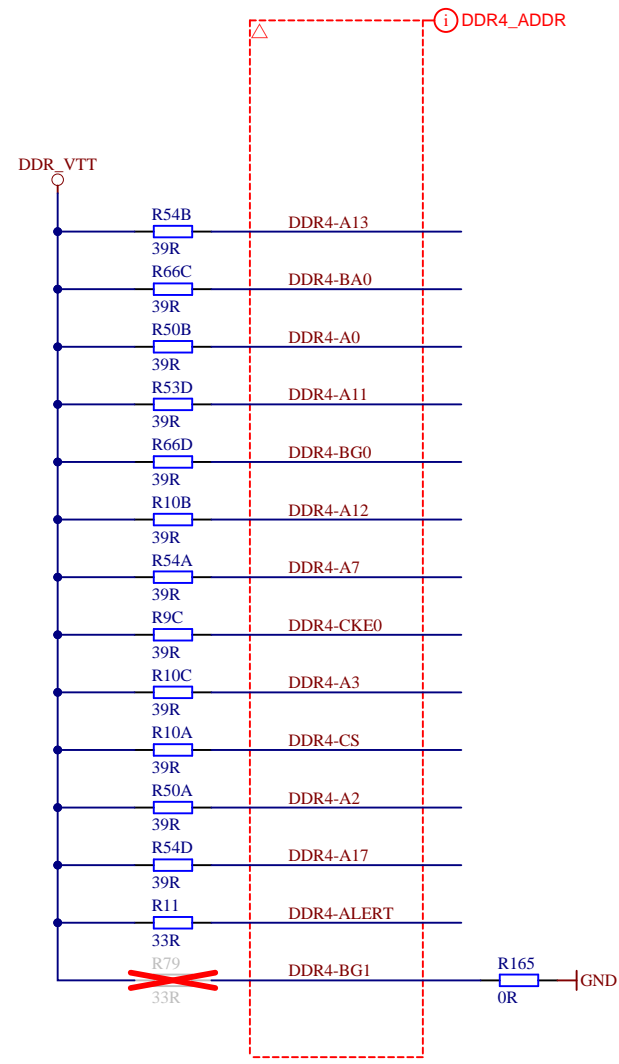
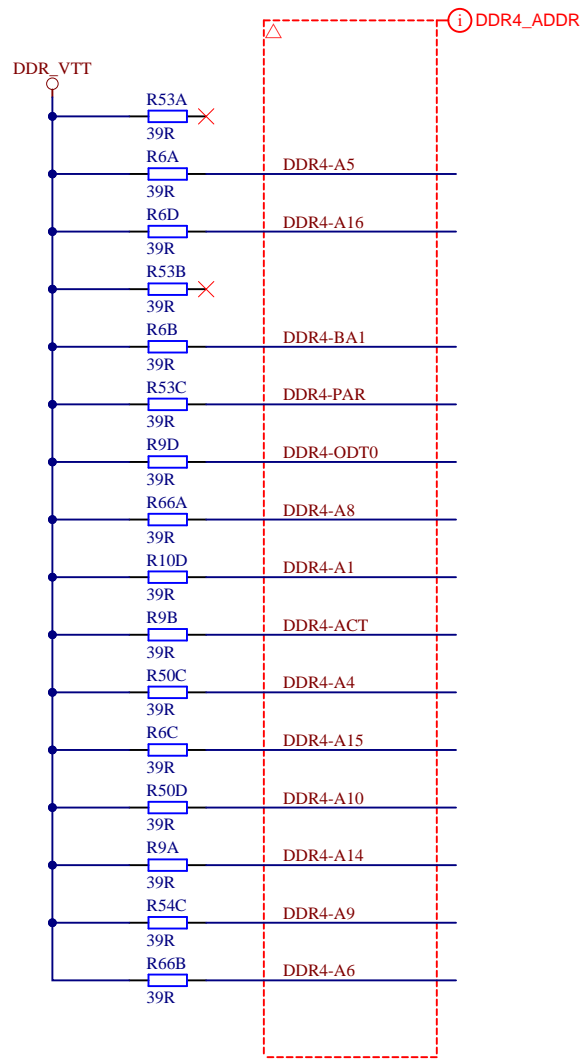
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Date: 2023-10-26	Copyright: Trenz Electronic GmbH	
Page 33 of 39		
Filename: DDR4-RAM_2.SchDoc		



Title: DDR4-RAM_3		
A4	Number: TE0835 UXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	
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Filename: DDR4-RAM_3.SchDoc		



Title: DDR4-RAM_4		
A4	Number: TE0835 UXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 35 of 39
Filename: DDR4-RAM_4.SchDoc		



Title: DDR4-TERM		
A4	Number: TE0835 UXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 36 of 39
Filename: DDR4-TERM.SchDoc		

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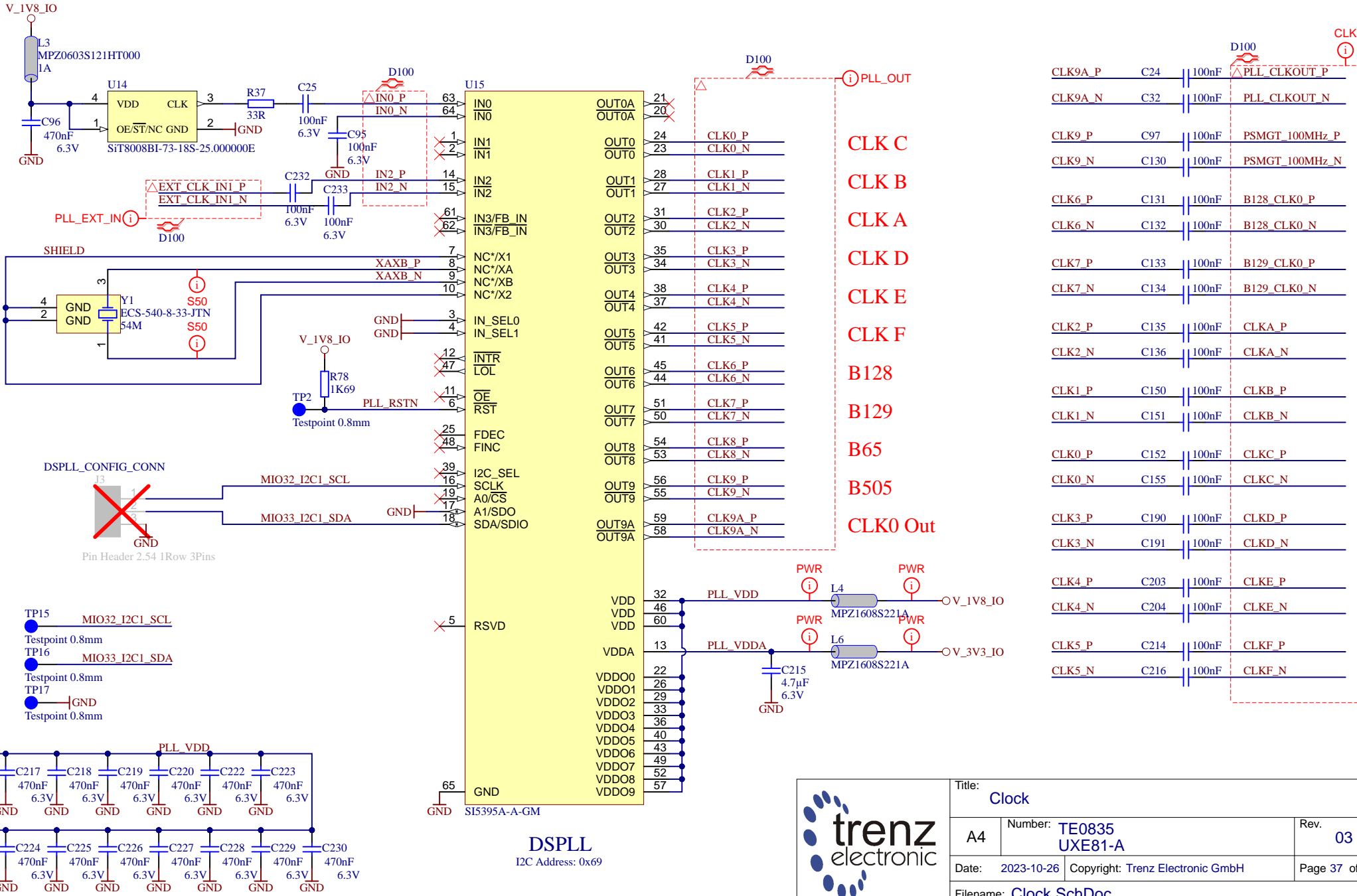
D

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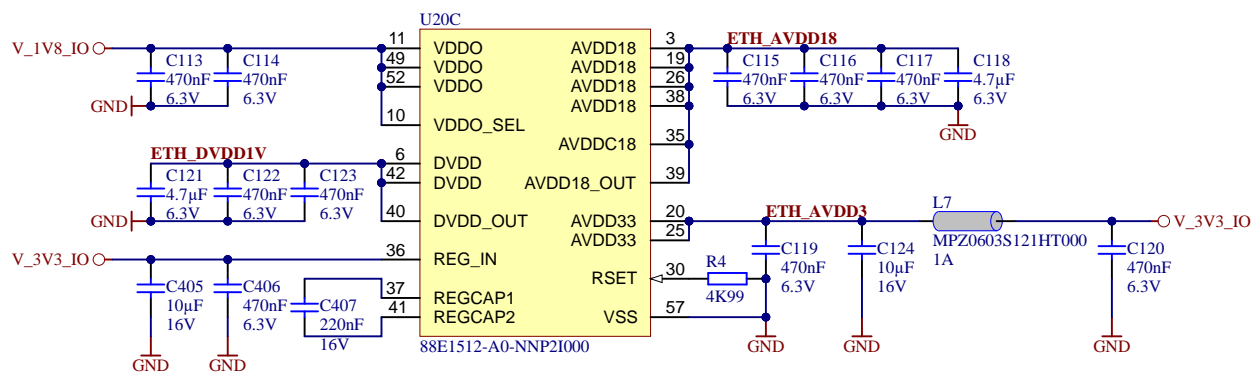
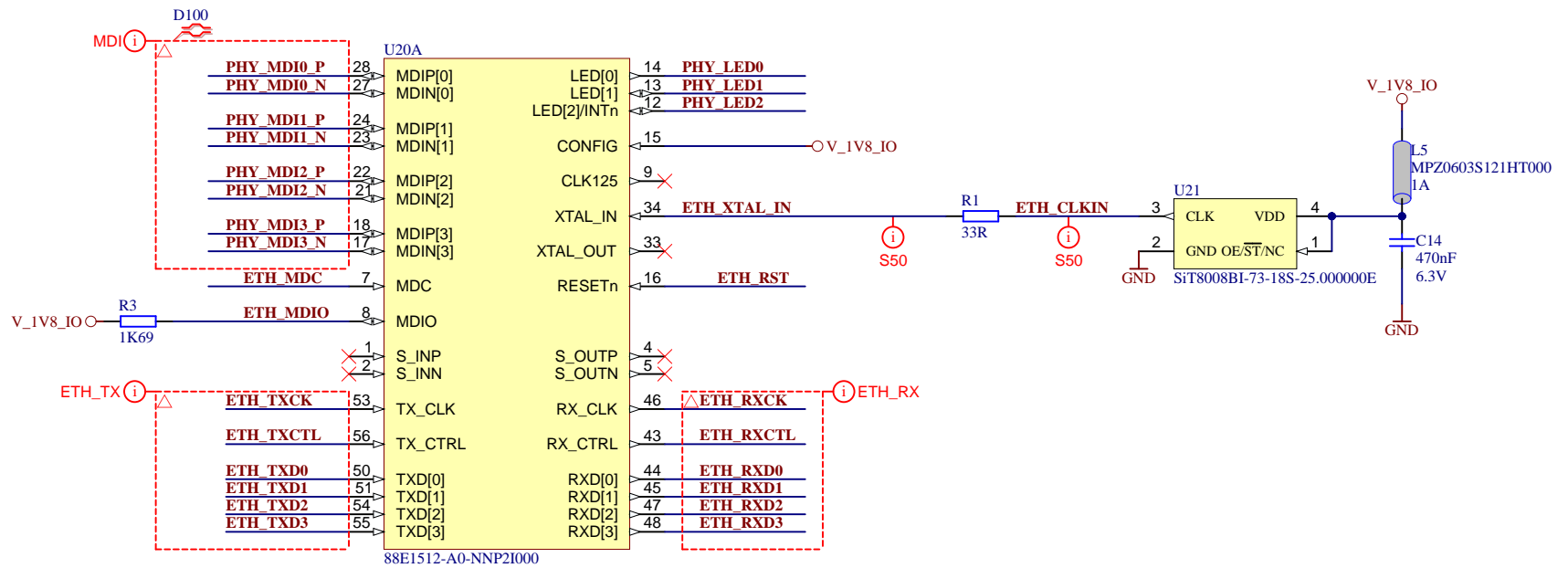
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DSPLL
I2C Address: 0x69



Title: Clock		
A4	Number: TE0835 UXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 37 of 39
Filename: Clock.SchDoc		



Title: Ethernet		
A4	Number: TE0835 UXE81-A	Rev. 03
Date: 2023-10-26	Copyright: Trenz Electronic GmbH	Page 38 of 39
Filename: Ethernet.SchDoc		

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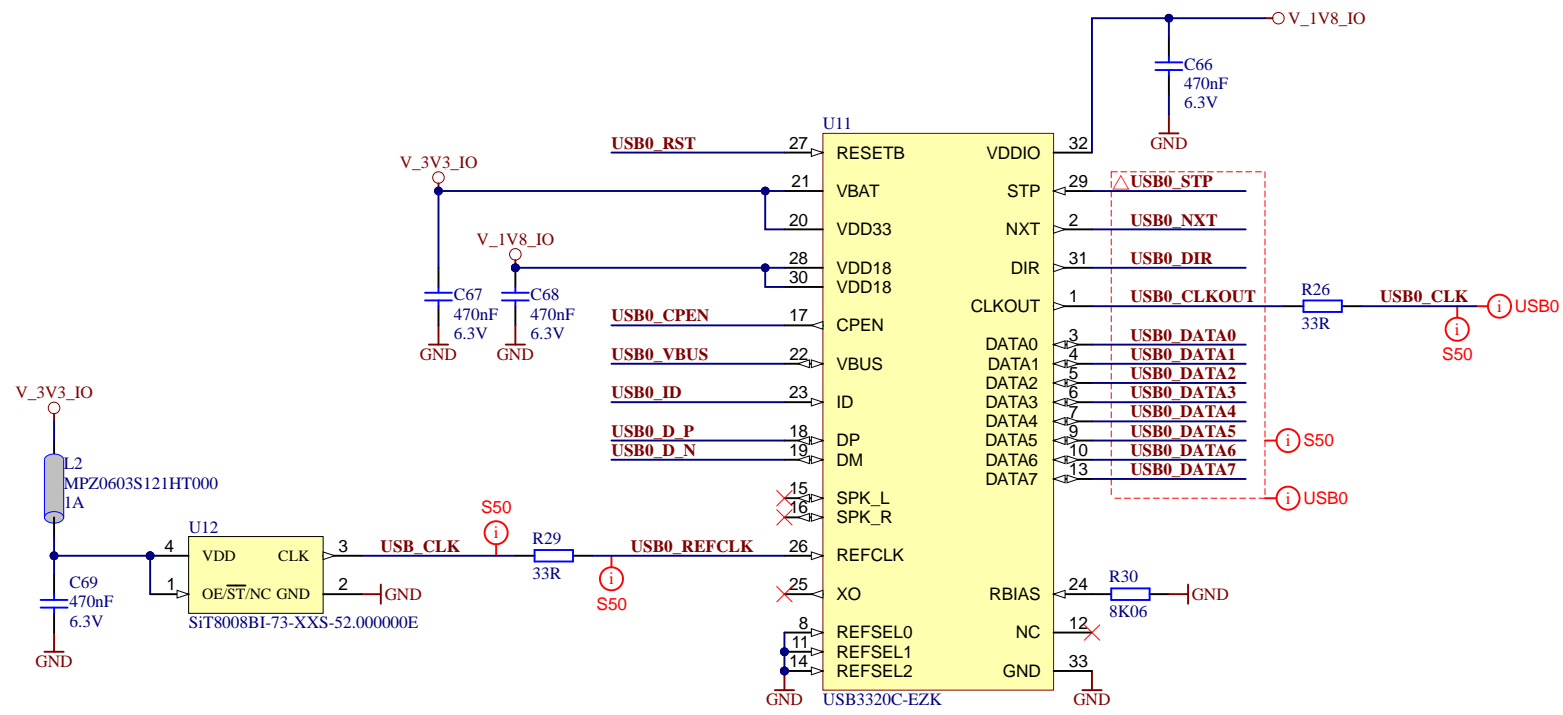
B


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		A4	Number: TE0835 UXE81-A
Date: 2023-10-26		Copyright: Trenz Electronic GmbH	
Filename: USB-PHY.SchDoc		Page 39 of 39	

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