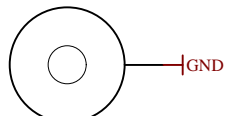
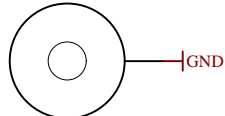


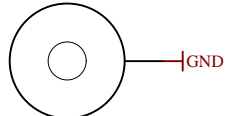
Mount.Hole 3.2mm für Unterlegscheibe



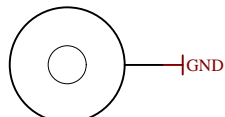
Mount.Hole 3.2mm für Unterlegscheibe



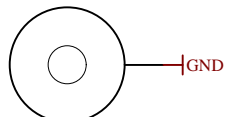
Mount.Hole 3.2mm für Unterlegscheibe



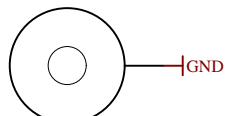
Mount.Hole 3.2mm für Unterlegscheibe



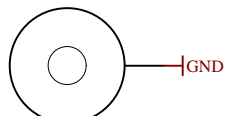
Mount.Hole 3.2mm für Unterlegscheibe



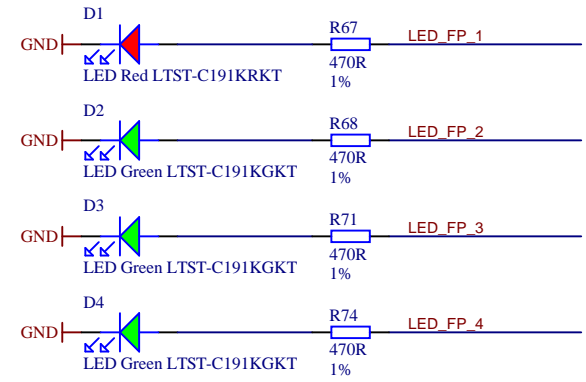
Mount.Hole 3.2mm für Unterlegscheibe



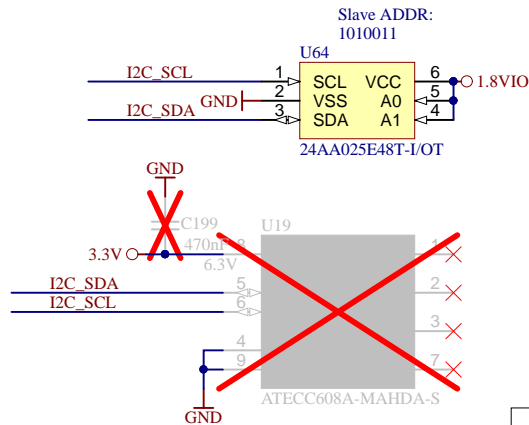
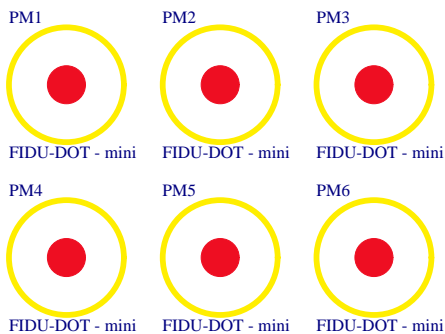
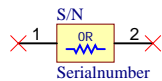
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



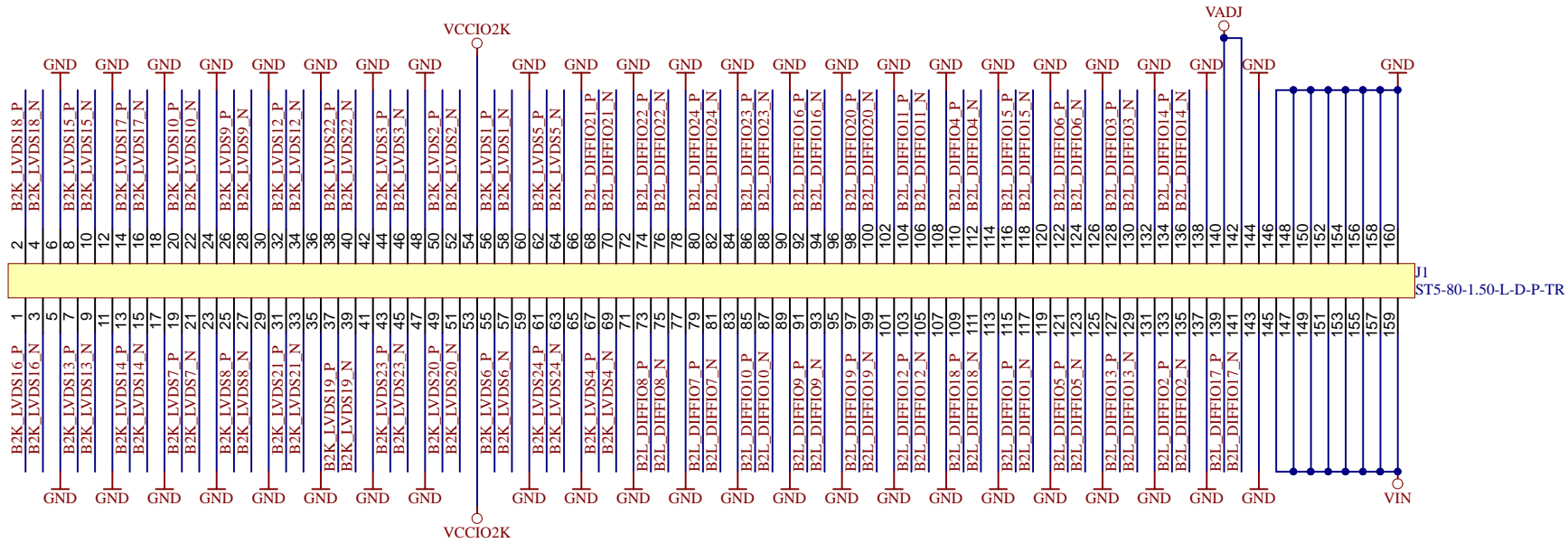
Serial  
 Serialnummer 6,3 x 6,3mm



Assembly variant	150-6E
Created by	VT
Modified by	VariantModifiedBy
Modified at	2020-04-23
SVN Revision	11759



Title: TEI0006		
A4	Number: TEI0006 150-6E	Rev. 02
Date: 2019-09-11	Copyright: Trenz Electronic GmbH / TT	Page1 of 22
Filename: TEI0006.SchDoc		



J1  
ST5-80-1.50-L-D-P-TR



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A4	Number: TEI0006 150-6E	Page 2 of 22
Date: 2019-09-11	Copyright: Trenz Electronic GmbH / TT	Page 2 of 22
Filename: J1.SchDoc		

1

2

3

4

A

A

B

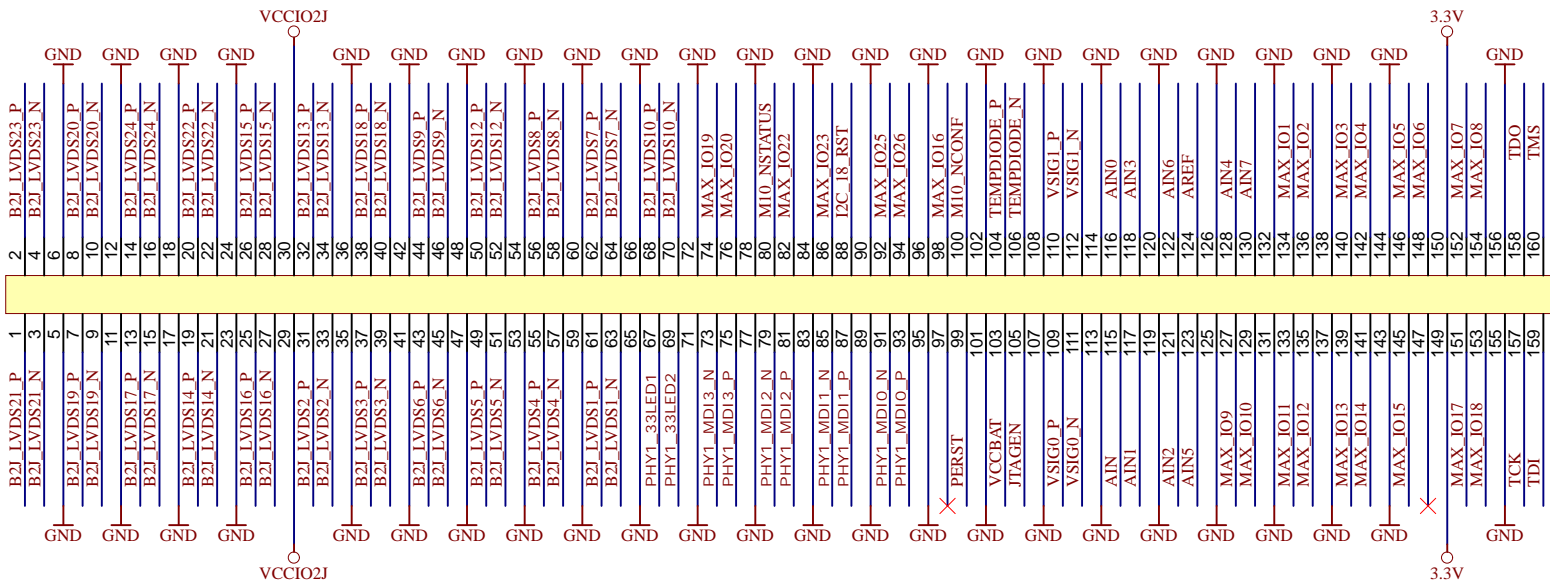
B


C

C

D

D



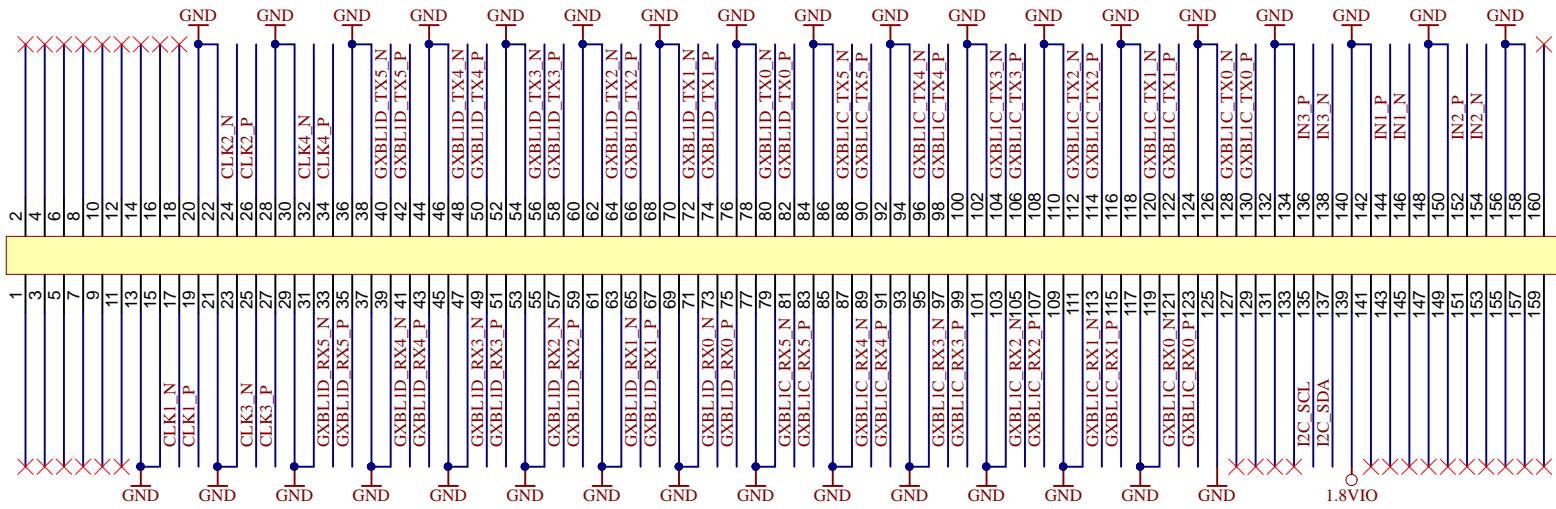
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		A4	Number: <b>TEI0006 150-6E</b>
Date: <b>2019-09-11</b>		Copyright: <b>Trenz Electronic GmbH / TT</b>	
Filename: <b>J2.SchDoc</b>		Page <b>3</b> of <b>22</b>	

1

2

3

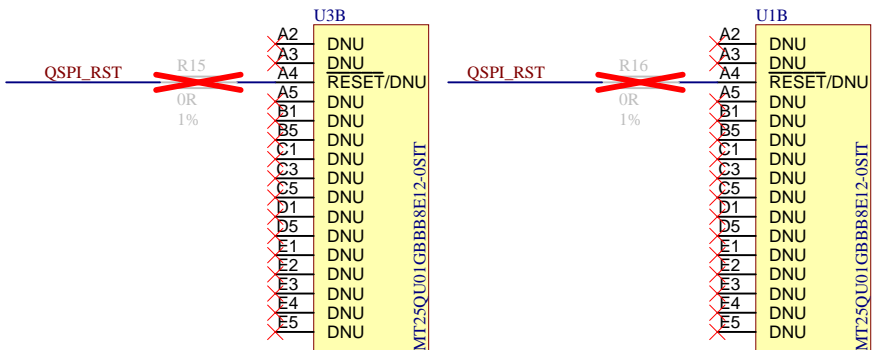
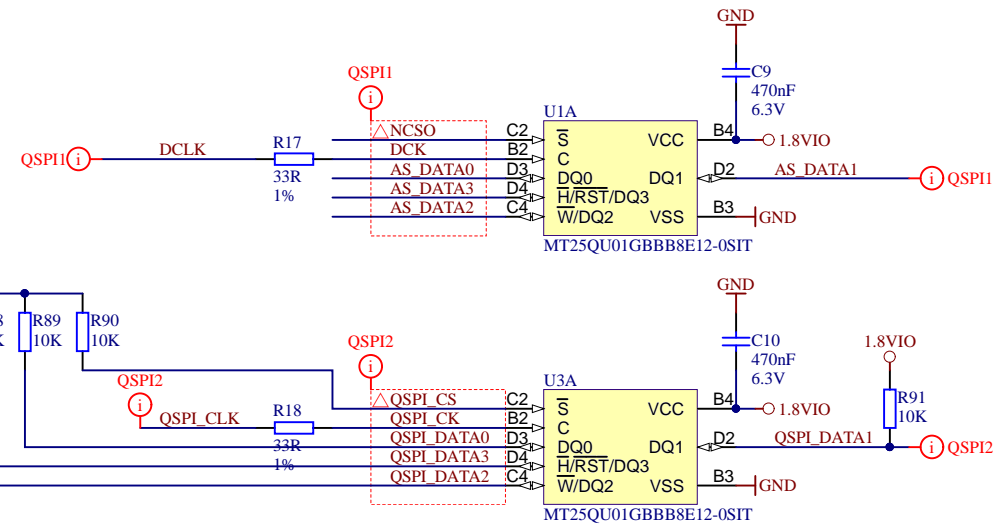
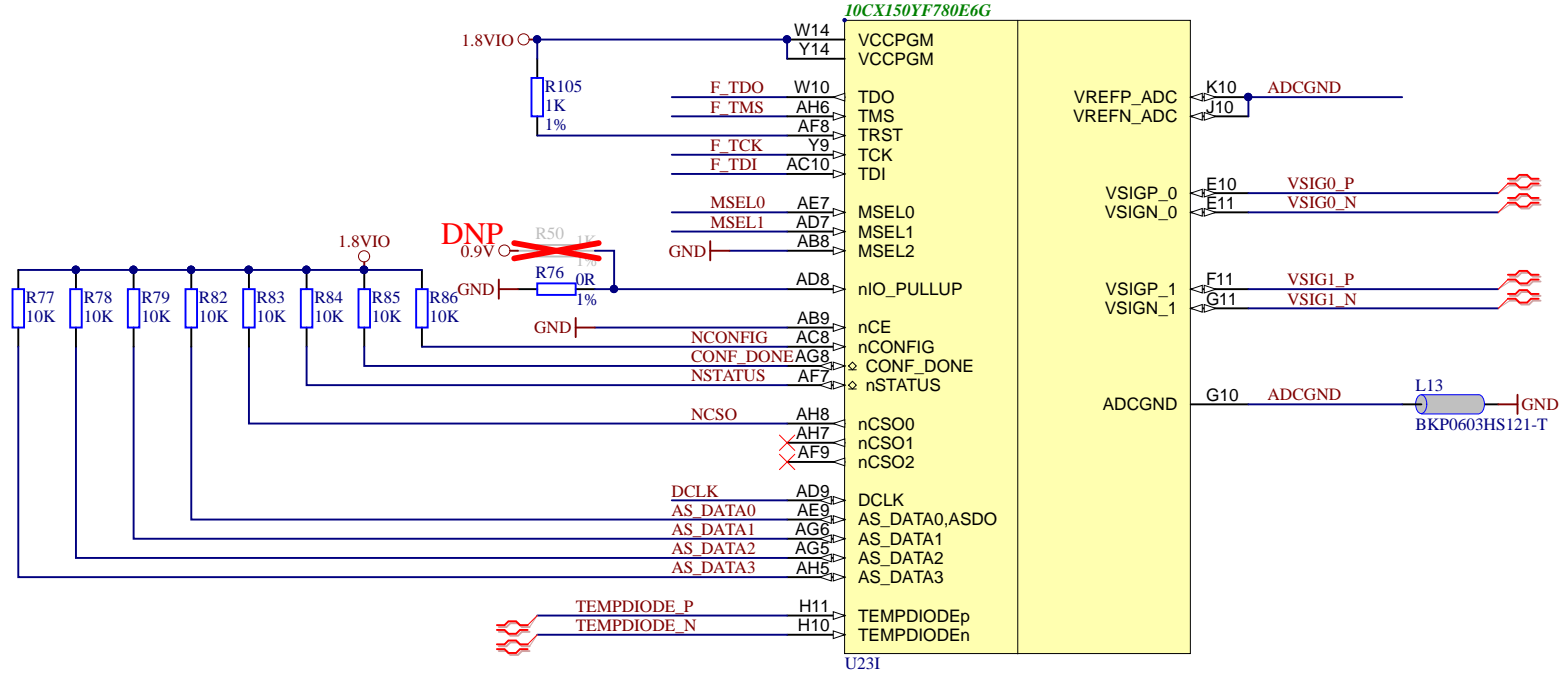
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J3  
ST5-80-1.50-L-D-P-TR

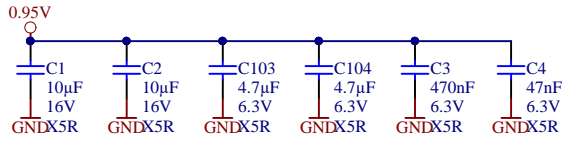


Title: TEI0006		
A4	Number: TEI0006 150-6E	Rev. 02
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Filename: J3.SchDoc		

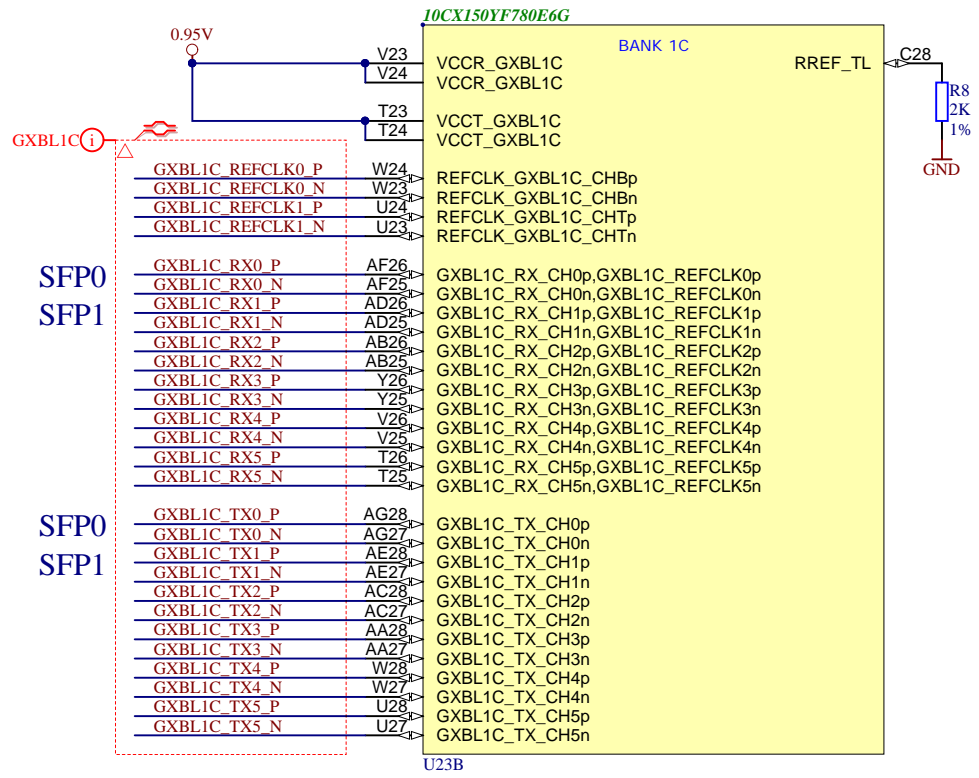
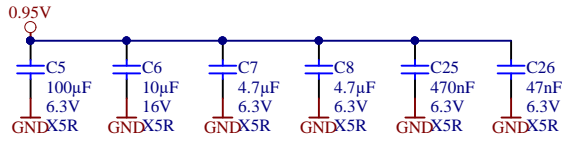


Title: TEI0006		
A4	Number: TEI0006 150-6E	Rev. 02
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Filename: C10GX_CFG.SchDoc		

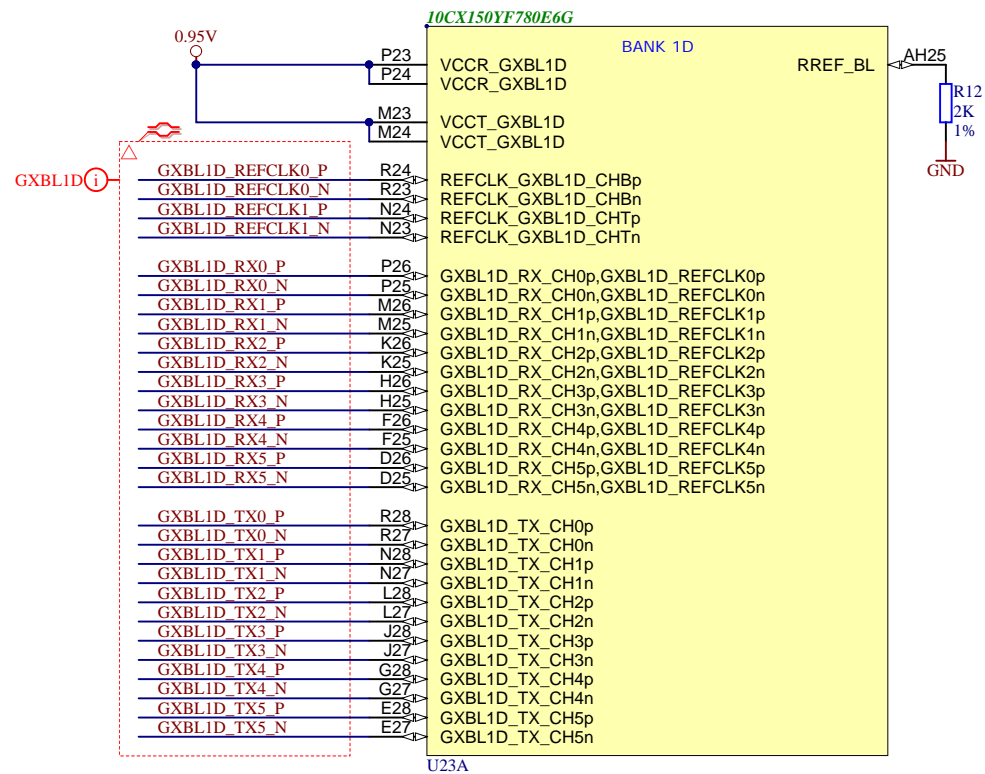
Placed at VCCT\_GXB pins




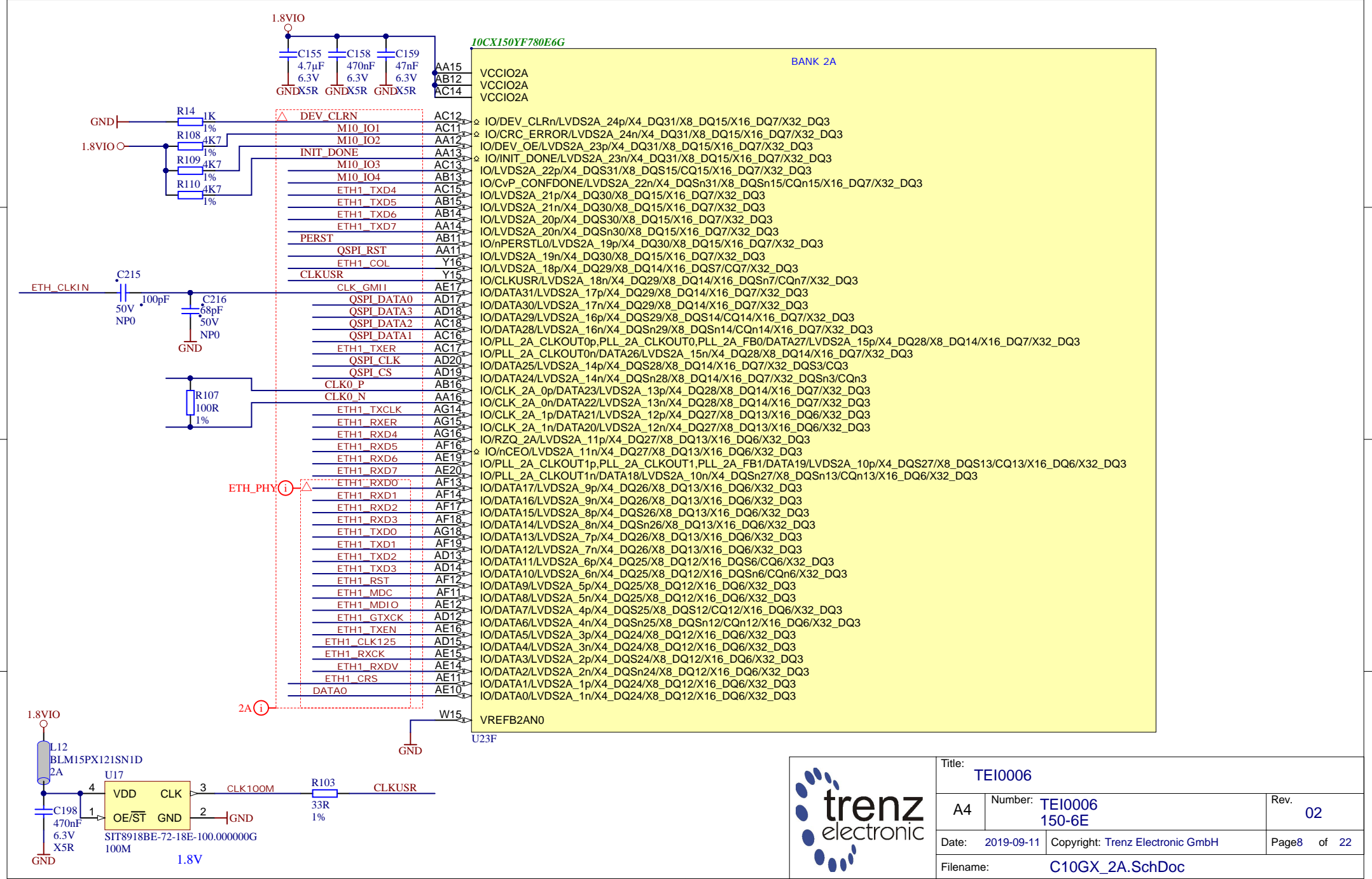
Placed at VCCR\_GXB pins



Title: TEI0006		
A4	Number: TEI0006 150-6E	Rev. 02
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Filename: C10GX_1C.SchDoc		

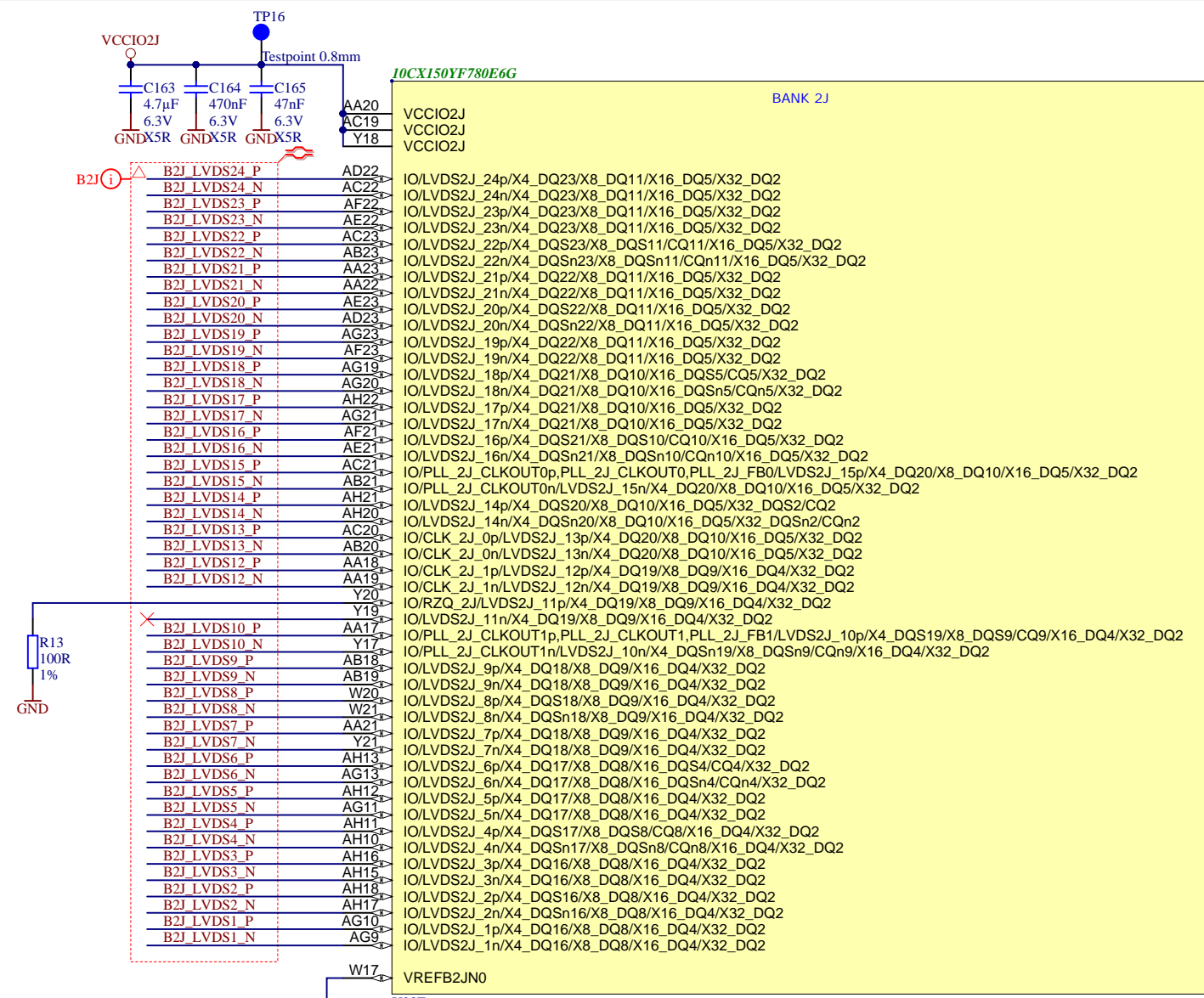


	Title: <b>TEI0006</b>		
	A4	Number: <b>TEI0006 150-6E</b>	Rev. <b>02</b>
	Date: <b>2019-09-11</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>7</b> of <b>22</b>
	Filename: <b>C10GX_1D.SchDoc</b>		

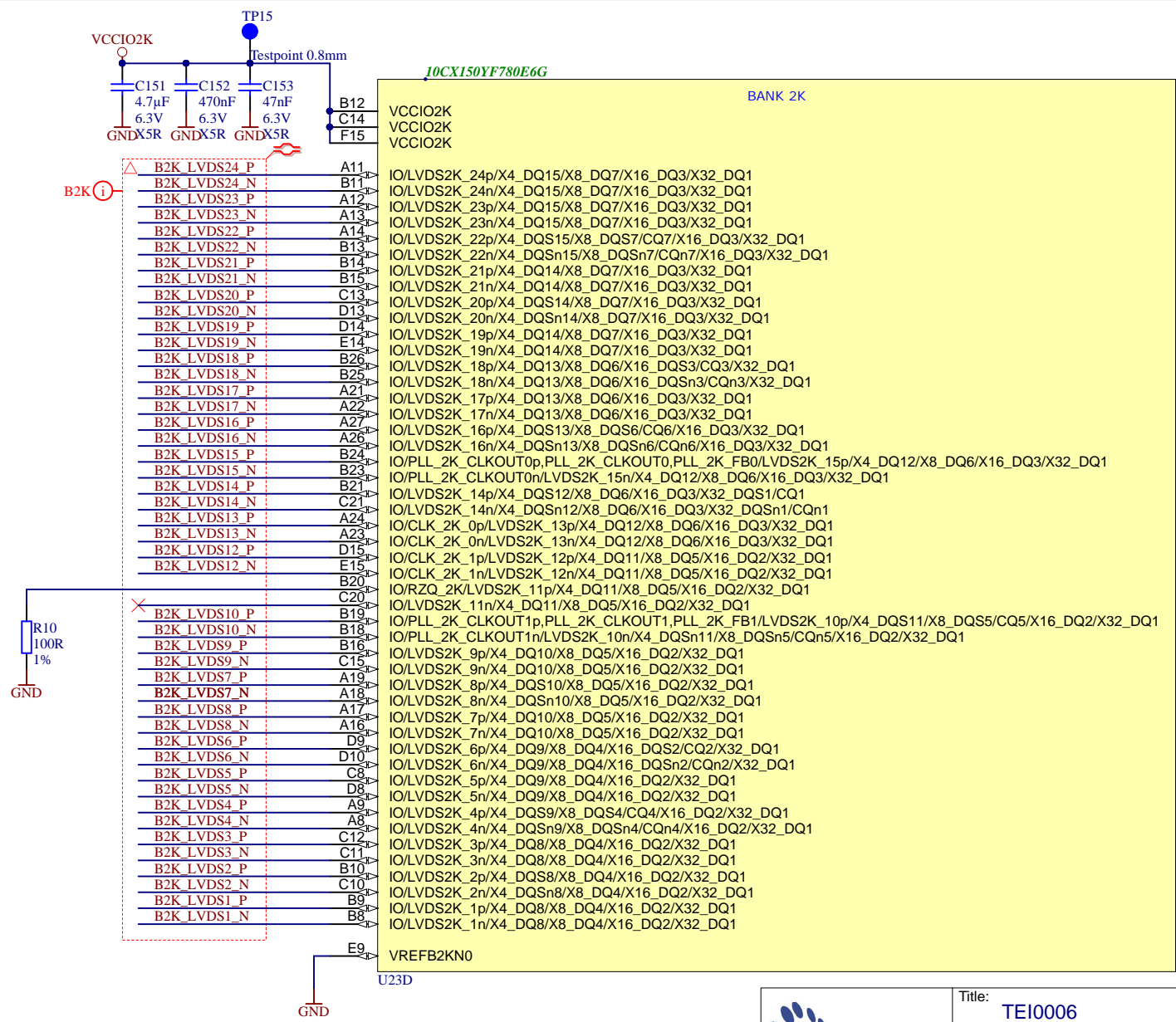


Title: <b>TEI0006</b>		
A4	Number: <b>TEI0006 150-6E</b>	Rev. <b>02</b>
Date: <b>2019-09-11</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>8</b> of <b>22</b>
Filename: <b>C10GX_2A.SchDoc</b>		

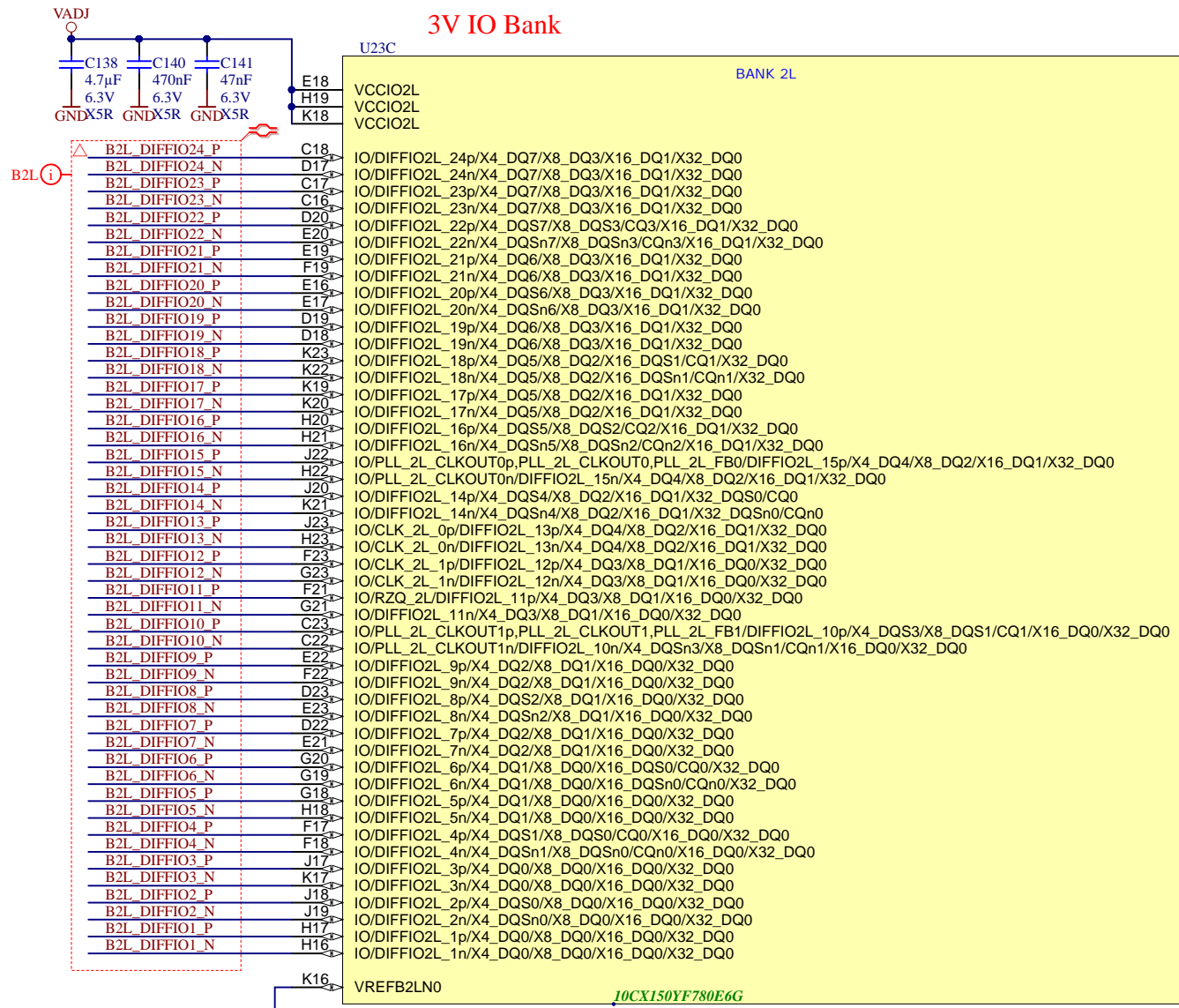




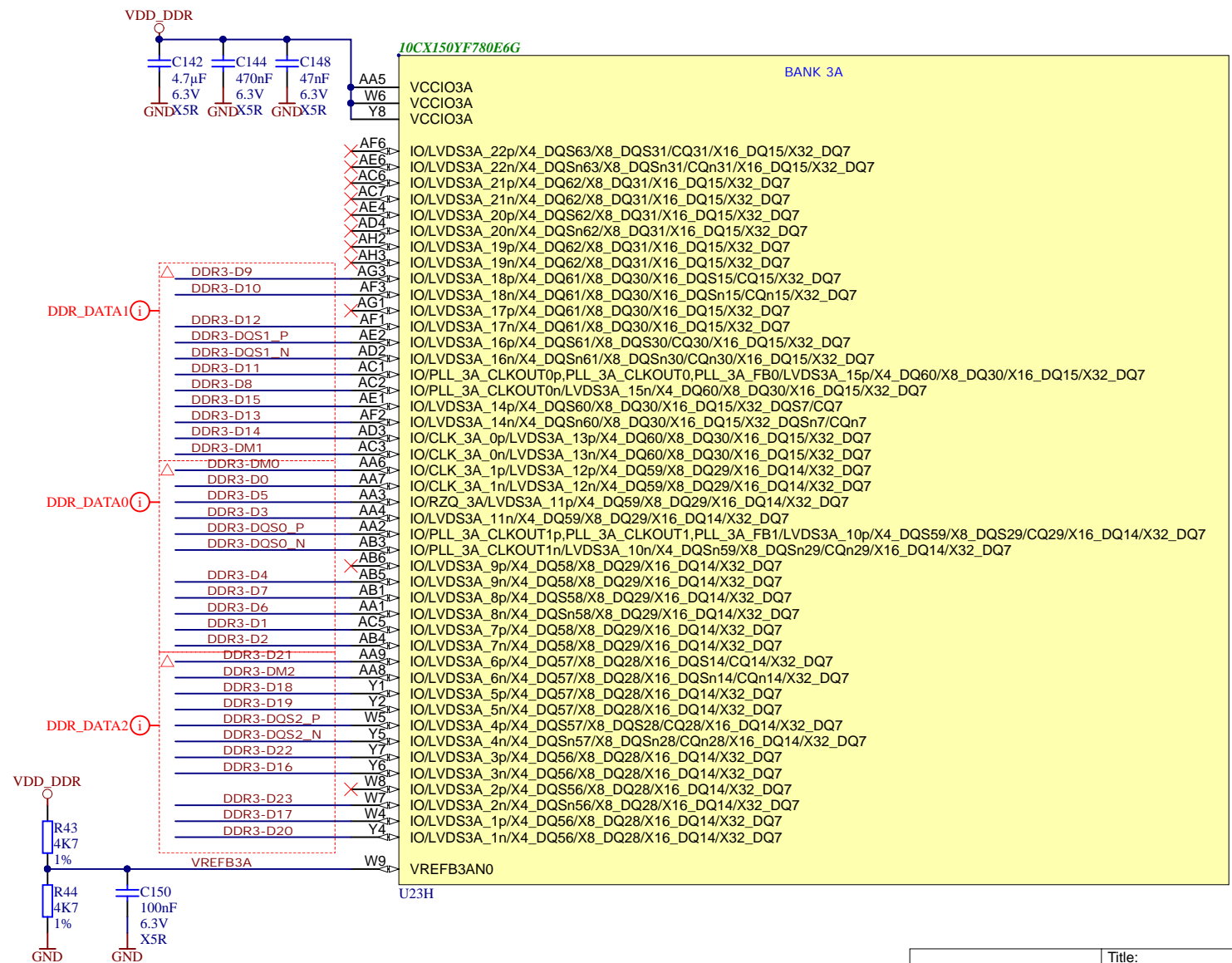
Title: TEI0006			
A4	Number: TEI0006 150-6E	Rev. 02	
Date: 2019-09-11	Copyright: Trenz Electronic GmbH	Page9 of 22	
Filename: C10GX_2J.SchDoc			



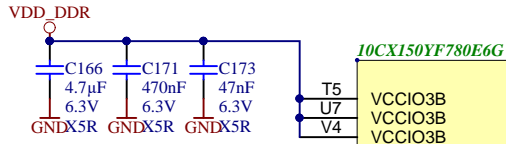
Title: TEI0006		
A4	Number: TEI0006 150-6E	Rev. 02
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A4	Number: TEI0006 150-6E	Rev. 02
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Filename: C10GX_2L.SchDoc		



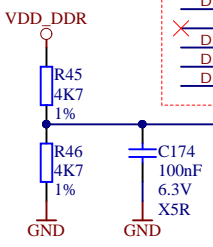
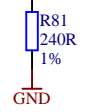
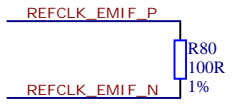
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A4	Number: <b>TEI0006 150-6E</b>	Rev. <b>02</b>
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Filename: <b>C10GX_3A.SchDoc</b>		



**10CX150YF780E6G**

**BANK 3B**

VCCIO3B	VCCIO3B
VCCIO3B	VCCIO3B
VCCIO3B	VCCIO3B
IO/LVDS3B_24p/X4_DQ55/X8_DQ27/X16_DQ13/X32_DQ6	W3
IO/LVDS3B_24n/X4_DQ55/X8_DQ27/X16_DQ13/X32_DQ6	V3
IO/LVDS3B_23p/X4_DQ55/X8_DQ27/X16_DQ13/X32_DQ6	W2
IO/LVDS3B_23n/X4_DQ55/X8_DQ27/X16_DQ13/X32_DQ6	V2
IO/LVDS3B_22p/X4_DQS55/X8_DQS27/CQ27/X16_DQ13/X32_DQ6	V5
IO/LVDS3B_22n/X4_DQS55/X8_DQS27/CQ27/X16_DQ13/X32_DQ6	V6
IO/LVDS3B_21p/X4_DQ54/X8_DQ27/X16_DQ13/X32_DQ6	U6
IO/LVDS3B_21n/X4_DQ54/X8_DQ27/X16_DQ13/X32_DQ6	V7
IO/LVDS3B_20p/X4_DQS54/X8_DQ27/X16_DQ13/X32_DQ6	V1
IO/LVDS3B_20n/X4_DQS54/X8_DQ27/X16_DQ13/X32_DQ6	U1
IO/LVDS3B_19p/X4_DQ54/X8_DQ27/X16_DQ13/X32_DQ6	U3
IO/LVDS3B_19n/X4_DQ54/X8_DQ27/X16_DQ13/X32_DQ6	U4
IO/LVDS3B_18p/X4_DQ53/X8_DQ26/X16_DQS13/CQ13/X32_DQ6	T1
IO/LVDS3B_18n/X4_DQ53/X8_DQ26/X16_DQS13/CQ13/X32_DQ6	R1
IO/LVDS3B_17p/X4_DQ53/X8_DQ26/X16_DQ13/X32_DQ6	L1
IO/LVDS3B_17n/X4_DQ53/X8_DQ26/X16_DQ13/X32_DQ6	K1
IO/LVDS3B_16p/X4_DQS53/X8_DQS26/CQ26/X16_DQ13/X32_DQ6	T2
IO/LVDS3B_16n/X4_DQS53/X8_DQS26/CQ26/X16_DQ13/X32_DQ6	R2
IO/PLL_3B_CLKOUT0p,PLL_3B_CLKOUT0,PLL_3B_FB0/LVDS3B_15p/X4_DQ52/X8_DQ26/X16_DQ13/X32_DQ6	P2
IO/PLL_3B_CLKOUT0n/LVDS3B_15n/X4_DQ52/X8_DQ26/X16_DQ13/X32_DQ6	H1
IO/LVDS3B_14p/X4_DQS52/X8_DQ26/X16_DQ13/X32_DQS6/CQ6	G1
IO/LVDS3B_14n/X4_DQS52/X8_DQ26/X16_DQ13/X32_DQS6/CQ6	N1
IO/CLK_3B_0p/LVDS3B_13p/X4_DQ52/X8_DQ26/X16_DQ13/X32_DQ6	M1
IO/CLK_3B_0n/LVDS3B_13n/X4_DQ52/X8_DQ26/X16_DQ13/X32_DQ6	L2
IO/CLK_3B_1p/LVDS3B_12p/X4_DQ51/X8_DQ25/X16_DQ12/X32_DQ6	L3
IO/CLK_3B_1n/LVDS3B_12n/X4_DQ51/X8_DQ25/X16_DQ12/X32_DQ6	K2
IO/RZQ_3B/LVDS3B_11p/X4_DQ51/X8_DQ25/X16_DQ12/X32_DQ6	J2
IO/LVDS3B_11n/X4_DQ51/X8_DQ25/X16_DQ12/X32_DQ6	H2
IO/PLL_3B_CLKOUT1p,PLL_3B_CLKOUT1,PLL_3B_FB1/LVDS3B_10p/X4_DQS51/X8_DQS25/CQ25/X16_DQ12/X32_DQ6	J3
IO/PLL_3B_CLKOUT1n/LVDS3B_10n/X4_DQS51/X8_DQS25/CQ25/X16_DQ12/X32_DQ6	N2
IO/LVDS3B_9p/X4_DQ50/X8_DQ25/X16_DQ12/X32_DQ6	N3
IO/LVDS3B_9n/X4_DQ50/X8_DQ25/X16_DQ12/X32_DQ6	K4
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IO/LVDS3B_6p/X4_DQ49/X8_DQ24/X16_DQS12/CQ12/X32_DQ6	V8
IO/LVDS3B_6n/X4_DQ49/X8_DQ24/X16_DQS12/CQ12/X32_DQ6	T4
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IO/LVDS3B_5n/X4_DQ49/X8_DQ24/X16_DQ12/X32_DQ6	R4
IO/LVDS3B_4p/X4_DQS49/X8_DQS24/CQ24/X16_DQ12/X32_DQ6	R5
IO/LVDS3B_4n/X4_DQS49/X8_DQS24/CQ24/X16_DQ12/X32_DQ6	T6
IO/LVDS3B_3p/X4_DQ48/X8_DQ24/X16_DQ12/X32_DQ6	T7
IO/LVDS3B_3n/X4_DQ48/X8_DQ24/X16_DQ12/X32_DQ6	T8
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IO/LVDS3B_1p/X4_DQ48/X8_DQ24/X16_DQ12/X32_DQ6	P4
IO/LVDS3B_1n/X4_DQ48/X8_DQ24/X16_DQ12/X32_DQ6	U9
VREFB3B0	U23G



Title: <b>TEI0006</b>		
A4	Number: <b>TEI0006 150-6E</b>	Rev. <b>02</b>
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Filename: <b>C10GX_3B.SchDoc</b>		

A

B

C

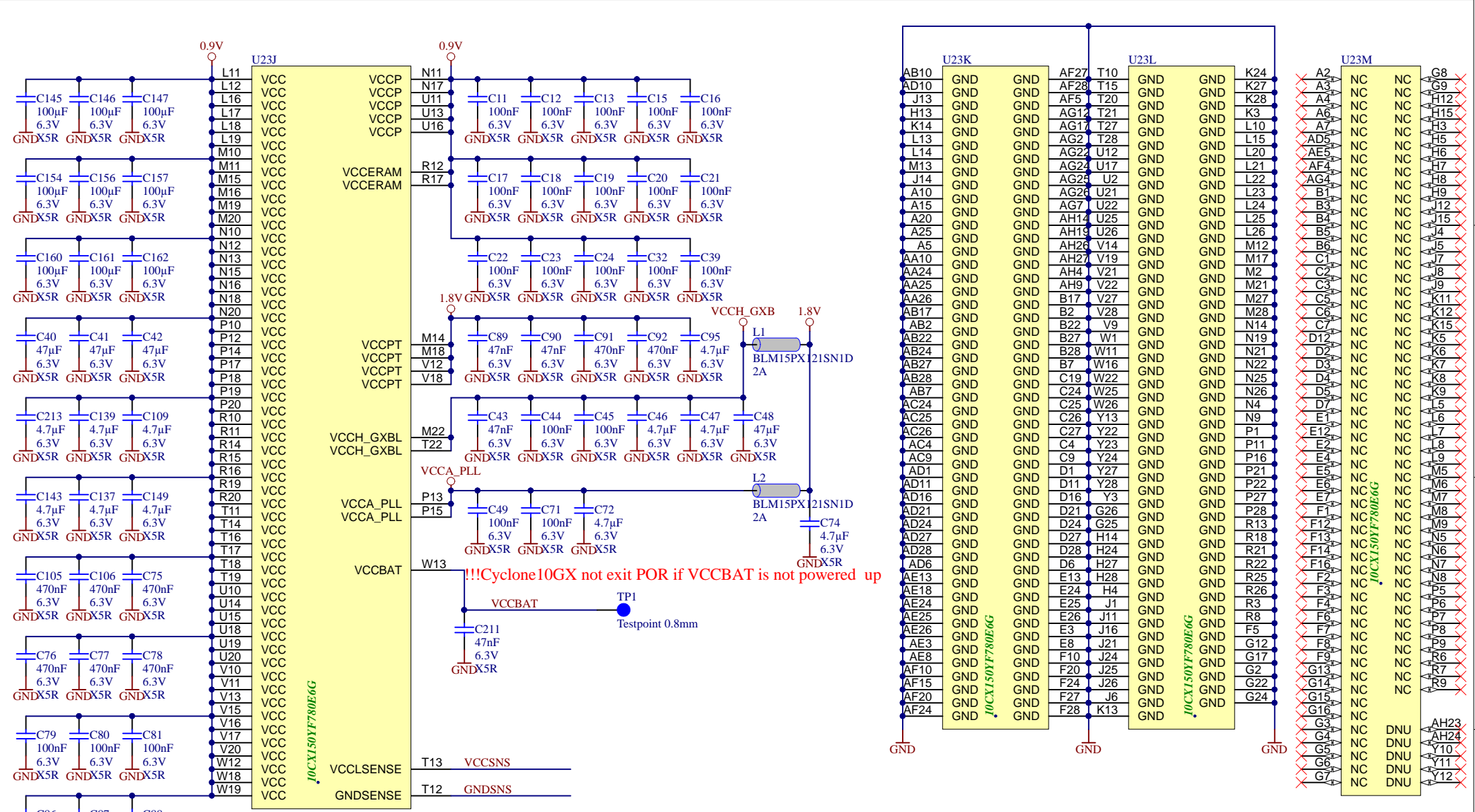
D

A

B

C

D



Title: TEI0006		
A4	Number: TEI0006 150-6E	Rev. 02
Date: 2019-09-11	Copyright: Trenz Electronic GmbH	Page 14 of 22
Filename: C10GX_PWR.SchDoc		

A

B

C

D

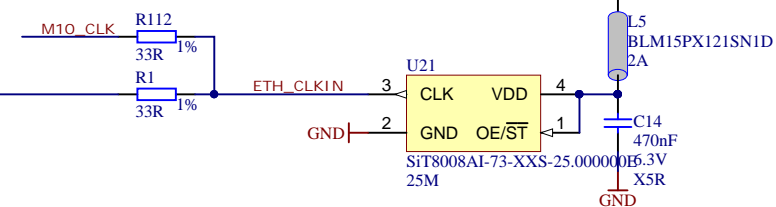
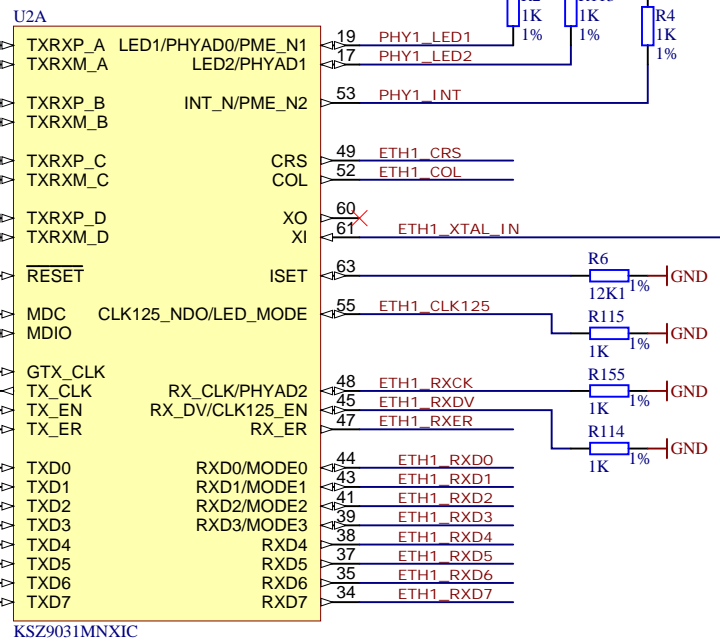
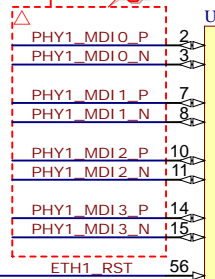
A

B

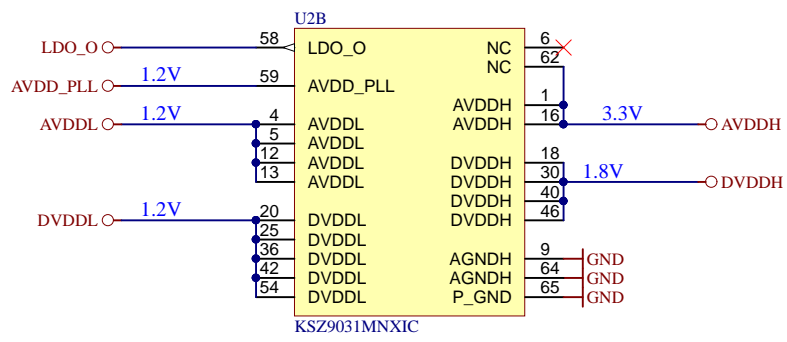
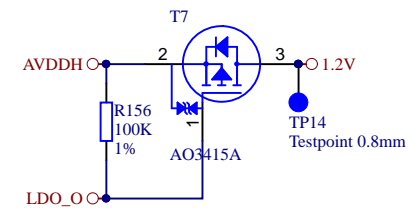
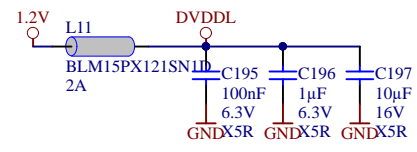
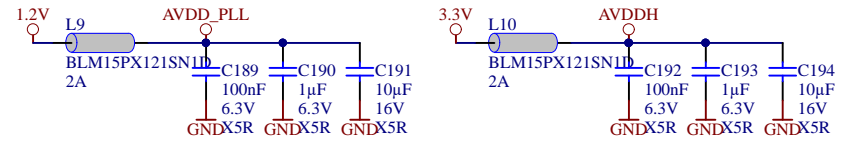
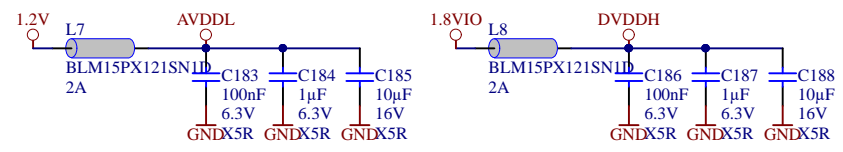
C

D

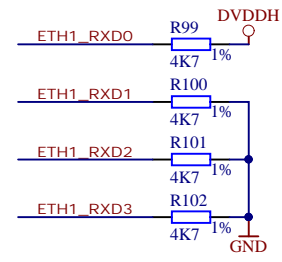
ETH\_MDI



PHY Address: 0001



MODE: 0001 -> GMII/MII mode



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A4	Number: TEI0006 150-6E	Rev. 02
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Filename: EthPHY1.SchDoc		

1

2

3

4

A

A

B

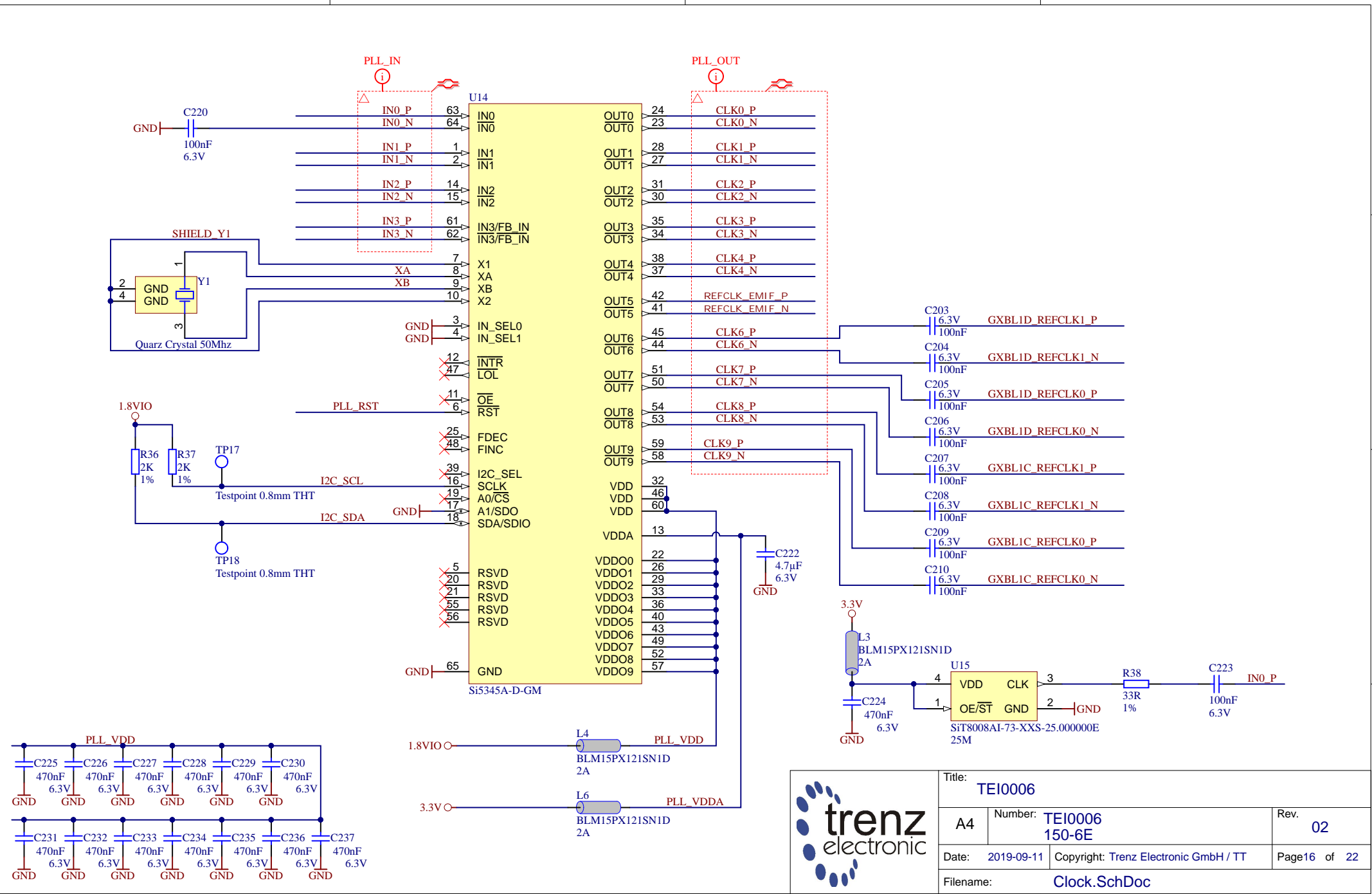
B

C

C

D

D



Title: <b>TEI0006</b>		
A4	Number: <b>TEI0006 150-6E</b>	Rev. <b>02</b>
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Filename: <b>Clock.SchDoc</b>		

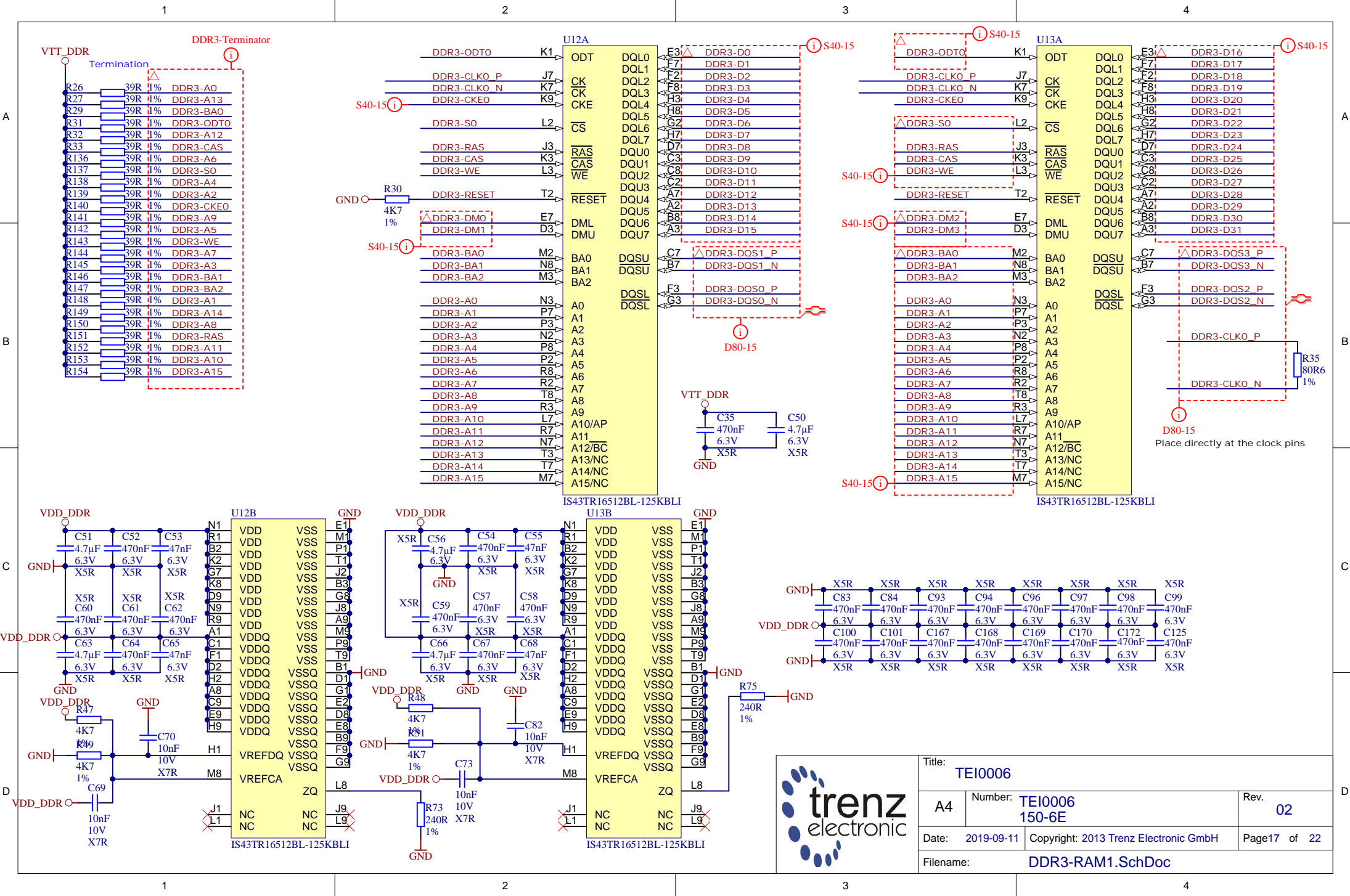
1

2

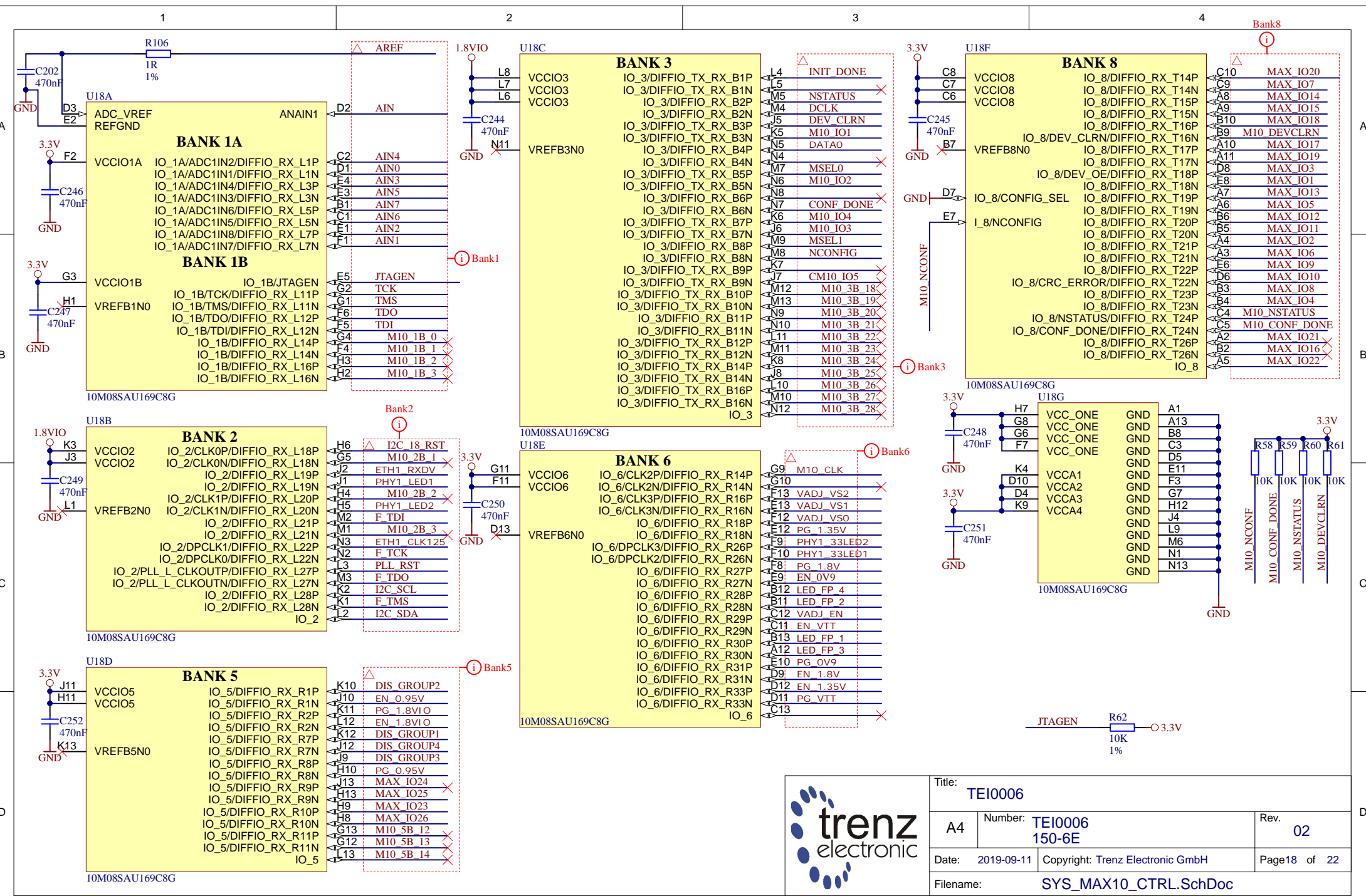
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4

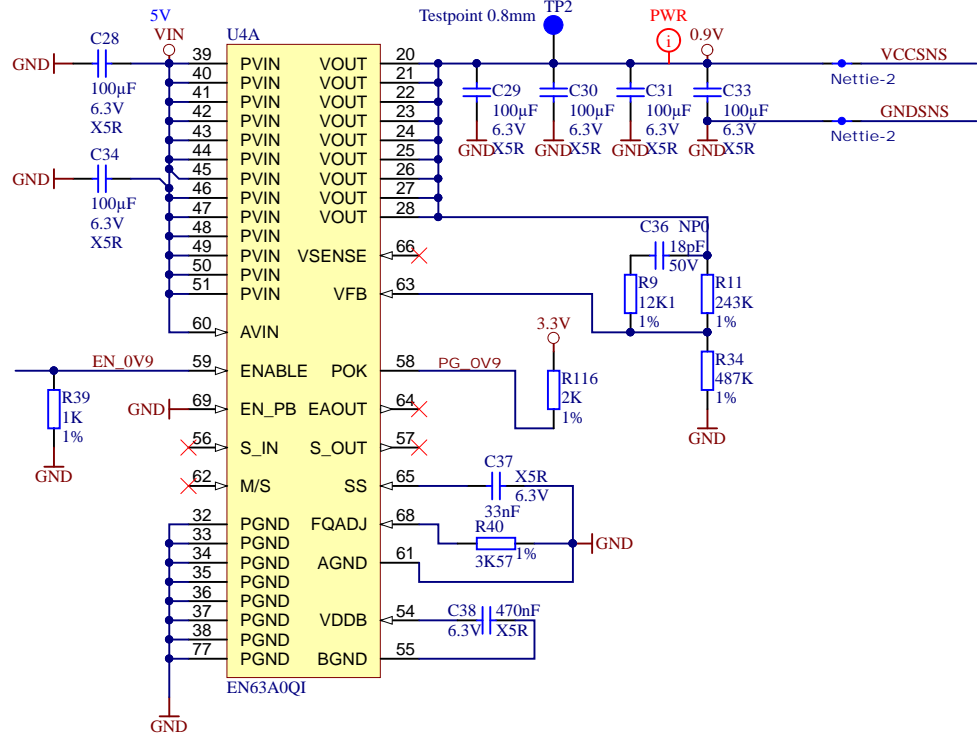




Title: TEI0006		
A4	Number: TEI0006 150-6E	Rev. 02
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Filename: DDR3-RAM1.SchDoc		



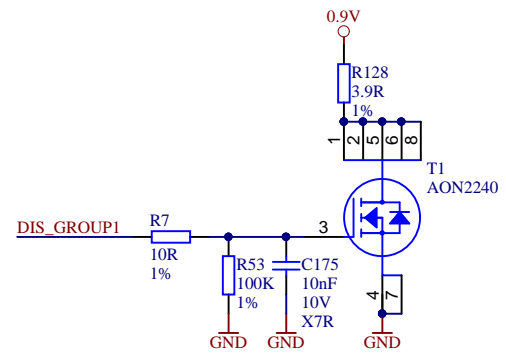
Title: <b>TEI0006</b>		
A4	Number: <b>TEI0006 150-6E</b>	Rev. <b>02</b>
Date: 2019-09-11	Copyright: Trenz Electronic GmbH	Page 18 of 22
Filename: <b>SYS_MAX10_CTRL.SchDoc</b>		



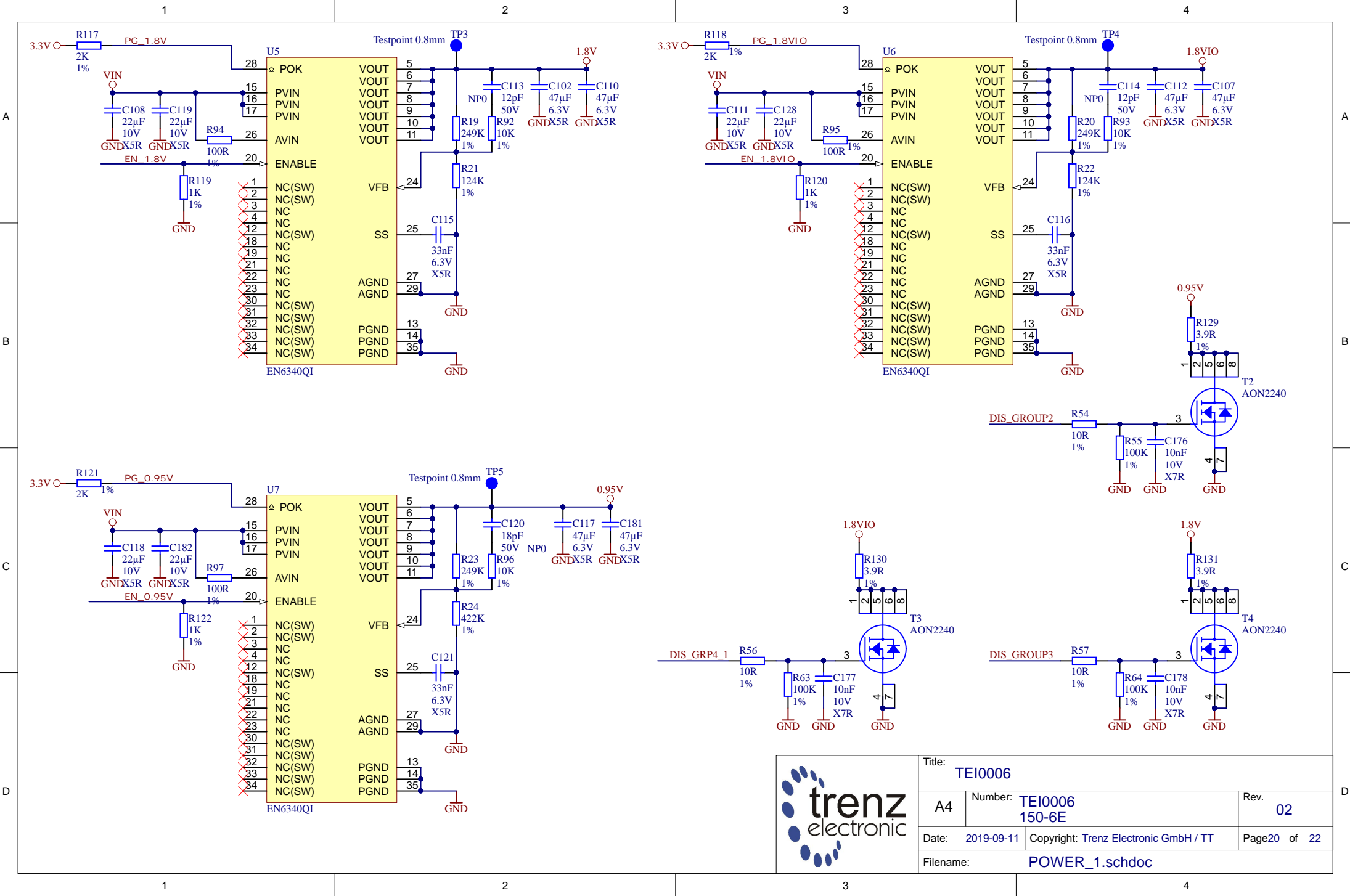
U4B

1	NC	NC	17
2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC	68
11	NC	NC(SW)	70
12	NC	NC(SW)	71
13	NC	NC	72
14	NC	NC	73
15	NC	NC	74
16	NC	NC	75
	NC	NC	76

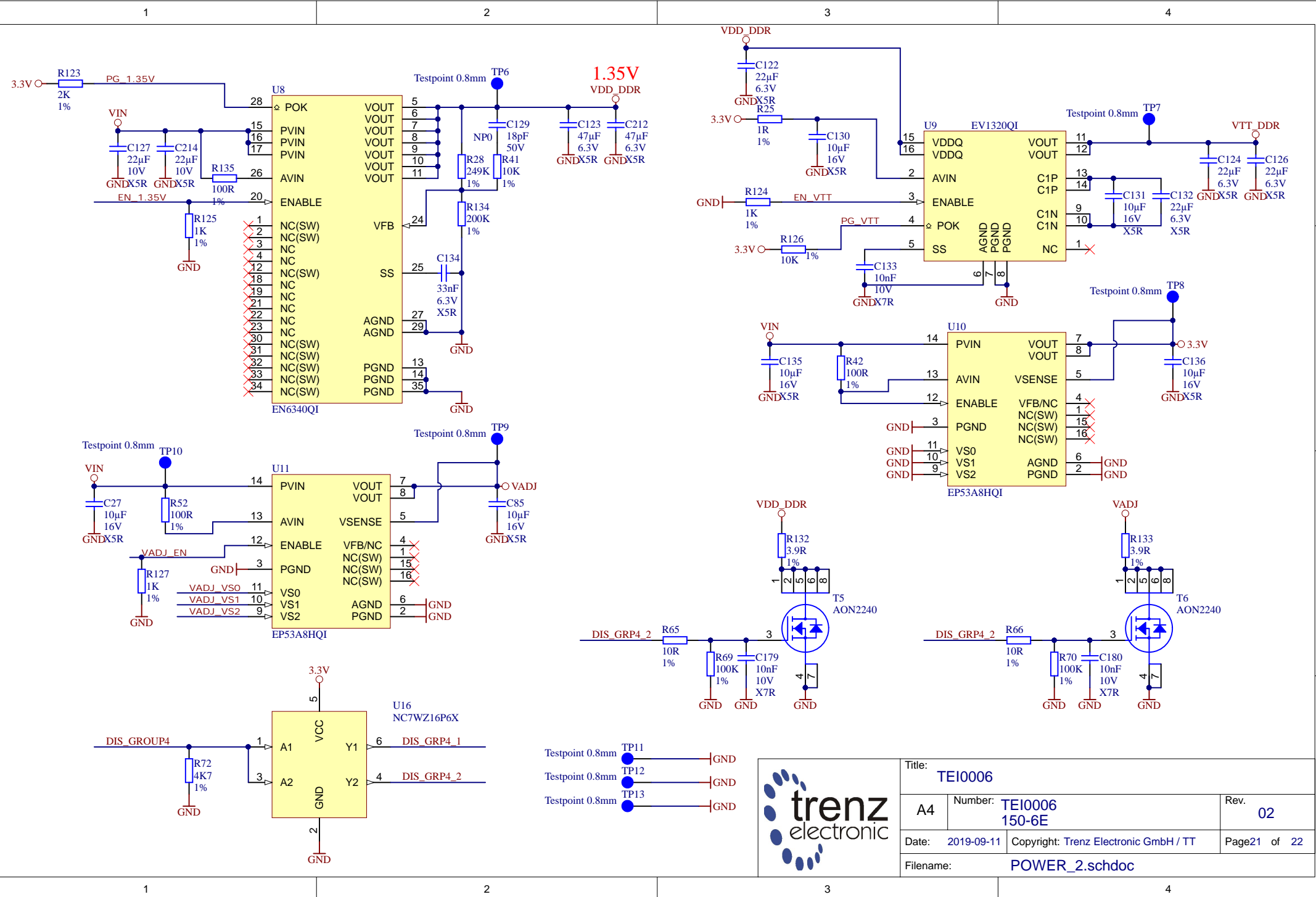
EN63A0QI



Title: TEI0006		
A4	Number: TEI0006 150-6E	Rev. 02
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Filename: PWR_CORE.SchDoc		



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- Testpoint 0.8mm TP11 — GND
- Testpoint 0.8mm TP12 — GND
- Testpoint 0.8mm TP13 — GND

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VT: Initial Rev (07.2018)

Changes from REV01 to REV02:

- 1) VT: added MEMS 100MHz clock oscillator to CLKUSR
- 2) VT: remove CLKUSR from J2
- 3) VT: replaced Si510 to SiT8008/CM3225-4pad
- 4) VT: remove DEVCLRN from J2, added pull-up
- 5) VT: remove M10\_nSTATUS from J2, added pull-up
- 6) VT: Added optional CryptoAuthentication chip U19 (DNP)

A

A

B


B

C

C

D

D

		Title: TEI0006 - Revision changes	
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