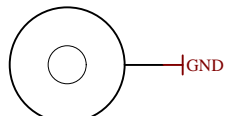
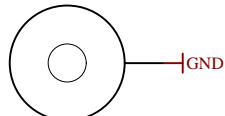


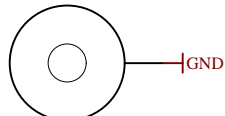
Mount.Hole 3.2mm für Unterlegscheibe



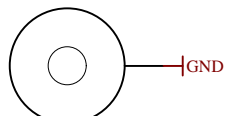
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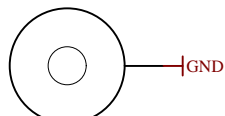
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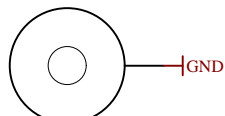
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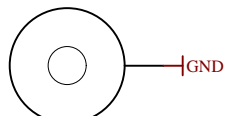
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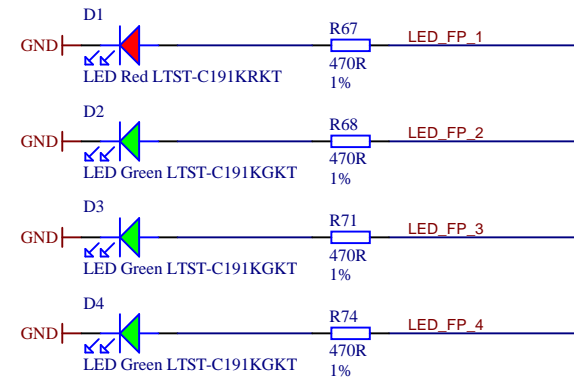
Mount.Hole 3.2mm für Unterlegscheibe



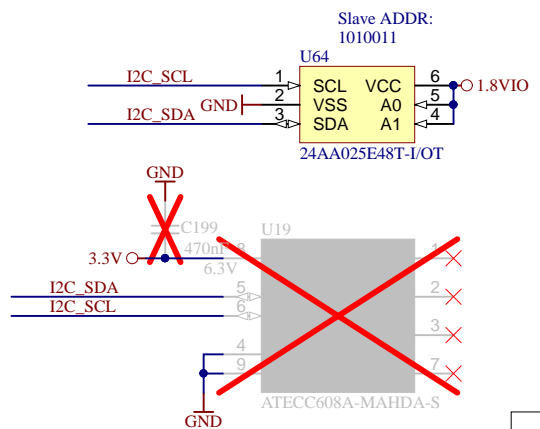
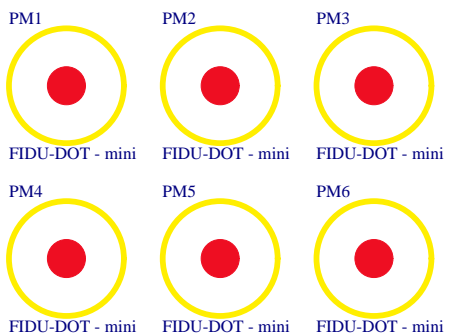
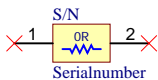
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Serial
 Serialnummer 6,3 x 6,3mm



Assembly variant	220-5I
Created by	VT
Modified by	VariantModifiedBy
Modified at	2019-09-12
SVN Revision	11740 [Locally Modified]



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Date: 2019-09-11	Copyright: Trenz Electronic GmbH / TT	Page1 of 22
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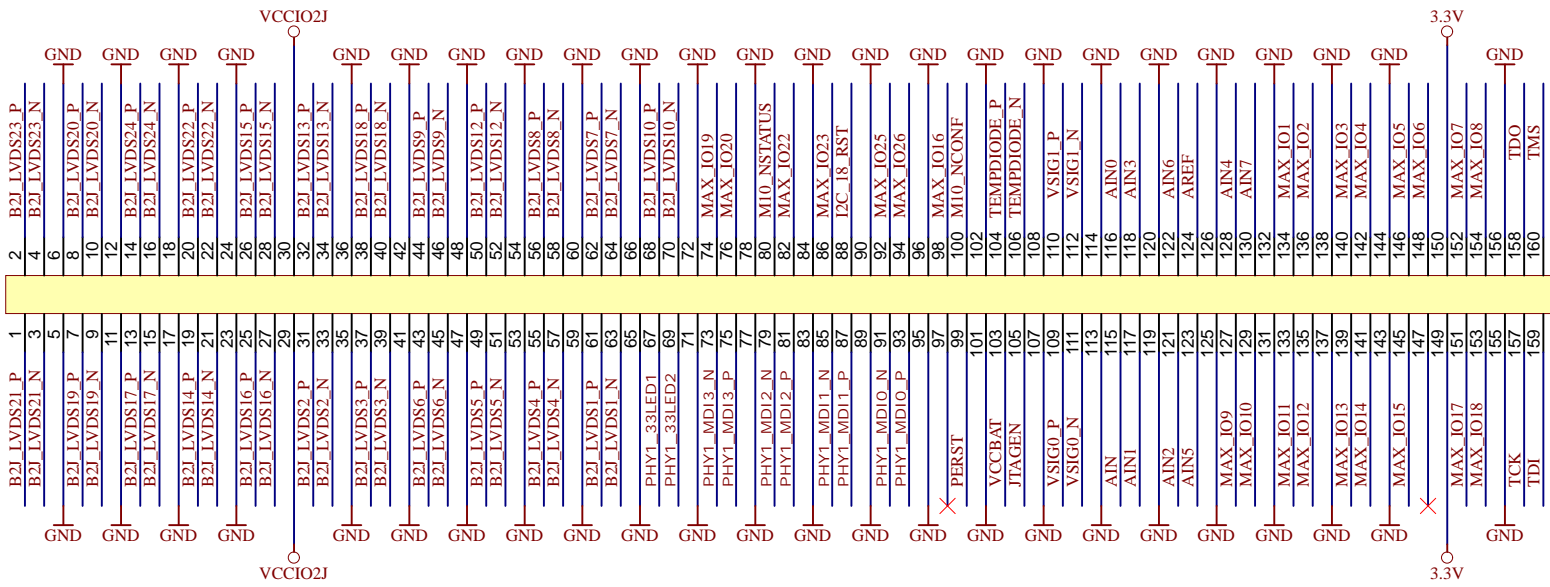
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J2
ST5-80-1.50-L-D-P-TR



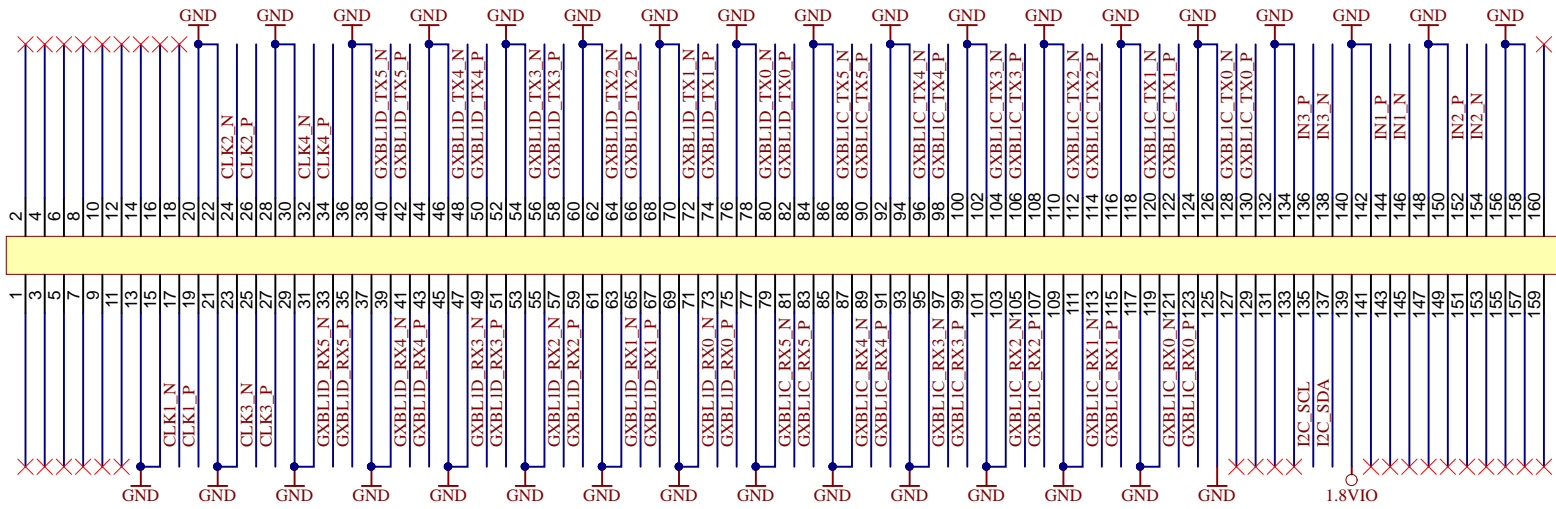
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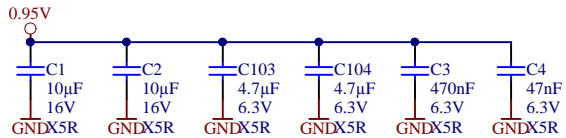


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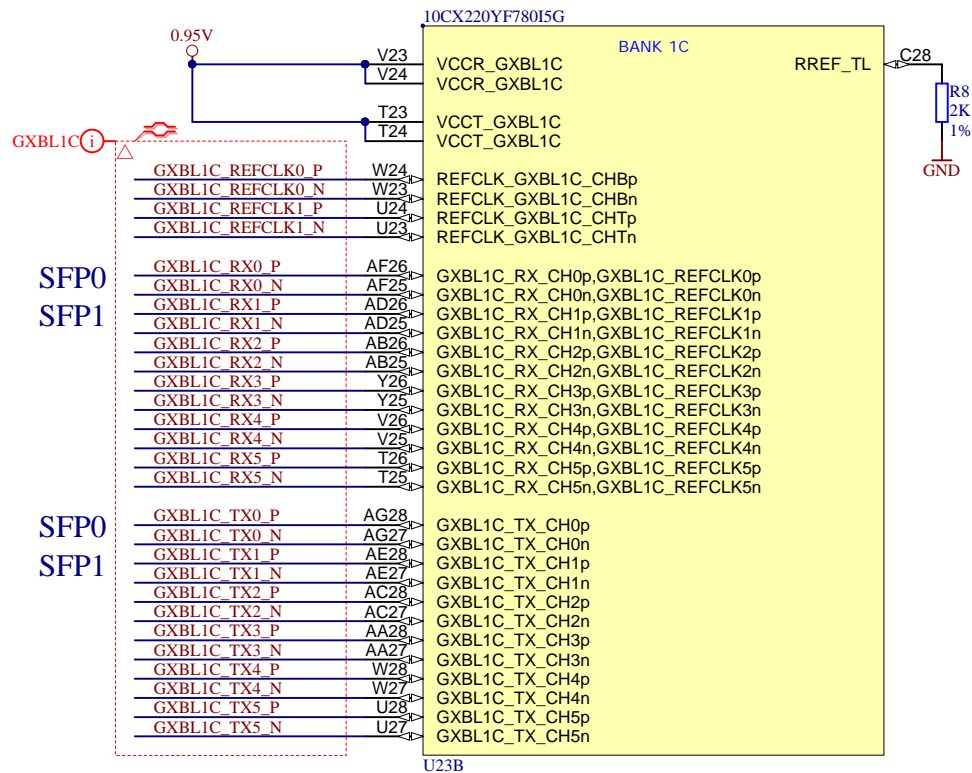
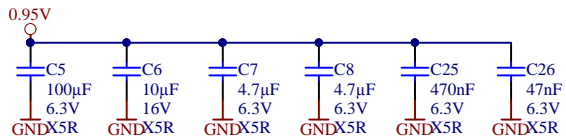


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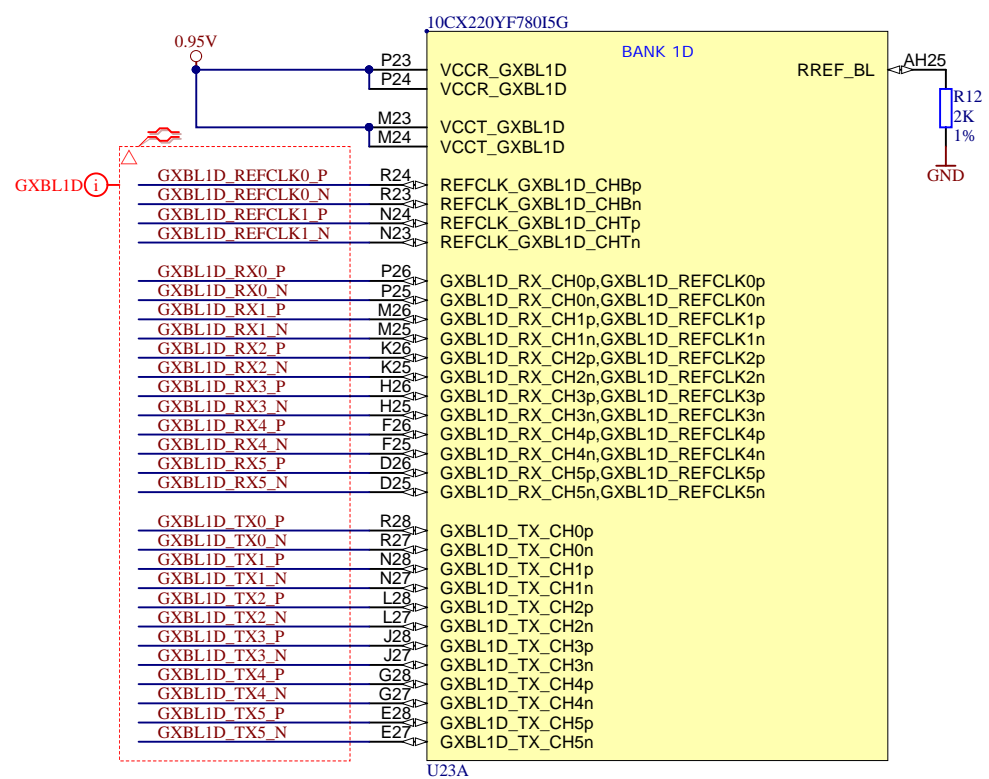
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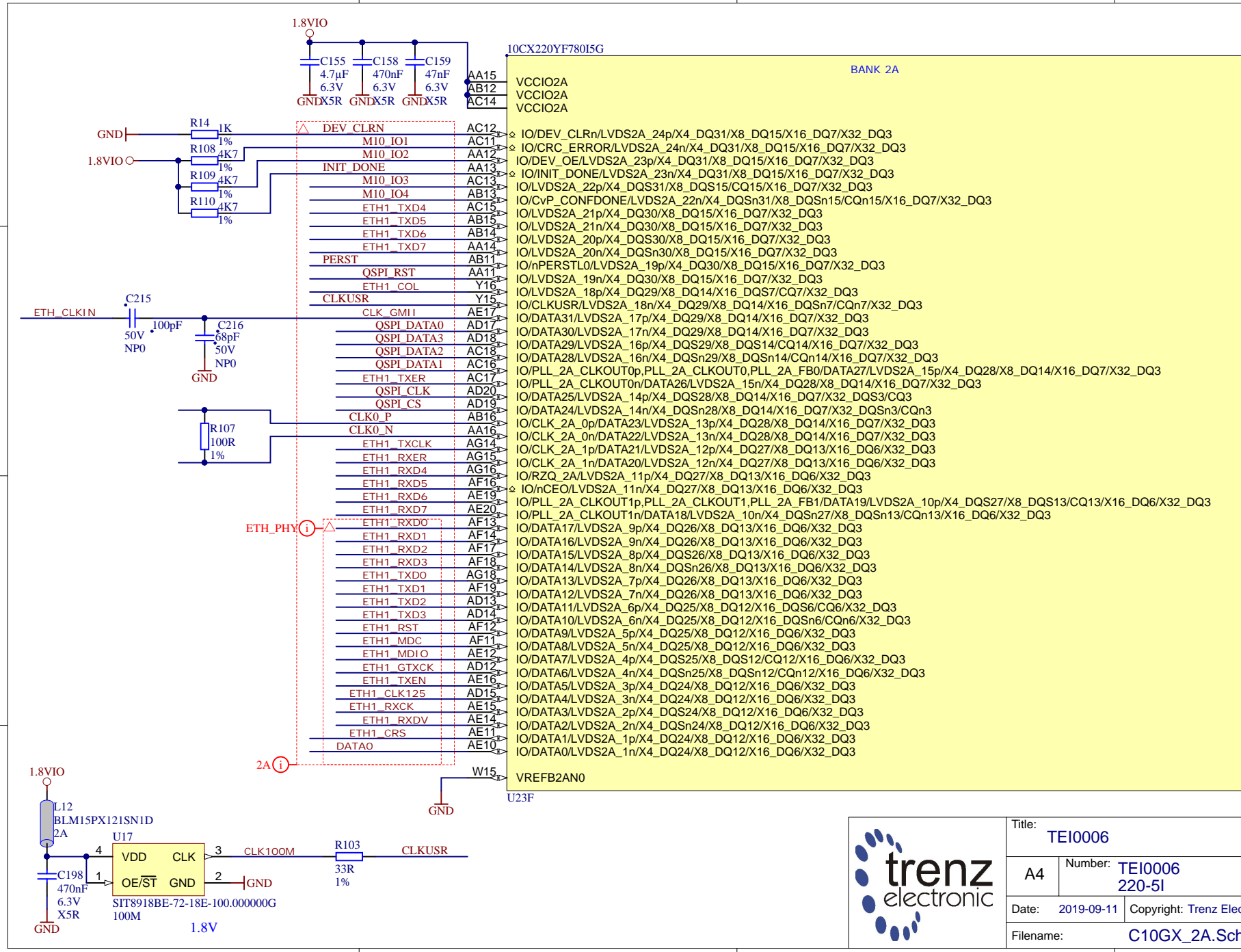
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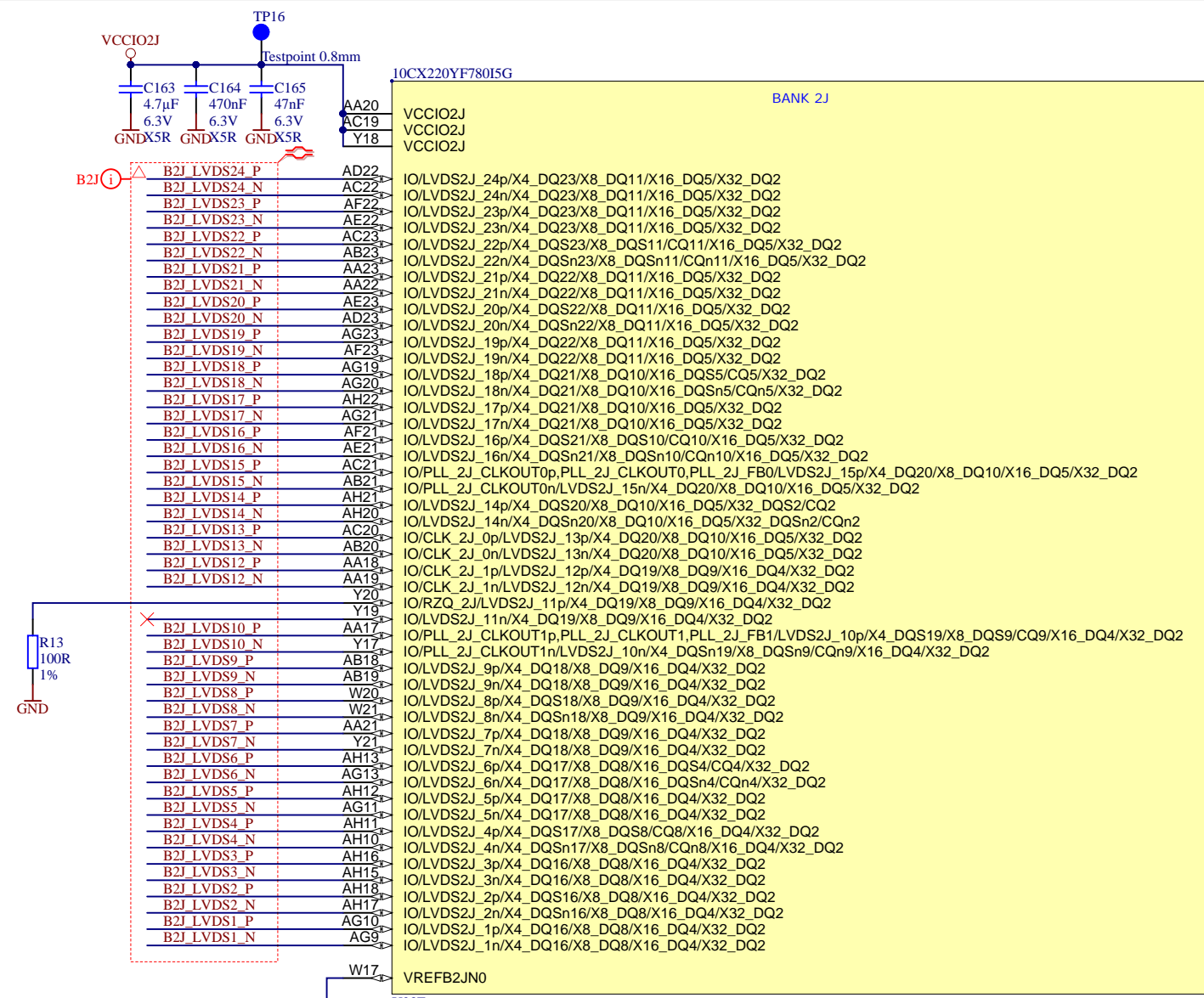
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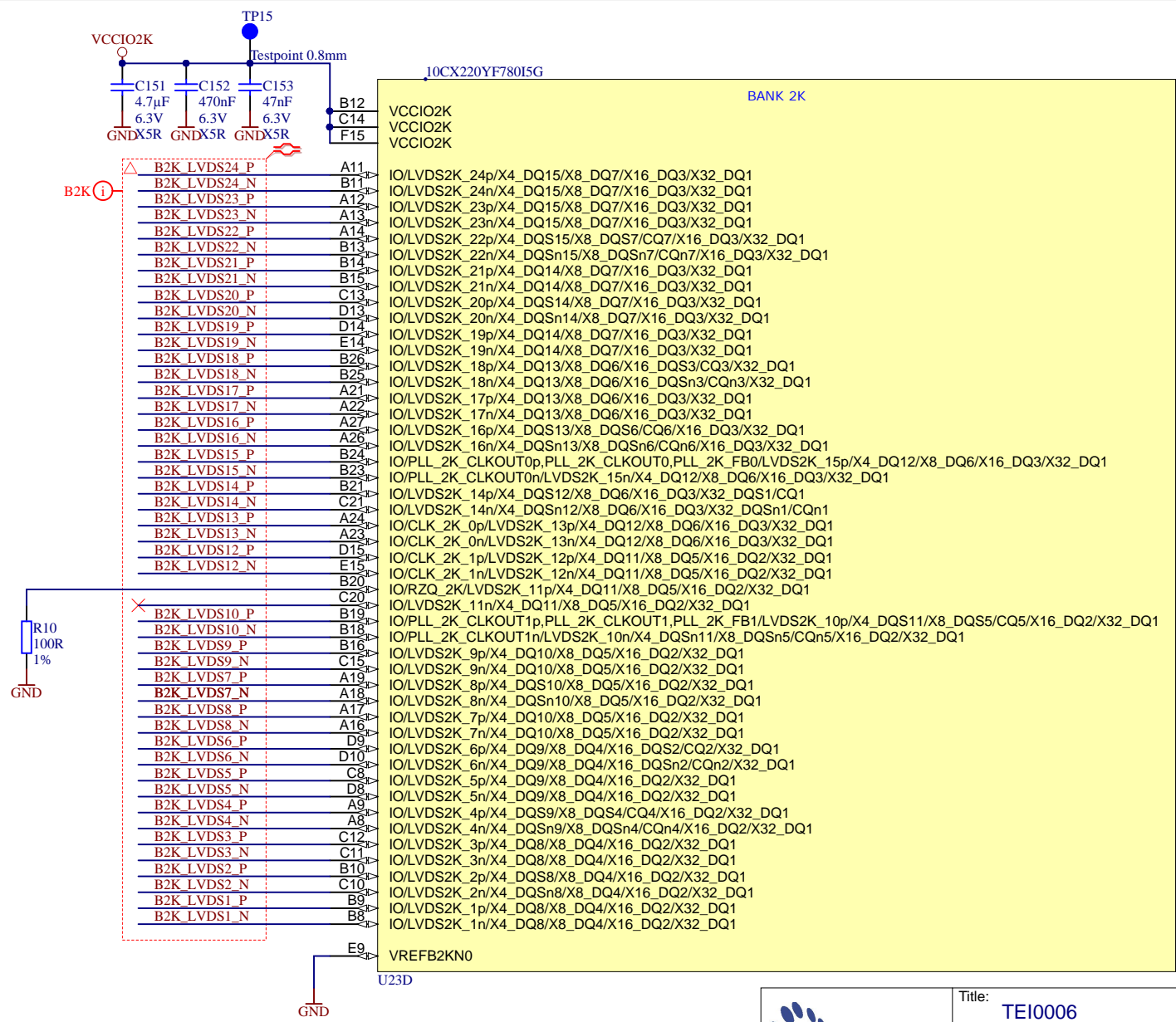
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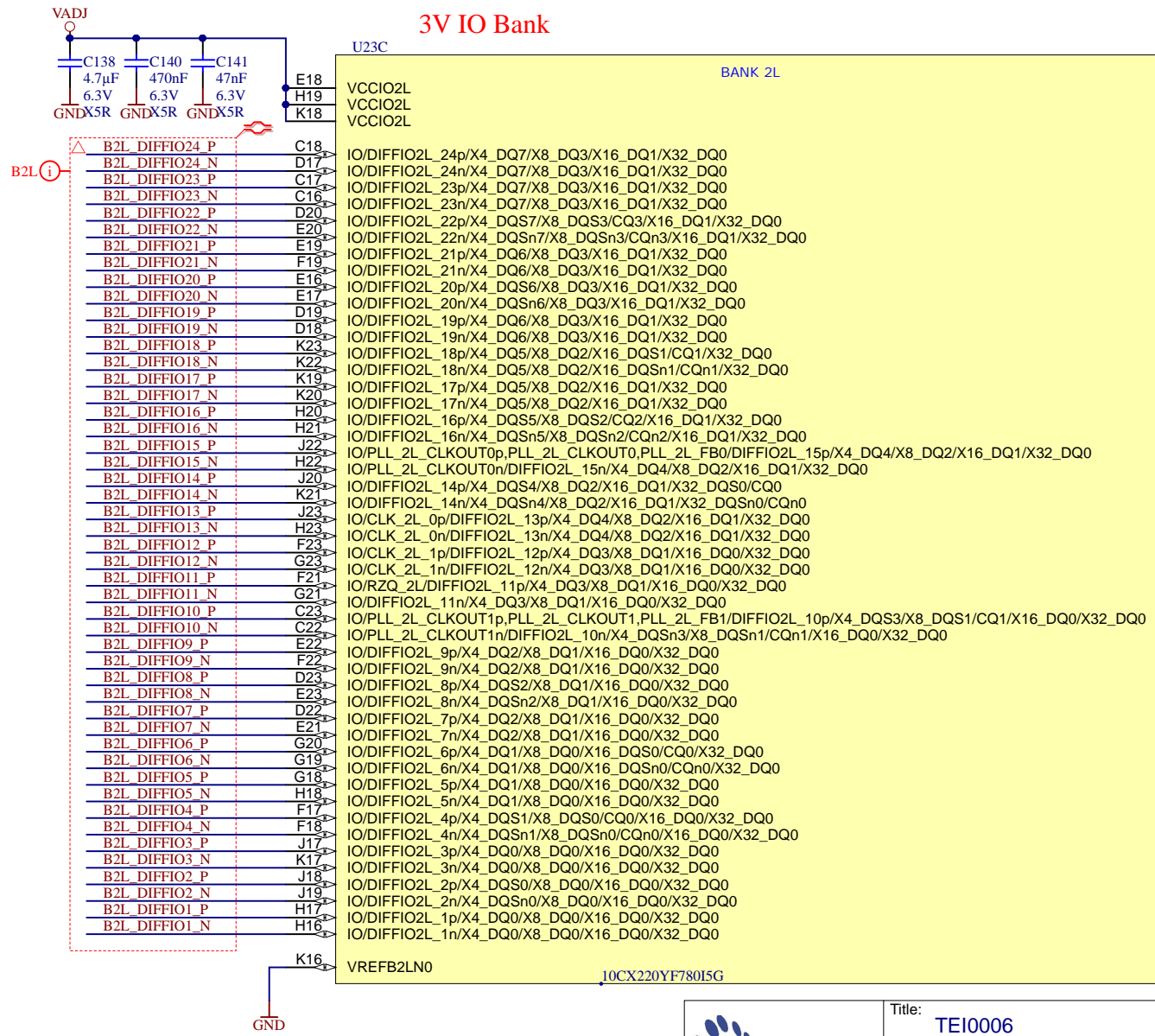
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3V IO Bank

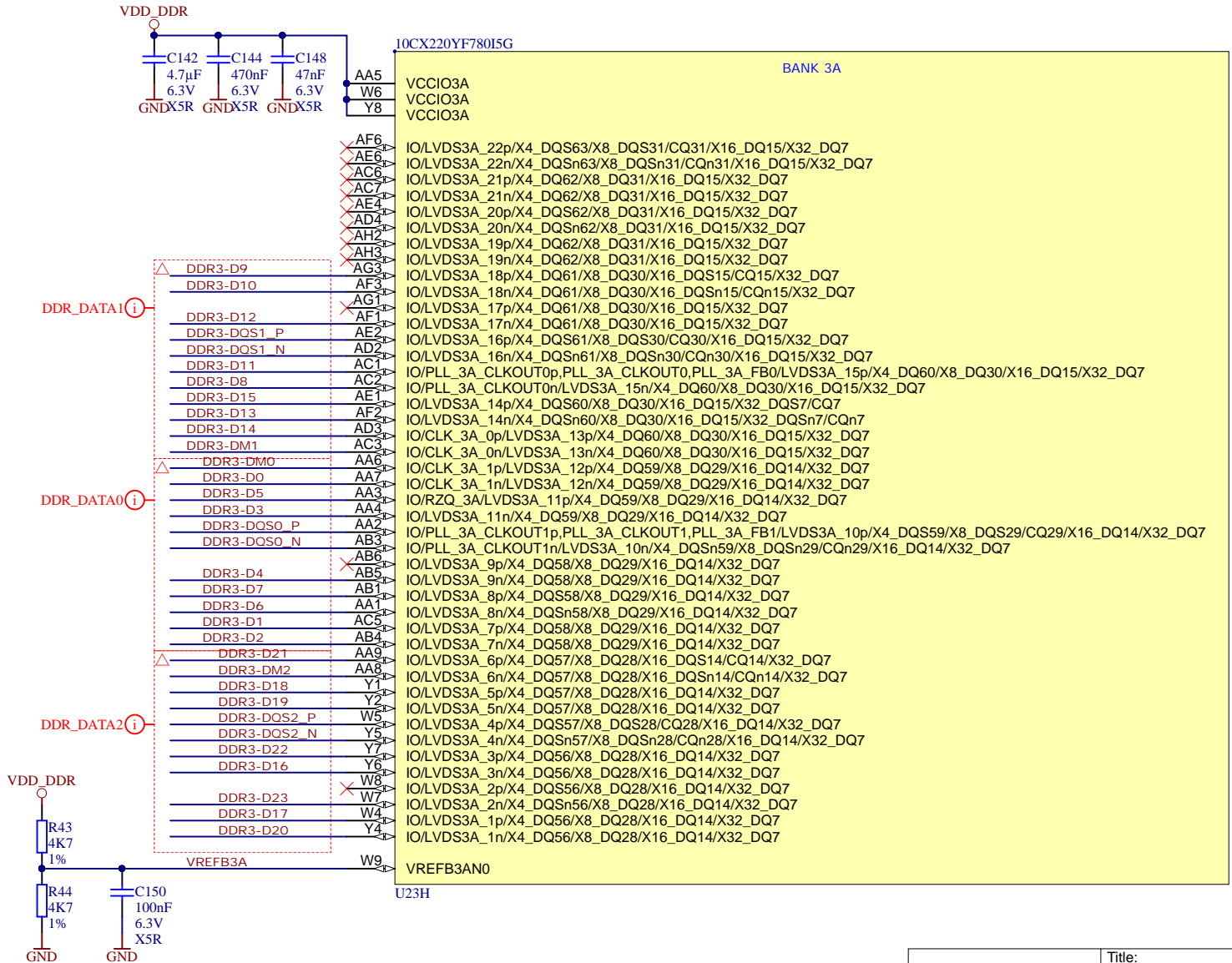
U23C

BANK 2L

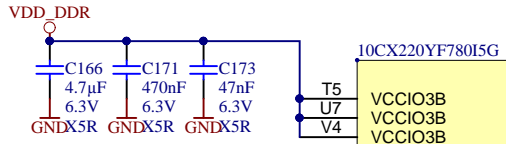
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VCCIO2L	H19	IO/DIFFIO2L_24n/X4_DQ7/X8_DQ3/X16_DQ1/X32_DQ0
VCCIO2L	K18	IO/DIFFIO2L_23p/X4_DQ7/X8_DQ3/X16_DQ1/X32_DQ0
		IO/DIFFIO2L_23n/X4_DQ7/X8_DQ3/X16_DQ1/X32_DQ0
		IO/DIFFIO2L_22p/X4_DQS7/X8_DQS3/CQ3/X16_DQ1/X32_DQ0
		IO/DIFFIO2L_22n/X4_DQSn7/X8_DQSn3/CQn3/X16_DQ1/X32_DQ0
		IO/DIFFIO2L_21p/X4_DQ6/X8_DQ3/X16_DQ1/X32_DQ0
		IO/DIFFIO2L_21n/X4_DQ6/X8_DQ3/X16_DQ1/X32_DQ0
		IO/DIFFIO2L_20p/X4_DQS6/X8_DQ3/X16_DQ1/X32_DQ0
		IO/DIFFIO2L_20n/X4_DQSn6/X8_DQ3/X16_DQ1/X32_DQ0
		IO/DIFFIO2L_19p/X4_DQ6/X8_DQ3/X16_DQ1/X32_DQ0
		IO/DIFFIO2L_19n/X4_DQ6/X8_DQ3/X16_DQ1/X32_DQ0
		IO/DIFFIO2L_18p/X4_DQ5/X8_DQ2/X16_DQS1/CQ1/X32_DQ0
		IO/DIFFIO2L_18n/X4_DQ5/X8_DQ2/X16_DQSn1/CQn1/X32_DQ0
		IO/DIFFIO2L_17p/X4_DQ5/X8_DQ2/X16_DQ1/X32_DQ0
		IO/DIFFIO2L_17n/X4_DQ5/X8_DQ2/X16_DQ1/X32_DQ0
		IO/DIFFIO2L_16p/X4_DQS5/X8_DQS2/CQ2/X16_DQ1/X32_DQ0
		IO/DIFFIO2L_16n/X4_DQSn5/X8_DQSn2/CQn2/X16_DQ1/X32_DQ0
		IO/PLL_2L_CLKOUT0p,PLL_2L_CLKOUT0,PLL_2L_FB0/DIFFIO2L_15p/X4_DQ4/X8_DQ2/X16_DQ1/X32_DQ0
		IO/PLL_2L_CLKOUT0n/DIFFIO2L_15n/X4_DQ4/X8_DQ2/X16_DQ1/X32_DQ0
		IO/DIFFIO2L_14p/X4_DQS4/X8_DQ2/X16_DQ1/X32_DQS0/CQ0
		IO/DIFFIO2L_14n/X4_DQSn4/X8_DQ2/X16_DQ1/X32_DQSn0/CQn0
		IO/CLK_2L_0p/DIFFIO2L_13p/X4_DQ4/X8_DQ2/X16_DQ1/X32_DQ0
		IO/CLK_2L_0n/DIFFIO2L_13n/X4_DQ4/X8_DQ2/X16_DQ1/X32_DQ0
		IO/CLK_2L_1p/DIFFIO2L_12p/X4_DQ3/X8_DQ1/X16_DQ0/X32_DQ0
		IO/CLK_2L_1n/DIFFIO2L_12n/X4_DQ3/X8_DQ1/X16_DQ0/X32_DQ0
		IO/RZQ_2L/DIFFIO2L_11p/X4_DQ3/X8_DQ1/X16_DQ0/X32_DQ0
		IO/DIFFIO2L_11n/X4_DQ3/X8_DQ1/X16_DQ0/X32_DQ0
		IO/PLL_2L_CLKOUT1p,PLL_2L_CLKOUT1,PLL_2L_FB1/DIFFIO2L_10p/X4_DQS3/X8_DQS1/CQ1/X16_DQ0/X32_DQ0
		IO/PLL_2L_CLKOUT1n/DIFFIO2L_10n/X4_DQSn3/X8_DQSn1/CQn1/X16_DQ0/X32_DQ0
		IO/DIFFIO2L_9p/X4_DQ2/X8_DQ1/X16_DQ0/X32_DQ0
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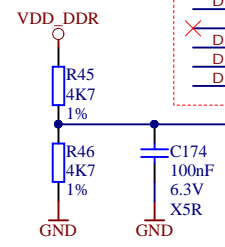
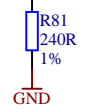
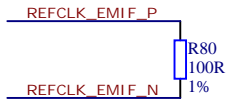
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10CX220YF78015G

BANK 3B

VCCIO3B	VCCIO3B	VCCIO3B
IO/LVDS3B_24p/X4_DQ55/X8_DQ27/X16_DQ13/X32_DQ6	W3	DDR3-WE
IO/LVDS3B_24n/X4_DQ55/X8_DQ27/X16_DQ13/X32_DQ6	V3	DDR3-RESET
IO/LVDS3B_23p/X4_DQ55/X8_DQ27/X16_DQ13/X32_DQ6	W2	DDR3-SO
IO/LVDS3B_23n/X4_DQ55/X8_DQ27/X16_DQ13/X32_DQ6	V2	DDR3-S1
IO/LVDS3B_22p/X4_DQS55/X8_DQS27/CQ27/X16_DQ13/X32_DQ6	V5	DDR3-ODT0
IO/LVDS3B_22n/X4_DQS55/X8_DQS27/CQ27/X16_DQ13/X32_DQ6	V6	DDR3-ODT1
IO/LVDS3B_21p/X4_DQ54/X8_DQ27/X16_DQ13/X32_DQ6	U6	DDR3-CKE0
IO/LVDS3B_21n/X4_DQ54/X8_DQ27/X16_DQ13/X32_DQ6	V7	DDR3-CKE1
IO/LVDS3B_20p/X4_DQS54/X8_DQ27/X16_DQ13/X32_DQ6	V1	DDR3-CKO_P
IO/LVDS3B_20n/X4_DQSn54/X8_DQ27/X16_DQ13/X32_DQ6	U1	DDR3-CKO_N
IO/LVDS3B_19p/X4_DQ54/X8_DQ27/X16_DQ13/X32_DQ6	U3	
IO/LVDS3B_19n/X4_DQ54/X8_DQ27/X16_DQ13/X32_DQ6	U4	
IO/LVDS3B_18p/X4_DQ53/X8_DQ26/X16_DQS13/CQ13/X32_DQ6	T1	DDR3-A0
IO/LVDS3B_18n/X4_DQ53/X8_DQ26/X16_DQSn13/CQn13/X32_DQ6	R1	DDR3-A1
IO/LVDS3B_17p/X4_DQ53/X8_DQ26/X16_DQ13/X32_DQ6	L1	DDR3-A2
IO/LVDS3B_17n/X4_DQ53/X8_DQ26/X16_DQ13/X32_DQ6	K1	DDR3-A3
IO/LVDS3B_16p/X4_DQS53/X8_DQS26/CQ26/X16_DQ13/X32_DQ6	T2	DDR3-A4
IO/LVDS3B_16n/X4_DQSn53/X8_DQSn26/CQn26/X16_DQ13/X32_DQ6	T3	DDR3-A5
IO/PLL_3B_CLKOUT0p,PLL_3B_CLKOUT0,PLL_3B_FB0/LVDS3B_15p/X4_DQ52/X8_DQ26/X16_DQ13/X32_DQ6	R2	DDR3-A6
IO/LVDS3B_14p/X4_DQS52/X8_DQ26/X16_DQ13/X32_DQS6/CQ6	P2	DDR3-A7
IO/LVDS3B_14n/X4_DQSn52/X8_DQ26/X16_DQ13/X32_DQS6/CQn6	H1	DDR3-A8
IO/CLK_3B_0p/LVDS3B_13p/X4_DQ52/X8_DQ26/X16_DQ13/X32_DQ6	G1	DDR3-A9
IO/CLK_3B_0n/LVDS3B_13n/X4_DQ52/X8_DQ26/X16_DQ13/X32_DQ6	N1	DDR3-A10
IO/CLK_3B_1p/LVDS3B_12p/X4_DQ51/X8_DQ25/X16_DQ12/X32_DQ6	M1	DDR3-A11
IO/CLK_3B_1n/LVDS3B_12n/X4_DQ51/X8_DQ25/X16_DQ12/X32_DQ6	L3	REFCLK_EMIF_P
IO/RZQ_3B/LVDS3B_11p/X4_DQ51/X8_DQ25/X16_DQ12/X32_DQ6	K2	REFCLK_EMIF_N
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IO/PLL_3B_CLKOUT1p,PLL_3B_CLKOUT1,PLL_3B_FB1/LVDS3B_10p/X4_DQS51/X8_DQS25/CQ25/X16_DQ12/X32_DQ6	H2	DDR3-A13
IO/PLL_3B_CLKOUT1n/LVDS3B_10n/X4_DQSn51/X8_DQSn25/CQn25/X16_DQ12/X32_DQ6	J3	DDR3-A14
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IO/LVDS3B_7p/X4_DQ50/X8_DQ25/X16_DQ12/X32_DQ6	M3	DDR3-BA1
IO/LVDS3B_7n/X4_DQ50/X8_DQ25/X16_DQ12/X32_DQ6	M4	DDR3-BA2
IO/LVDS3B_6p/X4_DQ49/X8_DQ24/X16_DQS12/CQ12/X32_DQ6	U8	DDR3-DM3
IO/LVDS3B_6n/X4_DQ49/X8_DQ24/X16_DQSn12/CQn12/X32_DQ6	V8	DDR3-D30
IO/LVDS3B_5p/X4_DQ49/X8_DQ24/X16_DQ12/X32_DQ6	T4	DDR3-D24
IO/LVDS3B_5n/X4_DQ49/X8_DQ24/X16_DQ12/X32_DQ6	U5	DDR3-D28
IO/LVDS3B_4p/X4_DQS49/X8_DQS24/CQ24/X16_DQ12/X32_DQ6	R4	DDR3-DQS3_P
IO/LVDS3B_4n/X4_DQSn49/X8_DQSn24/CQn24/X16_DQ12/X32_DQ6	R5	DDR3-DQS3_N
IO/LVDS3B_3p/X4_DQ48/X8_DQ24/X16_DQ12/X32_DQ6	T7	DDR3-D26
IO/LVDS3B_3n/X4_DQ48/X8_DQ24/X16_DQ12/X32_DQ6	T8	DDR3-D25
IO/LVDS3B_2p/X4_DQS48/X8_DQ24/X16_DQ12/X32_DQ6	T9	DDR3-D31
IO/LVDS3B_2n/X4_DQSn48/X8_DQ24/X16_DQ12/X32_DQ6	P3	DDR3-D29
IO/LVDS3B_1p/X4_DQ48/X8_DQ24/X16_DQ12/X32_DQ6	P4	DDR3-D27
IO/LVDS3B_1n/X4_DQ48/X8_DQ24/X16_DQ12/X32_DQ6	P4	



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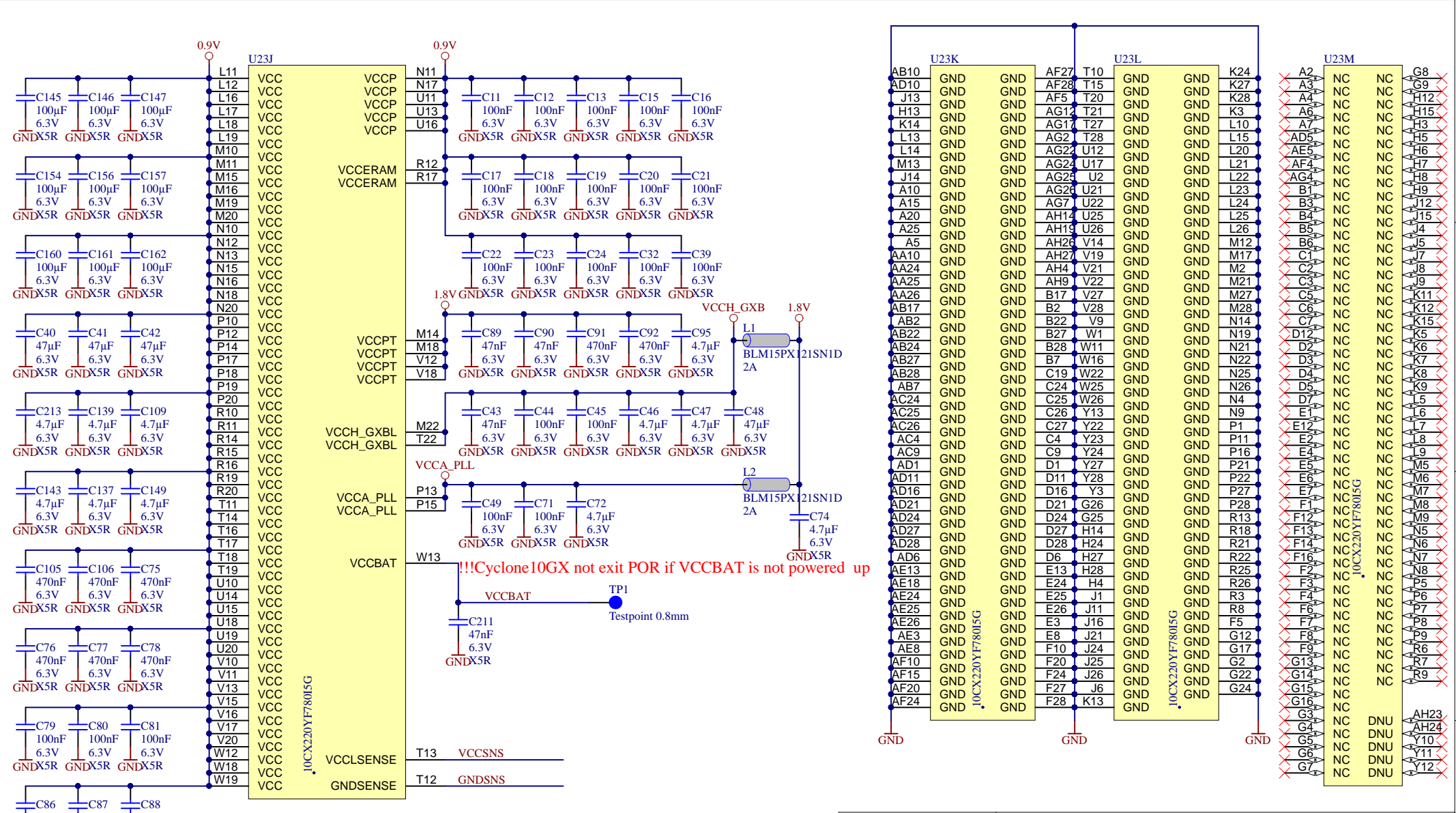
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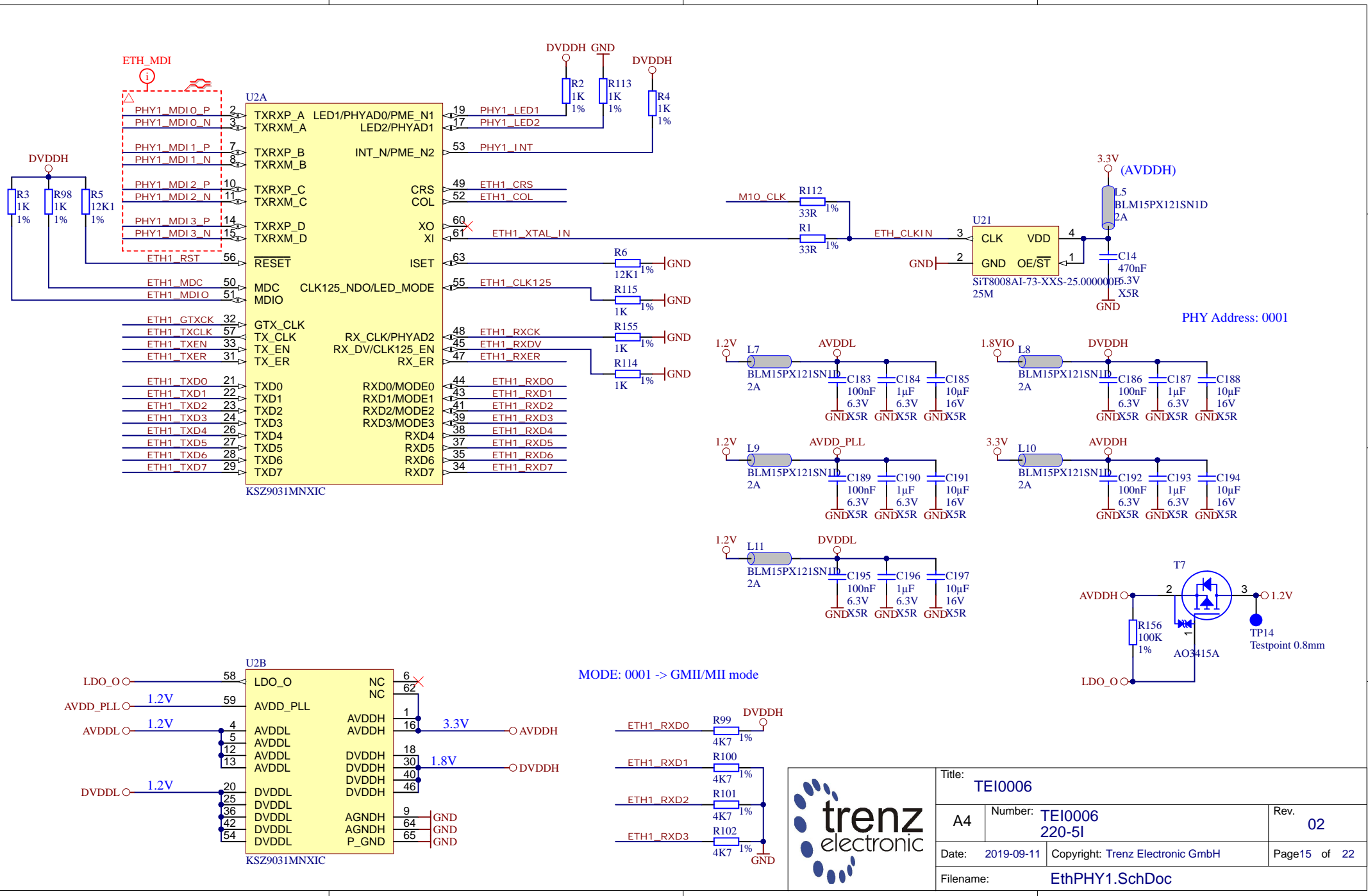
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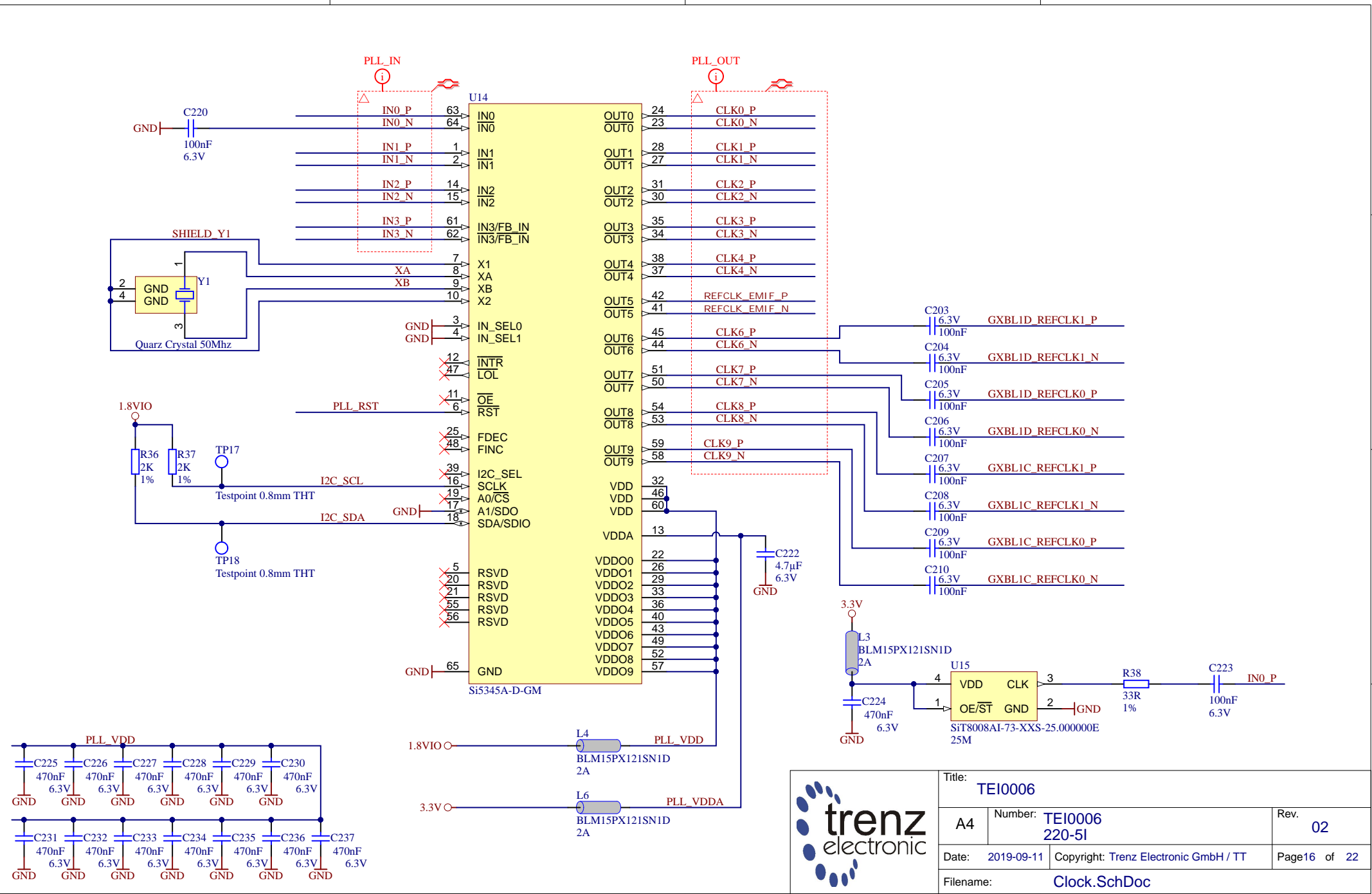
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Title: TEI0006		
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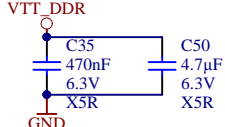
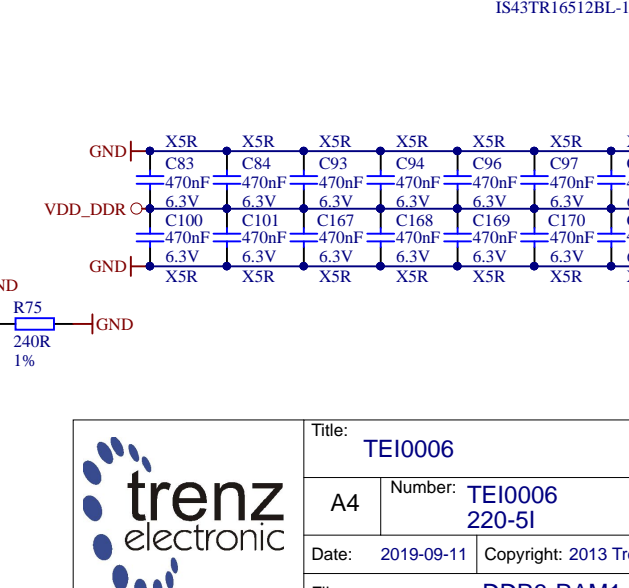
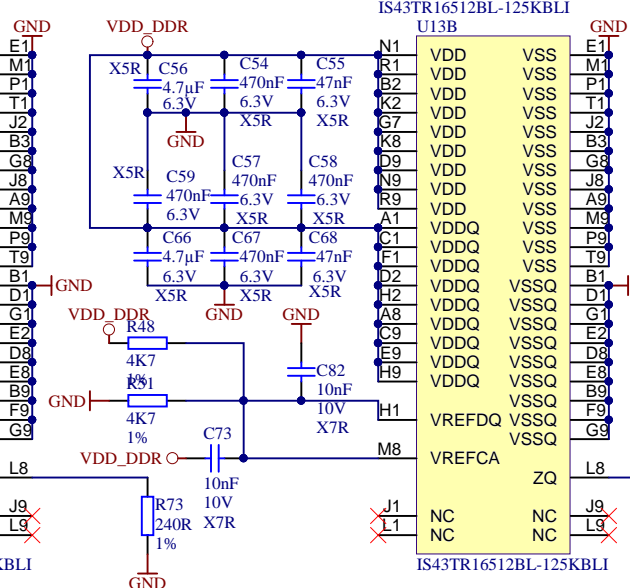
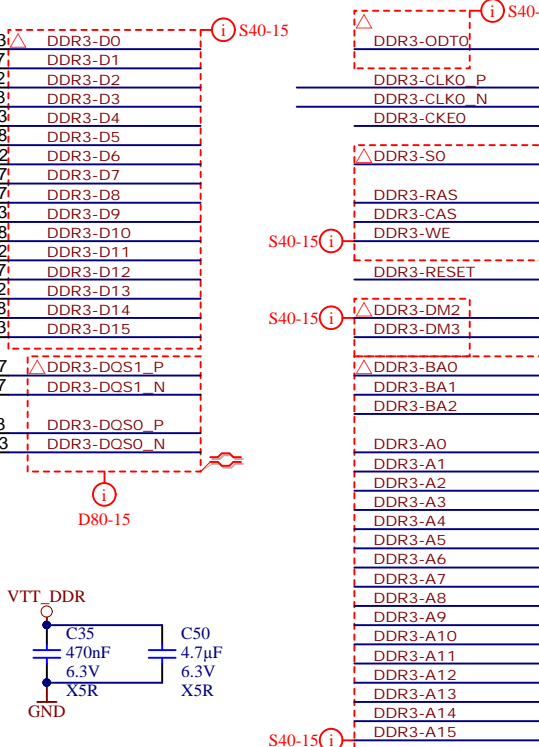
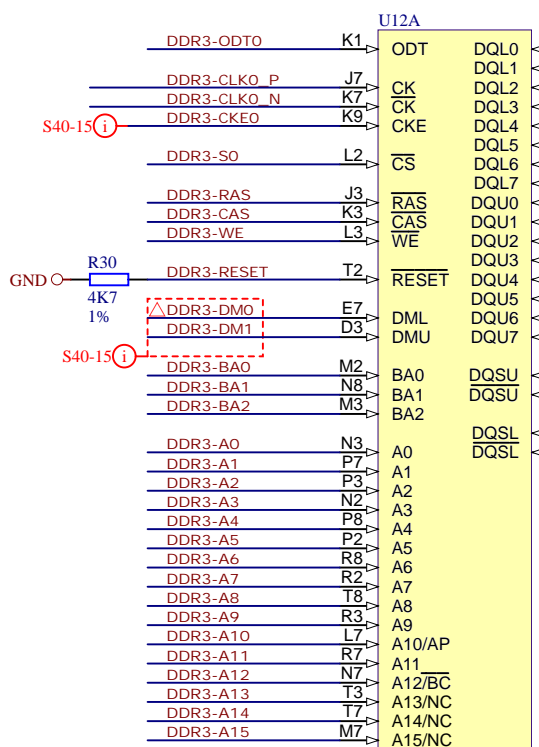
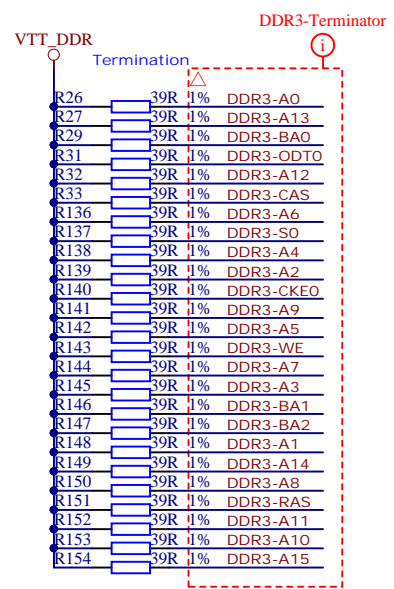
D

A

B

C

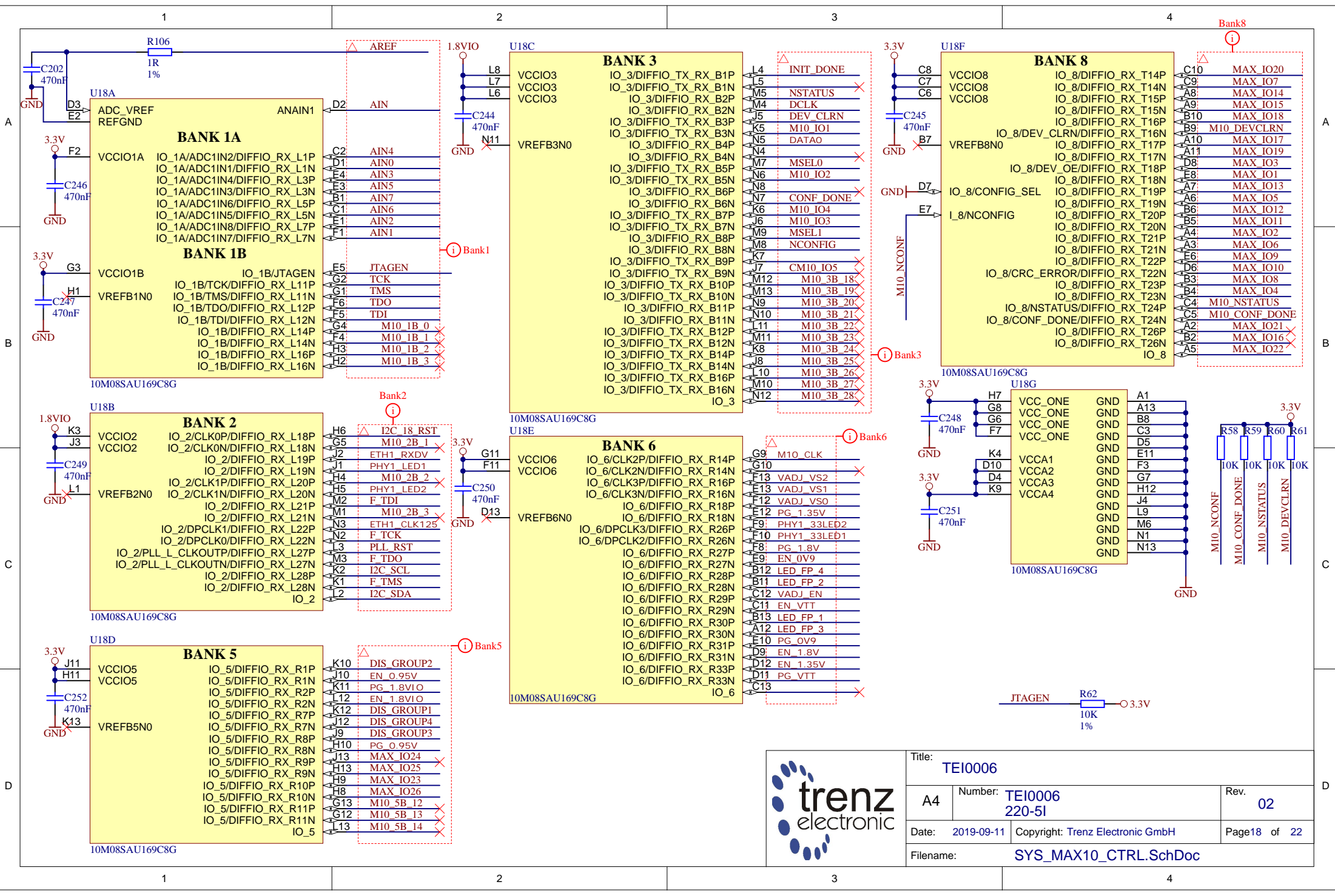
D



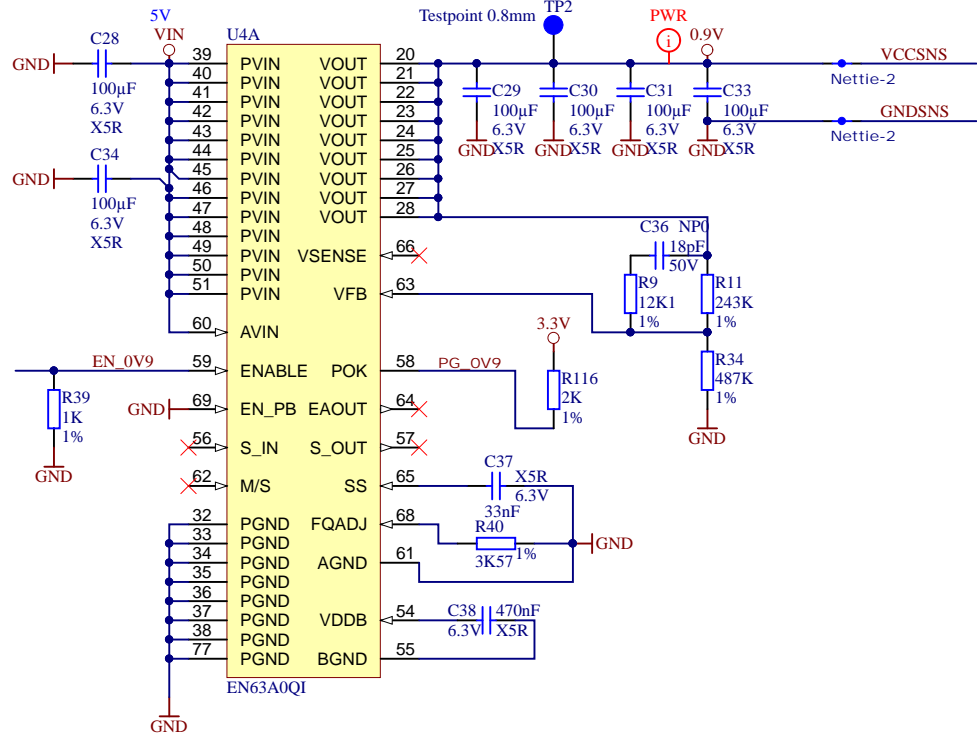
Place directly at the clock pins



Title: TEI0006		
A4	Number: TEI0006 220-51	Rev. 02
Date: 2019-09-11	Copyright: 2013 Trenz Electronic GmbH	Page 17 of 22
Filename: DDR3-RAM1.SchDoc		



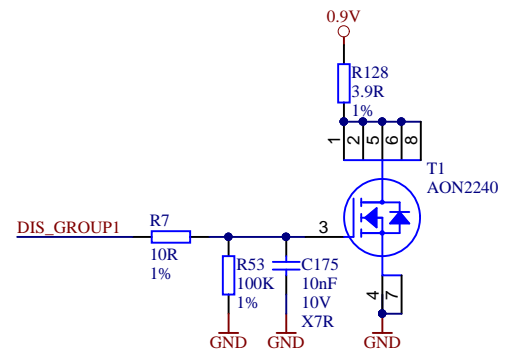
Title: TEI0006		
A4	Number: TEI0006 220-51	Rev. 02
Date: 2019-09-11	Copyright: Trenz Electronic GmbH	Page 18 of 22
Filename: SYS_MAX10_CTRL.SchDoc		



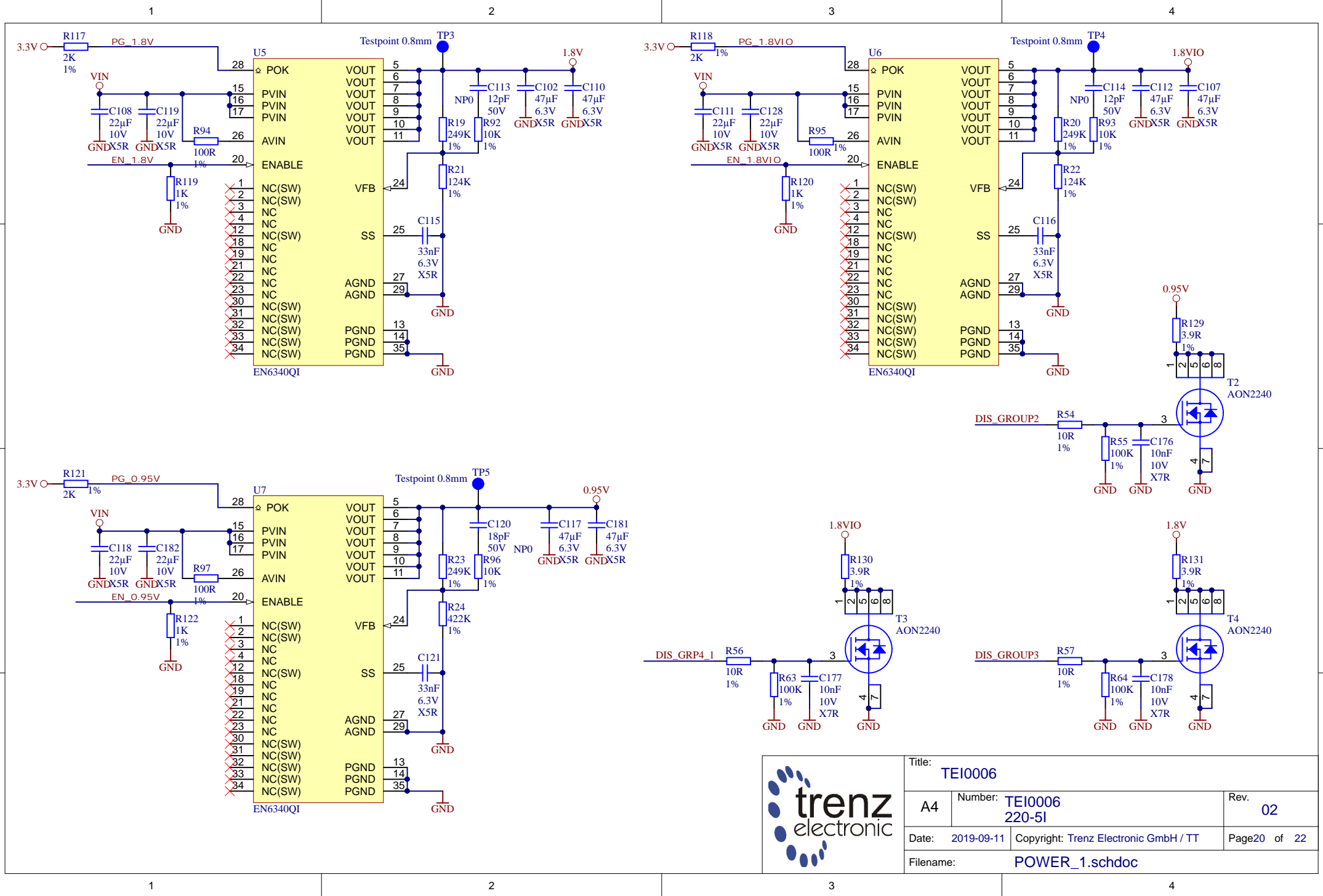
U4B

1	NC	NC	17
2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC	67
11	NC	NC(SW)	70
12	NC	NC(SW)	71
13	NC	NC	72
14	NC	NC	73
15	NC	NC	74
16	NC	NC	75
	NC	NC	76

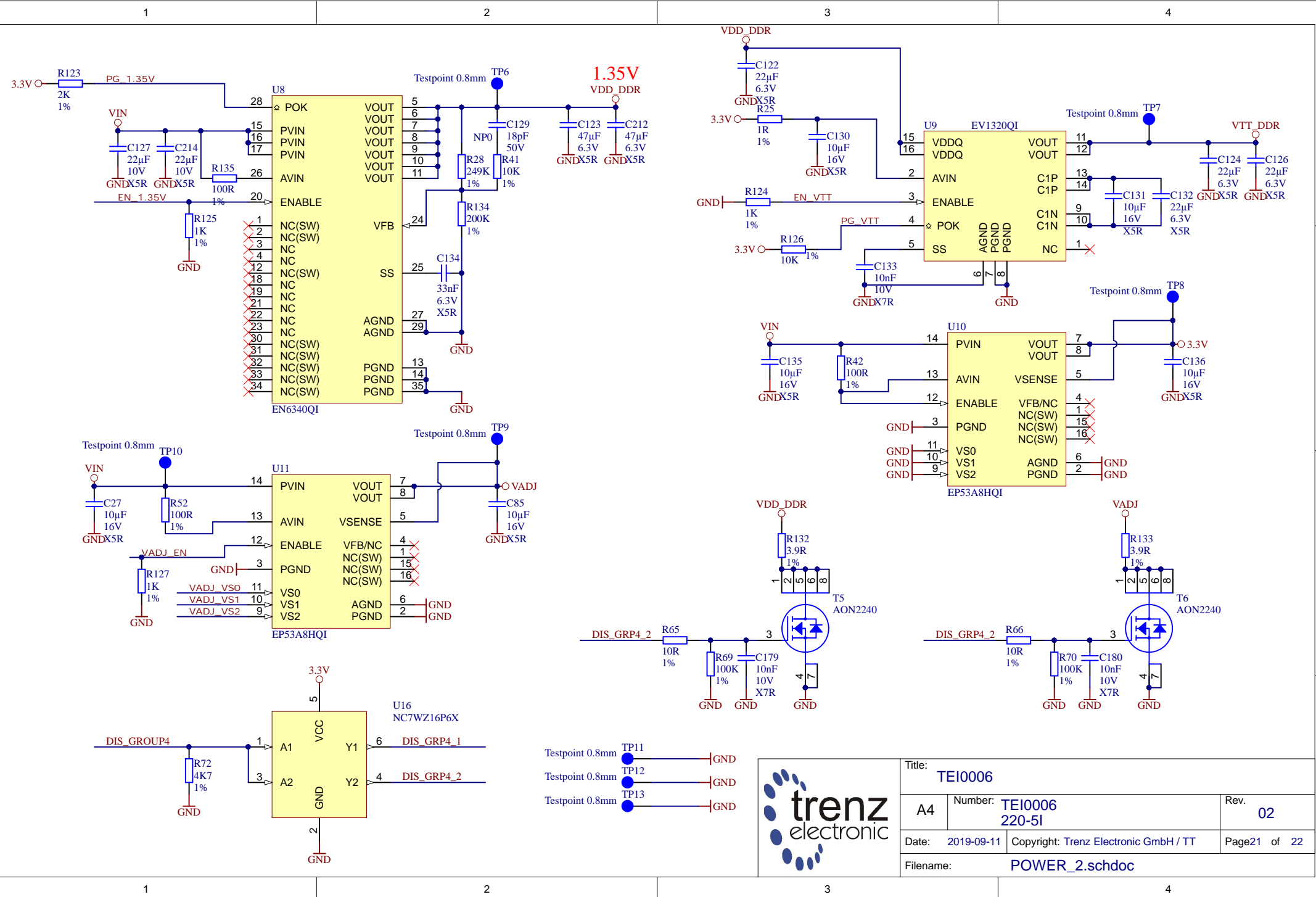
EN63A0QI



Title: TEI0006		
A4	Number: TEI0006 220-5I	Rev. 02
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Filename: PWR_CORE.SchDoc		



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A4	Number: TEI0006 220-51	Rev. 02
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Title: TEI0006		
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Filename: POWER_2.schdoc		

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VT: Initial Rev (07.2018)

Changes from REV01 to REV02:

- 1) VT: added MEMS 100MHz clock oscillator to CLKUSR
- 2) VT: remove CLKUSR from J2
- 3) VT: replaced Si510 to SiT8008/CM3225-4pad
- 4) VT: remove DEVCLRN from J2, added pull-up
- 5) VT: remove M10_nSTATUS from J2, added pull-up
- 6) VT: Added optional CryptoAuthentication chip U19 (DNP)

A

A

B


B

C

C

D

D

	Title: TEI0006 - Revision changes		
	A4	Number: TEI0006 220-5I	Rev. 02
	Date: 2019-09-11	Copyright: Trenz Electronic GmbH	Page 22 of 22
	Filename: Revision_Changes.SchDoc		

1

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