
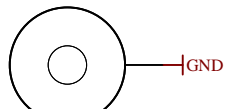


Regarding the usage of our schematics and alike documentation for Trenz module TEI0006.

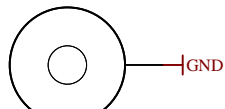
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Schematics and other handouts serve for informational purposes only!

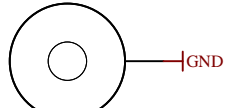
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	A4	Number: <b>TEI0006 220-5E</b>	Rev. <b>03</b>
	Date: <b>2020-08-31</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>1</b> of <b>23</b>
	Filename: <b>Legal Notices Modules.SchDoc</b>		



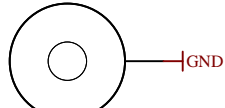
Mount.Hole 3.2mm für Unterlegscheibe



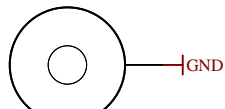
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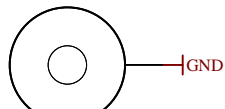
Mount.Hole 3.2mm für Unterlegscheibe



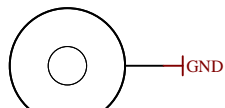
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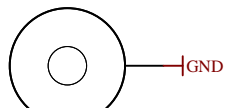
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe

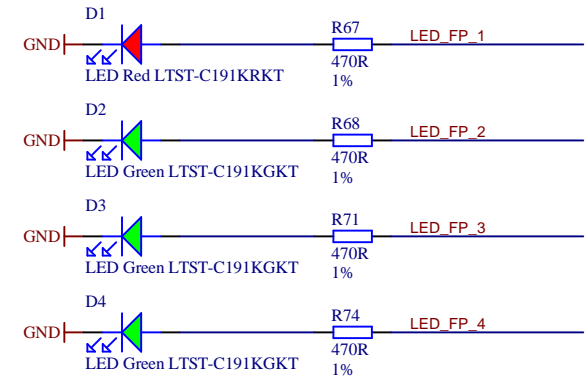
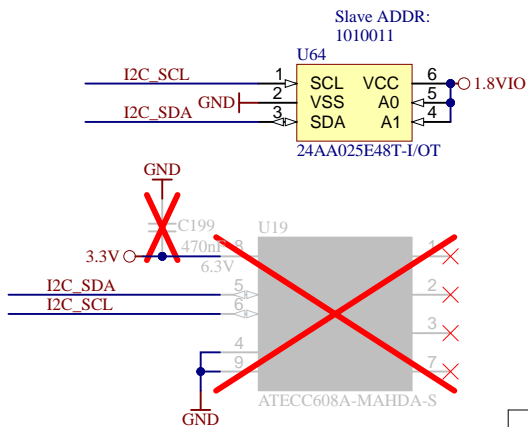
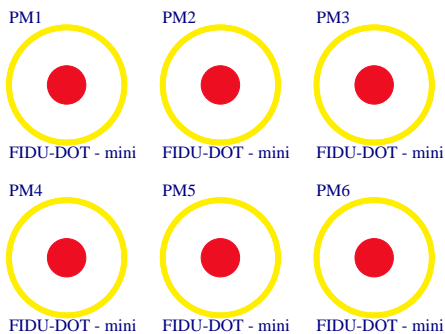


Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe

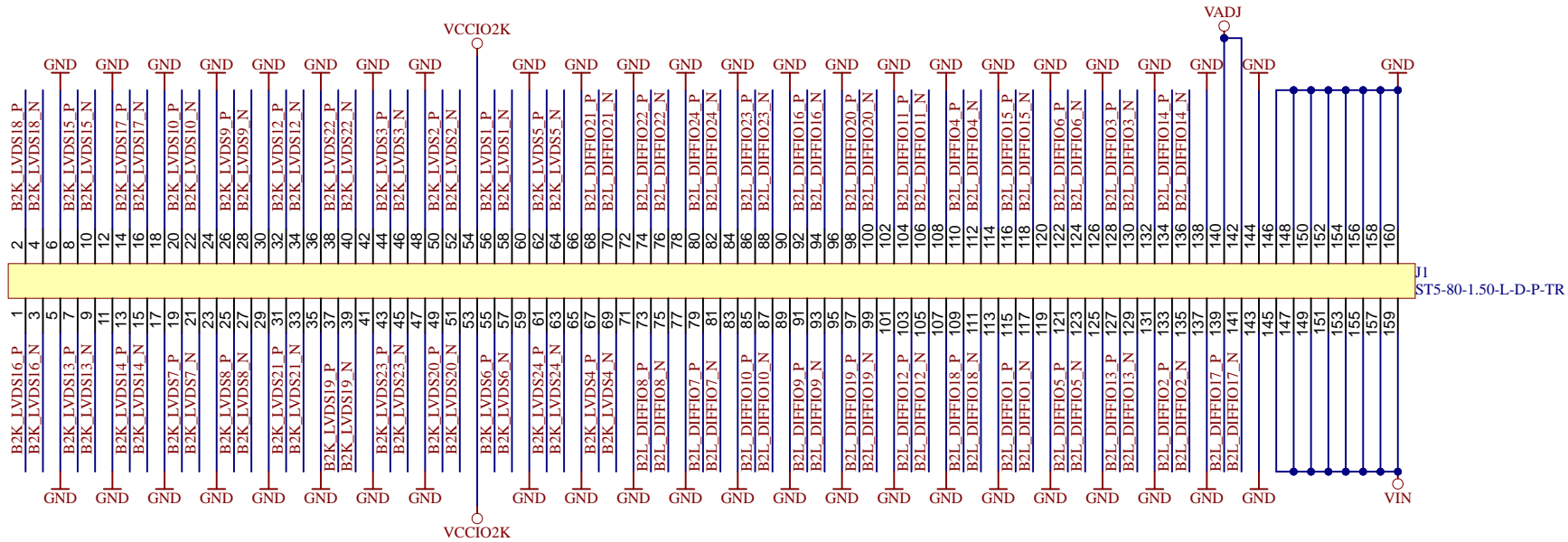
Serial  
Serialnummer 6,3 x 6,3mm



Assembly variant	220-5E
Created by	ED
Modified by	
Modified at	2022-04-01
SVN Revision	15170



Title: TEI0006		
A4	Number: TEI0006 220-5E	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH / TT	Page2 of 23
Filename: TEI0006.SchDoc		



Title: TEI0006		
A4	Number: TEI0006 220-5E	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH / TT	Page3 of 23
Filename: J1.SchDoc		

1

2

3

4

A

A

B

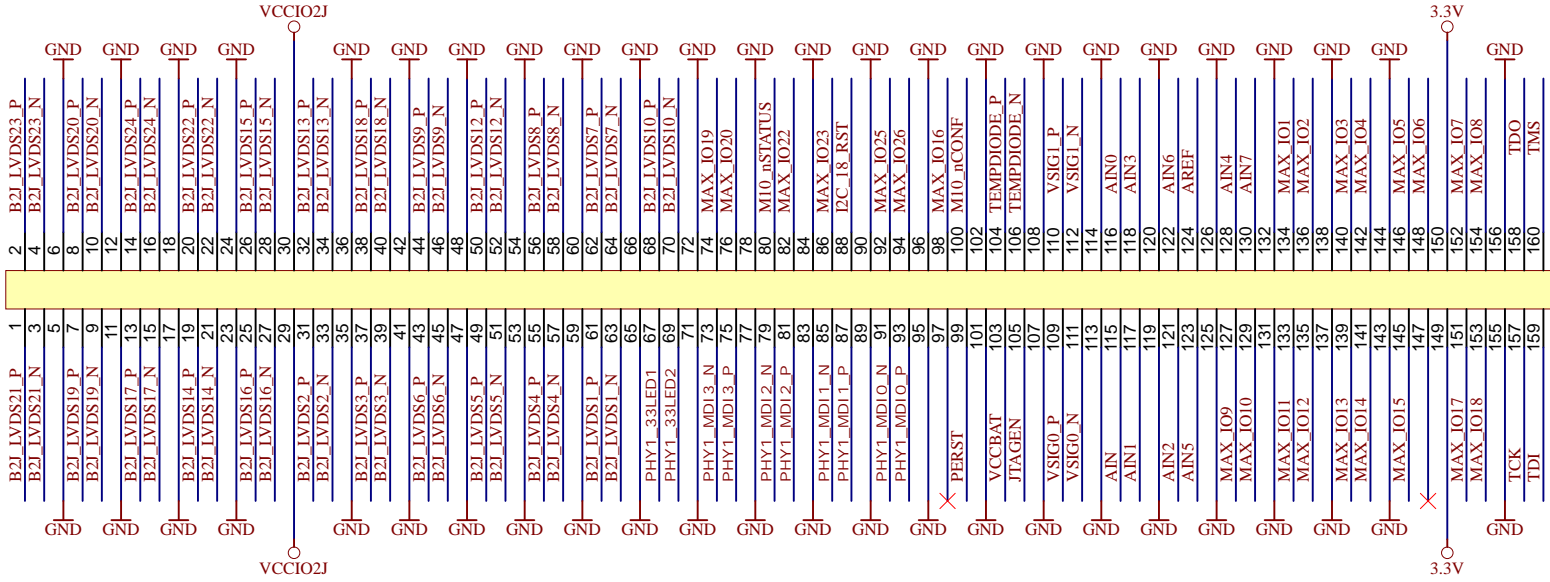
B

C

C

D

D



J2 ST5-80-1.50-L-D-P-TR



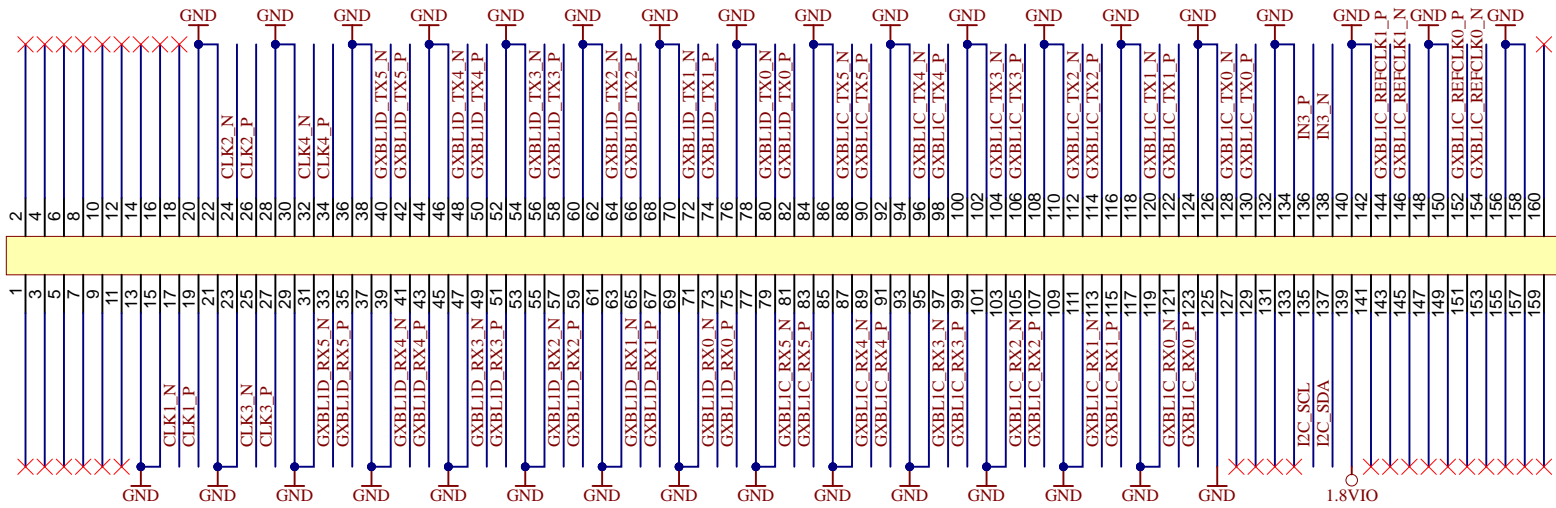
Title: TEI0006		
A4	Number: TEI0006 220-5E	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH / TT	Page4 of 23
Filename: J2.SchDoc		

1

2

3

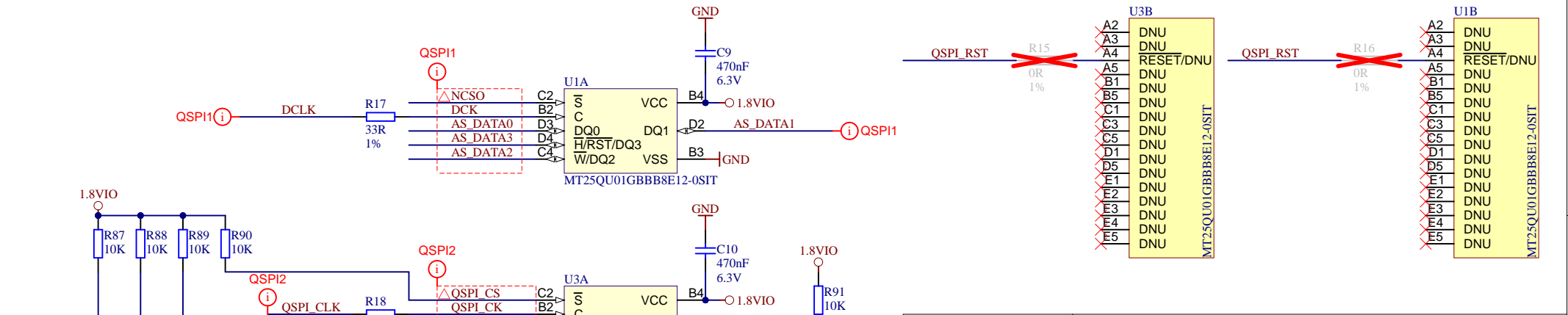
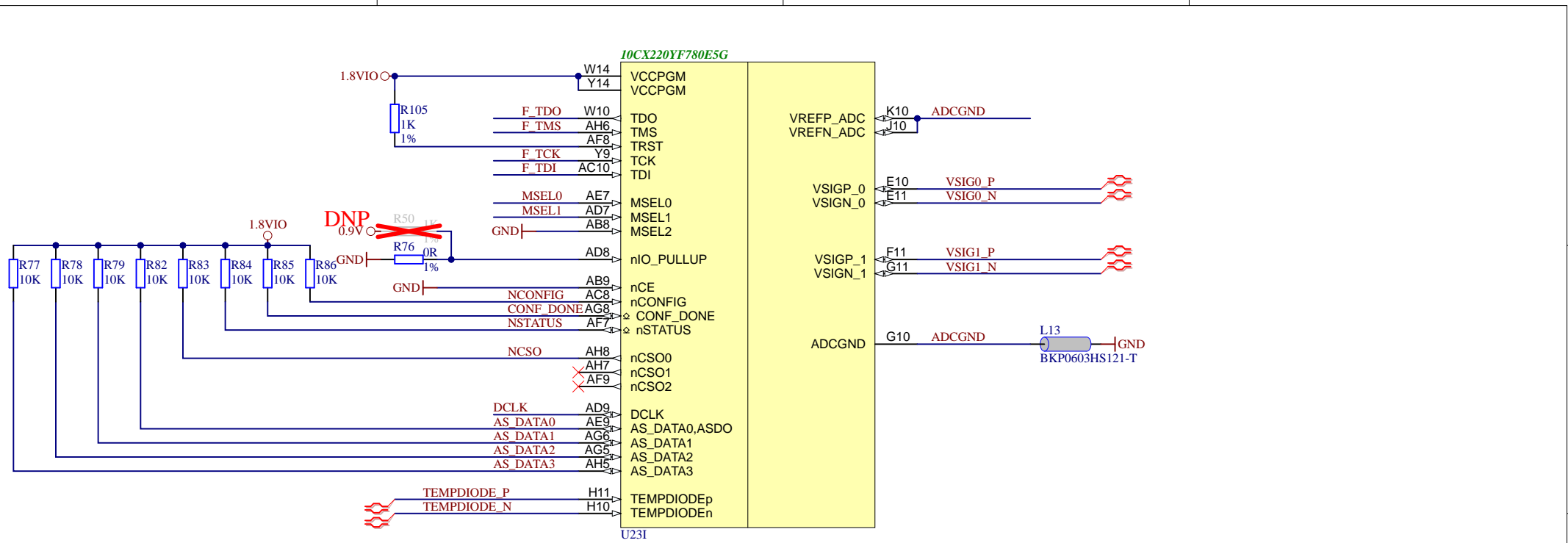

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U3  
 ST5-80-1.50-L-D-P-TR



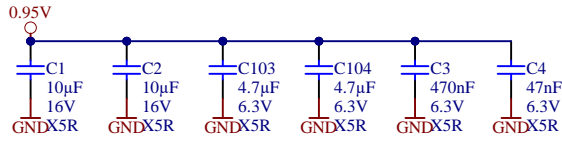
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A4	Number: <b>TEI0006 220-5E</b>	Rev. <b>03</b>
Date: <b>2020-08-31</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>5</b> of <b>23</b>
Filename: <b>J3.SchDoc</b>		

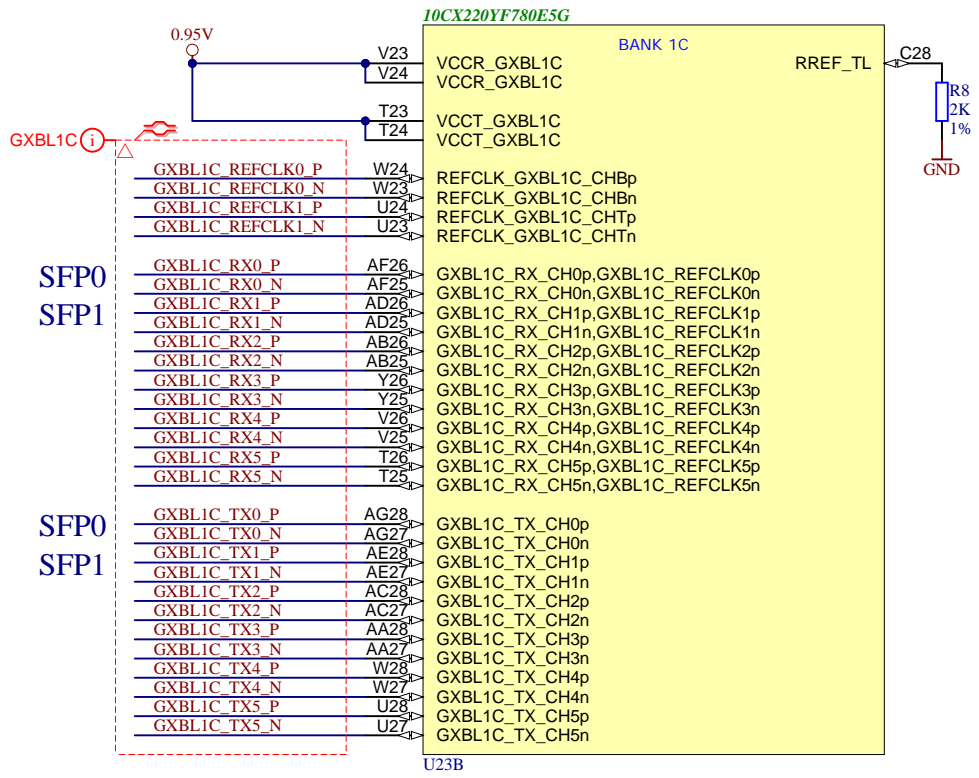
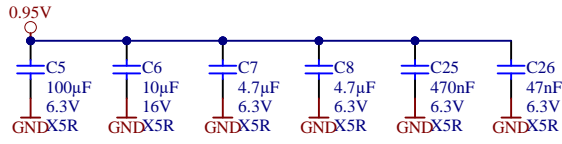
Title: TEI0006

A4	Number: TEI0006 220-5E	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 6 of 23
Filename: C10GX_CFG.SchDoc		

Placed at VCCT\_GXB pins




Placed at VCCR\_GXB pins

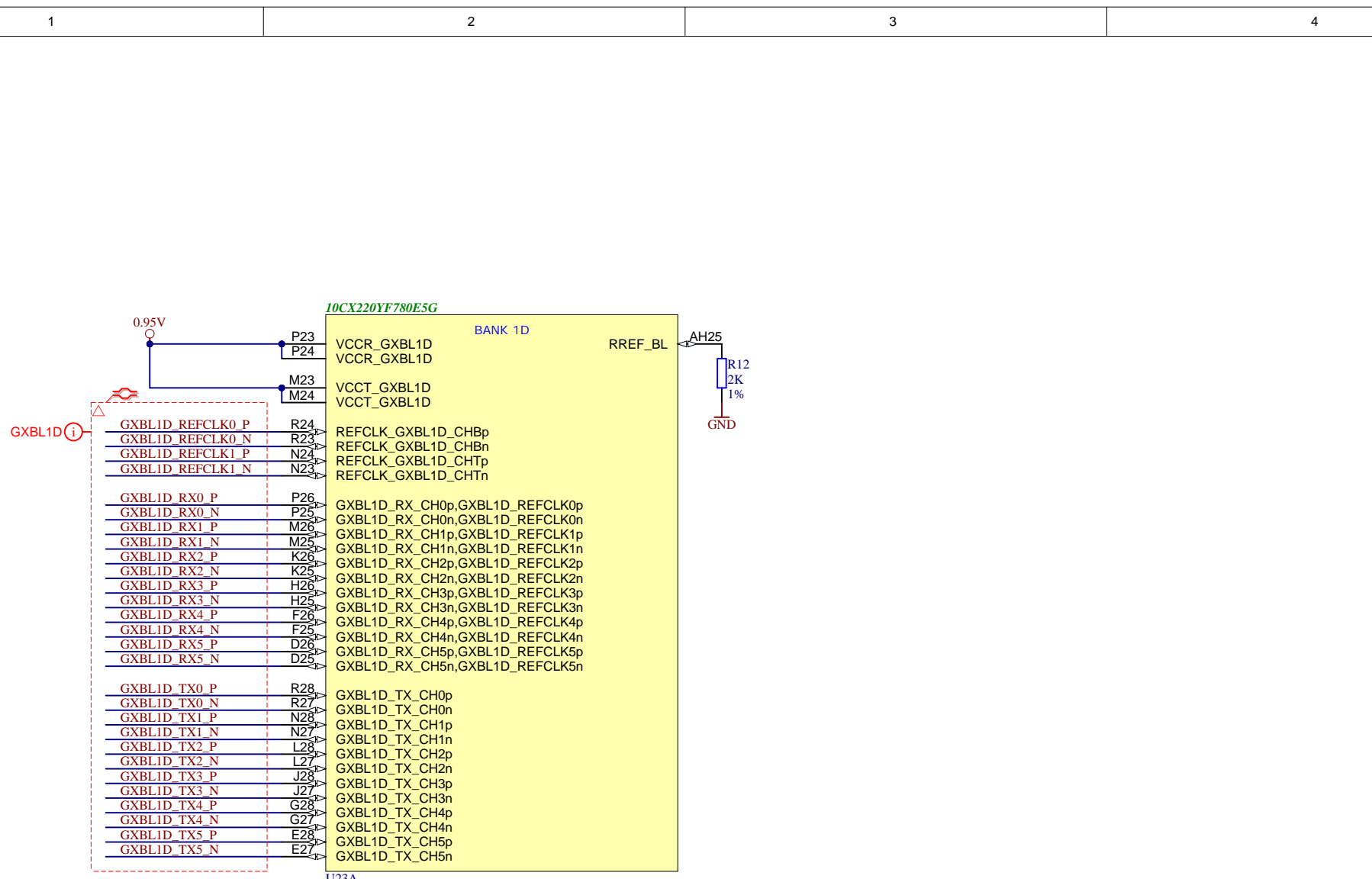



SFP0  
SFP1

SFP0  
SFP1

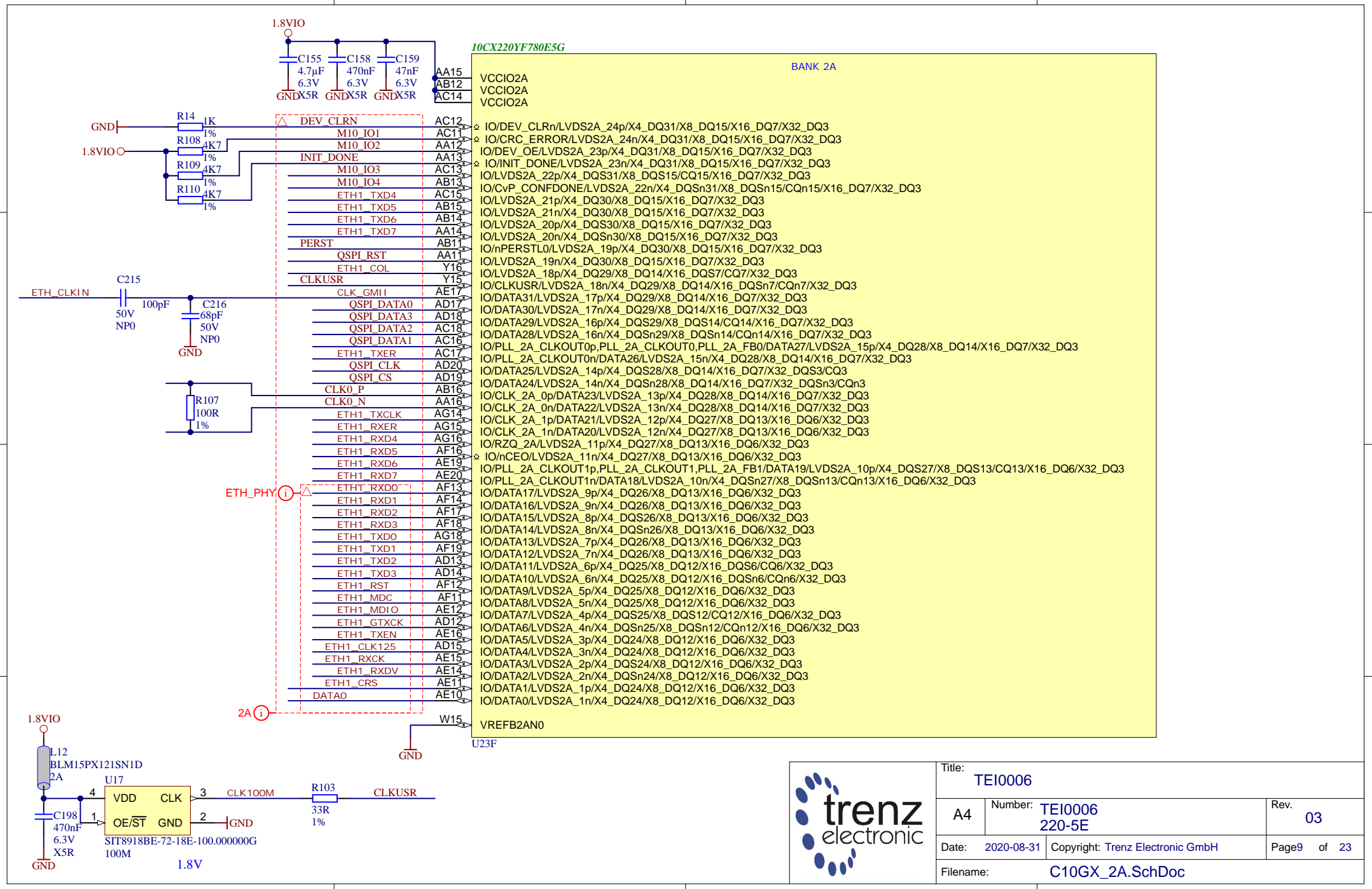


Title: TEI0006		
A4	Number: TEI0006 220-5E	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 7 of 23
Filename: C10GX_1C.SchDoc		

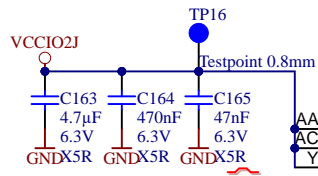


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	A4	Number: <b>TEI0006 220-5E</b>
	Date: <b>2020-08-31</b>	Copyright: <b>Trenz Electronic GmbH</b>
	Rev. <b>03</b>	Page <b>8</b> of <b>23</b>
Filename: <b>C10GX_1D.SchDoc</b>		





Title: <b>TEI0006</b>		
A4	Number: <b>TEI0006 220-5E</b>	Rev. <b>03</b>
Date: <b>2020-08-31</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>9</b> of <b>23</b>
Filename: <b>C10GX_2A.SchDoc</b>		



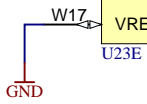
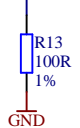
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BANK 2J

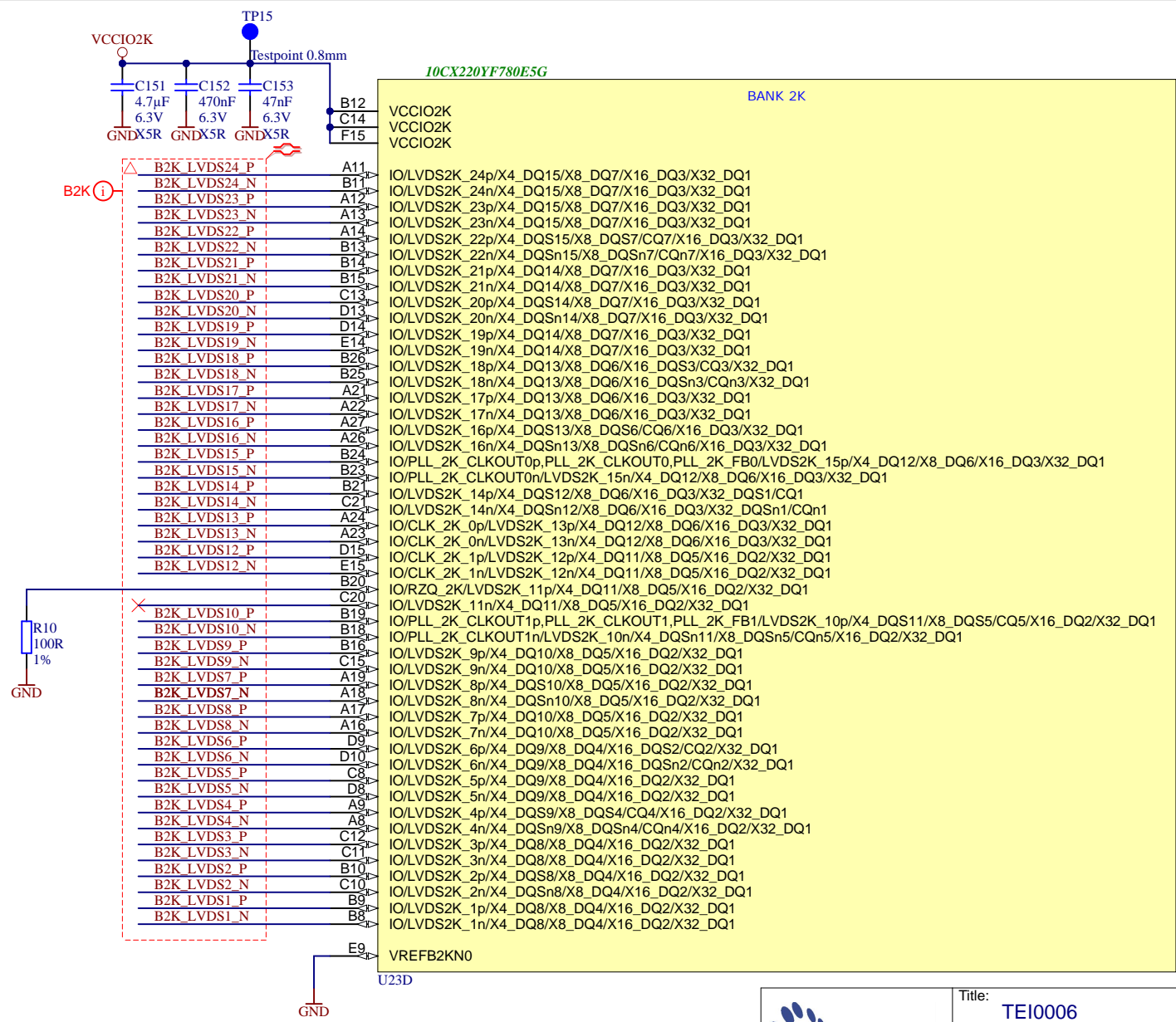
B2J (i)

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- B2J\_LVDS24\_N AC22
- B2J\_LVDS23\_P AF22
- B2J\_LVDS23\_N AE22
- B2J\_LVDS22\_P AC23
- B2J\_LVDS22\_N AB23
- B2J\_LVDS21\_P AA23
- B2J\_LVDS21\_N AA22
- B2J\_LVDS20\_P AE23
- B2J\_LVDS20\_N AD23
- B2J\_LVDS19\_P AG23
- B2J\_LVDS19\_N AF23
- B2J\_LVDS18\_P AG19
- B2J\_LVDS18\_N AG20
- B2J\_LVDS17\_P AH22
- B2J\_LVDS17\_N AG21
- B2J\_LVDS16\_P AF21
- B2J\_LVDS16\_N AE21
- B2J\_LVDS15\_P AC21
- B2J\_LVDS15\_N AB21
- B2J\_LVDS14\_P AH21
- B2J\_LVDS14\_N AH20
- B2J\_LVDS13\_P AC20
- B2J\_LVDS13\_N AB20
- B2J\_LVDS12\_P AA18
- B2J\_LVDS12\_N AA19
- Y20
- Y19
- X B2J\_LVDS10\_P AA17
- B2J\_LVDS10\_N Y17
- B2J\_LVDS9\_P AB18
- B2J\_LVDS9\_N AB19
- B2J\_LVDS8\_P W20
- B2J\_LVDS8\_N W21
- B2J\_LVDS7\_P AA21
- B2J\_LVDS7\_N Y21
- B2J\_LVDS6\_P AH13
- B2J\_LVDS6\_N AG13
- B2J\_LVDS5\_P AH12
- B2J\_LVDS5\_N AG11
- B2J\_LVDS4\_P AH11
- B2J\_LVDS4\_N AH10
- B2J\_LVDS3\_P AH16
- B2J\_LVDS3\_N AH15
- B2J\_LVDS2\_P AH18
- B2J\_LVDS2\_N AH17
- B2J\_LVDS1\_P AG10
- B2J\_LVDS1\_N AG9

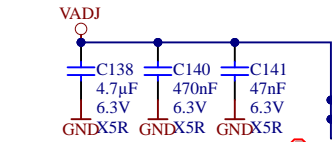
- VCCIO2J
- VCCIO2J
- VCCIO2J
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- IO/LVDS2J\_24n/X4\_DQ23/X8\_DQ11/X16\_DQ5/X32\_DQ2
- IO/LVDS2J\_23p/X4\_DQ23/X8\_DQ11/X16\_DQ5/X32\_DQ2
- IO/LVDS2J\_23n/X4\_DQ23/X8\_DQ11/X16\_DQ5/X32\_DQ2
- IO/LVDS2J\_22p/X4\_DQS23/X8\_DQS11/CQ11/X16\_DQ5/X32\_DQ2
- IO/LVDS2J\_22n/X4\_DQSn23/X8\_DQSn11/CQn11/X16\_DQ5/X32\_DQ2
- IO/LVDS2J\_21p/X4\_DQ22/X8\_DQ11/X16\_DQ5/X32\_DQ2
- IO/LVDS2J\_21n/X4\_DQ22/X8\_DQ11/X16\_DQ5/X32\_DQ2
- IO/LVDS2J\_20p/X4\_DQS22/X8\_DQ11/X16\_DQ5/X32\_DQ2
- IO/LVDS2J\_20n/X4\_DQSn22/X8\_DQ11/X16\_DQ5/X32\_DQ2
- IO/LVDS2J\_19p/X4\_DQ22/X8\_DQ11/X16\_DQ5/X32\_DQ2
- IO/LVDS2J\_19n/X4\_DQ22/X8\_DQ11/X16\_DQ5/X32\_DQ2
- IO/LVDS2J\_18p/X4\_DQ21/X8\_DQ10/X16\_DQS5/CQ5/X32\_DQ2
- IO/LVDS2J\_18n/X4\_DQ21/X8\_DQ10/X16\_DQSn5/CQn5/X32\_DQ2
- IO/LVDS2J\_17p/X4\_DQ21/X8\_DQ10/X16\_DQ5/X32\_DQ2
- IO/LVDS2J\_17n/X4\_DQ21/X8\_DQ10/X16\_DQ5/X32\_DQ2
- IO/LVDS2J\_16p/X4\_DQS21/X8\_DQS10/CQ10/X16\_DQ5/X32\_DQ2
- IO/LVDS2J\_16n/X4\_DQSn21/X8\_DQSn10/CQn10/X16\_DQ5/X32\_DQ2
- IO/PLL\_2J\_CLKOUT0p,PLL\_2J\_CLKOUT0,PLL\_2J\_FB0/LVDS2J\_15p/X4\_DQ20/X8\_DQ10/X16\_DQ5/X32\_DQ2
- IO/PLL\_2J\_CLKOUT0n/LVDS2J\_15n/X4\_DQ20/X8\_DQ10/X16\_DQ5/X32\_DQ2
- IO/LVDS2J\_14p/X4\_DQS20/X8\_DQ10/X16\_DQ5/X32\_DQS2/CQ2
- IO/LVDS2J\_14n/X4\_DQSn20/X8\_DQ10/X16\_DQ5/X32\_DQS2/CQn2
- IO/CLK\_2J\_0p/LVDS2J\_13p/X4\_DQ20/X8\_DQ10/X16\_DQ5/X32\_DQ2
- IO/CLK\_2J\_0n/LVDS2J\_13n/X4\_DQ20/X8\_DQ10/X16\_DQ5/X32\_DQ2
- IO/CLK\_2J\_1p/LVDS2J\_12p/X4\_DQ19/X8\_DQ9/X16\_DQ4/X32\_DQ2
- IO/CLK\_2J\_1n/LVDS2J\_12n/X4\_DQ19/X8\_DQ9/X16\_DQ4/X32\_DQ2
- IO/RZQ\_2J/LVDS2J\_11p/X4\_DQ19/X8\_DQ9/X16\_DQ4/X32\_DQ2
- IO/LVDS2J\_11n/X4\_DQ19/X8\_DQ9/X16\_DQ4/X32\_DQ2
- IO/PLL\_2J\_CLKOUT1p,PLL\_2J\_CLKOUT1,PLL\_2J\_FB1/LVDS2J\_10p/X4\_DQS19/X8\_DQS9/CQ9/X16\_DQ4/X32\_DQ2
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- IO/LVDS2J\_9p/X4\_DQ18/X8\_DQ9/X16\_DQ4/X32\_DQ2
- IO/LVDS2J\_9n/X4\_DQ18/X8\_DQ9/X16\_DQ4/X32\_DQ2
- IO/LVDS2J\_8p/X4\_DQS18/X8\_DQ9/X16\_DQ4/X32\_DQ2
- IO/LVDS2J\_8n/X4\_DQSn18/X8\_DQ9/X16\_DQ4/X32\_DQ2
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- IO/LVDS2J\_4n/X4\_DQSn17/X8\_DQSn8/CQn8/X16\_DQ4/X32\_DQ2
- IO/LVDS2J\_3p/X4\_DQ16/X8\_DQ8/X16\_DQ4/X32\_DQ2
- IO/LVDS2J\_3n/X4\_DQ16/X8\_DQ8/X16\_DQ4/X32\_DQ2
- IO/LVDS2J\_2p/X4\_DQS16/X8\_DQ8/X16\_DQ4/X32\_DQ2
- IO/LVDS2J\_2n/X4\_DQSn16/X8\_DQ8/X16\_DQ4/X32\_DQ2
- IO/LVDS2J\_1p/X4\_DQ16/X8\_DQ8/X16\_DQ4/X32\_DQ2
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Title: TEI0006		
A4	Number: TEI0006 220-5E	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 10 of 23
Filename: C10GX_2J.SchDoc		



Title: <b>TEI0006</b>		
A4	Number: <b>TEI0006 220-5E</b>	Rev. <b>03</b>
Date: <b>2020-08-31</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>11</b> of <b>23</b>
Filename: <b>C10GX_2K.SchDoc</b>		



### 3V IO Bank

U23C

BANK 2L

- B2L\_DIFFIO24 P
- B2L\_DIFFIO24 N
- B2L\_DIFFIO23 P
- B2L\_DIFFIO23 N
- B2L\_DIFFIO22 P
- B2L\_DIFFIO22 N
- B2L\_DIFFIO21 P
- B2L\_DIFFIO21 N
- B2L\_DIFFIO20 P
- B2L\_DIFFIO20 N
- B2L\_DIFFIO19 P
- B2L\_DIFFIO19 N
- B2L\_DIFFIO18 P
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- B2L\_DIFFIO17 P
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- B2L\_DIFFIO14 P
- B2L\_DIFFIO14 N
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- B2L\_DIFFIO8 N
- B2L\_DIFFIO7 P
- B2L\_DIFFIO7 N
- B2L\_DIFFIO6 P
- B2L\_DIFFIO6 N
- B2L\_DIFFIO5 P
- B2L\_DIFFIO5 N
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- B2L\_DIFFIO3 P
- B2L\_DIFFIO3 N
- B2L\_DIFFIO2 P
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- B2L\_DIFFIO1 P
- B2L\_DIFFIO1 N

- C18
- D17
- C17
- C16
- D20
- E20
- F19
- E16
- E17
- D19
- D18
- K23
- K22
- K19
- K20
- H20
- H21
- J22
- H22
- J20
- K21
- J23
- H23
- F23
- G23
- F21
- G21
- C23
- C22
- E22
- F22
- D23
- E23
- D22
- E21
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- H17
- H16

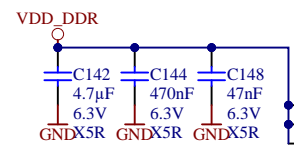
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 IO/DIFFIO2L\_23n/X4\_DQ7/X8\_DQ3/X16\_DQ1/X32\_DQ0  
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 IO/DIFFIO2L\_17n/X4\_DQ5/X8\_DQ2/X16\_DQ1/X32\_DQ0  
 IO/DIFFIO2L\_16p/X4\_DQS5/X8\_DQS2/CQ2/X16\_DQ1/X32\_DQ0  
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 IO/PLL\_2L\_CLKOUT0n/DIFFIO2L\_15n/X4\_DQ4/X8\_DQ2/X16\_DQ1/X32\_DQ0  
 IO/DIFFIO2L\_14p/X4\_DQS4/X8\_DQ2/X16\_DQ1/X32\_DQS0/CQ0  
 IO/DIFFIO2L\_14n/X4\_DQSn4/X8\_DQ2/X16\_DQ1/X32\_DQS0/CQn0  
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 IO/CLK\_2L\_0n/DIFFIO2L\_13n/X4\_DQ4/X8\_DQ2/X16\_DQ1/X32\_DQ0  
 IO/CLK\_2L\_1p/DIFFIO2L\_12p/X4\_DQ3/X8\_DQ1/X16\_DQ0/X32\_DQ0  
 IO/CLK\_2L\_1n/DIFFIO2L\_12n/X4\_DQ3/X8\_DQ1/X16\_DQ0/X32\_DQ0  
 IO/RZQ\_2L/DIFFIO2L\_11p/X4\_DQ3/X8\_DQ1/X16\_DQ0/X32\_DQ0  
 IO/DIFFIO2L\_11n/X4\_DQ3/X8\_DQ1/X16\_DQ0/X32\_DQ0  
 IO/PLL\_2L\_CLKOUT1p,PLL\_2L\_CLKOUT1,PLL\_2L\_FB1/DIFFIO2L\_10p/X4\_DQS3/X8\_DQS1/CQ1/X16\_DQ0/X32\_DQ0  
 IO/PLL\_2L\_CLKOUT1n/DIFFIO2L\_10n/X4\_DQSn3/X8\_DQSn1/CQn1/X16\_DQ0/X32\_DQ0  
 IO/DIFFIO2L\_9p/X4\_DQ2/X8\_DQ1/X16\_DQ0/X32\_DQ0  
 IO/DIFFIO2L\_9n/X4\_DQ2/X8\_DQ1/X16\_DQ0/X32\_DQ0  
 IO/DIFFIO2L\_8p/X4\_DQS2/X8\_DQ1/X16\_DQ0/X32\_DQ0  
 IO/DIFFIO2L\_8n/X4\_DQSn2/X8\_DQ1/X16\_DQ0/X32\_DQ0  
 IO/DIFFIO2L\_7p/X4\_DQ2/X8\_DQ1/X16\_DQ0/X32\_DQ0  
 IO/DIFFIO2L\_7n/X4\_DQ2/X8\_DQ1/X16\_DQ0/X32\_DQ0  
 IO/DIFFIO2L\_6p/X4\_DQ1/X8\_DQ0/X16\_DQS0/CQ0/X32\_DQ0  
 IO/DIFFIO2L\_6n/X4\_DQ1/X8\_DQ0/X16\_DQSn0/CQn0/X32\_DQ0  
 IO/DIFFIO2L\_5p/X4\_DQ1/X8\_DQ0/X16\_DQ0/X32\_DQ0  
 IO/DIFFIO2L\_5n/X4\_DQ1/X8\_DQ0/X16\_DQ0/X32\_DQ0  
 IO/DIFFIO2L\_4p/X4\_DQS1/X8\_DQS0/CQ0/X16\_DQ0/X32\_DQ0  
 IO/DIFFIO2L\_4n/X4\_DQSn1/X8\_DQSn0/CQn0/X16\_DQ0/X32\_DQ0  
 IO/DIFFIO2L\_3p/X4\_DQ0/X8\_DQ0/X16\_DQ0/X32\_DQ0  
 IO/DIFFIO2L\_3n/X4\_DQ0/X8\_DQ0/X16\_DQ0/X32\_DQ0  
 IO/DIFFIO2L\_2p/X4\_DQS0/X8\_DQ0/X16\_DQ0/X32\_DQ0  
 IO/DIFFIO2L\_2n/X4\_DQSn0/X8\_DQ0/X16\_DQ0/X32\_DQ0  
 IO/DIFFIO2L\_1p/X4\_DQ0/X8\_DQ0/X16\_DQ0/X32\_DQ0  
 IO/DIFFIO2L\_1n/X4\_DQ0/X8\_DQ0/X16\_DQ0/X32\_DQ0

VREFB2LN0

10CX220YF780E5G



Title: <b>TEI0006</b>		
A4	Number: <b>TEI0006 220-5E</b>	Rev. <b>03</b>
Date: <b>2020-08-31</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>12</b> of <b>23</b>
Filename: <b>C10GX_2L.SchDoc</b>		



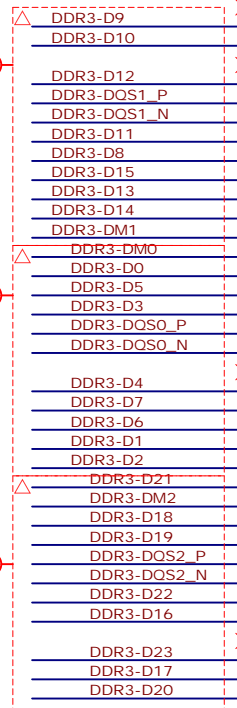
10CX220YF780E5G

BANK 3A

DDR\_DATA1 (i)

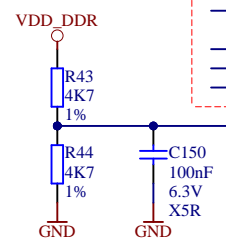
DDR\_DATA0 (i)

DDR\_DATA2 (i)



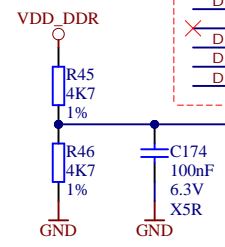
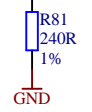
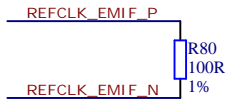
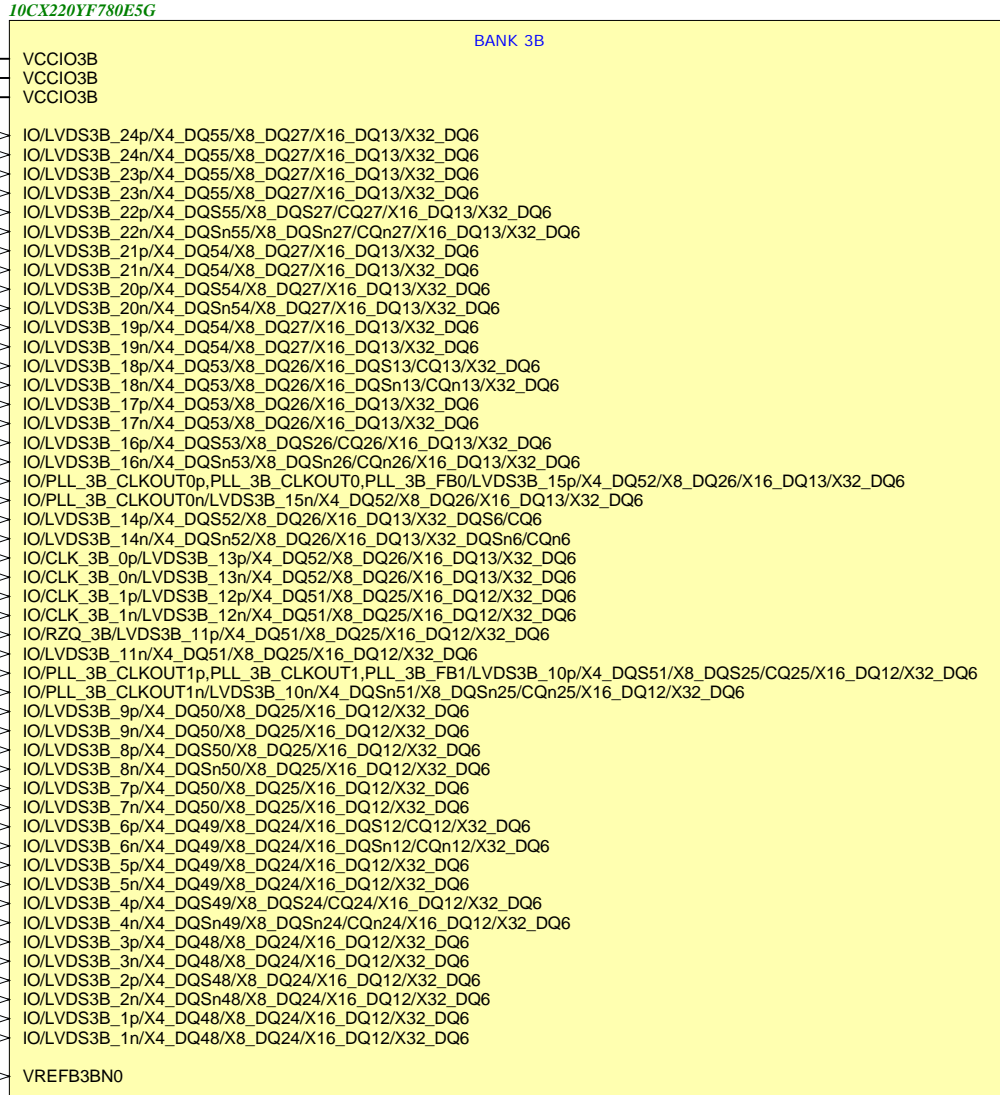
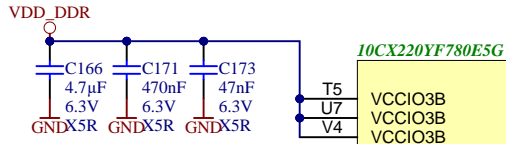
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W6	VCCIO3A
Y8	VCCIO3A
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AE6	IO/LVDS3A_22n/X4_DQSn63/X8_DQSn31/CQn31/X16_DQ15/X32_DQ7
AC6	IO/LVDS3A_21p/X4_DQ62/X8_DQ31/X16_DQ15/X32_DQ7
AC7	IO/LVDS3A_21n/X4_DQ62/X8_DQ31/X16_DQ15/X32_DQ7
AE4	IO/LVDS3A_20p/X4_DQS62/X8_DQ31/X16_DQ15/X32_DQ7
AD4	IO/LVDS3A_20n/X4_DQSn62/X8_DQ31/X16_DQ15/X32_DQ7
AH2	IO/LVDS3A_19p/X4_DQ62/X8_DQ31/X16_DQ15/X32_DQ7
AH3	IO/LVDS3A_19n/X4_DQ62/X8_DQ31/X16_DQ15/X32_DQ7
AG3	IO/LVDS3A_18p/X4_DQ61/X8_DQ30/X16_DQS15/CQ15/X32_DQ7
AF3	IO/LVDS3A_18n/X4_DQ61/X8_DQ30/X16_DQSn15/CQn15/X32_DQ7
AG1	IO/LVDS3A_17p/X4_DQ61/X8_DQ30/X16_DQ15/X32_DQ7
AF1	IO/LVDS3A_17n/X4_DQ61/X8_DQ30/X16_DQ15/X32_DQ7
AE2	IO/LVDS3A_16p/X4_DQS61/X8_DQS30/CQ30/X16_DQ15/X32_DQ7
AD2	IO/LVDS3A_16n/X4_DQSn61/X8_DQSn30/CQn30/X16_DQ15/X32_DQ7
AC1	IO/PLL_3A_CLKOUT0p,PLL_3A_CLKOUT0,PLL_3A_FB0/LVDS3A_15p/X4_DQ60/X8_DQ30/X16_DQ15/X32_DQ7
AC2	IO/PLL_3A_CLKOUT0n/LVDS3A_15n/X4_DQ60/X8_DQ30/X16_DQ15/X32_DQ7
AE1	IO/LVDS3A_14p/X4_DQS60/X8_DQ30/X16_DQ15/X32_DQS7/CQ7
AF2	IO/LVDS3A_14n/X4_DQSn60/X8_DQ30/X16_DQ15/X32_DQSn7/CQn7
AD3	IO/CLK_3A_0p/LVDS3A_13p/X4_DQ60/X8_DQ30/X16_DQ15/X32_DQ7
AC3	IO/CLK_3A_0n/LVDS3A_13n/X4_DQ60/X8_DQ30/X16_DQ15/X32_DQ7
AA6	IO/CLK_3A_1p/LVDS3A_12p/X4_DQ59/X8_DQ29/X16_DQ14/X32_DQ7
AA7	IO/CLK_3A_1n/LVDS3A_12n/X4_DQ59/X8_DQ29/X16_DQ14/X32_DQ7
AA3	IO/RZQ_3A/LVDS3A_11p/X4_DQ59/X8_DQ29/X16_DQ14/X32_DQ7
AA4	IO/LVDS3A_11n/X4_DQ59/X8_DQ29/X16_DQ14/X32_DQ7
AA2	IO/PLL_3A_CLKOUT1p,PLL_3A_CLKOUT1,PLL_3A_FB1/LVDS3A_10p/X4_DQS59/X8_DQS29/CQ29/X16_DQ14/X32_DQ7
AB3	IO/PLL_3A_CLKOUT1n/LVDS3A_10n/X4_DQSn59/X8_DQSn29/CQn29/X16_DQ14/X32_DQ7
AB6	IO/LVDS3A_9p/X4_DQ58/X8_DQ29/X16_DQ14/X32_DQ7
AB5	IO/LVDS3A_9n/X4_DQ58/X8_DQ29/X16_DQ14/X32_DQ7
AB1	IO/LVDS3A_8p/X4_DQS58/X8_DQ29/X16_DQ14/X32_DQ7
AA1	IO/LVDS3A_8n/X4_DQSn58/X8_DQ29/X16_DQ14/X32_DQ7
AC5	IO/LVDS3A_7p/X4_DQ58/X8_DQ29/X16_DQ14/X32_DQ7
AB4	IO/LVDS3A_7n/X4_DQ58/X8_DQ29/X16_DQ14/X32_DQ7
AA9	IO/LVDS3A_6p/X4_DQ57/X8_DQ28/X16_DQS14/CQ14/X32_DQ7
AA8	IO/LVDS3A_6n/X4_DQ57/X8_DQ28/X16_DQSn14/CQn14/X32_DQ7
Y1	IO/LVDS3A_5p/X4_DQ57/X8_DQ28/X16_DQ14/X32_DQ7
Y2	IO/LVDS3A_5n/X4_DQ57/X8_DQ28/X16_DQ14/X32_DQ7
W5	IO/LVDS3A_4p/X4_DQS57/X8_DQS28/CQ28/X16_DQ14/X32_DQ7
Y5	IO/LVDS3A_4n/X4_DQSn57/X8_DQSn28/CQn28/X16_DQ14/X32_DQ7
Y7	IO/LVDS3A_3p/X4_DQ56/X8_DQ28/X16_DQ14/X32_DQ7
Y6	IO/LVDS3A_3n/X4_DQ56/X8_DQ28/X16_DQ14/X32_DQ7
W8	IO/LVDS3A_2p/X4_DQS56/X8_DQ28/X16_DQ14/X32_DQ7
W7	IO/LVDS3A_2n/X4_DQSn56/X8_DQ28/X16_DQ14/X32_DQ7
W4	IO/LVDS3A_1p/X4_DQ56/X8_DQ28/X16_DQ14/X32_DQ7
Y4	IO/LVDS3A_1n/X4_DQ56/X8_DQ28/X16_DQ14/X32_DQ7

VREFB3A0  
U23H



Title: TEI0006		
A4	Number: TEI0006 220-5E	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page13 of 23
Filename: C10GX_3A.SchDoc		





Title: TEI0006		
A4	Number: TEI0006 220-5E	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 14 of 23
Filename: C10GX_3B.SchDoc		

A

B

C

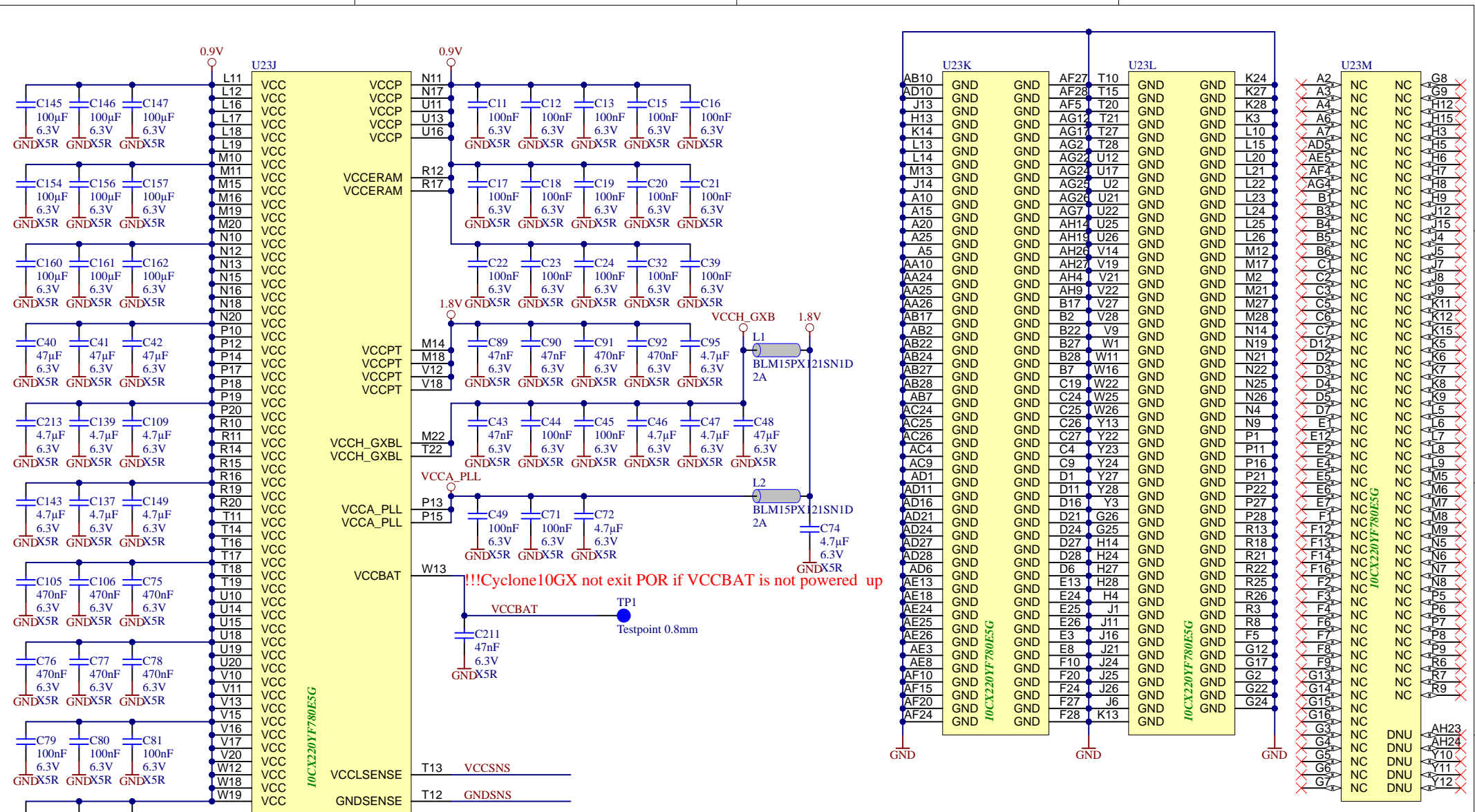
D

A

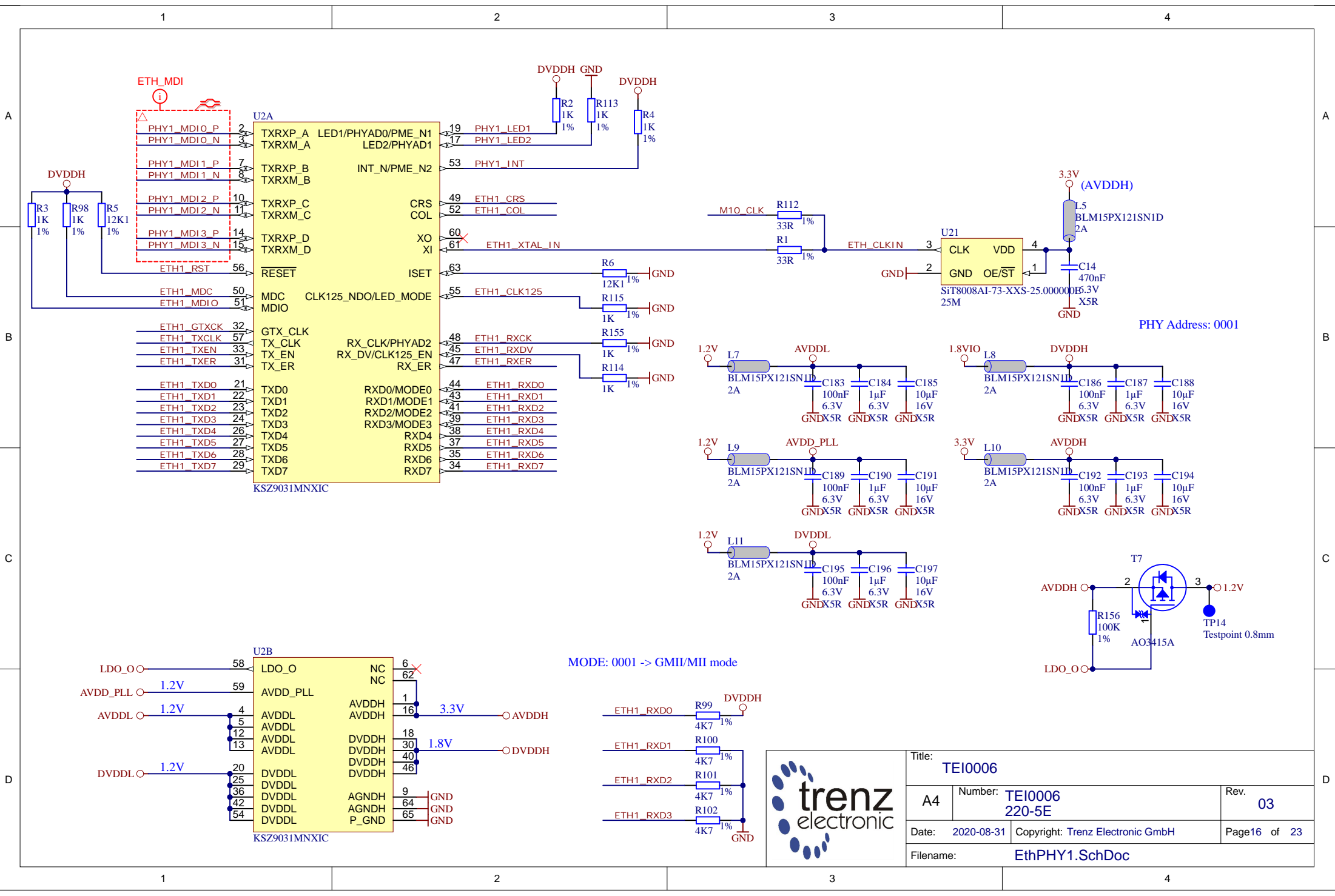
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C

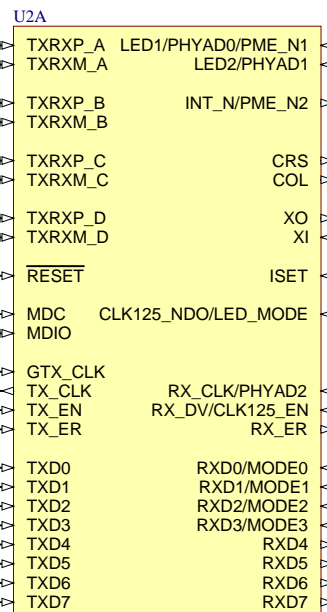
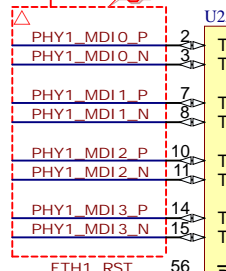
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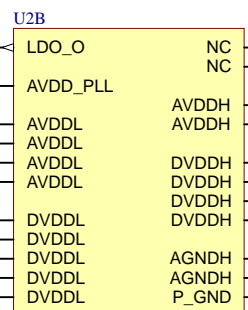
Title: TEI0006		
A4	Number: TEI0006 220-5E	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 15 of 23
Filename: C10GX_PWR.SchDoc		



ETH\_MDI

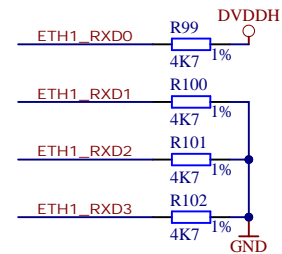


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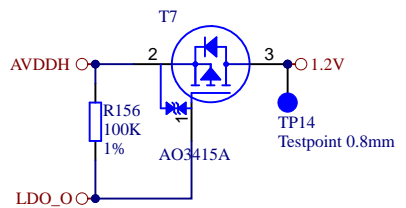
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MODE: 0001 -> GMII/MII mode



Title: TEI0006		
A4	Number: TEI0006 220-5E	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 16 of 23
Filename: EthPHY1_SchDoc		

PHY Address: 0001





1

2

3

4

A

A

B

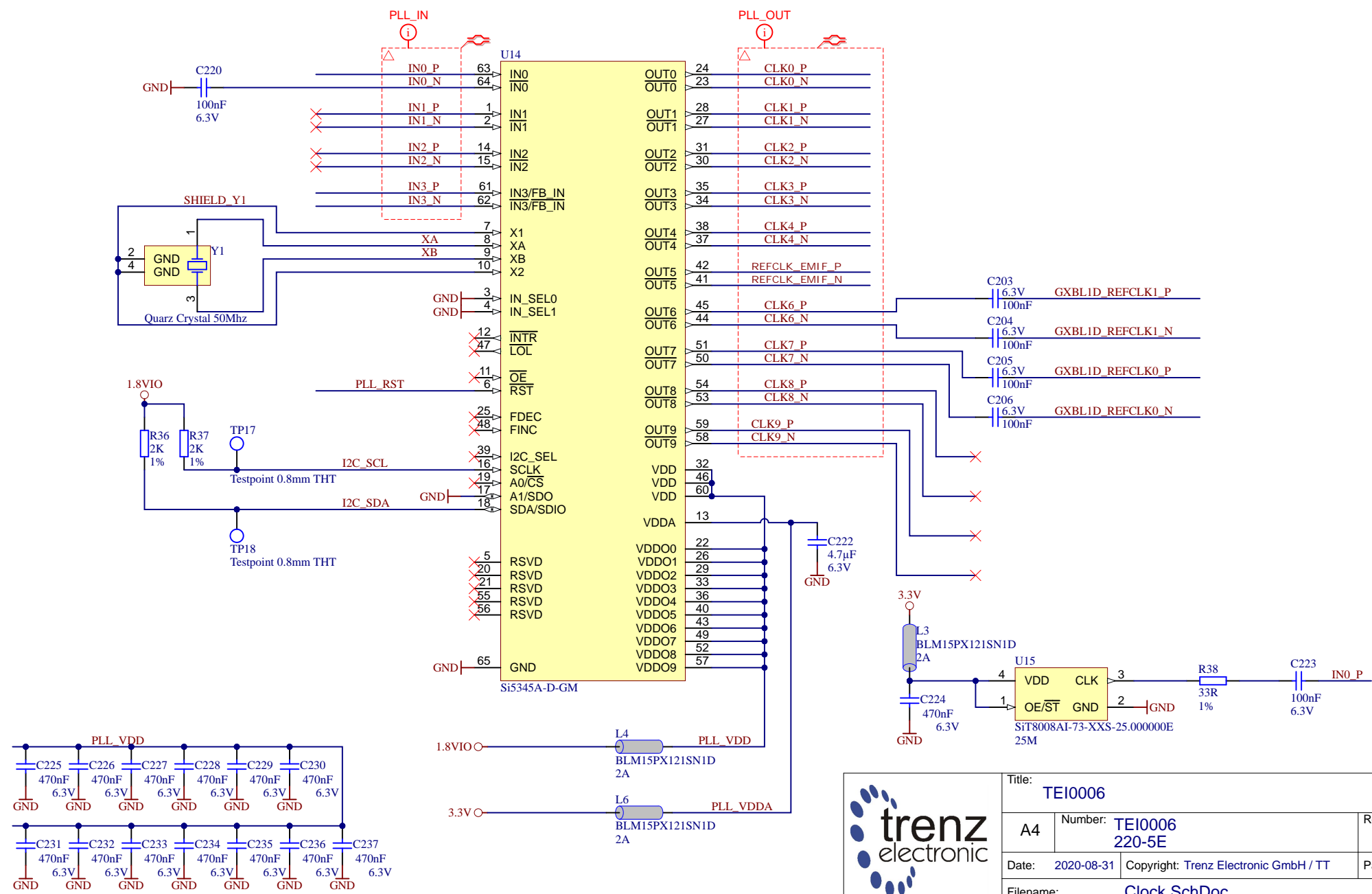
B

C

C

D

D



Title: <b>TEI0006</b>		
A4	Number: <b>TEI0006 220-5E</b>	Rev. <b>03</b>
Date: <b>2020-08-31</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>17</b> of <b>23</b>
Filename: <b>Clock.SchDoc</b>		

1

2

3

4

A

B

C

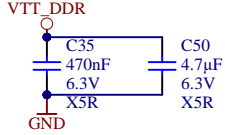
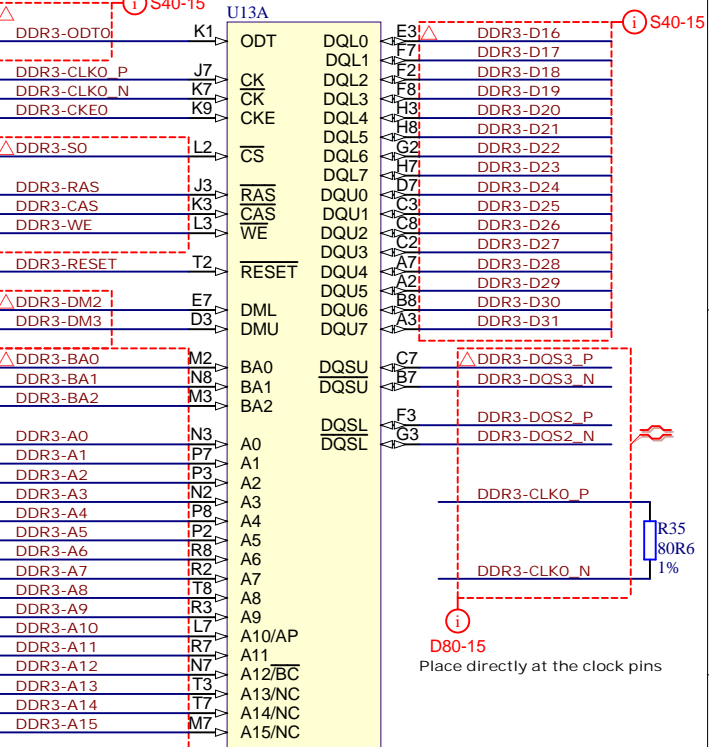
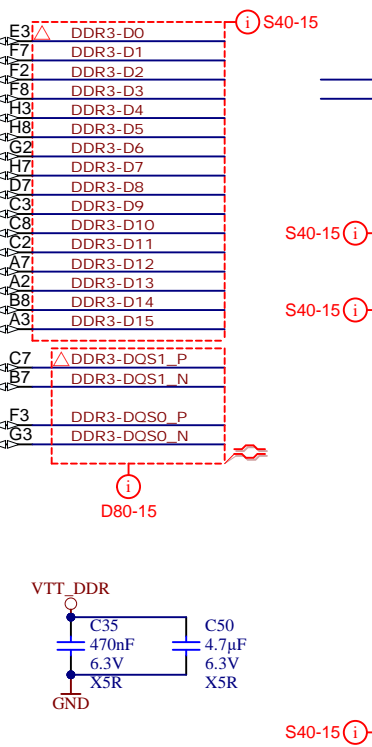
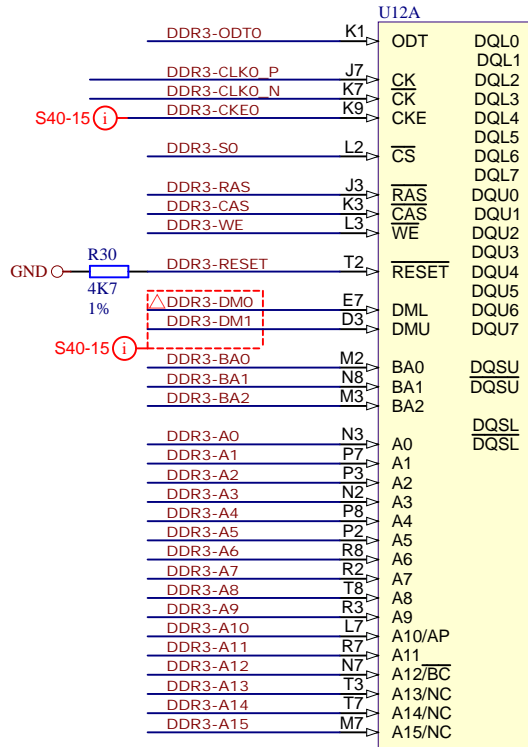
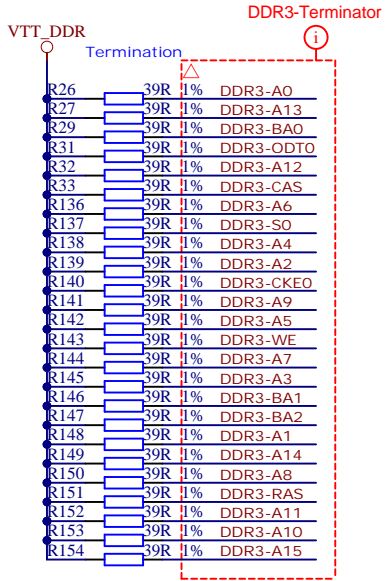
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A

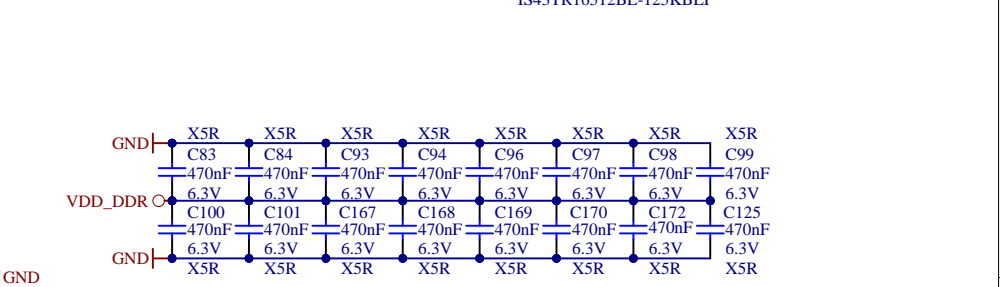
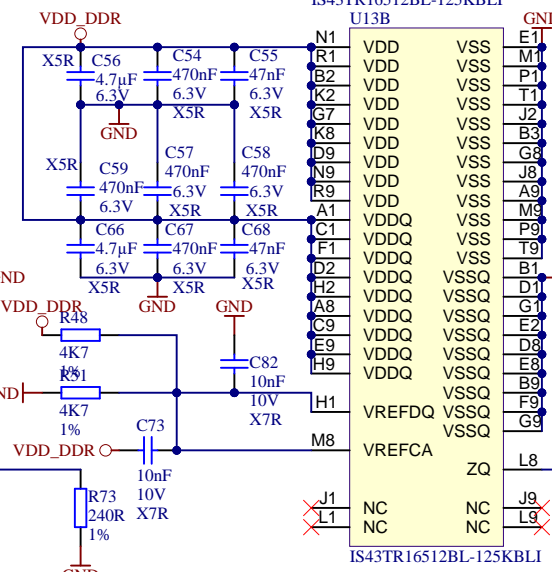
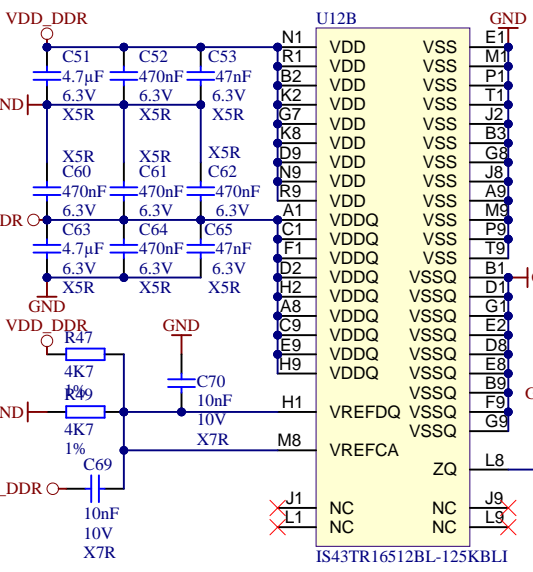
B

C

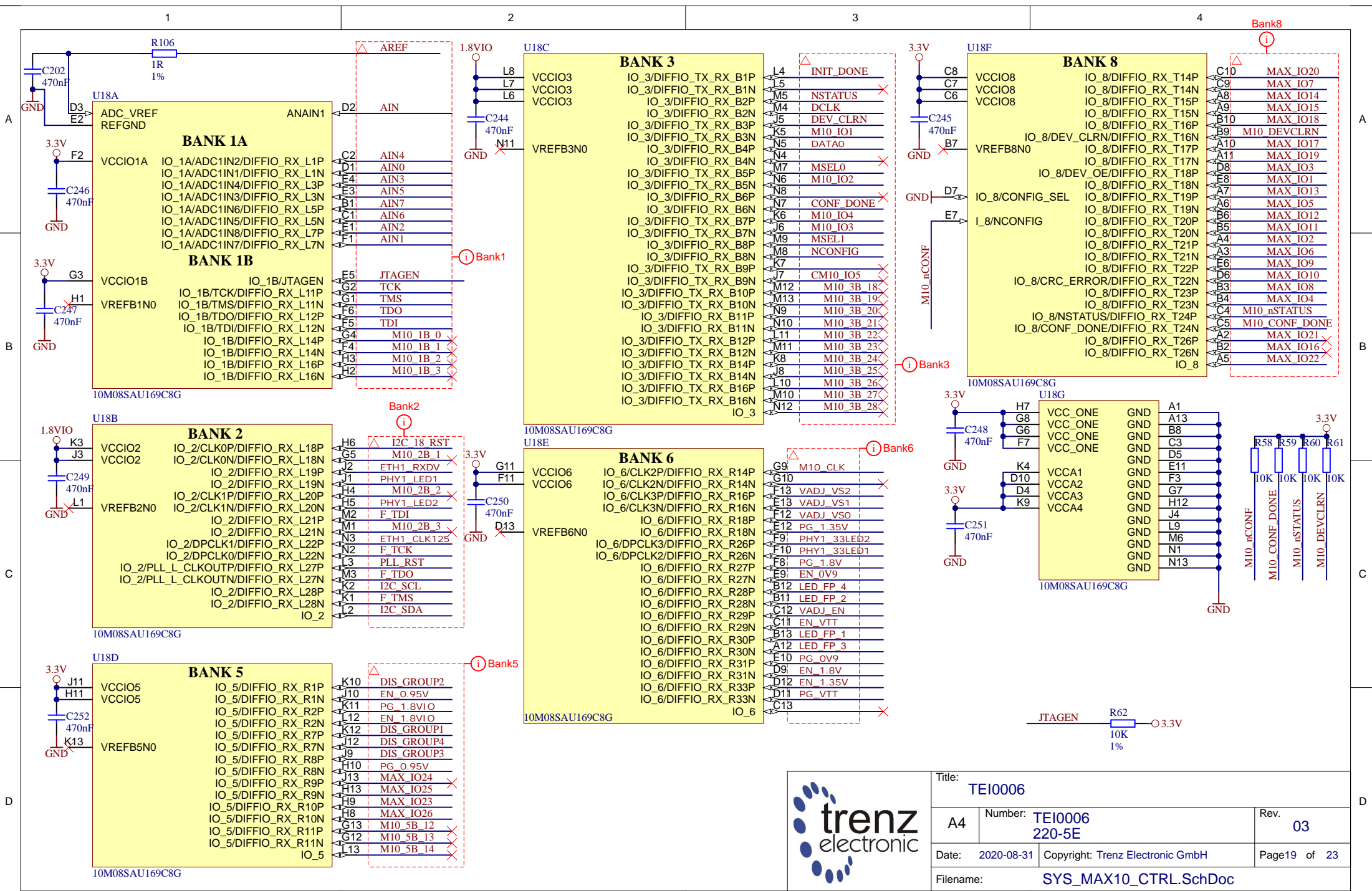
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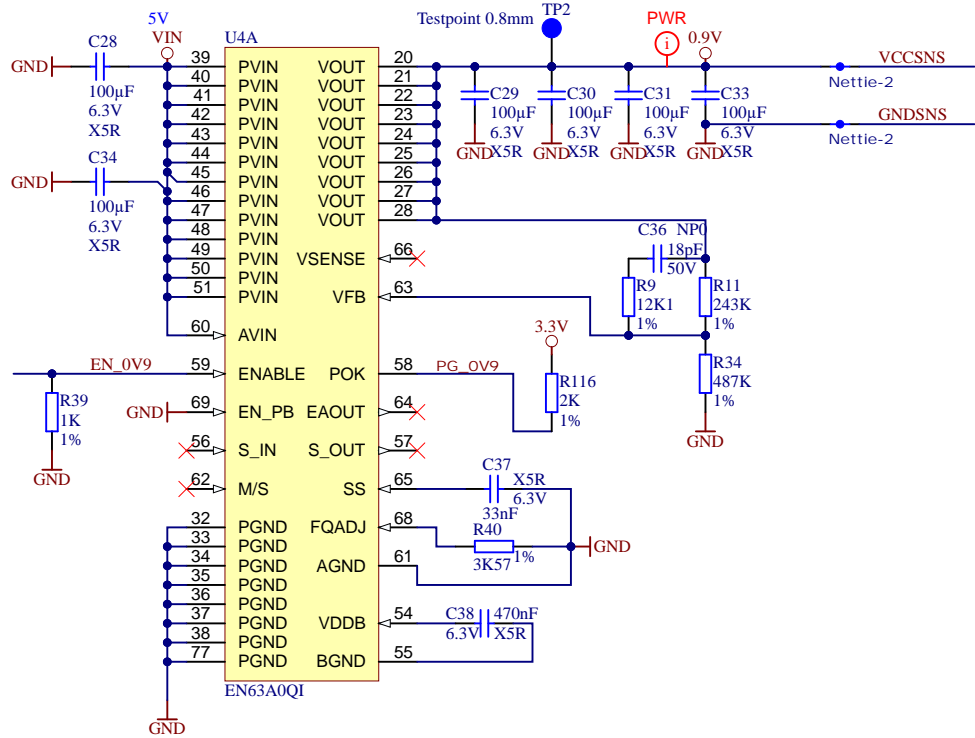
D80-15  
Place directly at the clock pins



Title: TEI0006		
A4	Number: TEI0006 220-5E	Rev. 03
Date: 2020-08-31	Copyright: 2013 Trenz Electronic GmbH	Page 18 of 23
Filename: DDR3-RAM1.SchDoc		

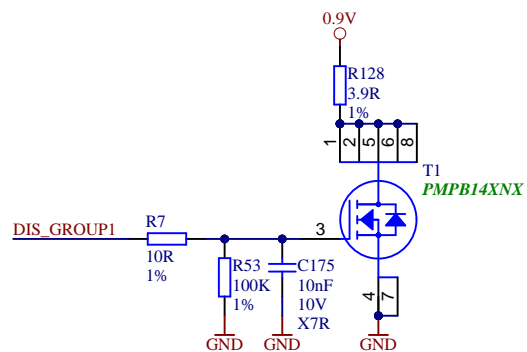


Title: <b>TEI0006</b>		
A4	Number: <b>TEI0006 220-5E</b>	Rev. <b>03</b>
Date: <b>2020-08-31</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>19</b> of <b>23</b>
Filename: <b>SYS_MAX10_CTRL.SchDoc</b>		

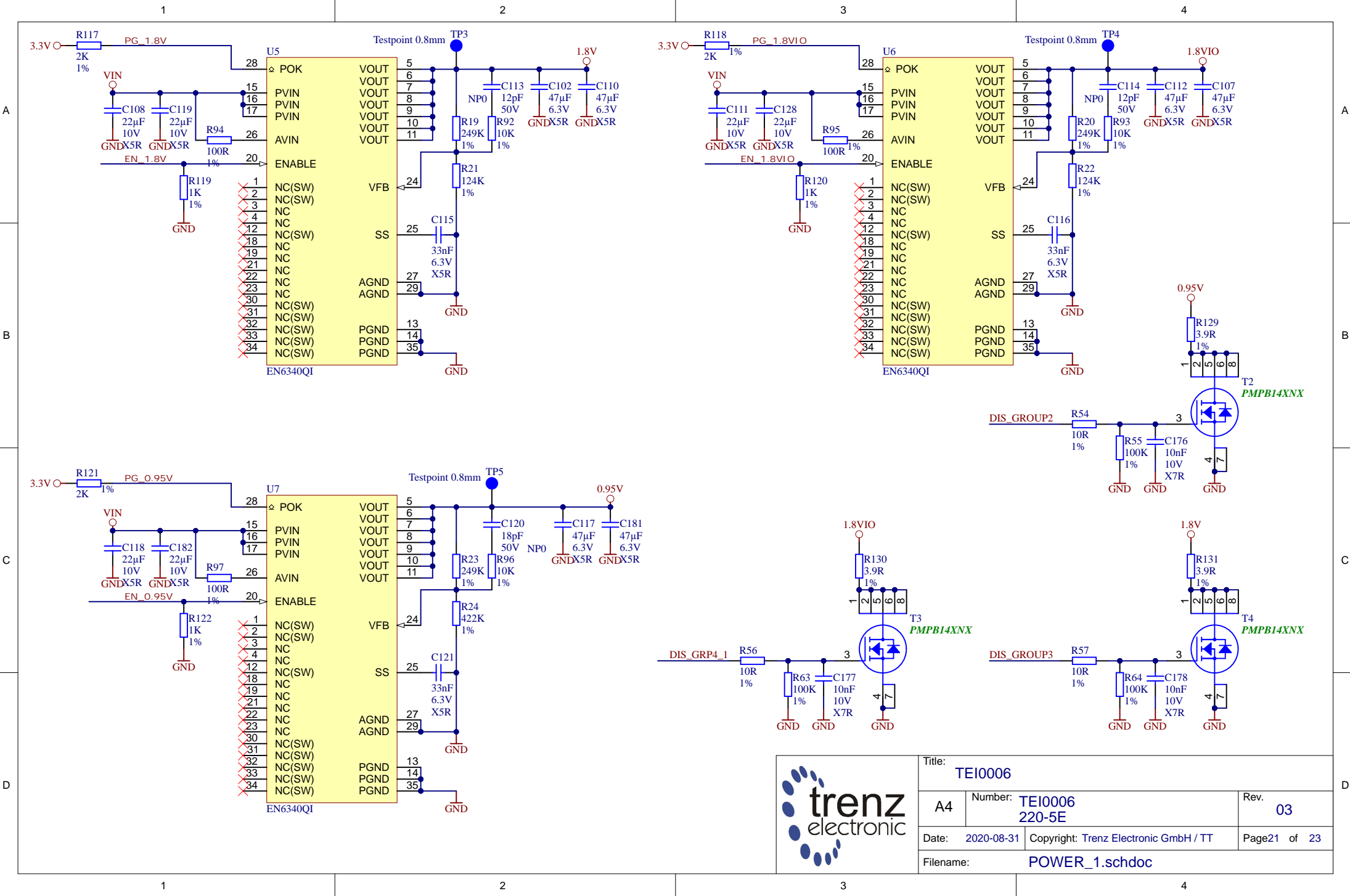


U4B			
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<del>2</del>	NC	NC	<del>18</del>
<del>3</del>	NC	NC	<del>19</del>
<del>4</del>	NC	NC	<del>29</del>
<del>5</del>	NC	NC	<del>30</del>
<del>6</del>	NC	NC(SW)	<del>31</del>
<del>7</del>	NC	NC(SW)	<del>52</del>
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<del>9</del>	NC	NC	<del>67</del>
<del>10</del>	NC	NC	<del>67</del>
<del>11</del>	NC	NC(SW)	<del>70</del>
<del>12</del>	NC	NC(SW)	<del>71</del>
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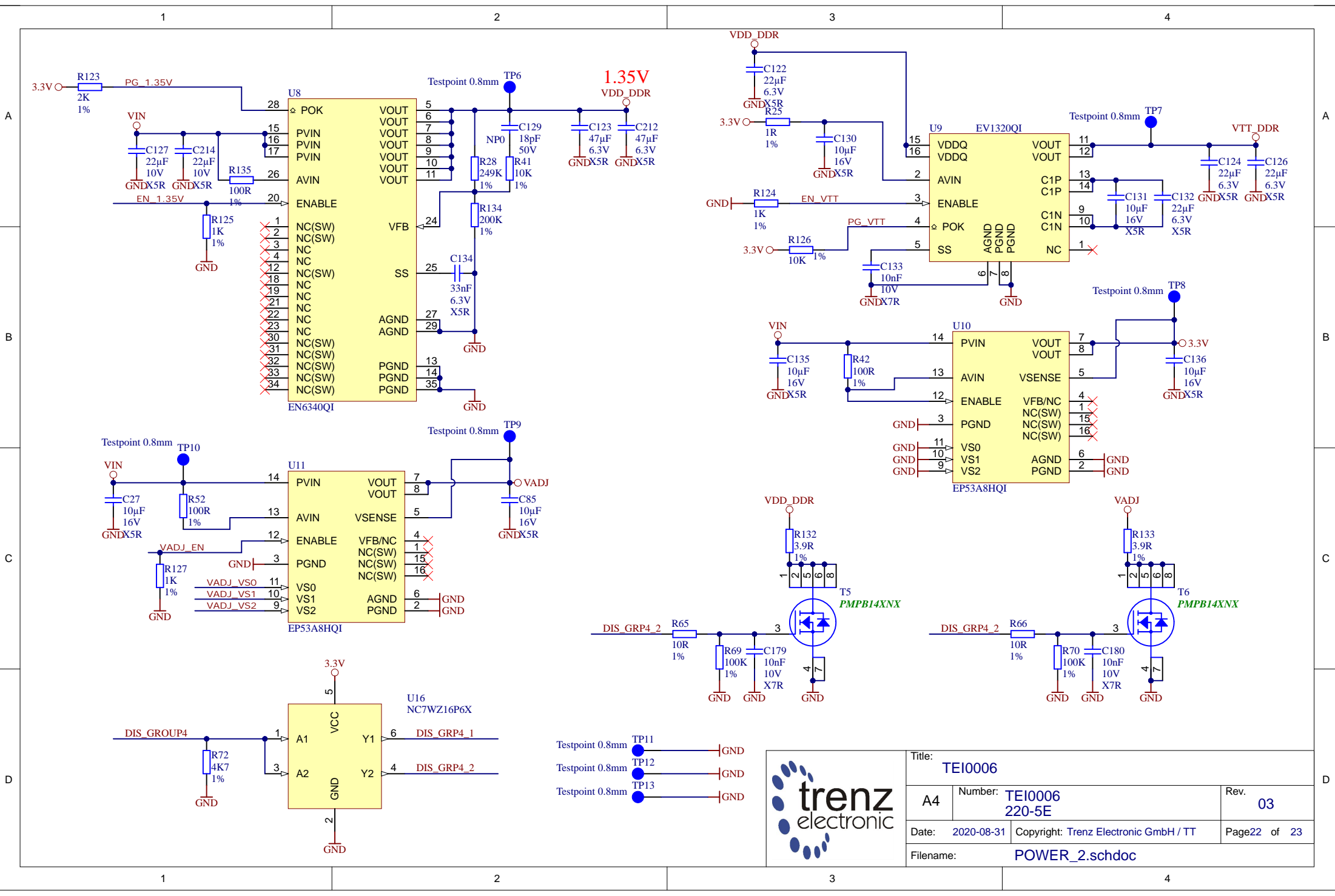
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Title: TEI0006		
A4	Number: TEI0006 220-5E	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page20 of 23
Filename: PWR_CORE.SchDoc		



Title: TEI0006		
A4	Number: TEI0006 220-5E	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH / TT	Page 21 of 23
Filename: POWER_1.schdoc		



Title: TEI0006		
A4	Number: TEI0006 220-5E	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH / TT	Page 22 of 23
Filename: POWER_2.schdoc		

VT: Initial Rev (07.2018)

Changes from REV01 to REV02:


- 1) VT: added MEMS 100MHz clock oscillator to CLKUSR
- 2) VT: remove CLKUSR from J2
- 3) VT: replaced Si510 to SiT8008/CM3225-4pad
- 4) VT: remove DEVCLR\_N from J2, added pull-up
- 5) VT: remove M10\_nSTATUS from J2, added pull-up
- 6) VT: Added optional CryptoAuthentication chip U19 (DNP)

Changes from REV02 to REV03 (08.2020):

- 1) VT: fixed CLK connections ( CLK's from FMC (on Baseboard) directly connected to GXBL1C bank)
- 2) VT: added heatsink
- 3) VT: full upd LIB
- 4) VT: added Legal Notices sheet

2020-12-23

- 5) VY: replaced not available transistors T1-T6 AON2240 to PMPB14XNX

	Title: <b>TEI0006 - Revision changes</b>		
	A4	Number: <b>TEI0006 220-5E</b>	Rev. <b>03</b>
	Date: <b>2020-08-31</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>23</b> of <b>23</b>
	Filename: <b>Revision_Changes.SchDoc</b>		