

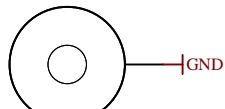
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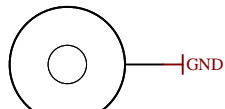
Schematics and other handouts serve for informational purposes only!



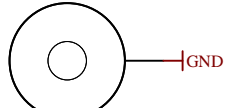
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A4	Number: TEI0006 ALC13A	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH / TT	Page 1 of 23
Filename: Legal Notices Modules.SchDoc		



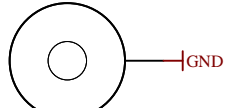
Mount.Hole 3.2mm für Unterlegscheibe



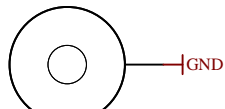
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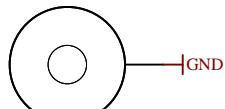
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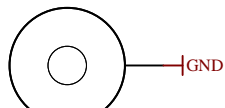
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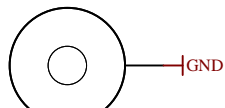
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Mount.Hole 3.2mm für Unterlegscheibe

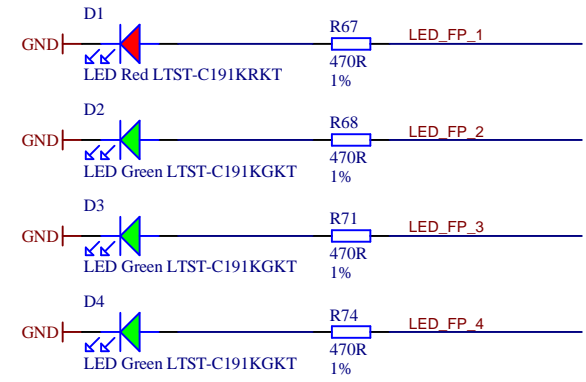
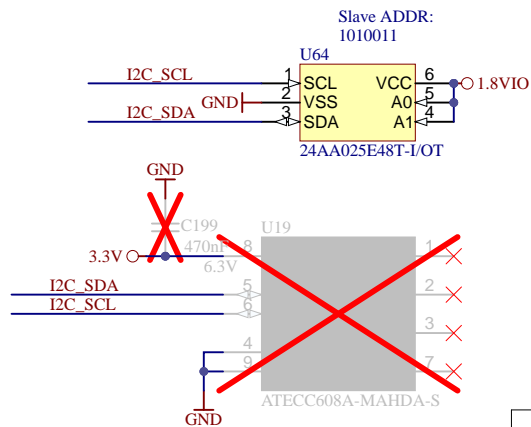
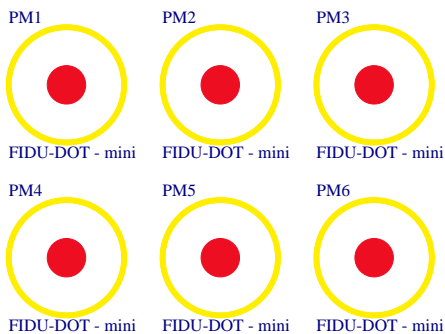


Mount.Hole 3.2mm für Unterlegscheibe



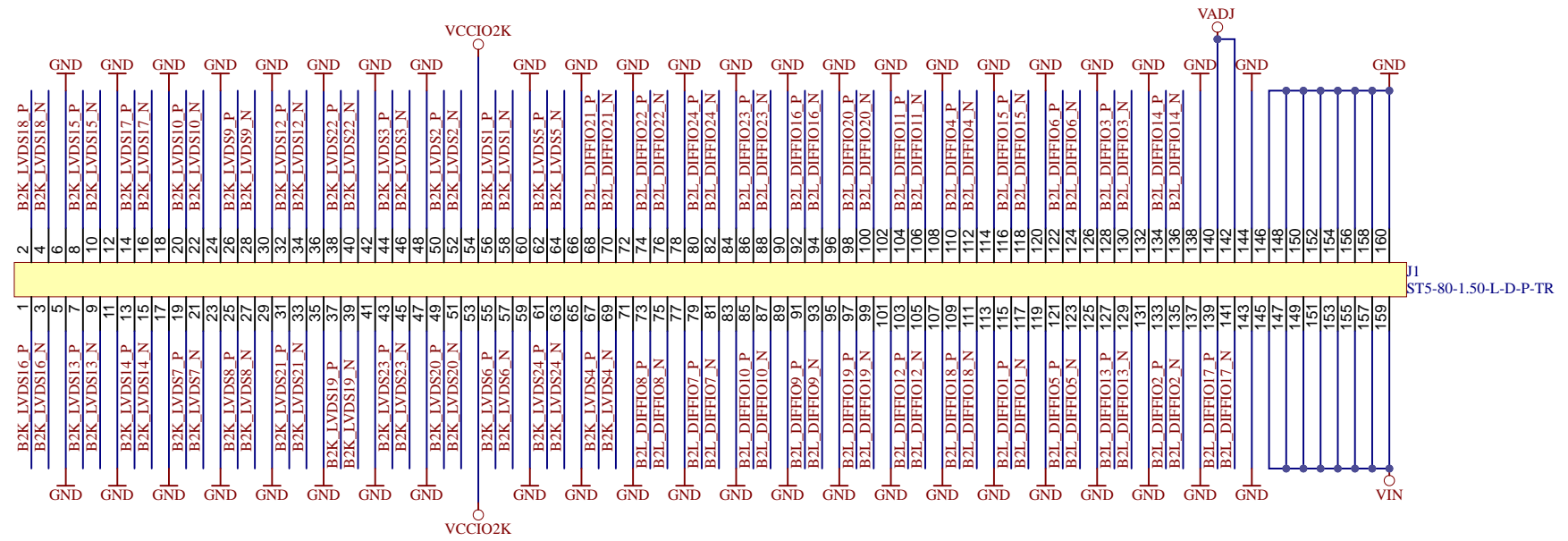
Mount.Hole 3.2mm für Unterlegscheibe


Serial
Serialnummer 6,3 x 6,3mm

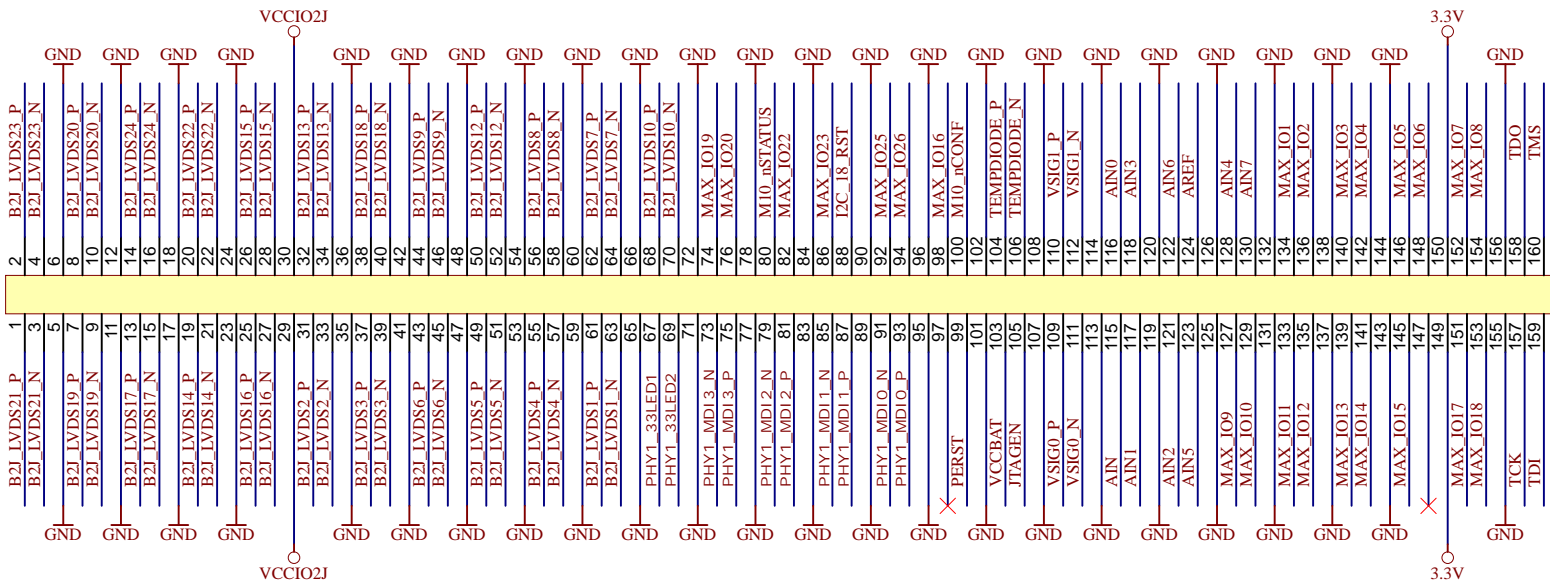


Assembly variant	ALC13A
Created by	VT
Modified by	
Modified at	2021-07-30
SVN Revision	15170

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A4	Number: TEI0006 ALC13A	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH / TT	Page2 of 23
Filename: TEI0006.SchDoc		



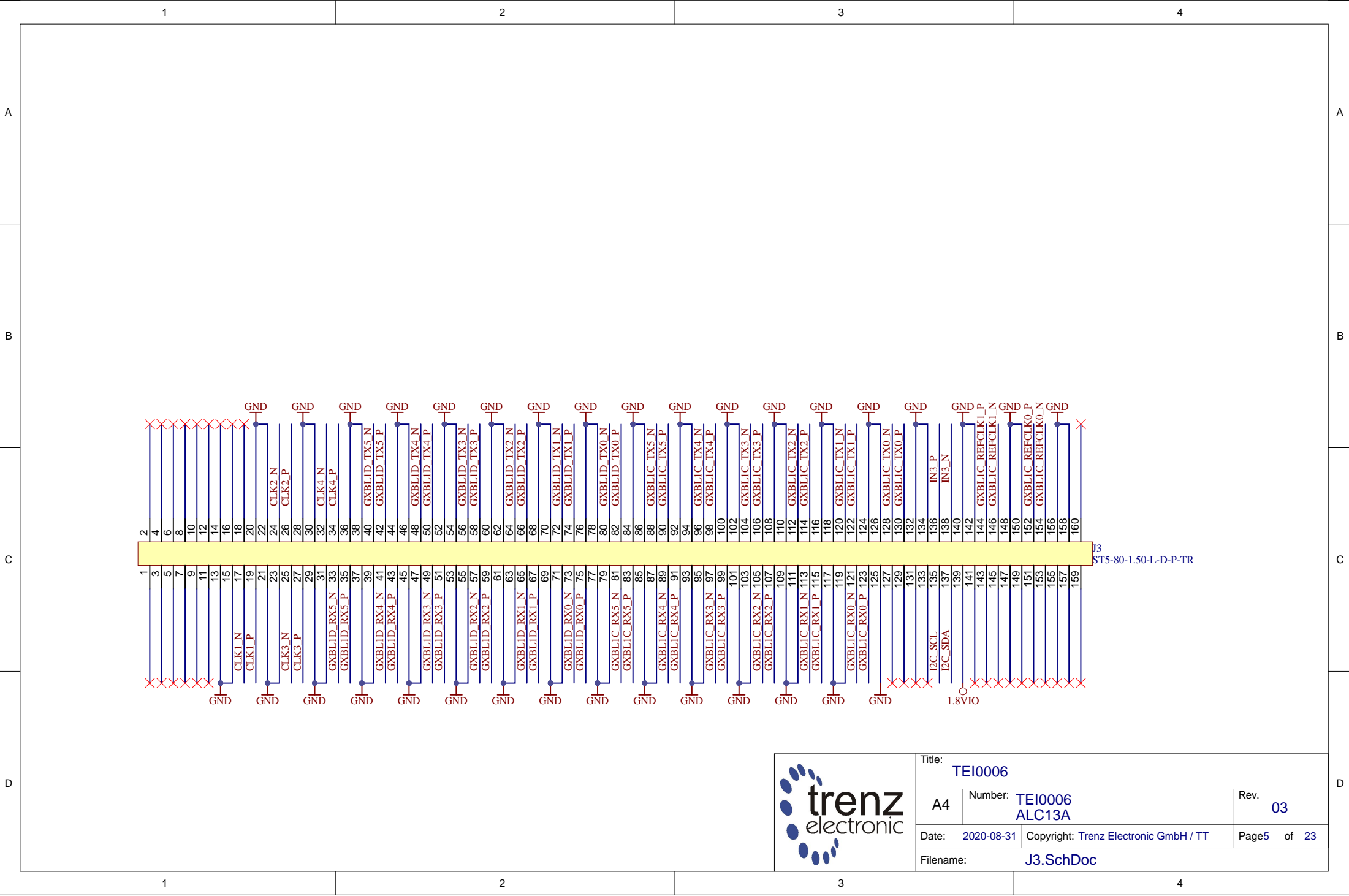
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	A4	Number: TEI0006 ALC13A
	Date: 2020-08-31	Copyright: Trenz Electronic GmbH / TT
	Rev. 03	Page 3 of 23
Filename: J1.SchDoc		




J2
ST5-80-1.50-L-D-P-TR



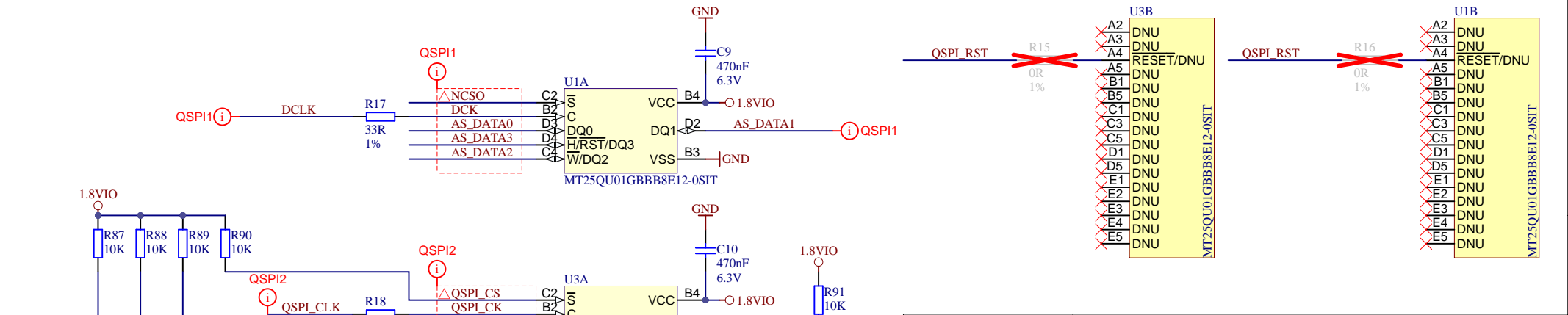
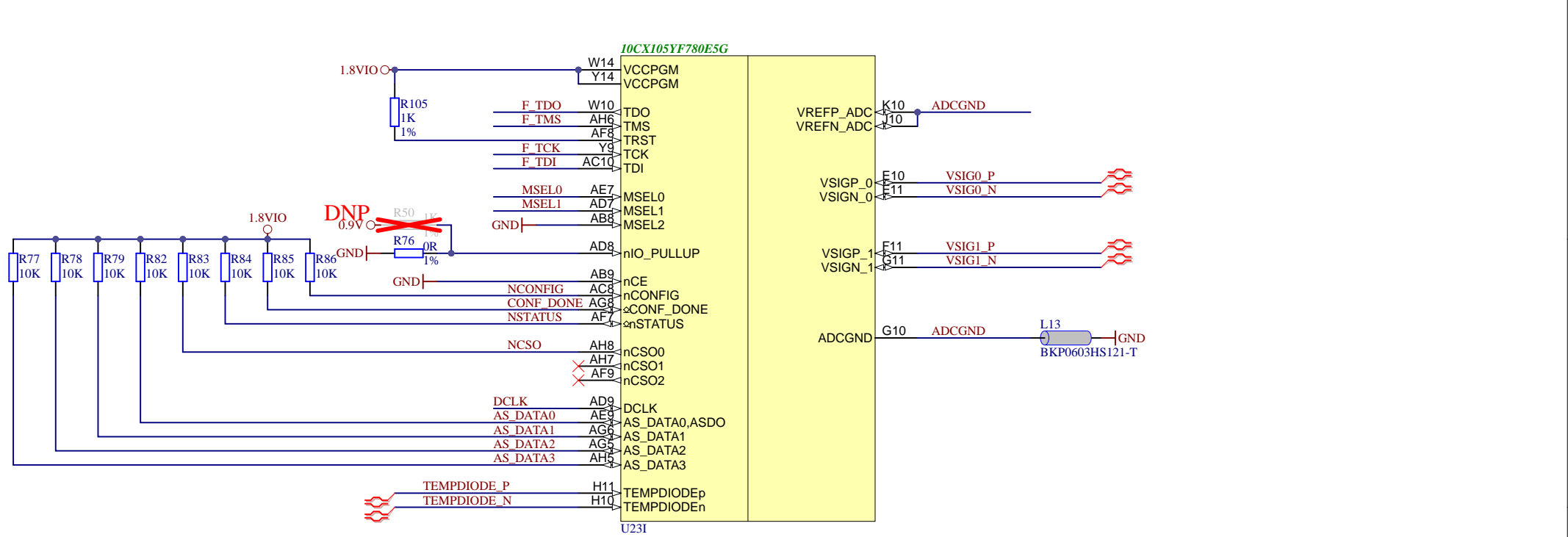
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Date: 2020-08-31	Copyright: Trenz Electronic GmbH / TT	Page 4 of 23
Filename: J2.SchDoc		



J3
ST5-80-1.50-L-D-P-TR

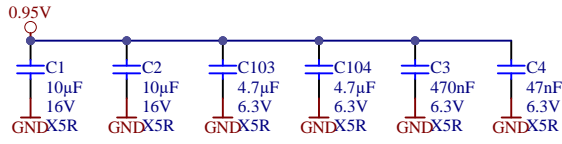


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Date: 2020-08-31	Copyright: Trenz Electronic GmbH / TT	Page5 of 23
Filename: J3.SchDoc		

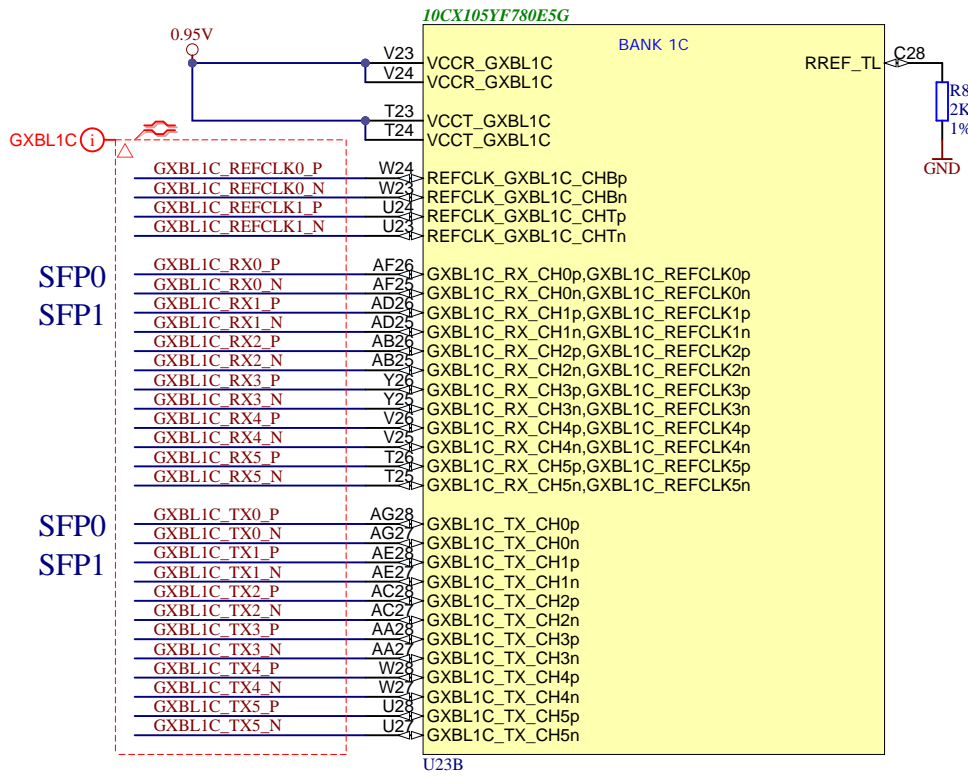
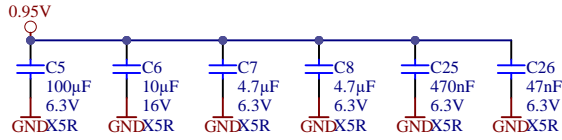



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 6 of 23
Filename: C10GX_CFG.SchDoc		

Placed at VCCT_GXB pins

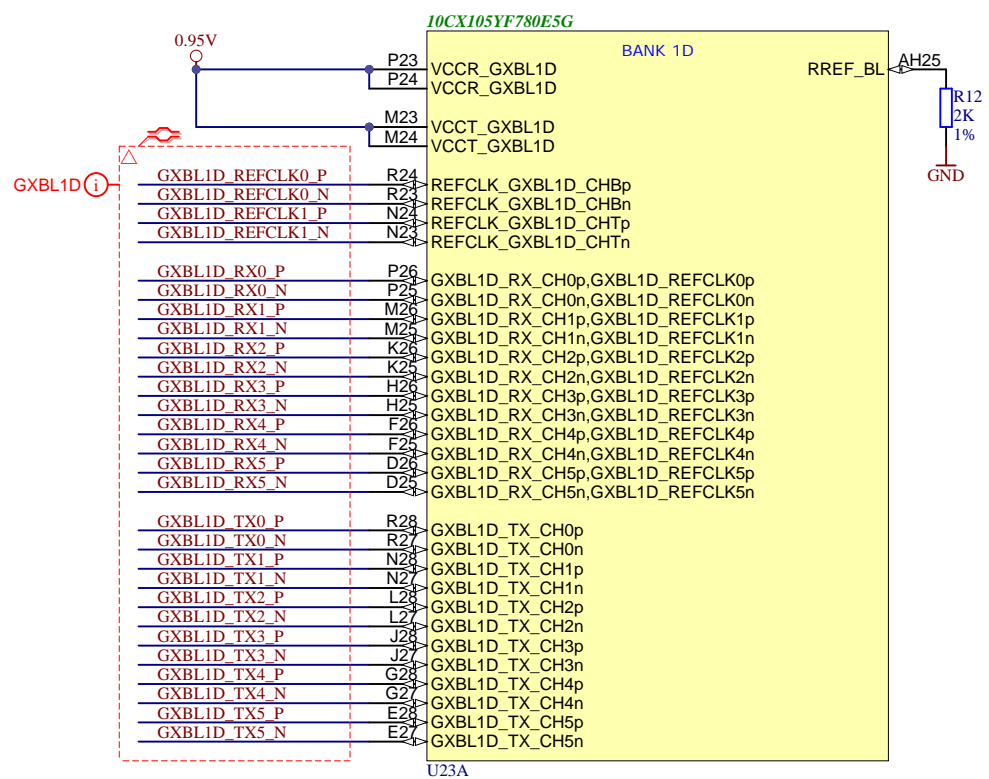


Placed at VCCR_GXB pins

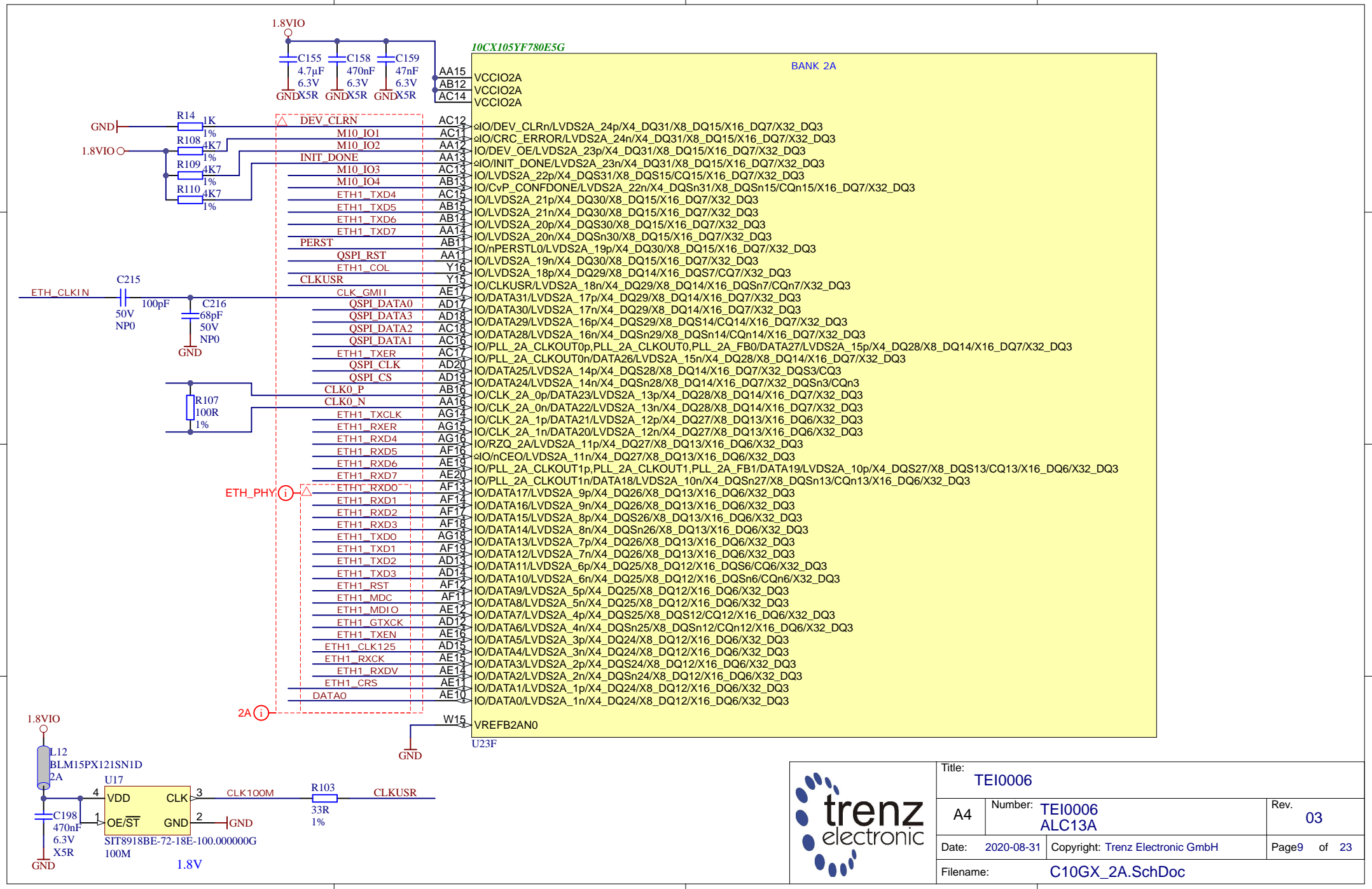



Title: **TEI0006**

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Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 7 of 23
Filename: C10GX_1C.SchDoc		



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	Date: 2020-08-31	Copyright: Trenz Electronic GmbH	
	Page 8 of 23		
Filename: C10GX_1D.SchDoc			



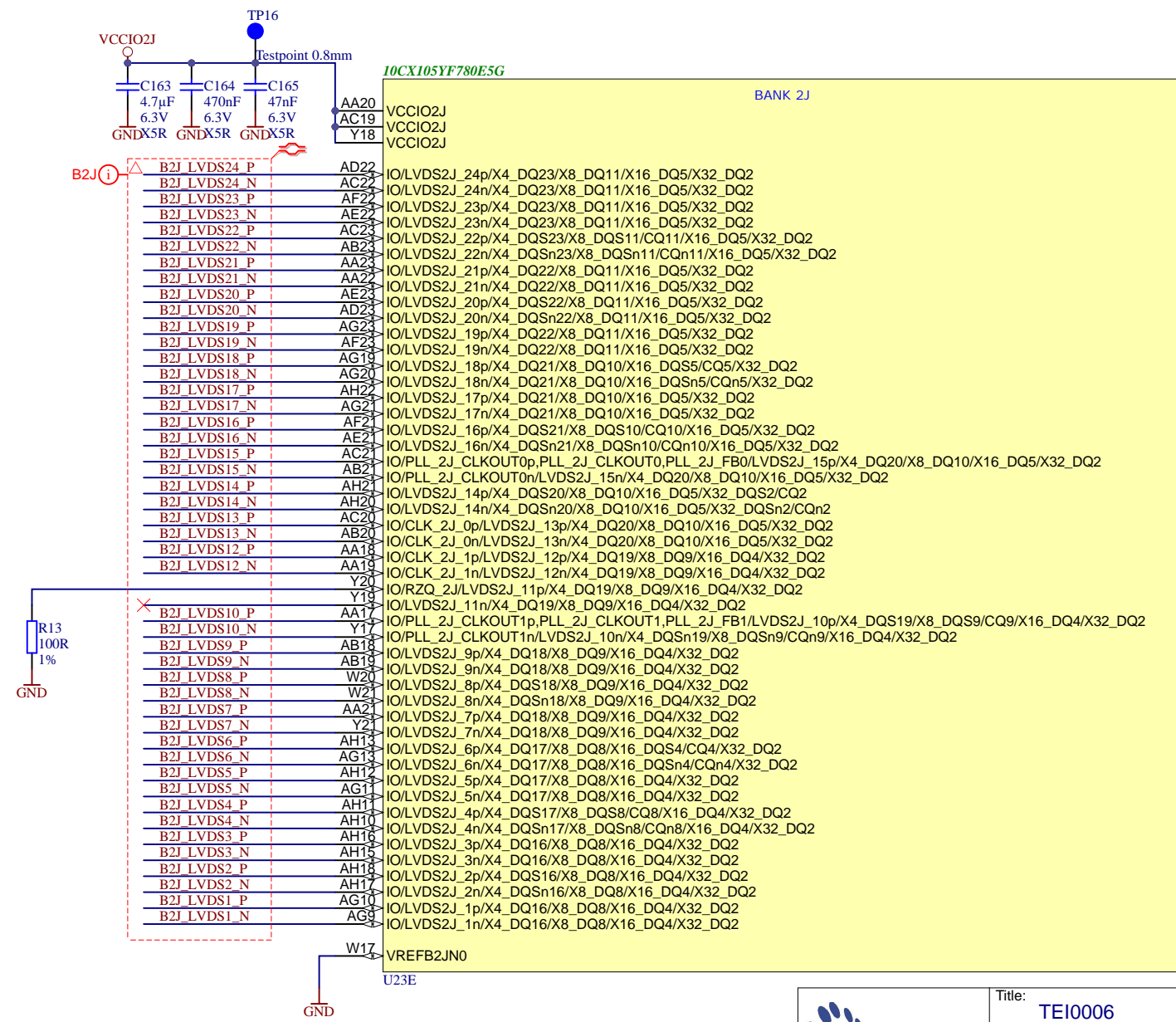
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BANK 2A

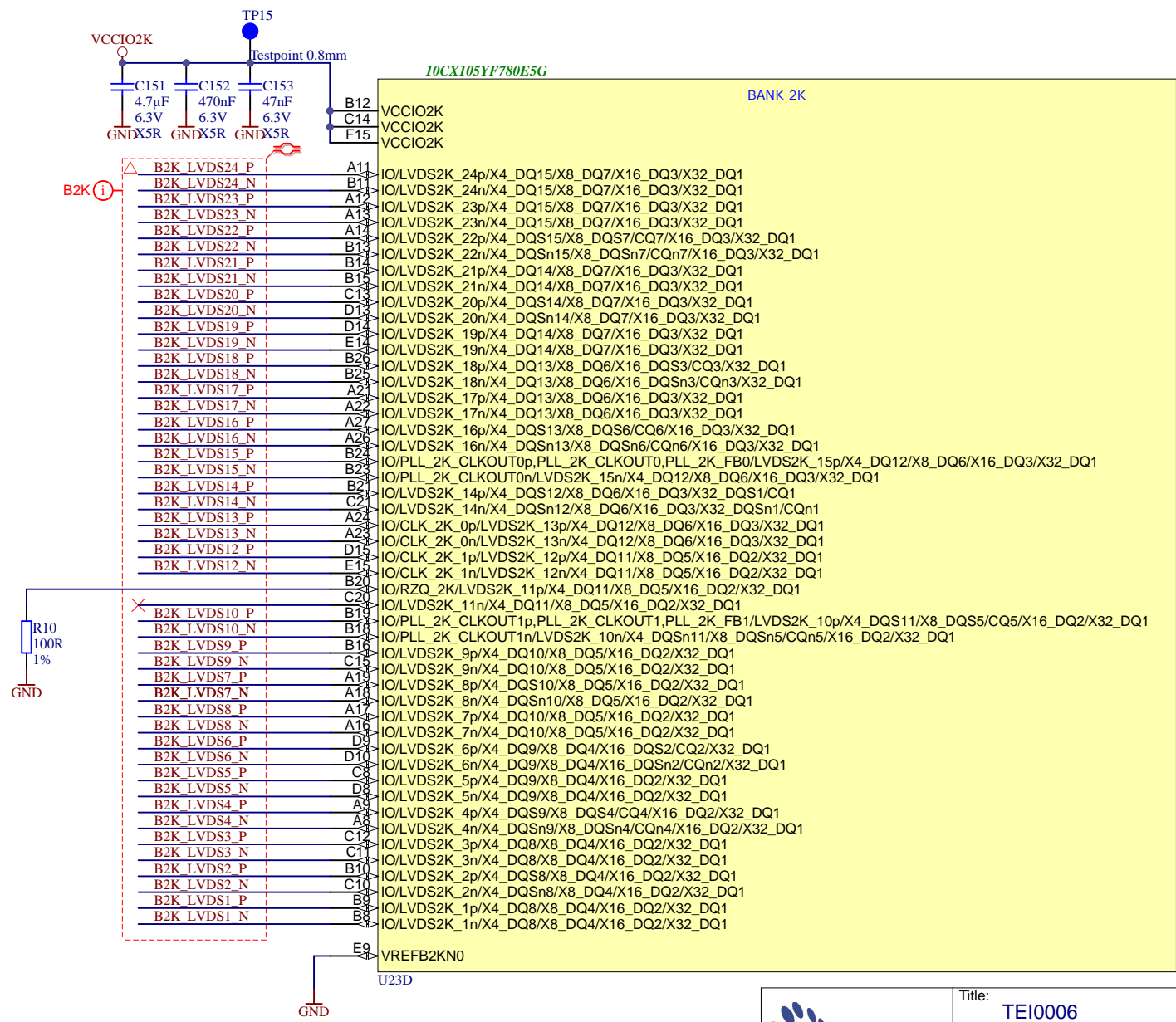
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AB12	VCCIO2A
AC14	VCCIO2A
AC12	IO/DEV_CLRn/LVDS2A_24p/X4_DQ31/X8_DQ15/X16_DQ7/X32_DQ3
AC1	IO/CRC_ERROR/LVDS2A_24n/X4_DQ31/X8_DQ15/X16_DQ7/X32_DQ3
AA13	IO/DEV_OE/LVDS2A_23p/X4_DQ31/X8_DQ15/X16_DQ7/X32_DQ3
AA13	IO/INIT_DONE/LVDS2A_23n/X4_DQ31/X8_DQ15/X16_DQ7/X32_DQ3
AB13	IO/LVDS2A_22p/X4_DQS31/X8_DQS15/CQ15/X16_DQ7/X32_DQ3
AB13	IO/CvP_CONF/DONE/LVDS2A_22n/X4_DQSn31/X8_DQSn15/CQn15/X16_DQ7/X32_DQ3
AC15	IO/LVDS2A_21p/X4_DQ30/X8_DQ15/X16_DQ7/X32_DQ3
AB15	IO/LVDS2A_21n/X4_DQ30/X8_DQ15/X16_DQ7/X32_DQ3
AB14	IO/LVDS2A_20p/X4_DQS30/X8_DQ15/X16_DQ7/X32_DQ3
AB14	IO/LVDS2A_20n/X4_DQSn30/X8_DQ15/X16_DQ7/X32_DQ3
AA14	IO/mPERSTL0/LVDS2A_19p/X4_DQ30/X8_DQ15/X16_DQ7/X32_DQ3
AA14	IO/LVDS2A_19n/X4_DQ30/X8_DQ15/X16_DQ7/X32_DQ3
Y16	IO/LVDS2A_18p/X4_DQ29/X8_DQ14/X16_DQS7/CQ7/X32_DQ3
Y15	IO/LVDS2A_18n/X4_DQ29/X8_DQ14/X16_DQS7/CQn7/X32_DQ3
AE17	IO/CLKUSR/LVDS2A_18n/X4_DQ29/X8_DQ14/X16_DQS7/CQn7/X32_DQ3
AD17	IO/DATA31/LVDS2A_17p/X4_DQ29/X8_DQ14/X16_DQ7/X32_DQ3
AD18	IO/DATA30/LVDS2A_17n/X4_DQ29/X8_DQ14/X16_DQ7/X32_DQ3
AC18	IO/DATA29/LVDS2A_16p/X4_DQS29/X8_DQS14/CQ14/X16_DQ7/X32_DQ3
AC16	IO/DATA28/LVDS2A_16n/X4_DQSn29/X8_DQSn14/CQn14/X16_DQ7/X32_DQ3
AC17	IO/PLL_2A_CLKOUT0p,PLL_2A_CLKOUT0,PLL_2A_FB0/DATA27/LVDS2A_15p/X4_DQ28/X8_DQ14/X16_DQ7/X32_DQ3
AD27	IO/PLL_2A_CLKOUT0n/DATA26/LVDS2A_15n/X4_DQ28/X8_DQ14/X16_DQ7/X32_DQ3
AD27	IO/DATA25/LVDS2A_14p/X4_DQS28/X8_DQ14/X16_DQ7/X32_DQS3/CQ3
AD19	IO/DATA24/LVDS2A_14n/X4_DQSn28/X8_DQ14/X16_DQ7/X32_DQSn3/CQn3
AB16	IO/CLK_2A_0p/DATA23/LVDS2A_13p/X4_DQ28/X8_DQ14/X16_DQ7/X32_DQ3
AA16	IO/CLK_2A_0n/DATA22/LVDS2A_13n/X4_DQ28/X8_DQ14/X16_DQ7/X32_DQ3
AG17	IO/CLK_2A_1p/DATA21/LVDS2A_12p/X4_DQ27/X8_DQ13/X16_DQ6/X32_DQ3
AG16	IO/CLK_2A_1n/DATA20/LVDS2A_12n/X4_DQ27/X8_DQ13/X16_DQ6/X32_DQ3
AE19	IO/RZQ_2A/LVDS2A_11p/X4_DQ27/X8_DQ13/X16_DQ6/X32_DQ3
AE19	IO/nCEO/LVDS2A_11n/X4_DQ27/X8_DQ13/X16_DQ6/X32_DQ3
AE27	IO/PLL_2A_CLKOUT1p,PLL_2A_CLKOUT1,PLL_2A_FB1/DATA19/LVDS2A_10p/X4_DQS27/X8_DQS13/CQ13/X16_DQ6/X32_DQ3
AE27	IO/PLL_2A_CLKOUT1n/DATA18/LVDS2A_10n/X4_DQSn27/X8_DQSn13/CQn13/X16_DQ6/X32_DQ3
AF17	IO/DATA17/LVDS2A_9p/X4_DQ26/X8_DQ13/X16_DQ6/X32_DQ3
AF17	IO/DATA16/LVDS2A_9n/X4_DQ26/X8_DQ13/X16_DQ6/X32_DQ3
AF18	IO/DATA15/LVDS2A_8p/X4_DQS26/X8_DQ13/X16_DQ6/X32_DQ3
AF18	IO/DATA14/LVDS2A_8n/X4_DQSn26/X8_DQ13/X16_DQ6/X32_DQ3
AG19	IO/DATA13/LVDS2A_7p/X4_DQ26/X8_DQ13/X16_DQ6/X32_DQ3
AF19	IO/DATA12/LVDS2A_7n/X4_DQ26/X8_DQ13/X16_DQ6/X32_DQ3
AD13	IO/DATA11/LVDS2A_6p/X4_DQ25/X8_DQ12/X16_DQS6/CQ6/X32_DQ3
AF17	IO/DATA10/LVDS2A_6n/X4_DQ25/X8_DQ12/X16_DQSn6/CQn6/X32_DQ3
AF17	IO/DATA9/LVDS2A_5p/X4_DQ25/X8_DQ12/X16_DQ6/X32_DQ3
AF17	IO/DATA8/LVDS2A_5n/X4_DQ25/X8_DQ12/X16_DQ6/X32_DQ3
AE17	IO/DATA7/LVDS2A_4p/X4_DQS25/X8_DQS12/CQ12/X16_DQ6/X32_DQ3
AD12	IO/DATA6/LVDS2A_4n/X4_DQSn25/X8_DQSn12/CQn12/X16_DQ6/X32_DQ3
AE16	IO/DATA5/LVDS2A_3p/X4_DQ24/X8_DQ12/X16_DQ6/X32_DQ3
AD11	IO/DATA4/LVDS2A_3n/X4_DQ24/X8_DQ12/X16_DQ6/X32_DQ3
AE15	IO/DATA3/LVDS2A_2p/X4_DQS24/X8_DQ12/X16_DQ6/X32_DQ3
AE14	IO/DATA2/LVDS2A_2n/X4_DQSn24/X8_DQ12/X16_DQ6/X32_DQ3
AE11	IO/DATA1/LVDS2A_1p/X4_DQ24/X8_DQ12/X16_DQ6/X32_DQ3
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U23F	



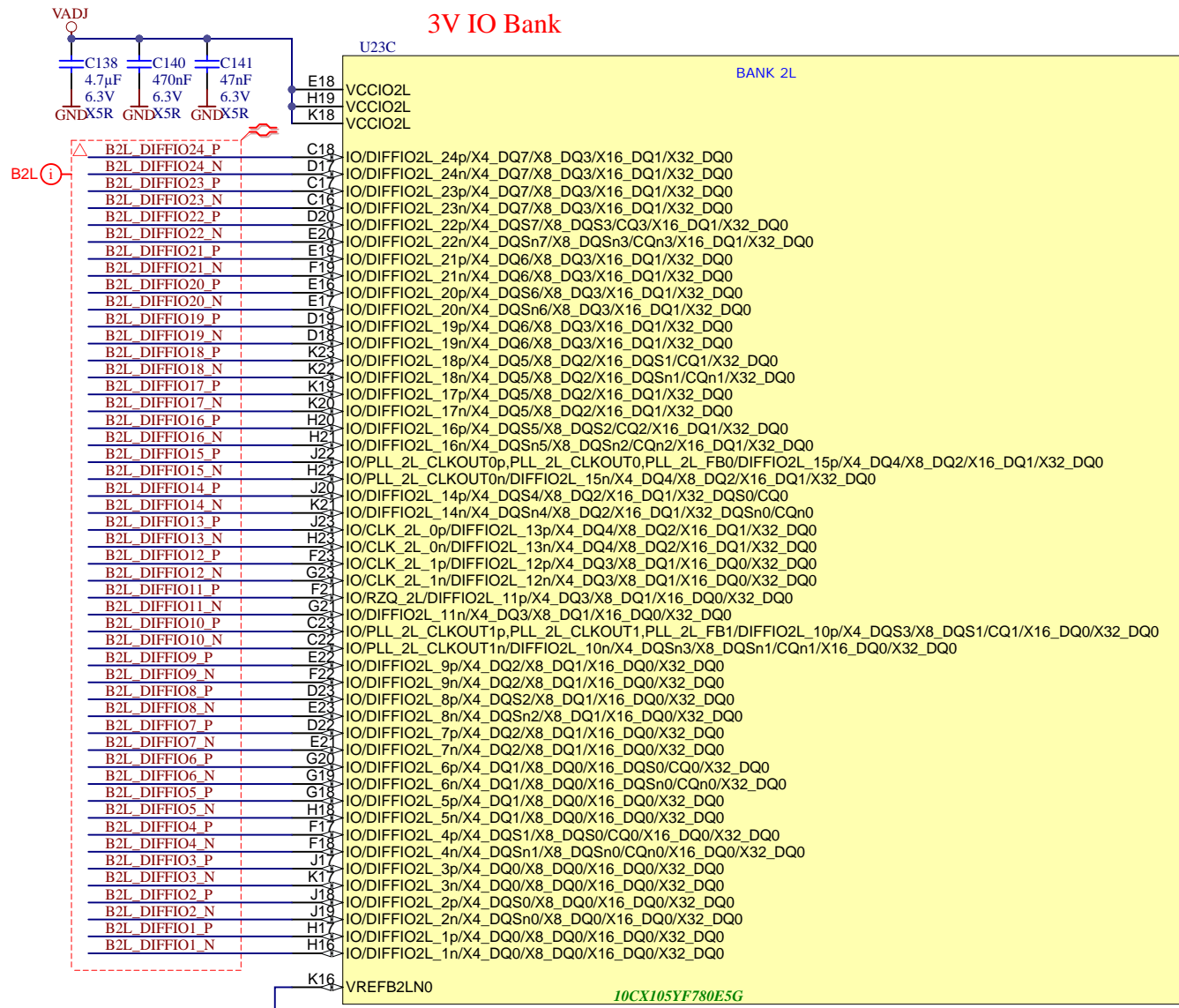
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Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 9 of 23
Filename: C10GX_2A.SchDoc		



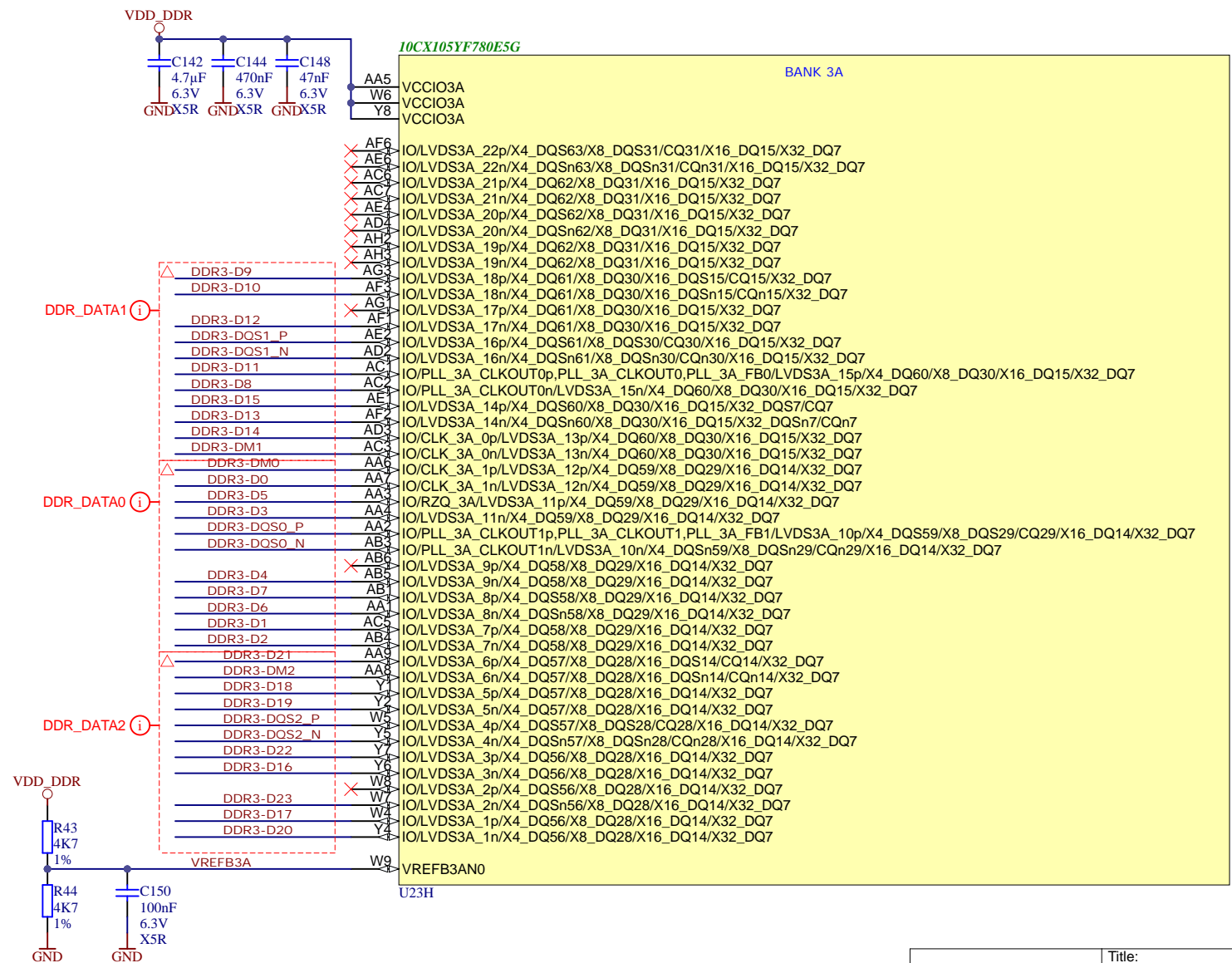

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Filename: C10GX_2J.SchDoc		



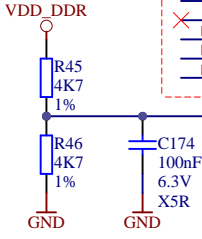
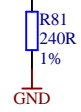
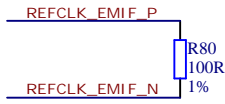
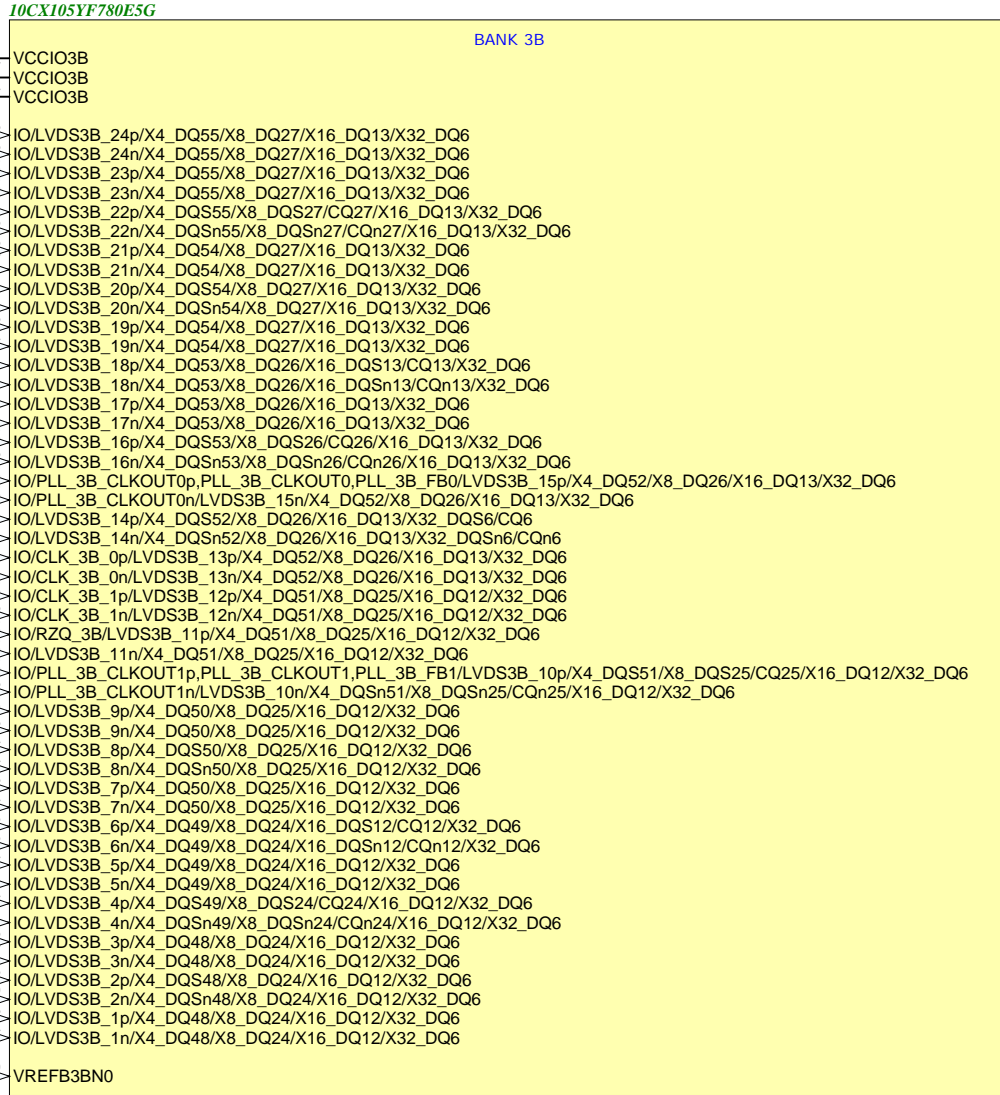
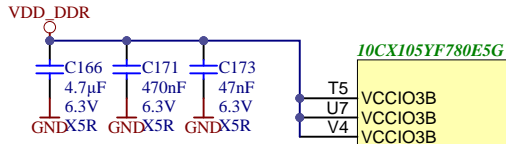
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Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 11 of 23
Filename: C10GX_2K.SchDoc		



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Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 12 of 23
Filename: C10GX_2L.SchDoc		

Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 13 of 23
Filename: C10GX_3A.SchDoc		



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 14 of 23
Filename: C10GX_3B.SchDoc		

A

B

C

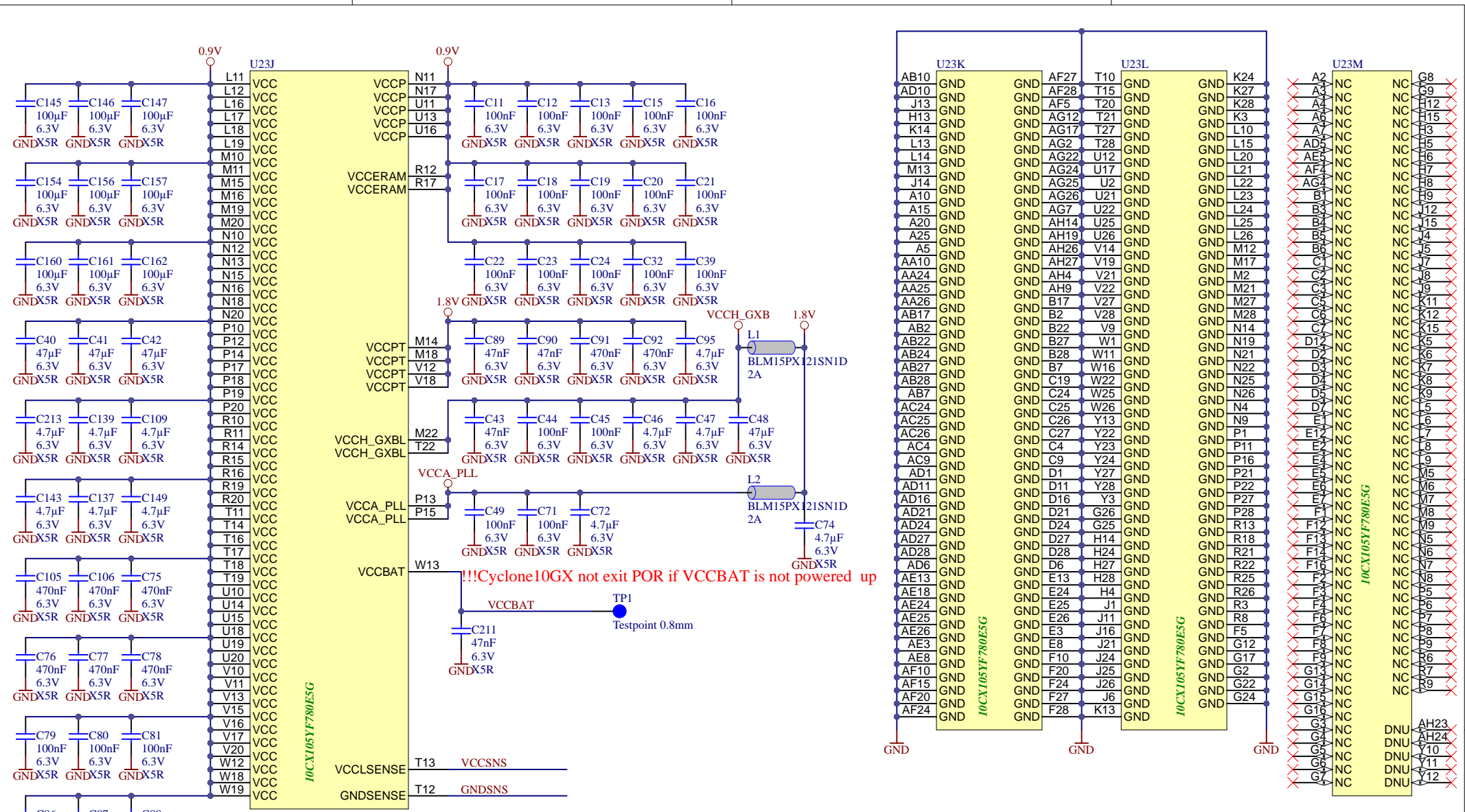
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A

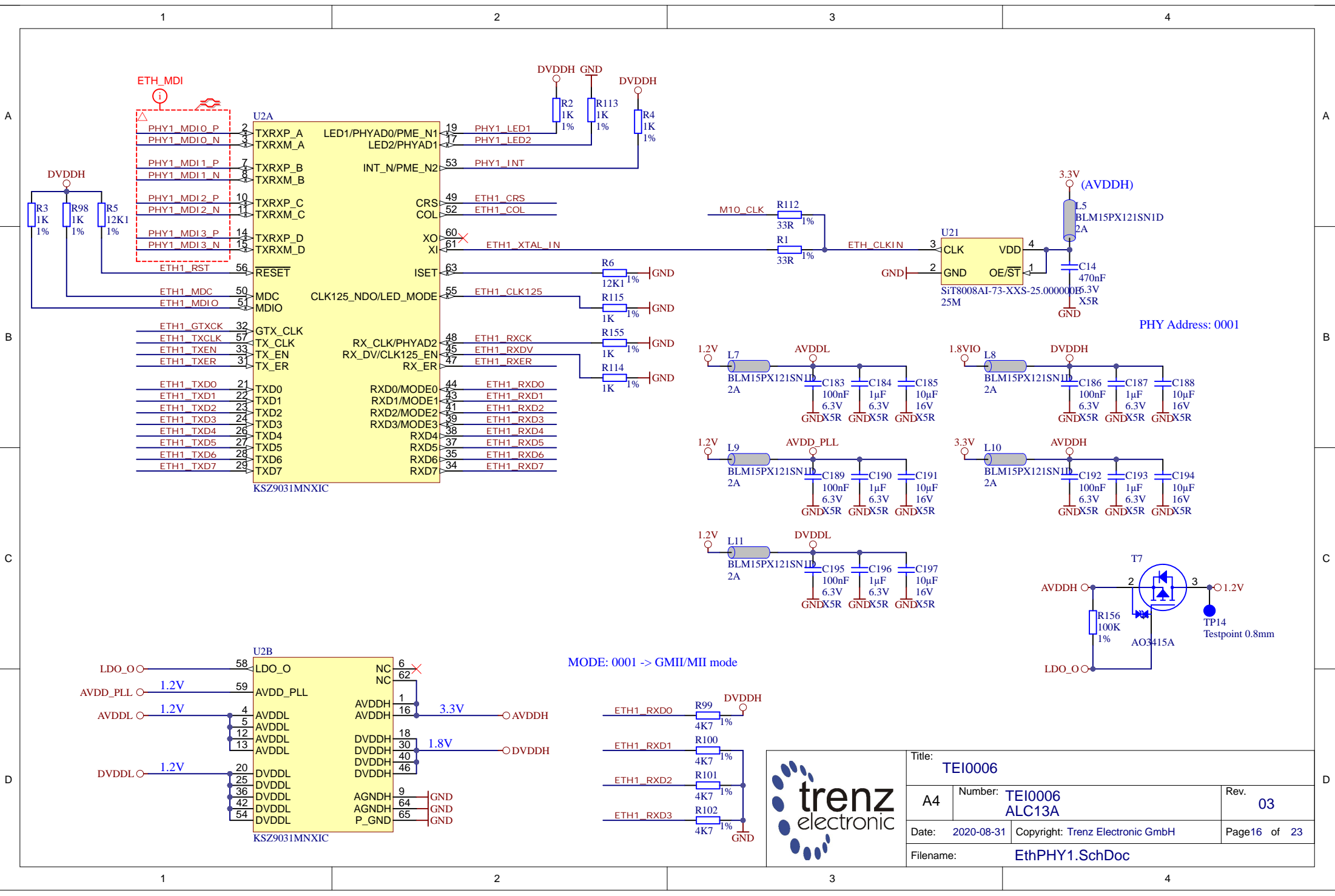
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C

D



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Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 15 of 23
Filename: C10GX_PWR.SchDoc		

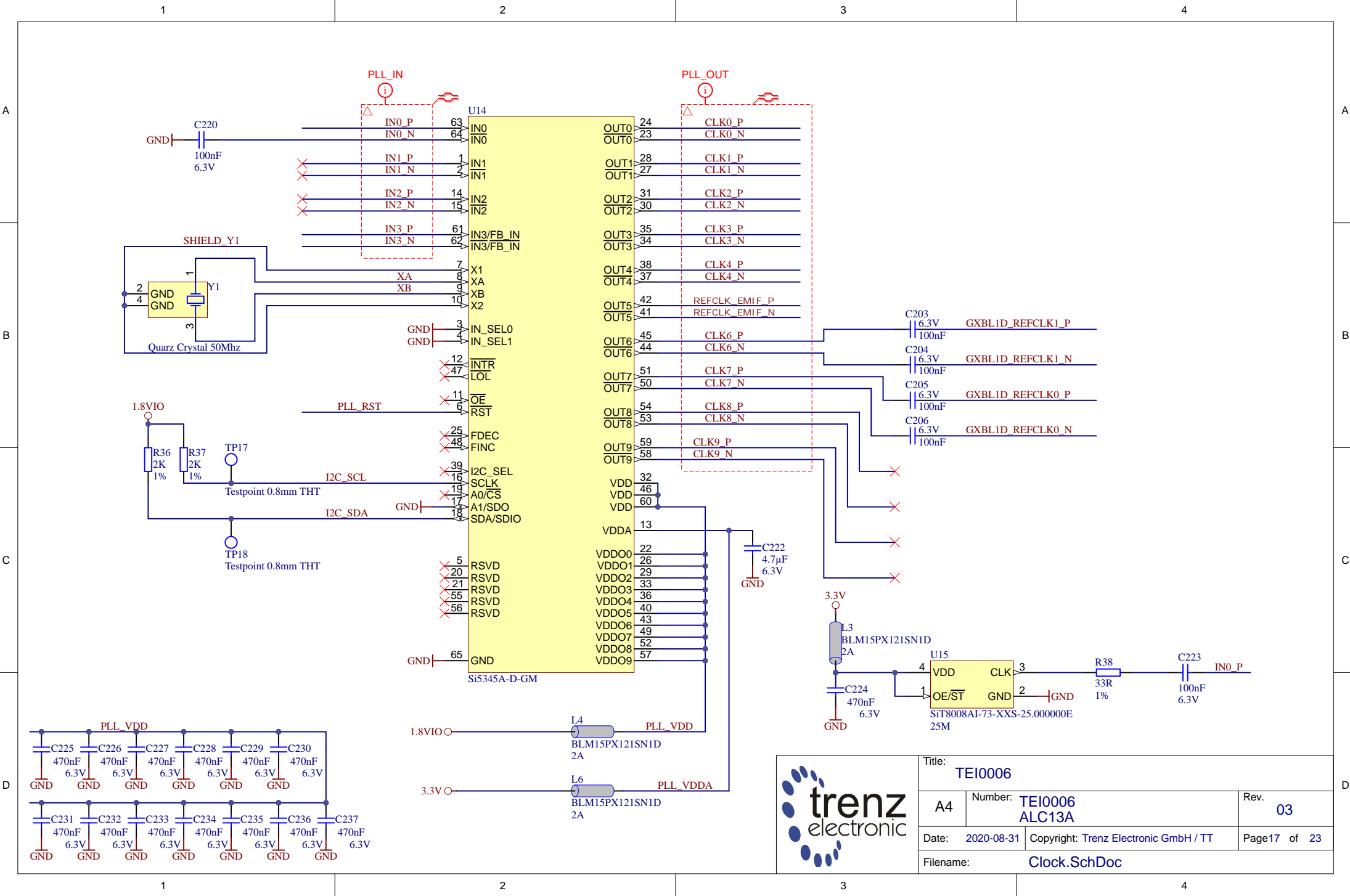


PHY Address: 0001

MODE: 0001 -> GMII/MII mode



Title: TEI0006		
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Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 16 of 23
Filename: EthPHY1.SchDoc		



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH / TT	Page 17 of 23
Filename: Clock.SchDoc		

A

A

B

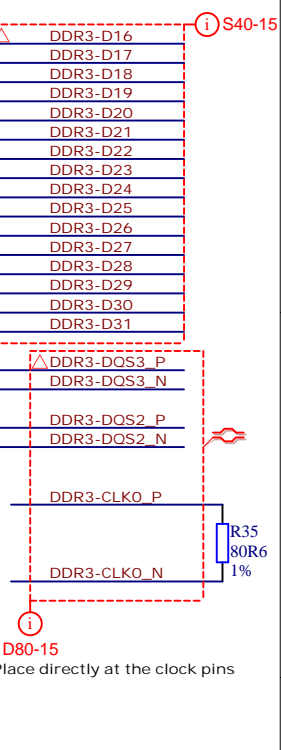
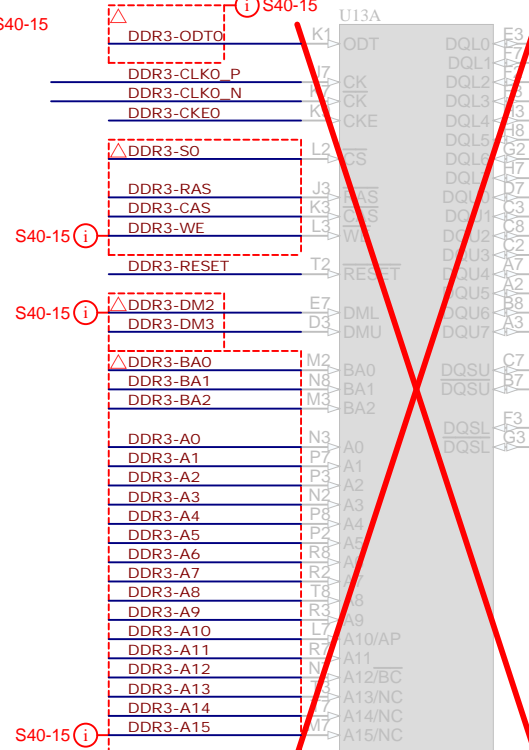
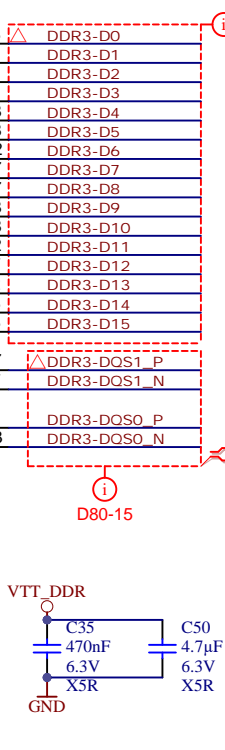
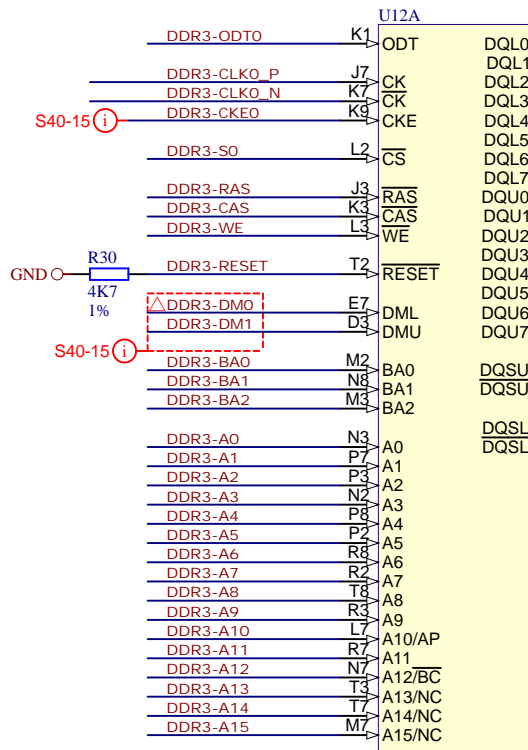
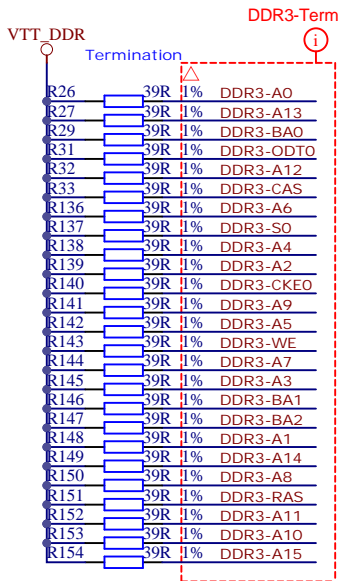
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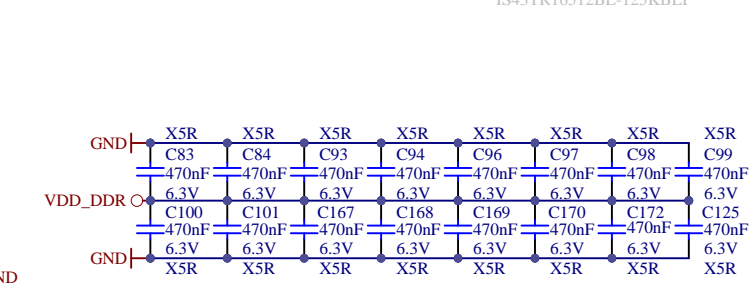
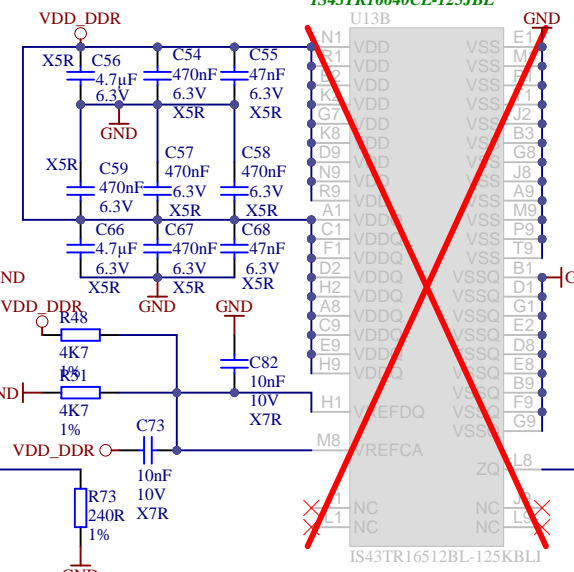
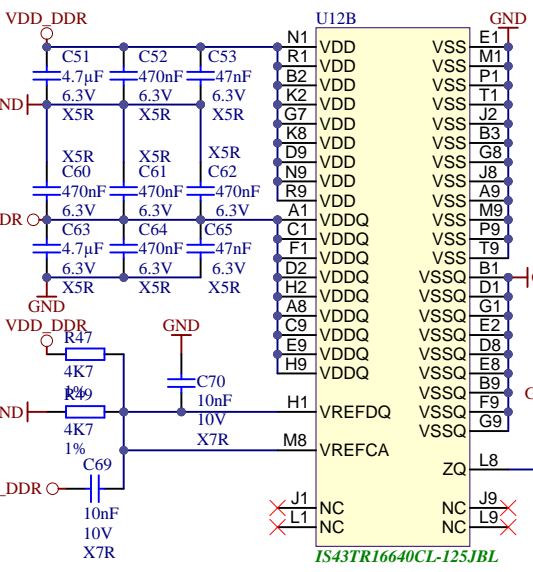
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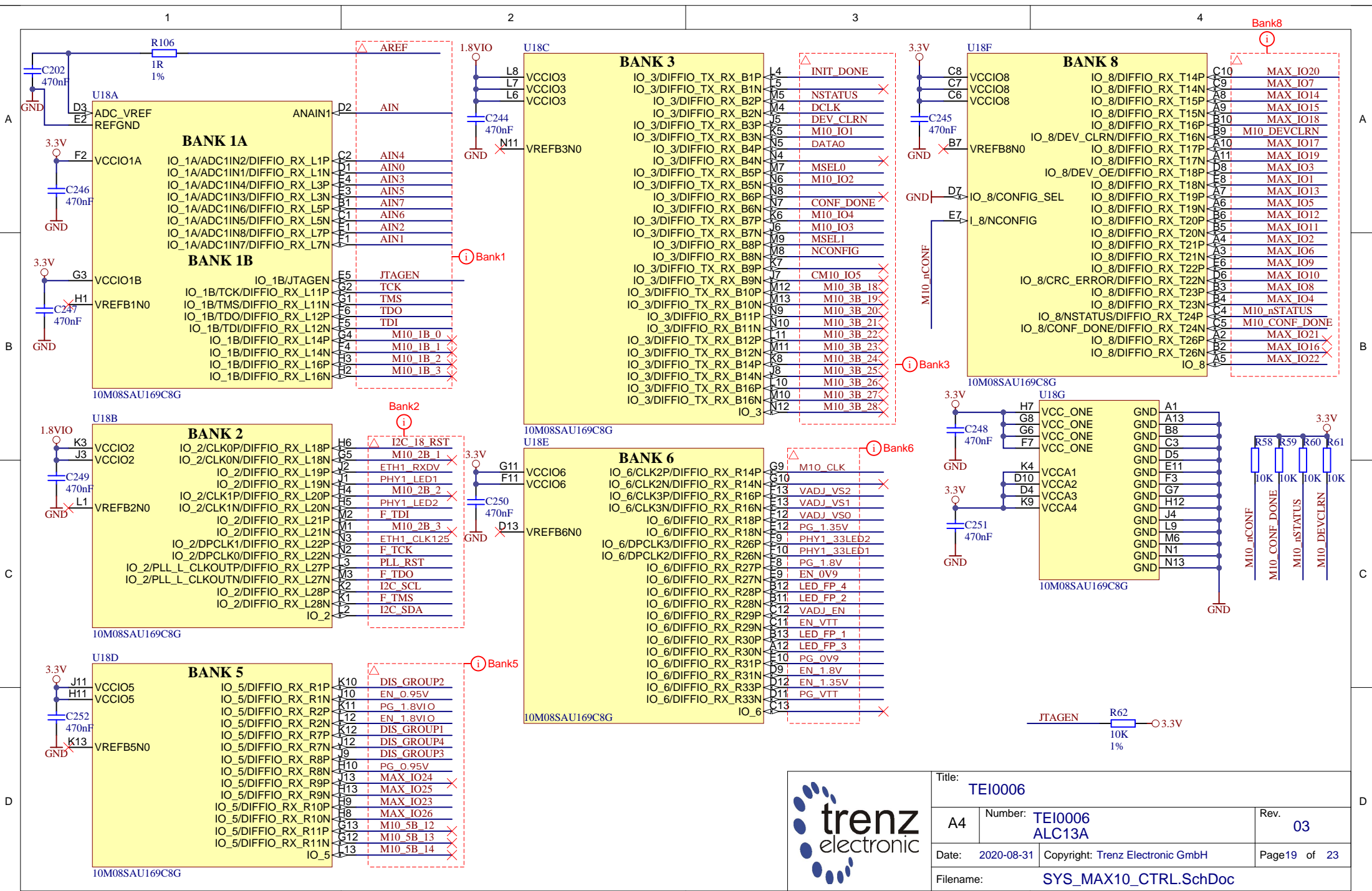
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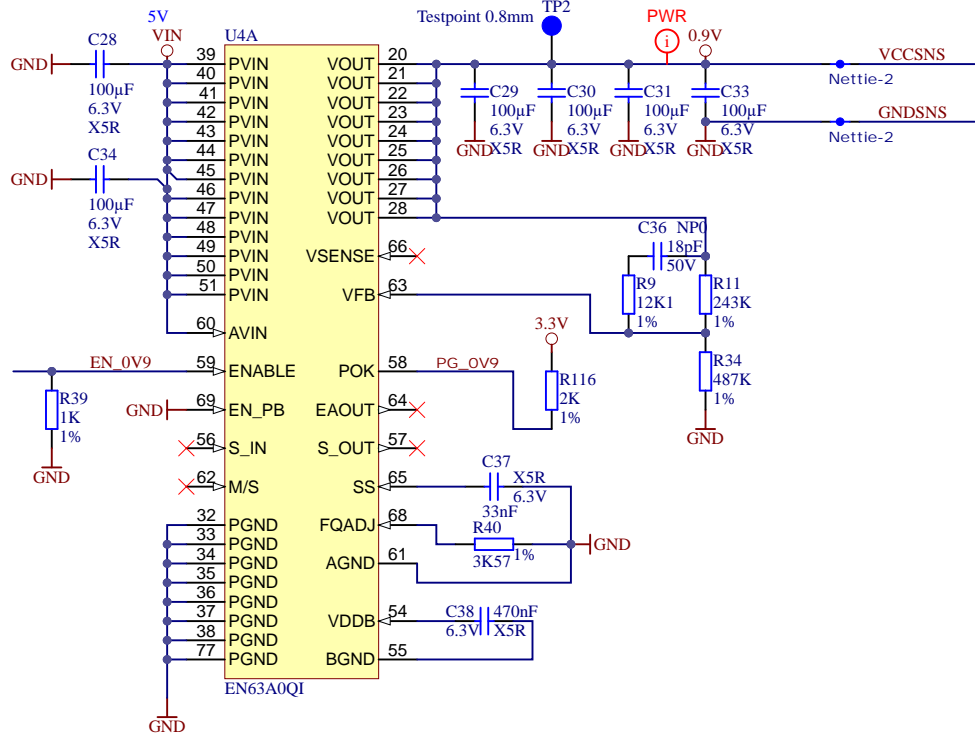
Place directly at the clock pins



Title: TEI0006		
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Date: 2020-08-31	Copyright: 2013 Trenz Electronic GmbH	Page 18 of 23
Filename: DDR3-RAM1.SchDoc		

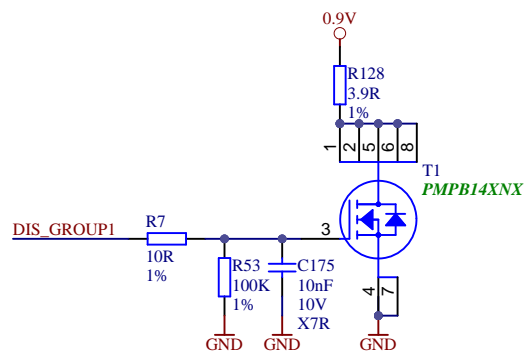



Title: TEI0006		
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Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 19 of 23
Filename: SYS_MAX10_CTRL.SchDoc		

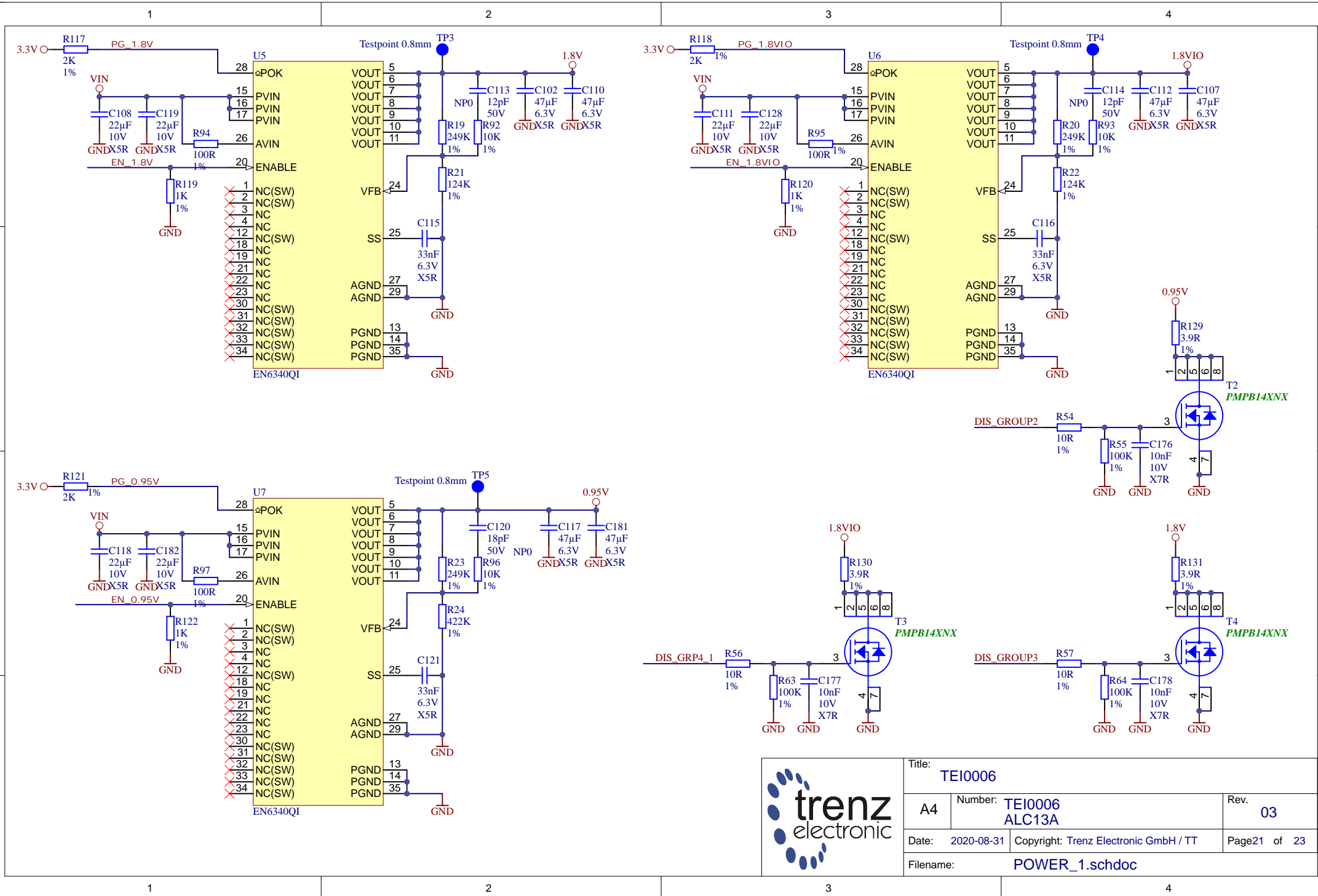


U4B		
1	NC	17
2	NC	18
3	NC	19
4	NC	29
5	NC	30
6	NC(SW)	31
7	NC(SW)	52
8	NC	53
9	NC	67
10	NC	70
11	NC(SW)	71
12	NC(SW)	72
13	NC	73
14	NC	74
15	NC	75
16	NC	76

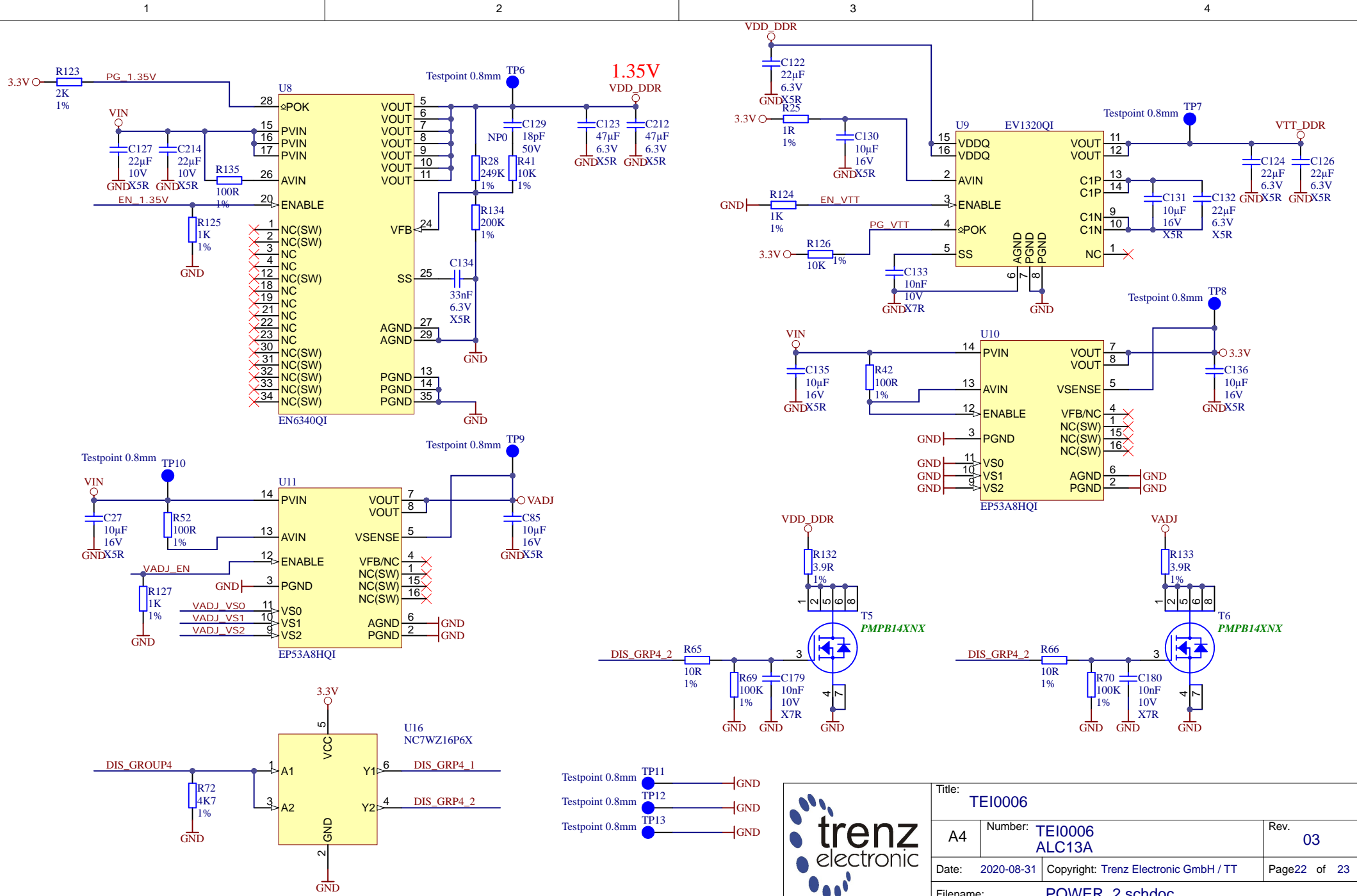
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	A4	Number: TEI0006 ALC13A	Rev. 03
	Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 20 of 23
	Filename: PWR_CORE.SchDoc		



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH / TT	Page 21 of 23
Filename: POWER_1.schdoc		



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH / TT	Page 22 of 23
Filename: POWER_2.schdoc		

VT: Initial Rev (07.2018)

Changes from REV01 to REV02:


- 1) VT: added MEMS 100MHz clock oscillator to CLKUSR
- 2) VT: remove CLKUSR from J2
- 3) VT: replaced Si510 to SiT8008/CM3225-4pad
- 4) VT: remove DEVCLRn from J2, added pull-up
- 5) VT: remove M10_nSTATUS from J2, added pull-up
- 6) VT: Added optional CryptoAuthentication chip U19 (DNP)

Changes from REV02 to REV03 (08.2020):

- 1) VT: fixed CLK connections (CLK's from FMC (on Baseboard) directly connected to GXBL1C bank)
- 2) VT: added heatsink
- 3) VT: full upd LIB
- 4) VT: added Legal Notices sheet

2020-12-23

- 5) VY: replaced not available transistors T1-T6 AON2240 to PMPB14XNX

	Title: TEI0006 - Revision changes		
	A4	Number: TEI0006 ALC13A	Rev. 03
	Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 23 of 23
	Filename: Revision_Changes.SchDoc		