
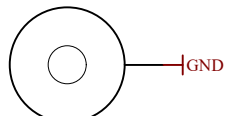


Regarding the usage of our schematics and alike documentation for Trenz module TEI0006.

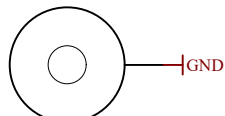
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Schematics and other handouts serve for informational purposes only!

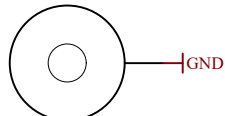
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	Date: 2020-08-31	Copyright: Trenz Electronic GmbH / TT	Page 1 of 23
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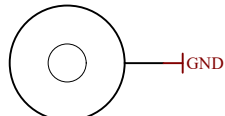
Mount.Hole 3.2mm für Unterlegscheibe



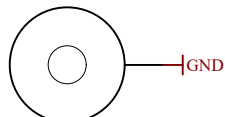
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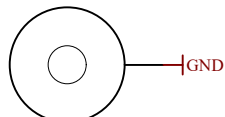
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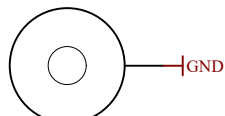
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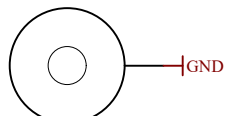
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Mount.Hole 3.2mm für Unterlegscheibe

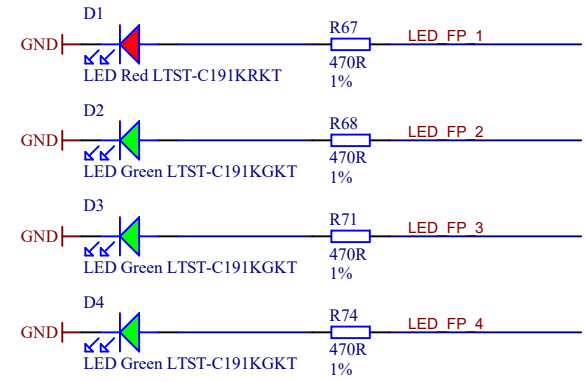
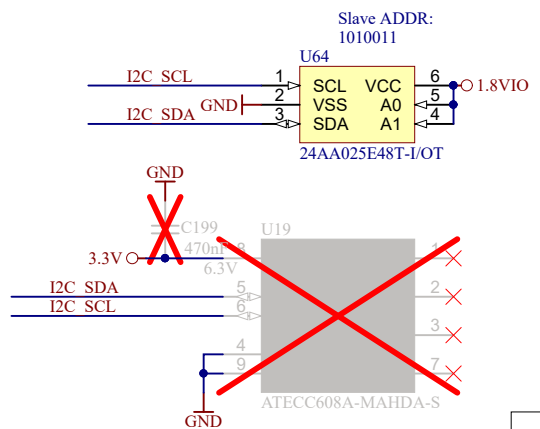
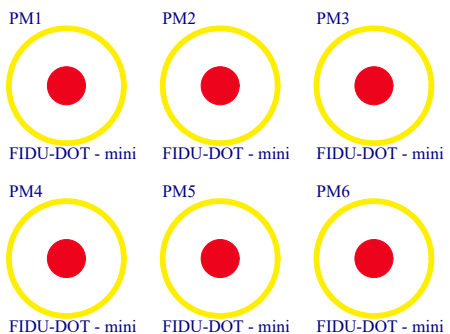


Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe

Serial
Serialnummer 6,3 x 6,3mm



J4
ATS-X53290G-C1-R0 NOT CHECKED!!!

Assembly variant	APC13-R
Created by	VY
Modified by	
Modified at	2020-12-22
SVN Revision	14946



Title: TEI0006		
A4	Number: TEI0006 APC13-R	Rev. 03
Date: 2020-08-31	Copyright: Trenz Electronic GmbH / TT	Page2 of 23
Filename: TEI0006.SchDoc		

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A

A

B

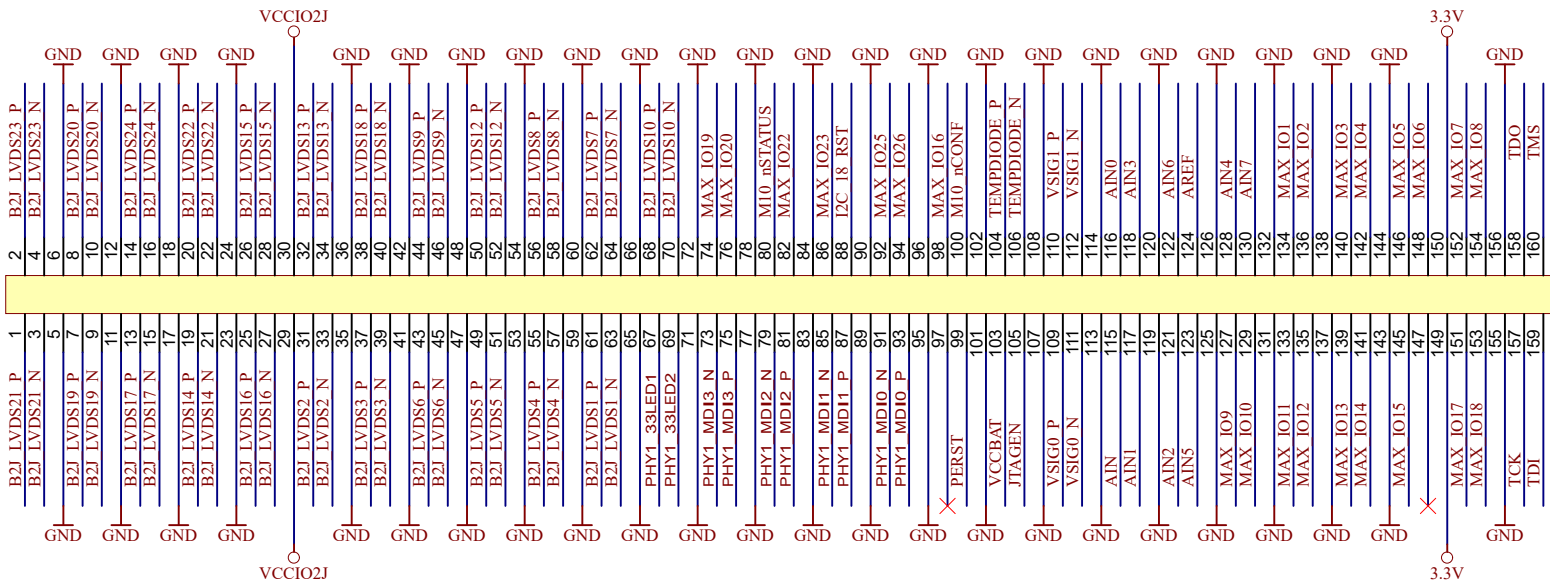
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C

C

D

D



J2
ST5-80-1.50-L-D-P-TR



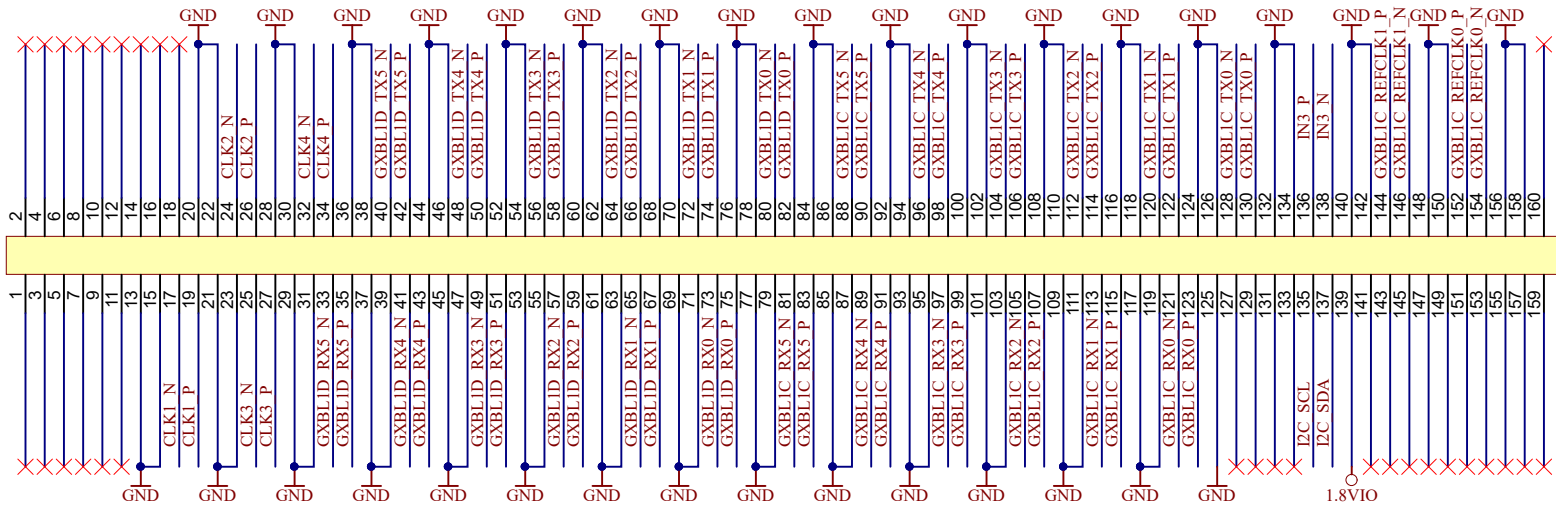
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Date: 2020-08-31	Copyright: Trenz Electronic GmbH / TT	Page4 of 23
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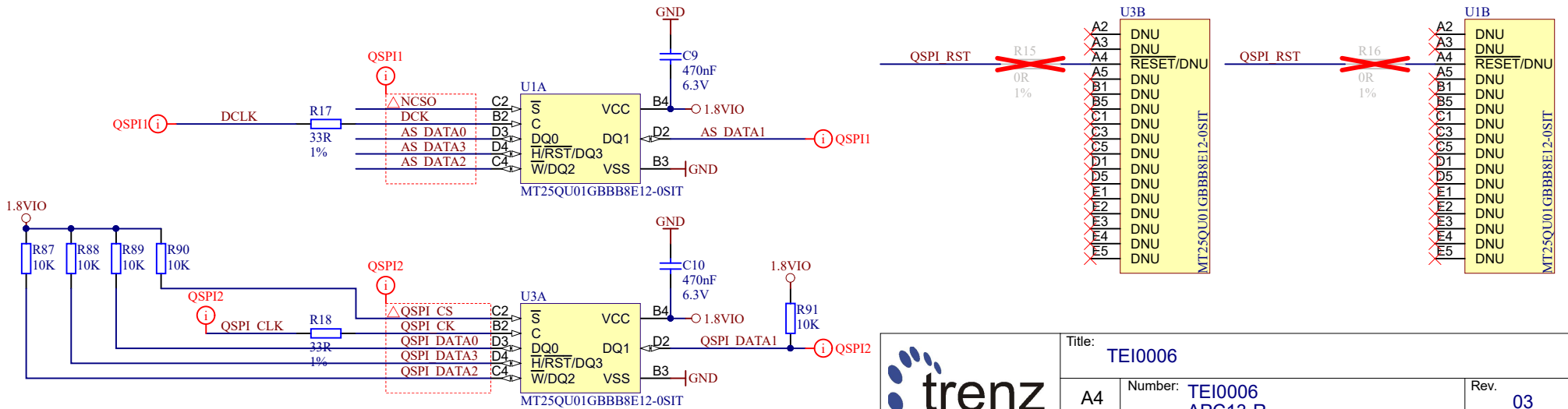
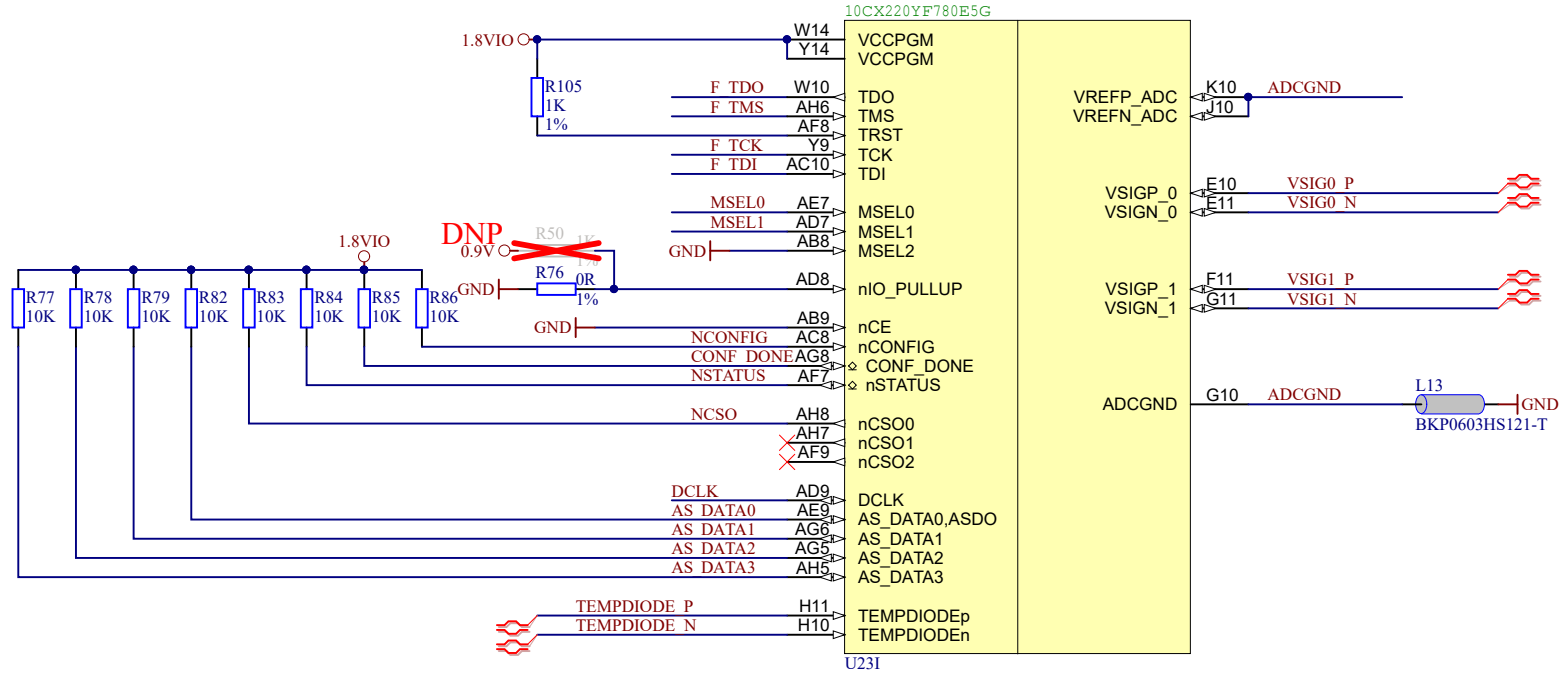


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ST5-80-1.50-L-D-P-TR

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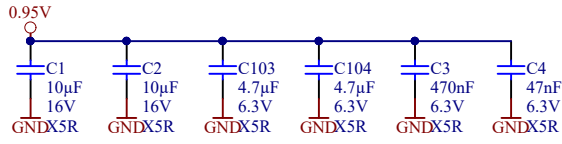
Rev. **03**

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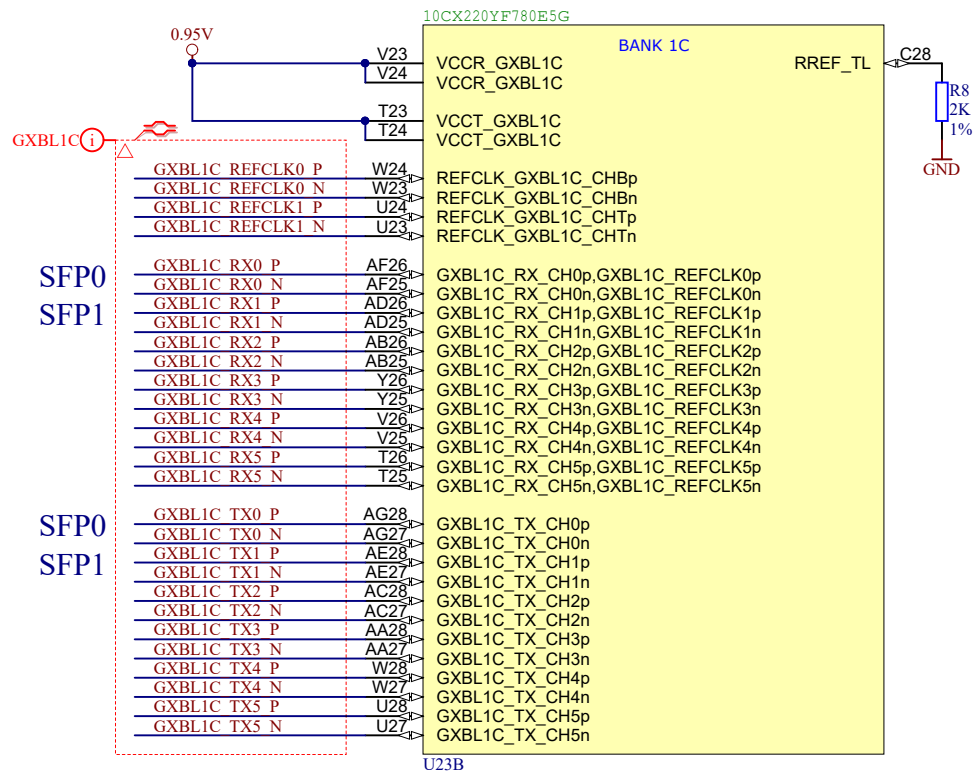
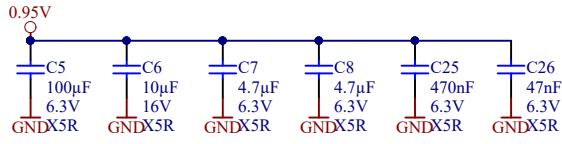


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Date: 2020-08-31	Copyright: Trenz Electronic GmbH	Page 6 of 23
Filename: C10GX_CFG.SchDoc		

Placed at VCCT_GXB pins



Placed at VCCR_GXB pins

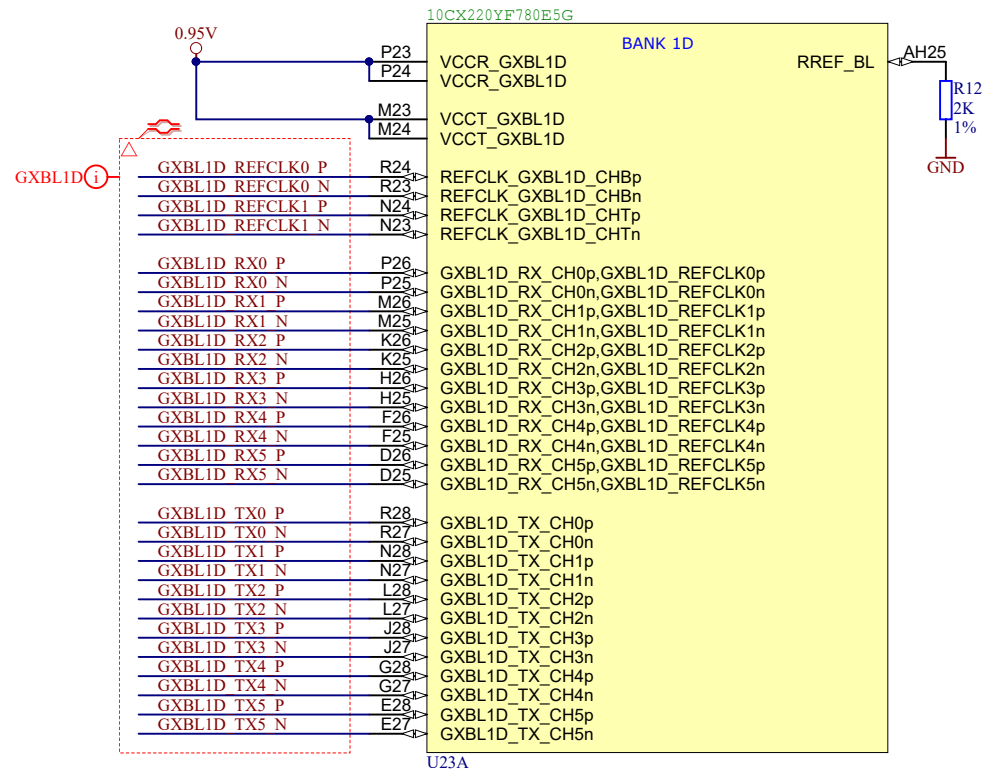


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SFP1

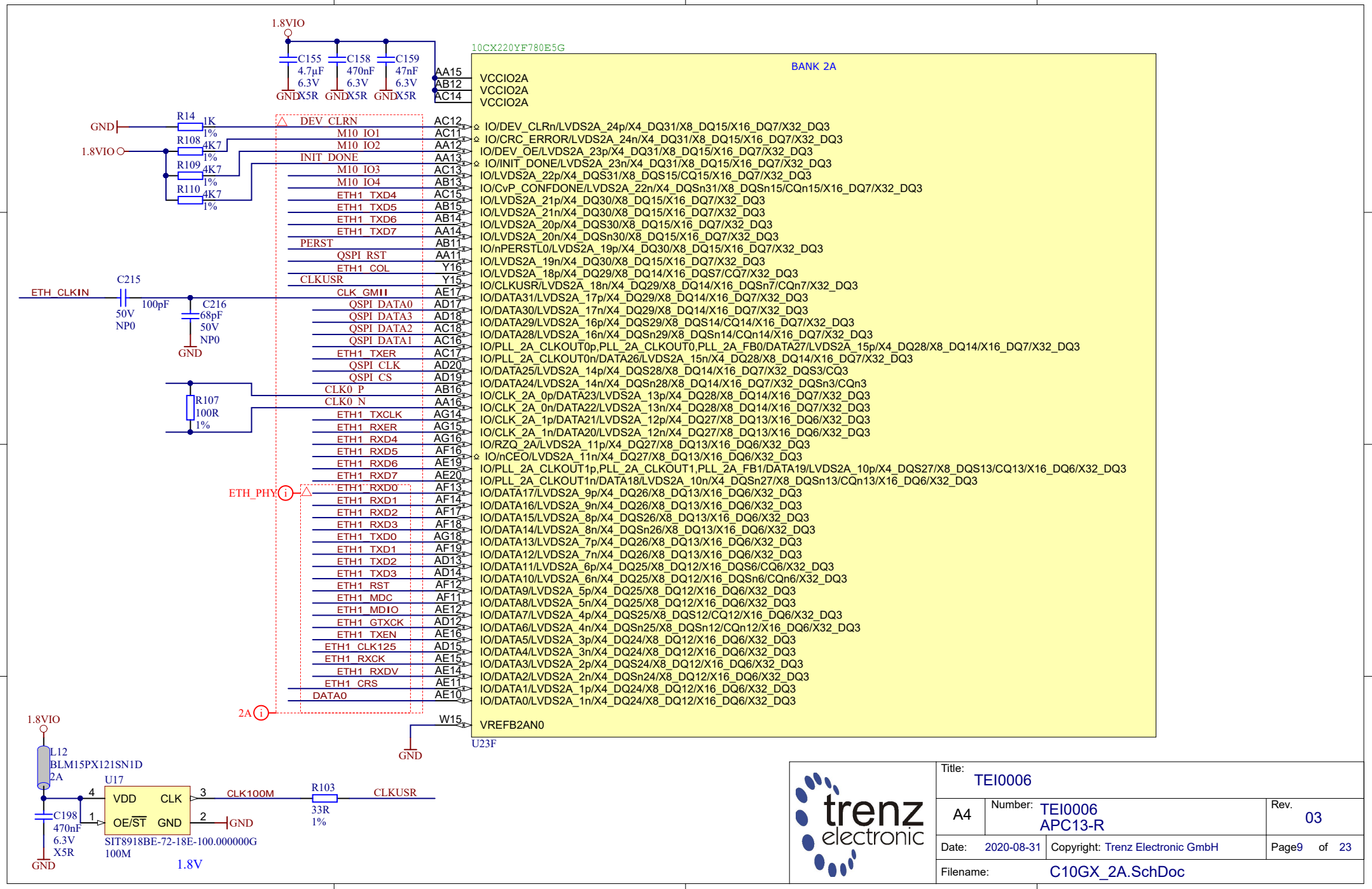
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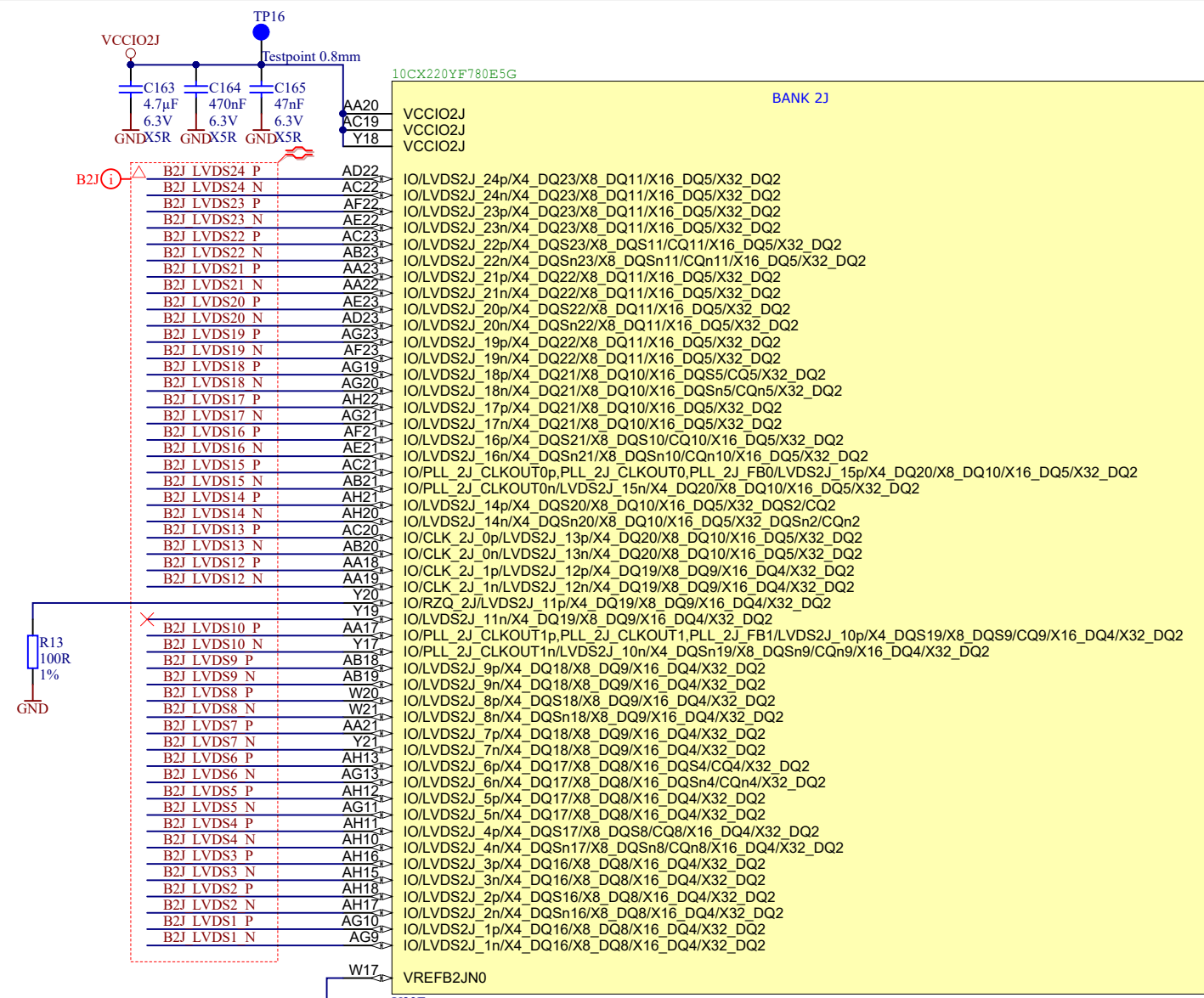
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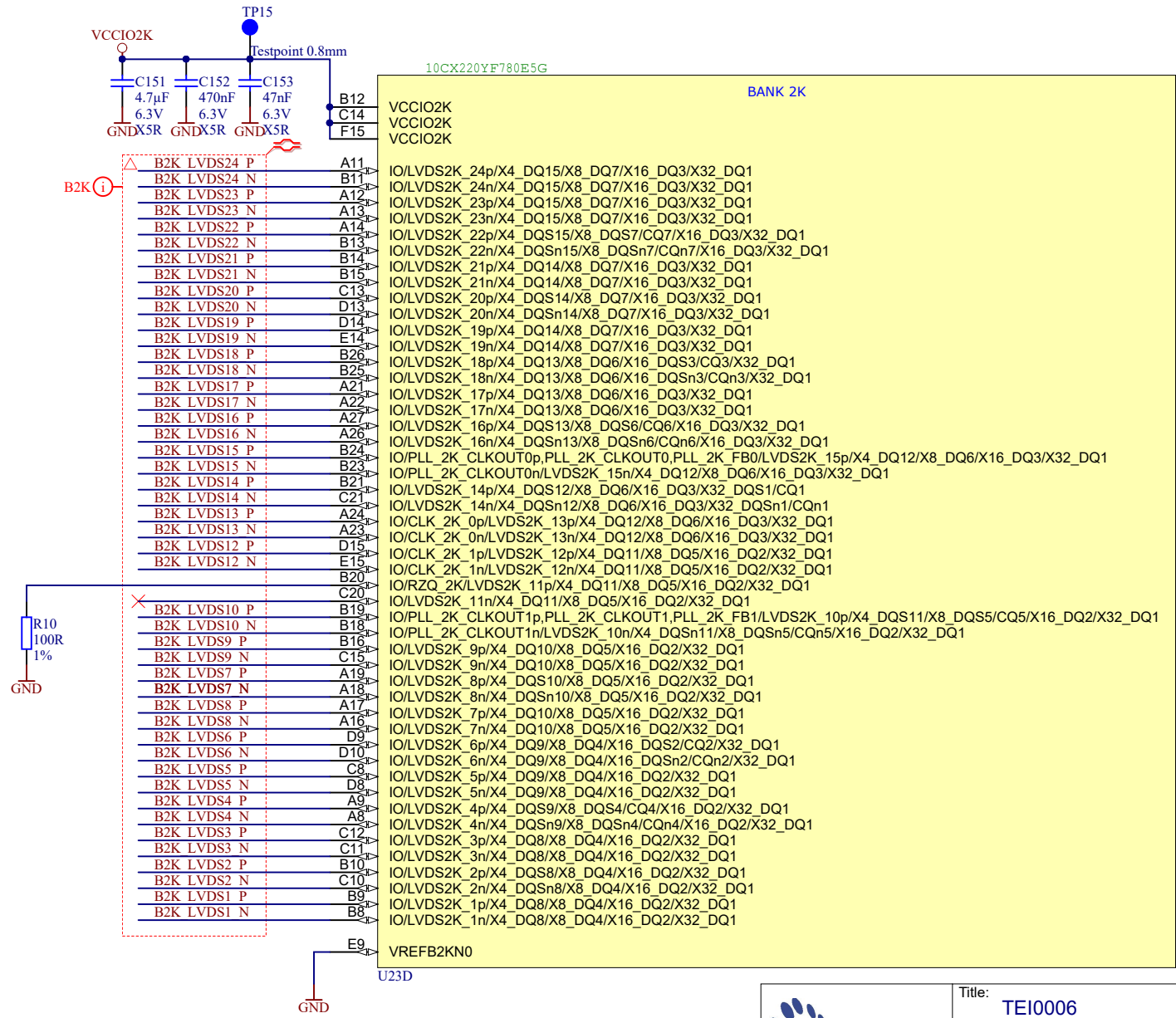
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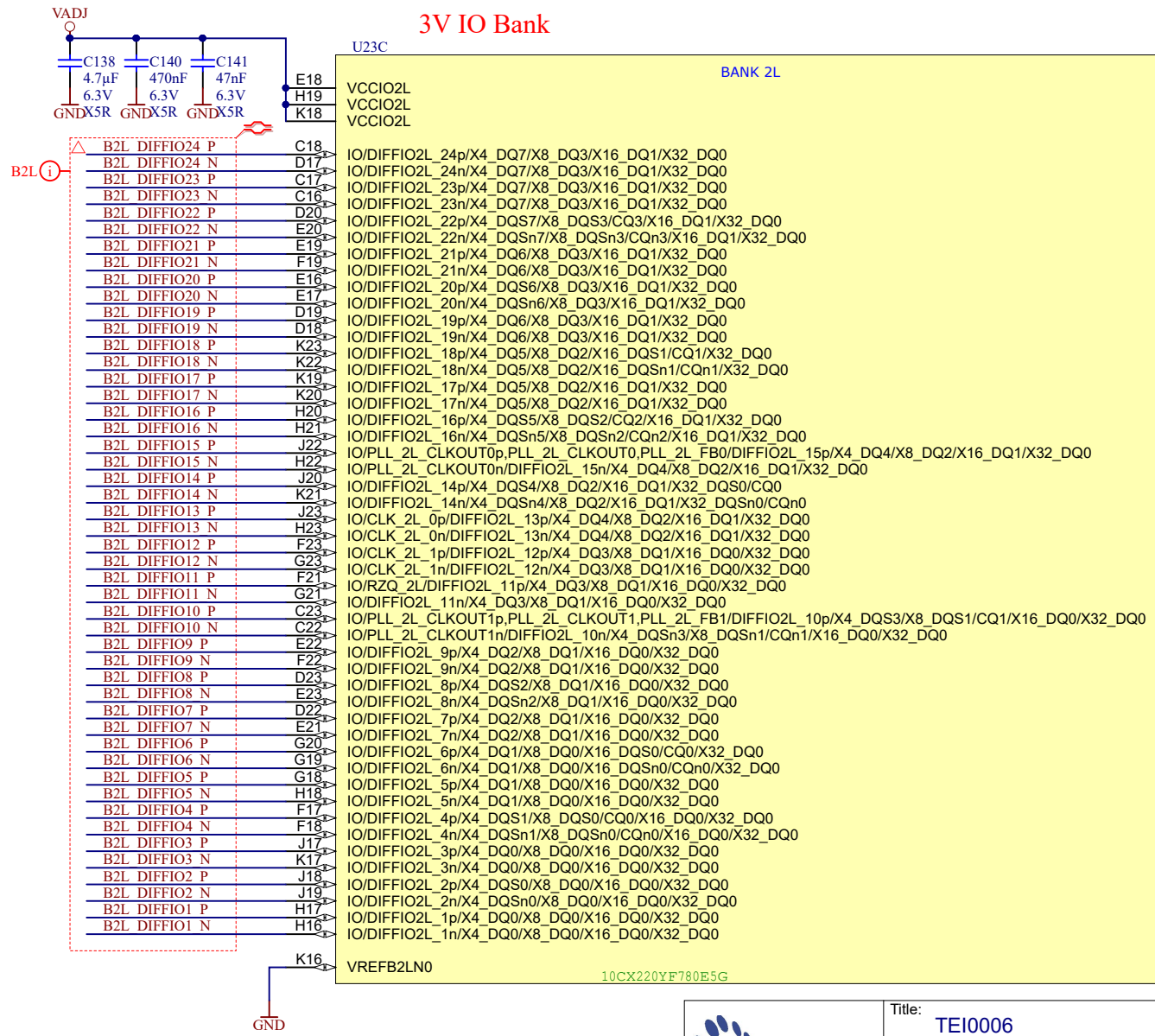
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3V IO Bank

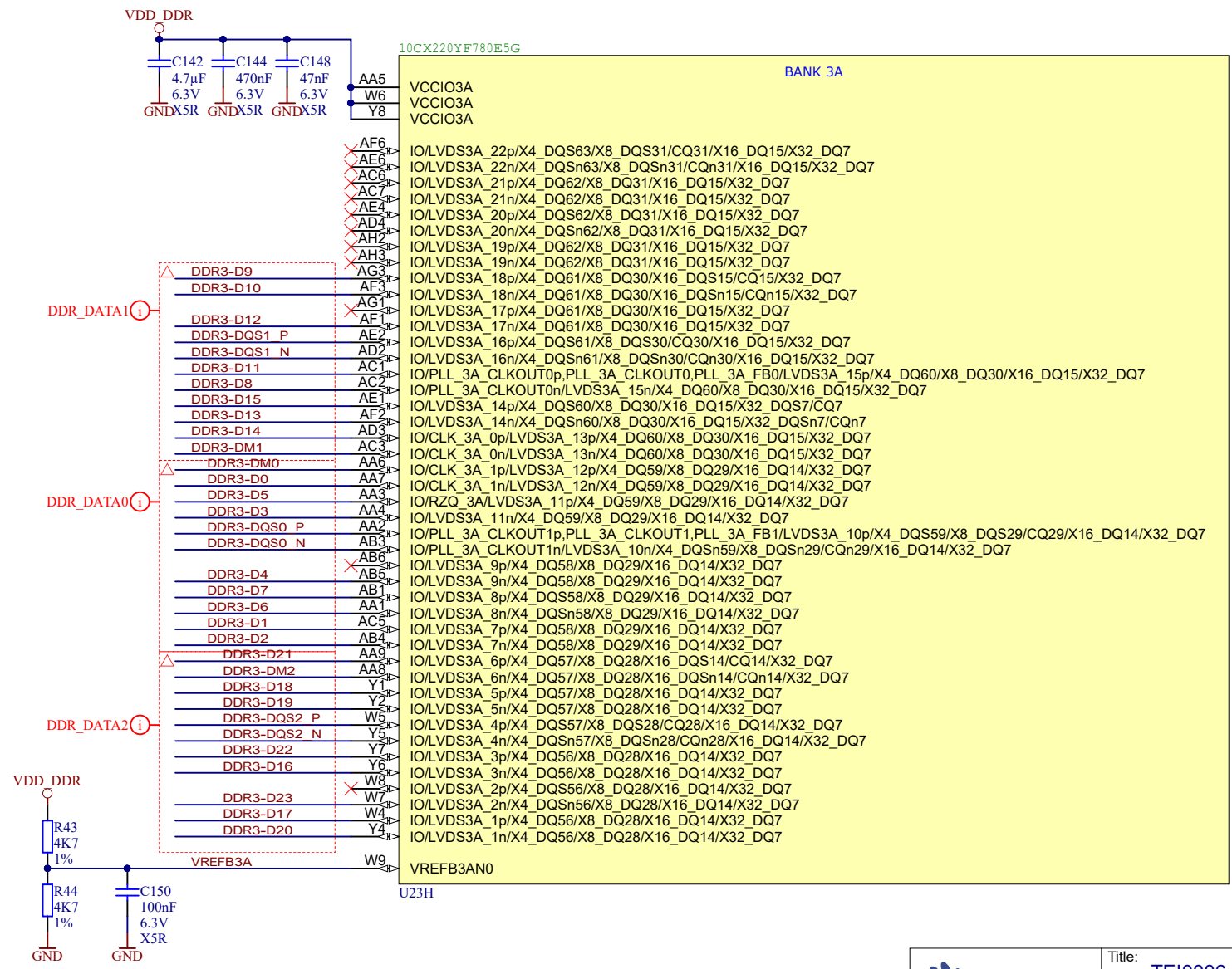

U23C

BANK 2L

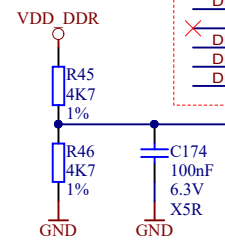
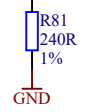
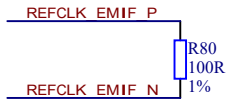
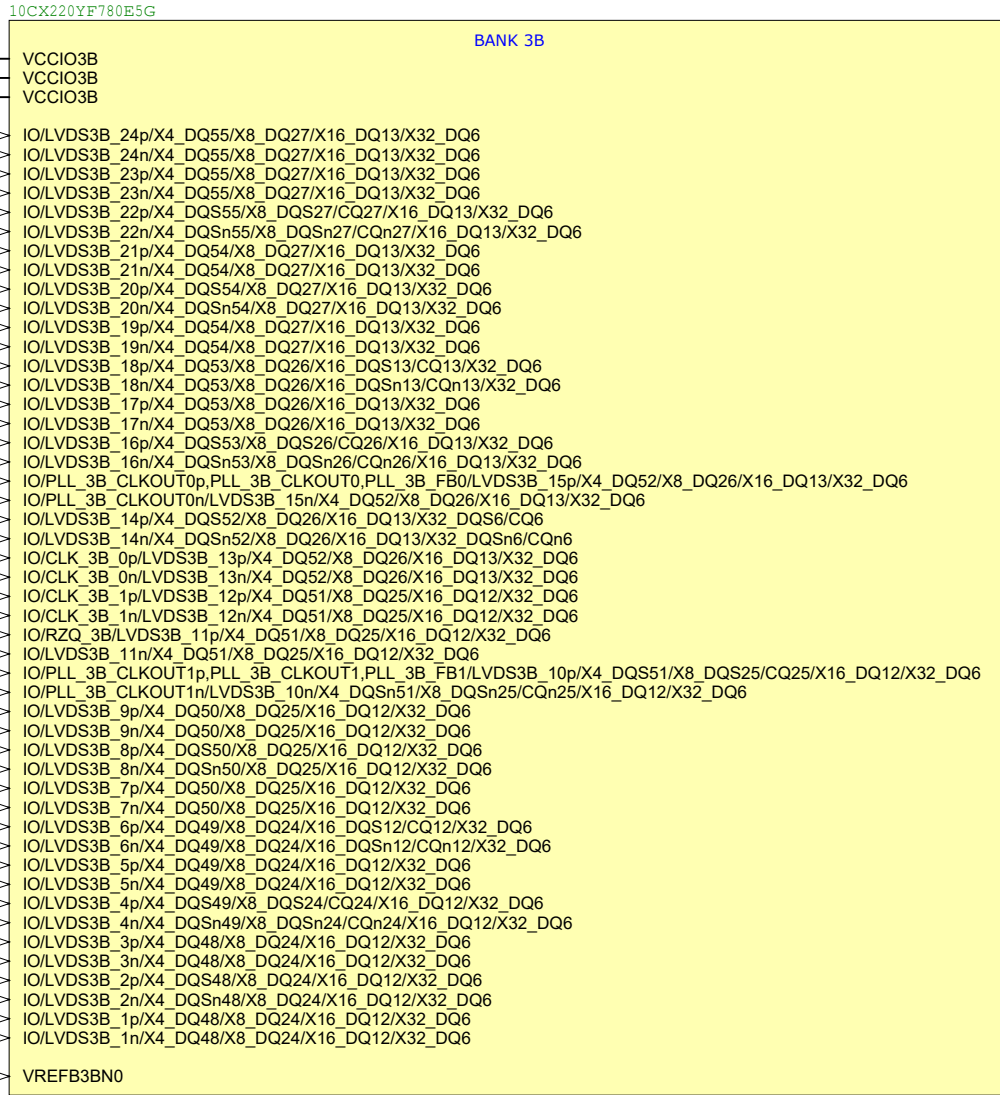
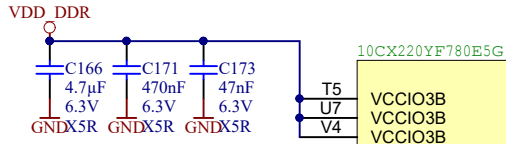
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VCCIO2L		
VCCIO2L		
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B2L DIFFIO24 N	D17	IO/DIFFIO2L_24n/X4_DQ7/X8_DQ3/X16_DQ1/X32_DQ0
B2L DIFFIO23 P	C17	IO/DIFFIO2L_23p/X4_DQ7/X8_DQ3/X16_DQ1/X32_DQ0
B2L DIFFIO23 N	C16	IO/DIFFIO2L_23n/X4_DQ7/X8_DQ3/X16_DQ1/X32_DQ0
B2L DIFFIO22 P	D20	IO/DIFFIO2L_22p/X4_DQS7/X8_DQS3/CQ3/X16_DQ1/X32_DQ0
B2L DIFFIO22 N	E20	IO/DIFFIO2L_22n/X4_DQSn7/X8_DQSn3/CQn3/X16_DQ1/X32_DQ0
B2L DIFFIO21 P	E19	IO/DIFFIO2L_21p/X4_DQ6/X8_DQ3/X16_DQ1/X32_DQ0
B2L DIFFIO21 N	F19	IO/DIFFIO2L_21n/X4_DQ6/X8_DQ3/X16_DQ1/X32_DQ0
B2L DIFFIO20 P	E16	IO/DIFFIO2L_20p/X4_DQS6/X8_DQ3/X16_DQ1/X32_DQ0
B2L DIFFIO20 N	E17	IO/DIFFIO2L_20n/X4_DQSn6/X8_DQ3/X16_DQ1/X32_DQ0
B2L DIFFIO19 P	D19	IO/DIFFIO2L_19p/X4_DQ6/X8_DQ3/X16_DQ1/X32_DQ0
B2L DIFFIO19 N	D18	IO/DIFFIO2L_19n/X4_DQ6/X8_DQ3/X16_DQ1/X32_DQ0
B2L DIFFIO18 P	K23	IO/DIFFIO2L_18p/X4_DQ5/X8_DQ2/X16_DQS1/CQ1/X32_DQ0
B2L DIFFIO18 N	K22	IO/DIFFIO2L_18n/X4_DQ5/X8_DQ2/X16_DQSn1/CQn1/X32_DQ0
B2L DIFFIO17 P	K19	IO/DIFFIO2L_17p/X4_DQ5/X8_DQ2/X16_DQ1/X32_DQ0
B2L DIFFIO17 N	K20	IO/DIFFIO2L_17n/X4_DQ5/X8_DQ2/X16_DQ1/X32_DQ0
B2L DIFFIO16 P	H20	IO/DIFFIO2L_16p/X4_DQS5/X8_DQS2/CQ2/X16_DQ1/X32_DQ0
B2L DIFFIO16 N	H21	IO/DIFFIO2L_16n/X4_DQS5/X8_DQS2/CQn2/X16_DQ1/X32_DQ0
B2L DIFFIO15 P	J22	IO/PLL_2L_CLKOUT0p,PLL_2L_CLKOUT0,PLL_2L_FB0/DIFFIO2L_15p/X4_DQ4/X8_DQ2/X16_DQ1/X32_DQ0
B2L DIFFIO15 N	H22	IO/PLL_2L_CLKOUT0n/DIFFIO2L_15n/X4_DQ4/X8_DQ2/X16_DQ1/X32_DQ0
B2L DIFFIO14 P	J20	IO/DIFFIO2L_14p/X4_DQS4/X8_DQ2/X16_DQ1/X32_DQS0/CQ0
B2L DIFFIO14 N	K21	IO/DIFFIO2L_14n/X4_DQSn4/X8_DQ2/X16_DQ1/X32_DQS0/CQn0
B2L DIFFIO13 P	J23	IO/CLK_2L_0p/DIFFIO2L_13p/X4_DQ4/X8_DQ2/X16_DQ1/X32_DQ0
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B2L DIFFIO11 N	G21	IO/DIFFIO2L_11n/X4_DQ3/X8_DQ1/X16_DQ0/X32_DQ0
B2L DIFFIO10 P	C23	IO/PLL_2L_CLKOUT1p,PLL_2L_CLKOUT1,PLL_2L_FB1/DIFFIO2L_10p/X4_DQS3/X8_DQS1/CQ1/X16_DQ0/X32_DQ0
B2L DIFFIO10 N	C22	IO/PLL_2L_CLKOUT1n/DIFFIO2L_10n/X4_DQSn3/X8_DQSn1/CQn1/X16_DQ0/X32_DQ0
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B2L DIFFIO9 N	F22	IO/DIFFIO2L_9n/X4_DQ2/X8_DQ1/X16_DQ0/X32_DQ0
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B2L DIFFIO6 N	G19	IO/DIFFIO2L_6p/X4_DQ1/X8_DQ0/X16_DQS0/CQ0/X32_DQ0
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B2L DIFFIO4 N	F18	IO/DIFFIO2L_4p/X4_DQS1/X8_DQS0/CQ0/X16_DQ0/X32_DQ0
B2L DIFFIO3 P	J17	IO/DIFFIO2L_4n/X4_DQSn1/X8_DQSn0/CQn0/X16_DQ0/X32_DQ0
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B2L DIFFIO2 P	J18	IO/DIFFIO2L_3n/X4_DQ0/X8_DQ0/X16_DQ0/X32_DQ0
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B2L DIFFIO1 P	H17	IO/DIFFIO2L_2n/X4_DQSn0/X8_DQ0/X16_DQ0/X32_DQ0
B2L DIFFIO1 N	H16	IO/DIFFIO2L_1p/X4_DQ0/X8_DQ0/X16_DQ0/X32_DQ0
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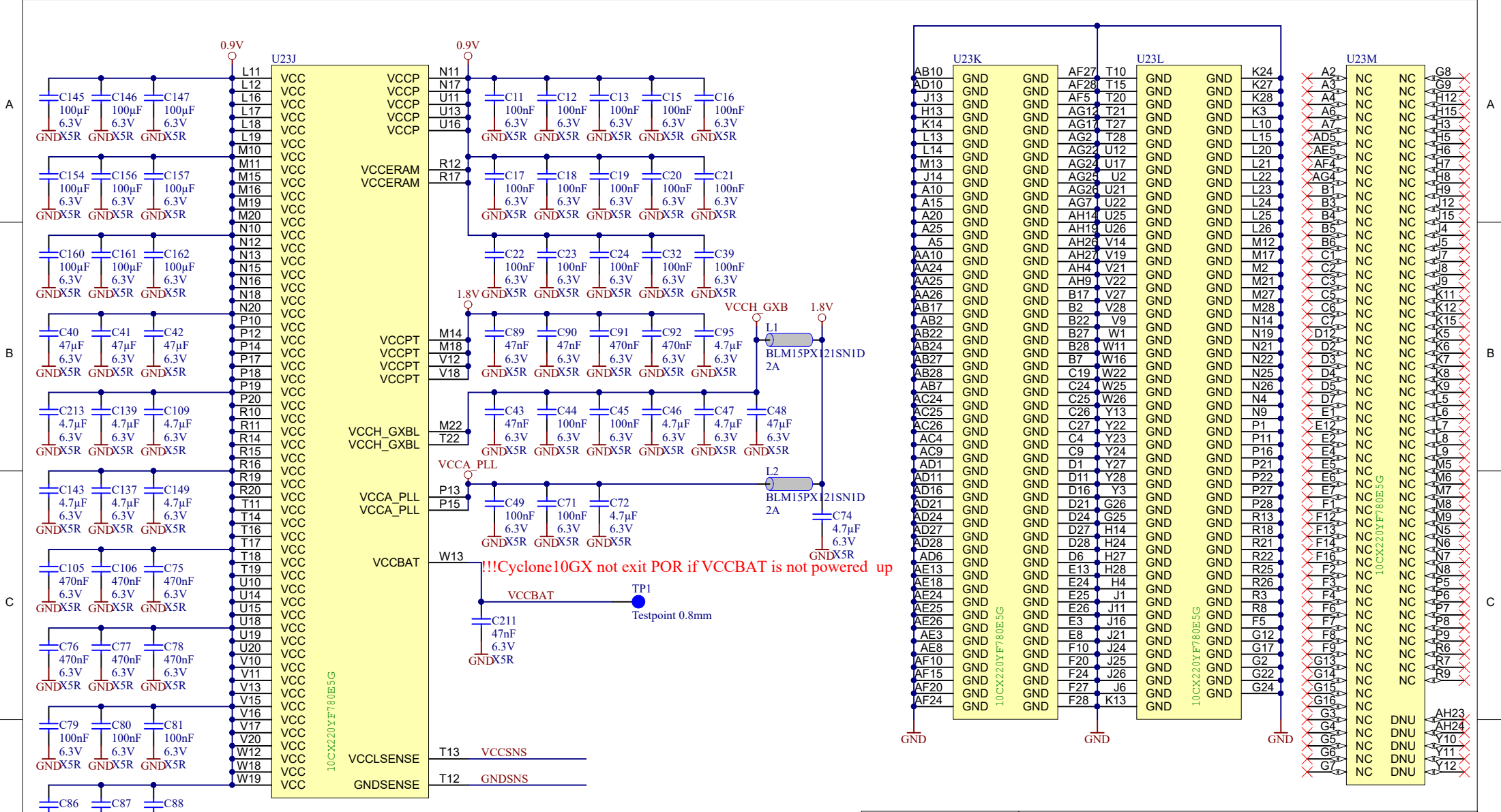
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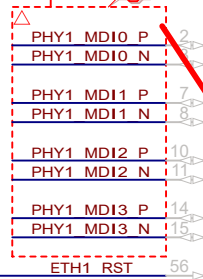
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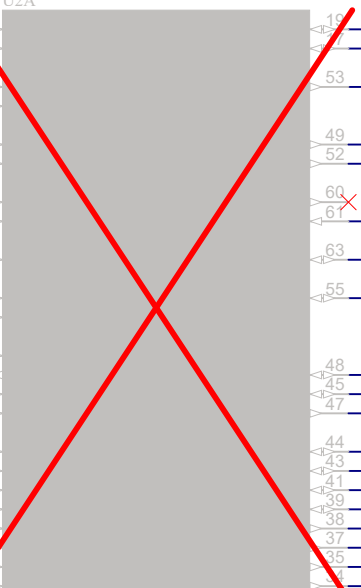
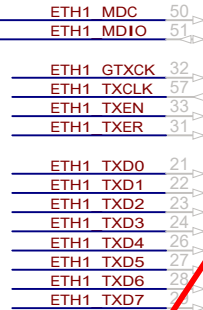
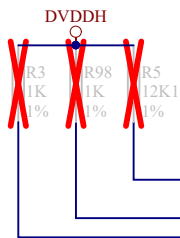
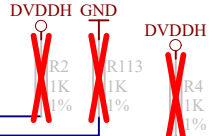
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ETH_MDI



U2A

KSZ9031MNXIC

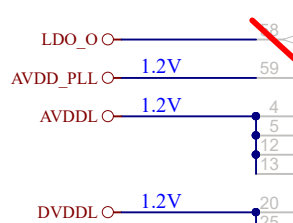
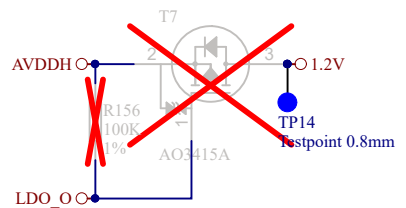
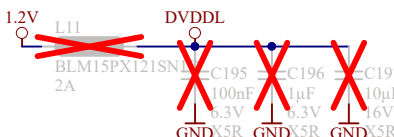
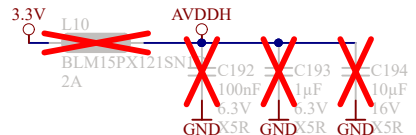
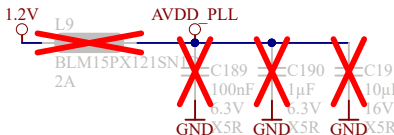
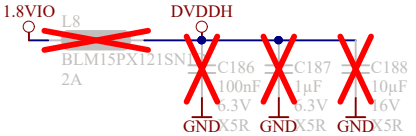
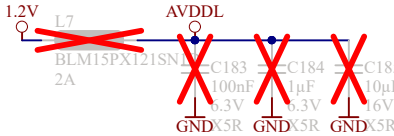


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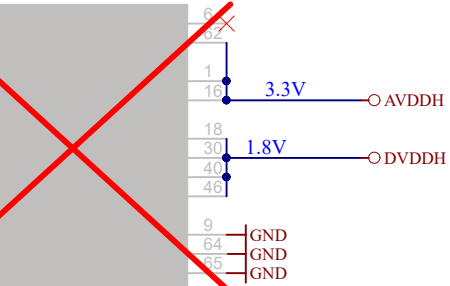
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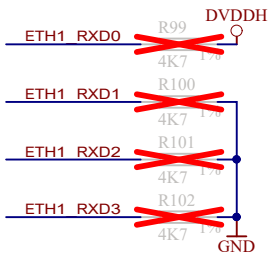


U2B

KSZ9031MNXIC



MODE: 0001 -> GMII/MII mode



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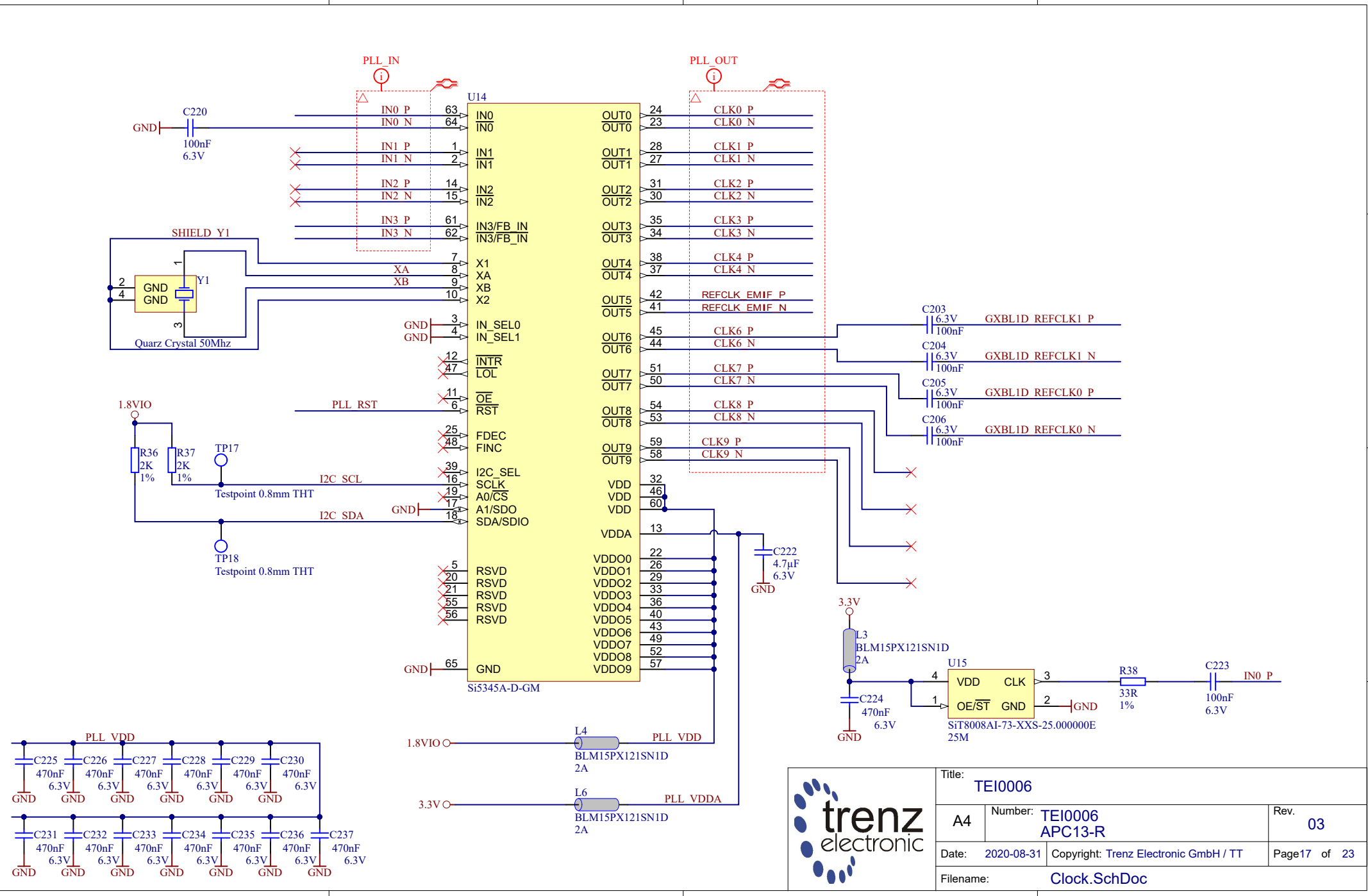
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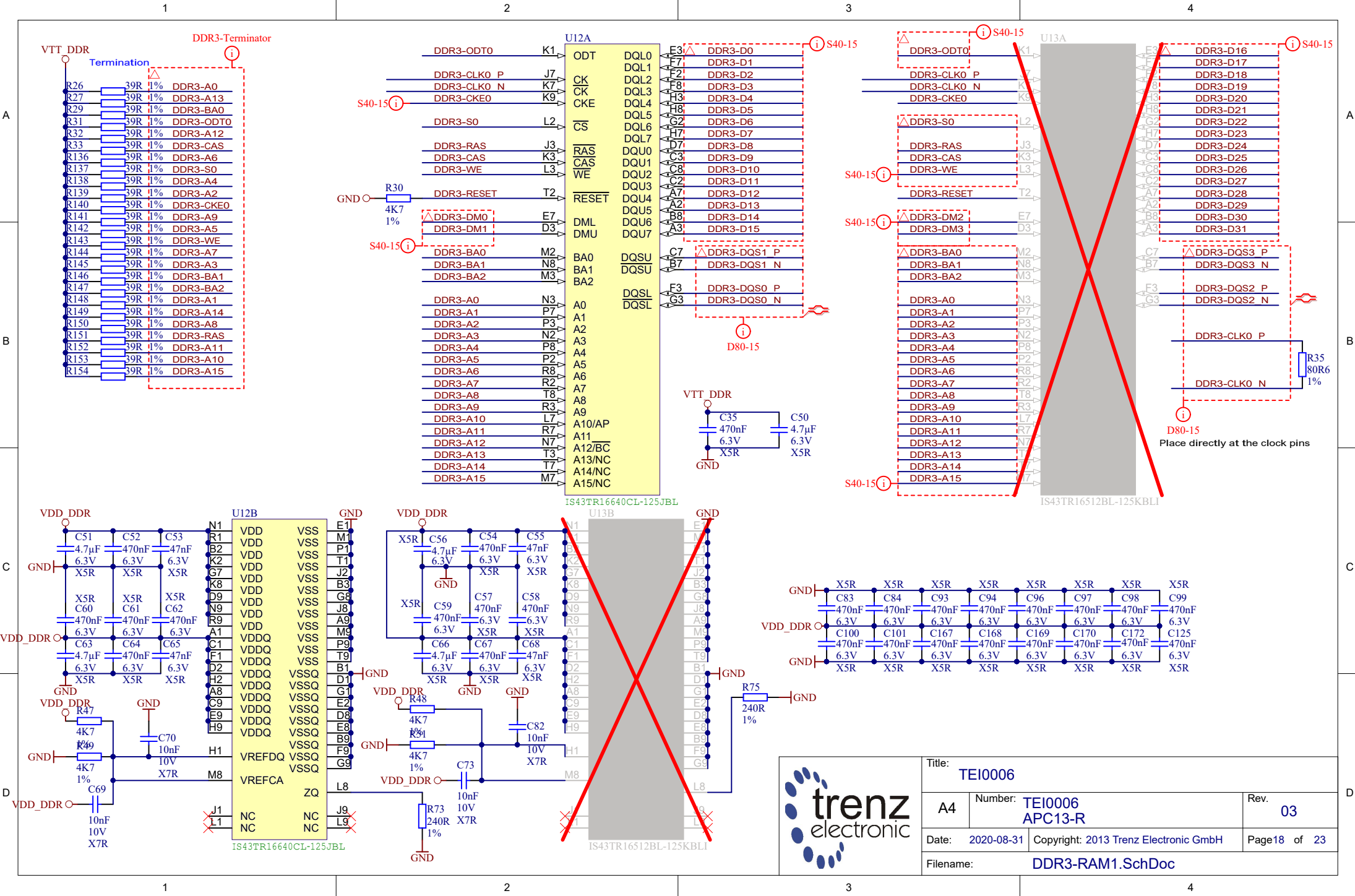
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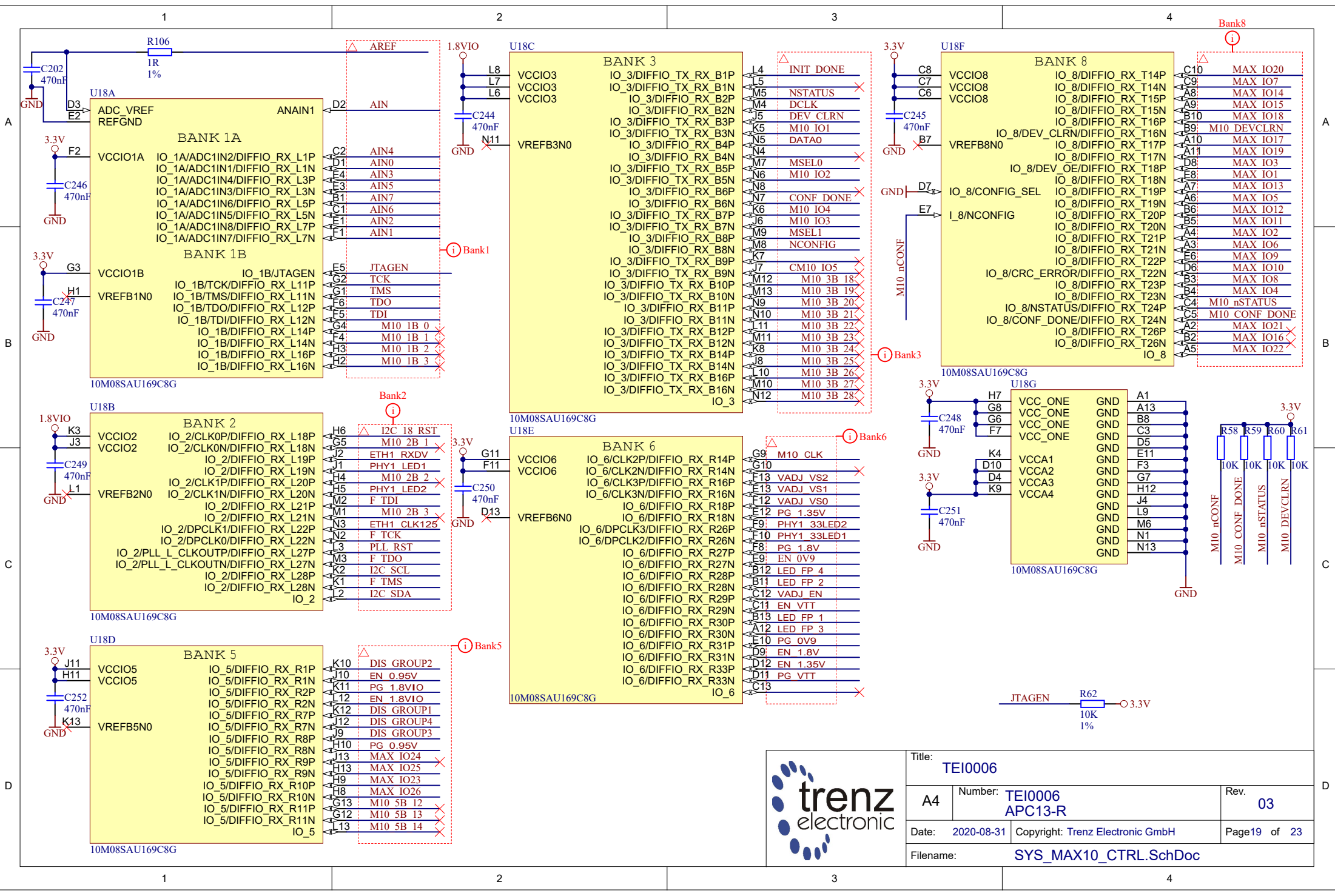
2

3

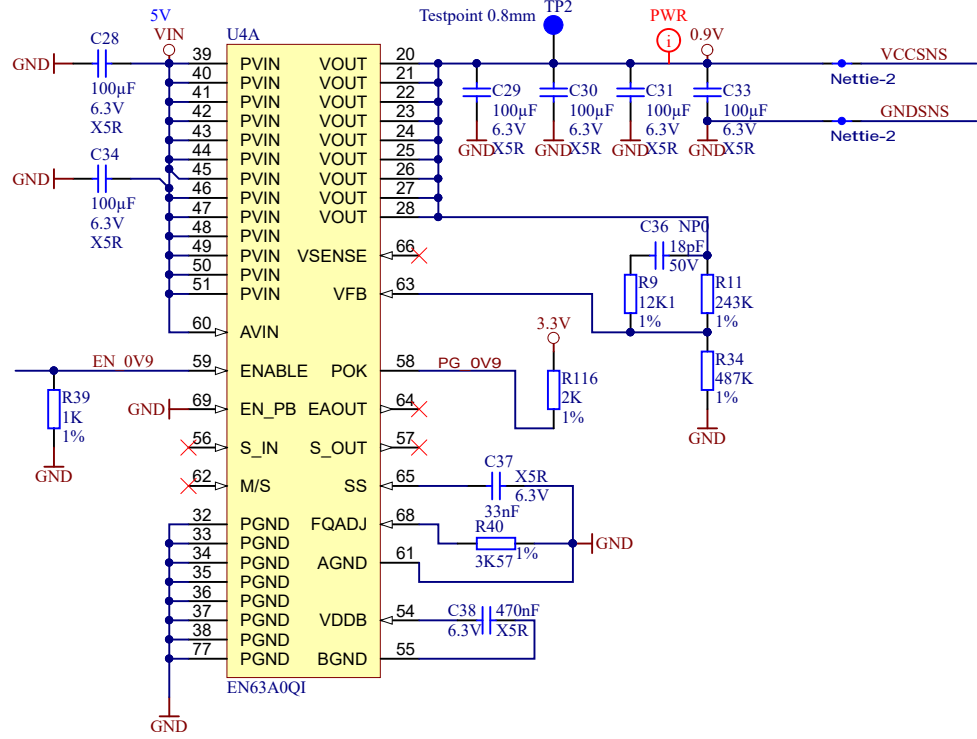
4



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Filename: DDR3-RAM1.SchDoc		



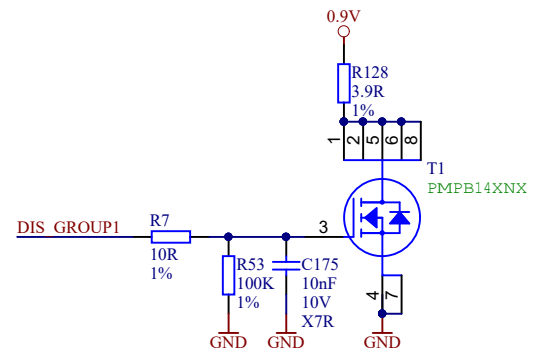
Title: TEI0006		
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Filename: SYS_MAX10_CTRL.SchDoc		



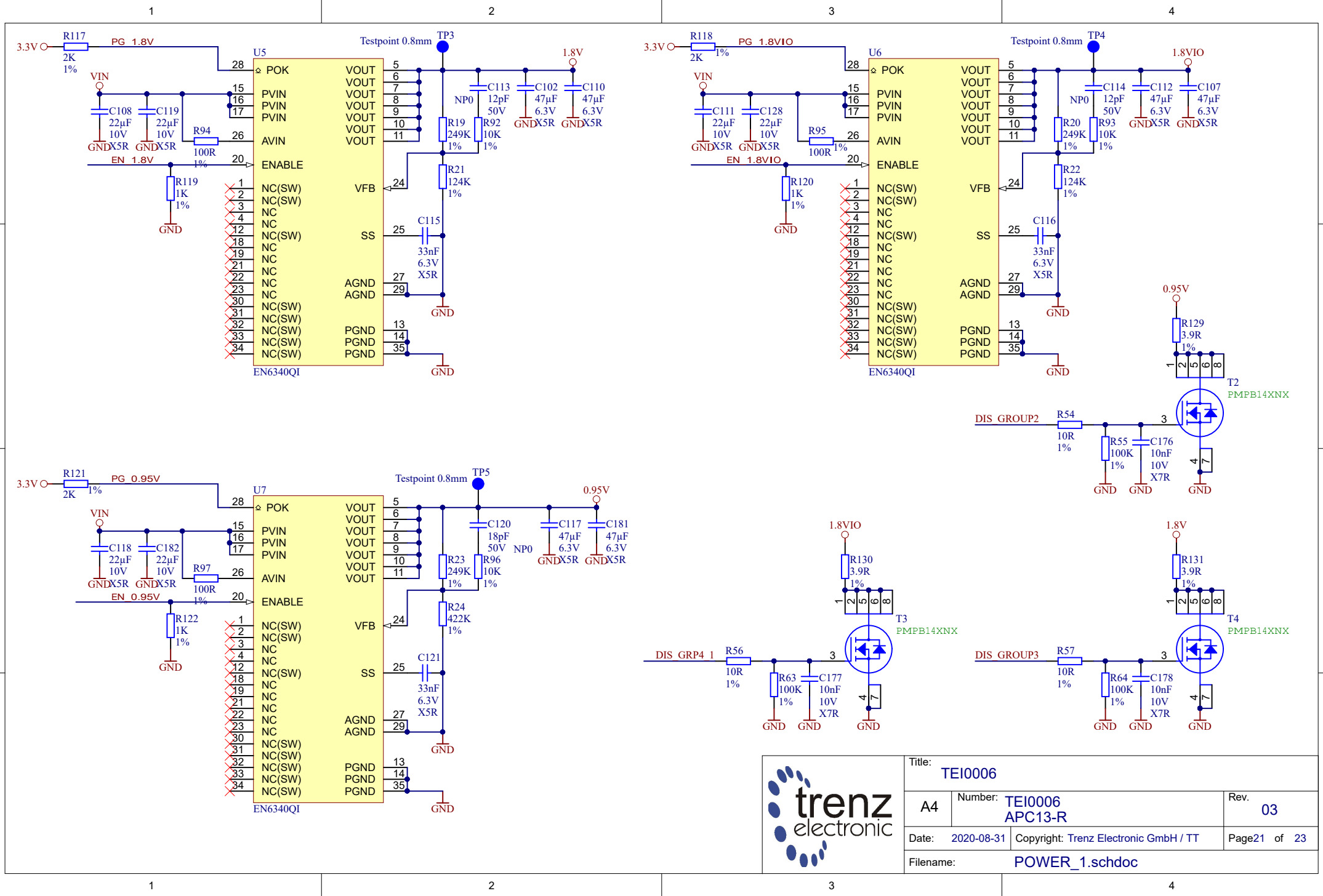
U4B

1	NC	NC	17
2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC	68
11	NC	NC(SW)	70
12	NC	NC(SW)	71
13	NC	NC	72
14	NC	NC	73
15	NC	NC	74
16	NC	NC	75
17	NC	NC	76

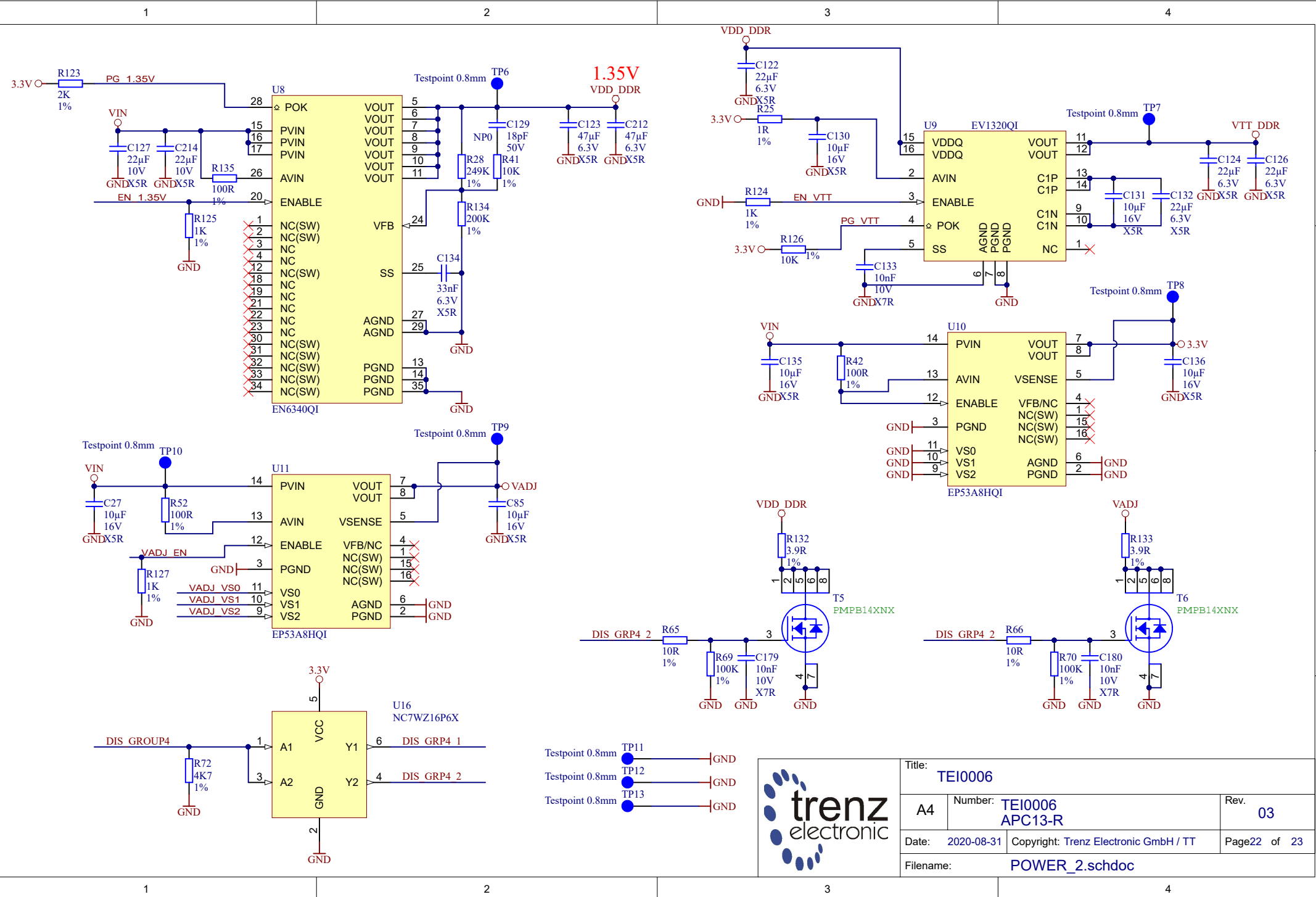
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VT: Initial Rev (07.2018)

Changes from REV01 to REV02:


- 1) VT: added MEMS 100MHz clock oscillator to CLKUSR
- 2) VT: remove CLKUSR from J2
- 3) VT: replaced Si510 to SiT8008/CM3225-4pad
- 4) VT: remove DEVCLRN from J2, added pull-up
- 5) VT: remove M10_nSTATUS from J2, added pull-up
- 6) VT: Added optional CryptoAuthentication chip U19 (DNP)

Changes from REV02 to REV03 (08.2020):

- 1) VT: fixed CLK connections (CLK's from FMC (on Baseboard) directly connected to GXBL1C bank)
- 2) VT: added heatsink
- 3) VT: full upd LIB
- 4) VT: added Legal Notices sheet

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- 5) VY: replaced not available transistors T1-T6 AON2240 to PMPB14XNX

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