


Regarding the usage of our schematics and alike documentation for Trenz module TEI0006.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TEI0006 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

	Title: TEI0006 - Legal Notices		
	A4	Number: TEI0006 ALC13A	Rev. 04
	Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 1 of 25
	Filename: Legal Notices Modules.SchDoc		

1

2

3

4

A

A

B

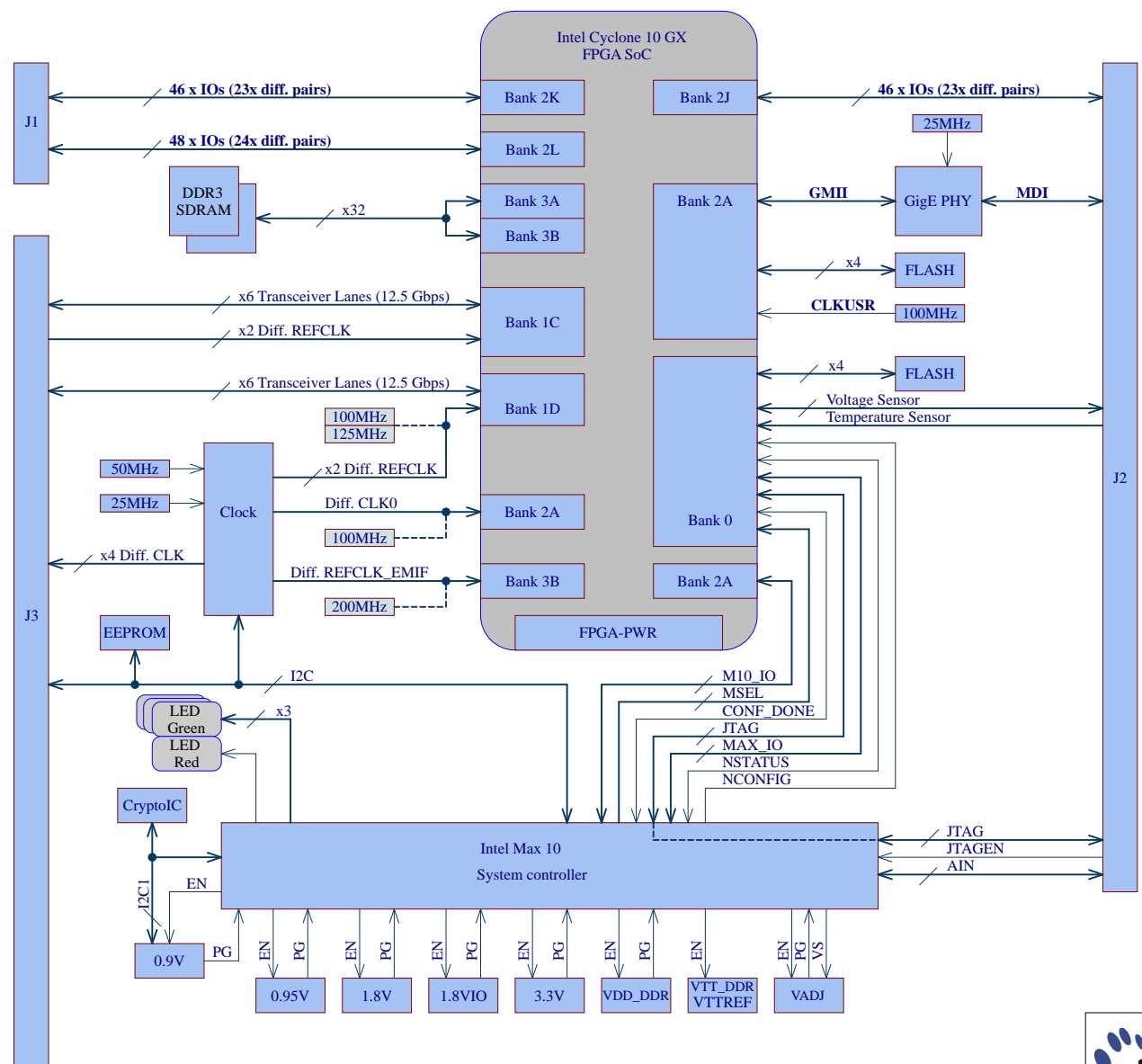
B

C

C

D

D



- U_Revision Changes
- U_TEI0006
- U_Power_Diagram

Special notes:



Title: TEI0006 - System Overview		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 2 of 25
Filename: Overview.SchDoc		


1

2

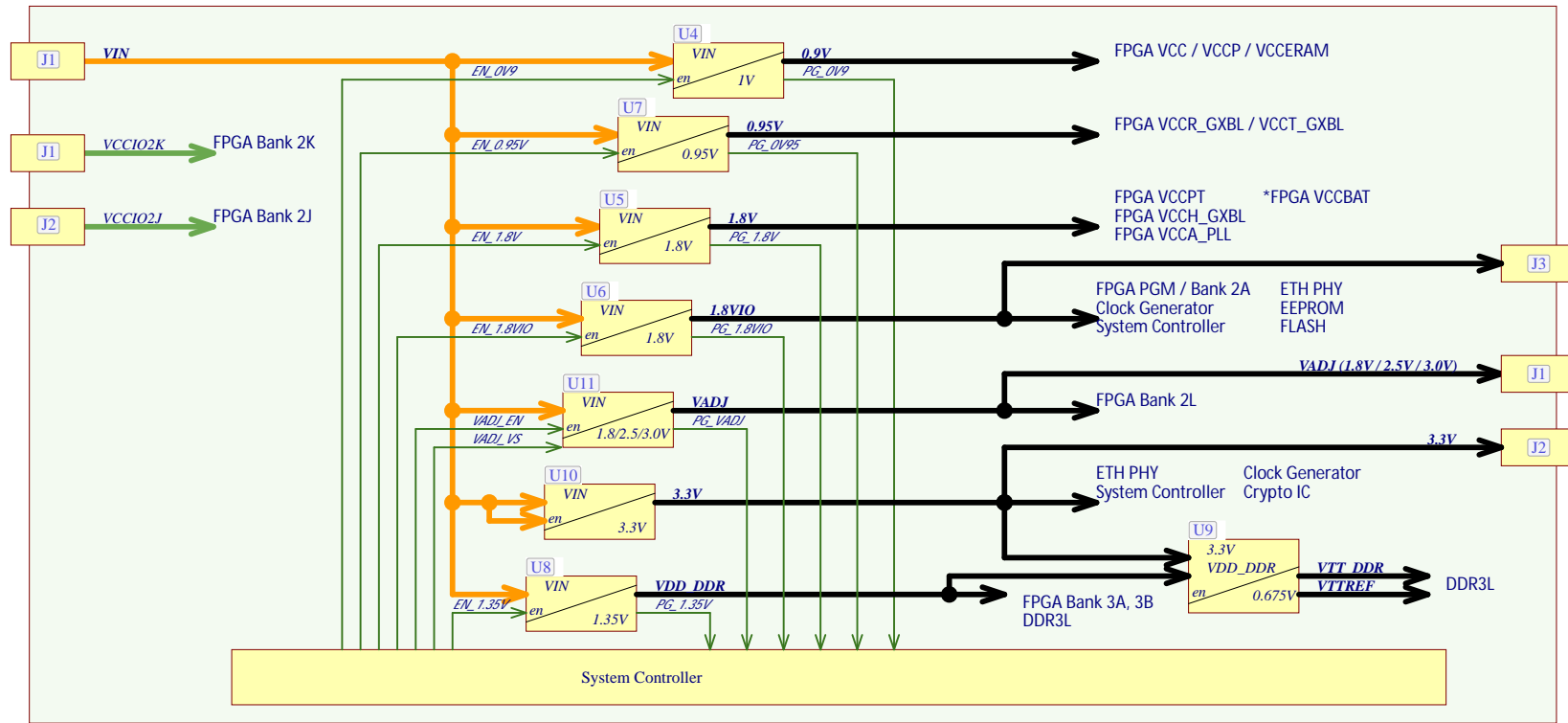
3

4

REV	Description	
-01	Initial revision	VT
-02	1) VT: added MEMS 100MHz clock oscillator to CLKUSR 2) VT: remove CLKUSR from J2 3) VT: replaced Si510 to SiT8008/CM3225-4pad 4) VT: remove DEVCLRN from J2, added pull-up 5) VT: remove M10_nSTATUS from J2, added pull-up 6) VT: Added optional CryptoAuthentication chip U19 (DNP)	VT
-03	1) VT: fixed CLK connections (CLK's from FMC (on Baseboard) directly connected to GXBLIC bank) 2) VT: added heatsink 3) VT: full upd LIB 4) VT: added Legal Notices sheet	VT
	5) VY: replaced not available transistors T1-T6 AON2240 to PMPB14XNX	VY
-04	1) VT: replaced EOL Power regulators: a) U4: EN63A0QI -> MP8869SGL-Z b) U5,U6,U7,U8: EN6340QI -> MPM3840GQV-Z c) U10, U11: EP53A8HQI -> MPM3834CGPA d) U9: EV1320QI -> TPS51206DSQ 2) VT: replaced not available buffer U16: NC7WZ16P6X ->SN74AUP2G17DCKR 3) VT: added dual transistor T8 for select VADJ Voltage (1.8V, 2.5V, 3.0V) 4) VT: remove signals VADJ_VS2 and PG_VTT from System Controller U18 5) VT: added DCDC I2C to System Controller U18 6) VT: added Testpoints to I2C1 I2C bus 7) VT: added optional MEMS LVDS Oscillators Y2,Y3,Y4,Y5 8) VT: remove Resistors R47,R48,R49,R51 9) VT: added optional Termination to REFCLK_EMIF 10) VT: U19-> use I2C 3.3V 11) VT: added diode D5 for VCCBAT 12) VT: added signal PG_VADJ to System Controller U18 13) VT: changed Commercial grade to Industrial for System Controller U18	VT

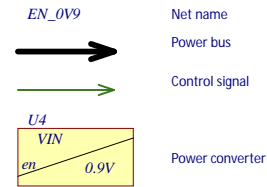
	Title: TEI0006 - Revision changes		
	A4	Number: TEI0006 ALC13A	Rev. 04
	Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 3 of 25
	Filename: Revision_Changes.SchDoc		

Power-on sequencing:

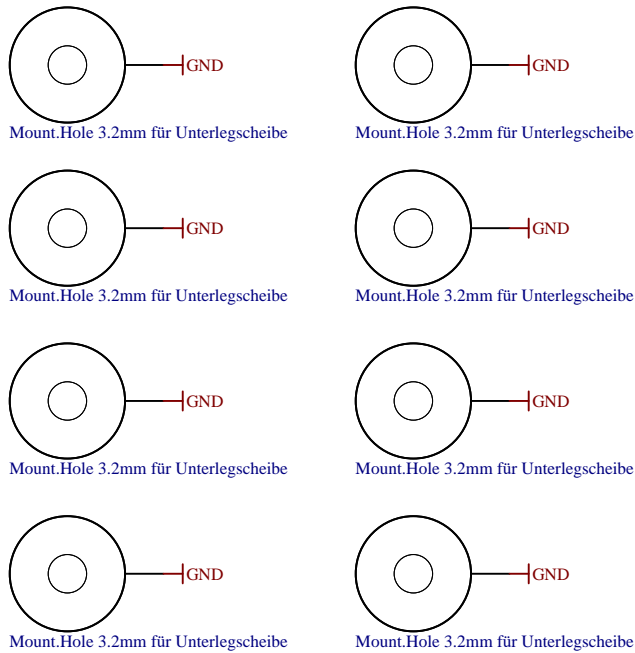


Recommended Operating Conditions

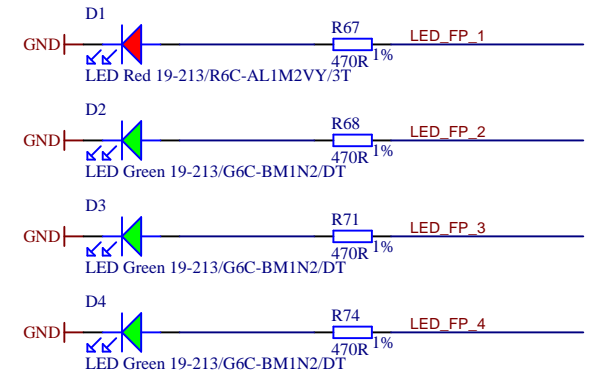
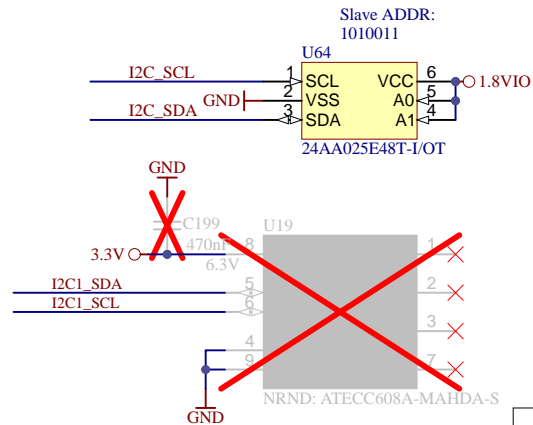
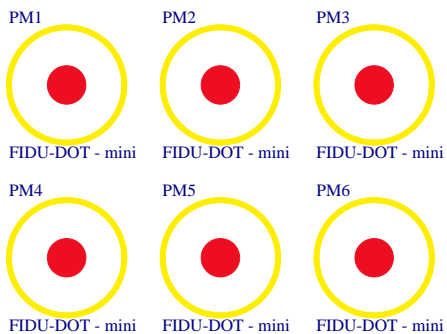
Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	5V	+/-5%	Micromodule Power	Mandatory
VCCIO2K	IN	1.2 - 1.8V	+/-3%	IO Bank 2K	-
VCCIO2J	IN	1.2 - 1.8V	+/-3%	IO Bank 2J	-
1.8VIO	OUT	1.8V	+/-3%	For Carrier card Periphery	-
VADJ	OUT	1.8 - 3.0V	+/-3%	For Carrier card Periphery	Voltage set by System Controller
3.3V	OUT	3.3V	+/-3%	For Carrier card Periphery	-



	Title: TEI0006 - Power Diagram	
	A4	Number: TEI0006 ALC13A
	Date: 2023-02-02	Rev. 04
	Copyright: Trenz Electronic GmbH	Page 4 of 25
Filename: Power_Diagram.SchDoc		



Serial
Serialnummer 6,3 x 6.3mm



UKCA
UKCA Logo on Top Overlay
UKCA-TOOVERLAY

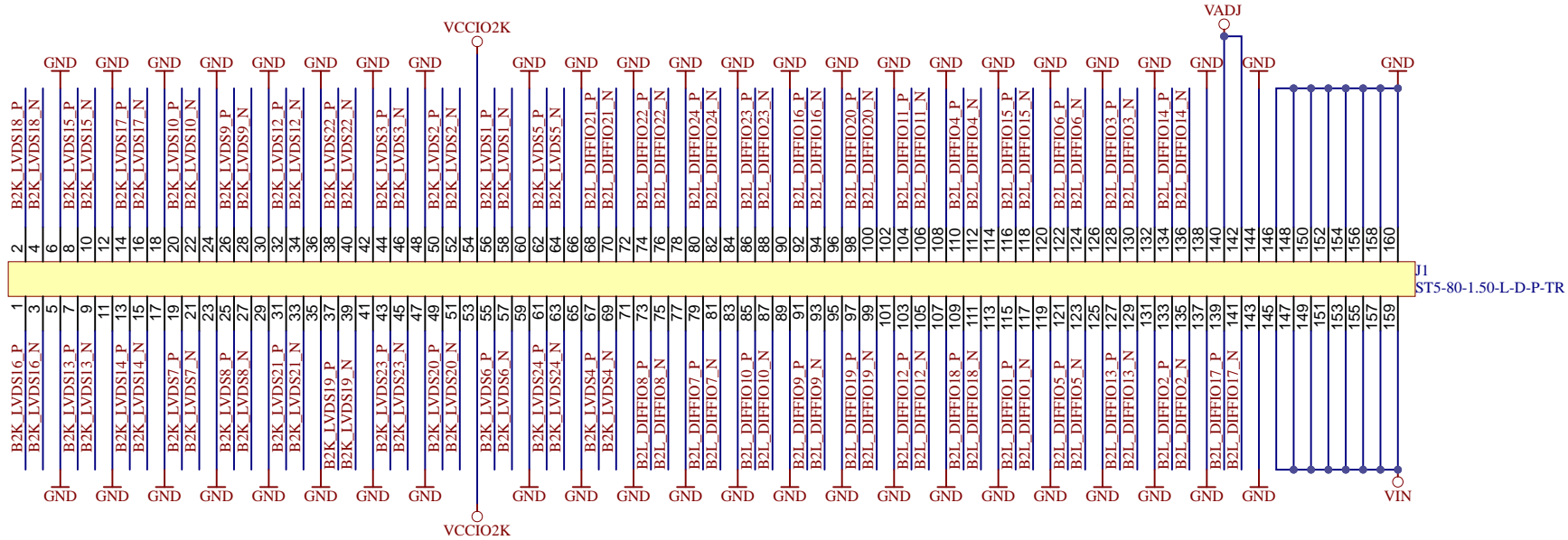
MECH2
TE Address Overlay
LOGO ADDRESS

LOGO1
TE Logo PRINT Layer
LOGO PRINT

Assembly variant	ALC13A
Created by	OT
Modified by	
Modified at	2023-05-03
SVN Revision	17814



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page5 of 25
Filename: TEI0006.SchDoc		



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 6 of 25
Filename: J1.SchDoc		

1

2

3

4

A

A

B

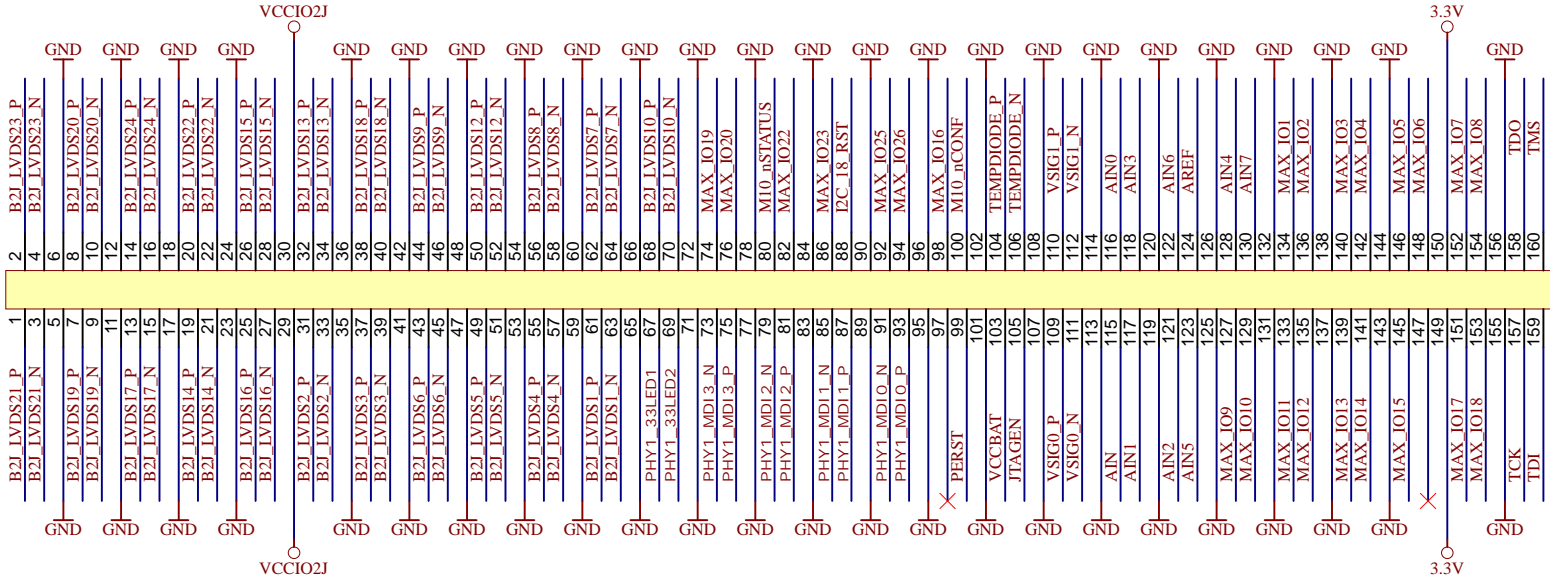
B

C

C

D

D



J2
ST5-80-1.50-L-D-P-TR



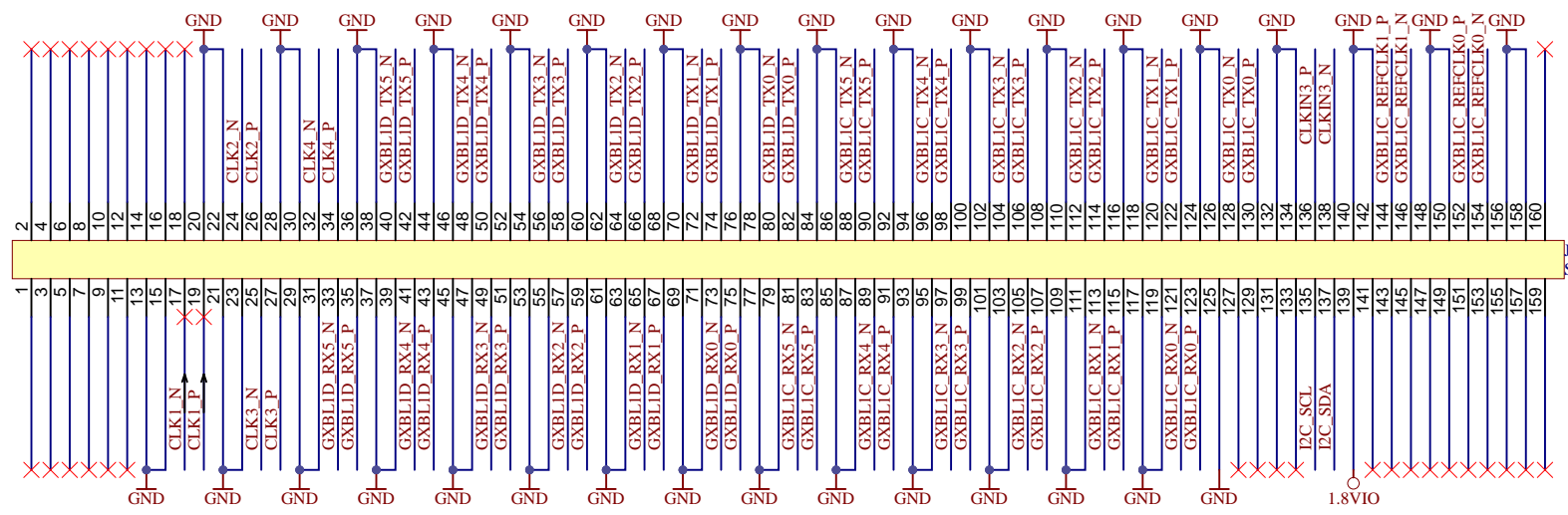
Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 7 of 25
Filename: J2.SchDoc		

1

2

3

4



J3
ST5-80-1.50-L-D-P-TR



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 8 of 25
Filename: J3.SchDoc		

1

2

3

4

A

A

B

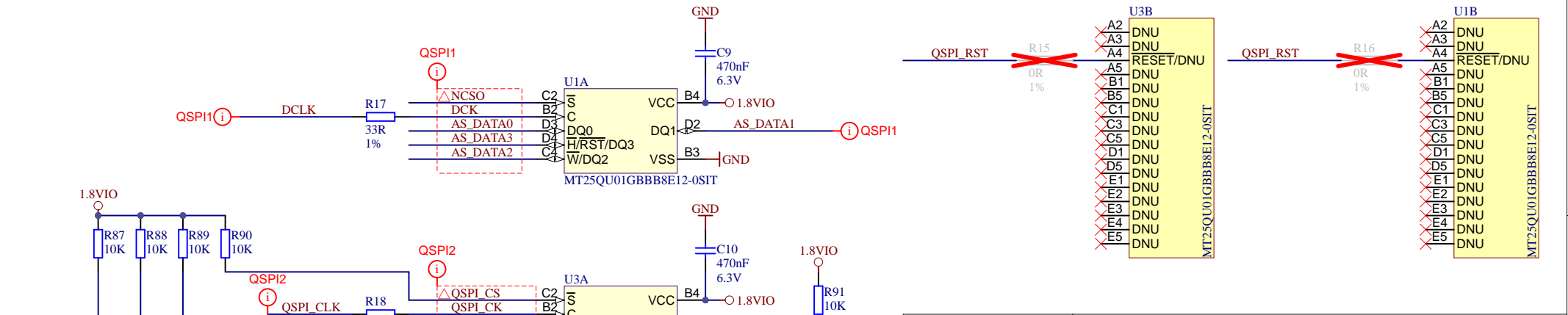
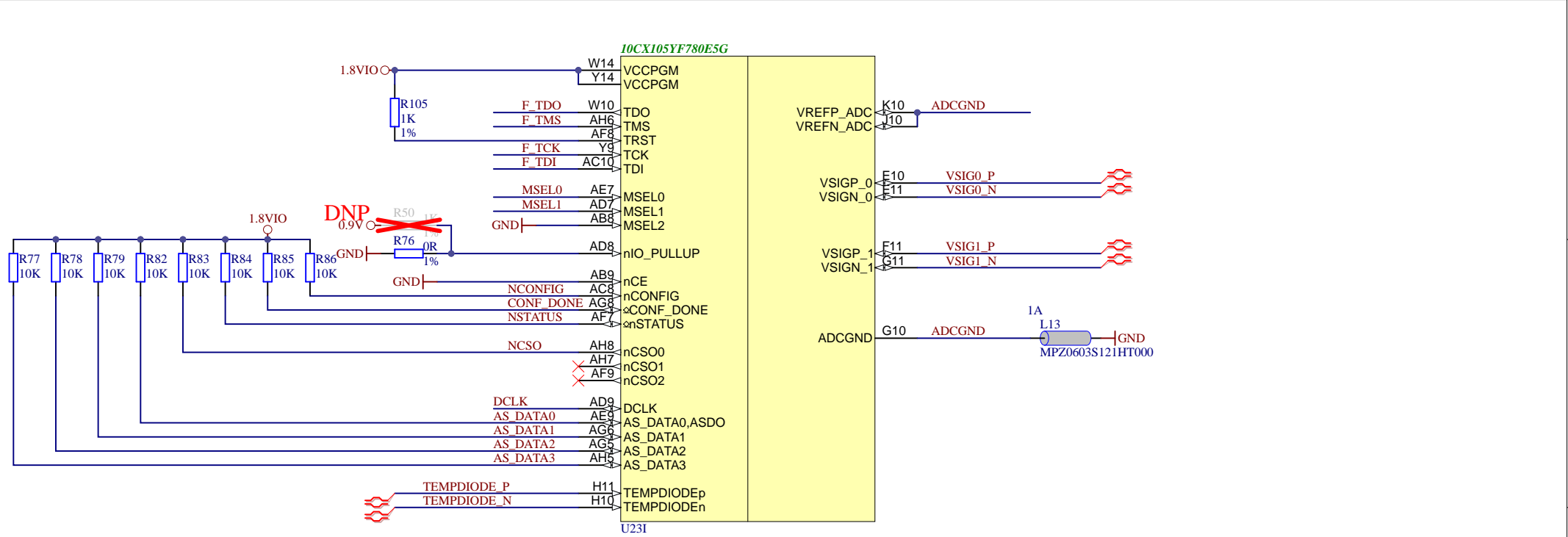
B

C

C

D

D



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page9 of 25
Filename: C10GX_CFG.SchDoc		

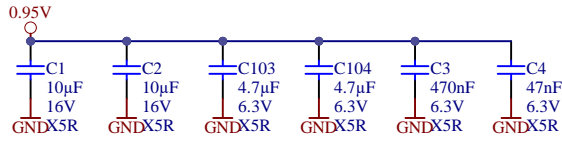
1

2

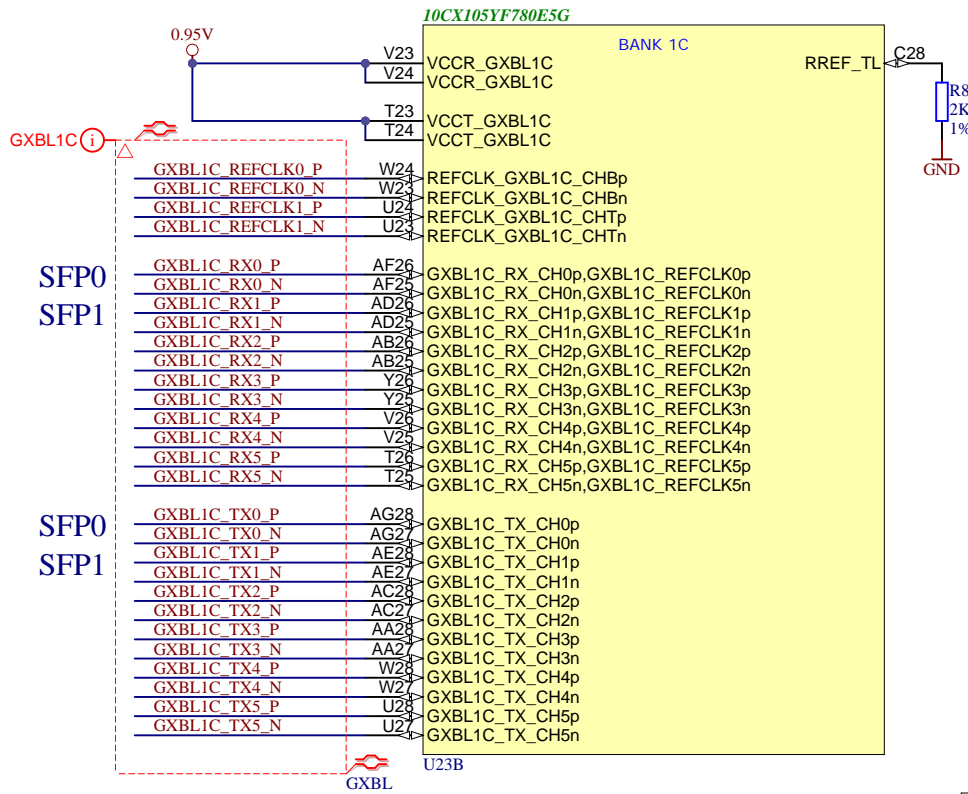
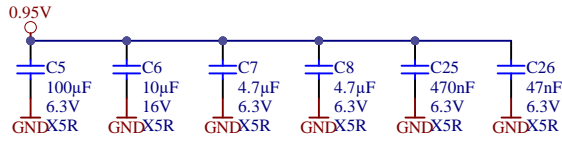

3

4

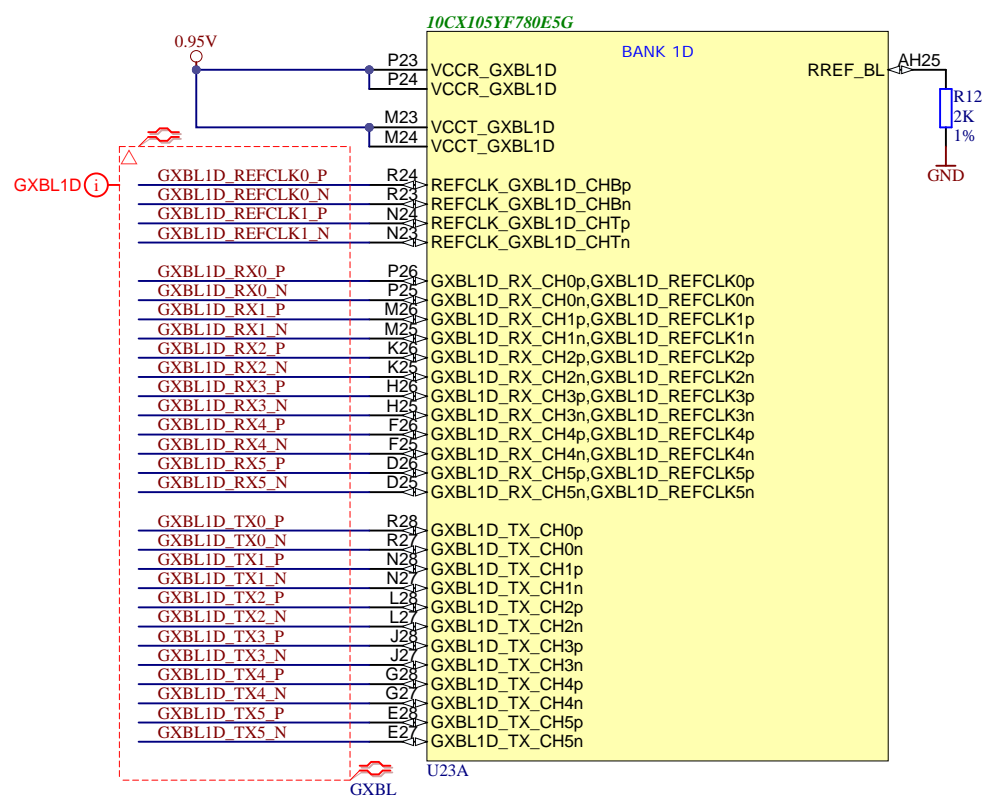
Placed at VCCT_GXB pins




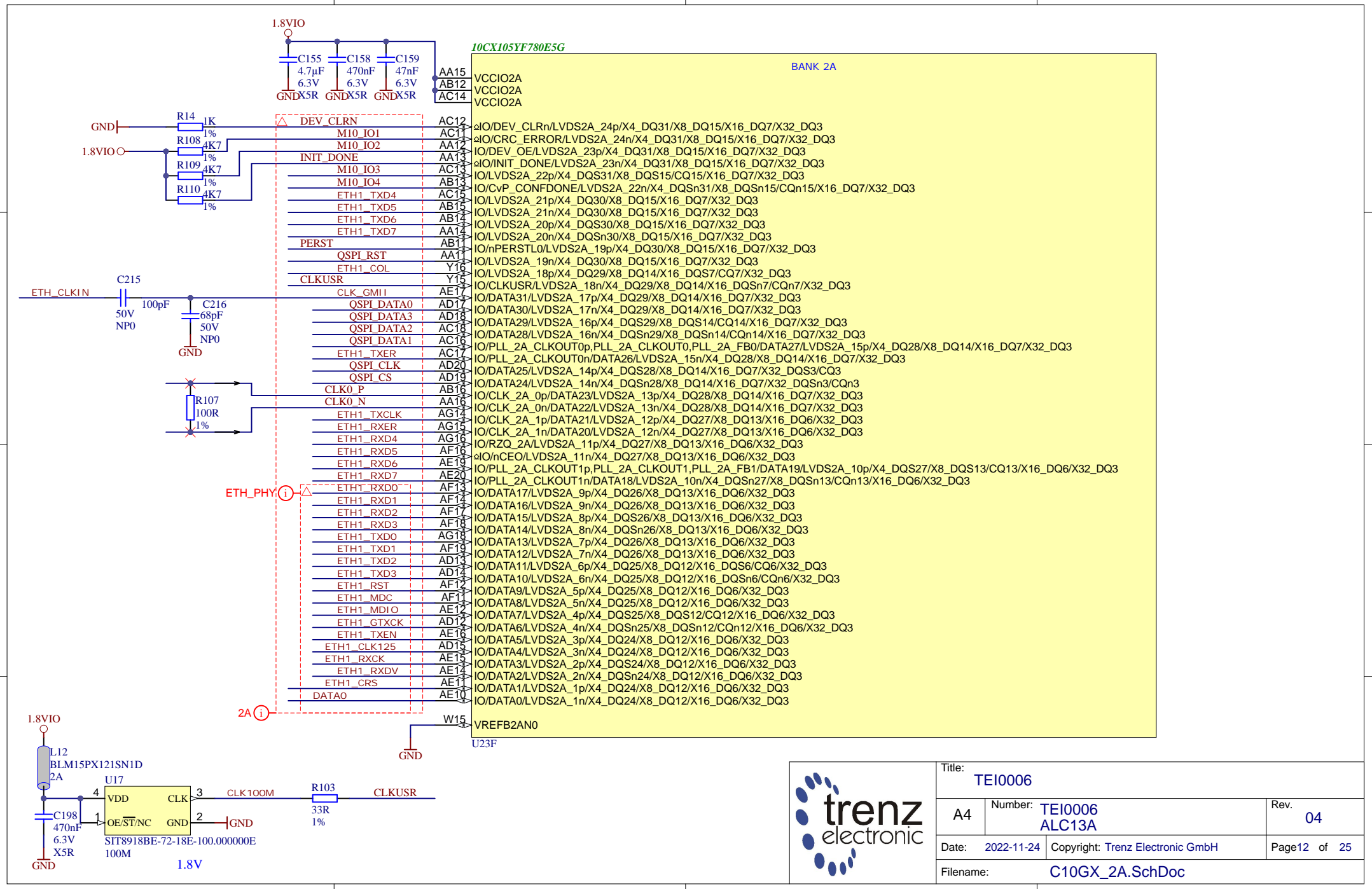
Placed at VCCR_GXB pins

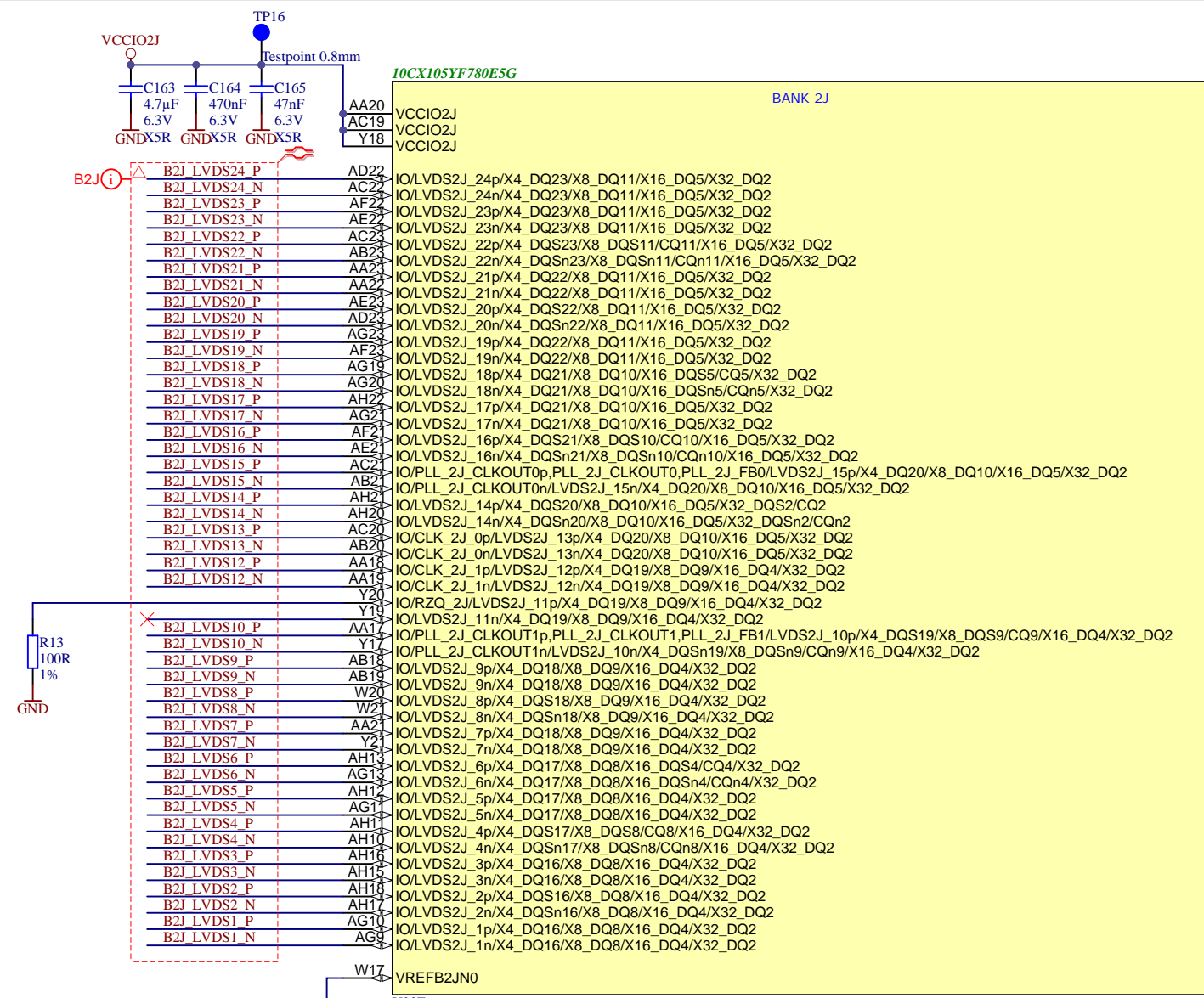
Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 10 of 25
Filename: C10GX_1C.SchDoc		



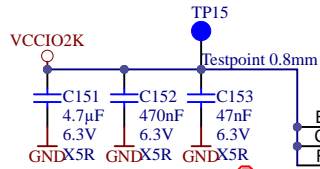
	Title: TEI0006		
	A4	Number: TEI0006 ALC13A	Rev. 04
	Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 11 of 25
	Filename: C10GX_1D.SchDoc		



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	
Page 12 of 25		
Filename: C10GX_2A.SchDoc		



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 13 of 25
Filename: C10GX_2J.SchDoc		



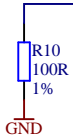
10CX105YF780ESG

BANK 2K

B2K i

B2K LVDS24 P	A11
B2K LVDS24 N	B1
B2K LVDS23 P	A12
B2K LVDS23 N	A1
B2K LVDS22 P	A13
B2K LVDS22 N	B1
B2K LVDS21 P	B12
B2K LVDS21 N	B15
B2K LVDS20 P	C1
B2K LVDS20 N	D1
B2K LVDS19 P	D12
B2K LVDS19 N	E12
B2K LVDS18 P	B26
B2K LVDS18 N	B25
B2K LVDS17 P	A2
B2K LVDS17 N	A22
B2K LVDS16 P	A27
B2K LVDS16 N	A26
B2K LVDS15 P	B2
B2K LVDS15 N	B25
B2K LVDS14 P	B21
B2K LVDS14 N	C2
B2K LVDS13 P	A24
B2K LVDS13 N	A23
B2K LVDS12 P	D15
B2K LVDS12 N	E15
B2K LVDS10 P	B20
B2K LVDS10 N	C20
B2K LVDS9 P	B13
B2K LVDS9 N	B16
B2K LVDS7 P	C15
B2K LVDS7 N	A19
B2K LVDS8 P	A17
B2K LVDS8 N	A16
B2K LVDS6 P	D9
B2K LVDS6 N	D10
B2K LVDS5 P	C5
B2K LVDS5 N	D5
B2K LVDS4 P	A9
B2K LVDS4 N	A8
B2K LVDS3 P	C12
B2K LVDS3 N	C11
B2K LVDS2 P	B10
B2K LVDS2 N	C10
B2K LVDS1 P	B9
B2K LVDS1 N	B8

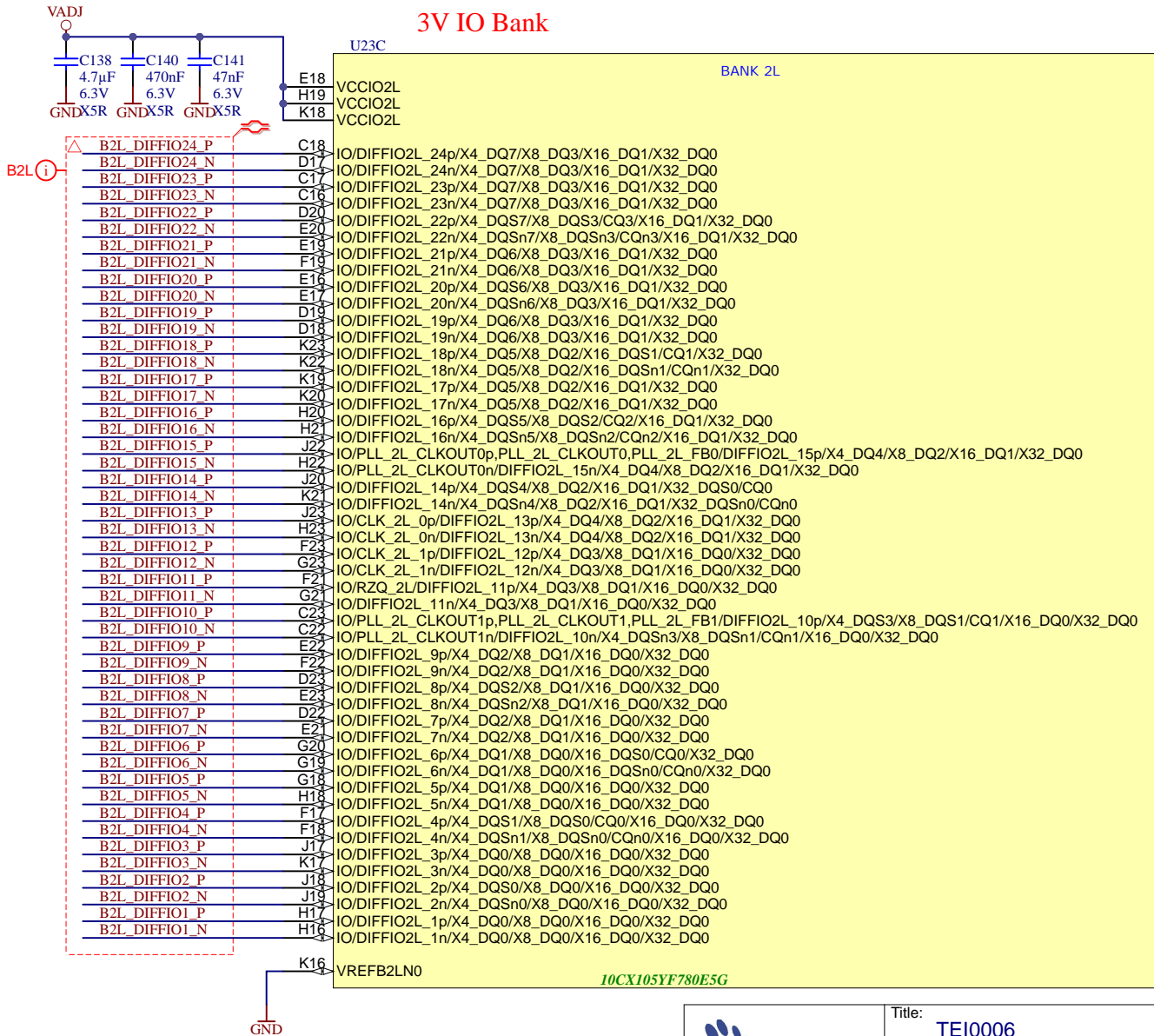
VCCIO2K	B12	IO/LVDS2K_24p/X4_DQ15/X8_DQ7/X16_DQ3/X32_DQ1
VCCIO2K	C14	IO/LVDS2K_24n/X4_DQ15/X8_DQ7/X16_DQ3/X32_DQ1
VCCIO2K	F15	IO/LVDS2K_23p/X4_DQ15/X8_DQ7/X16_DQ3/X32_DQ1
		IO/LVDS2K_23n/X4_DQ15/X8_DQ7/X16_DQ3/X32_DQ1
		IO/LVDS2K_22p/X4_DQS15/X8_DQS7/CQ7/X16_DQ3/X32_DQ1
		IO/LVDS2K_22n/X4_DQSn15/X8_DQSn7/CQn7/X16_DQ3/X32_DQ1
		IO/LVDS2K_21p/X4_DQ14/X8_DQ7/X16_DQ3/X32_DQ1
		IO/LVDS2K_21n/X4_DQ14/X8_DQ7/X16_DQ3/X32_DQ1
		IO/LVDS2K_20p/X4_DQS14/X8_DQ7/X16_DQ3/X32_DQ1
		IO/LVDS2K_20n/X4_DQSn14/X8_DQ7/X16_DQ3/X32_DQ1
		IO/LVDS2K_19p/X4_DQ14/X8_DQ7/X16_DQ3/X32_DQ1
		IO/LVDS2K_19n/X4_DQ14/X8_DQ7/X16_DQ3/X32_DQ1
		IO/LVDS2K_18p/X4_DQ13/X8_DQ6/X16_DQS3/CQ3/X32_DQ1
		IO/LVDS2K_18n/X4_DQ13/X8_DQ6/X16_DQSn3/CQn3/X32_DQ1
		IO/LVDS2K_17p/X4_DQ13/X8_DQ6/X16_DQ3/X32_DQ1
		IO/LVDS2K_17n/X4_DQ13/X8_DQ6/X16_DQ3/X32_DQ1
		IO/LVDS2K_16p/X4_DQS13/X8_DQS6/CQ6/X16_DQ3/X32_DQ1
		IO/LVDS2K_16n/X4_DQSn13/X8_DQSn6/CQn6/X16_DQ3/X32_DQ1
		IO/PLL_2K_CLKOUT0p,PLL_2K_CLKOUT0,PLL_2K_FB0/LVDS2K_15p/X4_DQ12/X8_DQ6/X16_DQ3/X32_DQ1
		IO/PLL_2K_CLKOUT0n/LVDS2K_15n/X4_DQ12/X8_DQ6/X16_DQ3/X32_DQ1
		IO/LVDS2K_14p/X4_DQS12/X8_DQ6/X16_DQ3/X32_DQS1/CQ1
		IO/LVDS2K_14n/X4_DQSn12/X8_DQ6/X16_DQ3/X32_DQSn1/CQn1
		IO/CLK_2K_0p/LVDS2K_13p/X4_DQ12/X8_DQ6/X16_DQ3/X32_DQ1
		IO/CLK_2K_0n/LVDS2K_13n/X4_DQ12/X8_DQ6/X16_DQ3/X32_DQ1
		IO/CLK_2K_1p/LVDS2K_12p/X4_DQ11/X8_DQ5/X16_DQ2/X32_DQ1
		IO/CLK_2K_1n/LVDS2K_12n/X4_DQ11/X8_DQ5/X16_DQ2/X32_DQ1
		IO/RZQ_2K/LVDS2K_11p/X4_DQ11/X8_DQ5/X16_DQ2/X32_DQ1
		IO/LVDS2K_11n/X4_DQ11/X8_DQ5/X16_DQ2/X32_DQ1
		IO/PLL_2K_CLKOUT1p,PLL_2K_CLKOUT1,PLL_2K_FB1/LVDS2K_10p/X4_DQS11/X8_DQS5/CQ5/X16_DQ2/X32_DQ1
		IO/PLL_2K_CLKOUT1n/LVDS2K_10n/X4_DQSn11/X8_DQSn5/CQn5/X16_DQ2/X32_DQ1
		IO/LVDS2K_9p/X4_DQ10/X8_DQ5/X16_DQ2/X32_DQ1
		IO/LVDS2K_9n/X4_DQ10/X8_DQ5/X16_DQ2/X32_DQ1
		IO/LVDS2K_8p/X4_DQS10/X8_DQ5/X16_DQ2/X32_DQ1
		IO/LVDS2K_8n/X4_DQSn10/X8_DQ5/X16_DQ2/X32_DQ1
		IO/LVDS2K_7p/X4_DQ10/X8_DQ5/X16_DQ2/X32_DQ1
		IO/LVDS2K_7n/X4_DQ10/X8_DQ5/X16_DQ2/X32_DQ1
		IO/LVDS2K_6p/X4_DQ9/X8_DQ4/X16_DQS2/CQ2/X32_DQ1
		IO/LVDS2K_6n/X4_DQ9/X8_DQ4/X16_DQSn2/CQn2/X32_DQ1
		IO/LVDS2K_5p/X4_DQ9/X8_DQ4/X16_DQ2/X32_DQ1
		IO/LVDS2K_5n/X4_DQ9/X8_DQ4/X16_DQ2/X32_DQ1
		IO/LVDS2K_4p/X4_DQS9/X8_DQS4/CQ4/X16_DQ2/X32_DQ1
		IO/LVDS2K_4n/X4_DQSn9/X8_DQSn4/CQn4/X16_DQ2/X32_DQ1
		IO/LVDS2K_3p/X4_DQ8/X8_DQ4/X16_DQ2/X32_DQ1
		IO/LVDS2K_3n/X4_DQ8/X8_DQ4/X16_DQ2/X32_DQ1
		IO/LVDS2K_2p/X4_DQS8/X8_DQ4/X16_DQ2/X32_DQ1
		IO/LVDS2K_2n/X4_DQSn8/X8_DQ4/X16_DQ2/X32_DQ1
		IO/LVDS2K_1p/X4_DQ8/X8_DQ4/X16_DQ2/X32_DQ1
		IO/LVDS2K_1n/X4_DQ8/X8_DQ4/X16_DQ2/X32_DQ1



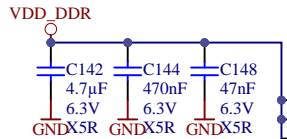
U23D



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 14 of 25
Filename: C10GX_2K.SchDoc		



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 15 of 25
Filename: C10GX_2L.SchDoc		



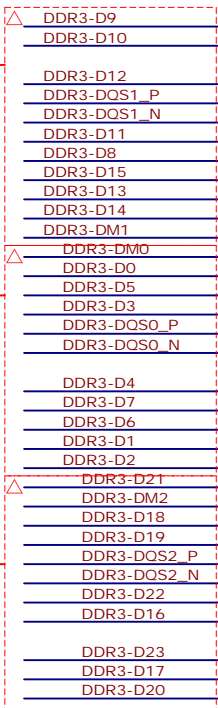
10CX105YF780ESG

BANK 3A

DDR_DATA1 (i)

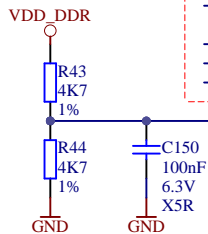
DDR_DATA0 (i)

DDR_DATA2 (i)

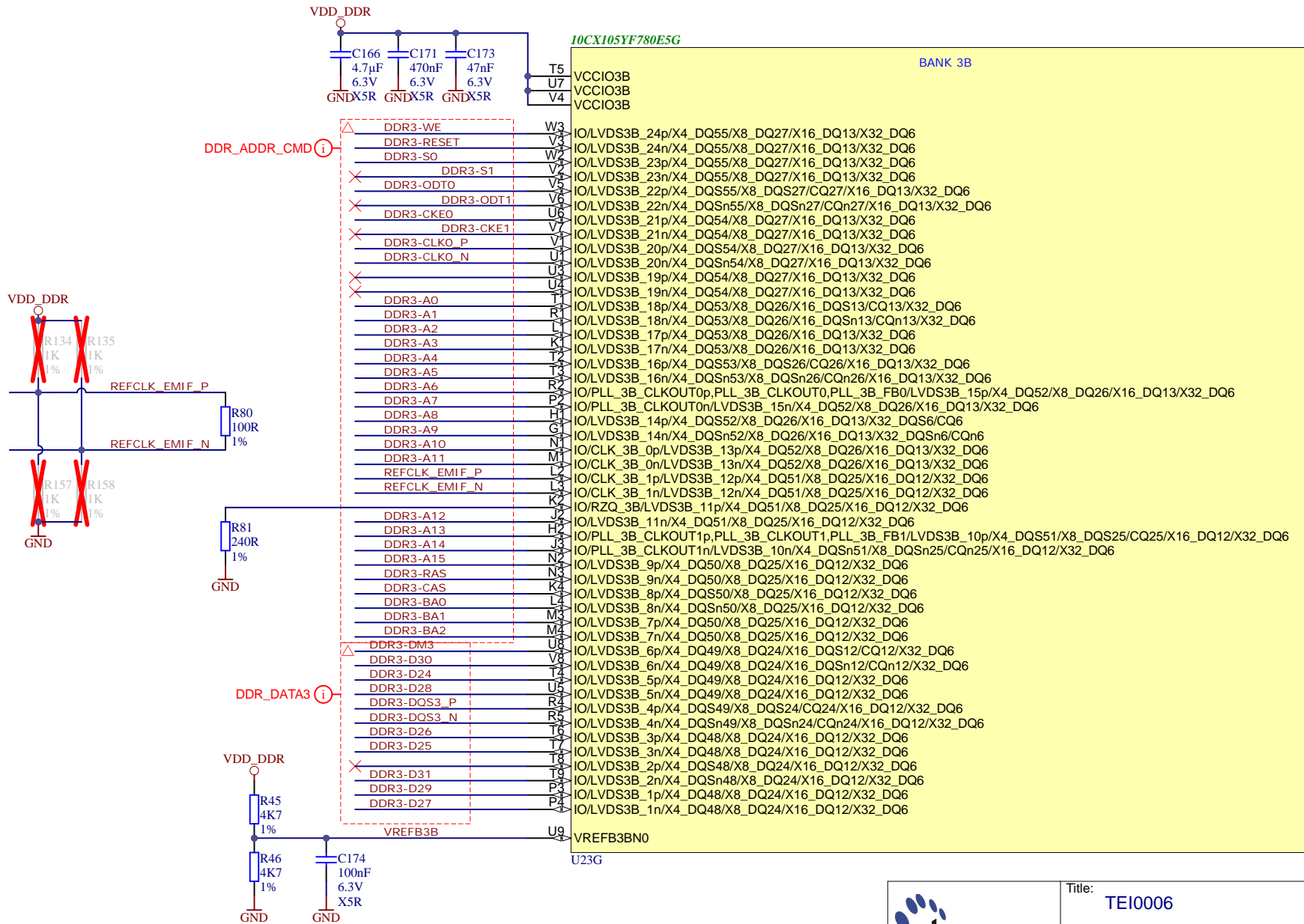


AA5	VCCIO3A
W6	VCCIO3A
Y8	VCCIO3A
AF6	IO/LVDS3A_22p/X4_DQS63/X8_DQS31/CQ31/X16_DQ15/X32_DQ7
AE6	IO/LVDS3A_22n/X4_DQS63/X8_DQS31/CQ31/X16_DQ15/X32_DQ7
AC6	IO/LVDS3A_21p/X4_DQ62/X8_DQ31/X16_DQ15/X32_DQ7
AC7	IO/LVDS3A_21n/X4_DQ62/X8_DQ31/X16_DQ15/X32_DQ7
AE4	IO/LVDS3A_20p/X4_DQS62/X8_DQ31/X16_DQ15/X32_DQ7
AD4	IO/LVDS3A_20n/X4_DQS62/X8_DQ31/X16_DQ15/X32_DQ7
AH4	IO/LVDS3A_19p/X4_DQ62/X8_DQ31/X16_DQ15/X32_DQ7
AH5	IO/LVDS3A_19n/X4_DQ62/X8_DQ31/X16_DQ15/X32_DQ7
AG3	IO/LVDS3A_18p/X4_DQ61/X8_DQ30/X16_DQS15/CQ15/X32_DQ7
AF3	IO/LVDS3A_18n/X4_DQ61/X8_DQ30/X16_DQS15/CQ15/X32_DQ7
AG1	IO/LVDS3A_17p/X4_DQ61/X8_DQ30/X16_DQ15/X32_DQ7
AF2	IO/LVDS3A_17n/X4_DQ61/X8_DQ30/X16_DQ15/X32_DQ7
AE2	IO/LVDS3A_16p/X4_DQS61/X8_DQS30/CQ30/X16_DQ15/X32_DQ7
AD2	IO/LVDS3A_16n/X4_DQS61/X8_DQS30/CQ30/X16_DQ15/X32_DQ7
AC2	IO/PLL_3A_CLKOUT0p,PLL_3A_CLKOUT0,PLL_3A_FB0/LVDS3A_15p/X4_DQ60/X8_DQ30/X16_DQ15/X32_DQ7
AC3	IO/PLL_3A_CLKOUT0n/LVDS3A_15n/X4_DQ60/X8_DQ30/X16_DQ15/X32_DQ7
AE1	IO/LVDS3A_14p/X4_DQS60/X8_DQ30/X16_DQ15/X32_DQS7/CQ7
AF4	IO/LVDS3A_14n/X4_DQS60/X8_DQ30/X16_DQ15/X32_DQS7/CQ7
AD3	IO/CLK_3A_0p/LVDS3A_13p/X4_DQ60/X8_DQ30/X16_DQ15/X32_DQ7
AC3	IO/CLK_3A_0n/LVDS3A_13n/X4_DQ60/X8_DQ30/X16_DQ15/X32_DQ7
AA7	IO/CLK_3A_1p/LVDS3A_12p/X4_DQ59/X8_DQ29/X16_DQ14/X32_DQ7
AA8	IO/CLK_3A_1n/LVDS3A_12n/X4_DQ59/X8_DQ29/X16_DQ14/X32_DQ7
AA4	IO/RZQ_3A/LVDS3A_11p/X4_DQ59/X8_DQ29/X16_DQ14/X32_DQ7
AA5	IO/LVDS3A_11n/X4_DQ59/X8_DQ29/X16_DQ14/X32_DQ7
AA2	IO/PLL_3A_CLKOUT1p,PLL_3A_CLKOUT1,PLL_3A_FB1/LVDS3A_10p/X4_DQS59/X8_DQS29/CQ29/X16_DQ14/X32_DQ7
AB3	IO/PLL_3A_CLKOUT1n/LVDS3A_10n/X4_DQS59/X8_DQS29/CQ29/X16_DQ14/X32_DQ7
AB6	IO/LVDS3A_9p/X4_DQ58/X8_DQ29/X16_DQ14/X32_DQ7
AB7	IO/LVDS3A_9n/X4_DQ58/X8_DQ29/X16_DQ14/X32_DQ7
AB1	IO/LVDS3A_8p/X4_DQS58/X8_DQ29/X16_DQ14/X32_DQ7
AA1	IO/LVDS3A_8n/X4_DQS58/X8_DQ29/X16_DQ14/X32_DQ7
AC5	IO/LVDS3A_7p/X4_DQ58/X8_DQ29/X16_DQ14/X32_DQ7
AB4	IO/LVDS3A_7n/X4_DQ58/X8_DQ29/X16_DQ14/X32_DQ7
AA9	IO/LVDS3A_6p/X4_DQ57/X8_DQ28/X16_DQS14/CQ14/X32_DQ7
AA8	IO/LVDS3A_6n/X4_DQ57/X8_DQ28/X16_DQS14/CQ14/X32_DQ7
Y1	IO/LVDS3A_5p/X4_DQ57/X8_DQ28/X16_DQ14/X32_DQ7
W5	IO/LVDS3A_5n/X4_DQ57/X8_DQ28/X16_DQ14/X32_DQ7
Y2	IO/LVDS3A_4p/X4_DQS57/X8_DQS28/CQ28/X16_DQ14/X32_DQ7
Y3	IO/LVDS3A_4n/X4_DQS57/X8_DQS28/CQ28/X16_DQ14/X32_DQ7
Y6	IO/LVDS3A_3p/X4_DQ56/X8_DQ28/X16_DQ14/X32_DQ7
Y8	IO/LVDS3A_3n/X4_DQ56/X8_DQ28/X16_DQ14/X32_DQ7
W7	IO/LVDS3A_2p/X4_DQS56/X8_DQ28/X16_DQ14/X32_DQ7
W4	IO/LVDS3A_2n/X4_DQS56/X8_DQ28/X16_DQ14/X32_DQ7
Y4	IO/LVDS3A_1p/X4_DQ56/X8_DQ28/X16_DQ14/X32_DQ7
Y5	IO/LVDS3A_1n/X4_DQ56/X8_DQ28/X16_DQ14/X32_DQ7

VREFB3A0 U23H



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 16 of 25
Filename: C10GX_3A.SchDoc		



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 17 of 25
Filename: C10GX_3B.SchDoc		

1

2

3

4

A

A

B

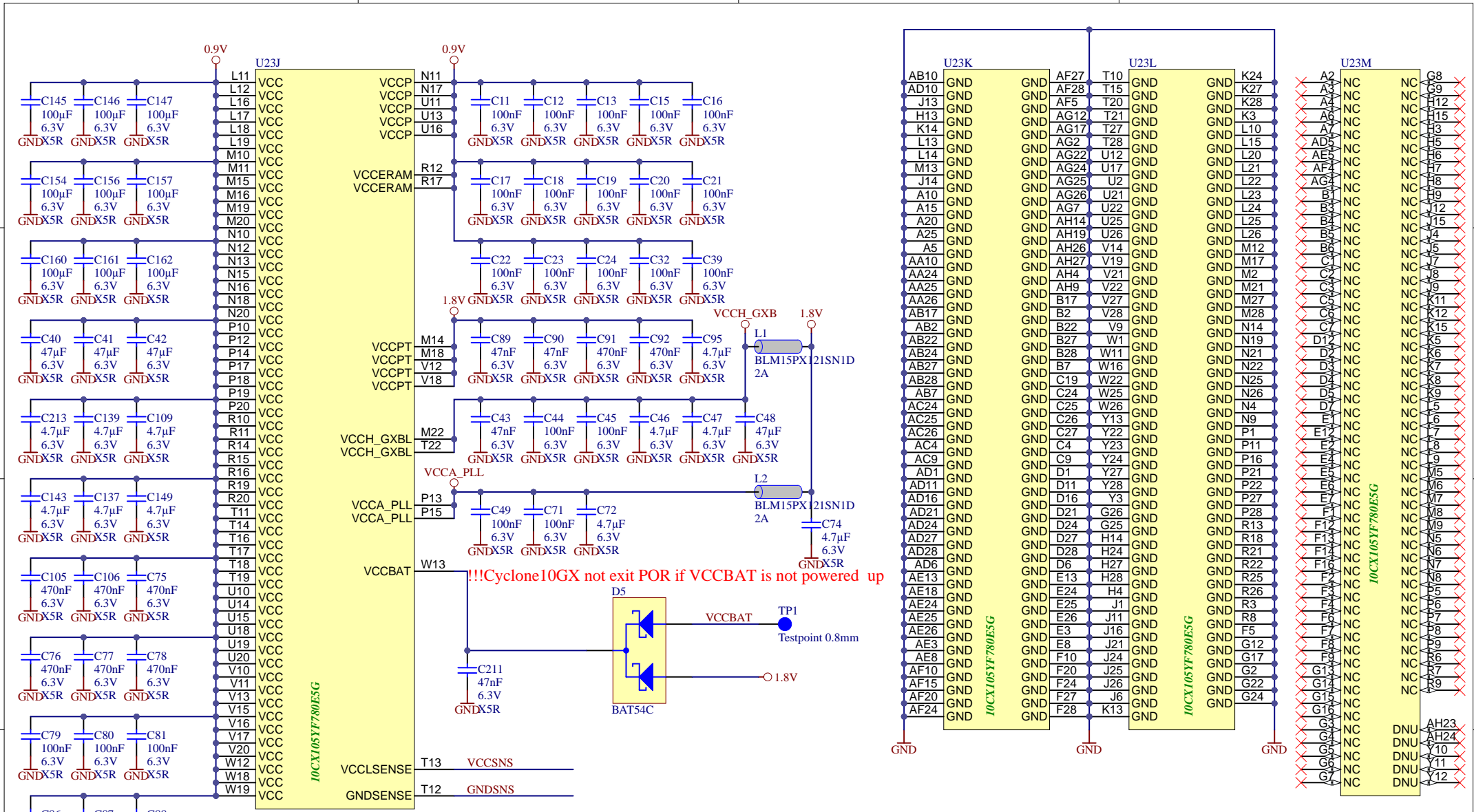
B

C

C

D

D



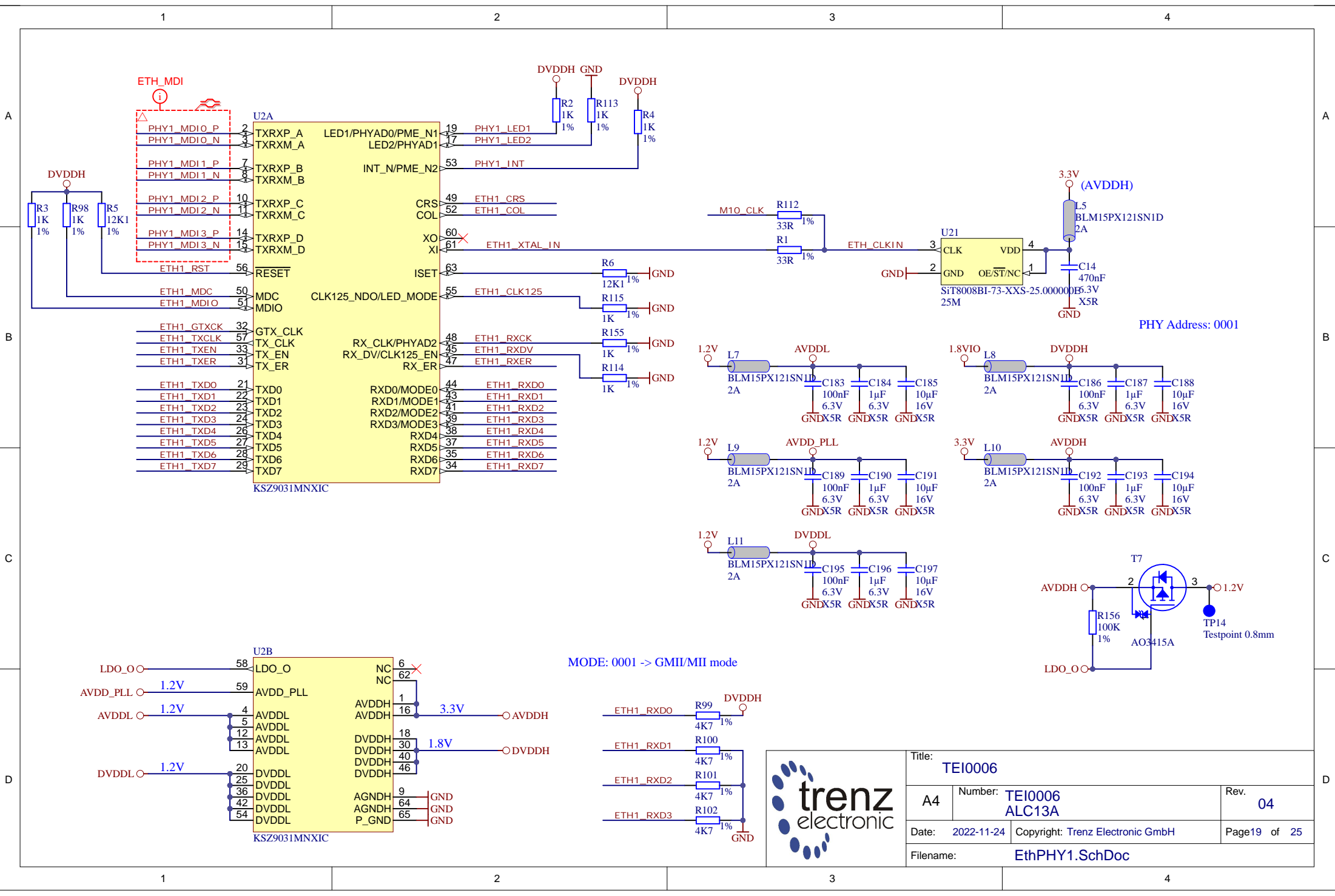
Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 18 of 25
Filename: C10GX_PWR.SchDoc		

1

2

3

4

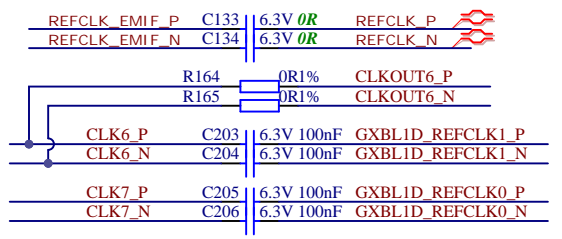
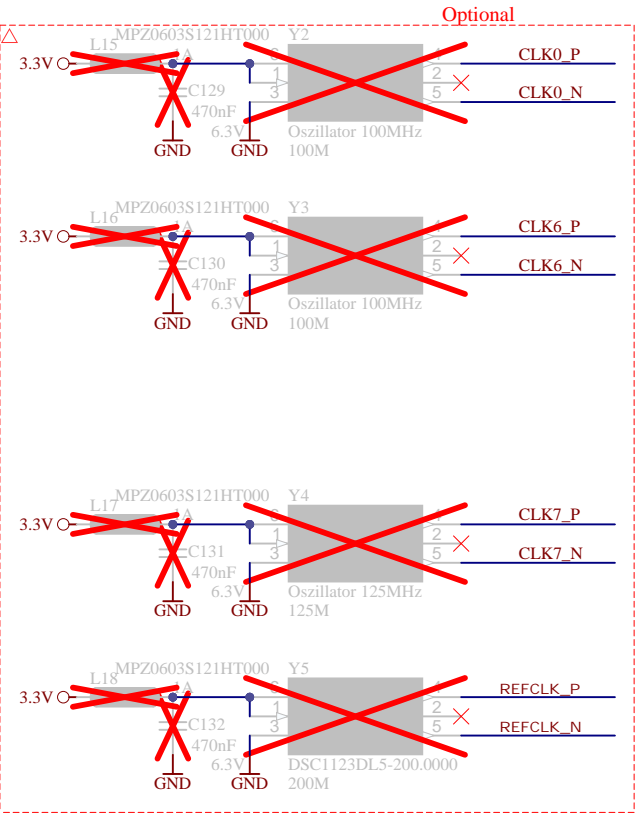
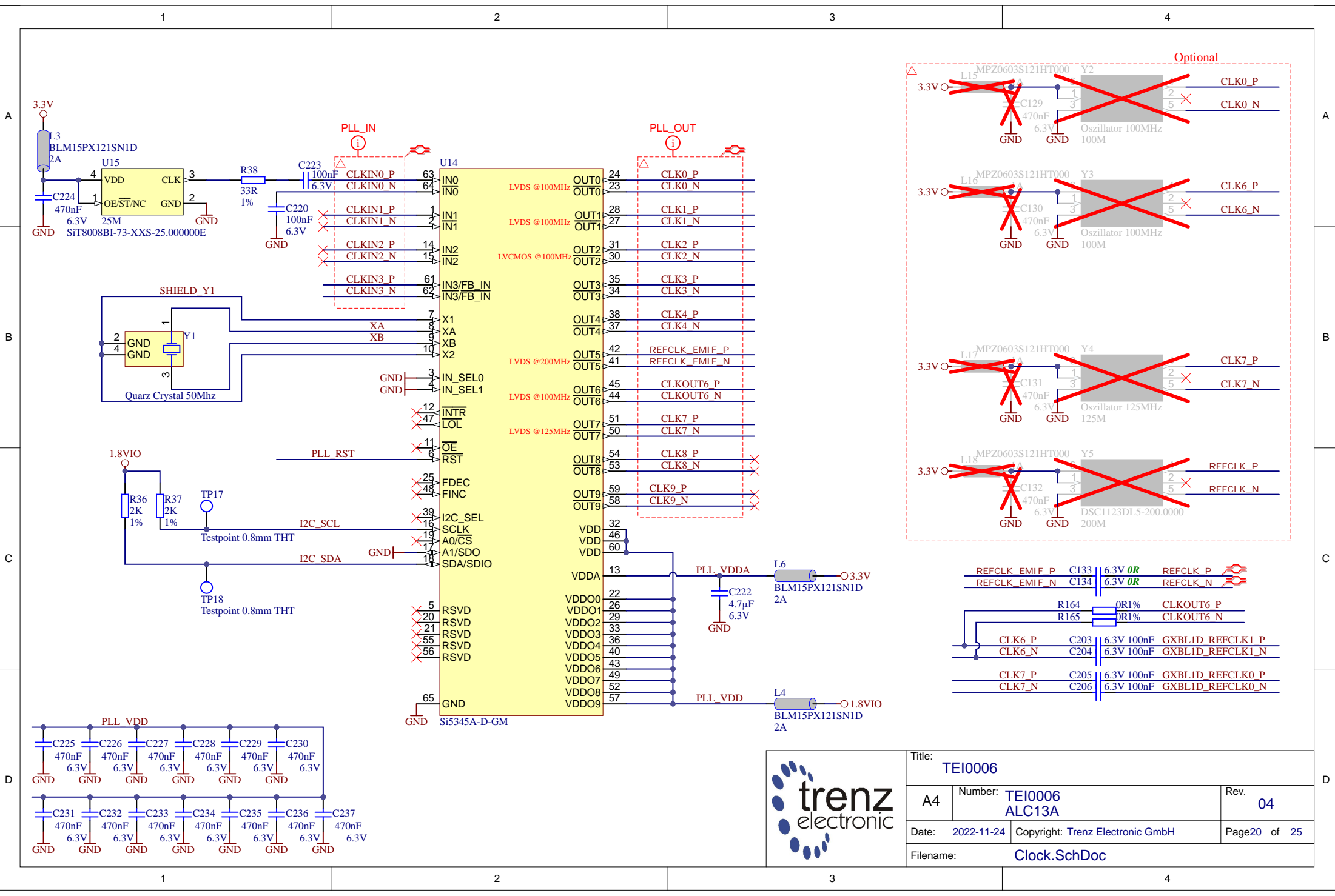


MODE: 0001 -> GMII/MII mode

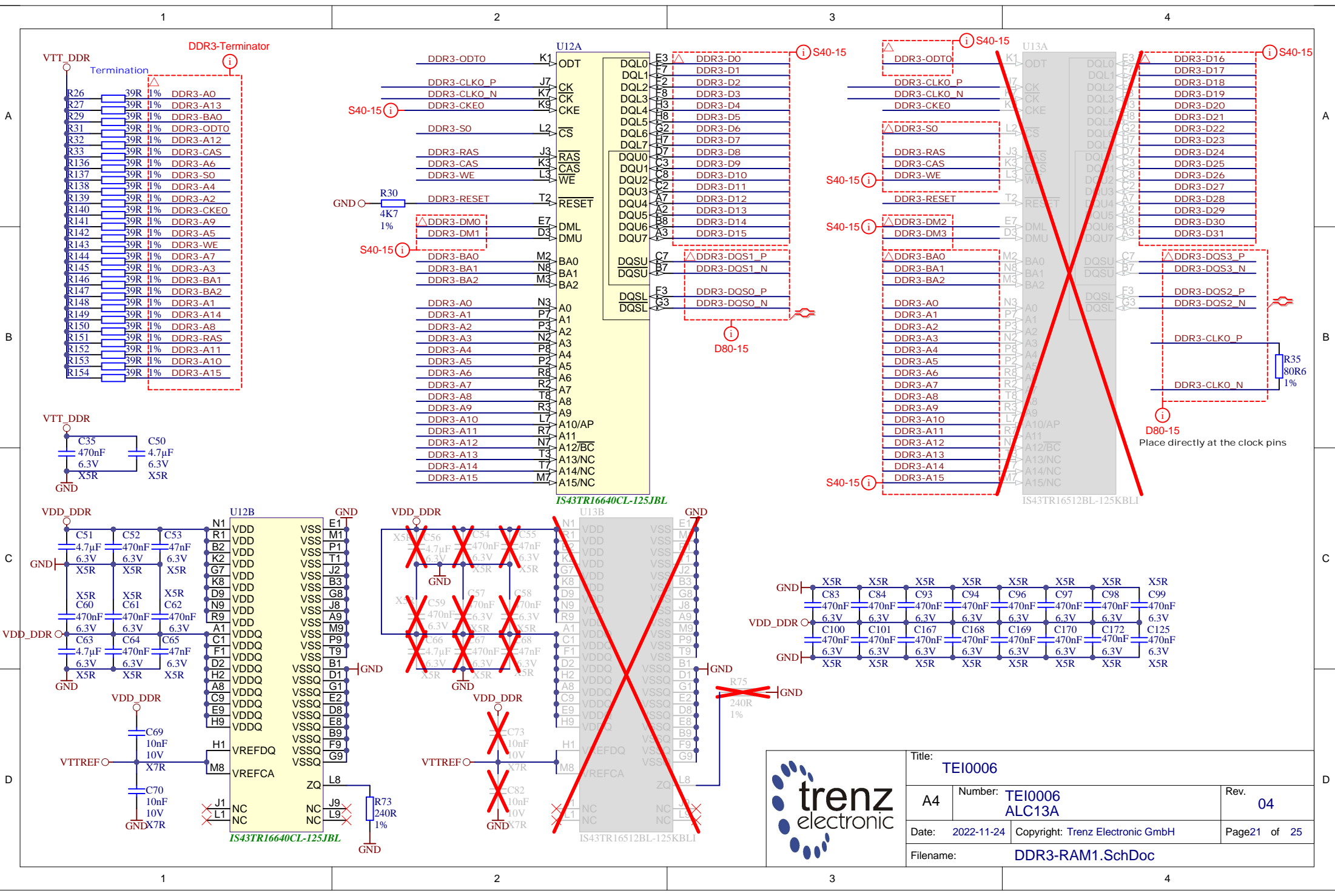
PHY Address: 0001



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 19 of 25
Filename: EthPHY1_SchDoc		

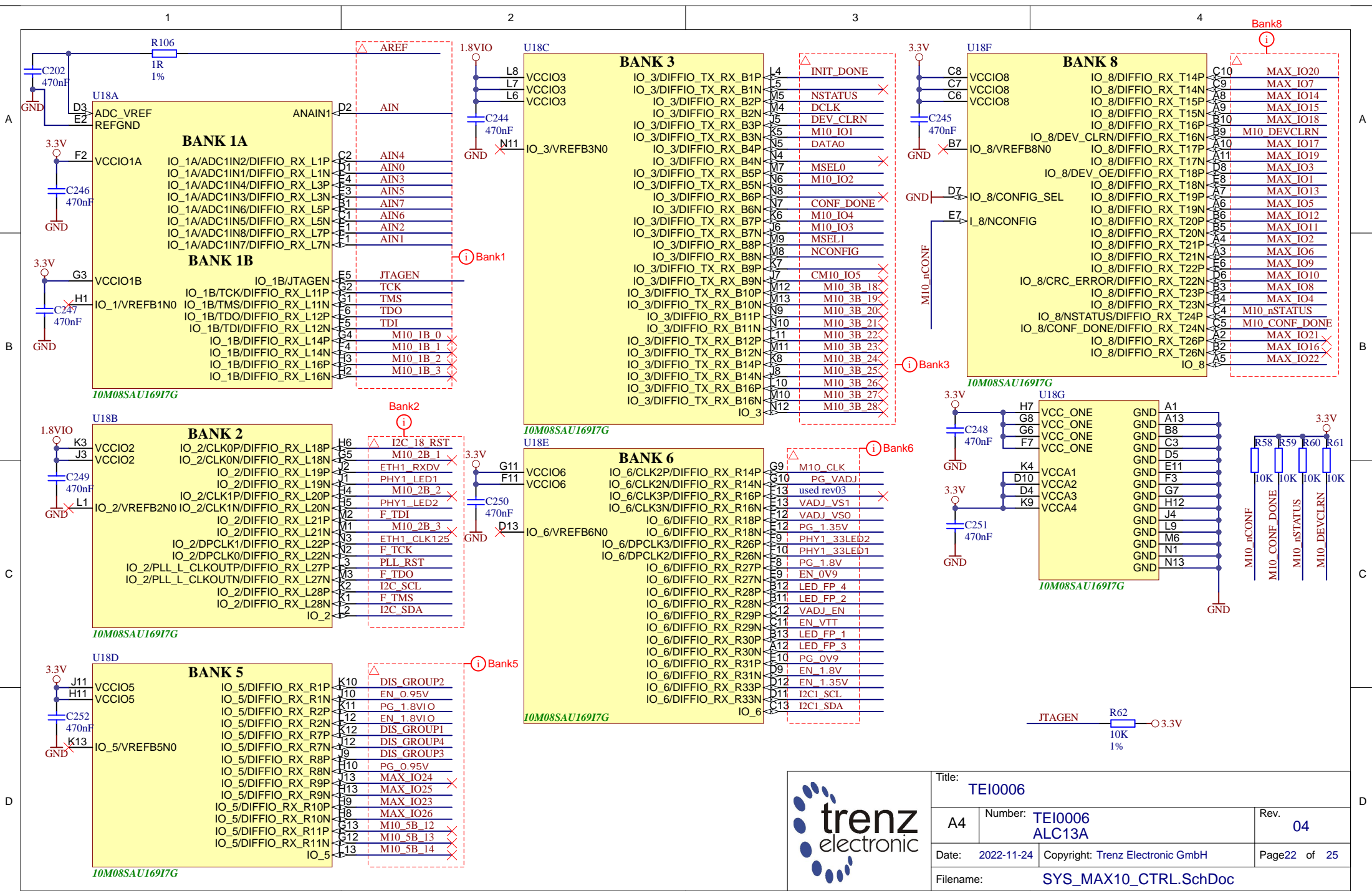


Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 20 of 25
Filename: Clock.SchDoc		

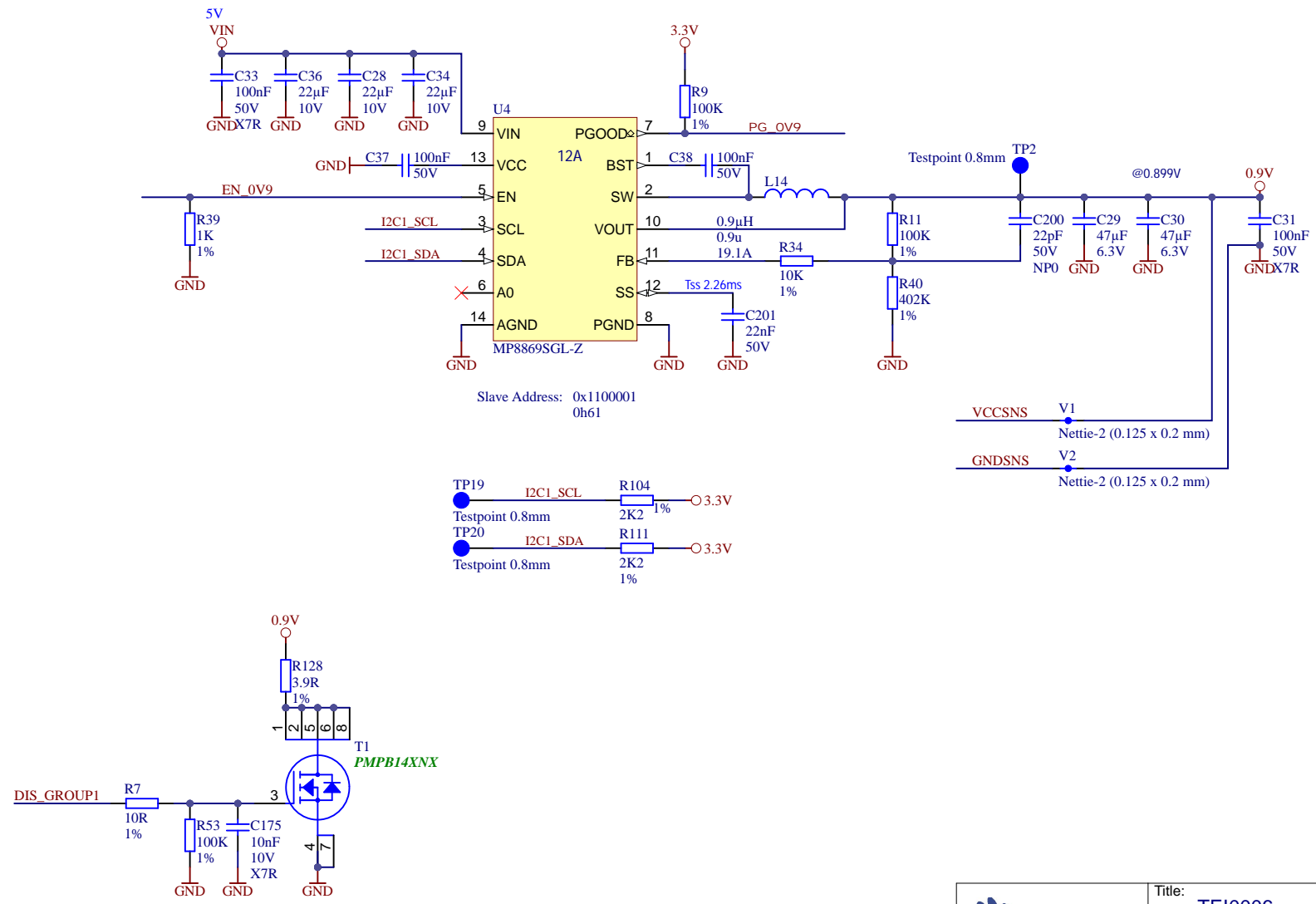


Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 21 of 25
Filename: DDR3-RAM1.SchDoc		

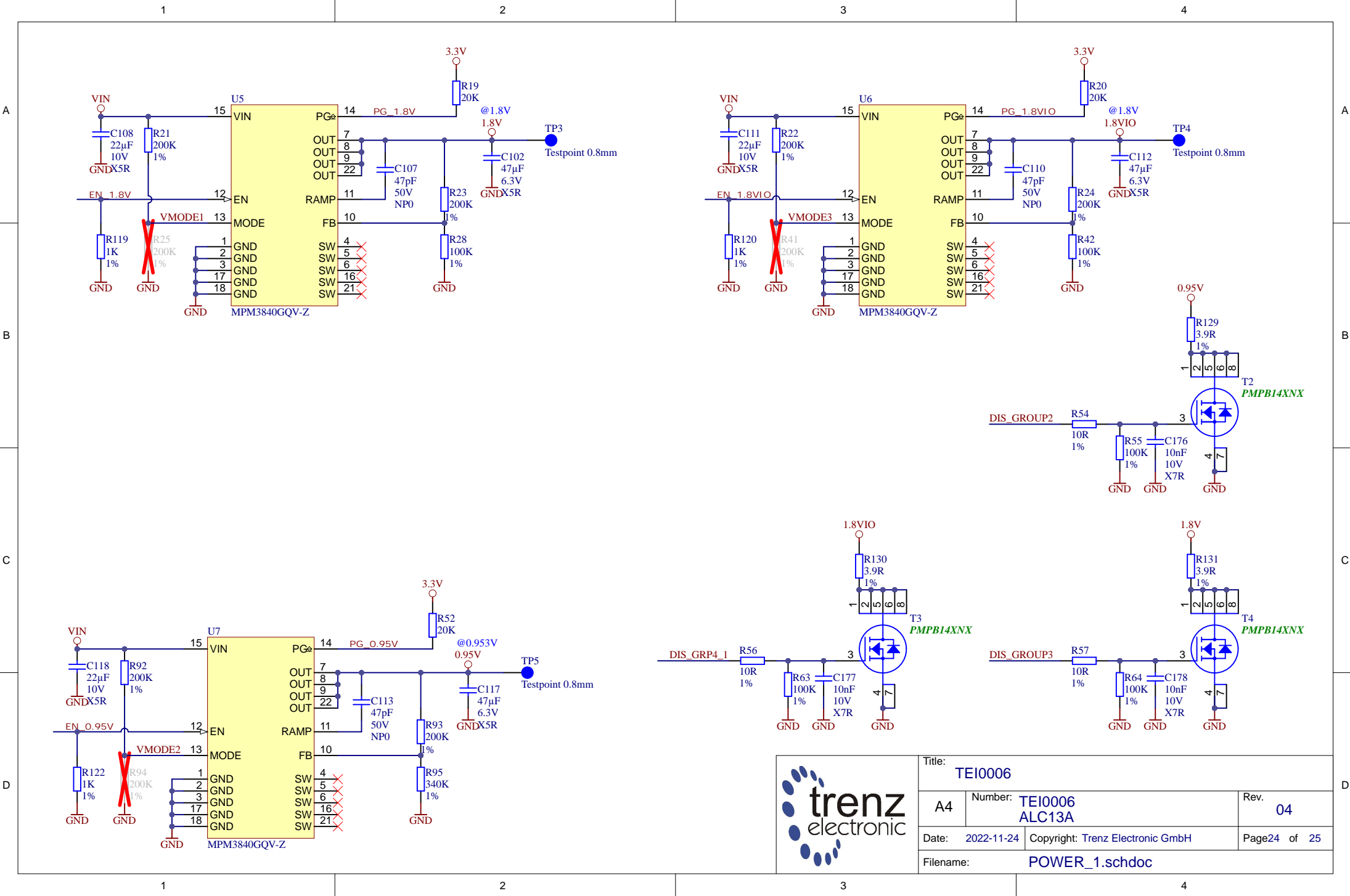
Place directly at the clock pins



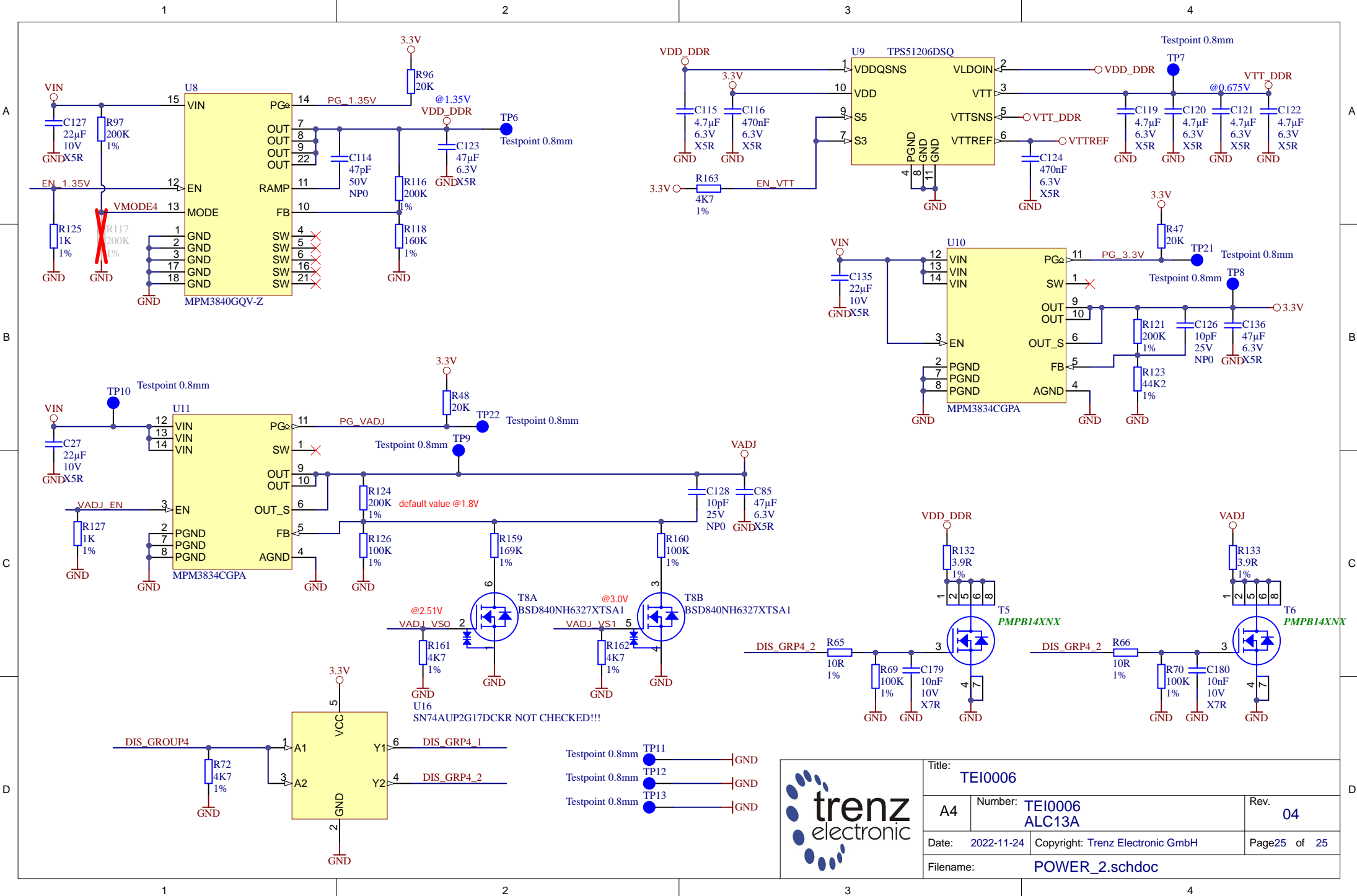
Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 22 of 25
Filename: SYS_MAX10_CTRL.SchDoc		



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page23 of 25
Filename: PWR_CORE.SchDoc		



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page24 of 25
Filename: POWER_1.schdoc		



Title: TEI0006		
A4	Number: TEI0006 ALC13A	Rev. 04
Date: 2022-11-24	Copyright: Trenz Electronic GmbH	Page 25 of 25
Filename: POWER_2.schdoc		