
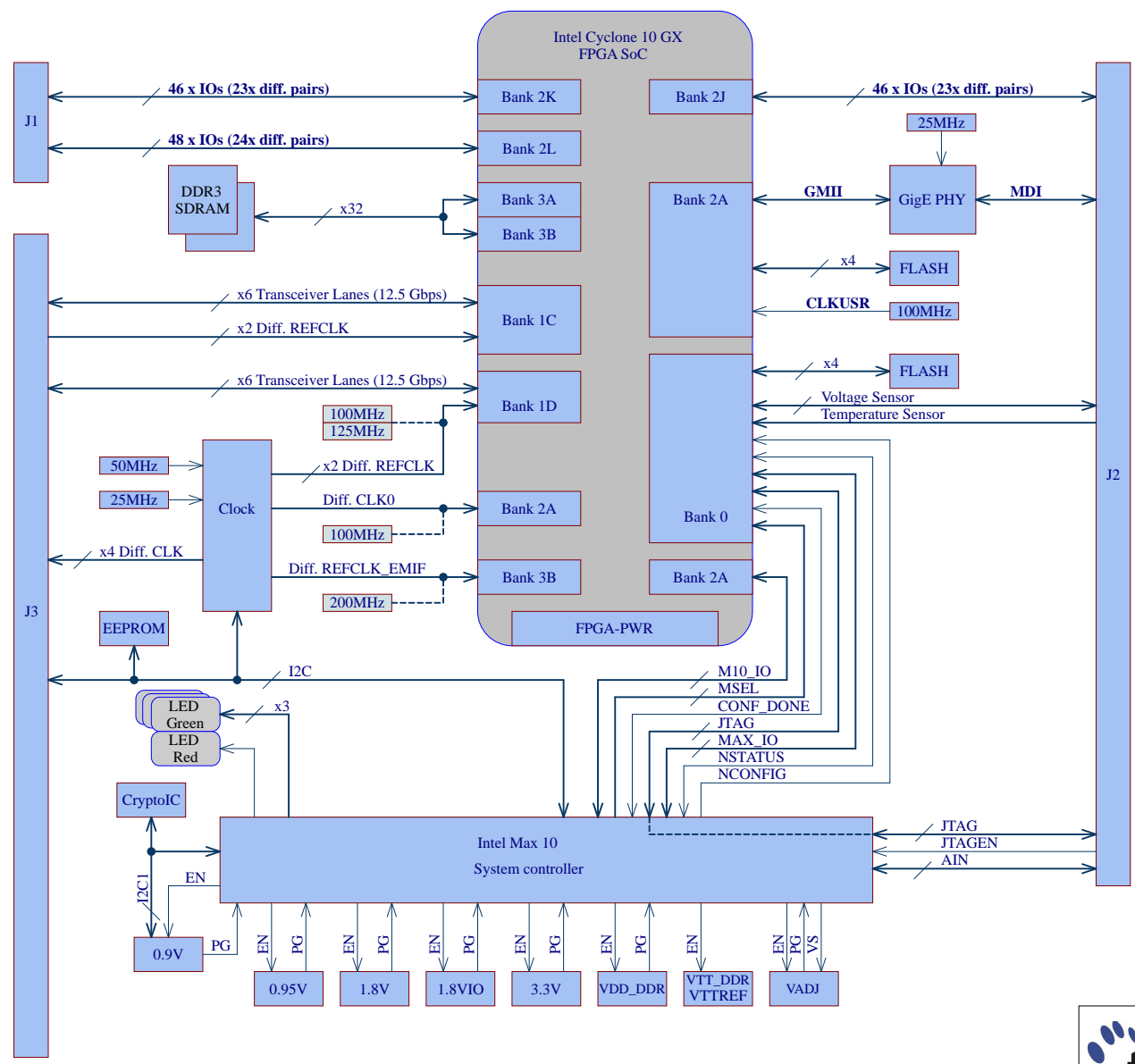


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	Title: TEI0006 - Legal Notices		
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- U_Revision Changes
- U_TEI0006
- U_Power_Diagram

Special notes:

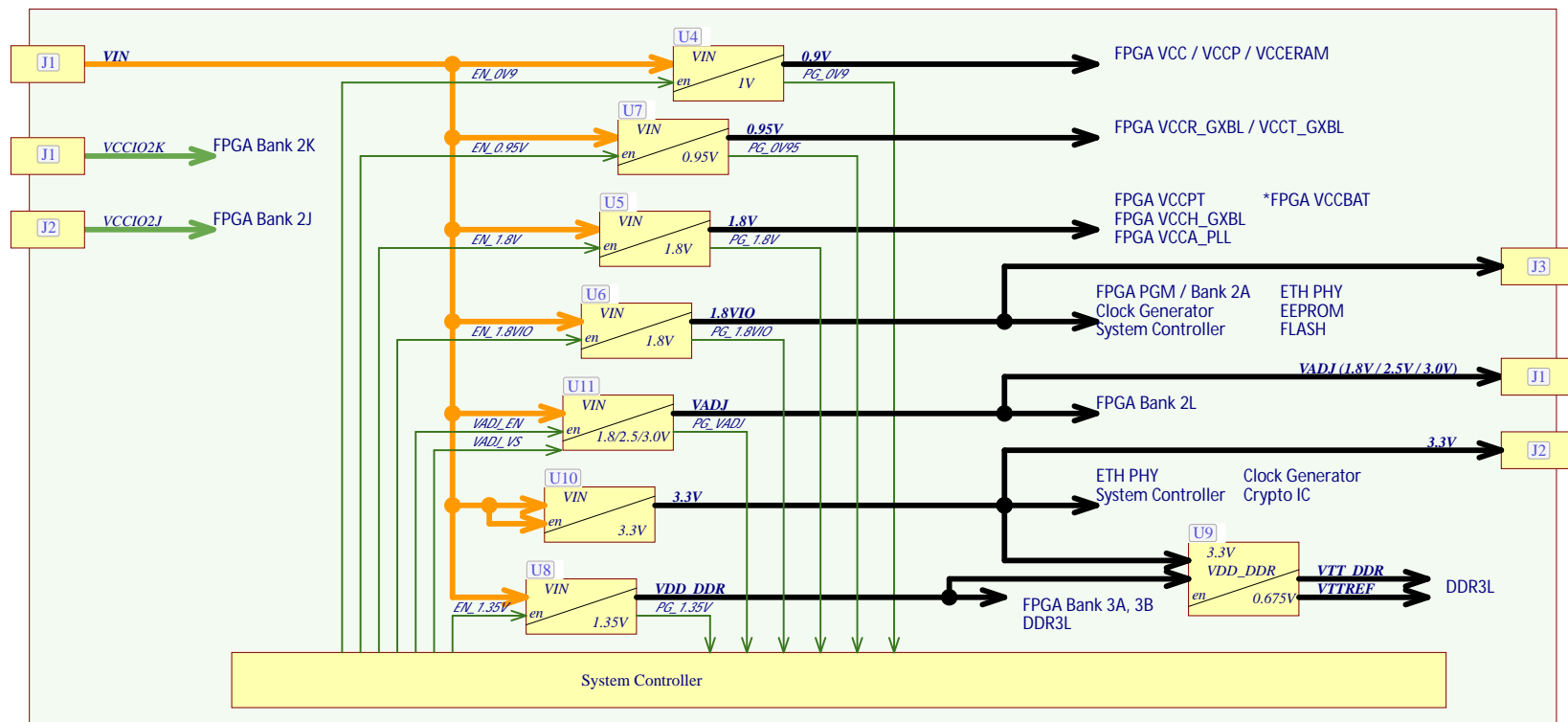


Title: TEI0006 - System Overview		
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REV	Description	
-01	Initial revision	VT
-02	1) VT: added MEMS 100MHz clock oscillator to CLKUSR 2) VT: remove CLKUSR from J2 3) VT: replaced Si510 to SiT8008/CM3225-4pad 4) VT: remove DEVCLRN from J2, added pull-up 5) VT: remove M10_nSTATUS from J2, added pull-up 6) VT: Added optional CryptoAuthentication chip U19 (DNP)	VT
-03	1) VT: fixed CLK connections (CLK's from FMC (on Baseboard) directly connected to GXBLIC bank) 2) VT: added heatsink 3) VT: full upd LIB 4) VT: added Legal Notices sheet	VT
	5) VY: replaced not available transistors T1-T6 AON2240 to PMPB14XNX	VY
-04	1) VT: replaced EOL Power regulators: a) U4: EN63A0QI -> MP8869SGL-Z b) U5,U6,U7,U8: EN6340QI -> MPM3840GQV-Z c) U10, U11: EP53A8HQI -> MPM3834CGPA d) U9: EV1320QI -> TPS51206DSQ 2) VT: replaced not available buffer U16: NC7WZ16P6X ->SN74AUP2G17DCKR 3) VT: added dual transistor T8 for select VADJ Voltage (1.8V, 2.5V, 3.0V) 4) VT: remove signals VADJ_VS2 and PG_VTT from System Controller U18 5) VT: added DCDC I2C to System Controller U18 6) VT: added Testpoints to I2C1 I2C bus 7) VT: added optional MEMS LVDS Oscillators Y2,Y3,Y4,Y5 8) VT: remove Resistors R47,R48,R49,R51 9) VT: added optional Termination to REFCLK_EMIF 10) VT: U19-> use I2C 3.3V 11) VT: added diode D5 for VCCBAT 12) VT: added signal PG_VADJ to System Controller U18 13) VT: changed Commercial grade to Industrial for System Controller U18	VT

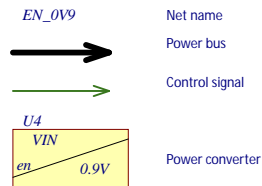
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Power-on sequencing:

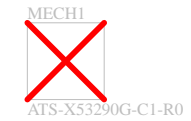
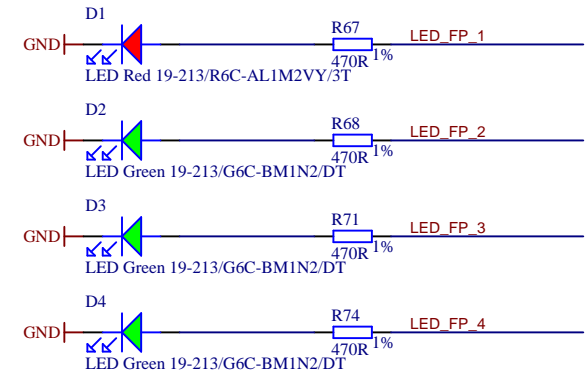
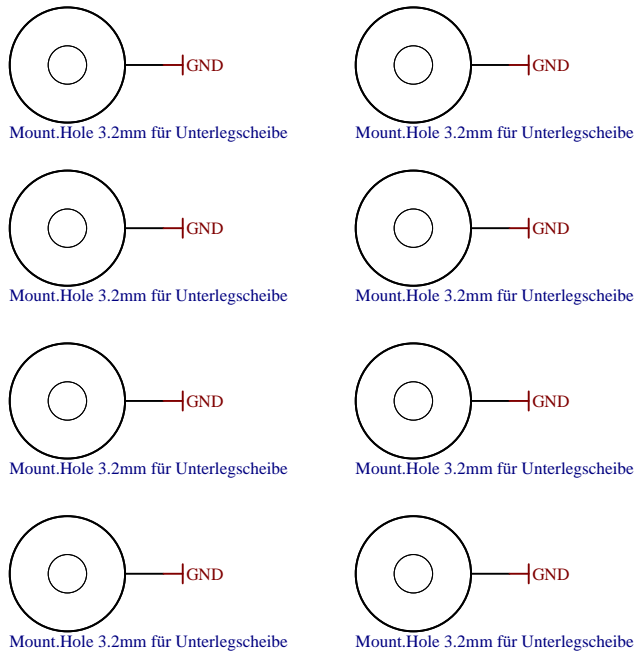


Recommended Operating Conditions

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	5V	+/-5%	Micromodule Power	Mandatory
VCCIO2K	IN	1.2 - 1.8V	+/-3%	IO Bank 2K	-
VCCIO2J	IN	1.2 - 1.8V	+/-3%	IO Bank 2J	-
1.8VIO	OUT	1.8V	+/-3%	For Carrier card Periphery	-
VADJ	OUT	1.8 - 3.0V	+/-3%	For Carrier card Periphery	Voltage set by System Controller
3.3V	OUT	3.3V	+/-3%	For Carrier card Periphery	-



			Title: TEI0006 - Power Diagram	
			A4	Number: TEI0006 ALE13A
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Filename: Power_Diagram.SchDoc				



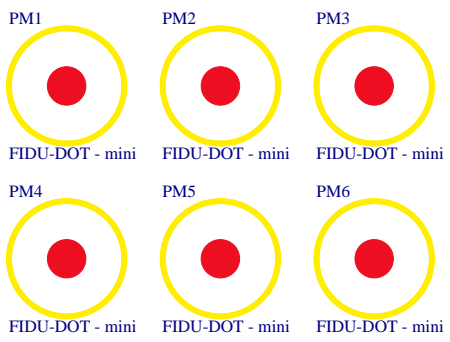
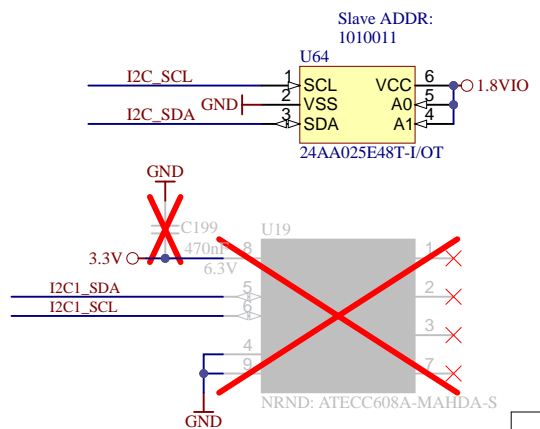
UKCA
 UKCA Logo on Top Overlay
 UKCA-TOOVERLAY

MECH2
 TE Address Overlay
 LOGO ADDRESS

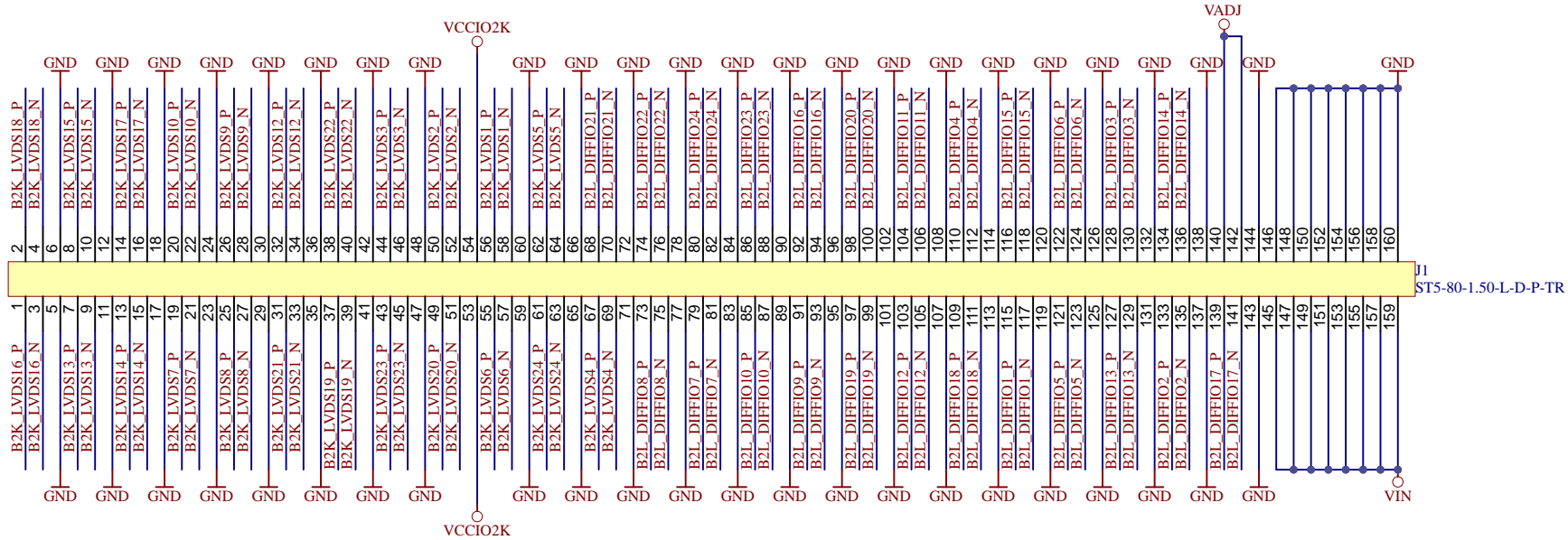
LOGO1
 TE Logo PRINT Layer
 LOGO PRINT

Assembly variant	ALE13A
Created by	VT
Modified by	
Modified at	2023-05-03
SVN Revision	17814

Serial
 Serialnummer 6,3 x 6,3mm



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1

2

3

4

A

A

B

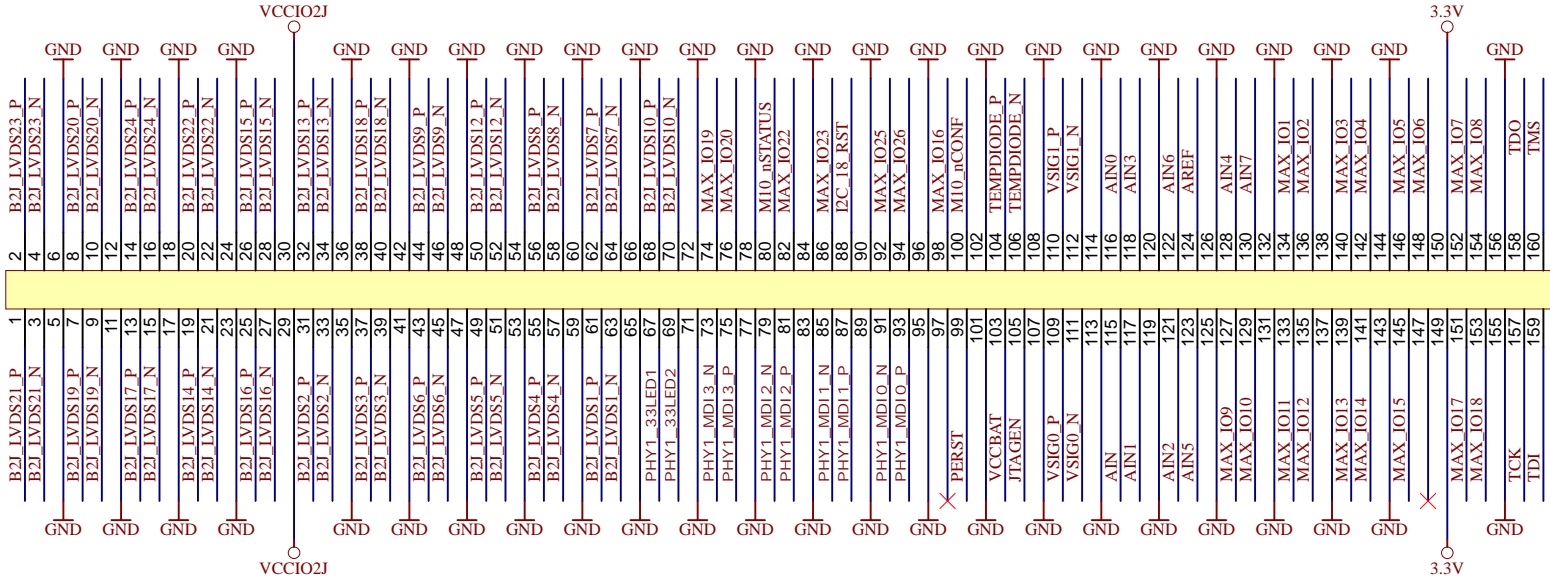
B

C

C

D

D



J2 ST5-80-1.50-L-D-P-TR



Title: TEI0006		
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1

2

3

4

1

2

3

4

A

A

B

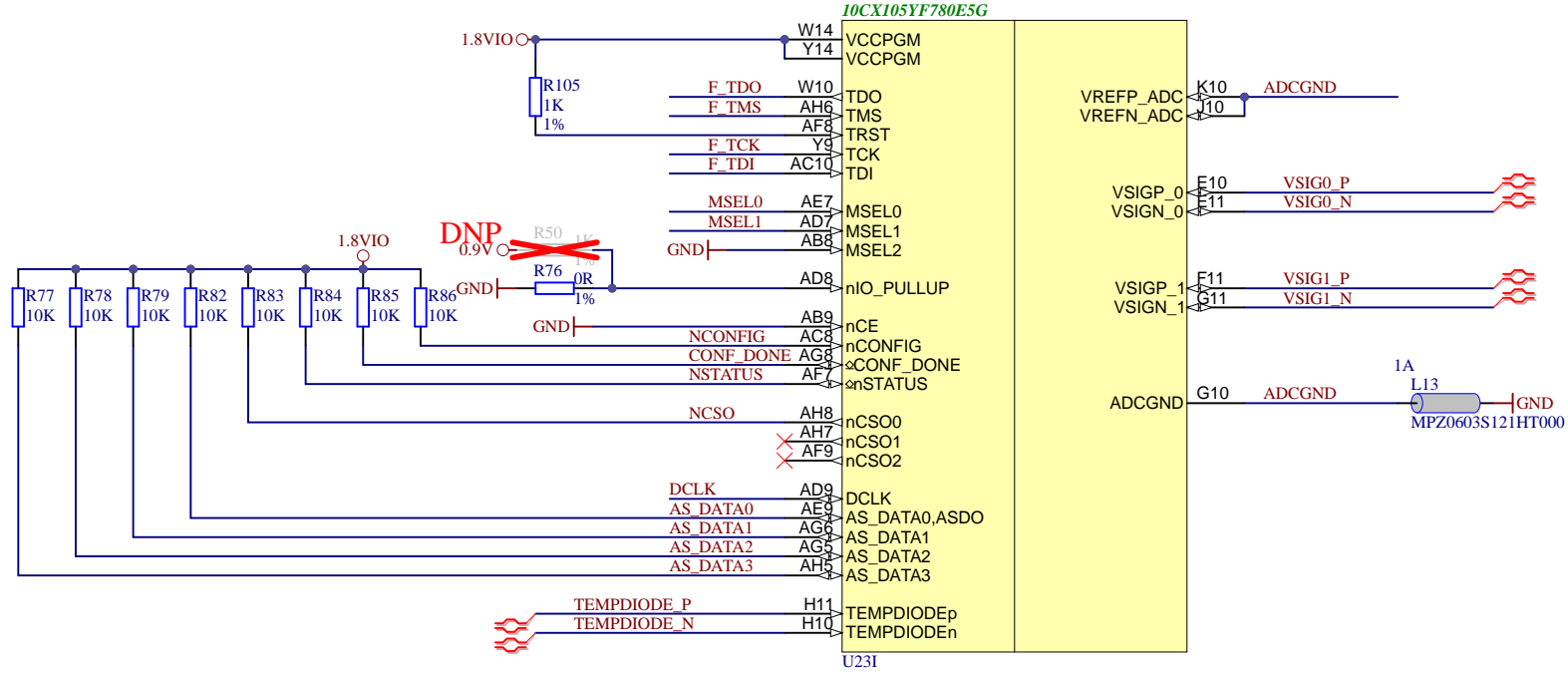
B

C

C

D

D

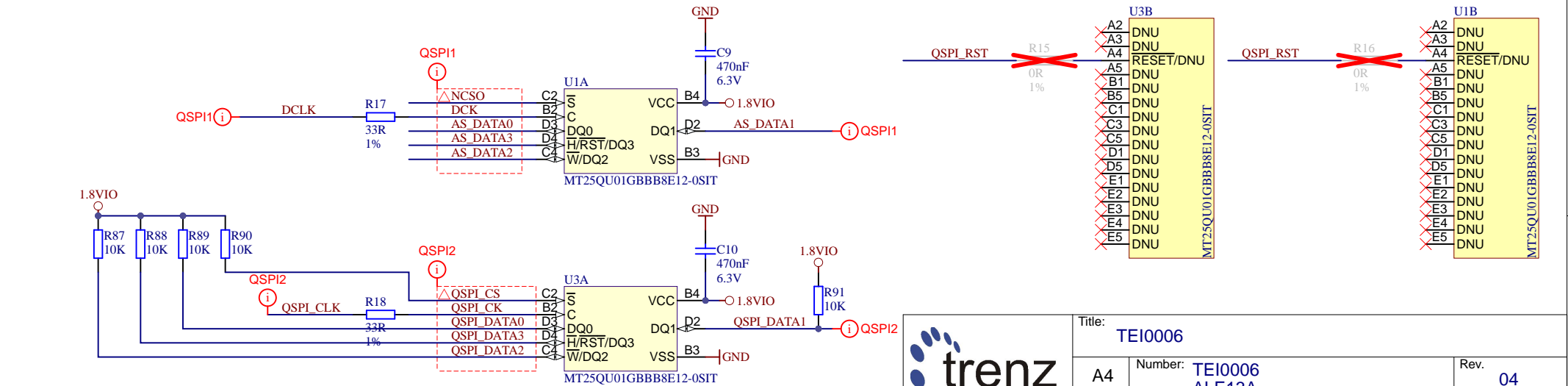


1

2

3

4



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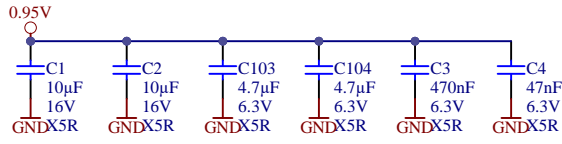
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2

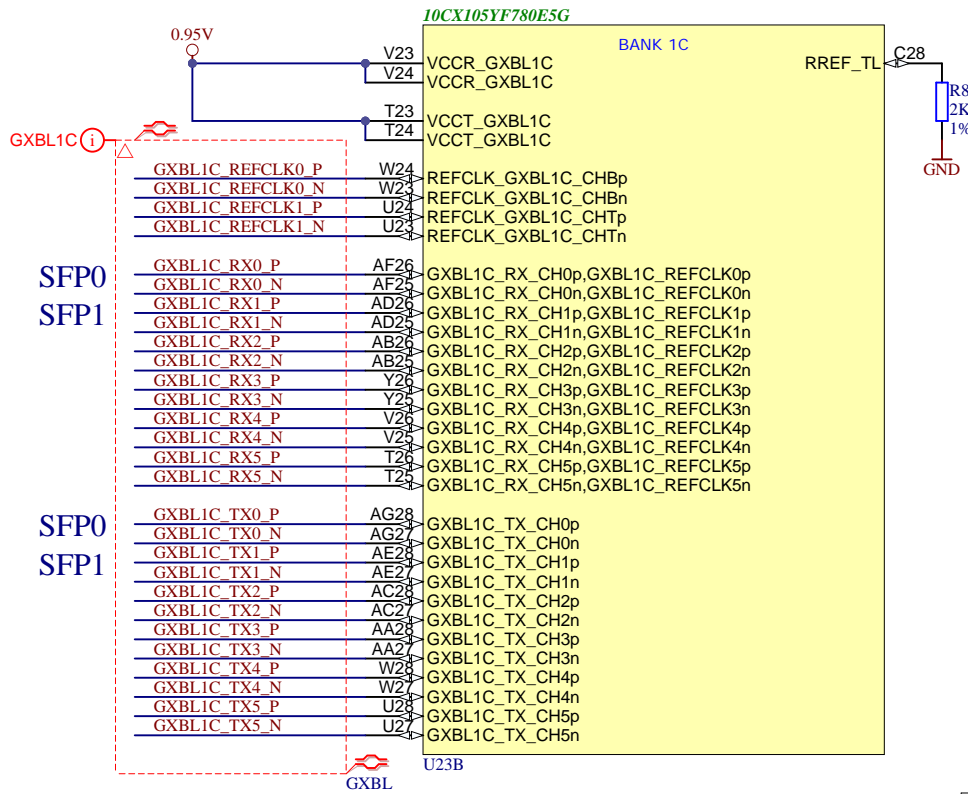
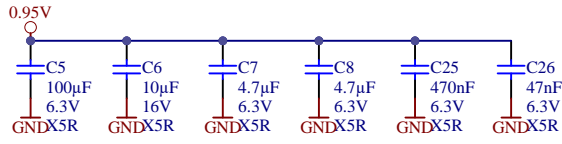

3

4

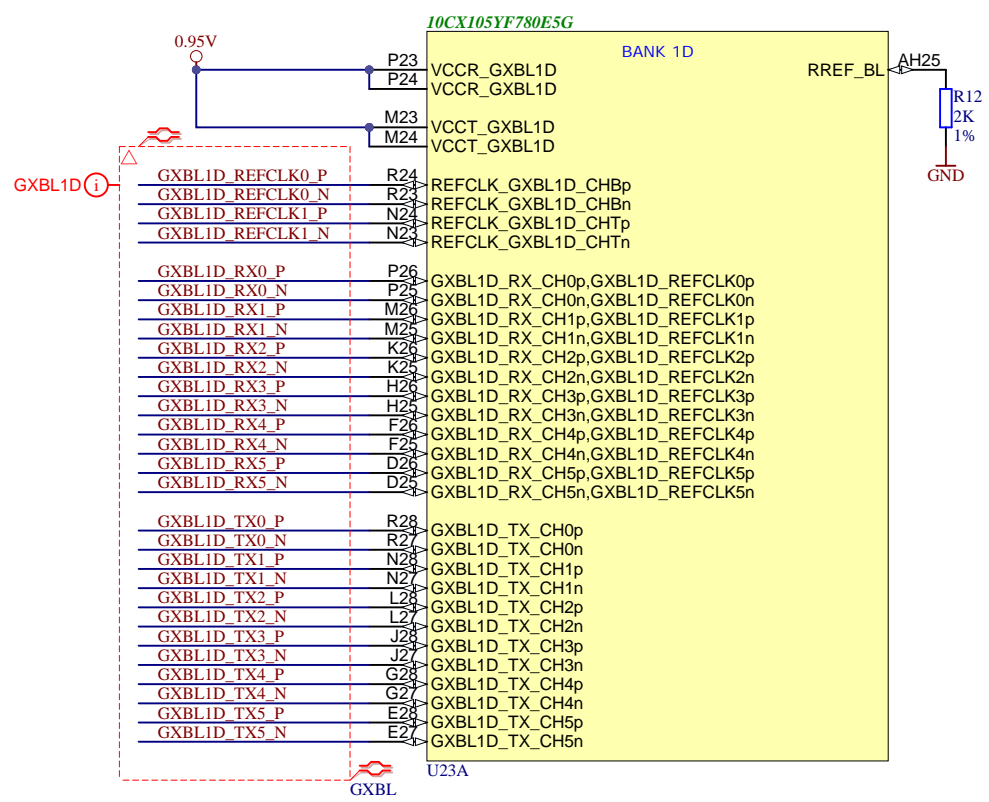
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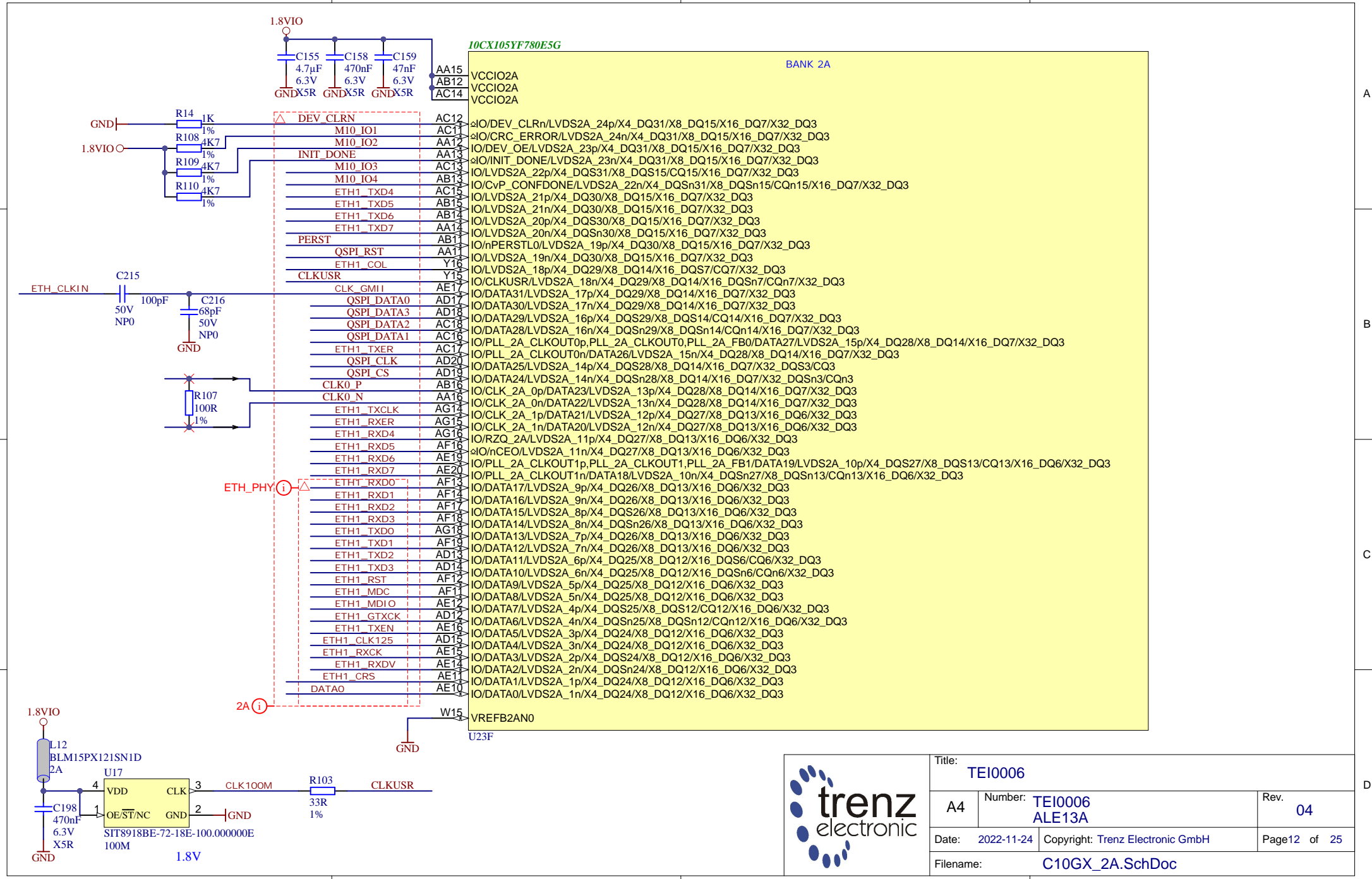
Placed at VCCR_GXB pins

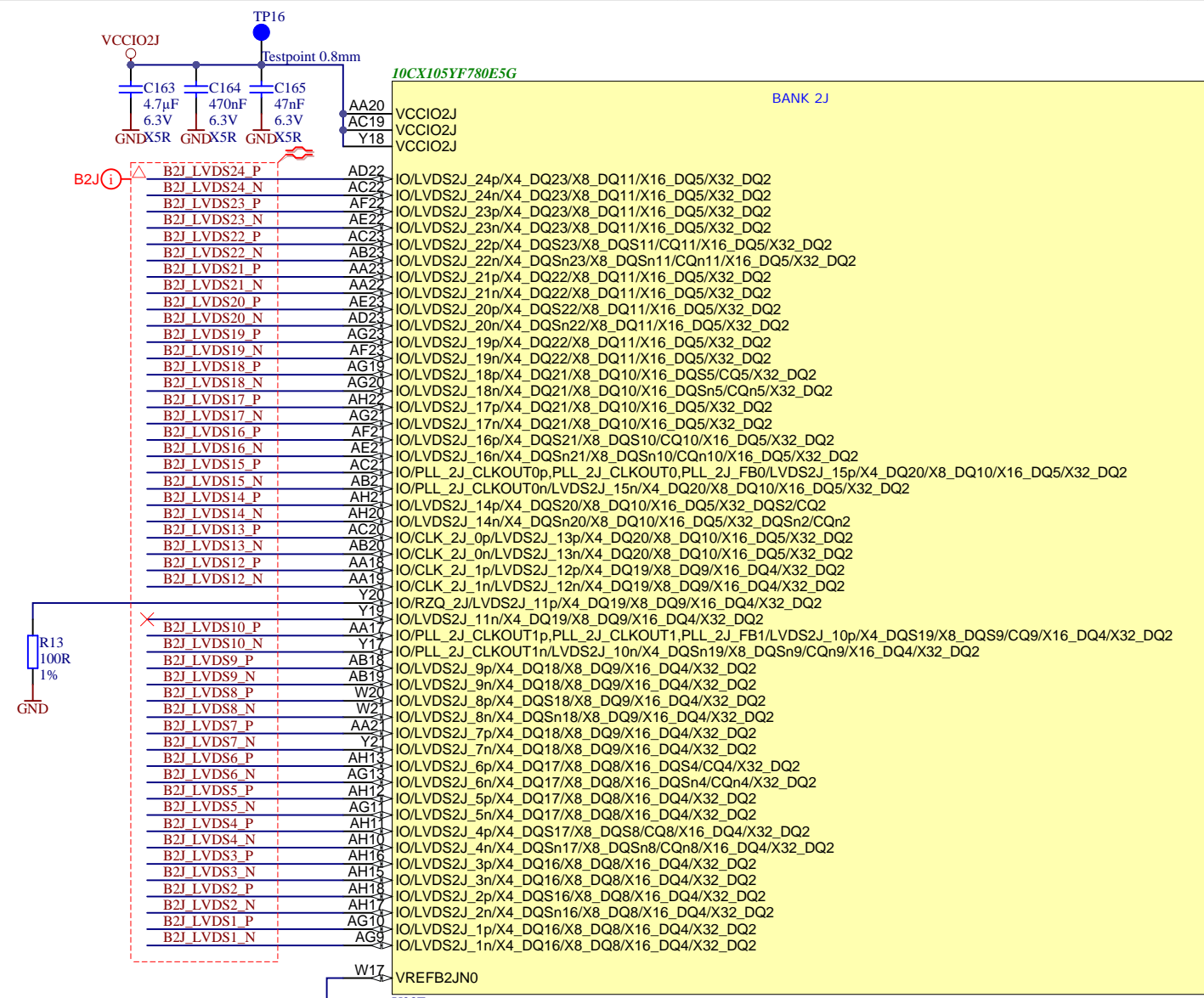
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Filename: C10GX_1C.SchDoc		



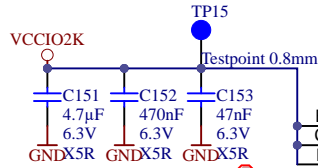
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Copyright: Trenz Electronic GmbH		Page 11 of 25
Filename: C10GX_1D.SchDoc		



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A4	Number: TEI0006 ALE13A	Rev. 04
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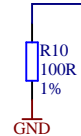
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Filename: C10GX_2J.SchDoc		



10CX105YF780ESG

BANK 2K

B2K i



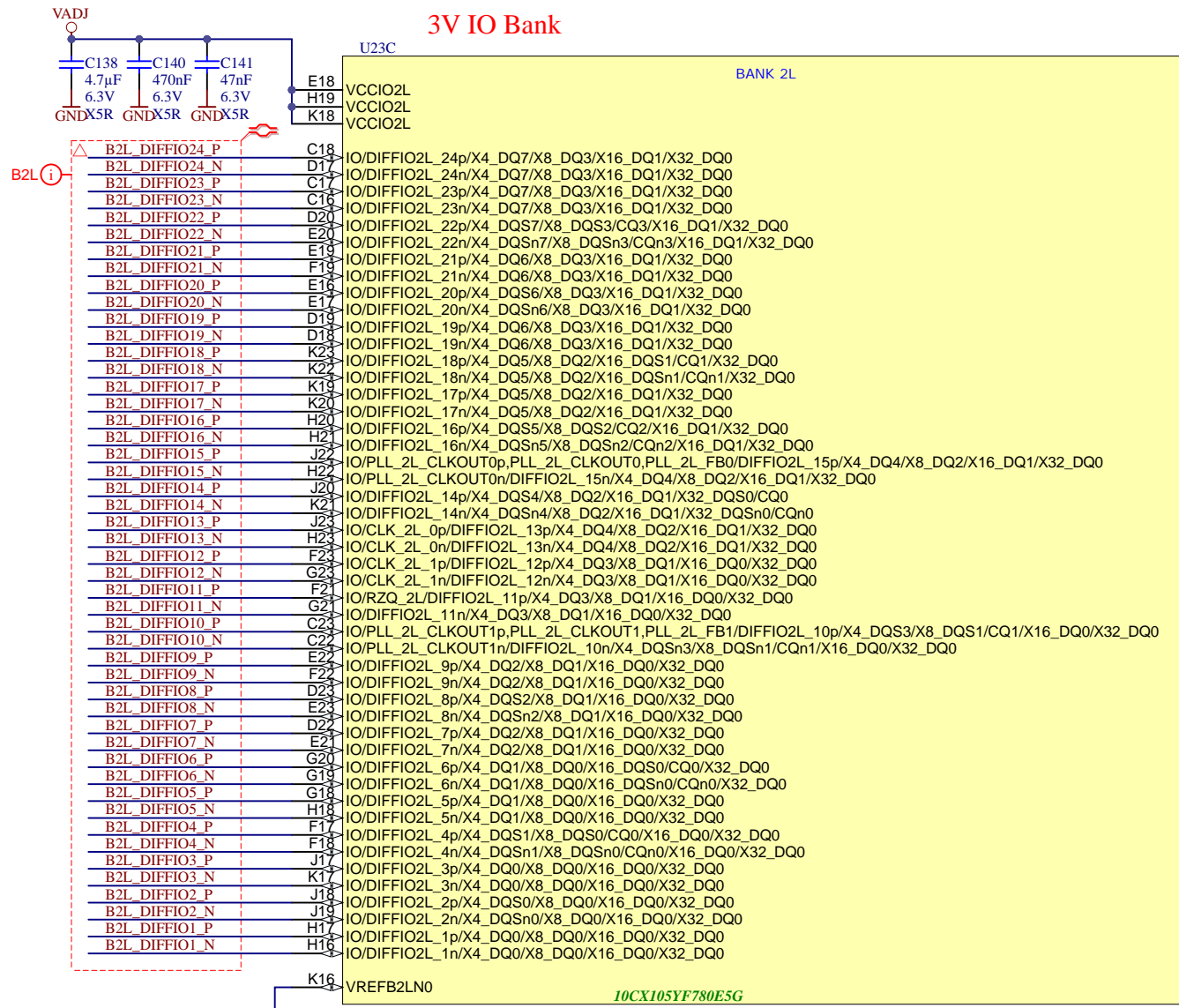
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B2K LVDS24 N	B1
B2K LVDS23 P	A12
B2K LVDS23 N	A1
B2K LVDS22 P	A13
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B2K LVDS21 P	B12
B2K LVDS21 N	B15
B2K LVDS20 P	C1
B2K LVDS20 N	D1
B2K LVDS19 P	D12
B2K LVDS19 N	E12
B2K LVDS18 P	B26
B2K LVDS18 N	B25
B2K LVDS17 P	A2
B2K LVDS17 N	A22
B2K LVDS16 P	A27
B2K LVDS16 N	A26
B2K LVDS15 P	B2
B2K LVDS15 N	B25
B2K LVDS14 P	B21
B2K LVDS14 N	C2
B2K LVDS13 P	A24
B2K LVDS13 N	A23
B2K LVDS12 P	D15
B2K LVDS12 N	E15
B2K LVDS10 P	B20
B2K LVDS10 N	C20
B2K LVDS9 P	B13
B2K LVDS9 N	B16
B2K LVDS7 P	C15
B2K LVDS7 N	A19
B2K LVDS8 P	A17
B2K LVDS8 N	A16
B2K LVDS6 P	D9
B2K LVDS6 N	D10
B2K LVDS5 P	C5
B2K LVDS5 N	D5
B2K LVDS4 P	A9
B2K LVDS4 N	A8
B2K LVDS3 P	C12
B2K LVDS3 N	C1
B2K LVDS2 P	B10
B2K LVDS2 N	C10
B2K LVDS1 P	B9
B2K LVDS1 N	B8

VCCIO2K	B12	IO/LVDS2K_24p/X4_DQ15/X8_DQ7/X16_DQ3/X32_DQ1
VCCIO2K	C14	IO/LVDS2K_24n/X4_DQ15/X8_DQ7/X16_DQ3/X32_DQ1
VCCIO2K	F15	IO/LVDS2K_23p/X4_DQ15/X8_DQ7/X16_DQ3/X32_DQ1
		IO/LVDS2K_23n/X4_DQ15/X8_DQ7/X16_DQ3/X32_DQ1
		IO/LVDS2K_22p/X4_DQS15/X8_DQS7/CQ7/X16_DQ3/X32_DQ1
		IO/LVDS2K_22n/X4_DQSn15/X8_DQSn7/CQn7/X16_DQ3/X32_DQ1
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		IO/LVDS2K_17p/X4_DQ13/X8_DQ6/X16_DQ3/X32_DQ1
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		IO/LVDS2K_16n/X4_DQSn13/X8_DQSn6/CQn6/X16_DQ3/X32_DQ1
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		IO/PLL_2K_CLKOUT0n/LVDS2K_15n/X4_DQ12/X8_DQ6/X16_DQ3/X32_DQ1
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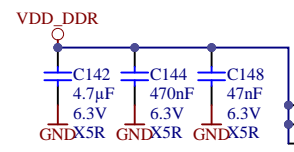
VREFB2KN0
U23D



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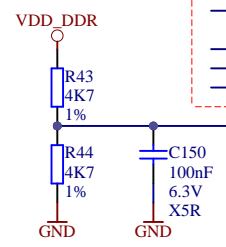
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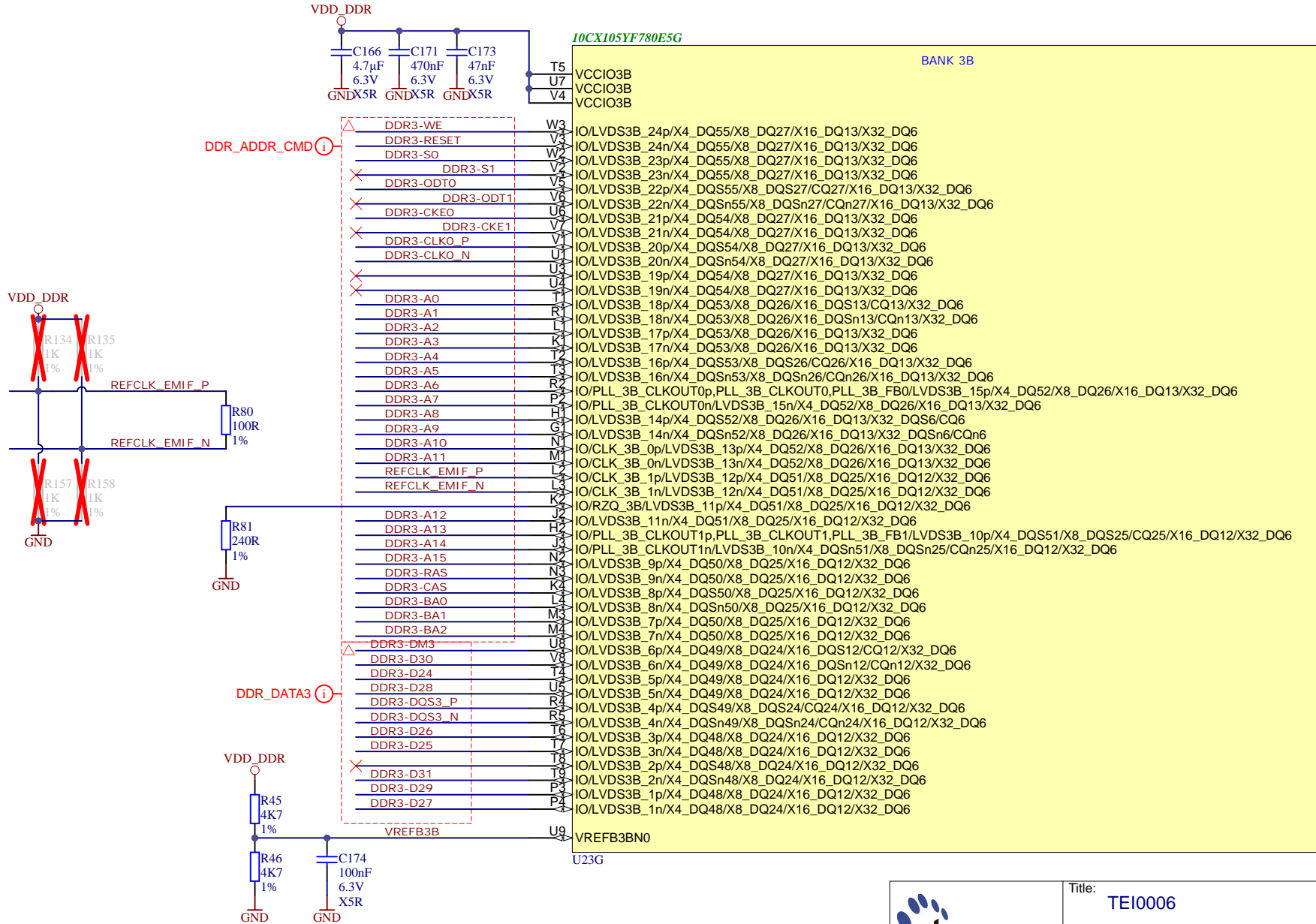
DDR_DATA1 (i)

DDR_DATA0 (i)

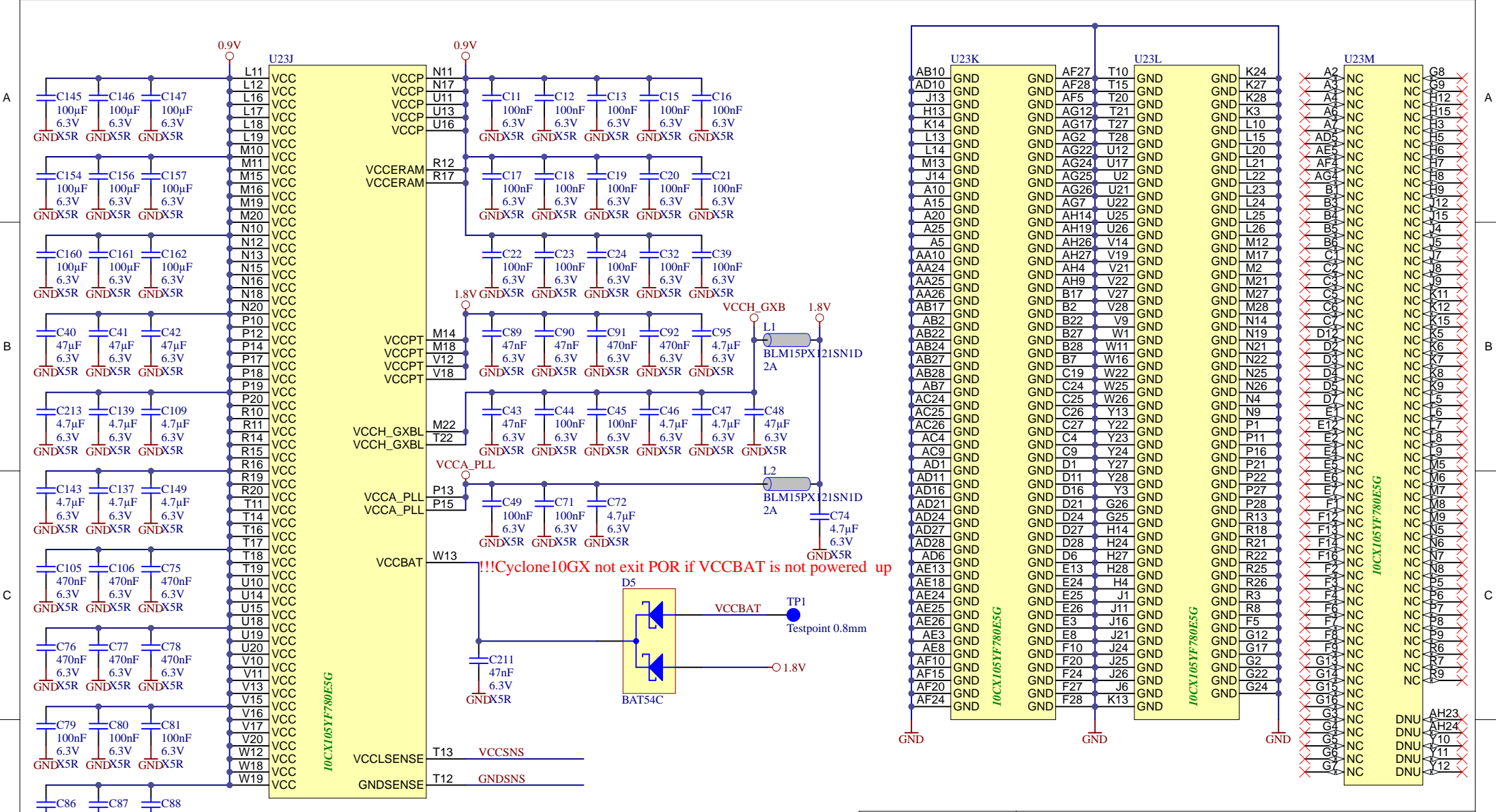
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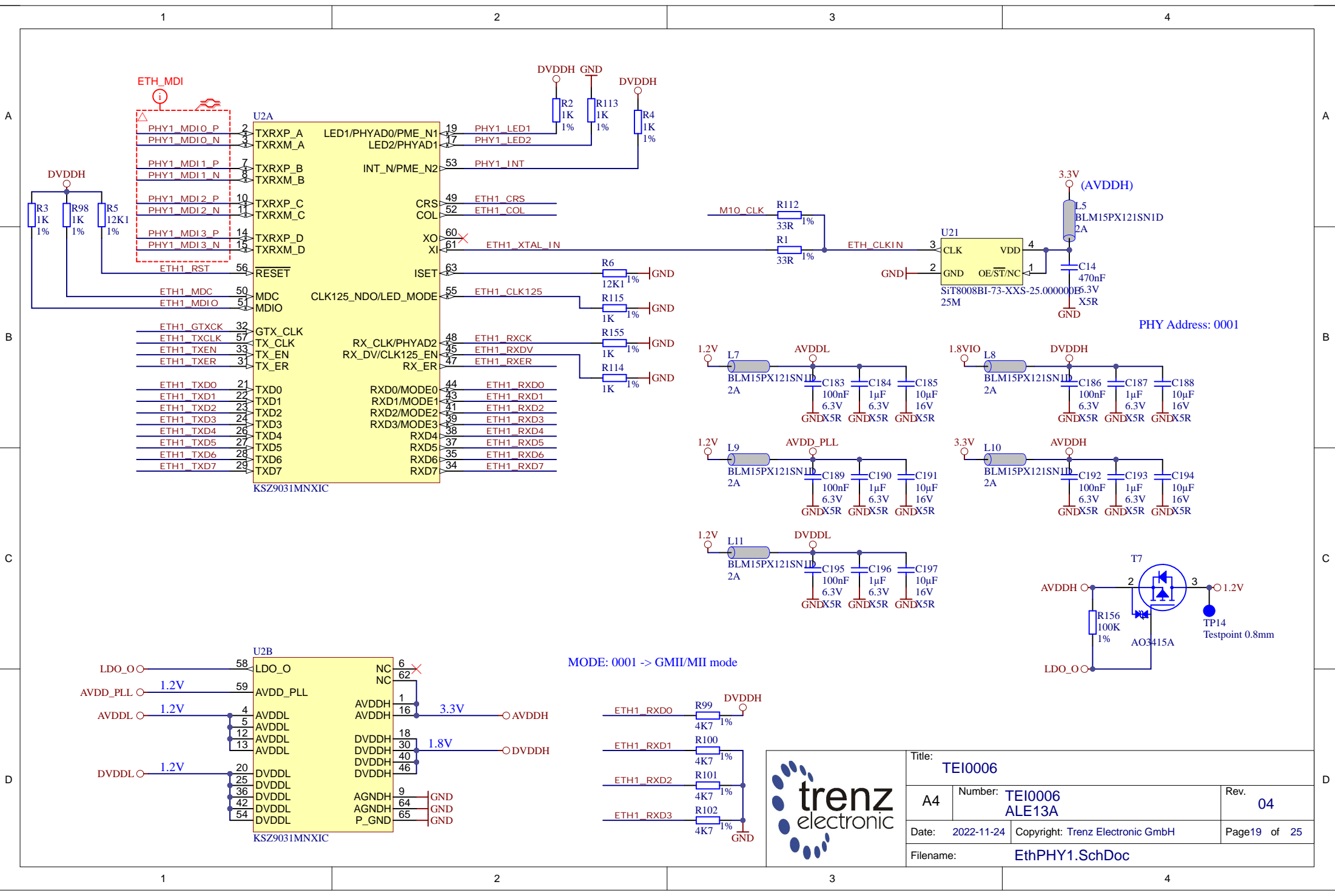
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MODE: 0001 -> GMII/MII mode

PHY Address: 0001



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A

B

C

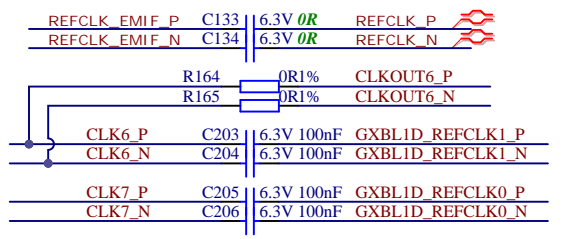
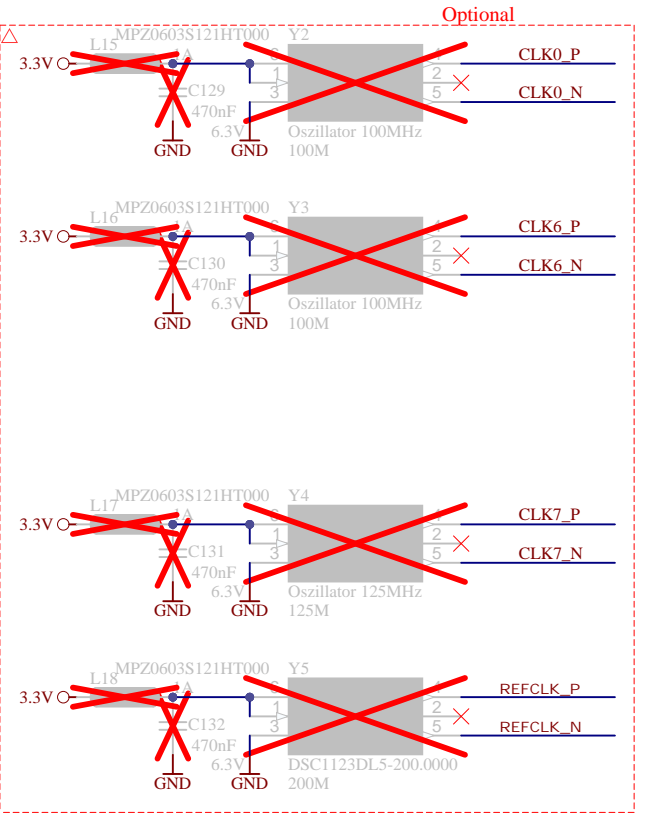
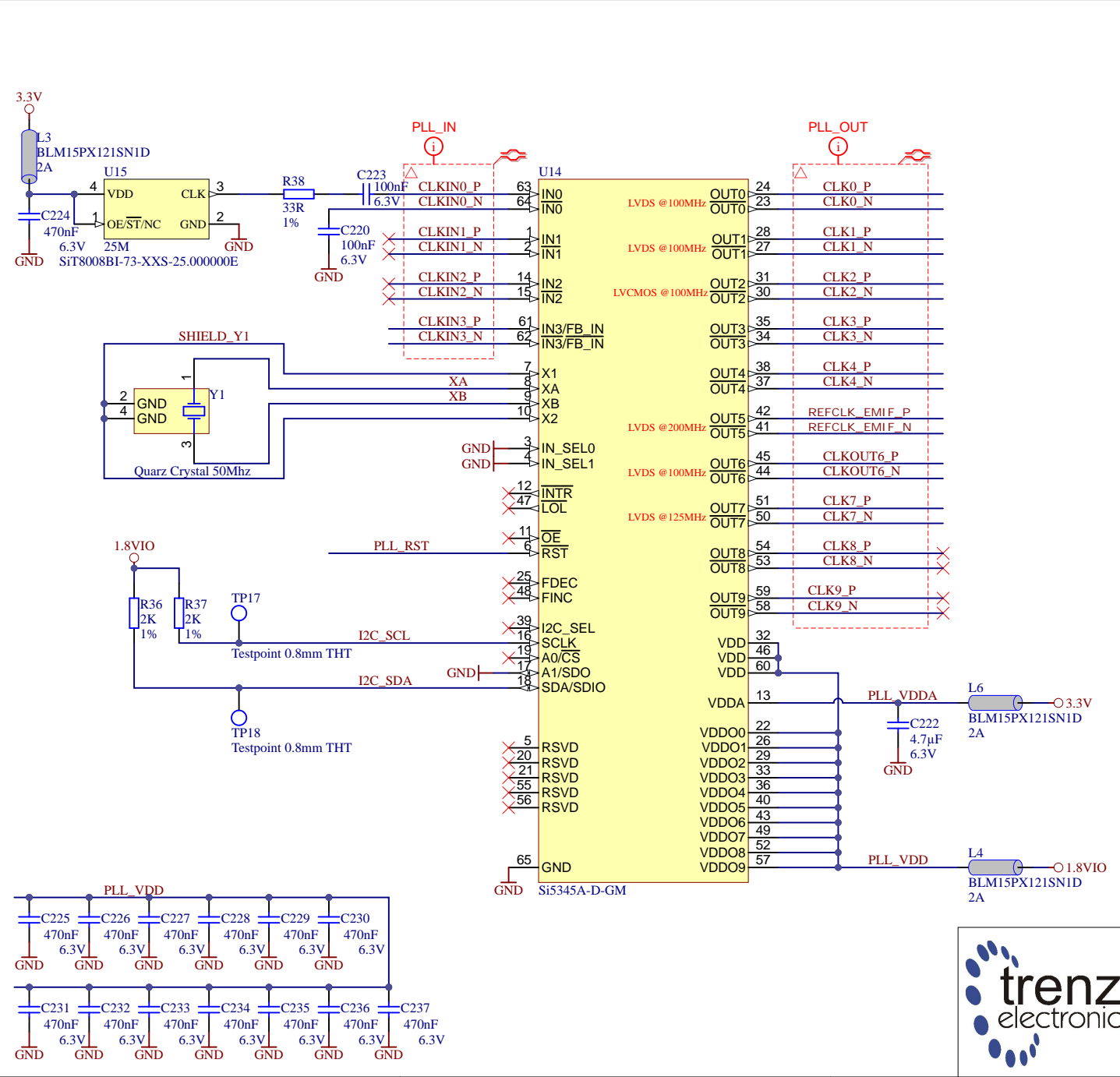
D

A

B

C

D



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A

A

B

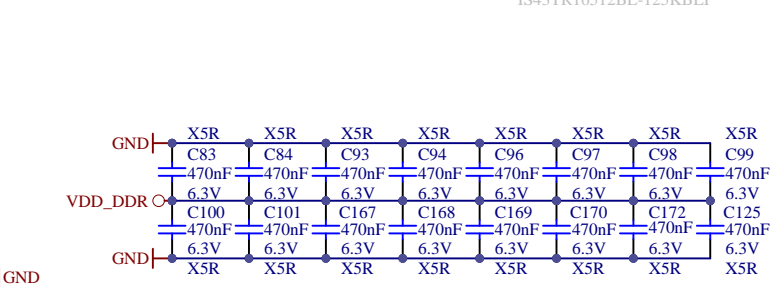
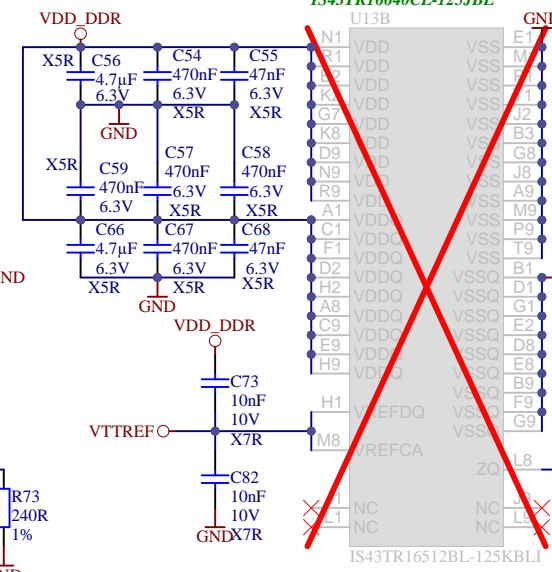
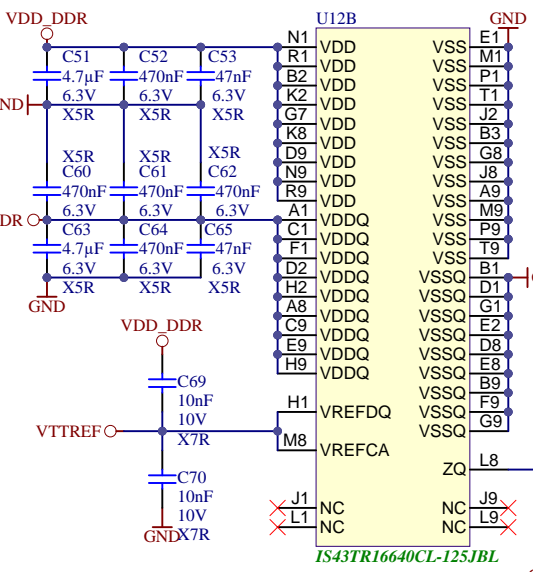
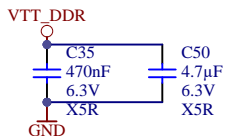
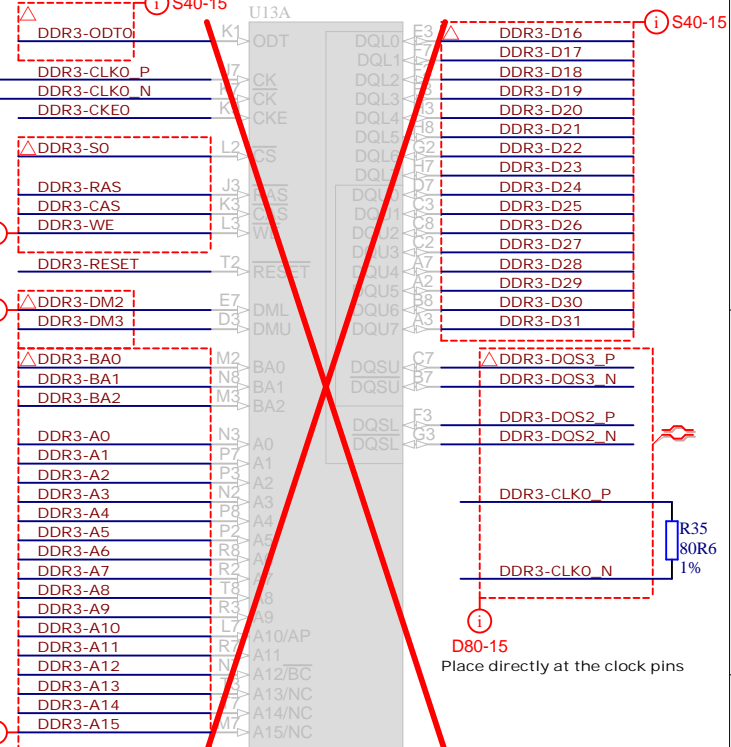
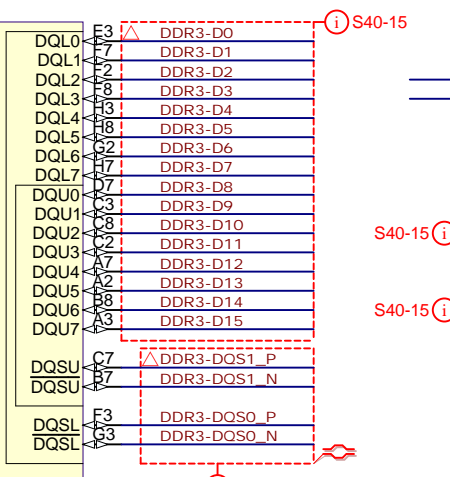
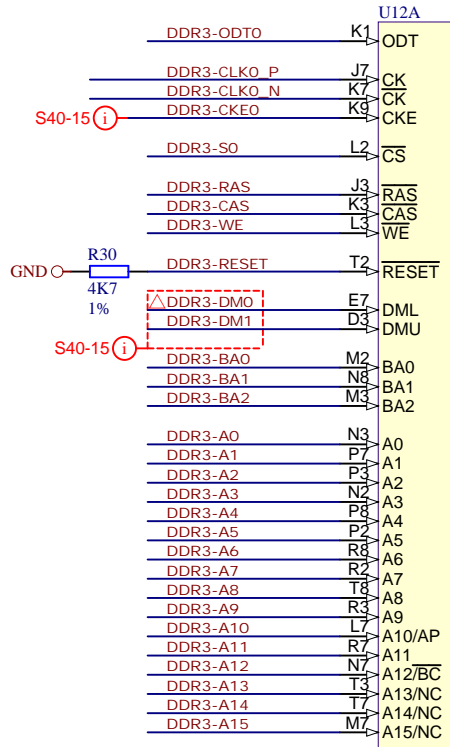
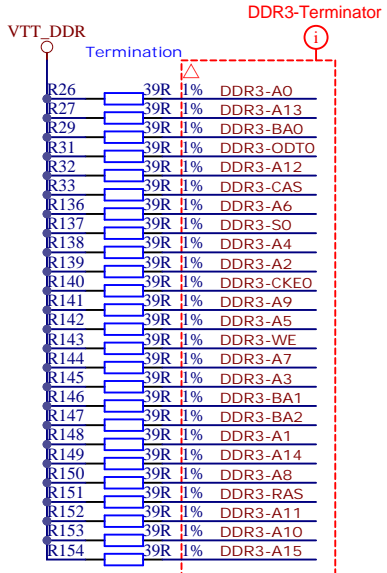
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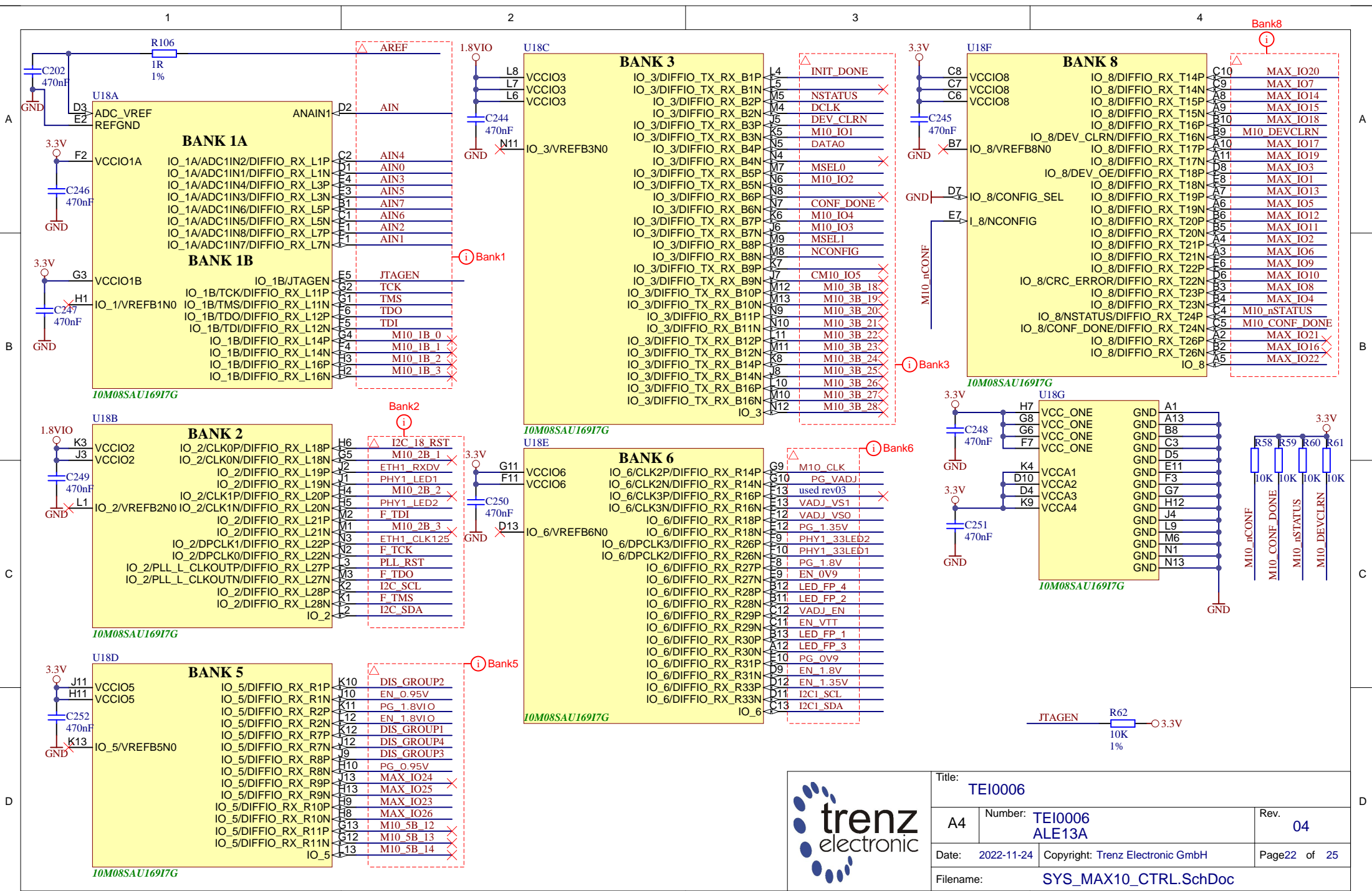
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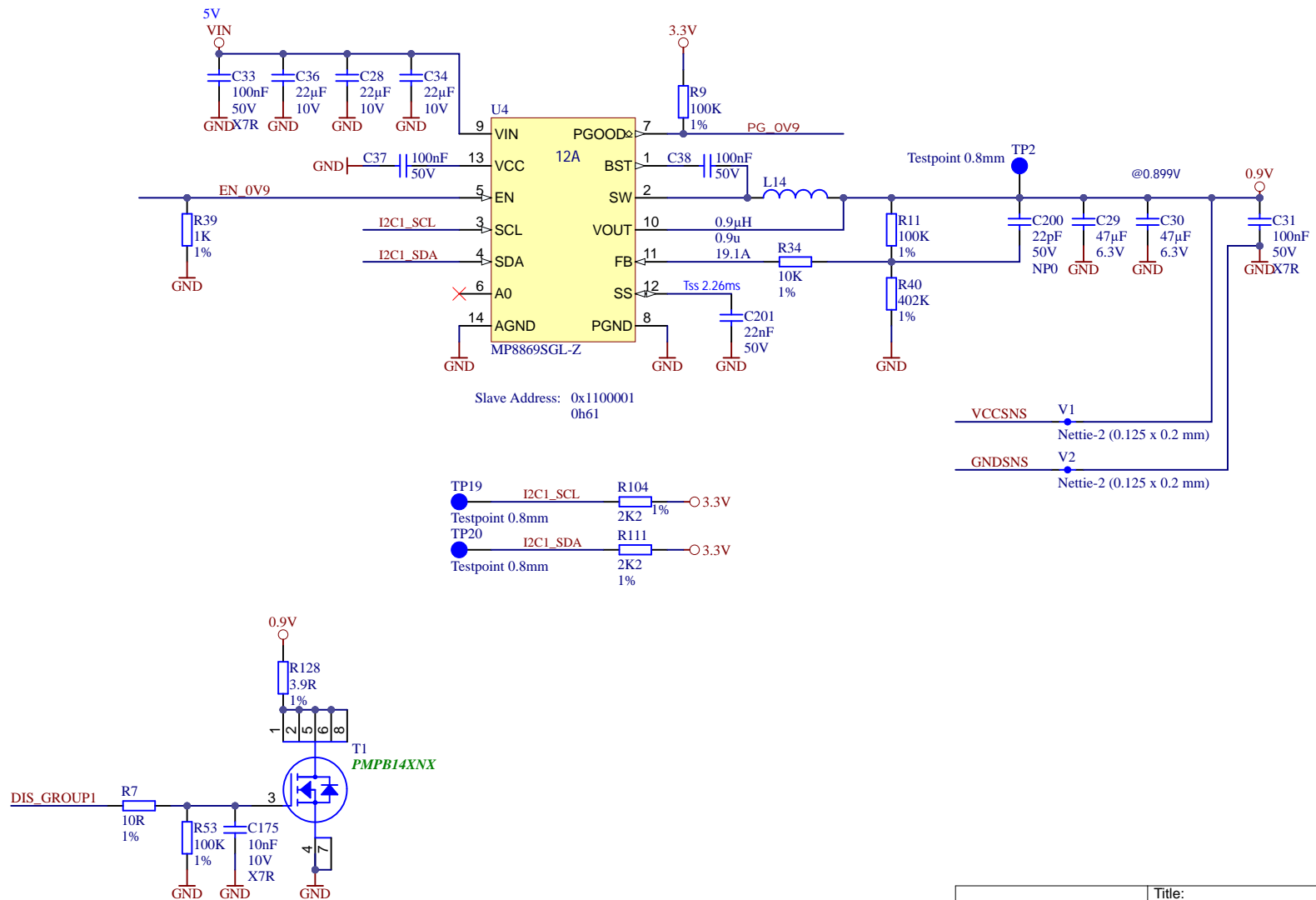
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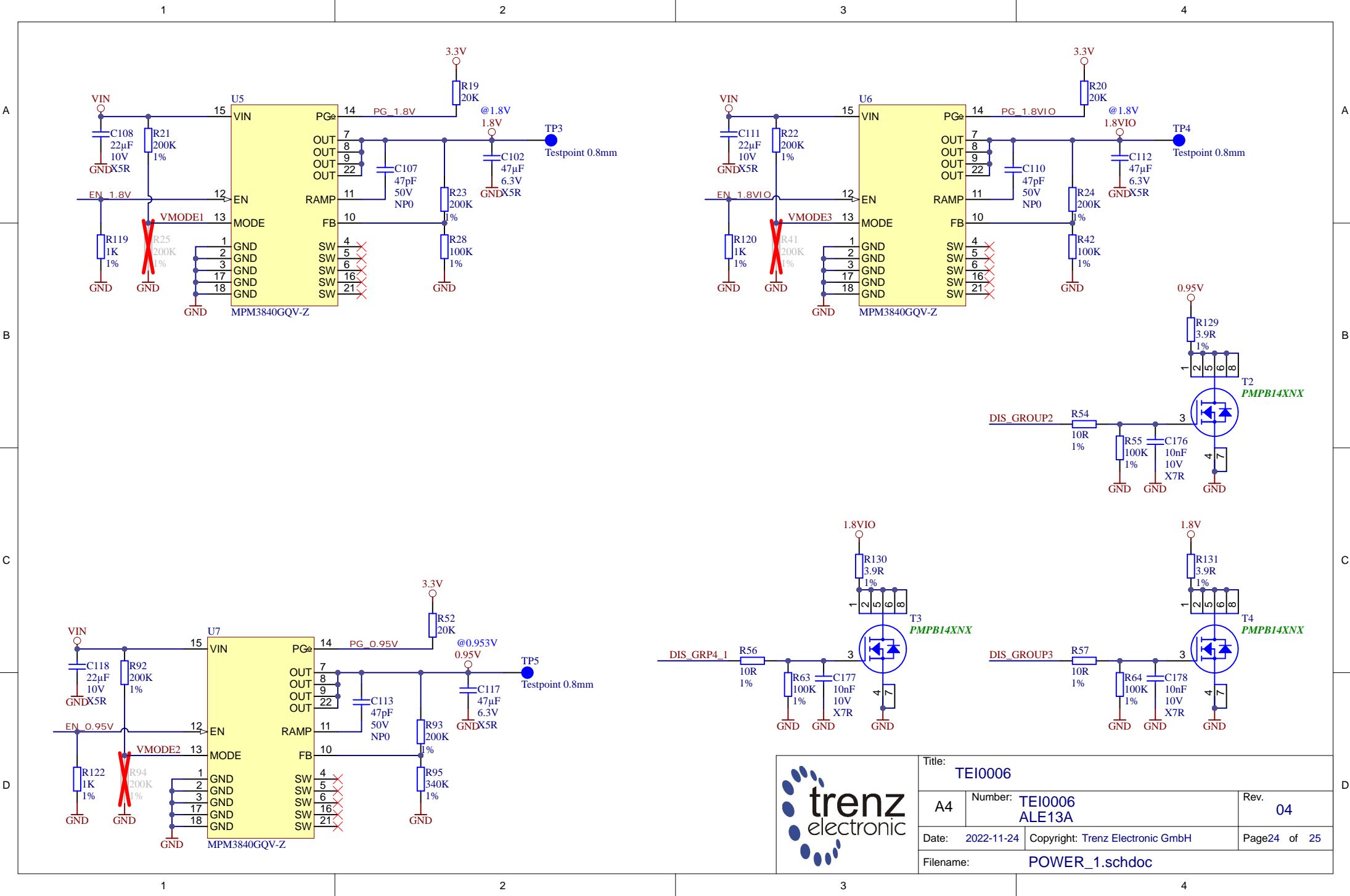
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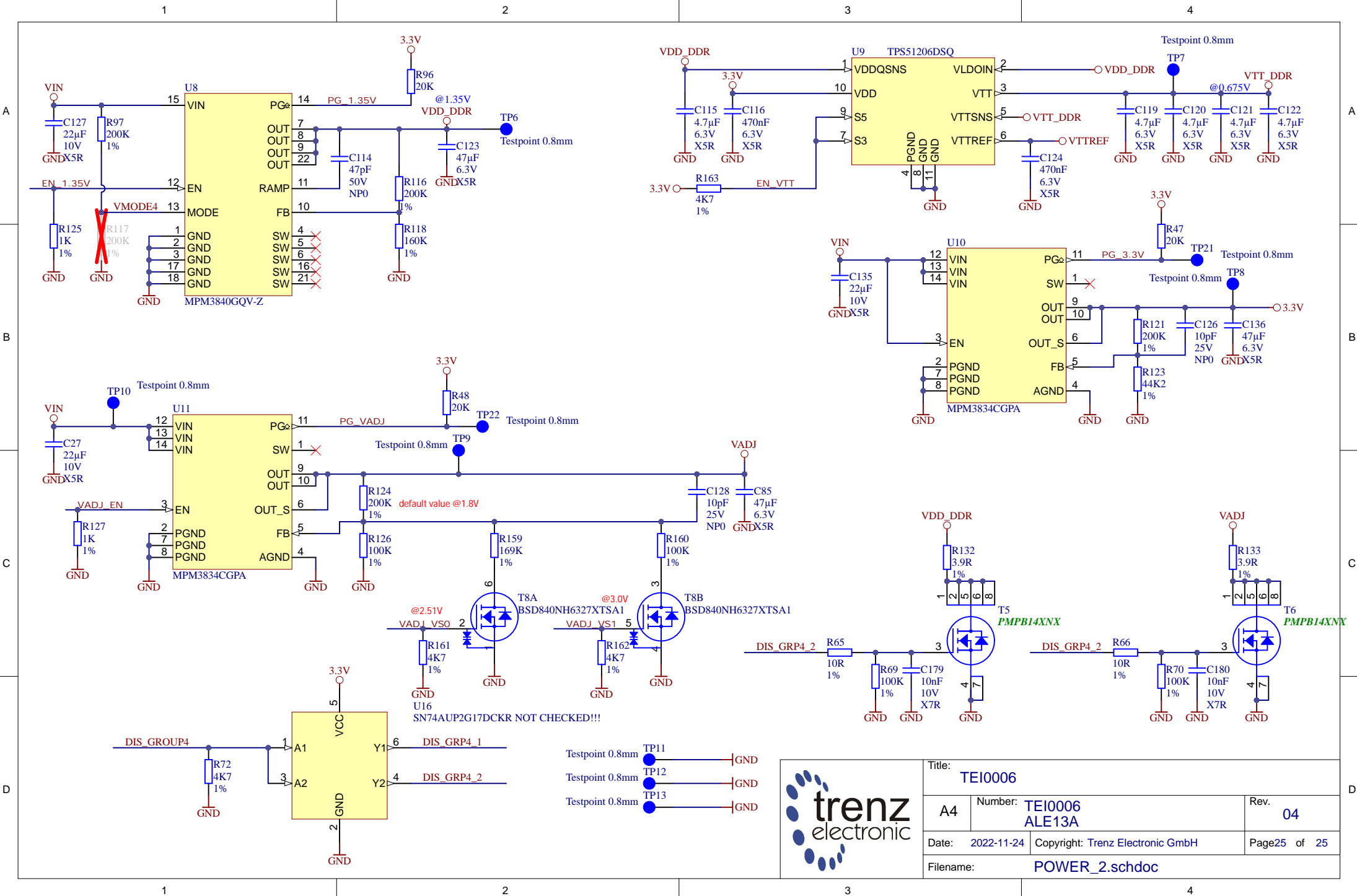
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