
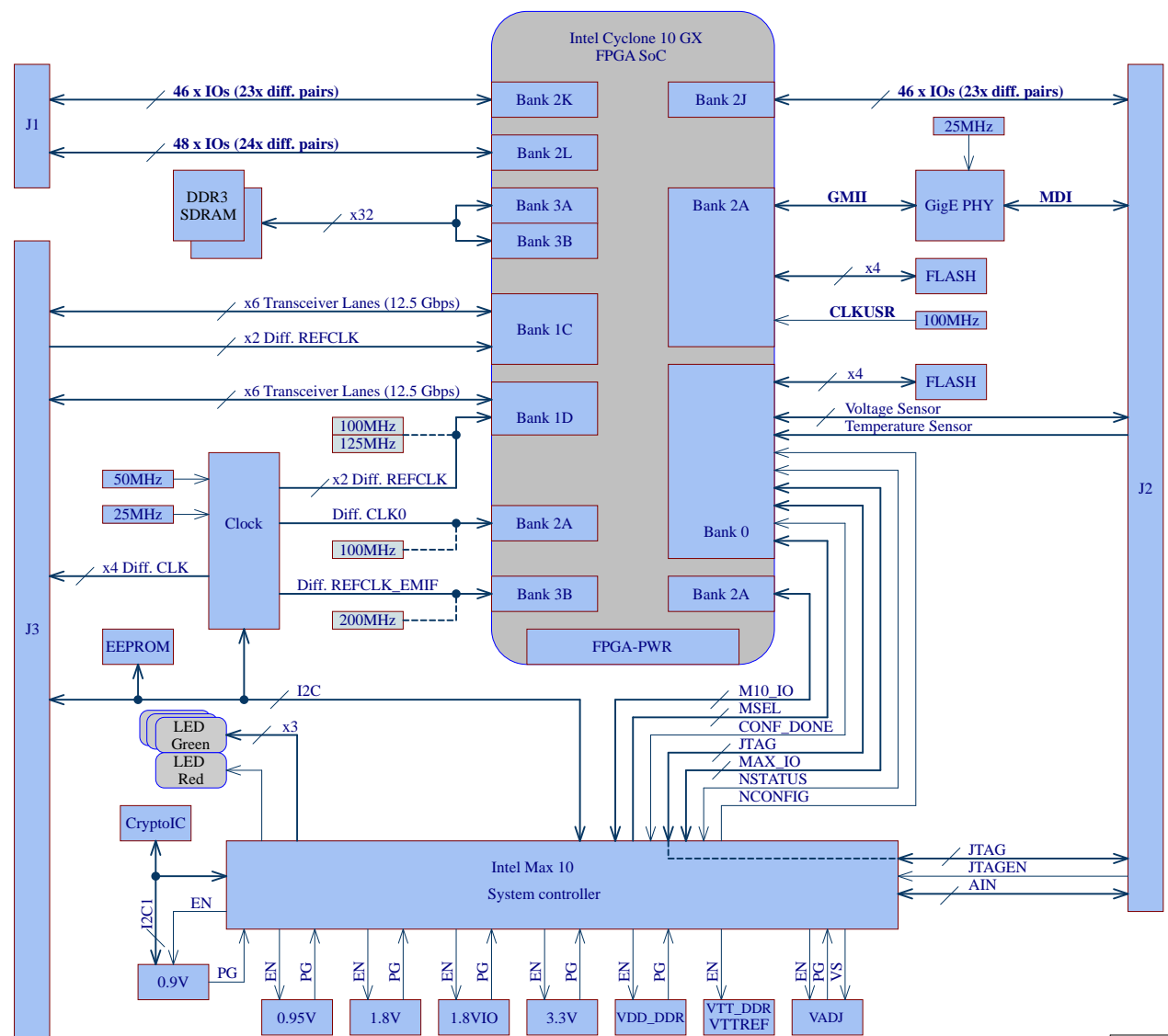


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Schematics and other handouts serve for informational purposes only!

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- U_Revision Changes
- U_TEI0006
- U_Power_Diagram

Special notes:

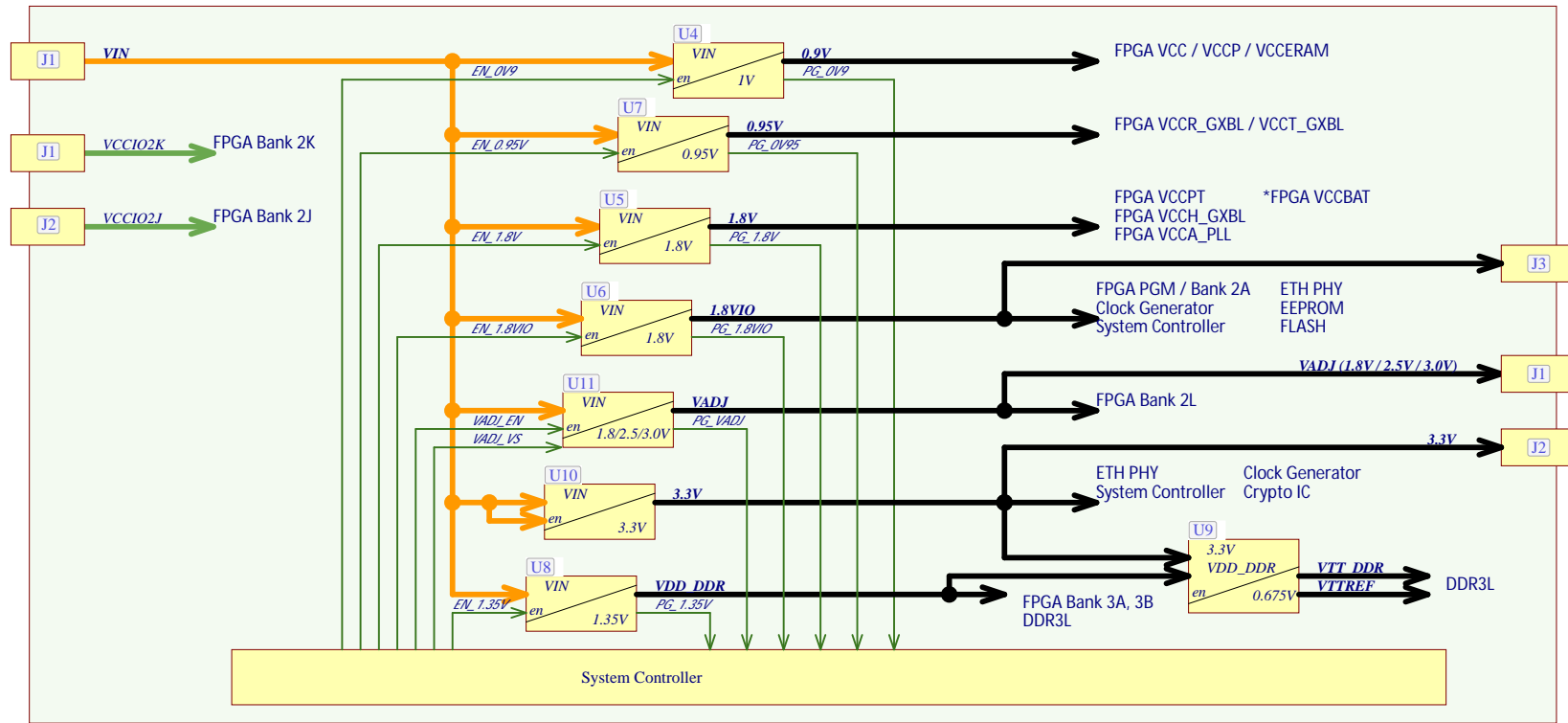


Title: TEI0006 - System Overview		
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REV	Description	
-01	Initial revision	VT
-02	1) VT: added MEMS 100MHz clock oscillator to CLKUSR 2) VT: remove CLKUSR from J2 3) VT: replaced Si510 to SiT8008/CM3225-4pad 4) VT: remove DEVCLRN from J2, added pull-up 5) VT: remove M10_nSTATUS from J2, added pull-up 6) VT: Added optional CryptoAuthentication chip U19 (DNP)	VT
-03	1) VT: fixed CLK connections (CLK's from FMC (on Baseboard) directly connected to GXBLIC bank) 2) VT: added heatsink 3) VT: full upd LIB 4) VT: added Legal Notices sheet	VT
	5) VY: replaced not available transistors T1-T6 AON2240 to PMPB14XNX	VY
-04	1) VT: replaced EOL Power regulators: a) U4: EN63A0QI -> MP8869SGL-Z b) U5,U6,U7,U8: EN6340QI -> MPM3840GQV-Z c) U10, U11: EP53A8HQI -> MPM3834CGPA d) U9: EV1320QI -> TPS51206DSQ 2) VT: replaced not available buffer U16: NC7WZ16P6X ->SN74AUP2G17DCKR 3) VT: added dual transistor T8 for select VADJ Voltage (1.8V, 2.5V, 3.0V) 4) VT: remove signals VADJ_VS2 and PG_VTT from System Controller U18 5) VT: added DCDC I2C to System Controller U18 6) VT: added Testpoints to I2C1 I2C bus 7) VT: added optional MEMS LVDS Oscillators Y2,Y3,Y4,Y5 8) VT: remove Resistors R47,R48,R49,R51 9) VT: added optional Termination to REFCLK_EMIF 10) VT: U19-> use I2C 3.3V 11) VT: added diode D5 for VCCBAT 12) VT: added signal PG_VADJ to System Controller U18 13) VT: changed Commercial grade to Industrial for System Controller U18	VT

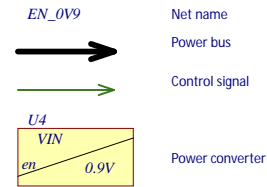
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Filename: Revision_Changes.SchDoc			

Power-on sequencing:

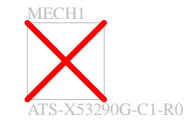
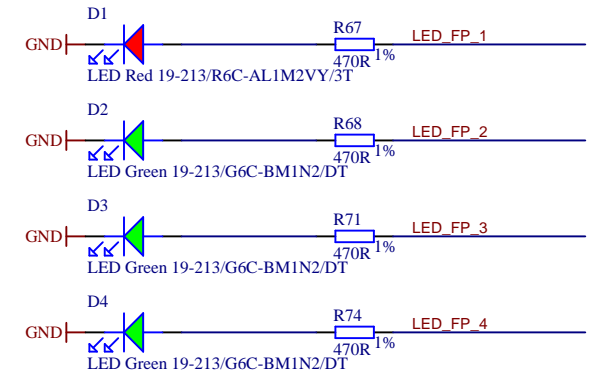
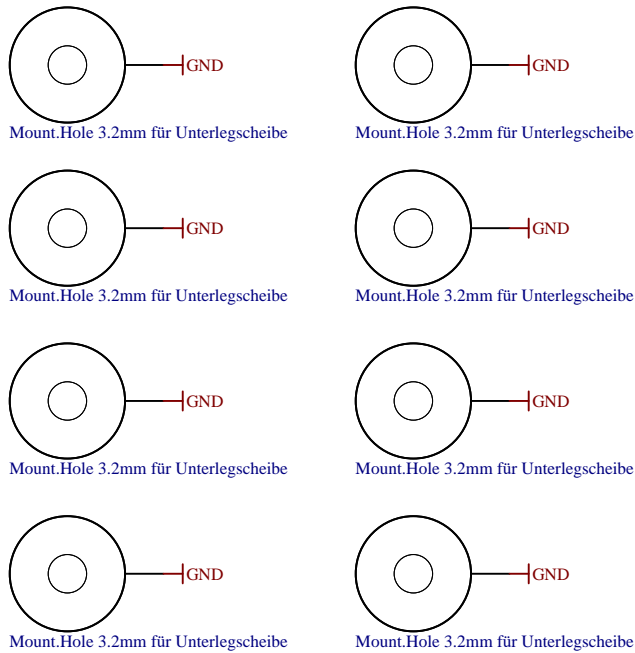


Recommended Operating Conditions

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	5V	+/-5%	Micromodule Power	Mandatory
VCCIO2K	IN	1.2 - 1.8V	+/-3%	IO Bank 2K	-
VCCIO2J	IN	1.2 - 1.8V	+/-3%	IO Bank 2J	-
1.8VIO	OUT	1.8V	+/-3%	For Carrier card Periphery	-
VADJ	OUT	1.8 - 3.0V	+/-3%	For Carrier card Periphery	Voltage set by System Controller
3.3V	OUT	3.3V	+/-3%	For Carrier card Periphery	-



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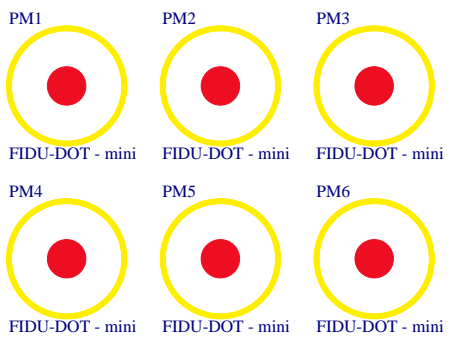
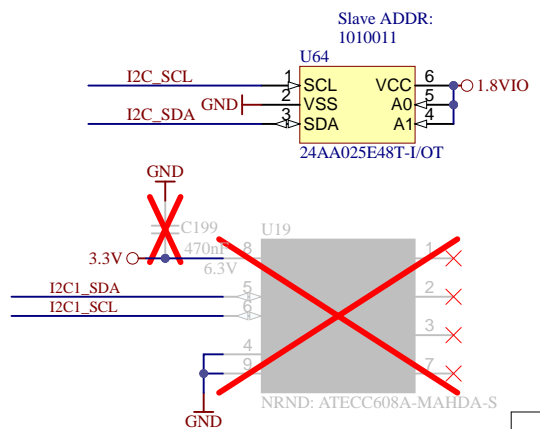
UKCA
UKCA Logo on Top Overlay
UKCA-TOOVERLAY

MECH2
TE Address Overlay
LOGO ADDRESS

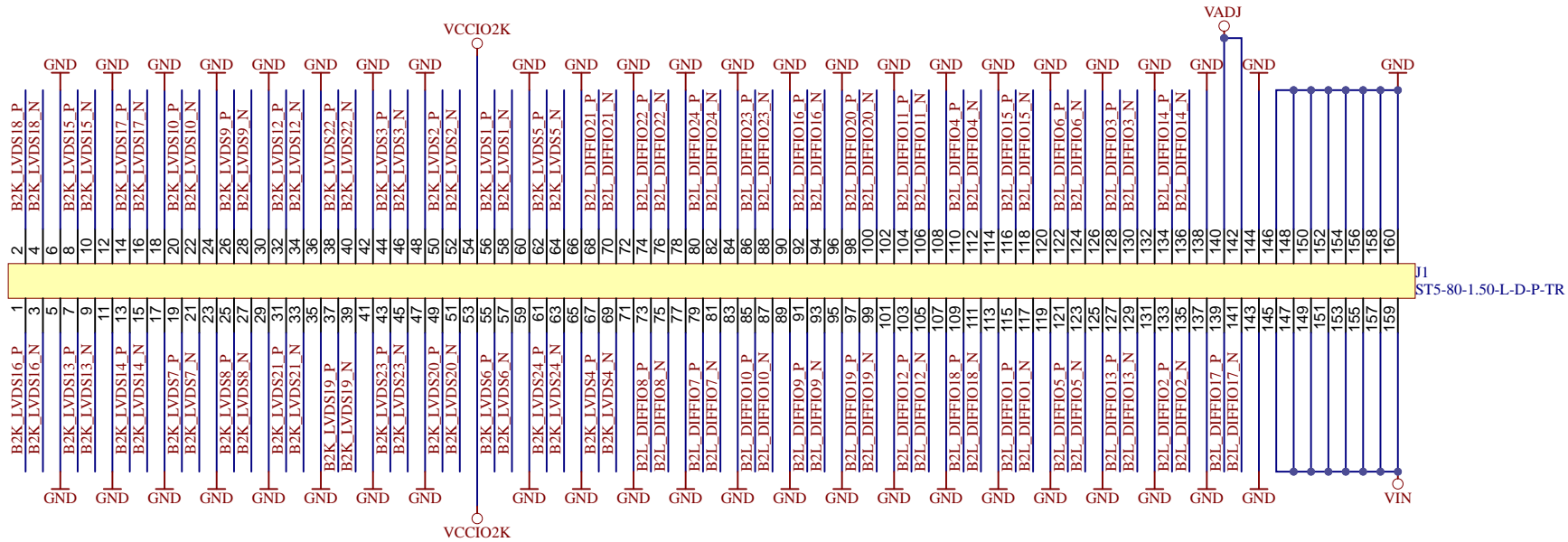
LOGO1
TE Logo PRINT Layer
LOGO PRINT

Assembly variant	APE23A
Created by	VT
Modified by	
Modified at	2023-05-03
SVN Revision	17814

Serial
Serialnumber 6,3 x 6.3mm



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1

2

3

4

A

A

B

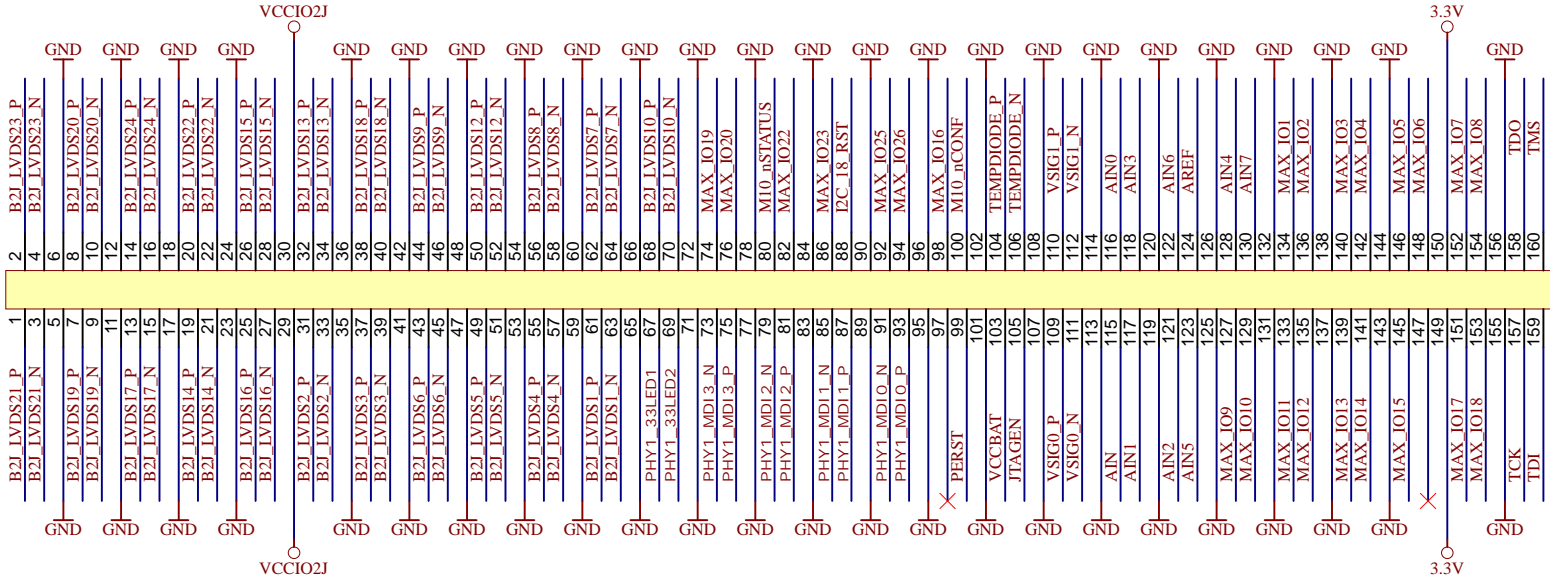
B

C

C

D

D



J2
ST5-80-1.50-L-D-P-TR



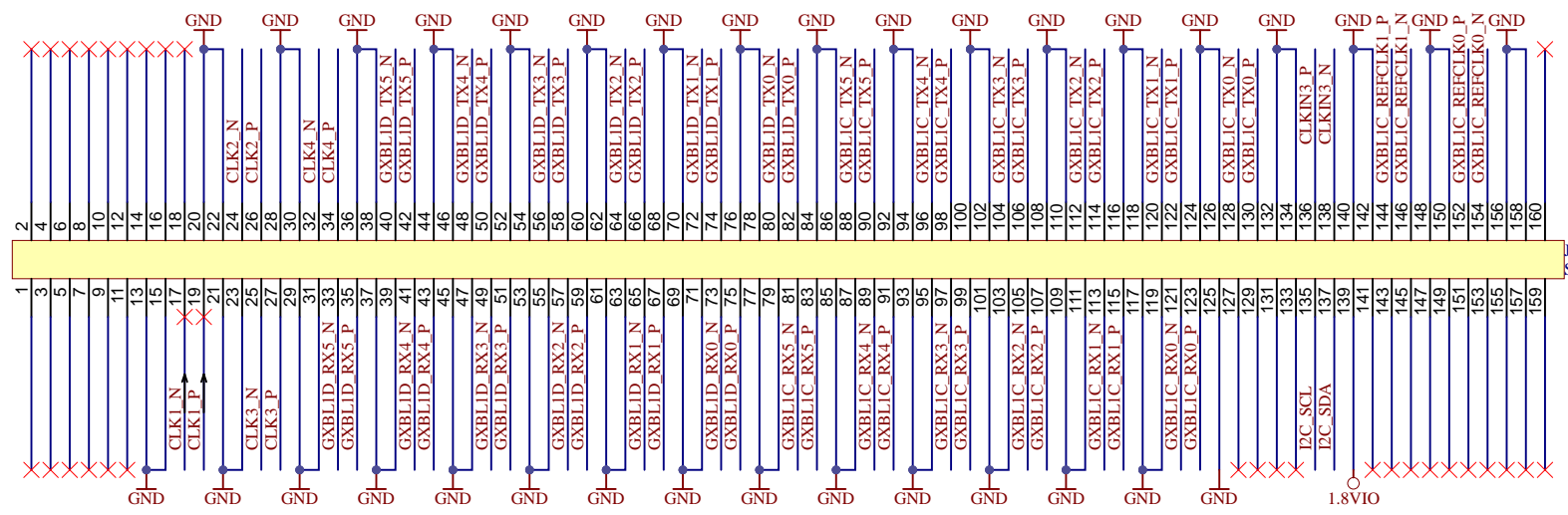
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Filename: J2.SchDoc		

1


2

3

4



J3
ST5-80-1.50-L-D-P-TR



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A

A

B

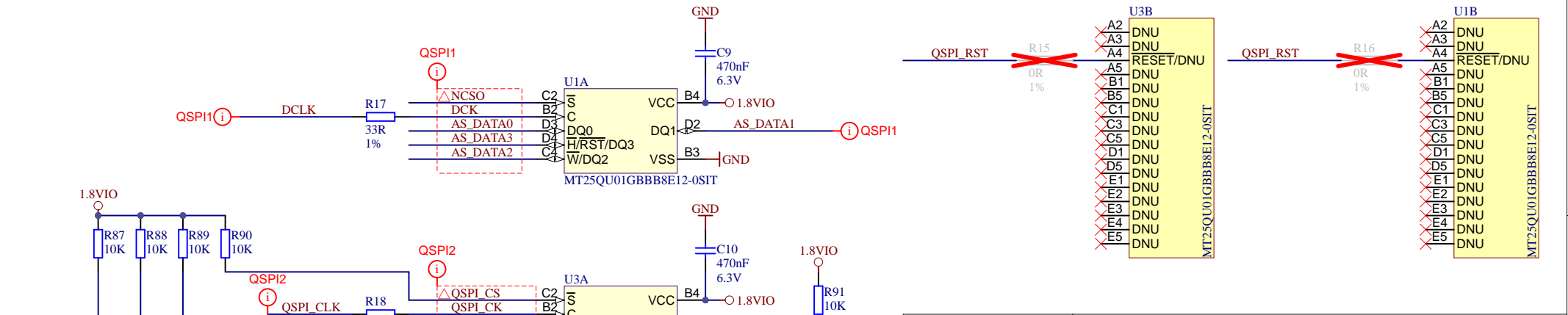
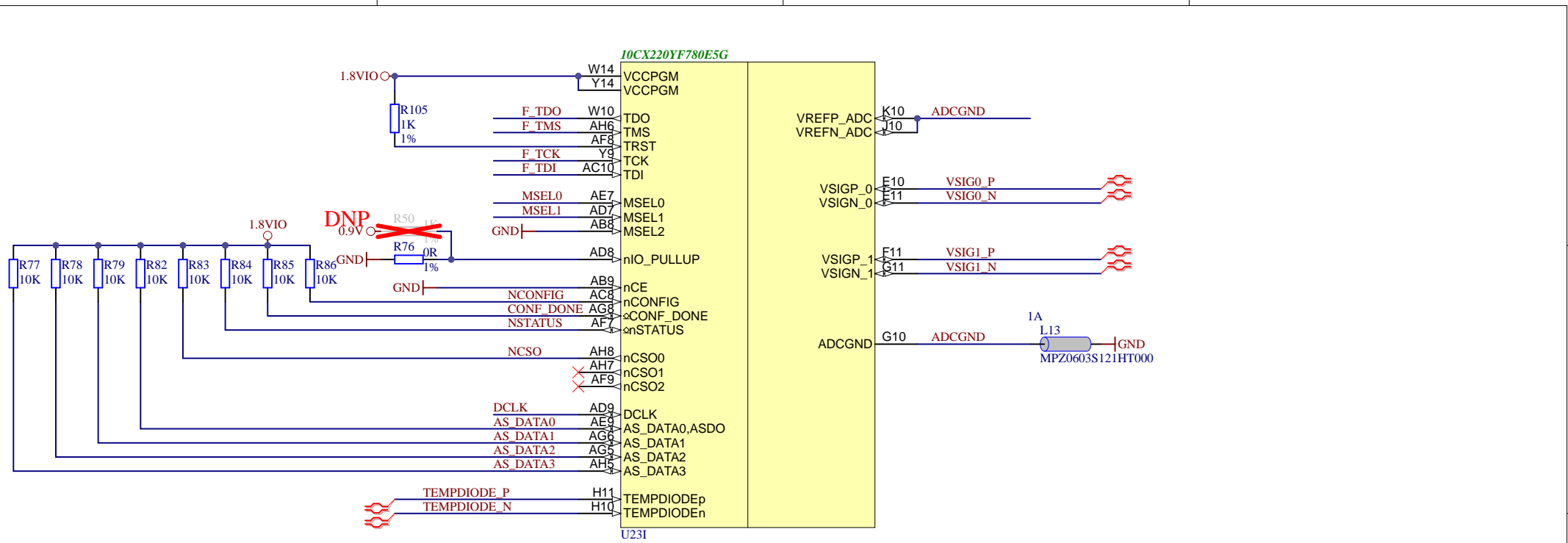
B

C

C

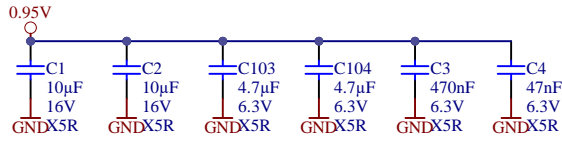
D

D

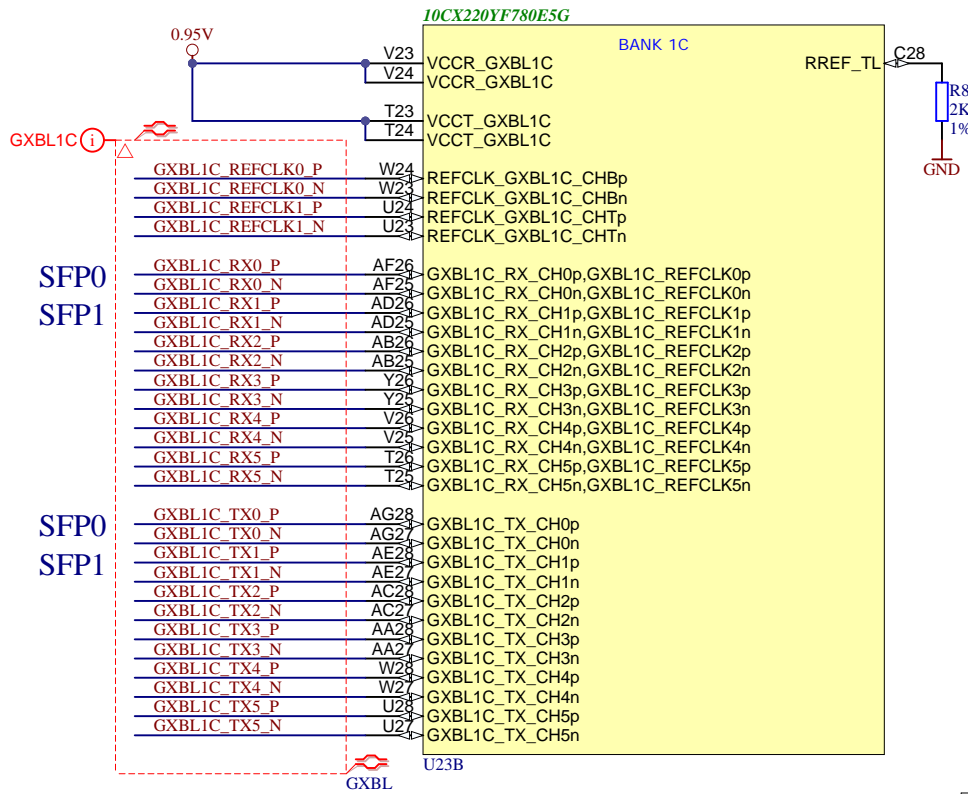
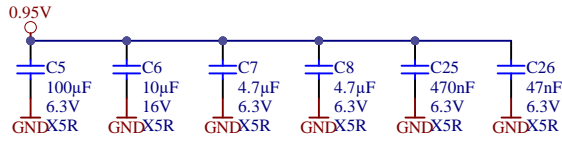



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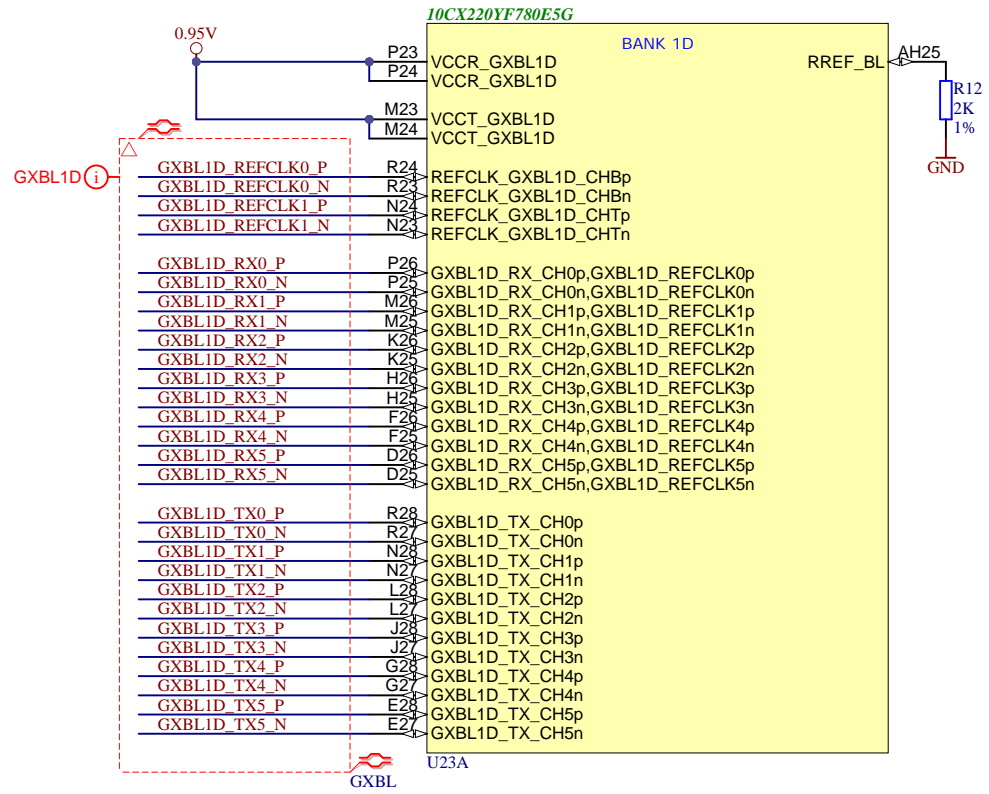
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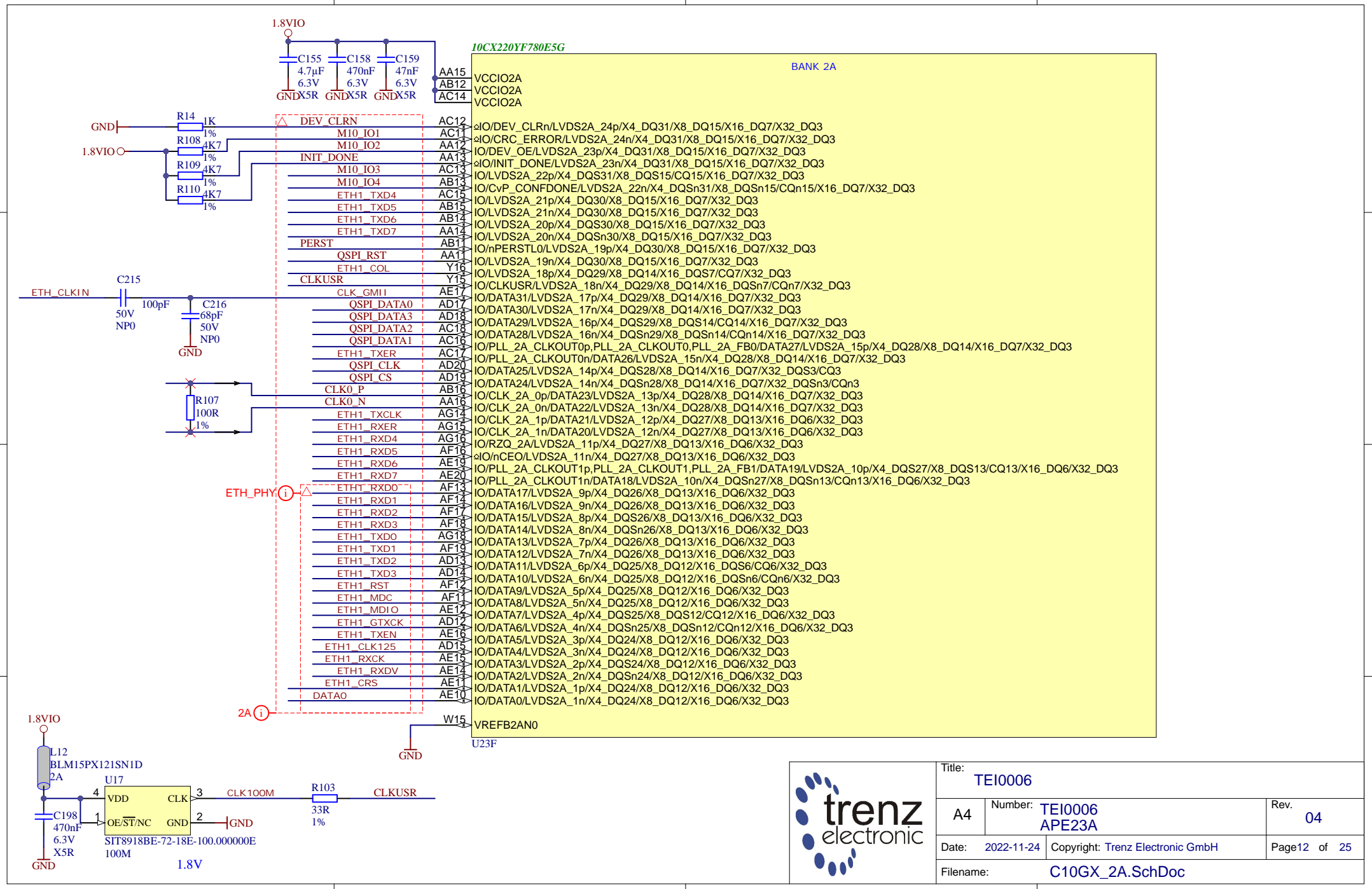
Placed at VCCR_GXB pins



			Title: TEI0006	
			A4	Number: TEI0006 APE23A
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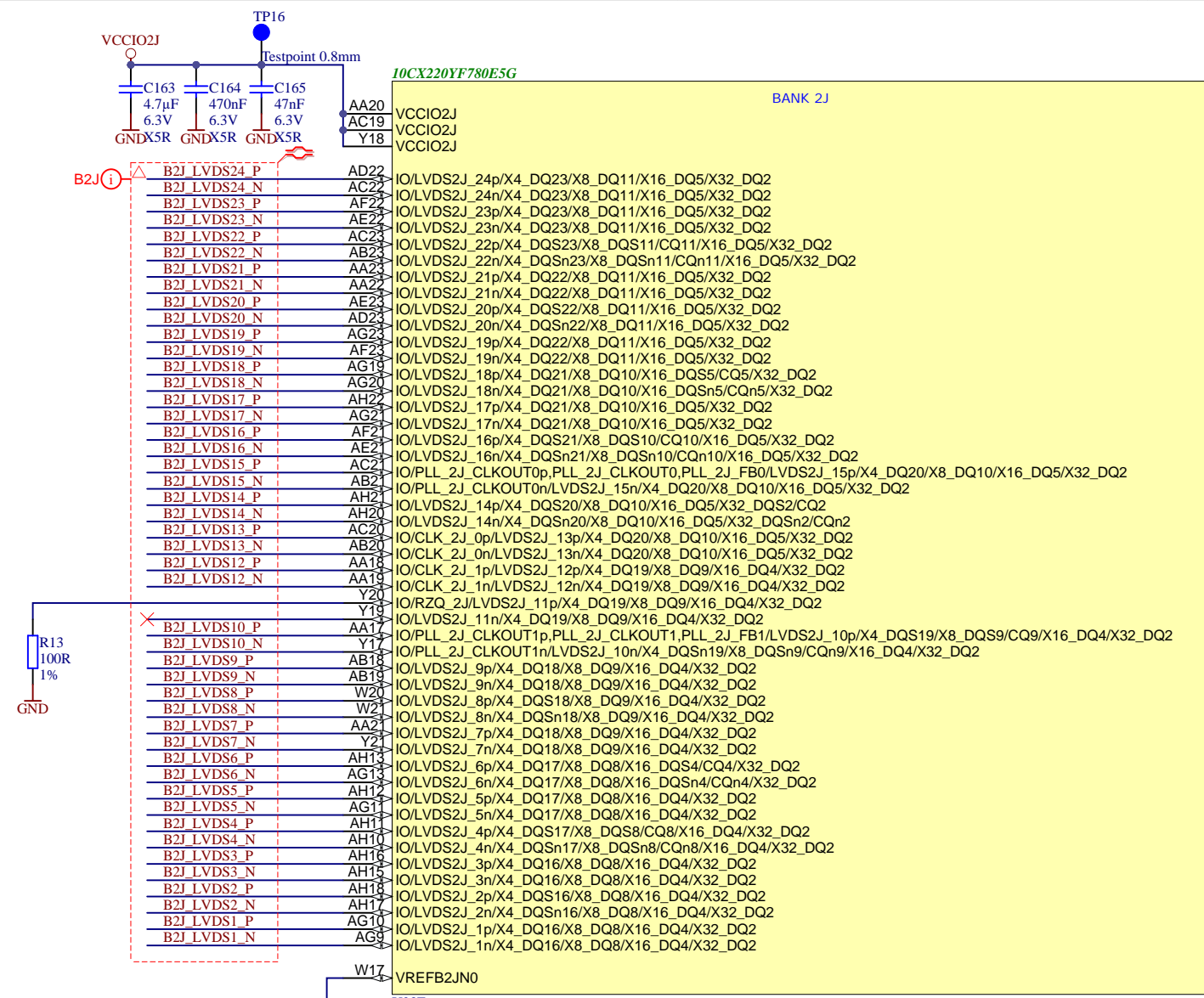
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BANK 2A

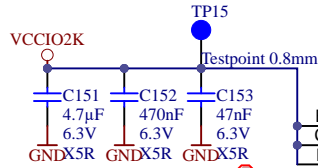
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AB12	VCCIO2A
AC14	VCCIO2A
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AC1	IO/CRC_ERROR/LVDS2A_24n/X4_DQ31/X8_DQ15/X16_DQ7/X32_DQ3
AA13	IO/DEV_OE/LVDS2A_23p/X4_DQ31/X8_DQ15/X16_DQ7/X32_DQ3
AA13	IO/INIT_DONE/LVDS2A_23n/X4_DQ31/X8_DQ15/X16_DQ7/X32_DQ3
AB13	IO/LVDS2A_22p/X4_DQS31/X8_DQS15/CQ15/X16_DQ7/X32_DQ3
AC13	IO/CvP_CONF/DONE/LVDS2A_22n/X4_DQSn31/X8_DQSn15/CQn15/X16_DQ7/X32_DQ3
AB13	IO/LVDS2A_21p/X4_DQ30/X8_DQ15/X16_DQ7/X32_DQ3
AC13	IO/LVDS2A_21n/X4_DQ30/X8_DQ15/X16_DQ7/X32_DQ3
AB13	IO/LVDS2A_20p/X4_DQS30/X8_DQ15/X16_DQ7/X32_DQ3
AB13	IO/LVDS2A_20n/X4_DQSn30/X8_DQ15/X16_DQ7/X32_DQ3
AA14	IO/mPERSTL0/LVDS2A_19p/X4_DQ30/X8_DQ15/X16_DQ7/X32_DQ3
AB1	IO/LVDS2A_19n/X4_DQ30/X8_DQ15/X16_DQ7/X32_DQ3
Y16	IO/LVDS2A_18p/X4_DQ29/X8_DQ14/X16_DQS7/CQ7/X32_DQ3
Y15	IO/CLKUSR/LVDS2A_18n/X4_DQ29/X8_DQ14/X16_DQSn7/CQn7/X32_DQ3
AE1	IO/DATA31/LVDS2A_17p/X4_DQ29/X8_DQ14/X16_DQ7/X32_DQ3
AD1	IO/DATA30/LVDS2A_17n/X4_DQ29/X8_DQ14/X16_DQ7/X32_DQ3
AD18	IO/DATA29/LVDS2A_16p/X4_DQS29/X8_DQS14/CQ14/X16_DQ7/X32_DQ3
AC18	IO/DATA28/LVDS2A_16n/X4_DQSn29/X8_DQSn14/CQn14/X16_DQ7/X32_DQ3
AC16	IO/PLL_2A_CLKOUT0p,PLL_2A_CLKOUT0,PLL_2A_FB0/DATA27/LVDS2A_15p/X4_DQ28/X8_DQ14/X16_DQ7/X32_DQ3
AD2	IO/DATA25/LVDS2A_14p/X4_DQS28/X8_DQ14/X16_DQ7/X32_DQS3/CQ3
AD19	IO/DATA24/LVDS2A_14n/X4_DQSn28/X8_DQ14/X16_DQ7/X32_DQSn3/CQn3
AB16	IO/CLK_2A_0p/DATA23/LVDS2A_13p/X4_DQ28/X8_DQ14/X16_DQ7/X32_DQ3
AA16	IO/CLK_2A_0n/DATA22/LVDS2A_13n/X4_DQ28/X8_DQ14/X16_DQ7/X32_DQ3
AG1	IO/CLK_2A_1p/DATA21/LVDS2A_12p/X4_DQ27/X8_DQ13/X16_DQ6/X32_DQ3
AG16	IO/CLK_2A_1n/DATA20/LVDS2A_12n/X4_DQ27/X8_DQ13/X16_DQ6/X32_DQ3
AF16	IO/RZQ_2A/LVDS2A_11p/X4_DQ27/X8_DQ13/X16_DQ6/X32_DQ3
AE19	IO/nCEO/LVDS2A_11n/X4_DQ27/X8_DQ13/X16_DQ6/X32_DQ3
AE2	IO/PLL_2A_CLKOUT1p,PLL_2A_CLKOUT1,PLL_2A_FB1/DATA19/LVDS2A_10p/X4_DQS27/X8_DQS13/CQ13/X16_DQ6/X32_DQ3
AF1	IO/DATA17/LVDS2A_9p/X4_DQ26/X8_DQ13/X16_DQ6/X32_DQ3
AF14	IO/DATA16/LVDS2A_9n/X4_DQ26/X8_DQ13/X16_DQ6/X32_DQ3
AF17	IO/DATA15/LVDS2A_8p/X4_DQS26/X8_DQ13/X16_DQ6/X32_DQ3
AF18	IO/DATA14/LVDS2A_8n/X4_DQSn26/X8_DQ13/X16_DQ6/X32_DQ3
AG13	IO/DATA13/LVDS2A_7p/X4_DQ26/X8_DQ13/X16_DQ6/X32_DQ3
AF19	IO/DATA12/LVDS2A_7n/X4_DQ26/X8_DQ13/X16_DQ6/X32_DQ3
AD13	IO/DATA11/LVDS2A_6p/X4_DQ25/X8_DQ12/X16_DQS6/CQ6/X32_DQ3
AF1	IO/DATA10/LVDS2A_6n/X4_DQ25/X8_DQ12/X16_DQSn6/CQn6/X32_DQ3
AF1	IO/DATA9/LVDS2A_5p/X4_DQ25/X8_DQ12/X16_DQ6/X32_DQ3
AF1	IO/DATA8/LVDS2A_5n/X4_DQ25/X8_DQ12/X16_DQ6/X32_DQ3
AE12	IO/DATA7/LVDS2A_4p/X4_DQS25/X8_DQS12/CQ12/X16_DQ6/X32_DQ3
AD12	IO/DATA6/LVDS2A_4n/X4_DQSn25/X8_DQSn12/CQn12/X16_DQ6/X32_DQ3
AE16	IO/DATA5/LVDS2A_3p/X4_DQ24/X8_DQ12/X16_DQ6/X32_DQ3
AD1	IO/DATA4/LVDS2A_3n/X4_DQ24/X8_DQ12/X16_DQ6/X32_DQ3
AE13	IO/DATA3/LVDS2A_2p/X4_DQS24/X8_DQ12/X16_DQ6/X32_DQ3
AE14	IO/DATA2/LVDS2A_2n/X4_DQSn24/X8_DQ12/X16_DQ6/X32_DQ3
AE11	IO/DATA1/LVDS2A_1p/X4_DQ24/X8_DQ12/X16_DQ6/X32_DQ3
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W15	VREFB2A0
U23F	



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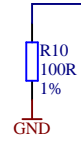
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10CX220YF780ESG

BANK 2K

B2K i



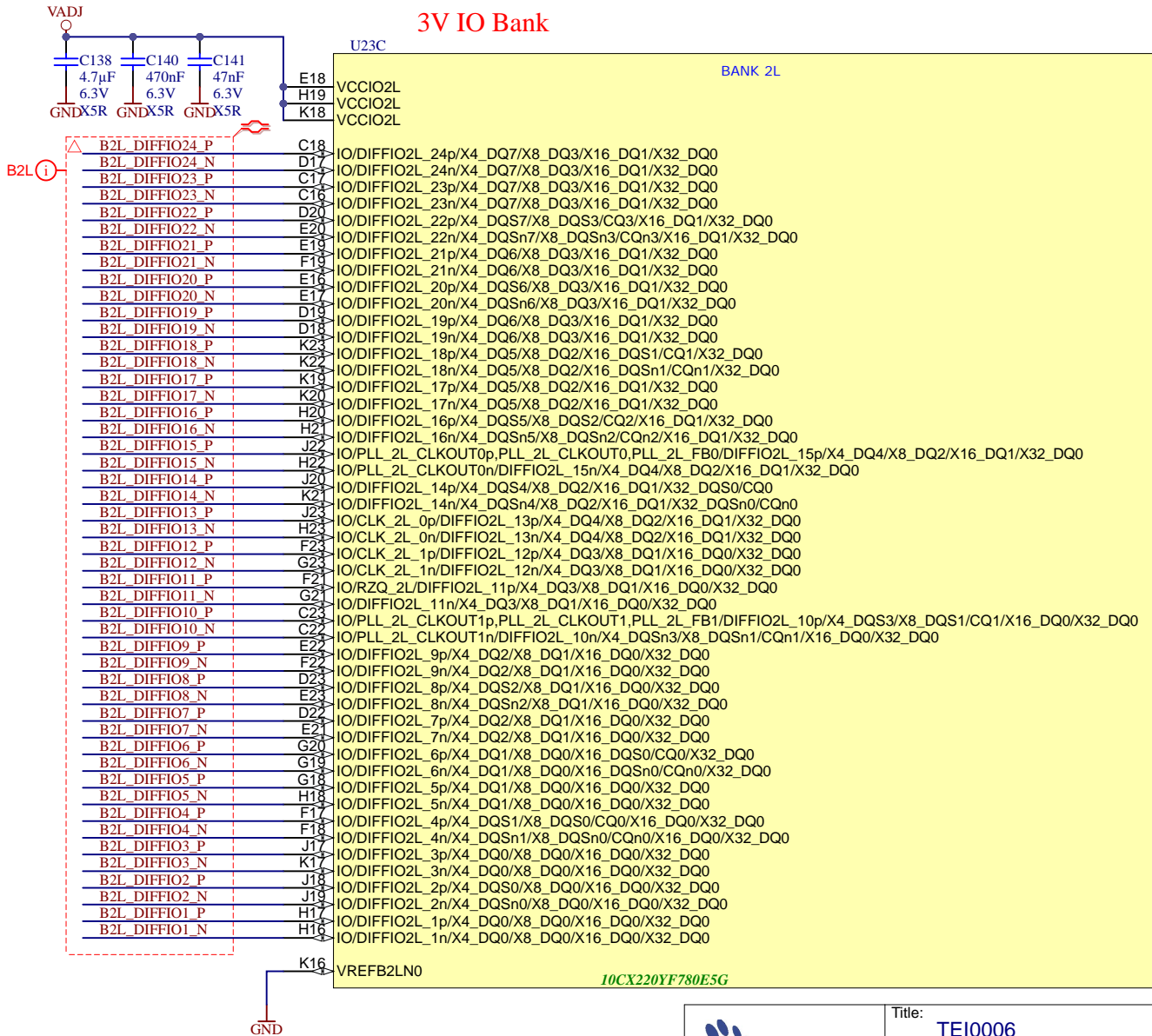
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B2K LVDS18 N	B25
B2K LVDS17 P	A21
B2K LVDS17 N	A22
B2K LVDS16 P	A27
B2K LVDS16 N	A26
B2K LVDS15 P	B27
B2K LVDS15 N	B25
B2K LVDS14 P	B21
B2K LVDS14 N	C21
B2K LVDS13 P	A24
B2K LVDS13 N	A23
B2K LVDS12 P	D11
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B2K LVDS10 P	B20
B2K LVDS10 N	C20
B2K LVDS9 P	B11
B2K LVDS9 N	B10
B2K LVDS7 P	C15
B2K LVDS7 N	A19
B2K LVDS8 P	A1
B2K LVDS8 N	A16
B2K LVDS6 P	D9
B2K LVDS6 N	D10
B2K LVDS5 P	C5
B2K LVDS5 N	D8
B2K LVDS4 P	A9
B2K LVDS4 N	A8
B2K LVDS3 P	C17
B2K LVDS3 N	C1
B2K LVDS2 P	B10
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B2K LVDS1 P	B9
B2K LVDS1 N	B8

VCCIO2K	B12	IO/LVDS2K_24p/X4_DQ15/X8_DQ7/X16_DQ3/X32_DQ1
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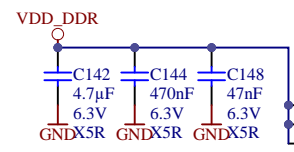
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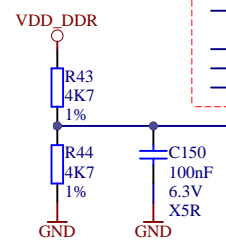
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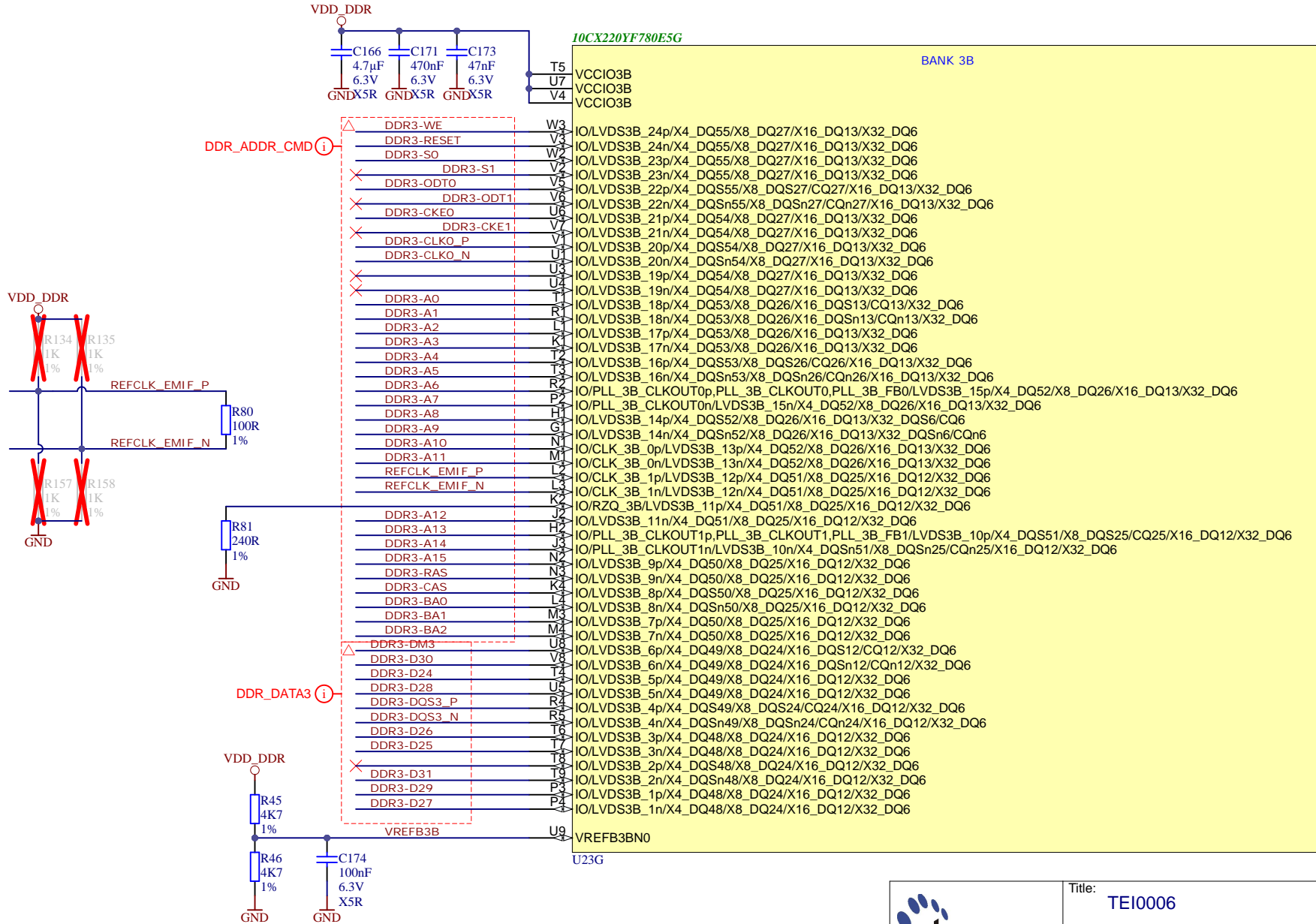
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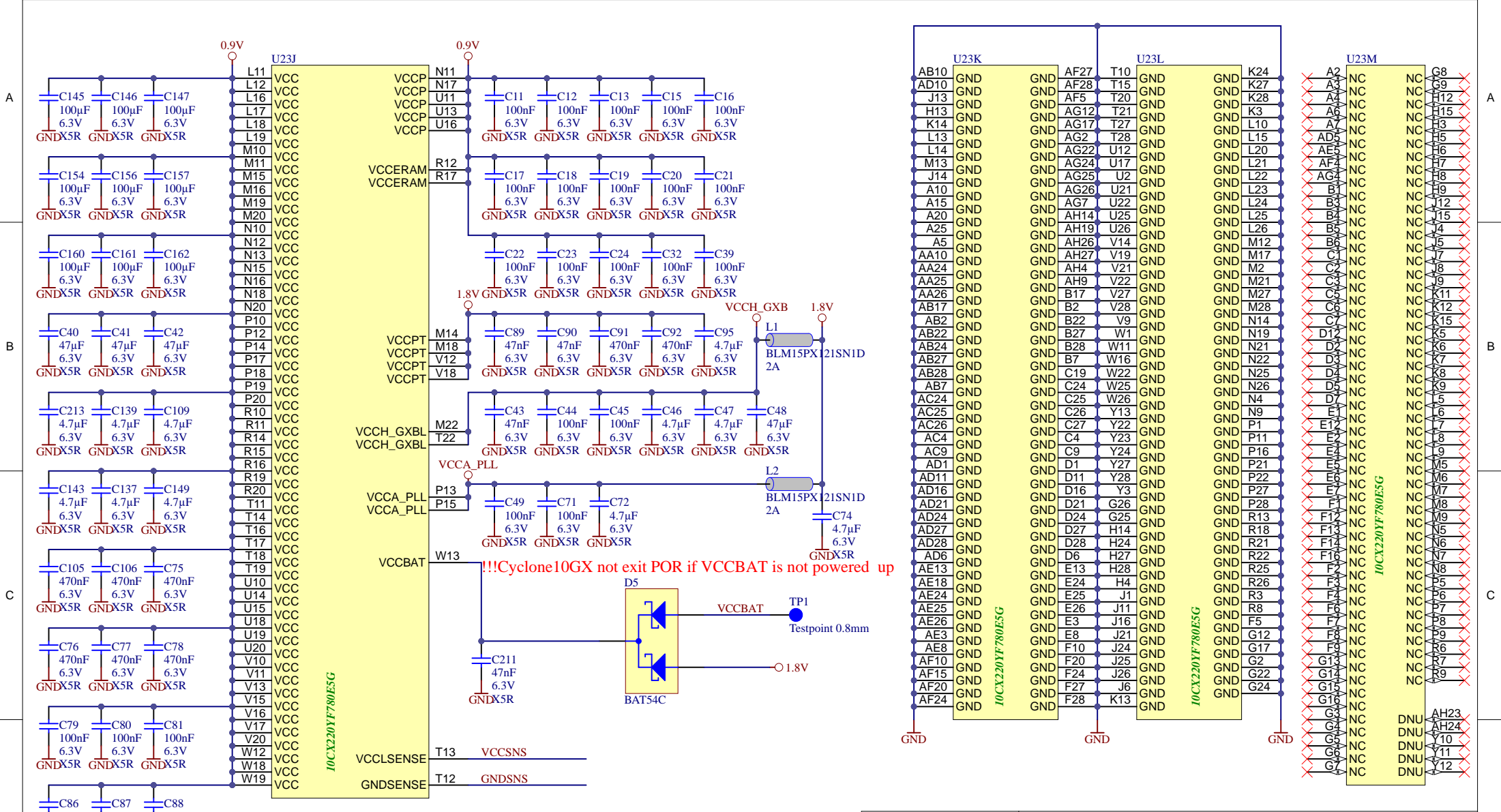
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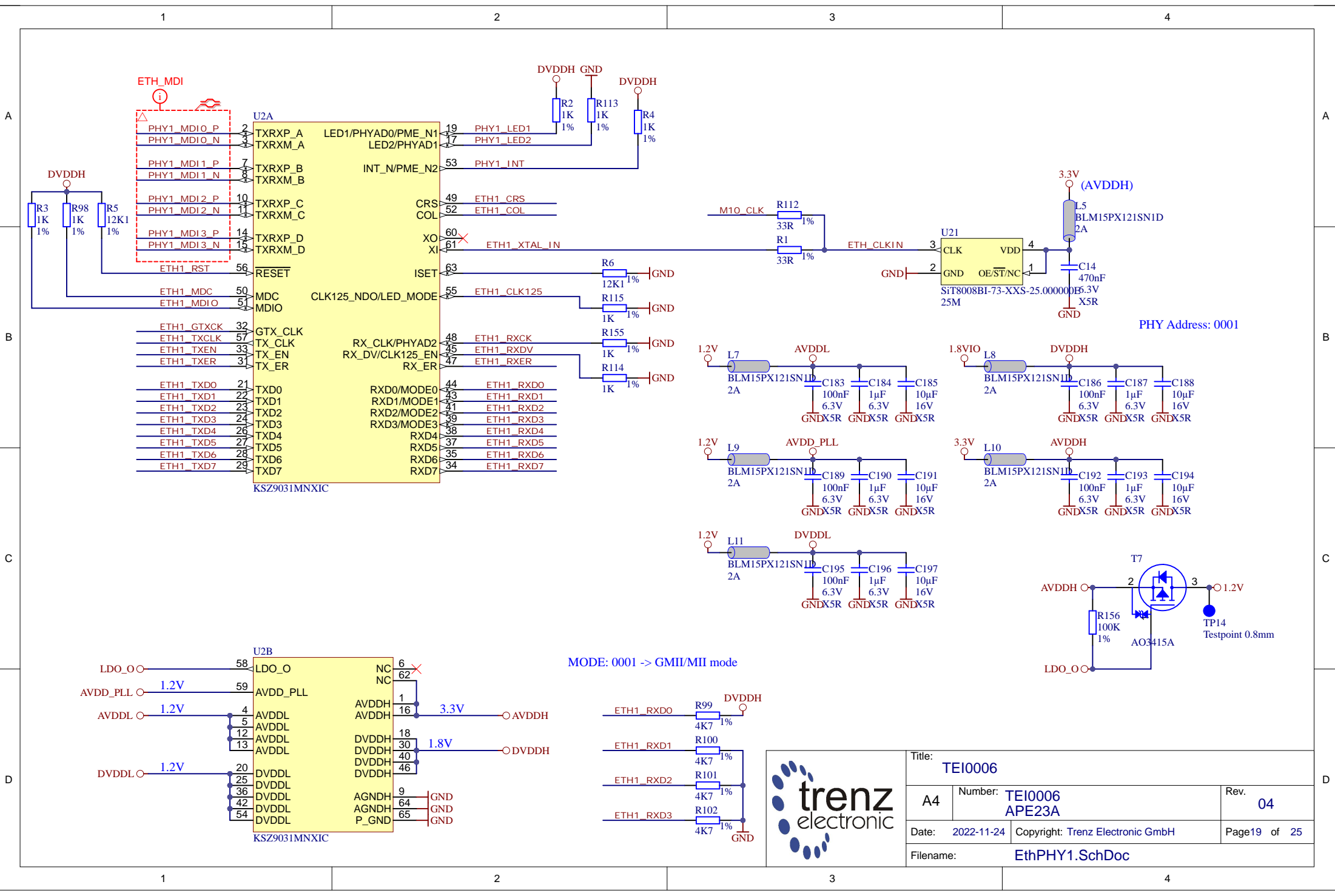
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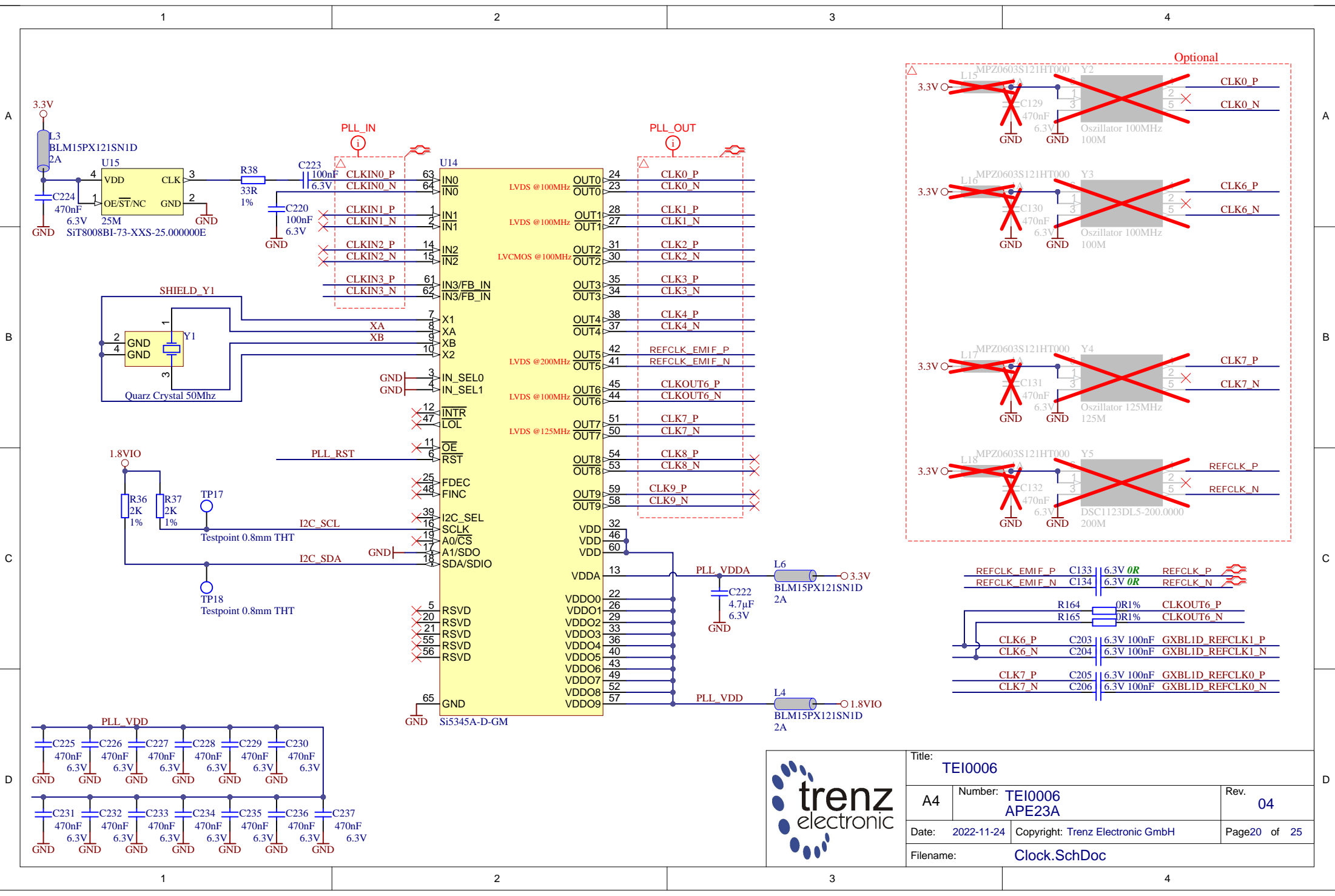
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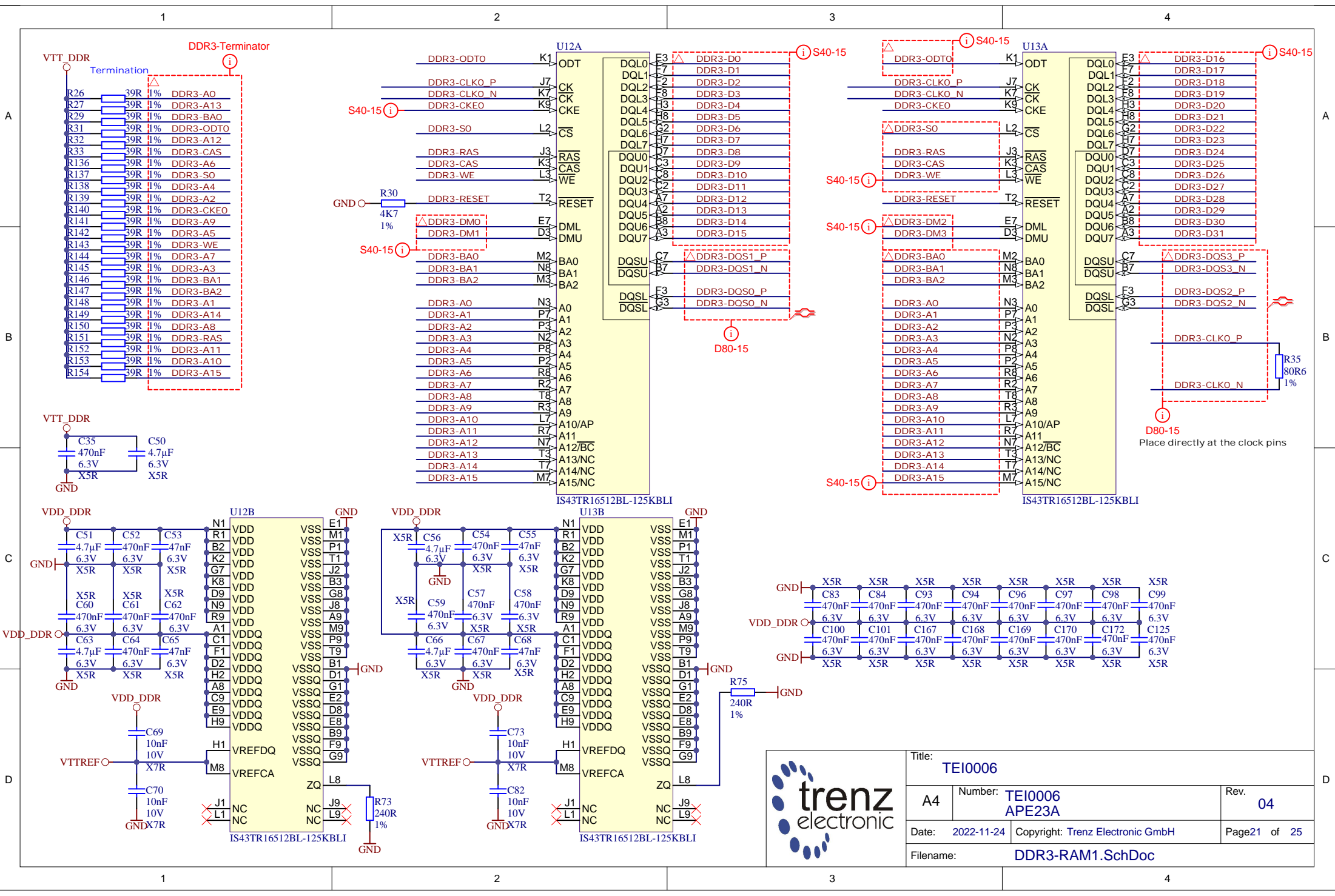


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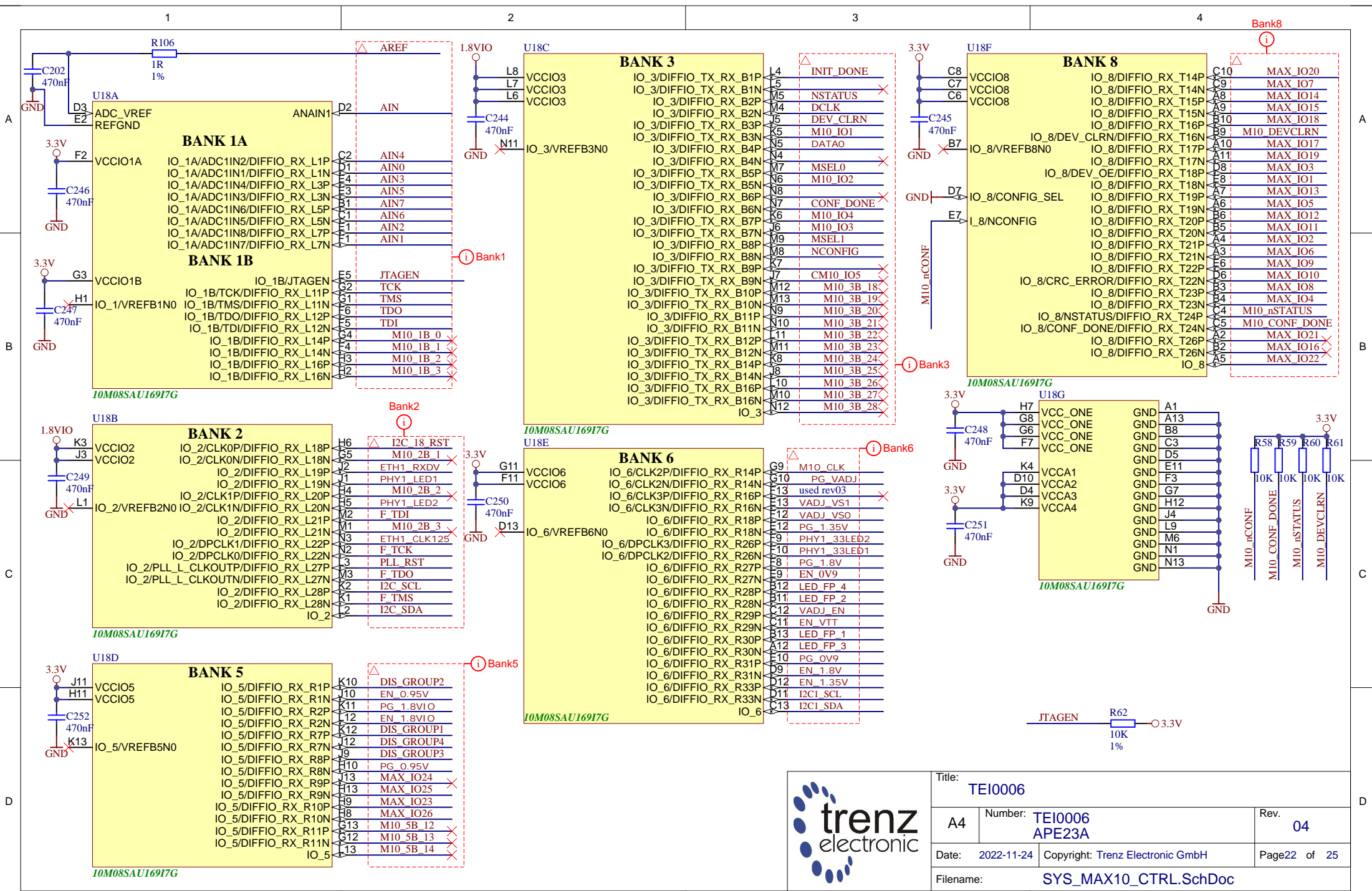


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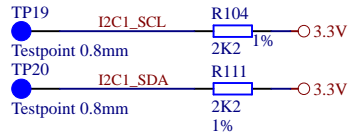
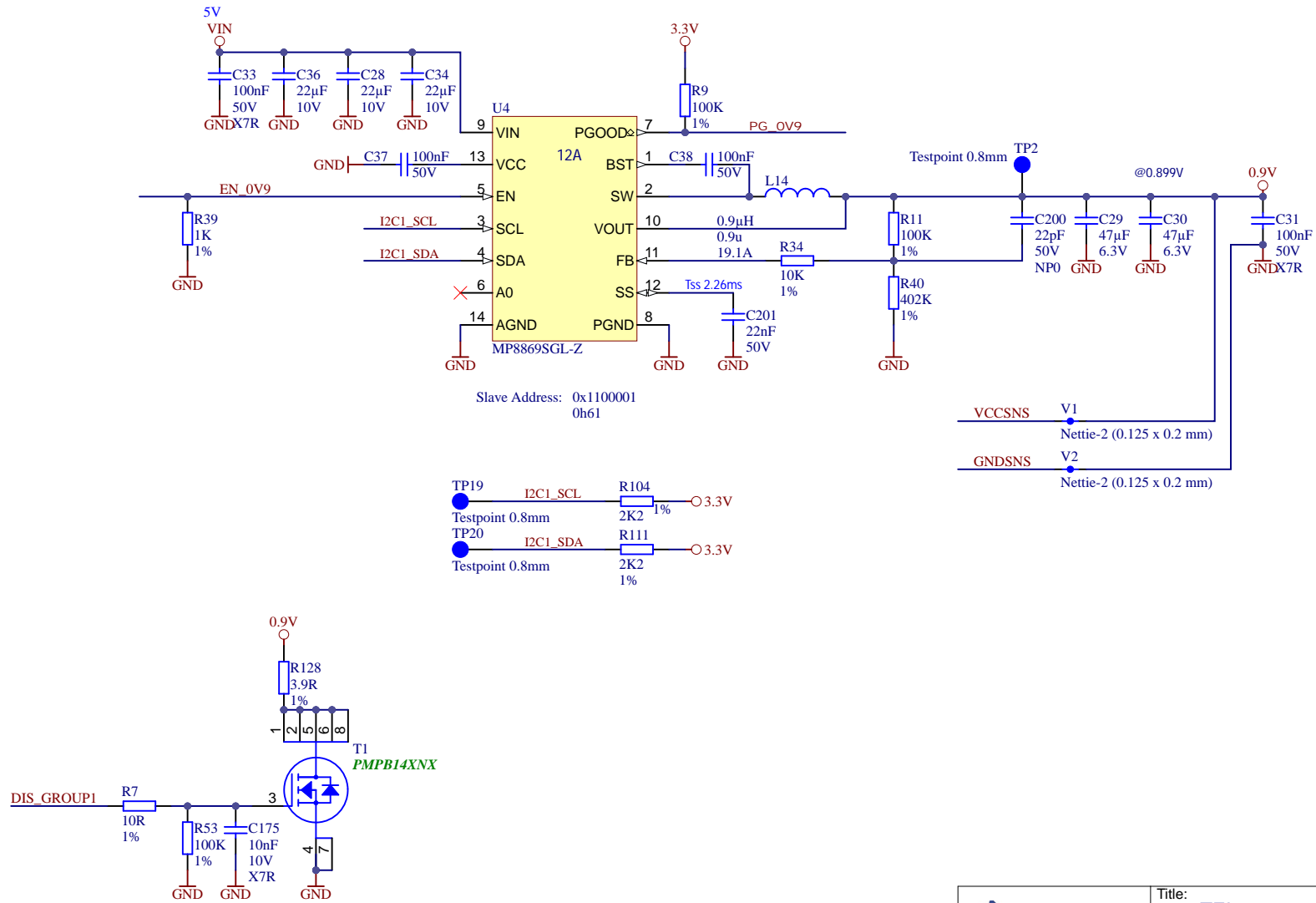




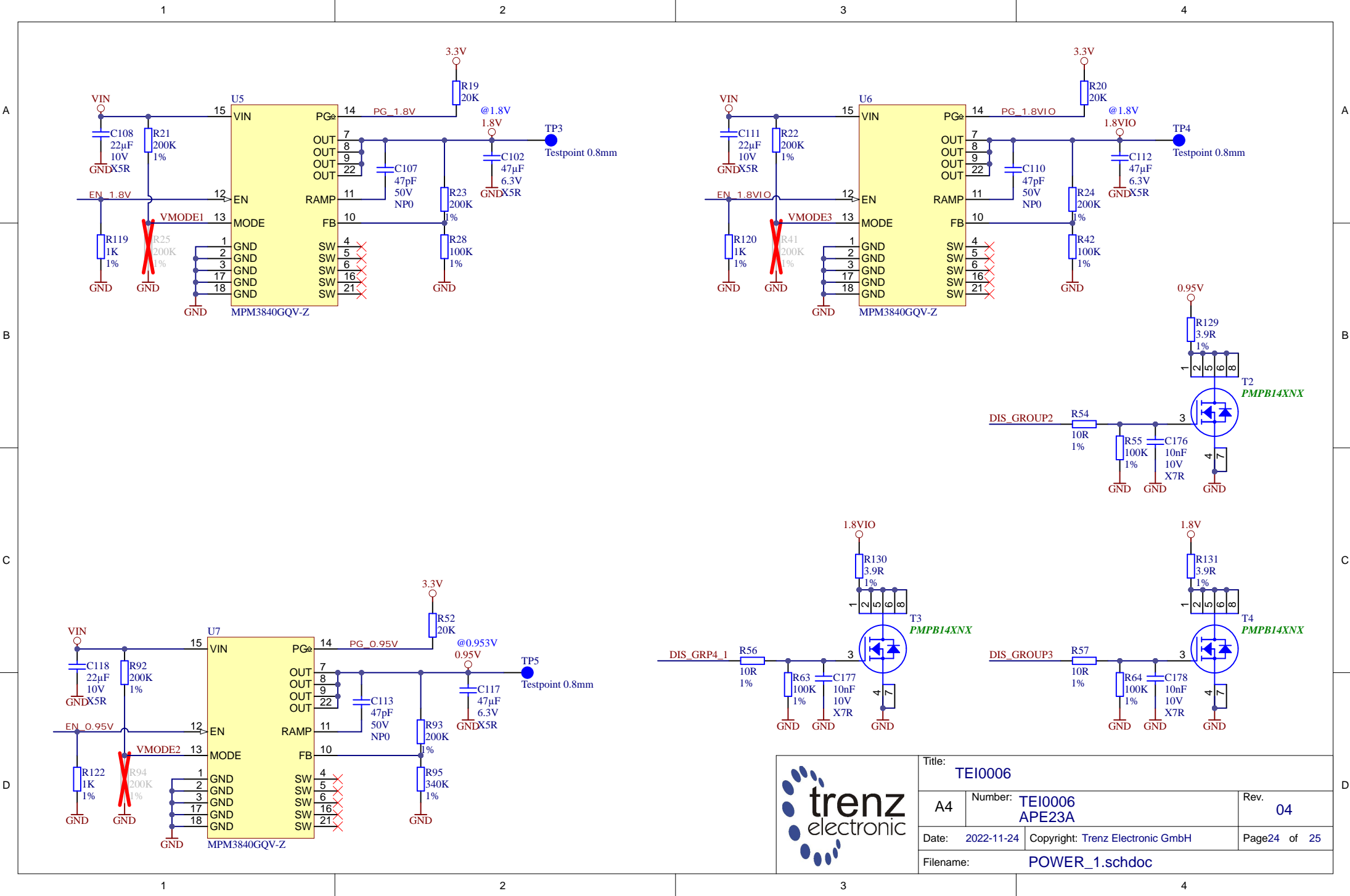

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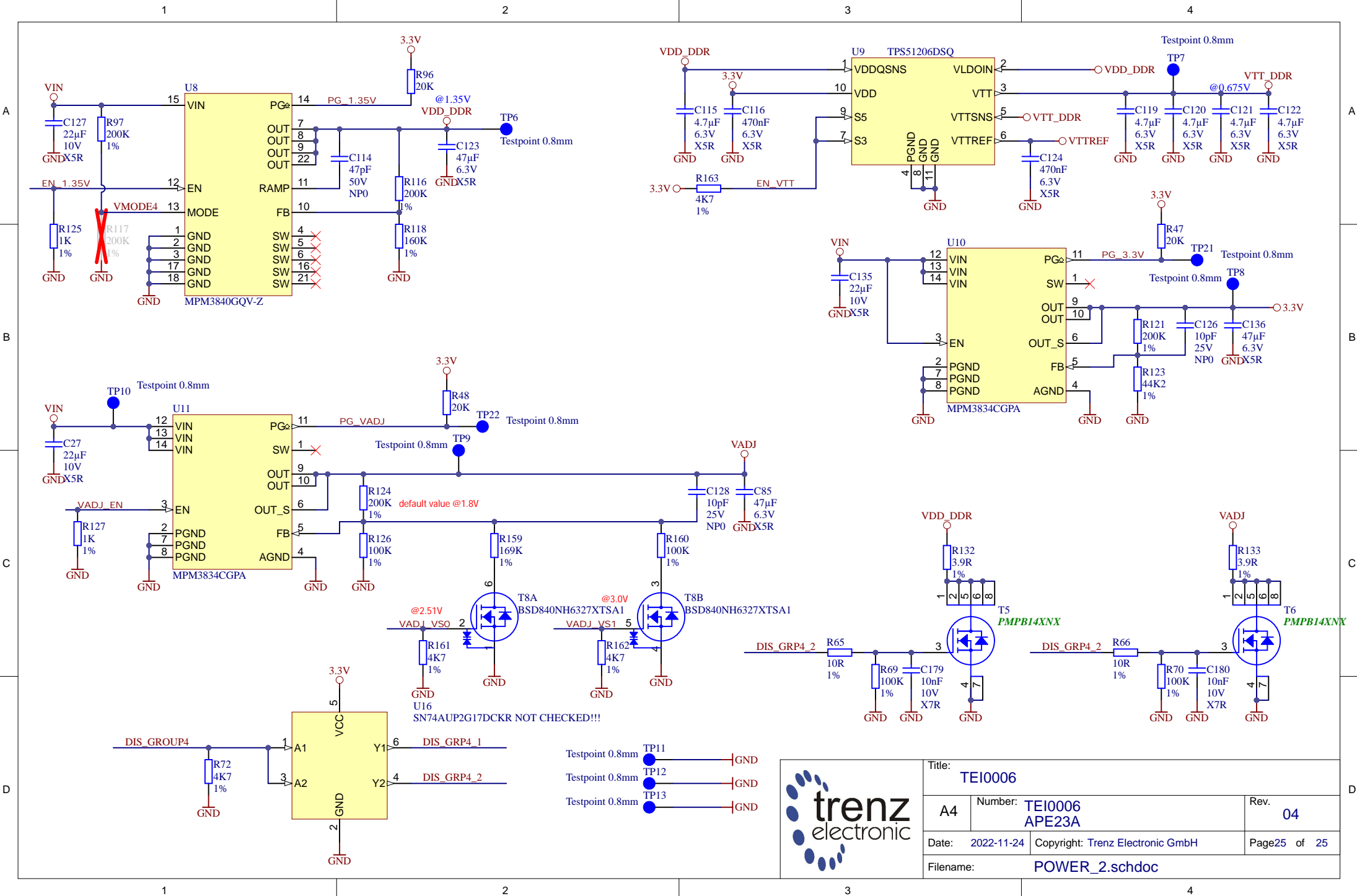
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