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U_DDR3-RAM
DDR3-RAM.SchDoc

U_Ethernet
Ethernet.SchDoc

U_USB-PHY
USB-PHY.SchDoc

U_SOC
SOC.SchDoc

U_CPLD
CPLD.SchDoc

U_POWER2
POWER2.SchDoc

U_HyperFlash_RAM
HyperFlash_RAM.SchDoc

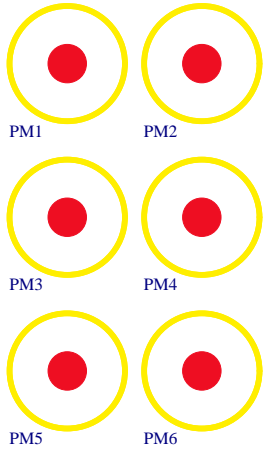
U_Clock
Clock.SchDoc

U_eMMC
eMMC.SchDoc

U_Connectors
Connectors.SchDoc

U_POWER
POWER.SchDoc

LOGO1
TE Logo PRINT Layer
LOGO PRINT



Serial
Serialnumber 6,3 x 6.3mm



Title: TE0782 - Overview		
A4	Number: TE0782 92I33FA	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page1 of 31
Filename: TE0782.SchDoc		

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U_HSMC_CONN_J1
HSMC_CONN_J1.SchDoc



U_HSMC_CONN_J2
HSMC_CONN_J2.SchDoc



U_HSMC_CONN_J3
HSMC_CONN_J3.SchDoc



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			Title: TE0782 - Connectors		
			A4	Number: TE0782 92I33FA	Rev. 02
Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page 2 of 31	
Filename: Connectors.SchDoc					

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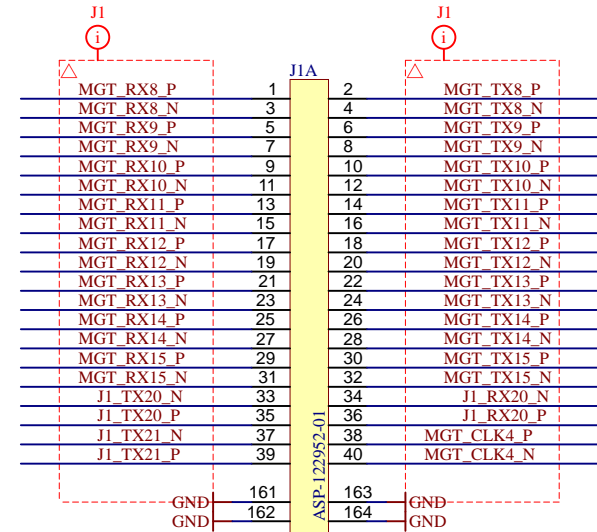
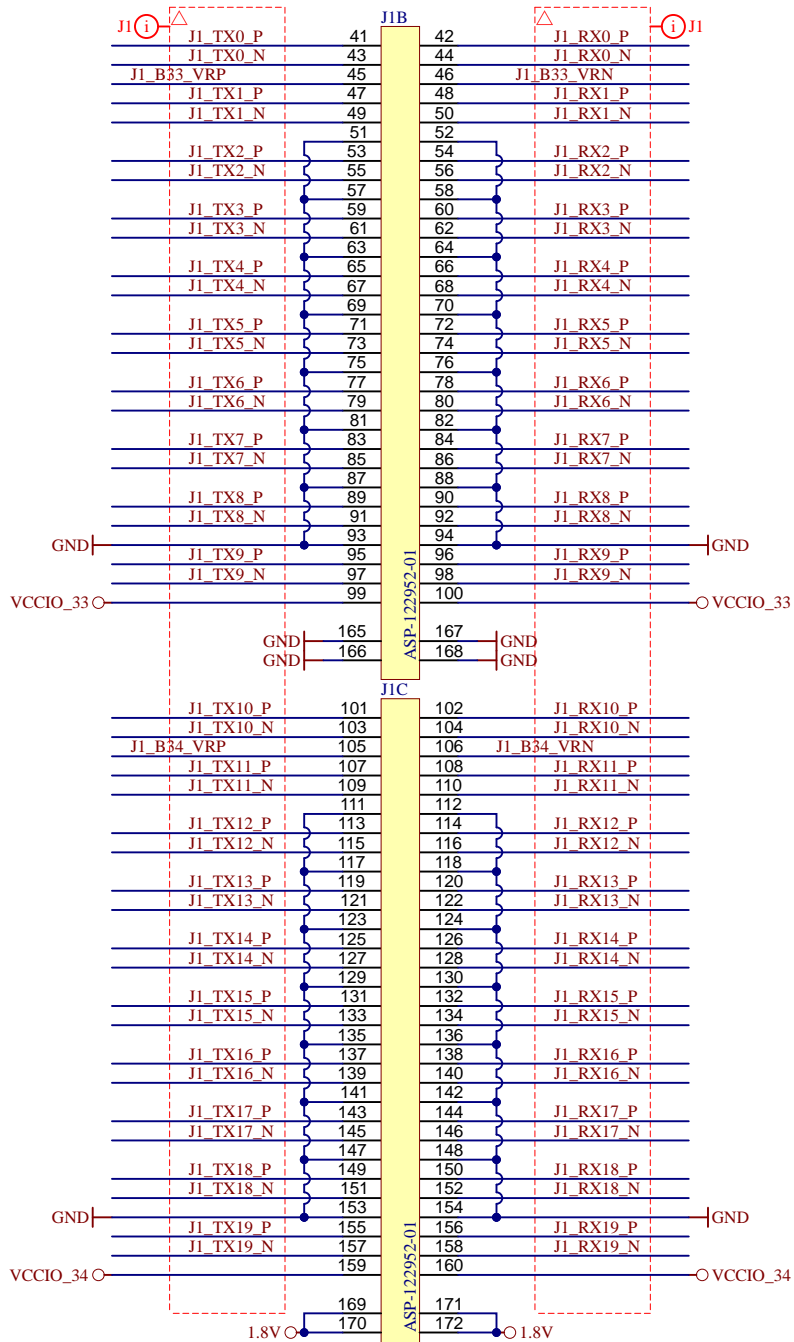

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Title: TE0782 - HSMC_Connector_J1		
A4	Number: TE0782 92I33FA	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page3 of 31
Filename: HSMC_CONN_J1.SchDoc		

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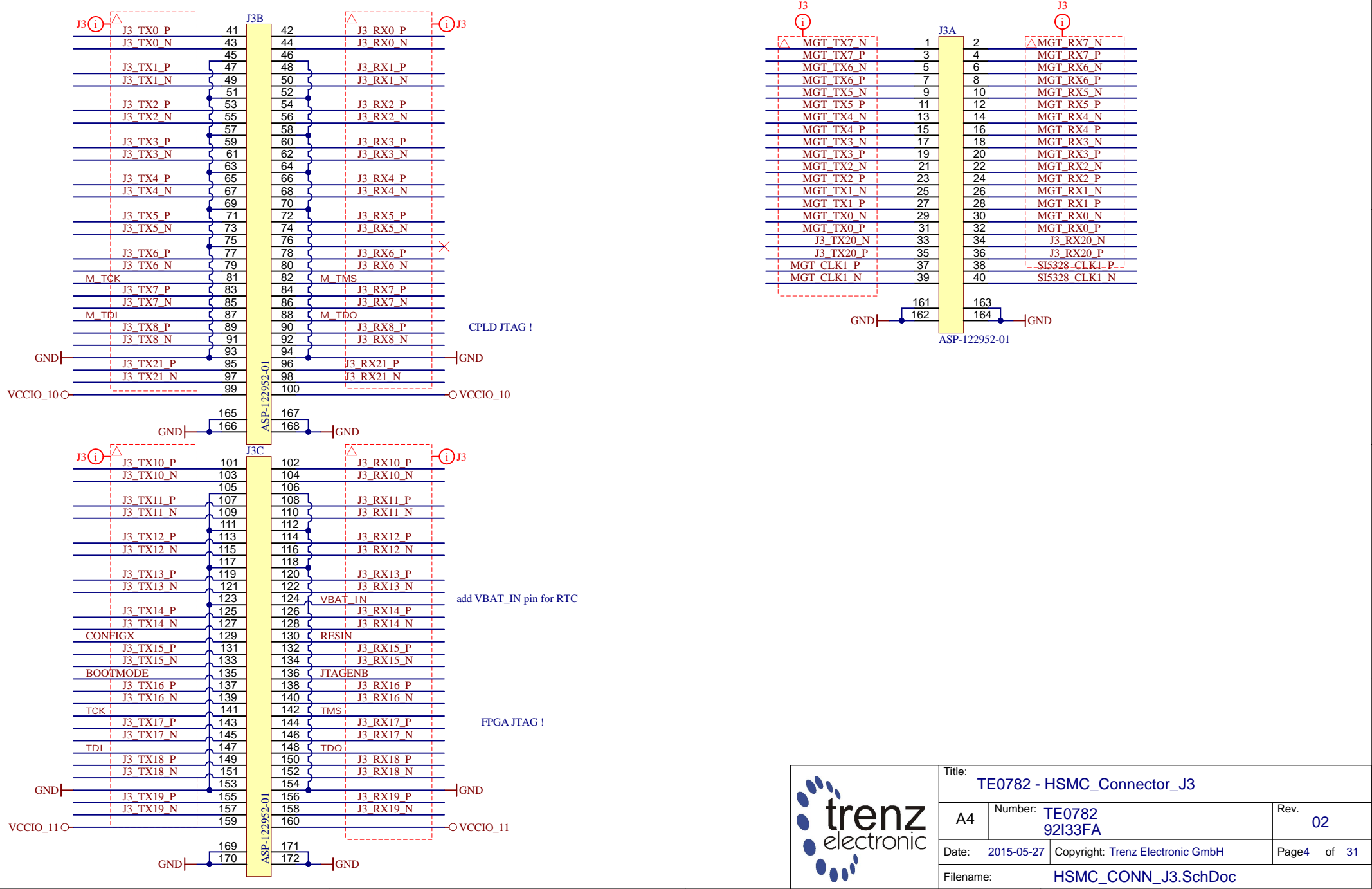
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Title: TE0782 - HSMC_Connector_J3		
A4	Number: TE0782 92I33FA	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page4 of 31
Filename: HSMC_CONN_J3.SchDoc		

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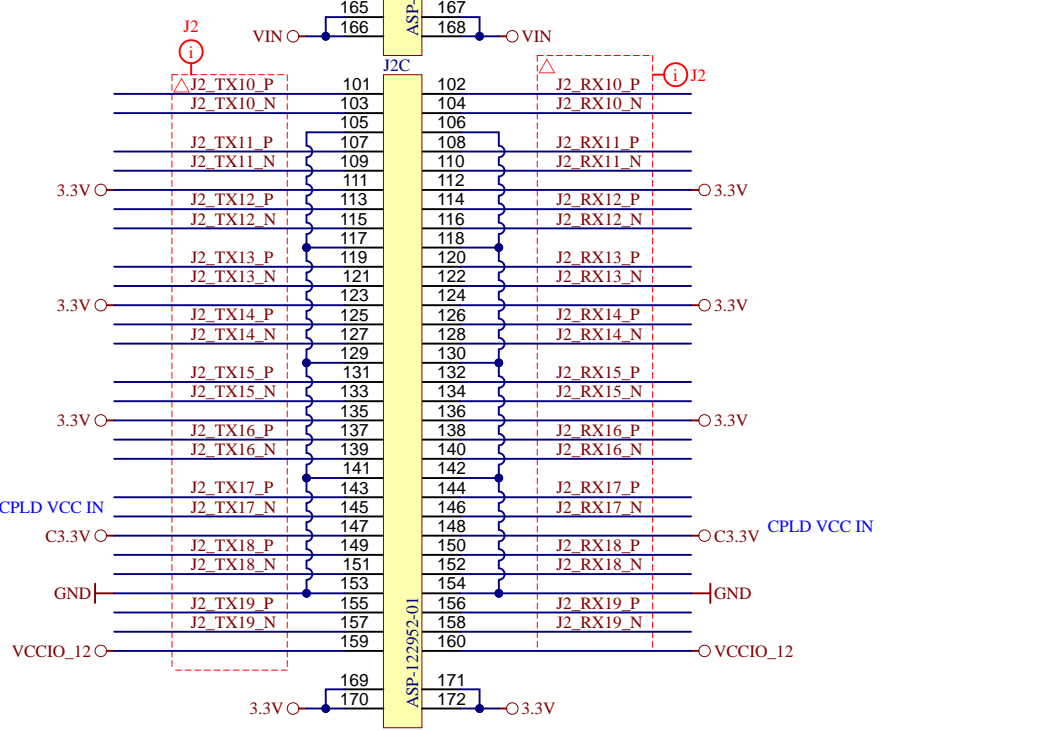
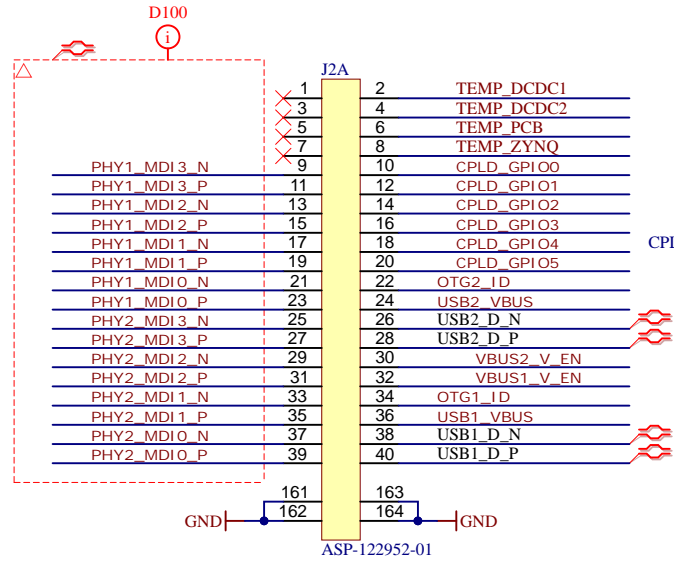
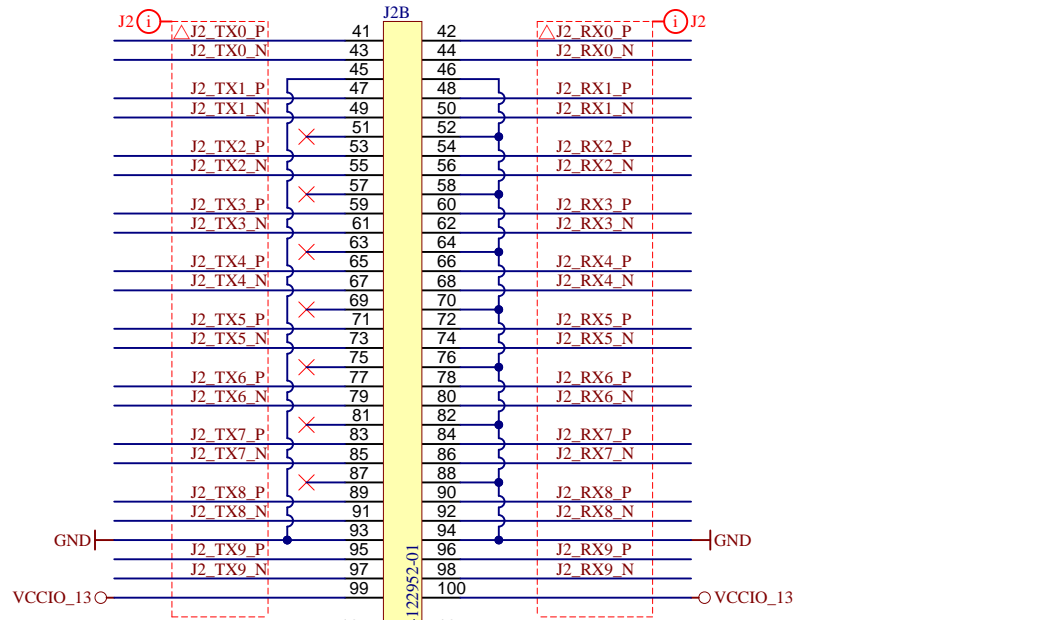
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Title: TE0782 - HSMC_Connector_J2		
A4	Number: TE0782 92I33FA	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page5 of 31
Filename: HSMC_CONN_J2.SchDoc		

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U_PS-DDR
PS-DDR.SchDoc



U_B9
B9.SchDoc



U_MIO-BANKS
MIO-BANKS.SchDoc



U_B10
B10.SchDoc



U_HP-BANKS
HP-BANKS.SchDoc



U_B11
B11.SchDoc



B

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U_FPGA-MGT
FPGA-MGT.SchDoc



U_B12
B12.SchDoc



U_FPGA-CFG
FPGA-CFG.SchDoc



U_B13
B13.SchDoc



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U_FPGA-PWR
FPGA-PWR.SchDoc



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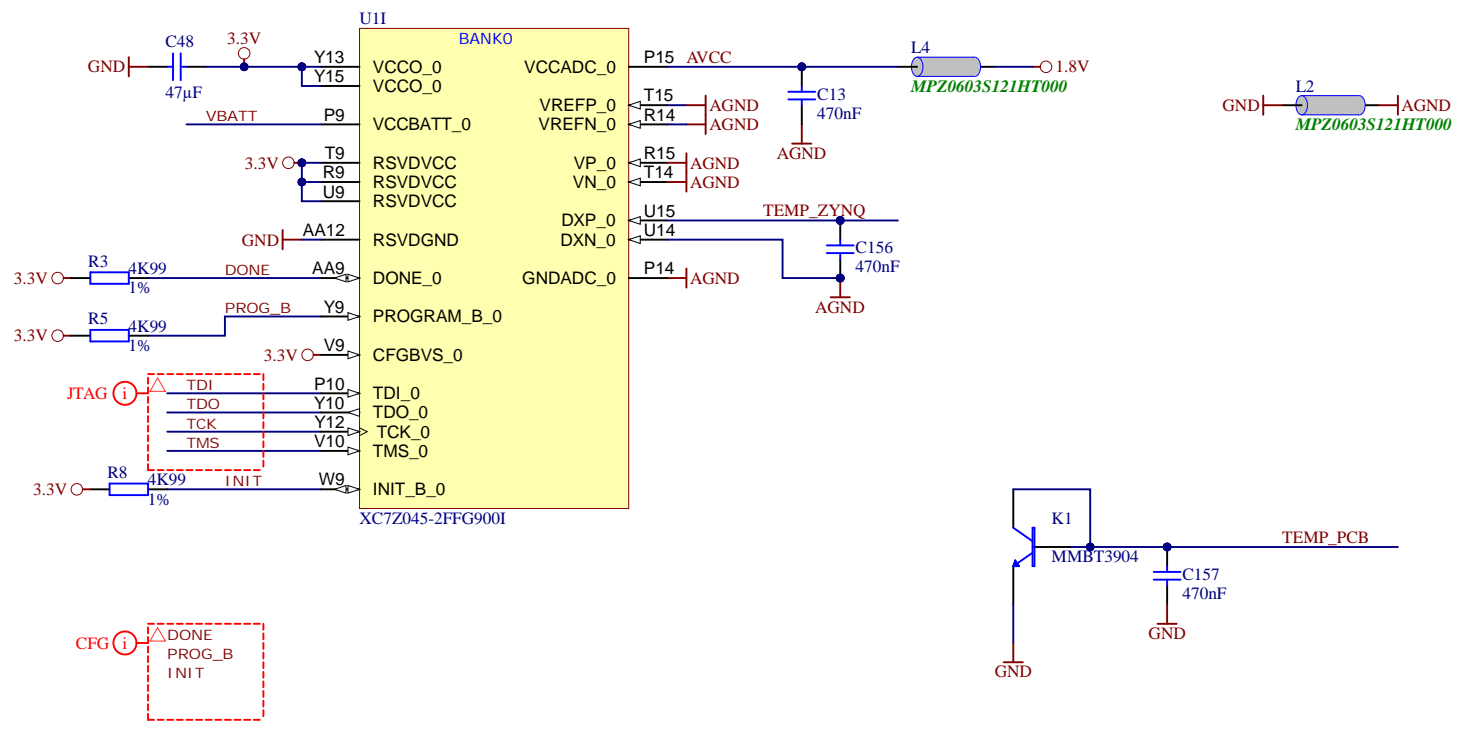
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Date: 2015-05-27		Copyright: Trenz Electronic GmbH	
Filename: SOC.SchDoc		Page6 of 31	


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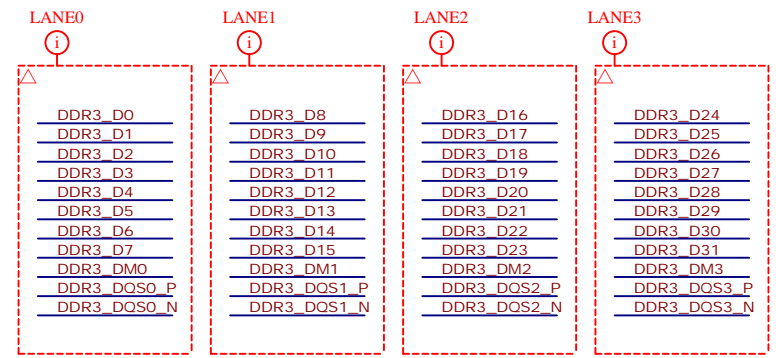
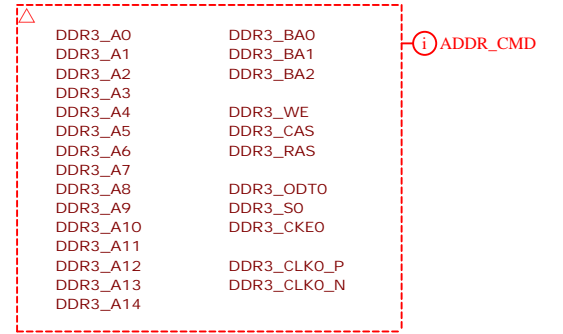
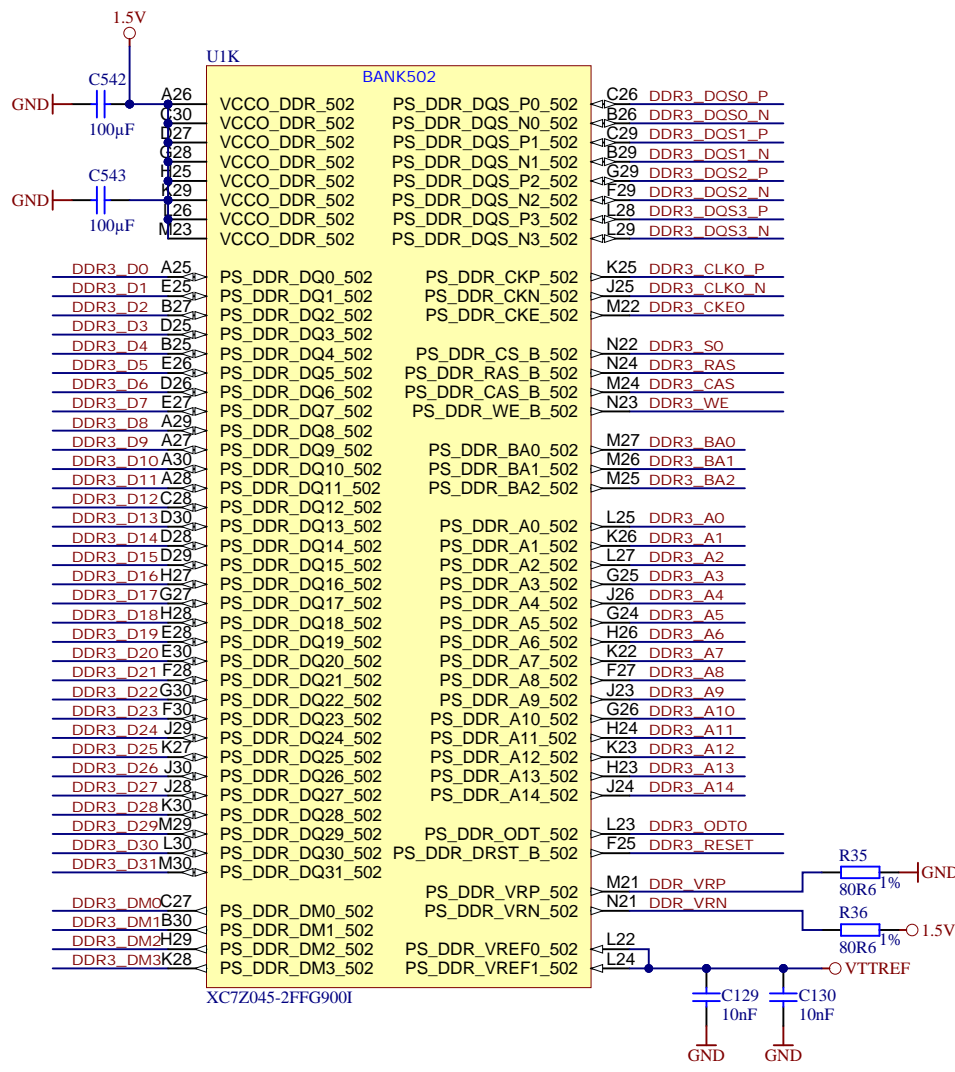
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Datum: 2015-05-27		Zeichner: Trenz Electronic GmbH	
Filename: FPGA-CFG.SchDoc		Blatt 7 von 31	

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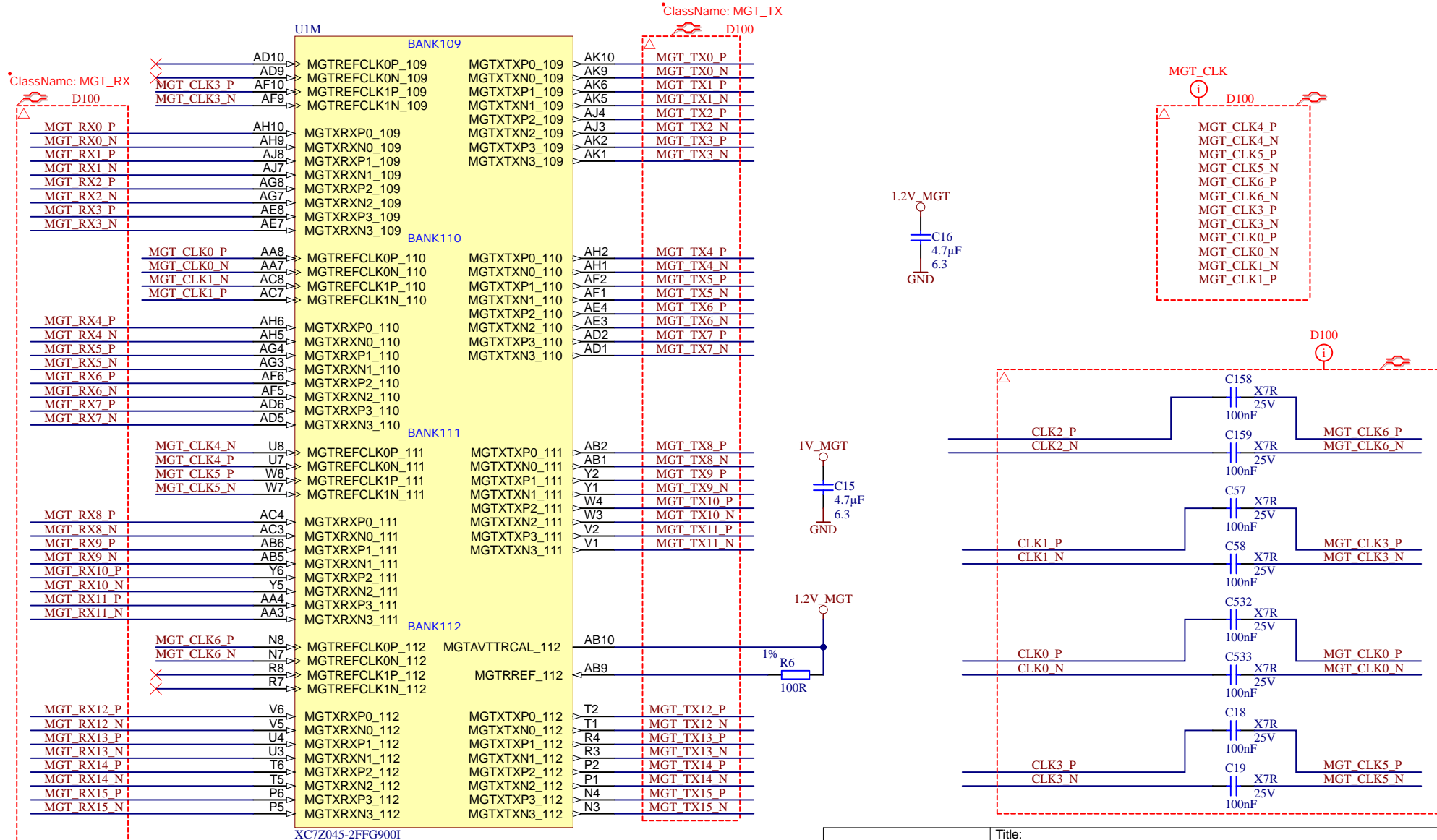
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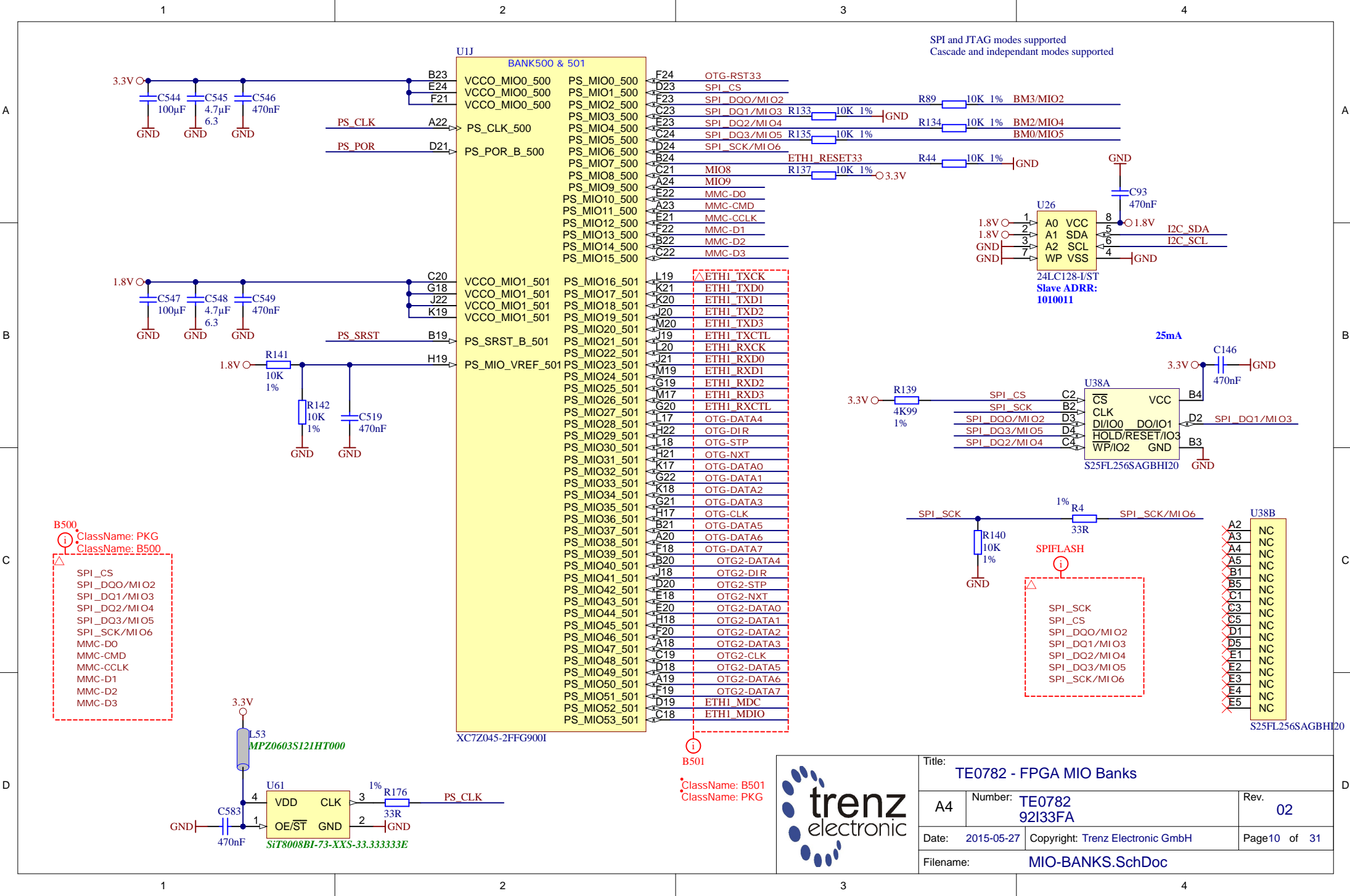
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Title: TE0782 - FPGA DDR Banks		
A4	Number: TE0782 92I33FA	Rev. 02
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Filename: PS-DDR.SchDoc		



Title: TE0782 - FPGA MGT		
A4	Number: TE0782 92133FA	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page9 of 31
Filename: FPGA-MGT.SchDoc		



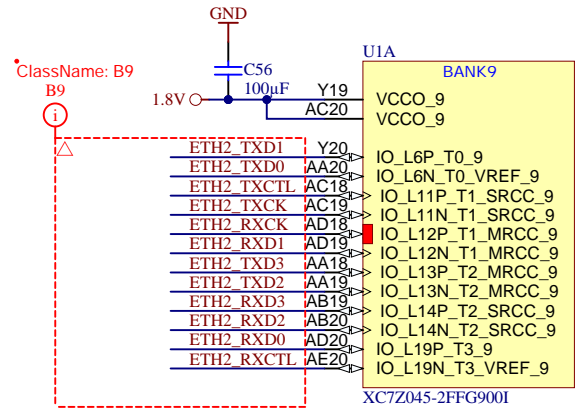
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 ⓘ ClassName: B500
- SPI_CS
 - SPI_DQ0/MIO2
 - SPI_DQ1/MIO3
 - SPI_DQ2/MIO4
 - SPI_DQ3/MIO5
 - SPI_SCK/MIO6
 - MMC-D0
 - MMC-CMD
 - MMC-CCLK
 - MMC-D1
 - MMC-D2
 - MMC-D3

- SPIFLASH**
 ⓘ
- SPI_SCK
 - SPI_CS
 - SPI_DQ0/MIO2
 - SPI_DQ1/MIO3
 - SPI_DQ2/MIO4
 - SPI_DQ3/MIO5
 - SPI_SCK/MIO6

- U38B**
- A2 NC
 - A3 NC
 - A4 NC
 - A5 NC
 - B1 NC
 - B5 NC
 - C1 NC
 - C3 NC
 - C5 NC
 - D1 NC
 - D5 NC
 - E1 NC
 - E2 NC
 - E3 NC
 - E4 NC
 - E5 NC



Title: TE0782 - FPGA MIO Banks		
A4	Number: TE0782 92133FA	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 10 of 31
Filename: MIO-BANKS.SchDoc		



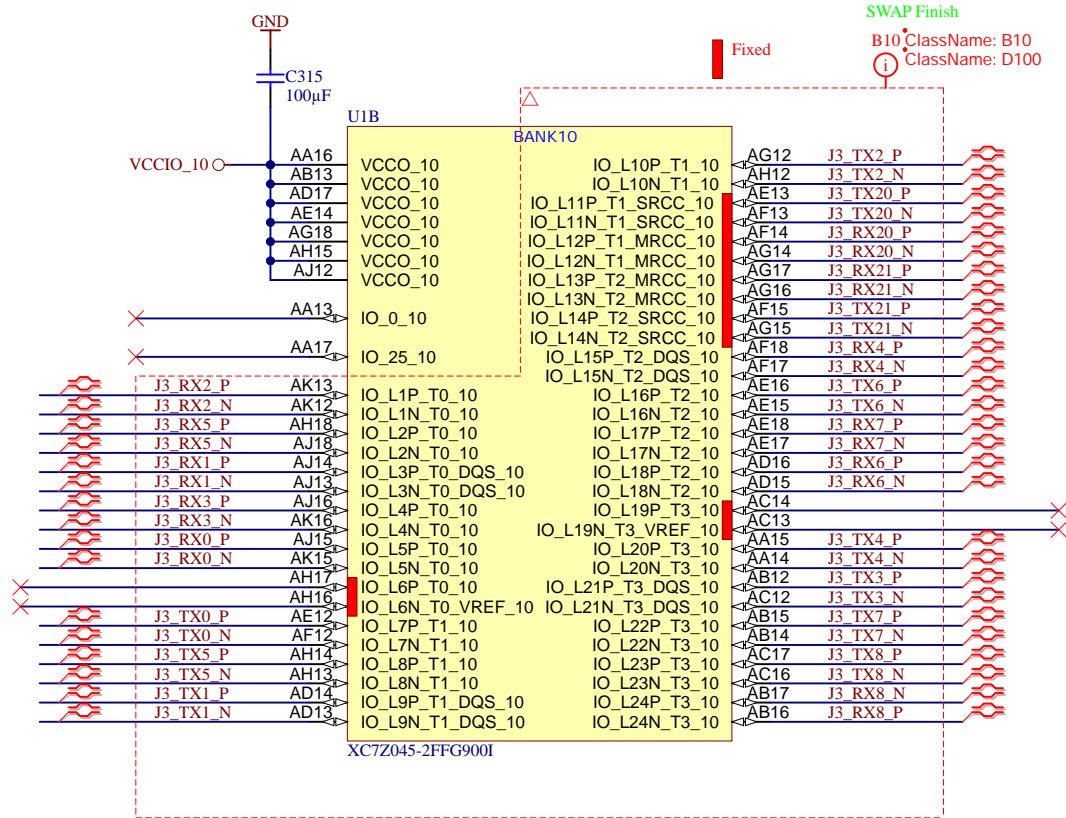
RXCK Fix to MRCC

Fixed

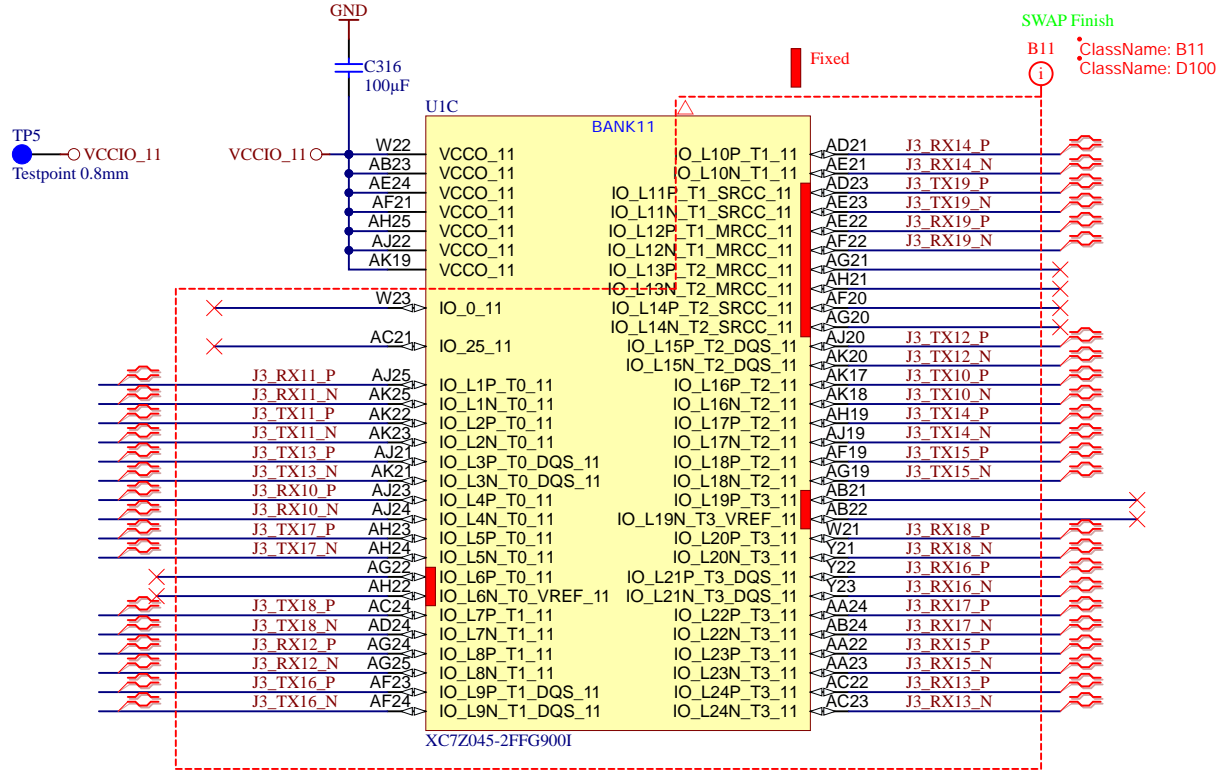



Title: TE0782 - FPGA B9		
A4	Number: TE0782 92I33FA	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 11 of 31
Filename: B9.SchDoc		


TP4
 ● ○ VCCIO_10
 Testpoint 0.8mm

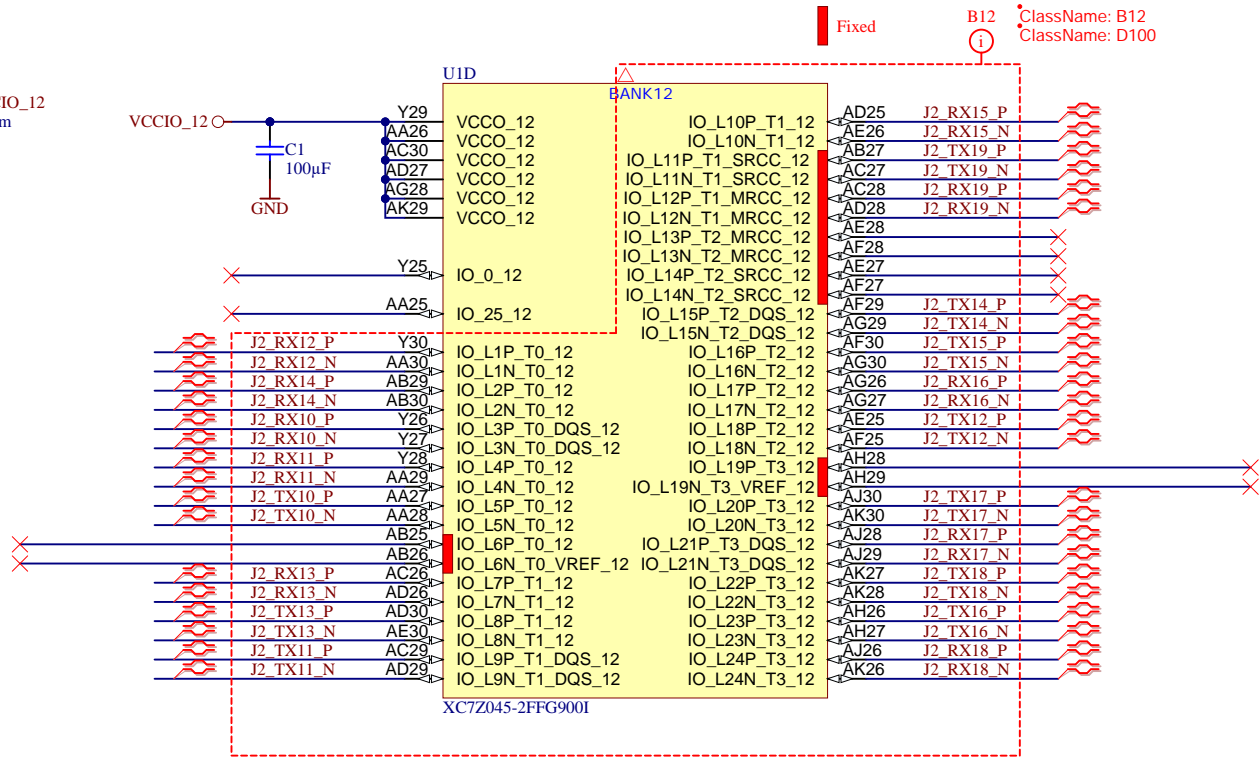


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Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 12 of 31
Filename: B10.SchDoc		




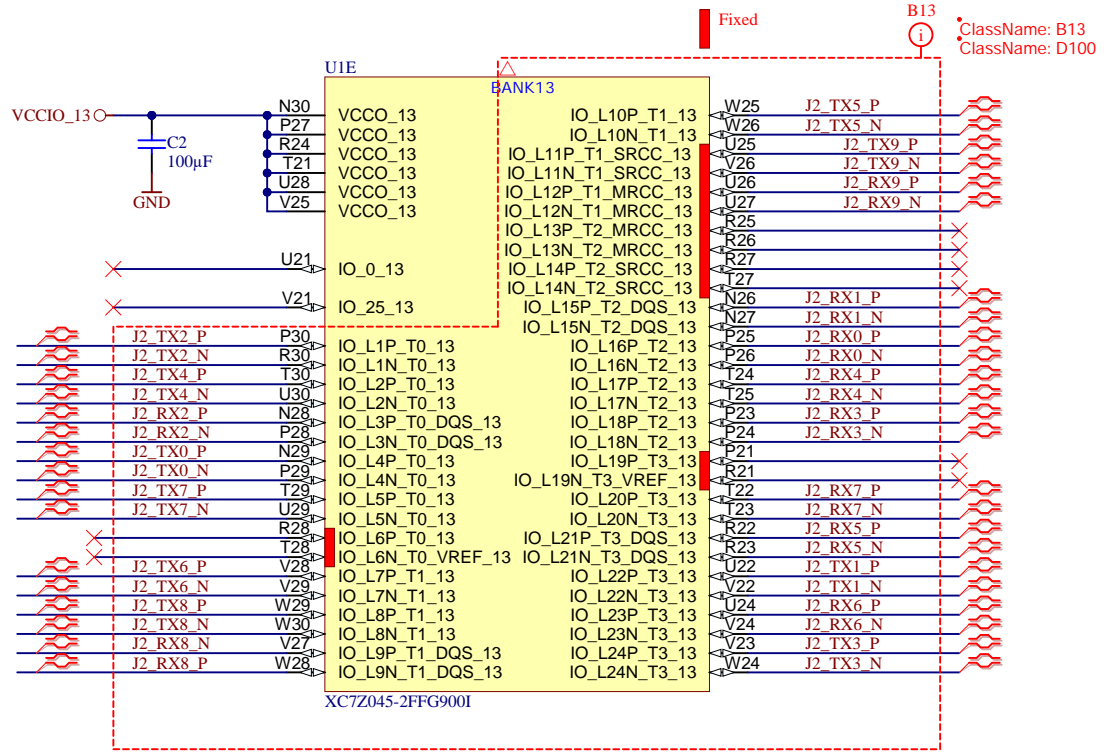
			Title: TE0782 - FPGA B11	
			A4	Number: TE0782 92I33FA
Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page13 of 31
Filename: B11.SchDoc				


TP1
 VCCIO_12
 Testpoint 0.8mm



Title: TE0782 - FPGA B12		
A4	Number: TE0782 92I33FA	Rev. 02
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Filename: B12.SchDoc		

TP2
 VCCIO_13
 Testpoint 0.8mm



	Title: TE0782 - FPGA B13		
	A4	Number: TE0782 92I33FA	Rev. 02
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	Filename: B13.SchDoc		

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U_B33
B33.SchDoc



U_B34
B34.SchDoc



U_B35
B35.SchDoc



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			Title: TES0782 - FPGA HP Banks		
			A4	Number: TE0782 92I33FA	Rev. 02
Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page 16 of 31	
Filename: HP-BANKS.SchDoc					

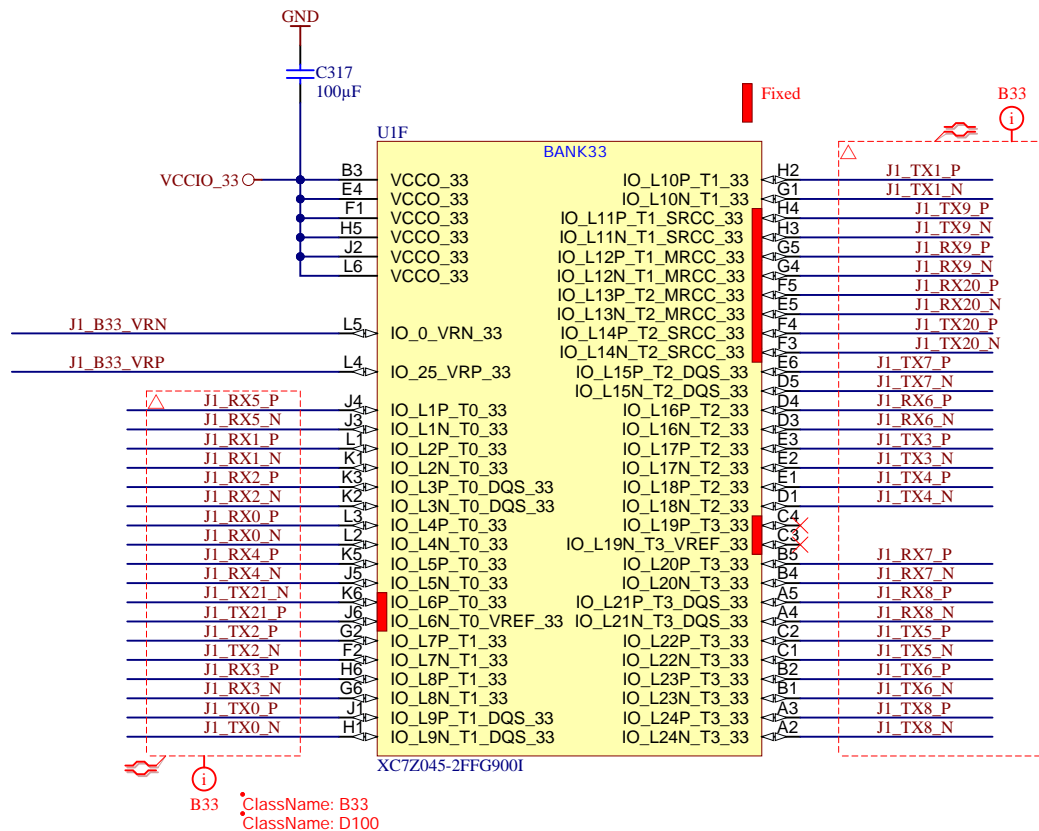
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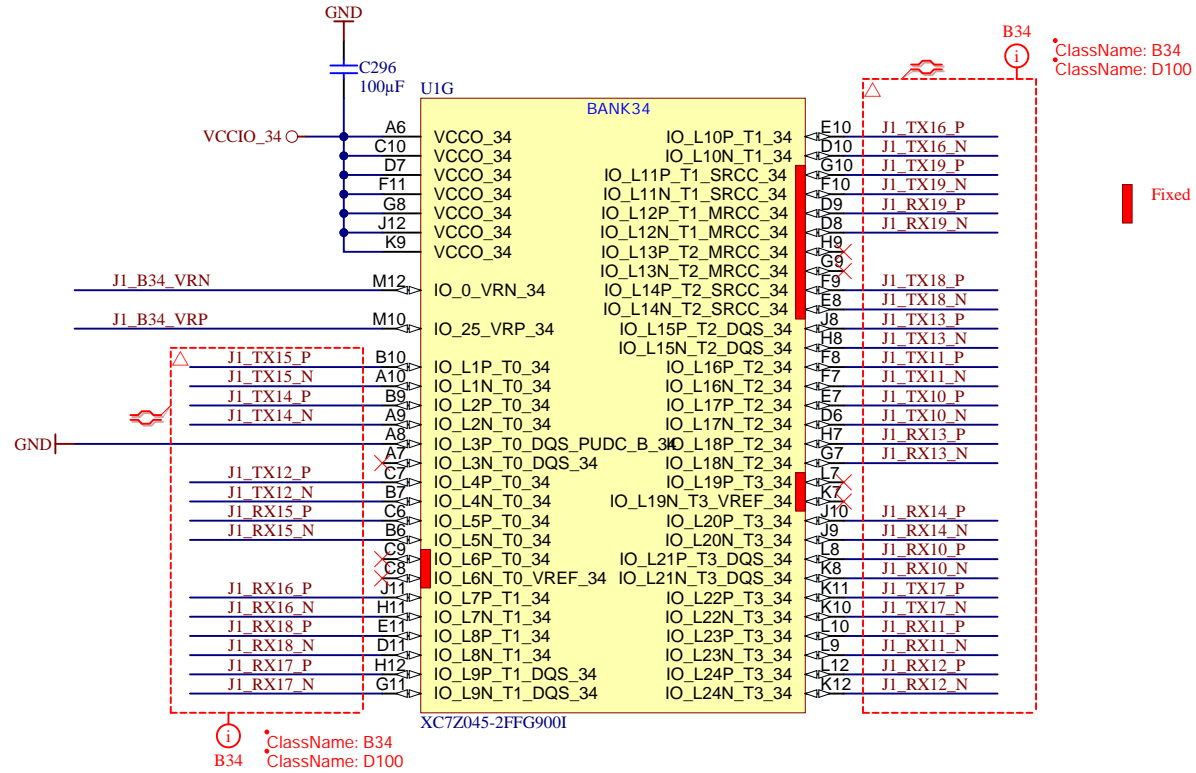
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TP6
 VCCIO_33
 Testpoint 0.8mm

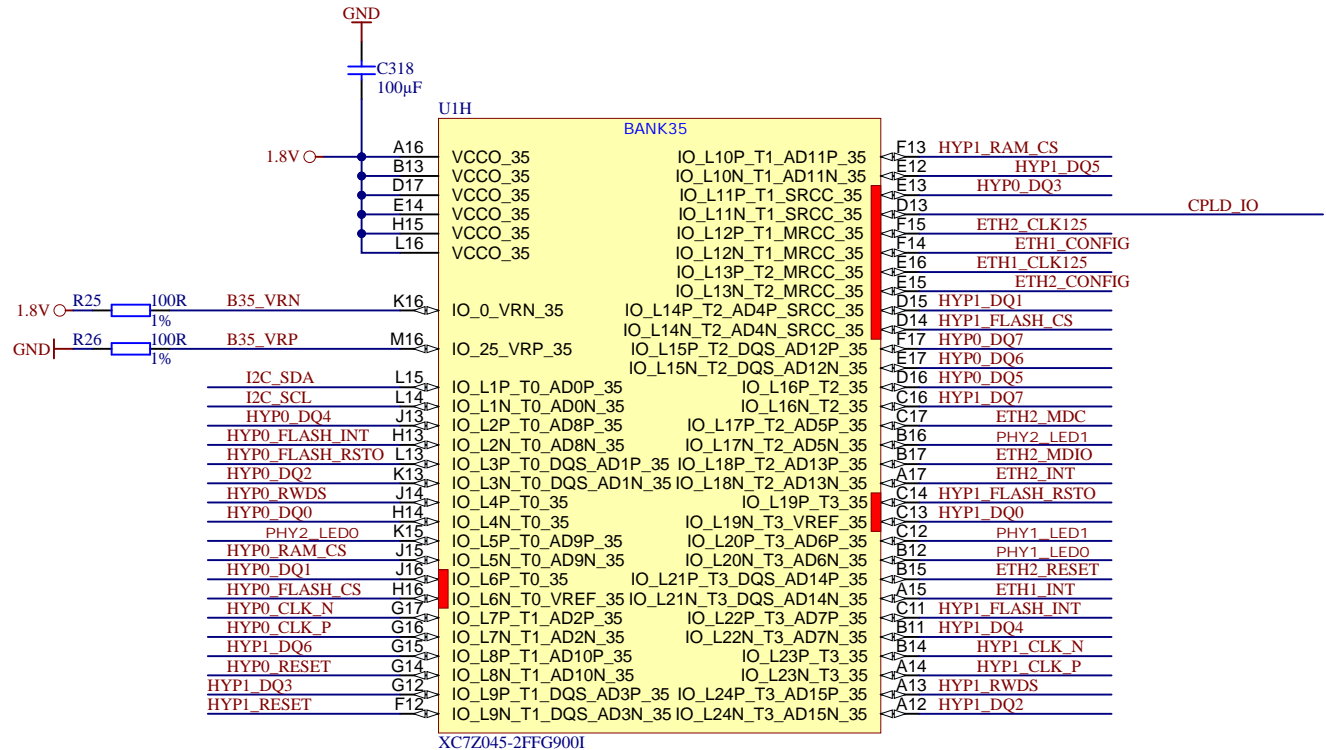


	Title: TE0782 - FPGA B33		
	A4	Number: TE0782 92I33FA	Rev. 02
	Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 17 of 31
	Filename: B33.SchDoc		

TP3
 VCCIO_34
 Testpoint 0.8mm



Title: TE0782 - FPGA B34		
A4	Number: TE0782 92I33FA	Rev. 02
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Filename: B34.SchDoc		

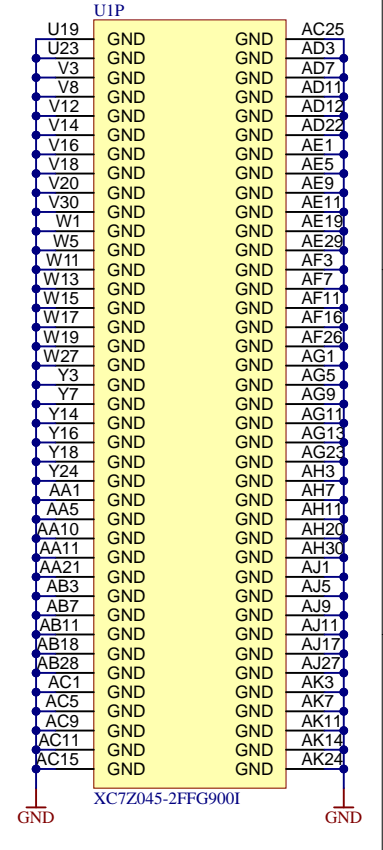
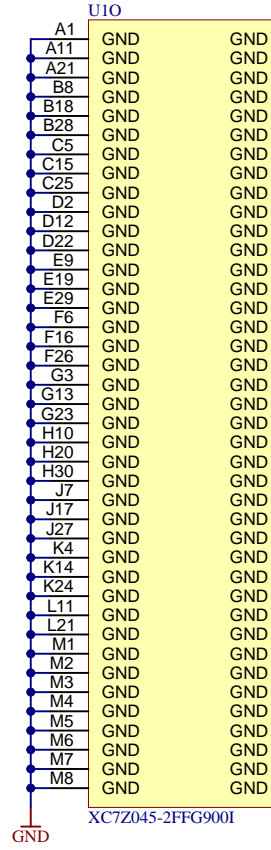
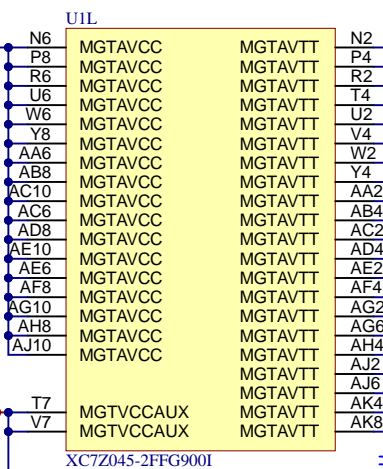
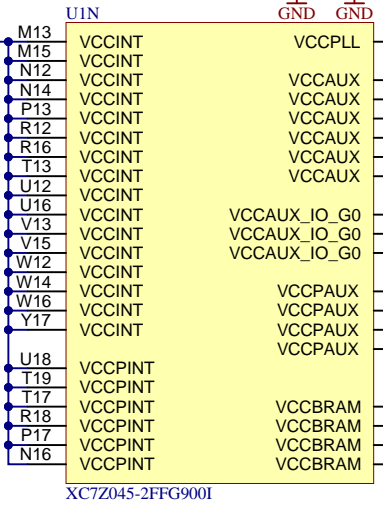
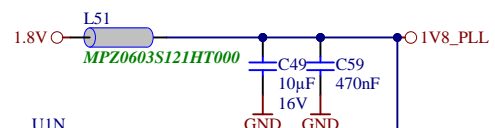
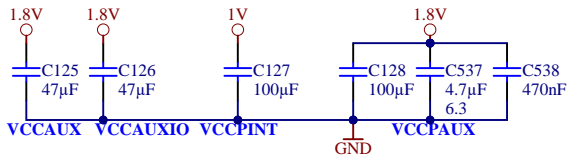
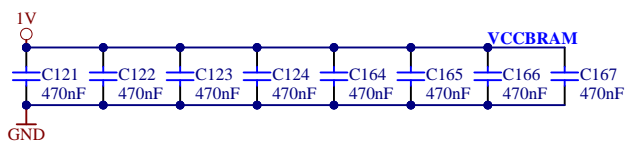
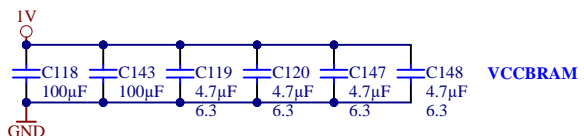
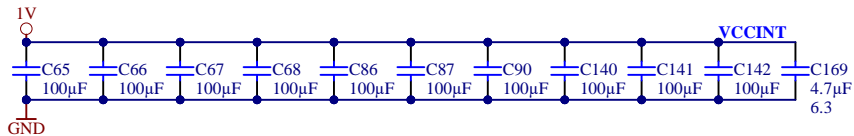
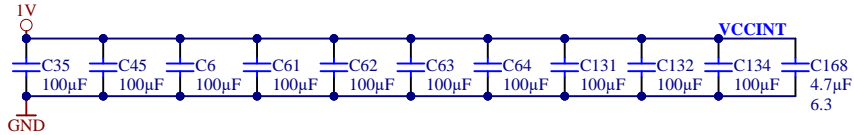


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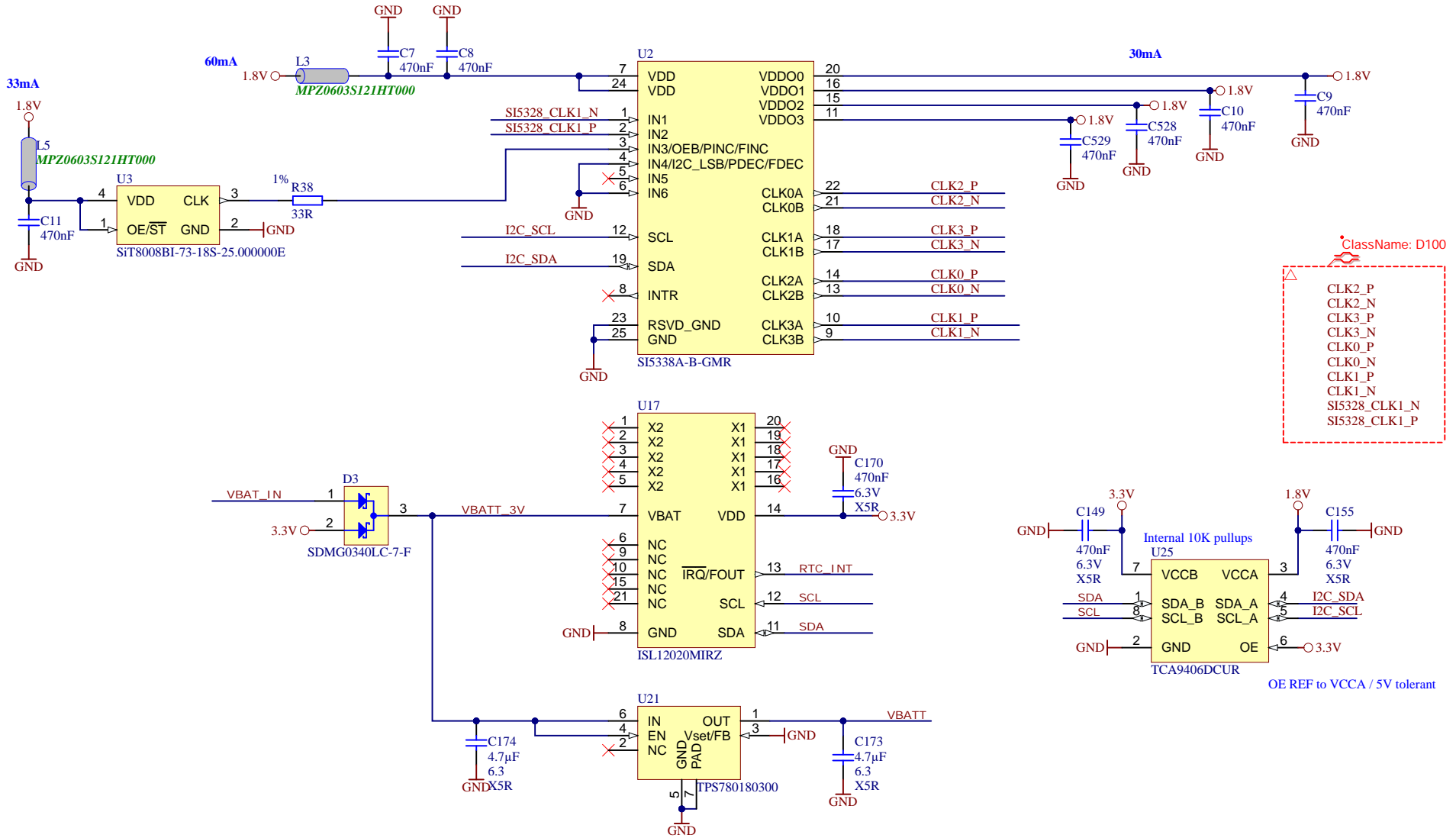


Title: TE0782 - FPGA B35		
A4	Number: TE0782 92I33FA	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 19 of 31
Filename: B35.SchDoc		

Capacitors suitable for XC7Z100



Title: TE0782 - ZYNQ POWER		
A4	Number: TE0782 92I33FA	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	
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Filename: FPGA-PWR.SchDoc		



Title: TE0782 - Clock		
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Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 21 of 31
Filename: Clock.SchDoc		

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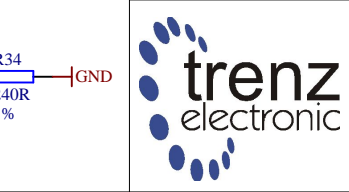
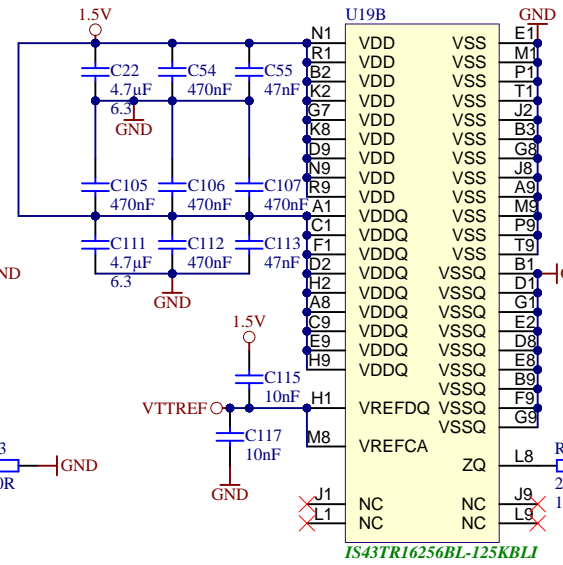
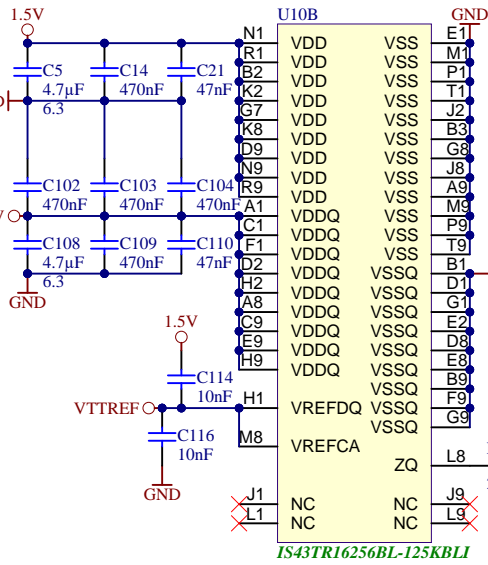
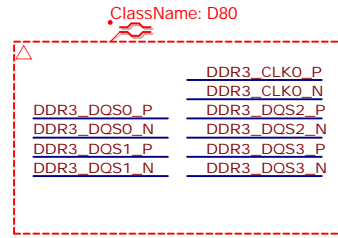
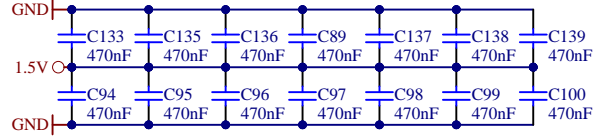
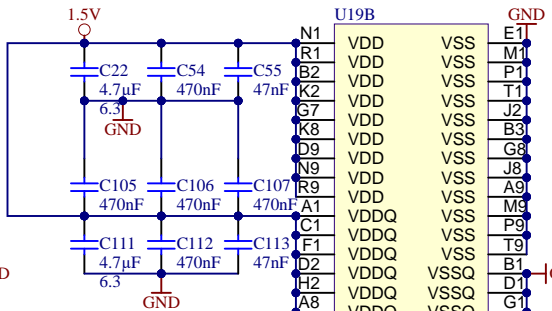
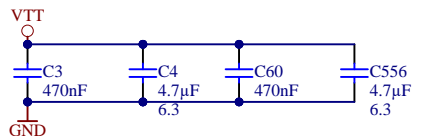
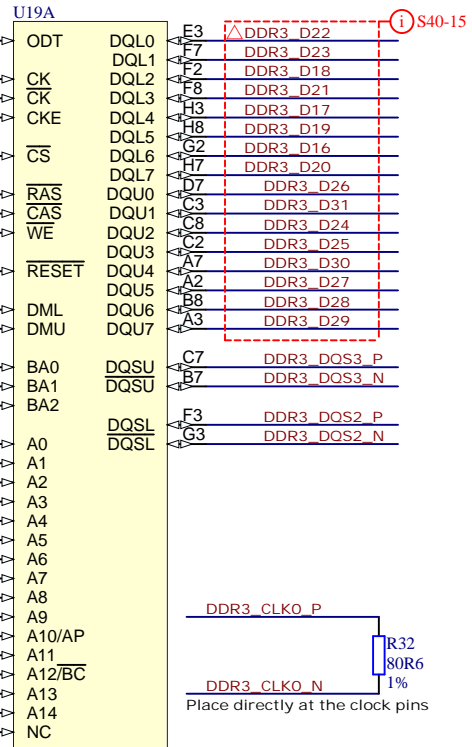
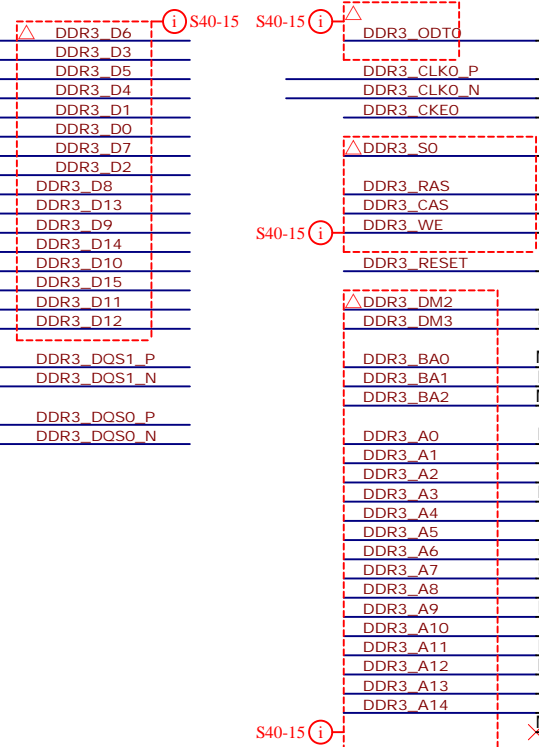
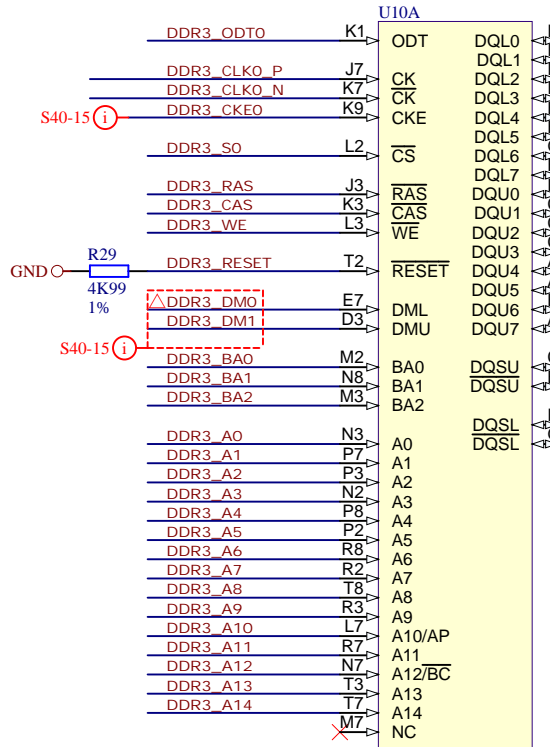
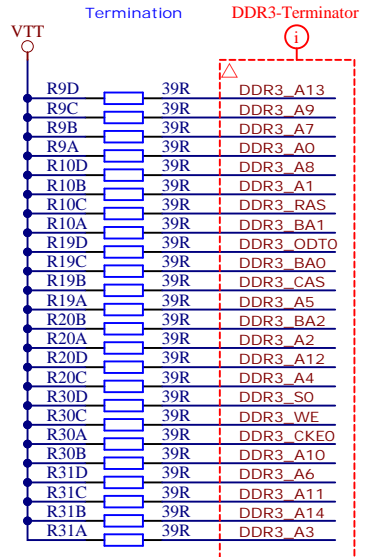
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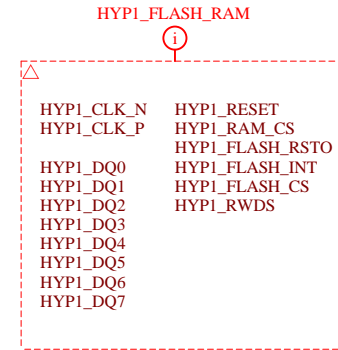
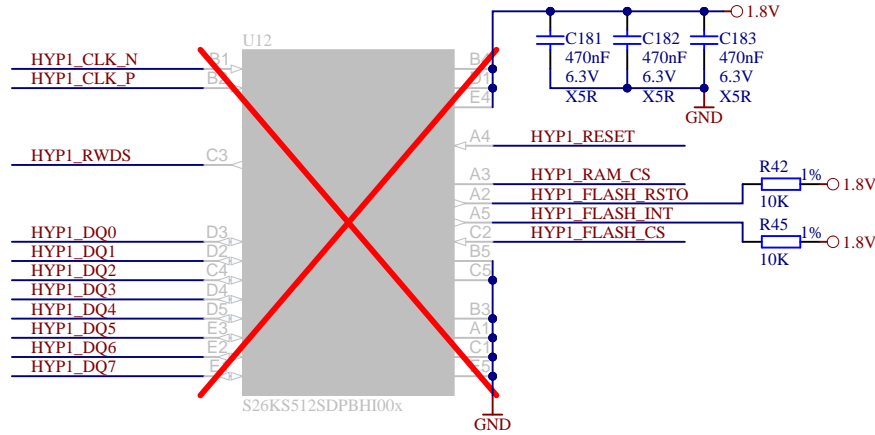
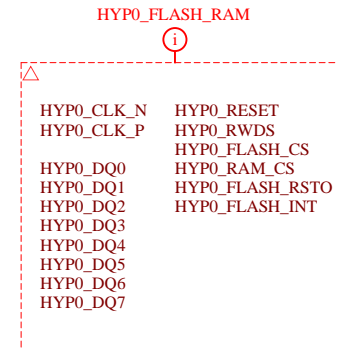
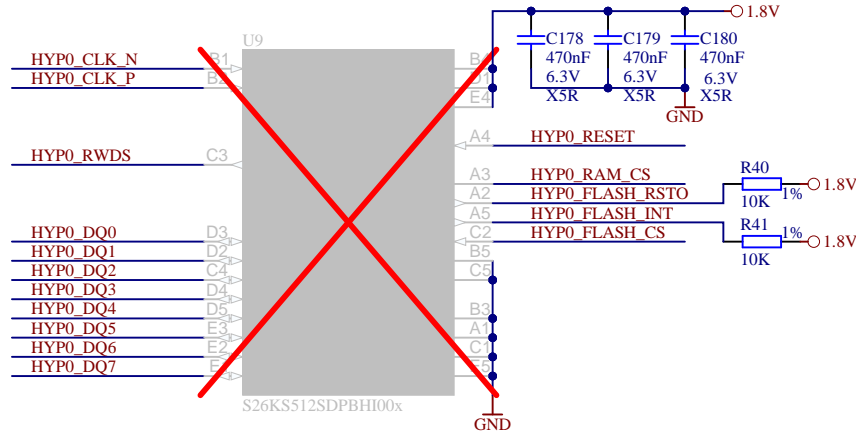
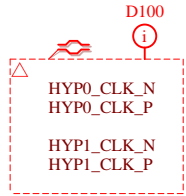
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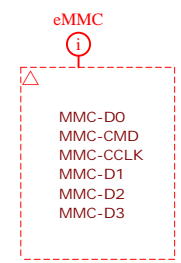
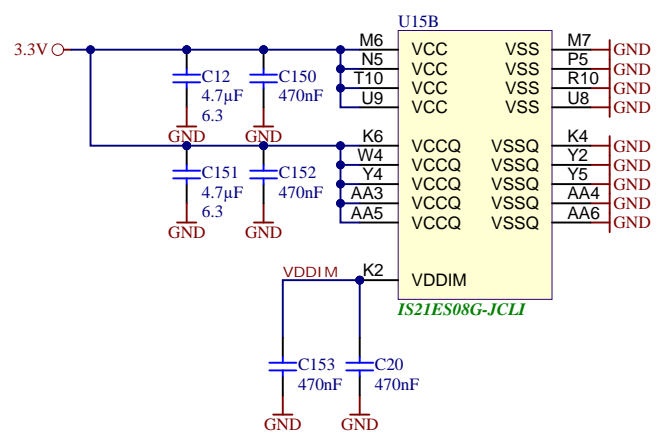
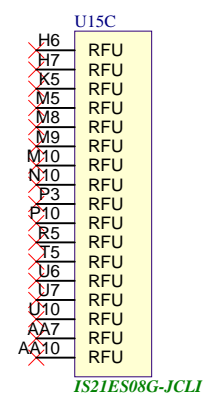
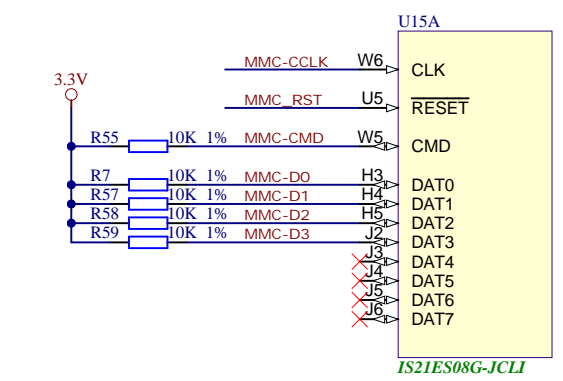
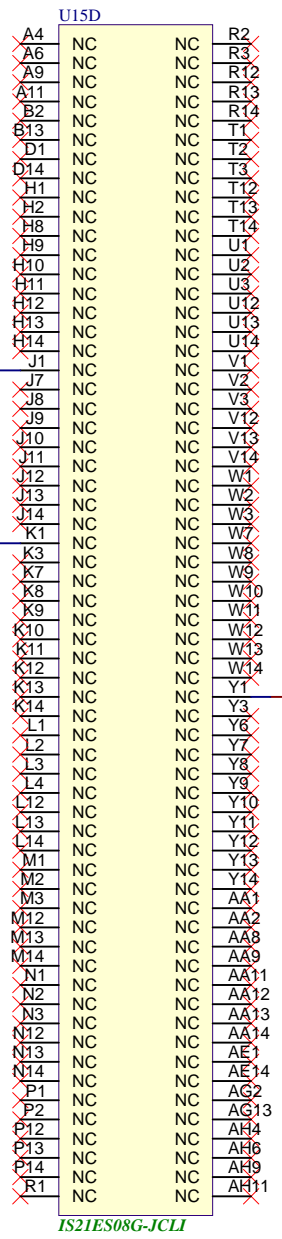


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Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 22 of 31
Filename: DDR3-RAM.SchDoc		

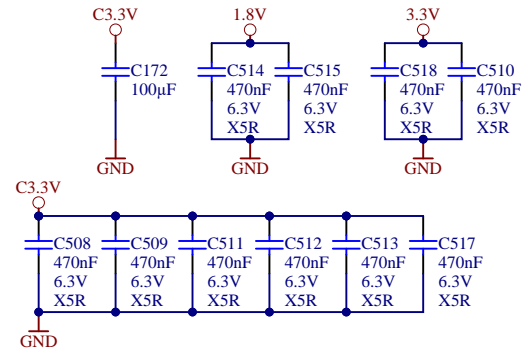
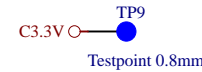
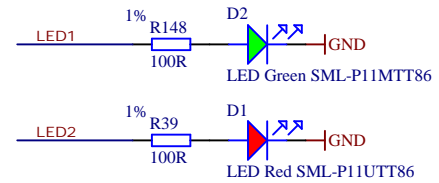
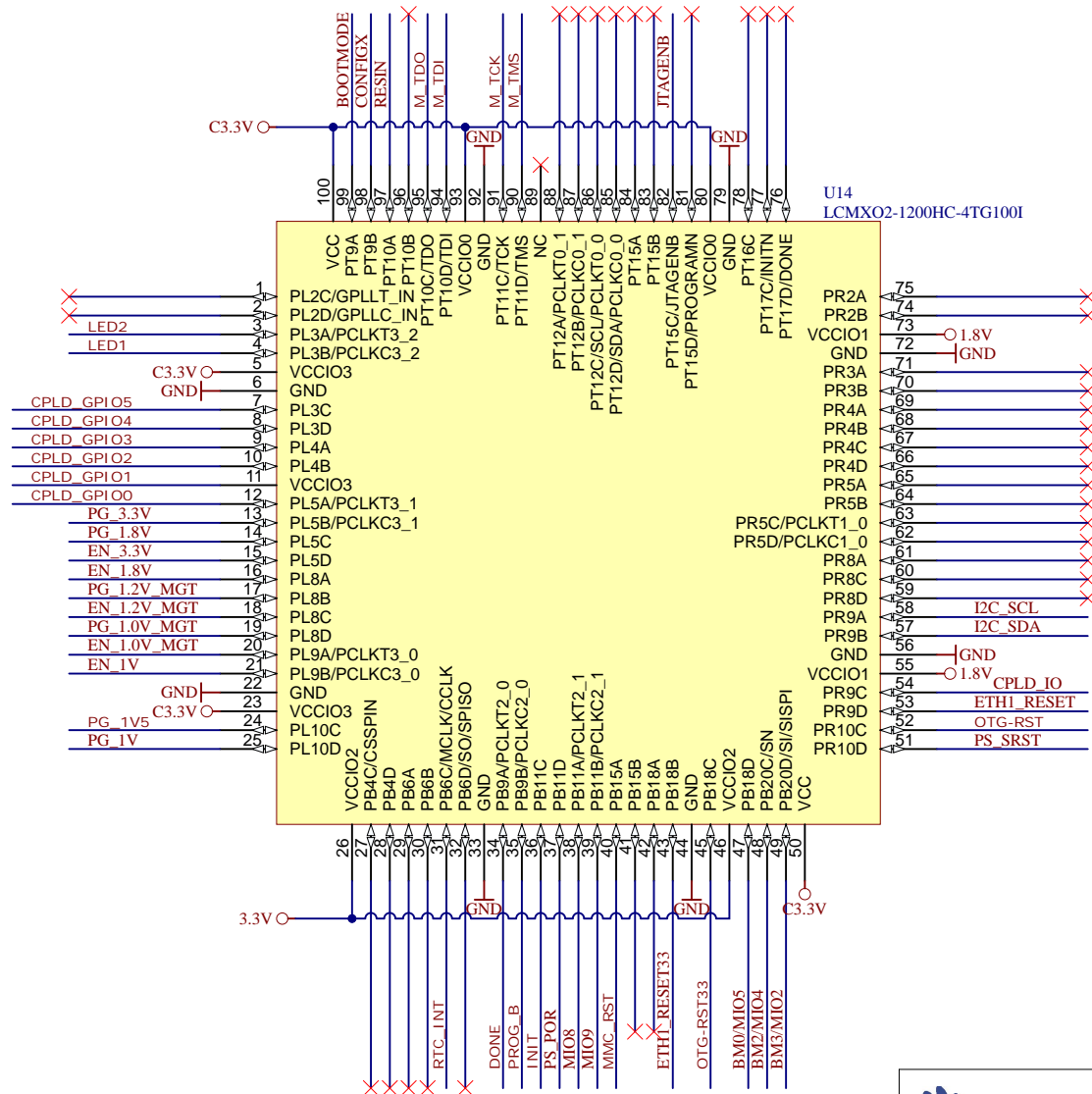


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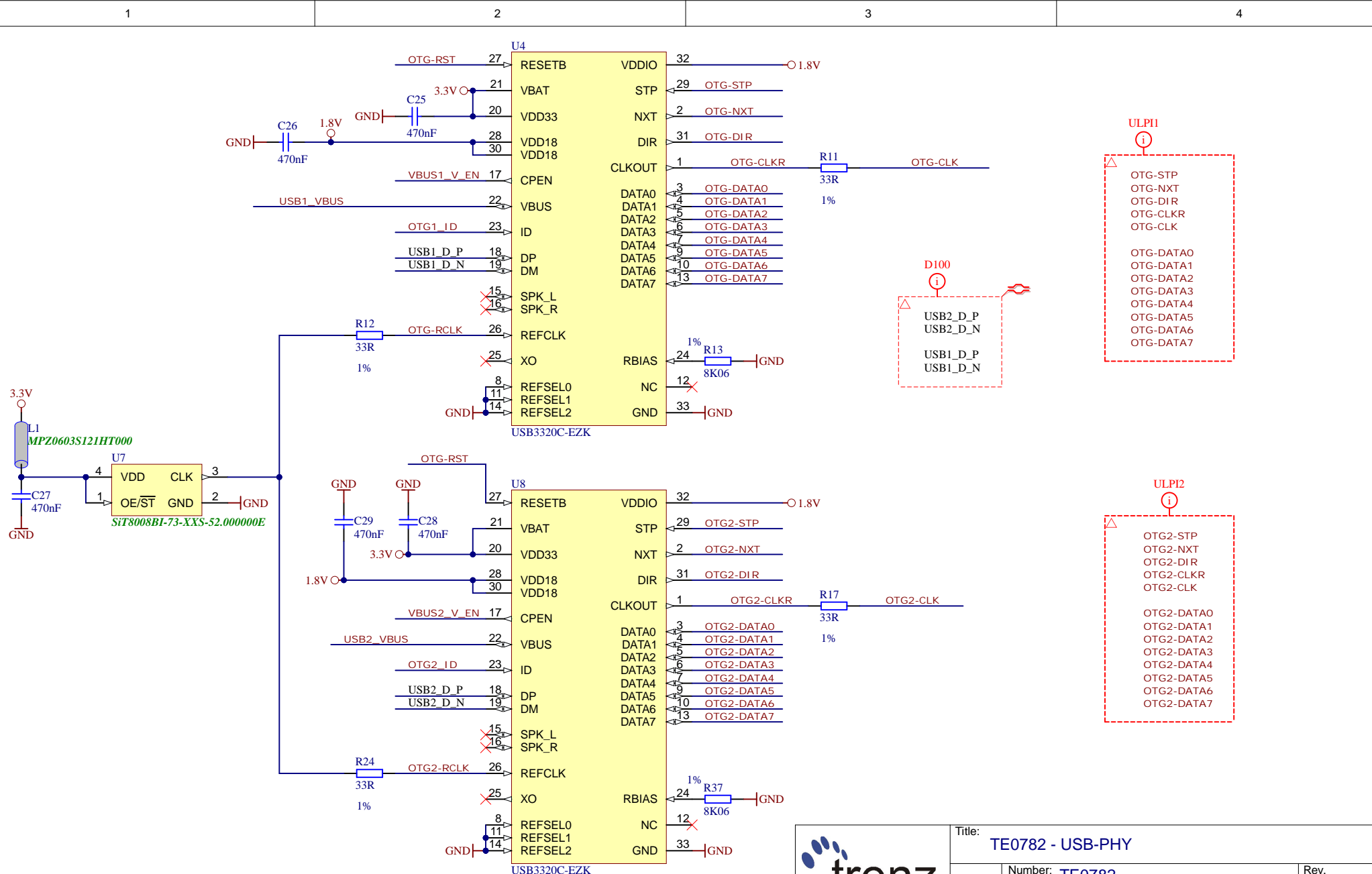
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Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page23 of 31
Filename: HyperFlash_RAM.SchDoc		




Title: TE0782 - eMMC		
A4	Number: TE0782 92133FA	Rev. 02
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Filename: eMMC.SchDoc		



Title: TE0782 - CPLD		
A4	Number: TE0782 92133FA	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	
Filename: CPLD.SchDoc		Page 25 of 31



			Title: TE0782 - USB-PHY	
			A4	Number: TE0782 92I33FA
Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page 26 of 31
Filename: USB-PHY.SchDoc				

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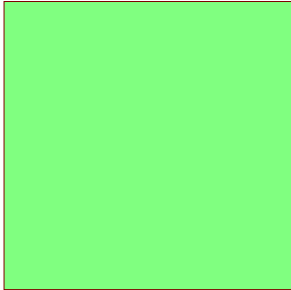
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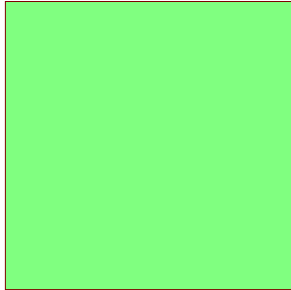
D

D

U_ETH1
ETH1.SchDoc



U_ETH2
ETH2.SchDoc



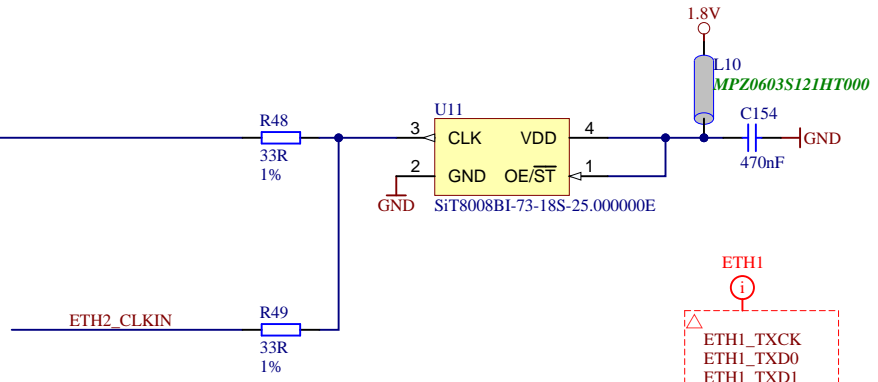
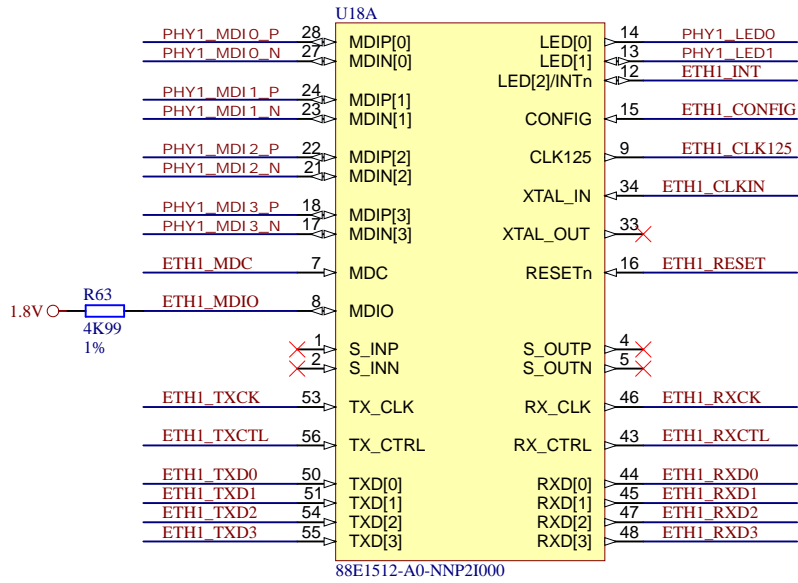
Title: TE0782 - Ethernet		
A4	Number: TE0782 92I33FA	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 27 of 31
Filename: Ethernet.SchDoc		

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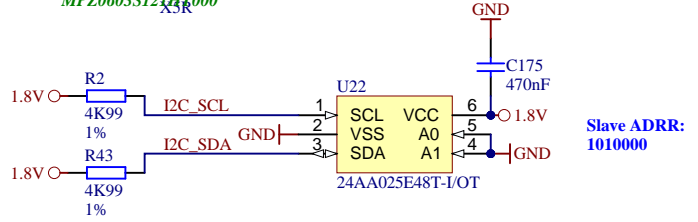
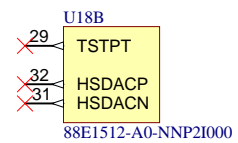
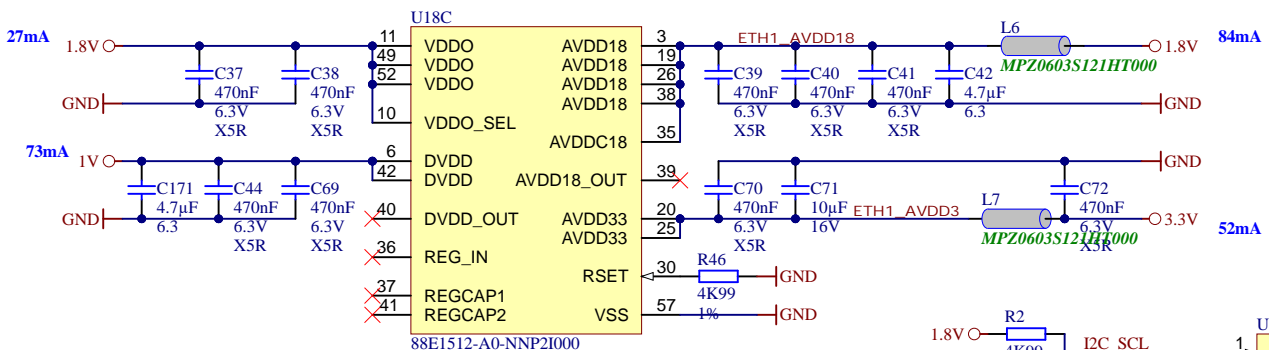
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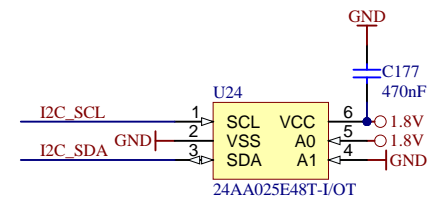
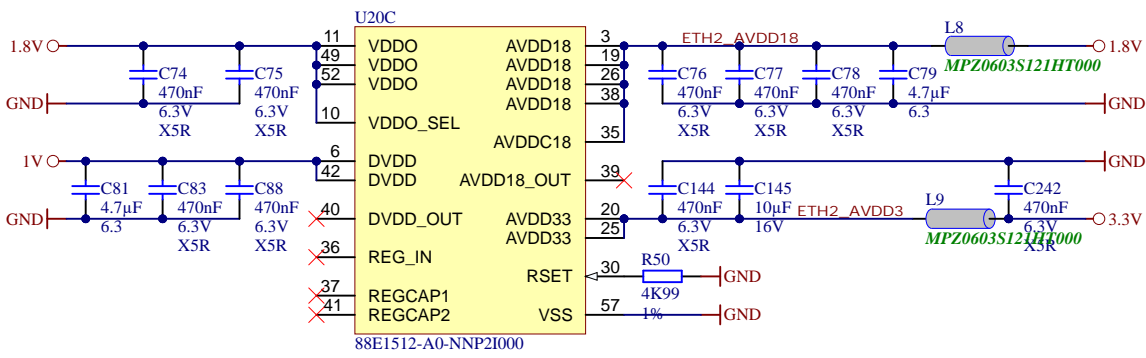
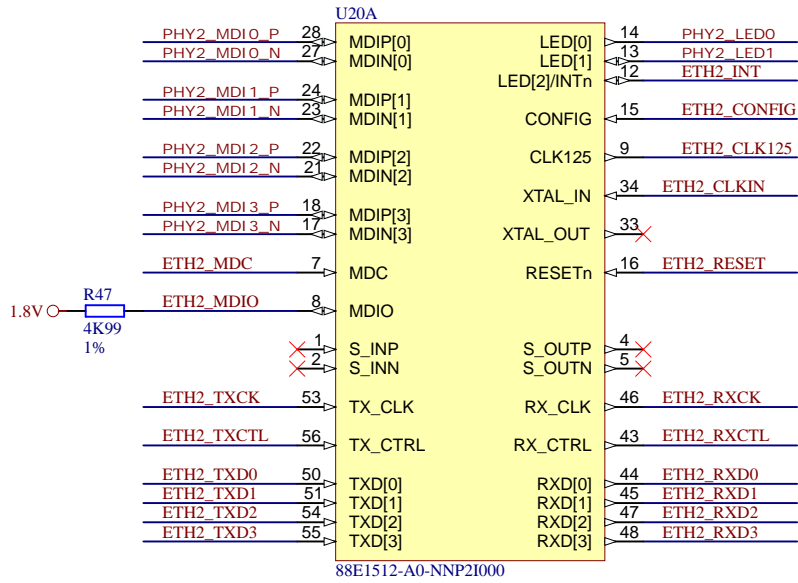
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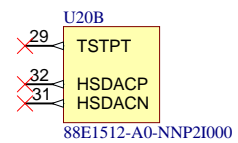
- ETH1**
- ETH1_TXCK
 - ETH1_TXD0
 - ETH1_TXD1
 - ETH1_TXD2
 - ETH1_TXD3
 - ETH1_TXCTL
 - ETH1_RXCK
 - ETH1_RXD0
 - ETH1_RXD1
 - ETH1_RXD2
 - ETH1_RXD3
 - ETH1_RXCTL
 - ETH1_MDC
 - ETH1_MDIO
- PHY1_LED0
PHY1_LED1
ETH1_INT
ETH1_CONFIG
ETH1_CLK125
ETH1_RESET



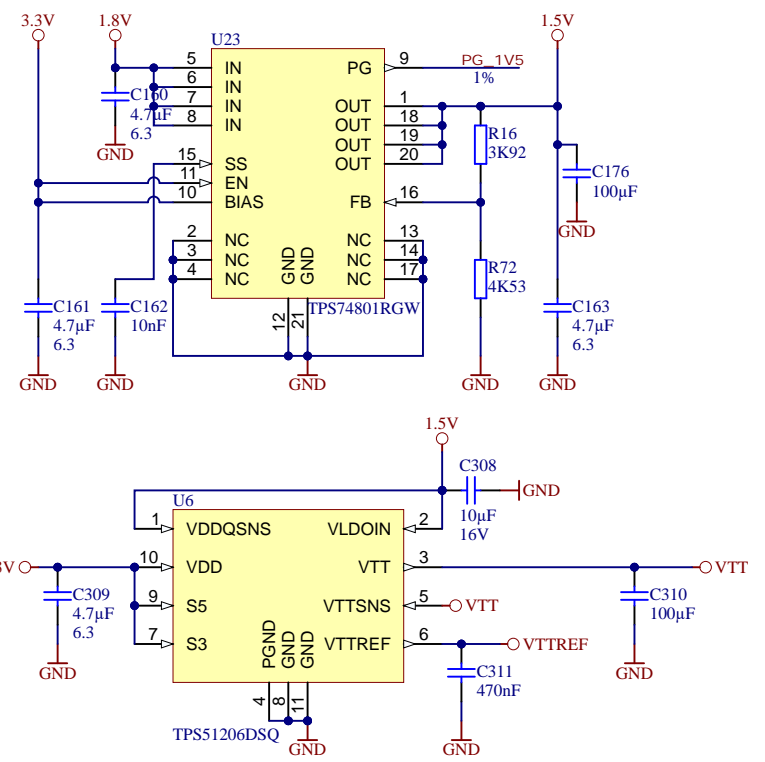
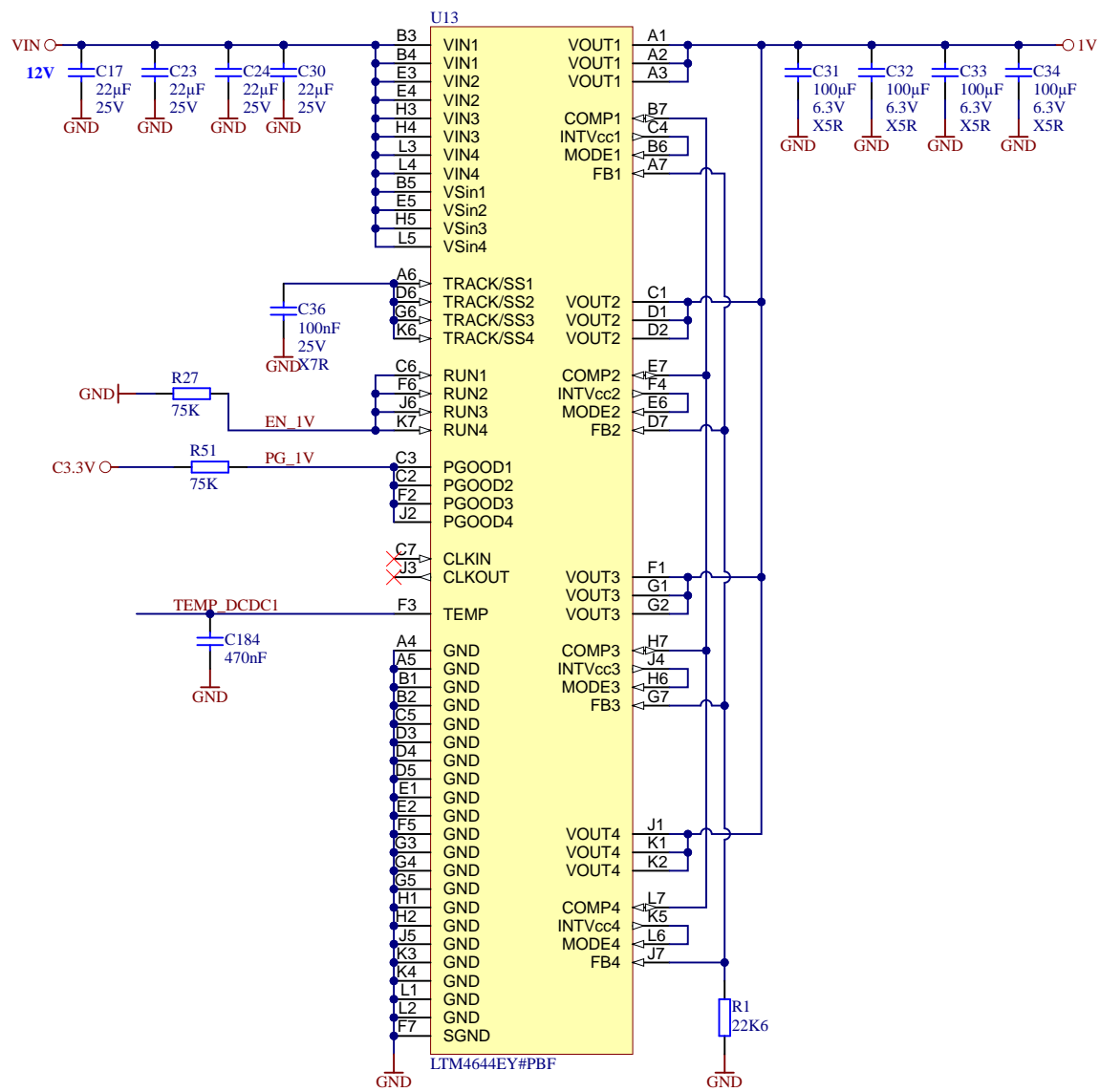
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Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page 28 of 31
Filename: ETH1.SchDoc				




Slave ADDR:
1010001

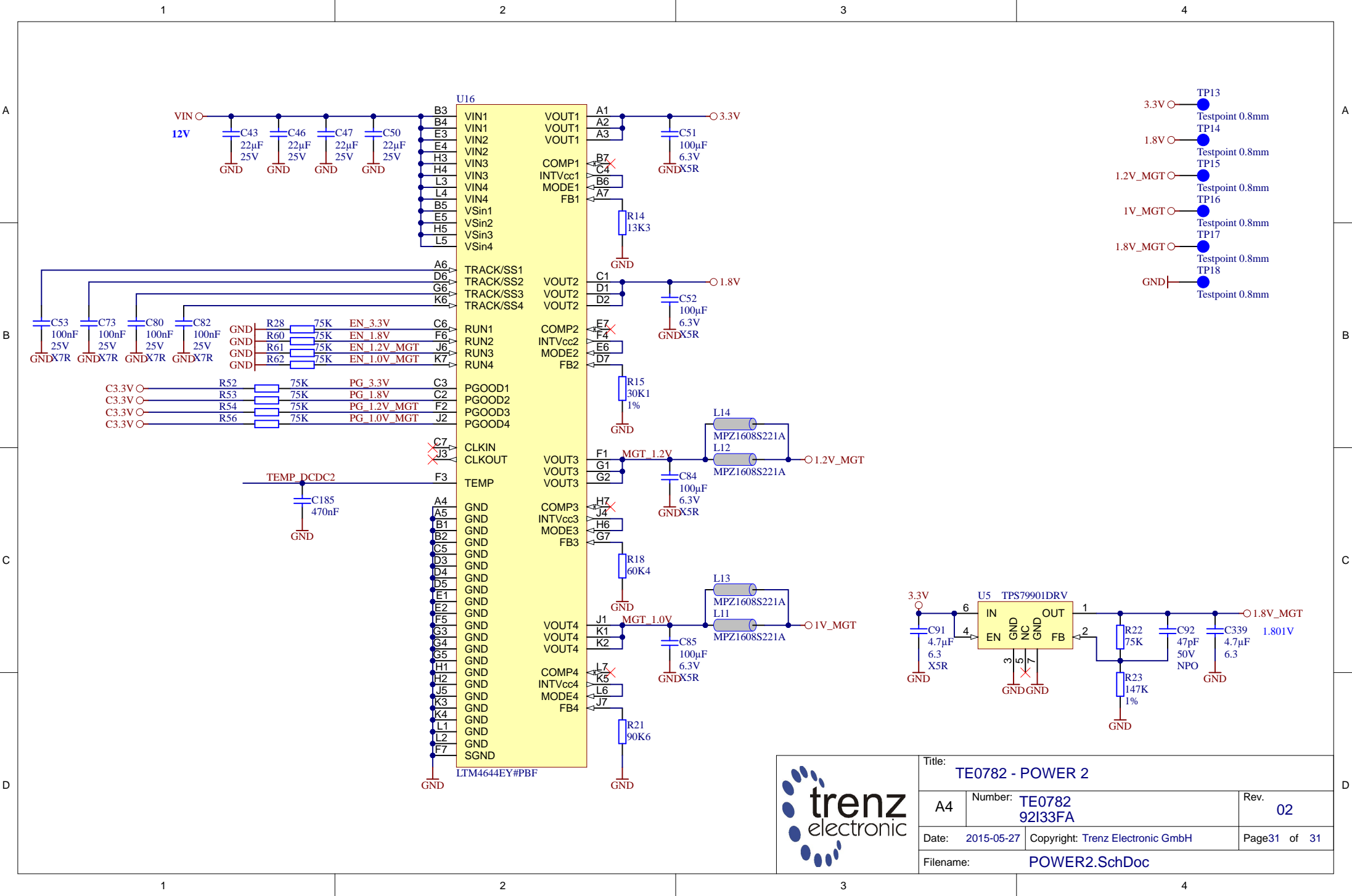



	Title: TE0782 - ETH_PHY2		
	A4	Number: TE0782 92133FA	Rev. 02
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	Filename: ETH2.SchDoc		



- TP7 1V Testpoint 0.8mm
- TP8 GND Testpoint 0.8mm
- TP10 1.5V Testpoint 0.8mm
- TP11 VTT Testpoint 0.8mm
- TP12 VTTREF0 Testpoint 0.8mm

			Title: TE0782 - POWER	
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		Title: TE0782 - POWER 2	
		A4	Number: TE0782 92133FA
Date: 2015-05-27		Copyright: Trenz Electronic GmbH	
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Filename: POWER2.SchDoc			