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U_DDR3-RAM
DDR3-RAM.SchDoc

U_USB-PHY
USB-PHY.SchDoc

U_ETH1
ETH1.SchDoc

U_SOC
SOC.SchDoc

U_CPLD
CPLD.SchDoc

U_POWER2
POWER2.SchDoc

U_Clock
Clock.SchDoc

U_eMMC
eMMC.SchDoc

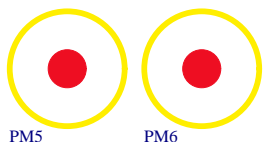
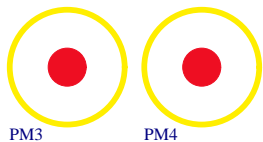
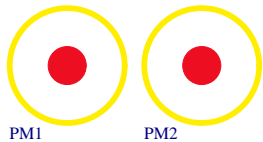
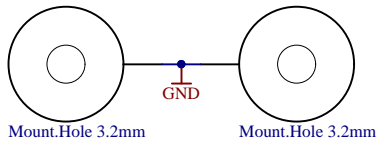
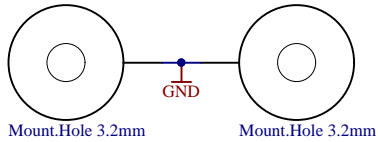
U_Connectors
Connectors.SchDoc

U_POWER
POWER.SchDoc

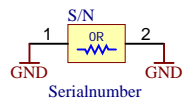
U_POWER3
POWER3.SchDoc

LOGO1
TE Logo PRINT Layer

LOGO PRINT



Serial
Serialnumber 6,3 x 6.3mm



Title: Overview		
A4	Number: TE0783 035-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page1 of 31
Filename: TE0783.SchDoc		

1

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A

A

B

B

C

C

D

D

1

2

3

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A

A

U_HSMC_CONN_J1
HSMC_CONN_J1.SchDoc



U_HSMC_CONN_J2
HSMC_CONN_J2.SchDoc



U_HSMC_CONN_J3
HSMC_CONN_J3.SchDoc



B

B

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C

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D

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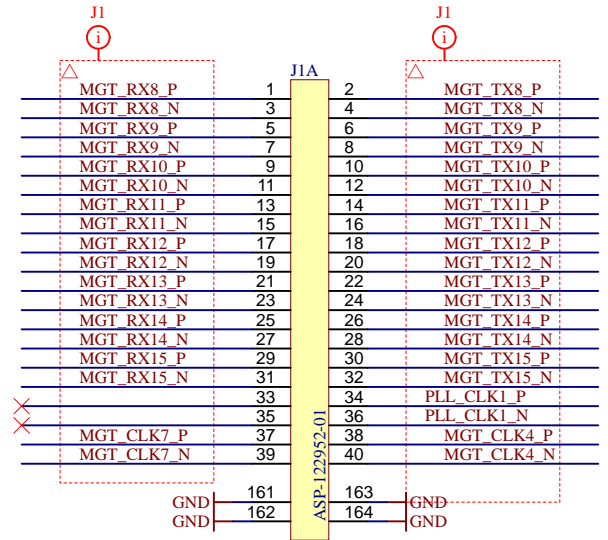
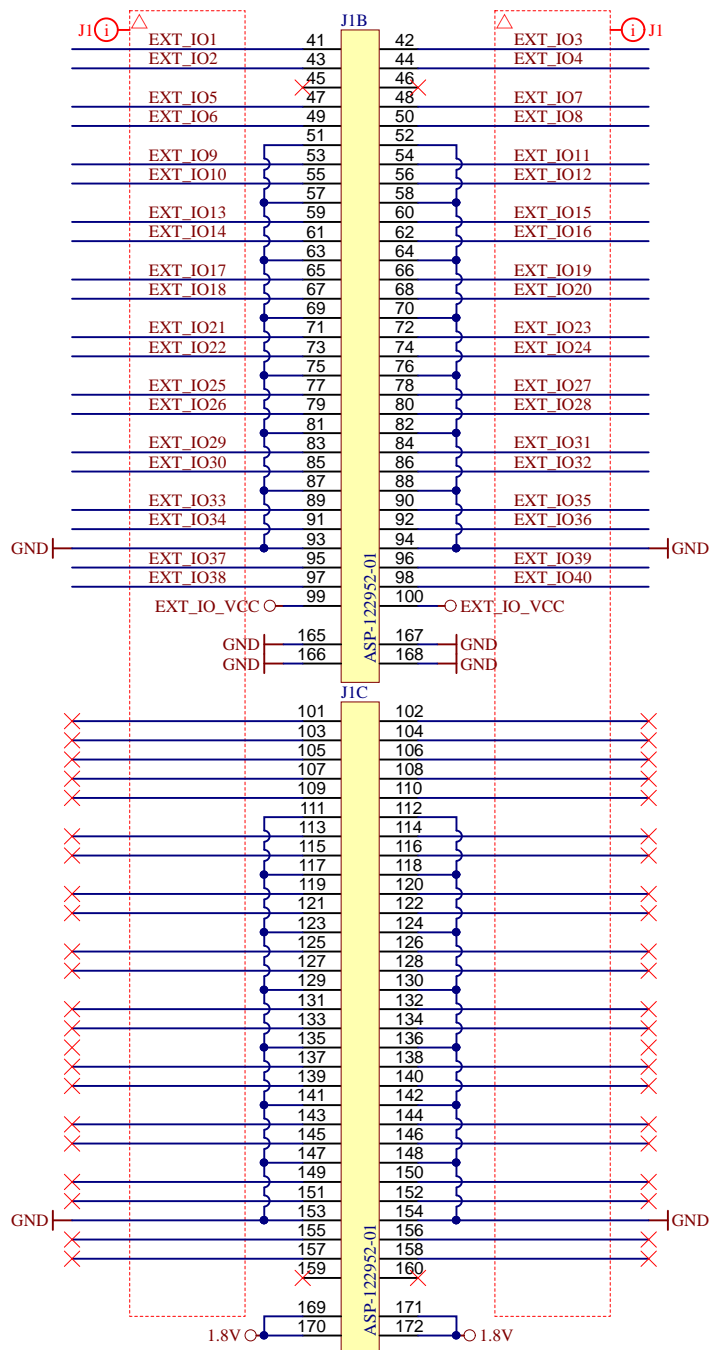
			Title: Connectors		
			A4	Number: TE0783 035-2I	Rev. 01
Date: 15.05.2018		Copyright: Trenz Electronic GmbH		Page 2 of 31	
Filename: Connectors.SchDoc					

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Next signals has different functionality in TE0782 and TEBT0782.

TE0782
J1_TX20_N
J1_TX20_P
J1_TX21_N
J1_TX21_P

Next signals has different functionality in TE0782 and TEBT0782.

TE0782
J1_RX20_N
J1_RX20_P



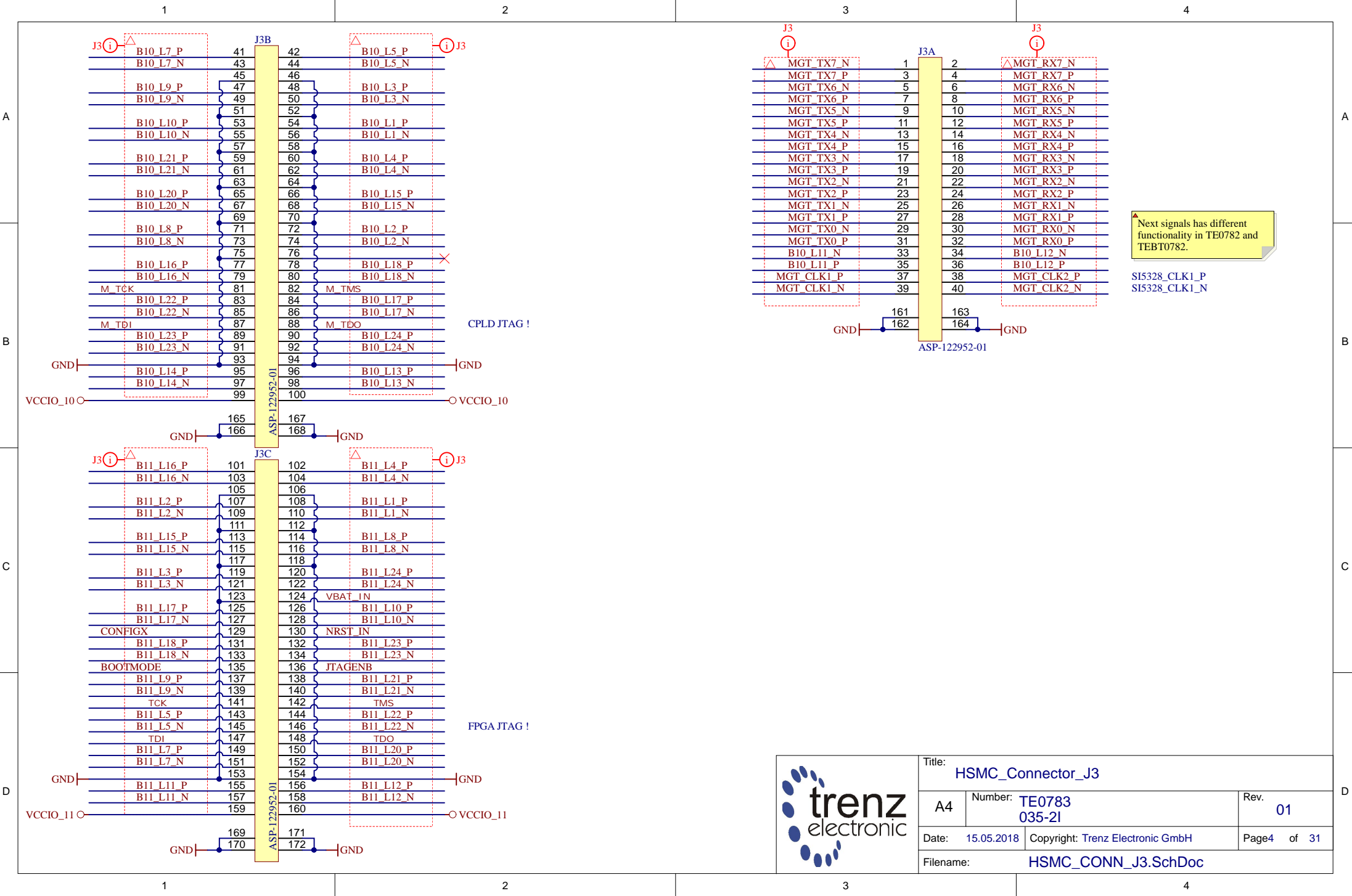
Title: HSMC_Connector_J1		
A4	Number: TE0783 035-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 3 of 31
Filename: HSMC_CONN_J1.SchDoc		

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Next signals has different functionality in TE0782 and TEBT0782.

S15328_CLK1_P
S15328_CLK1_N



Title: HSMC_Connector_J3		
A4	Number: TE0783 035-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page4 of 31
Filename: HSMC_CONN_J3.SchDoc		

A

B

C

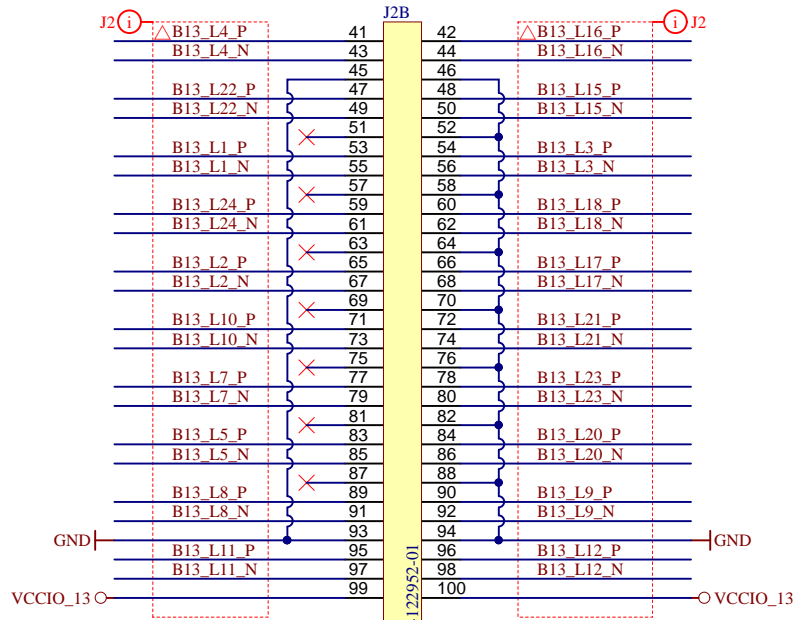
D

A

B

C

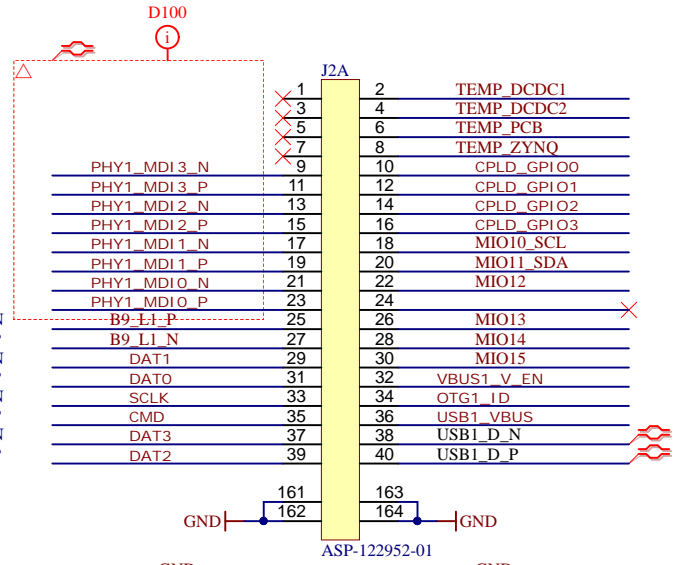
D



Next signals has different functionality in TE0782 and TEBT0782.

TE0782

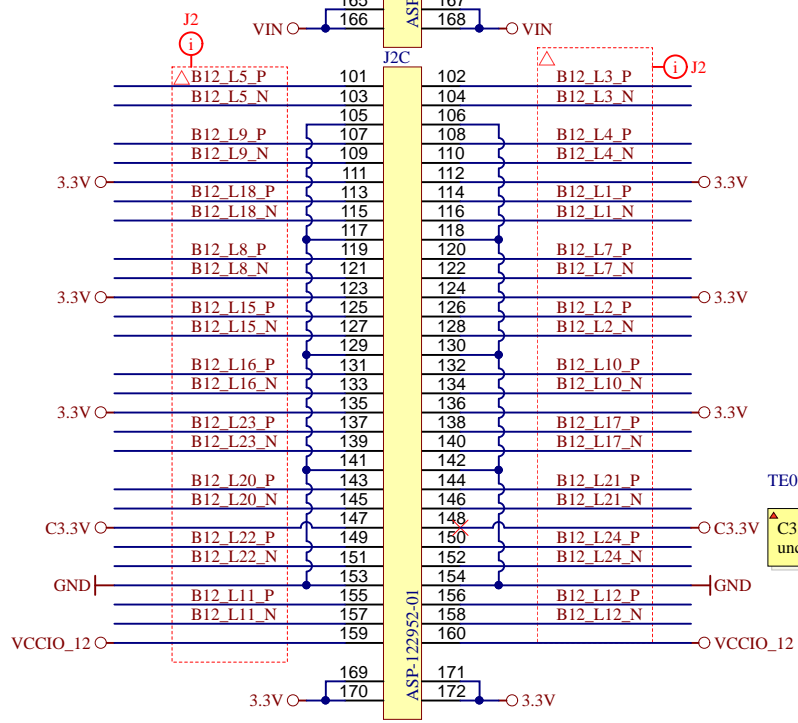
- PHY2_MDI3_N
- PHY2_MDI3_P
- PHY2_MDI2_N
- PHY2_MDI2_P
- PHY2_MDI1_N
- PHY2_MDI1_P
- PHY2_MDI0_N
- PHY2_MDI0_P



Next signals has different functionality in TE0782 and TEBT0782.

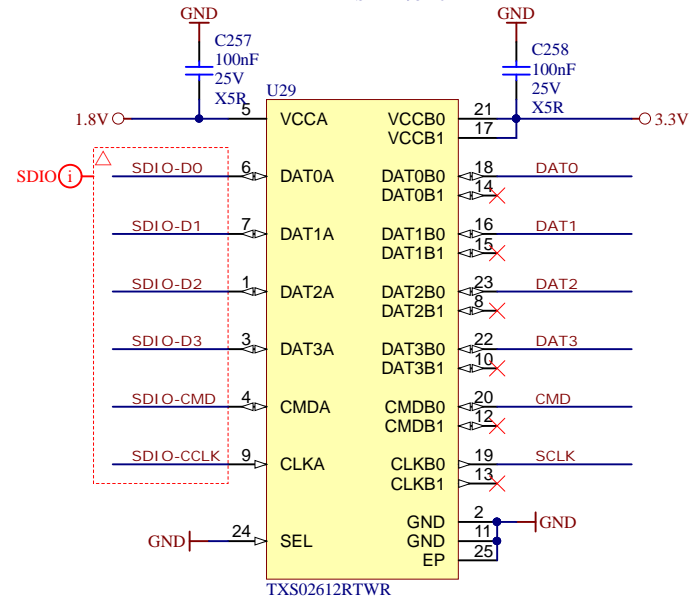
TE0782

- CPLD_GPIO4
- CPLD_GPIO5
- OTG2_ID
- USB2_VBUS
- USB2_D_N
- USB2_D_P
- VBUS2_V_EN



TE0782: External 3.3V

C3.3V: Normally leave unconnected



SDCARD

- DAT0
- DAT1
- DAT2
- DAT3
- CMD
- SCLK



Title: HSMC_Connector_J2		
A4	Number: TE0783 035-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page5 of 31
Filename: HSMC_CONN_J2.SchDoc		

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A

A

U_PS-DDR
PS-DDR.SchDoc



U_B9
B9.SchDoc



U_MIO-BANKS
MIO-BANKS.SchDoc



U_B10
B10.SchDoc



U_HP-BANKS
HP-BANKS.SchDoc



U_B11
B11.SchDoc



B

B

U_FPGA-MGT
FPGA-MGT.SchDoc



U_B12
B12.SchDoc



U_FPGA-CFG
FPGA-CFG.SchDoc



U_B13
B13.SchDoc



C

C

U_FPGA-PWR
FPGA-PWR.SchDoc



D

D



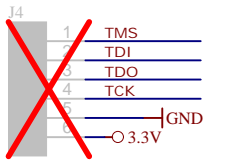
Title: SOC		
A4	Number: TE0783 035-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 6 of 31
Filename: SOC.SchDoc		

1

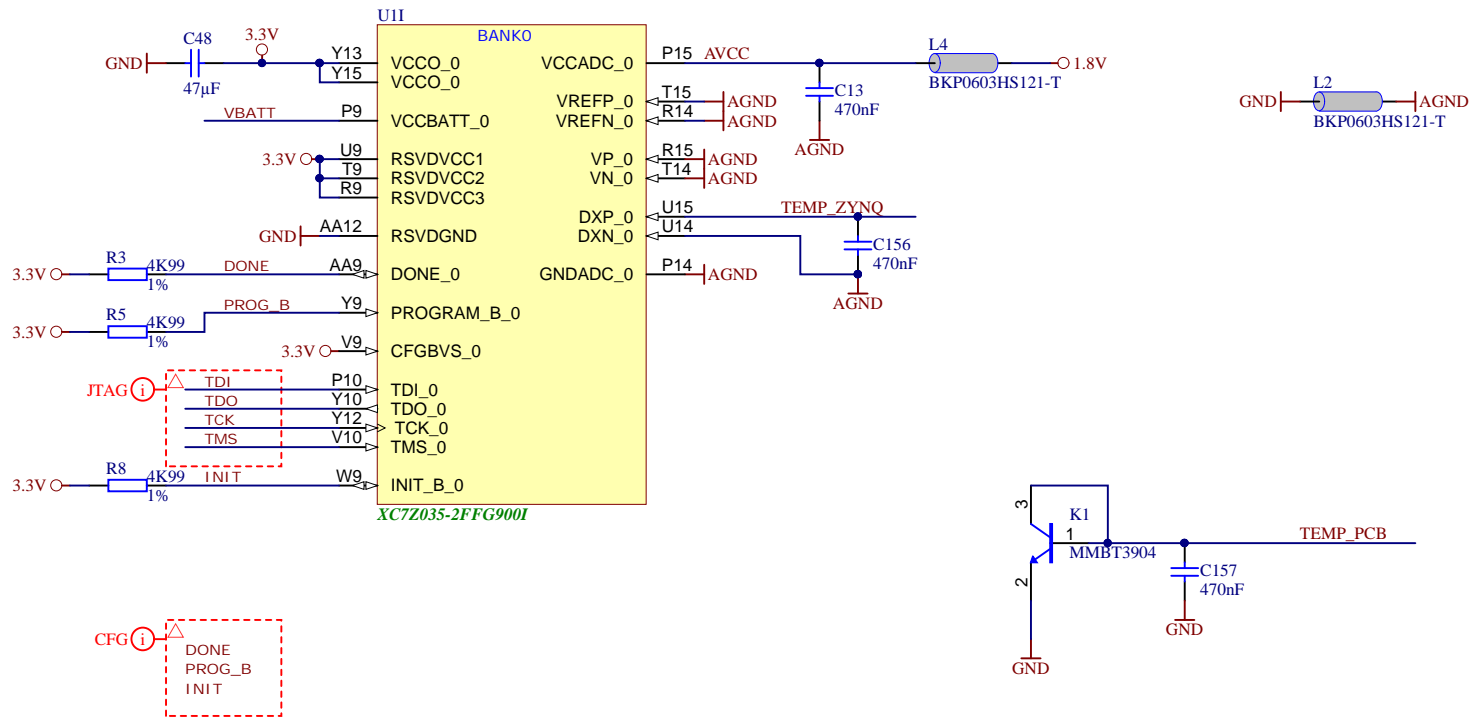
2

3

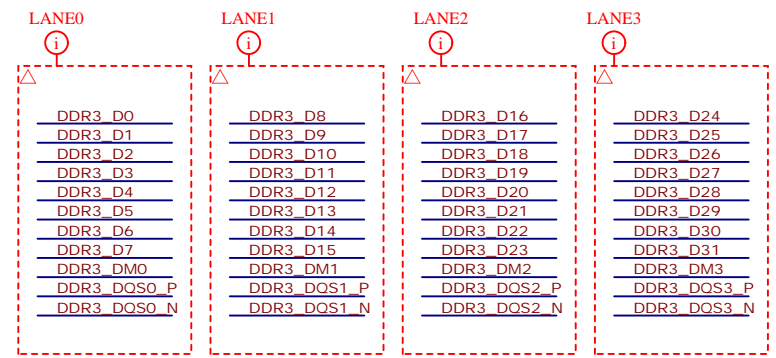
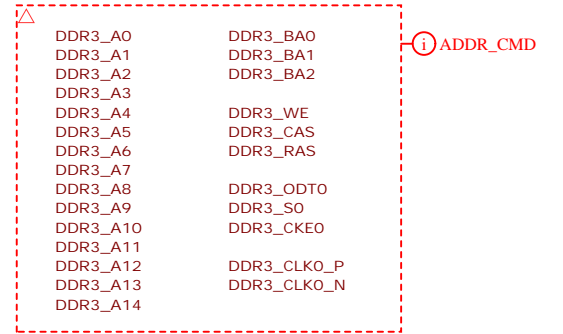
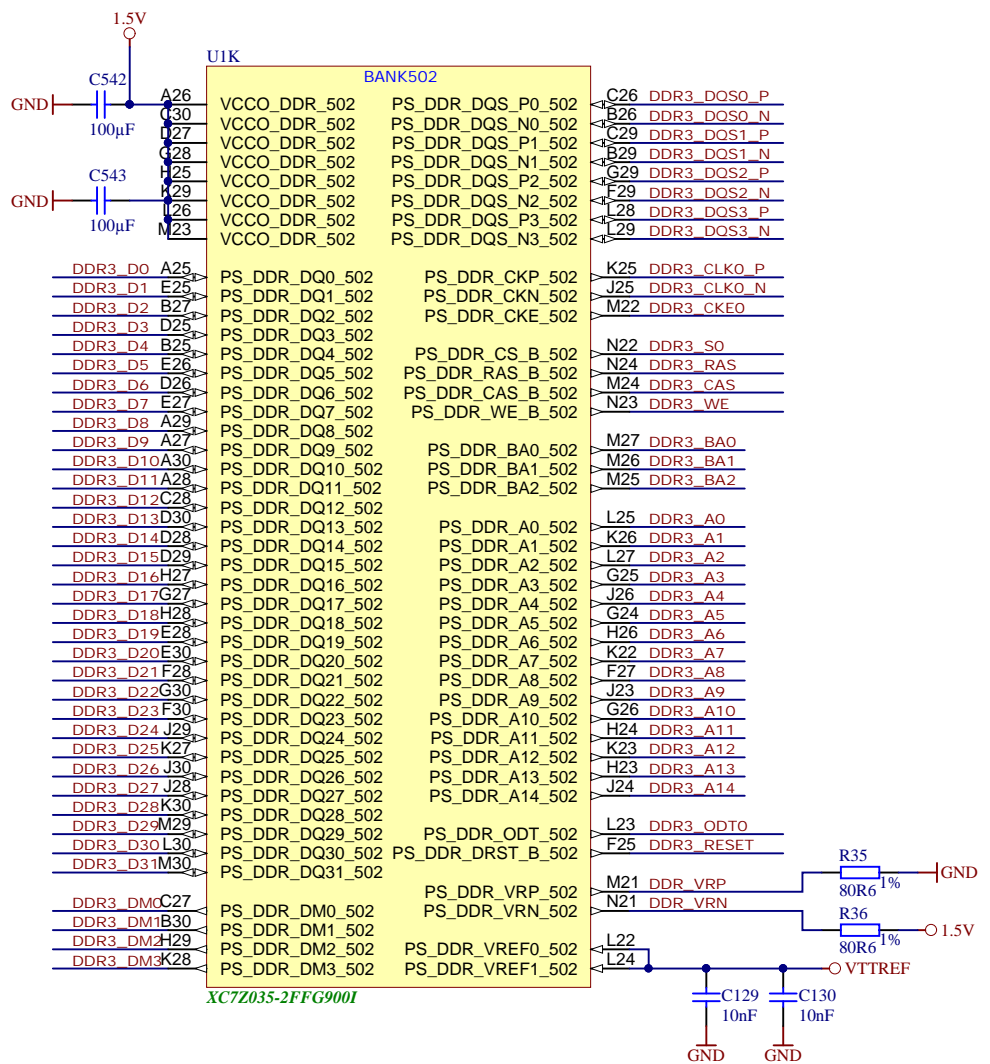
4



Placeholder 1 row 6 pin header



	Title: FPGA Configuration		
	A4	Nummer: TE0783 035-2I	Rev. 01
	Datum: 15.05.2018	Zeichner: Trenz Electronic GmbH	Blatt 7 von 31
	Filename: FPGA-CFG.SchDoc		



Title: FPGA DDR Banks		
A4	Number: TE0783 035-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 8 of 31
Filename: PS-DDR.SchDoc		

U1M

ClassName: MGT_TX

D100

BANK109

MGT_CLK2_P AD10
 MGT_CLK2_N AD9
 MGT_CLK3_P AF10
 MGT_CLK3_N AF9

MGTREFCLK0P_109
 MGTREFCLK0N_109
 MGTREFCLK1P_109
 MGTREFCLK1N_109

MGTXTXP0_109
 MGTXTXN0_109
 MGTXTXP1_109
 MGTXTXN1_109
 MGTXTXP2_109
 MGTXTXN2_109
 MGTXTXP3_109
 MGTXTXN3_109

AK10 MGT_TX0_P
 AK9 MGT_TX0_N
 AK6 MGT_TX1_P
 AK5 MGT_TX1_N
 AJ4 MGT_TX2_P
 AJ3 MGT_TX2_N
 AK2 MGT_TX3_P
 AK1 MGT_TX3_N

BANK110

MGT_CLK0_P AA8
 MGT_CLK0_N AA7
 MGT_CLK1_N AC8
 MGT_CLK1_P AC7

MGTREFCLK0P_110
 MGTREFCLK0N_110
 MGTREFCLK1P_110
 MGTREFCLK1N_110

MGTXTXP0_110
 MGTXTXN0_110
 MGTXTXP1_110
 MGTXTXN1_110
 MGTXTXP2_110
 MGTXTXN2_110
 MGTXTXP3_110
 MGTXTXN3_110

AH2 MGT_TX4_P
 AH1 MGT_TX4_N
 AF2 MGT_TX5_P
 AF1 MGT_TX5_N
 AE4 MGT_TX6_P
 AE3 MGT_TX6_N
 AD2 MGT_TX7_P
 AD1 MGT_TX7_N

BANK111

MGT_CLK4_N U8
 MGT_CLK4_P U7
 MGT_CLK5_P W8
 MGT_CLK5_N W7

MGTREFCLK0P_111
 MGTREFCLK0N_111
 MGTREFCLK1P_111
 MGTREFCLK1N_111

MGTXTXP0_111
 MGTXTXN0_111
 MGTXTXP1_111
 MGTXTXN1_111
 MGTXTXP2_111
 MGTXTXN2_111
 MGTXTXP3_111
 MGTXTXN3_111

AB2 MGT_TX8_P
 AB1 MGT_TX8_N
 Y2 MGT_TX9_P
 Y1 MGT_TX9_N
 W4 MGT_TX10_P
 W3 MGT_TX10_N
 V2 MGT_TX11_P
 V1 MGT_TX11_N

BANK112

MGT_CLK6_P N8
 MGT_CLK6_N N7
 MGT_CLK7_P R8
 MGT_CLK7_N R7

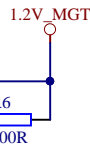
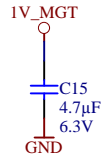
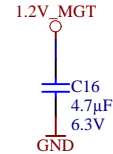
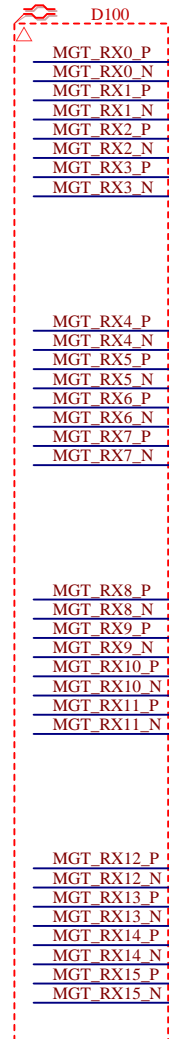
MGTREFCLK0P_112
 MGTREFCLK0N_112
 MGTREFCLK1P_112
 MGTREFCLK1N_112

MGTXTXP0_112
 MGTXTXN0_112
 MGTXTXP1_112
 MGTXTXN1_112
 MGTXTXP2_112
 MGTXTXN2_112
 MGTXTXP3_112
 MGTXTXN3_112

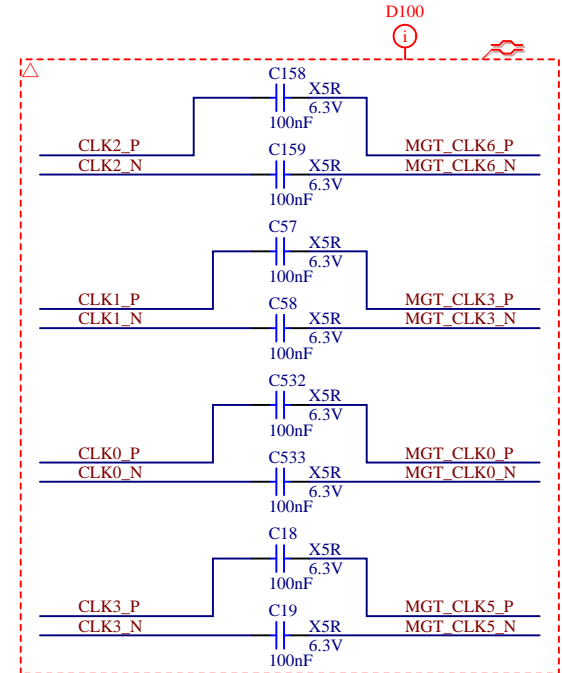
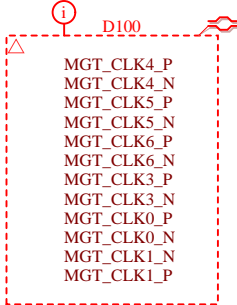
AB10 MGT_TX12_P
 AB9 MGT_TX12_N
 T2 MGT_TX12_P
 T1 MGT_TX12_N
 R4 MGT_TX13_P
 R3 MGT_TX13_N
 P2 MGT_TX14_P
 P1 MGT_TX14_N
 N4 MGT_TX15_P
 N3 MGT_TX15_N

XC7Z035-2FFG900I

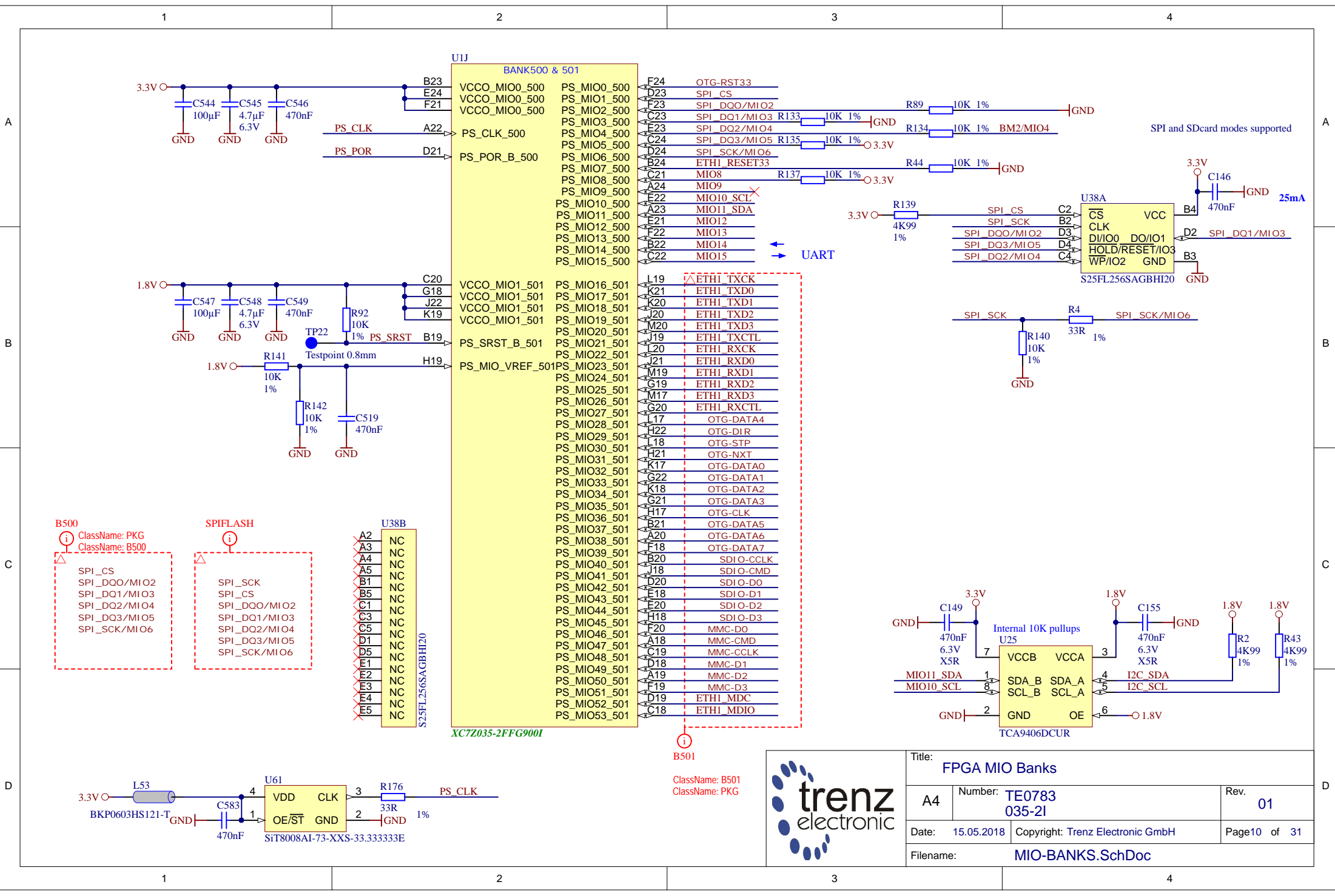
ClassName: MGT_RX



MGT_CLK

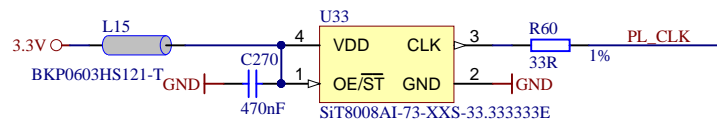
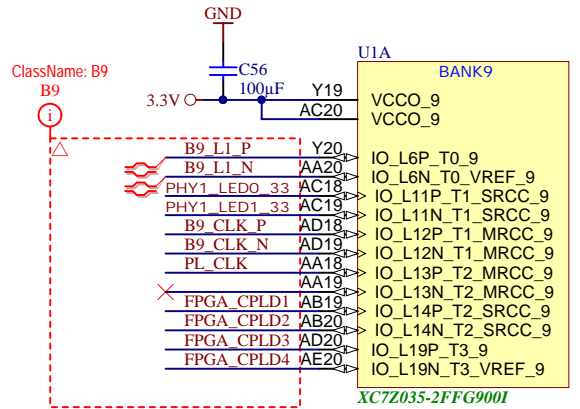



Title: FPGA MGT		
A4	Number: TE0783 035-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 9 of 31
Filename: FPGA-MGT.SchDoc		



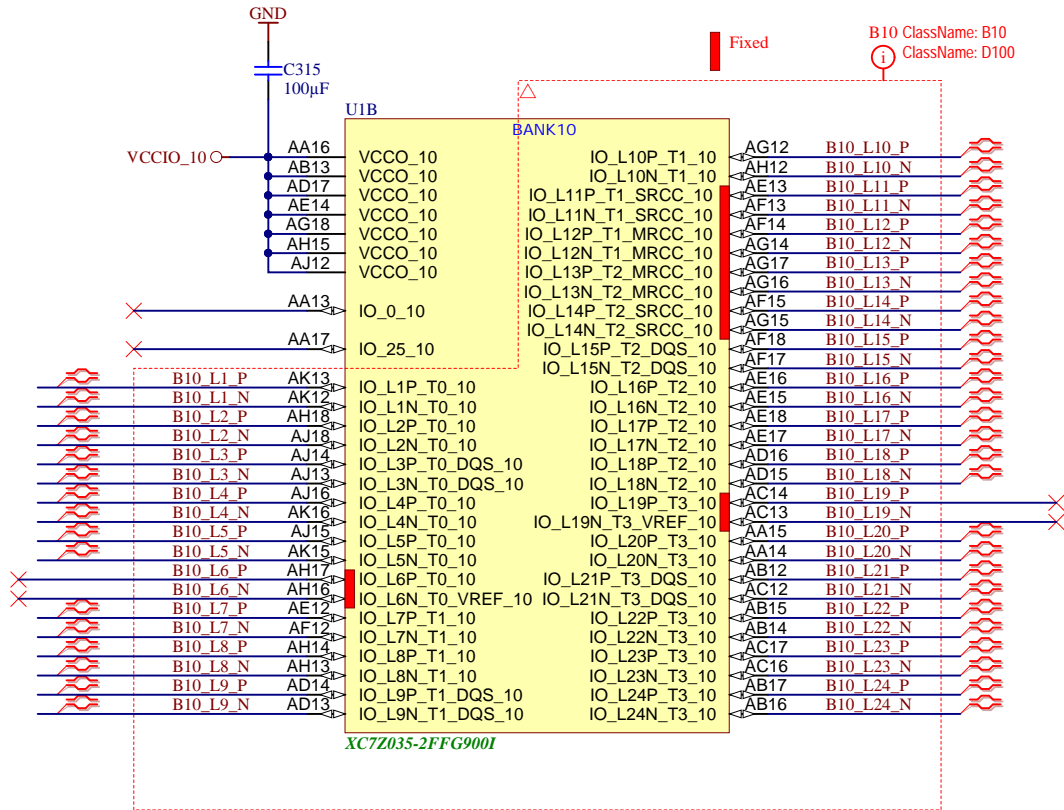
Title: FPGA MIO Banks		
A4	Number: TE0783 035-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 10 of 31
Filename: MIO-BANKS.SchDoc		

ClassName: B501
ClassName: PKG



			Title: FPGA B9	
			A4	Number: TE0783 035-2I
Date: 15.05.2018		Copyright: Trenz Electronic GmbH		Page 11 of 31
Filename: B9.SchDoc				

TP4
 ● VCCIO_10
 ○ Testpoint 0.8mm



Title: FPGA B10		
A4	Number: TE0783 035-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 12 of 31
Filename: B10.SchDoc		

A

A

B

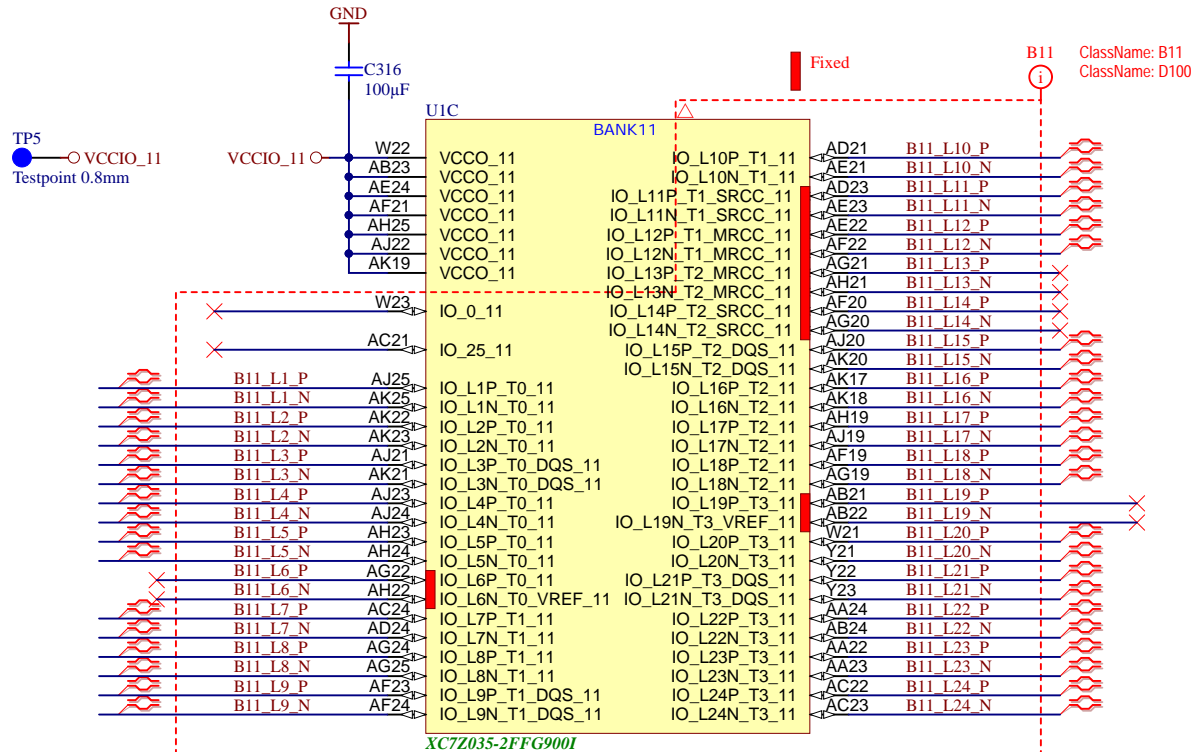
B


C


C

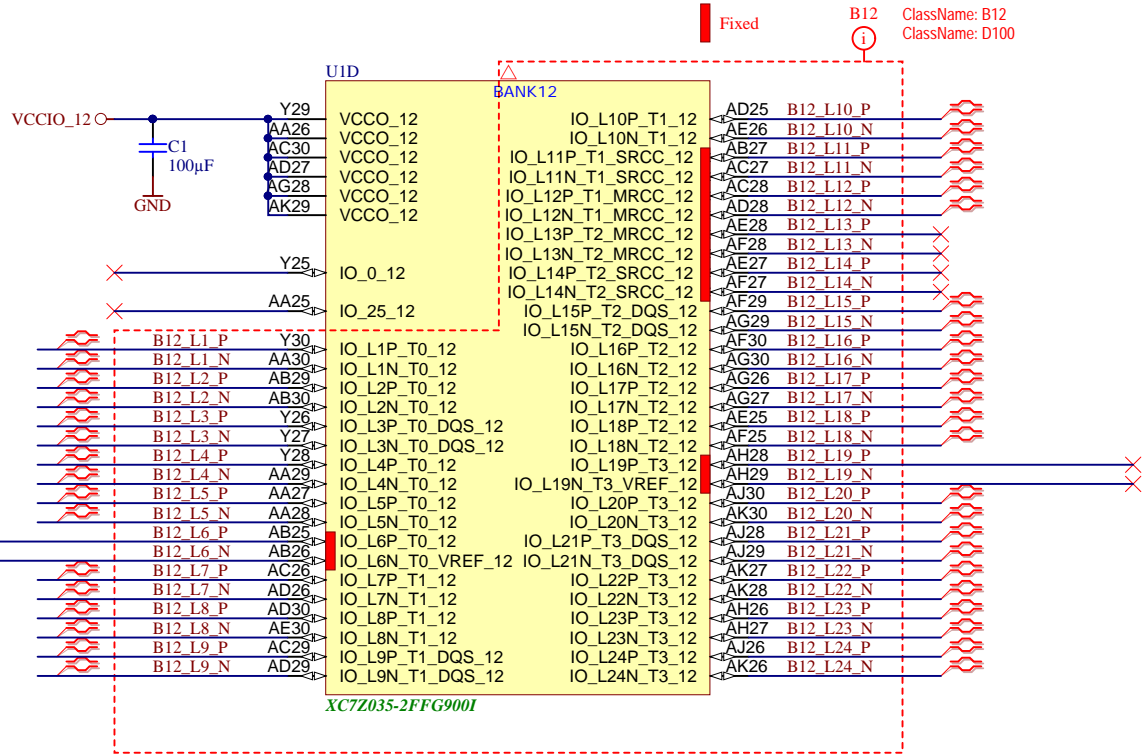
D

D



		Title: FPGA B11	
		A4	Number: TE0783 035-2I
Date: 15.05.2018		Copyright: Trenz Electronic GmbH	
Filename: B11.SchDoc		Page 13 of 31	

TP1
 VCCIO_12
 Testpoint 0.8mm

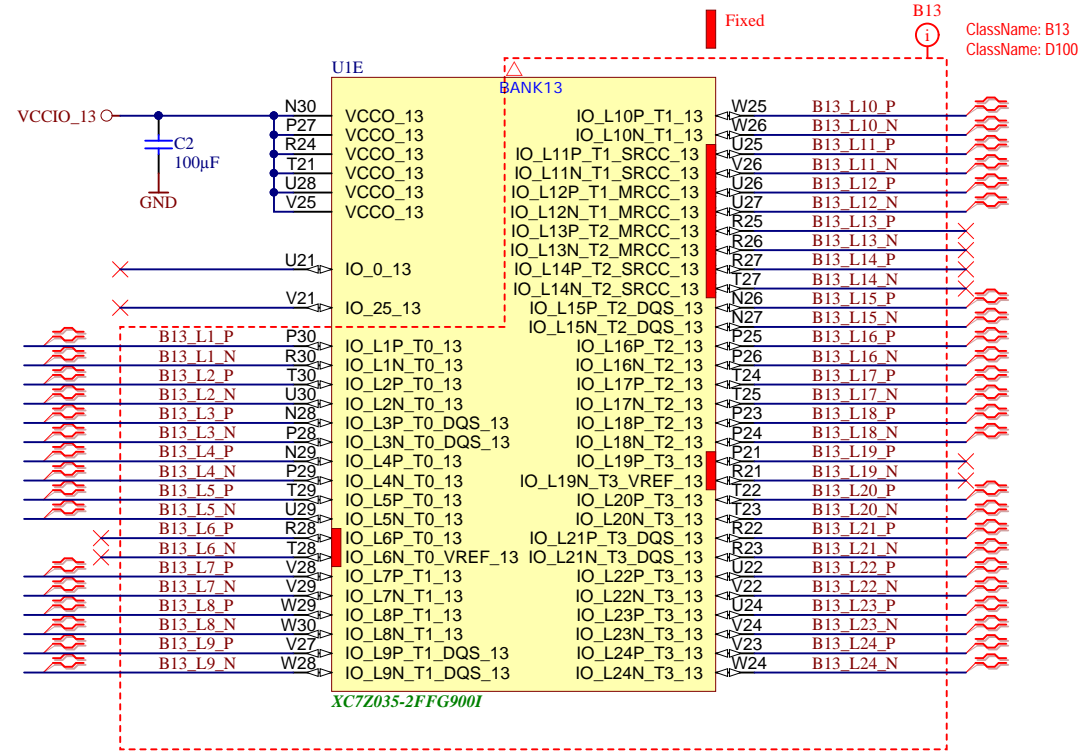


XC7Z035-2FFG900I



Title: FPGA B12		
A4	Number: TE0783 035-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 14 of 31
Filename: B12.SchDoc		

TP2
 ● ○ VCCIO_13
 Testpoint 0.8mm



Title: FPGA B13		
A4	Number: TE0783 035-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 15 of 31
Filename: B13.SchDoc		

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U_B33
B33.SchDoc



U_B34
B34.SchDoc



U_B35
B35.SchDoc



U_DDR3-RAM-PL1
DDR3-RAM-PL1.SchDoc



U_DDR3-RAM-PL2
DDR3-RAM-PL2.SchDoc



A

A

B

B

C

C

D

D



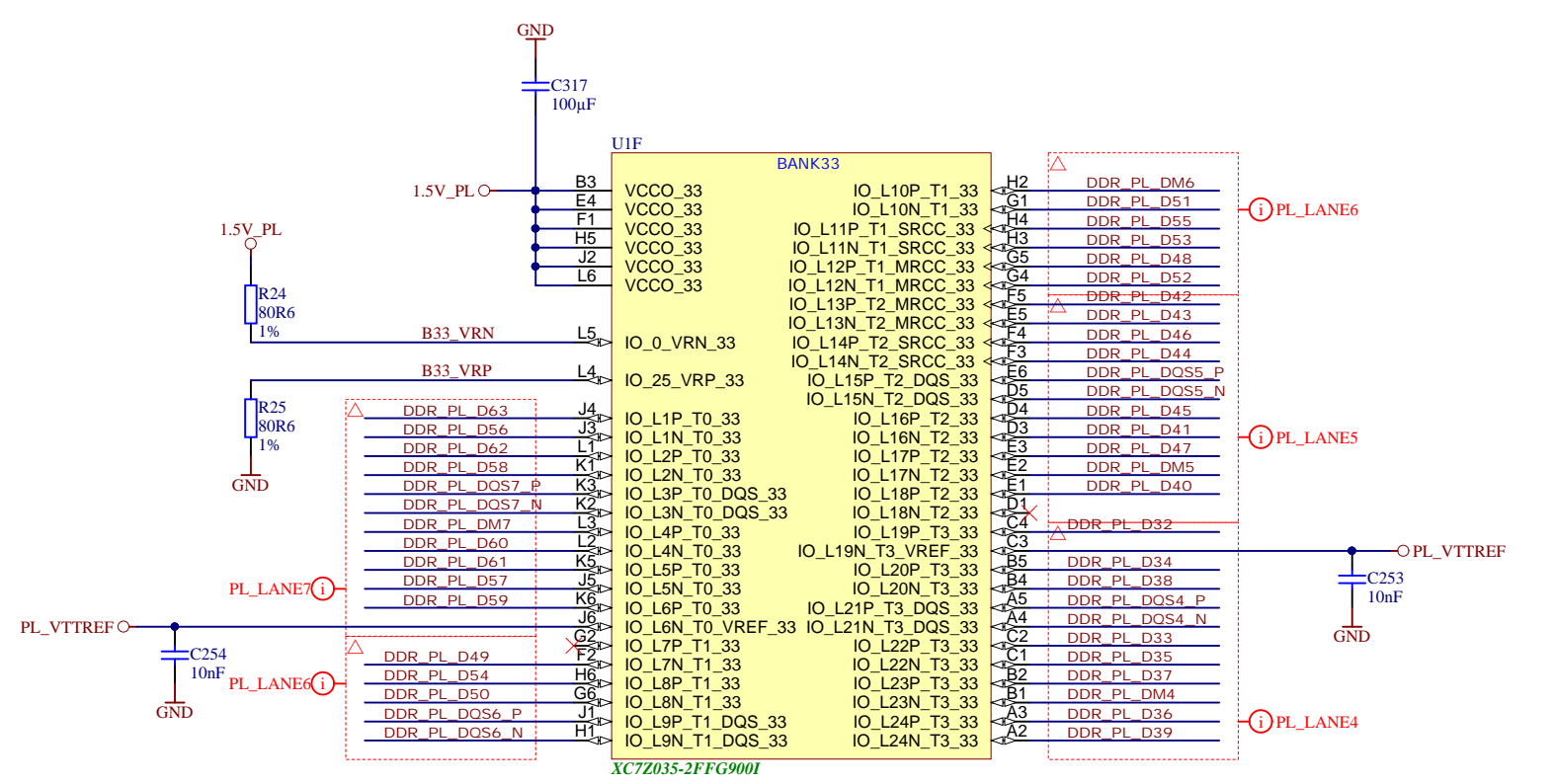
Title: FPGA HP Banks		
A4	Number: TE0783 035-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 16 of 31
Filename: HP-BANKS.SchDoc		

1

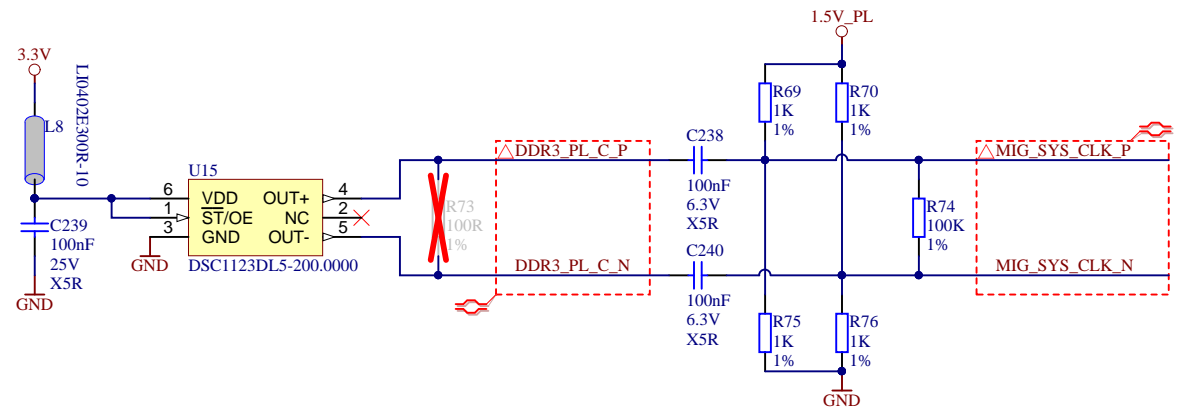
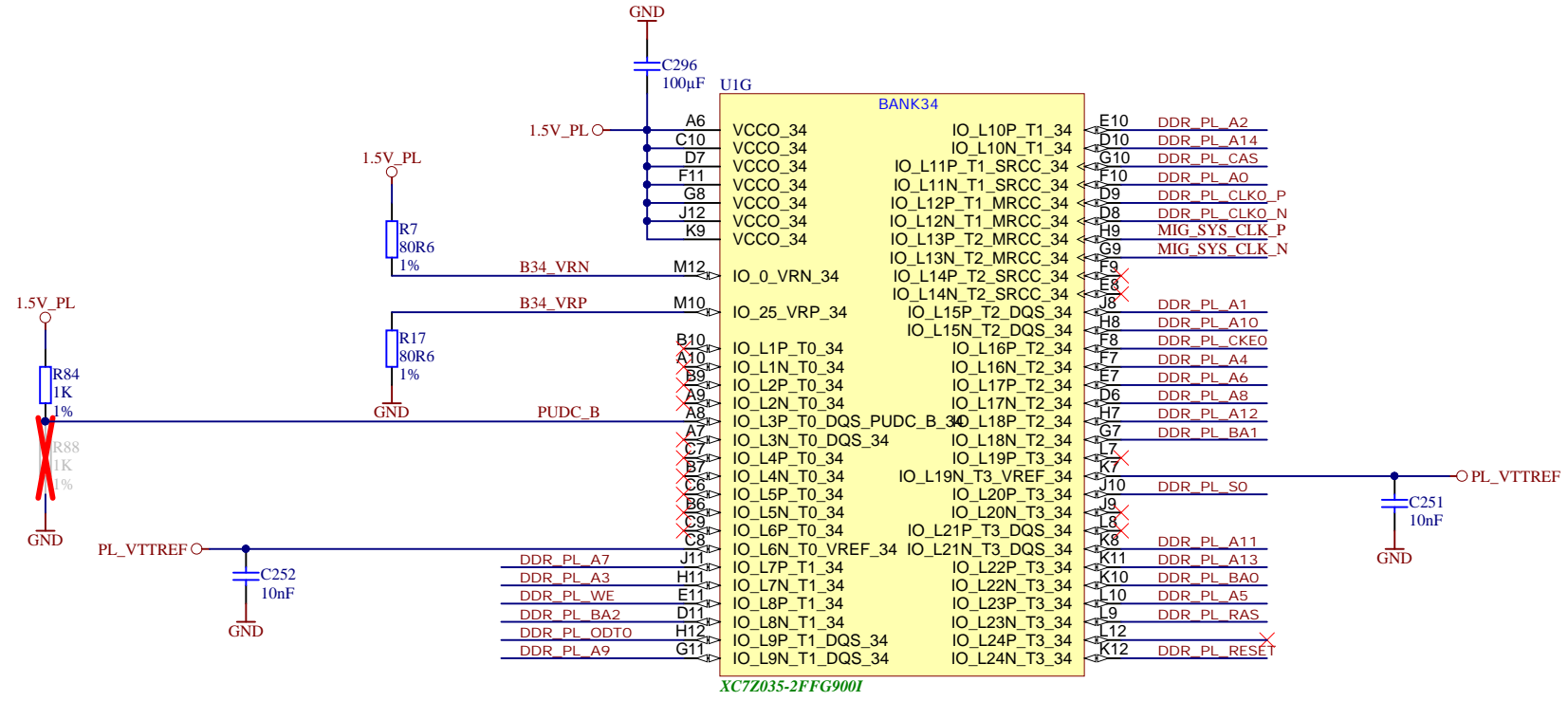
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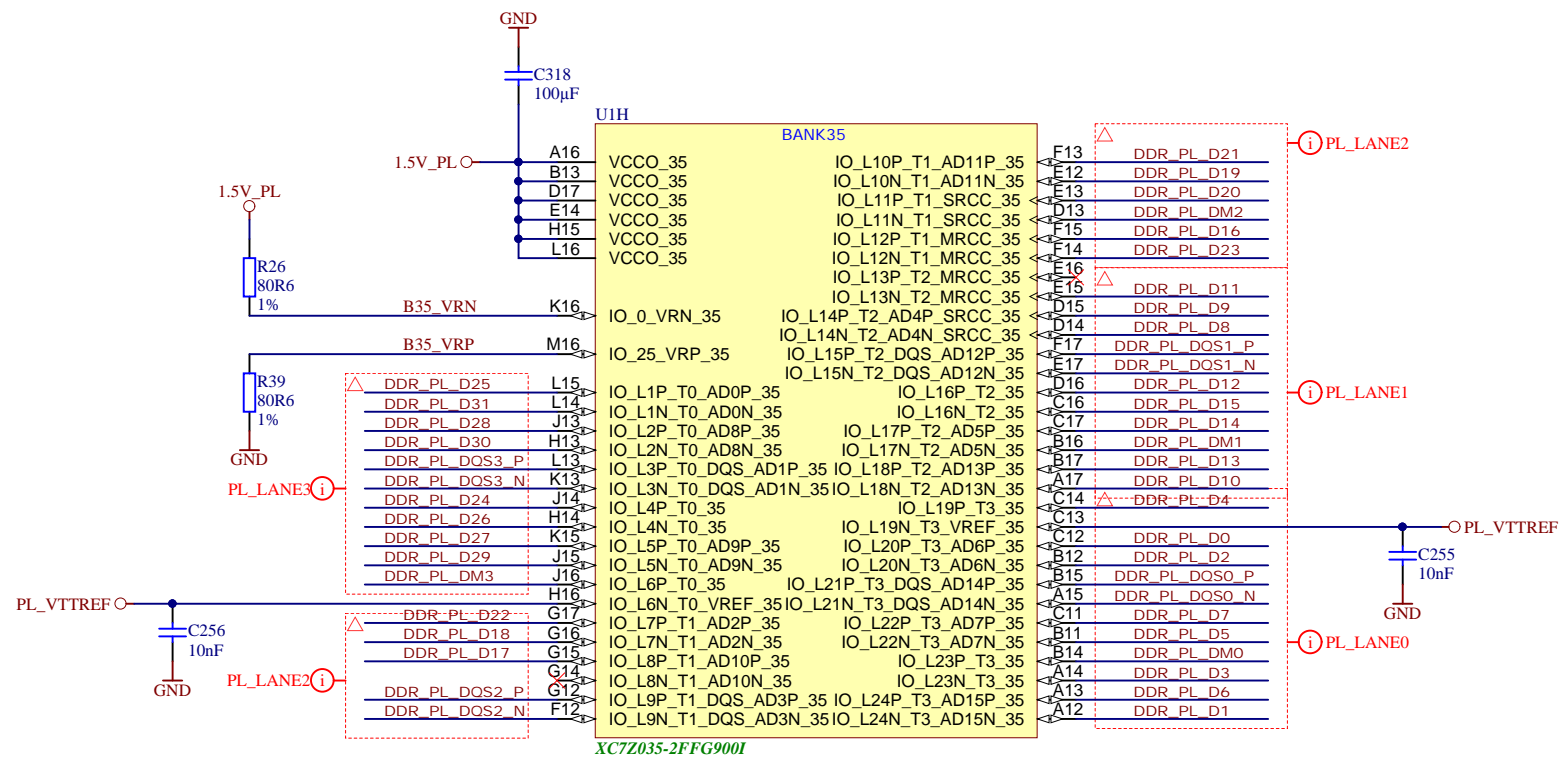
Title: FPGA B33		
A4	Number: TE0783 035-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 17 of 31
Filename: B33.SchDoc		




Check clock source. R74 100R changed to 100K

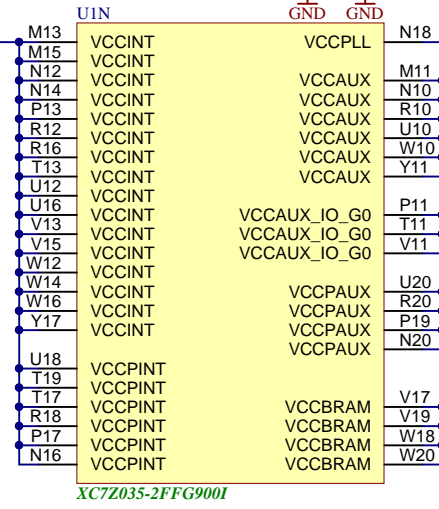
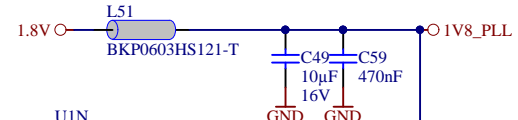
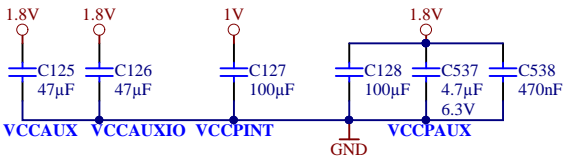
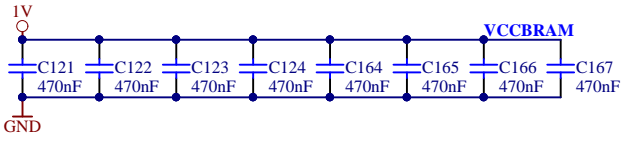
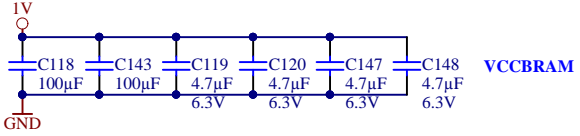
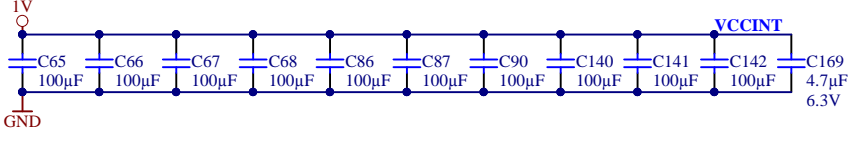
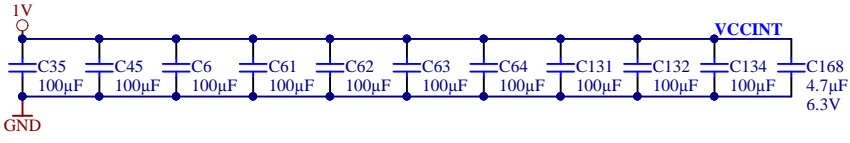


Title: FPGA B34		
A4	Number: TE0783 035-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 18 of 31
Filename: B34.SchDoc		

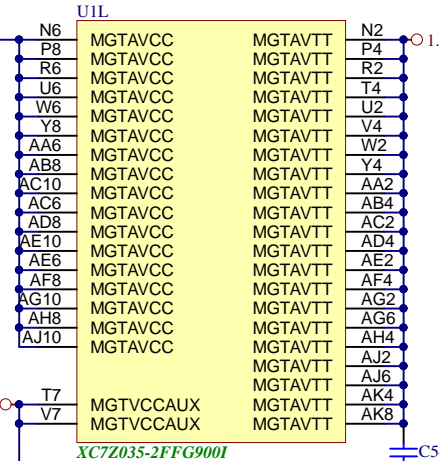


	Title: FPGA B35		
	A4	Number: TE0783 035-2I	Rev. 01
	Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 19 of 31
	Filename: B35.SchDoc		

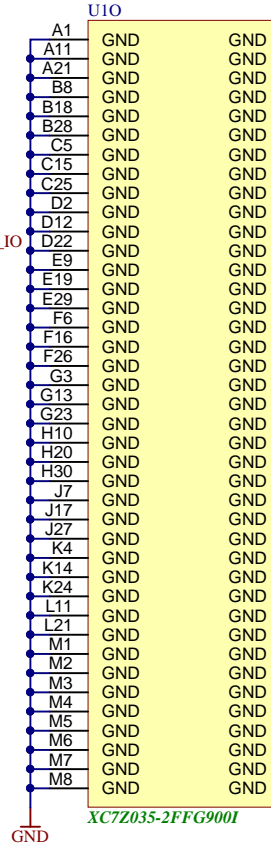
Capacitors suitable for XC7Z100



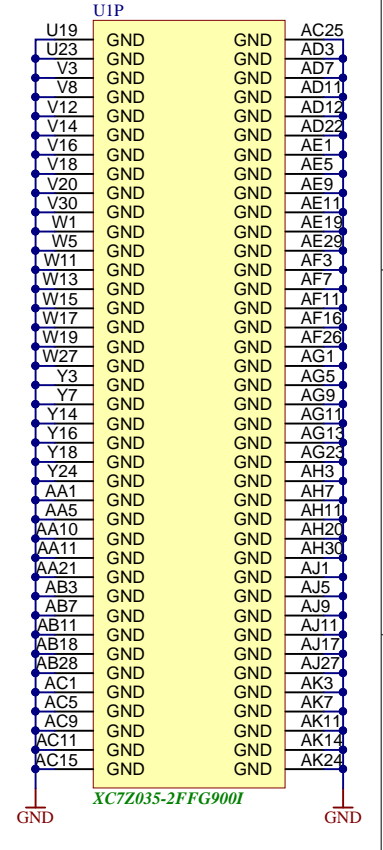
XC7Z035-2FFG9001



XC7Z035-2FFG9001



XC7Z035-2FFG9001



XC7Z035-2FFG9001



Title: ZYNQ POWER		
A4	Number: TE0783 035-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page20 of 31
Filename: FPGA-PWR.SchDoc		

A

B

C

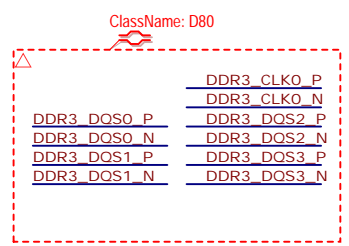
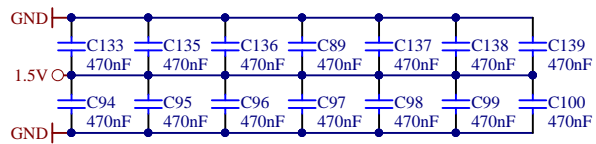
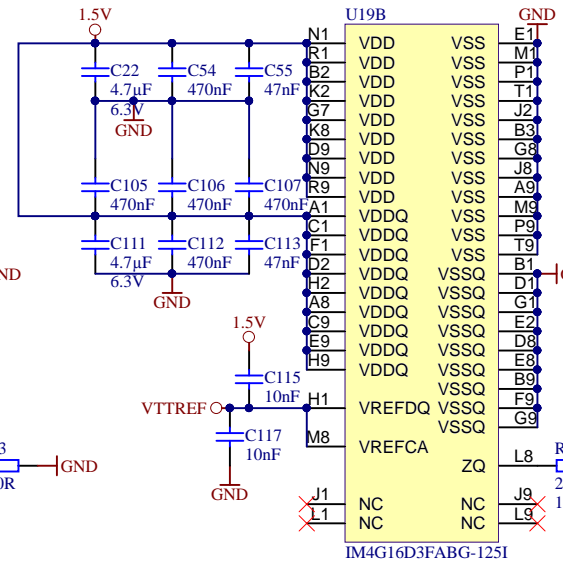
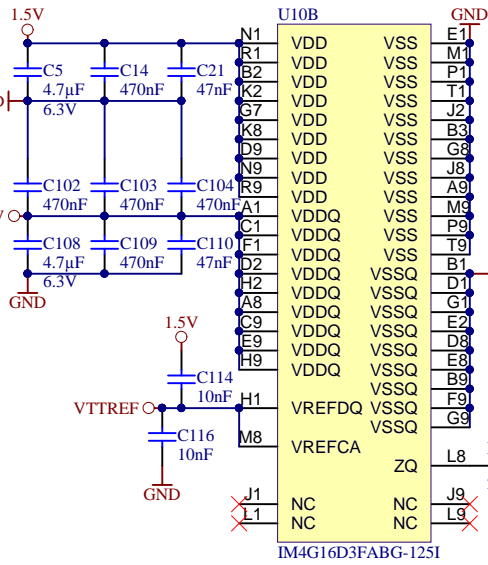
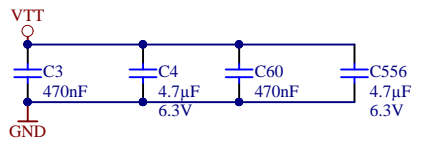
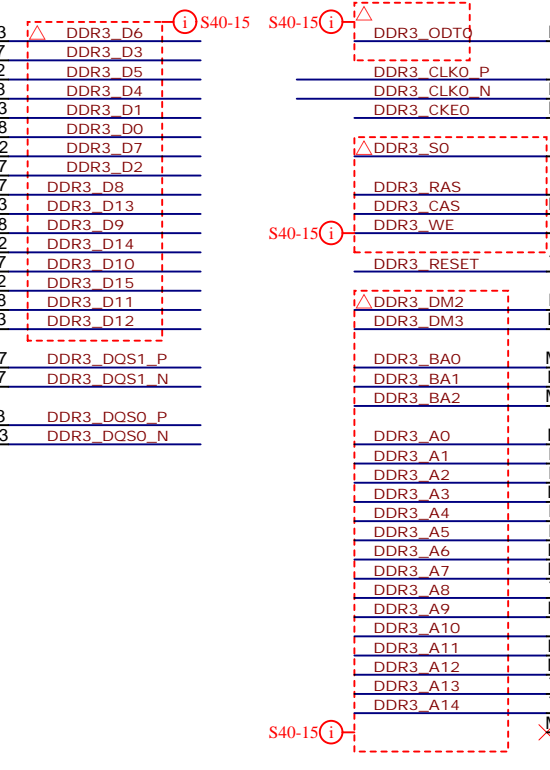
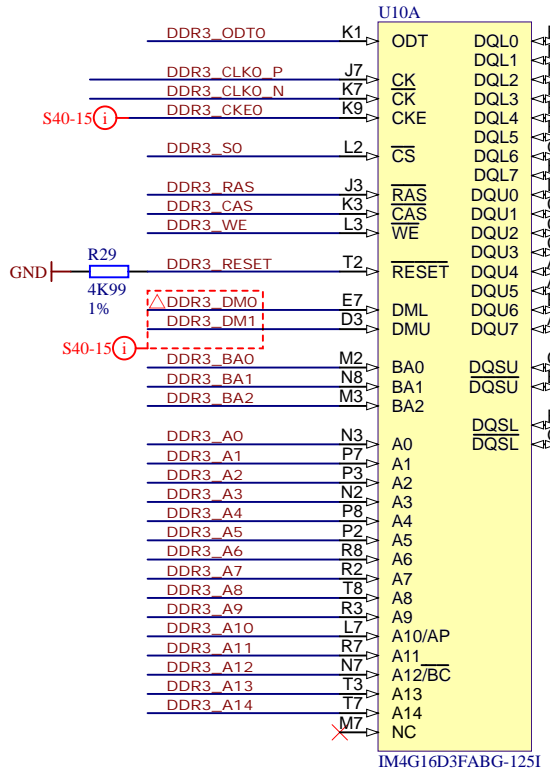
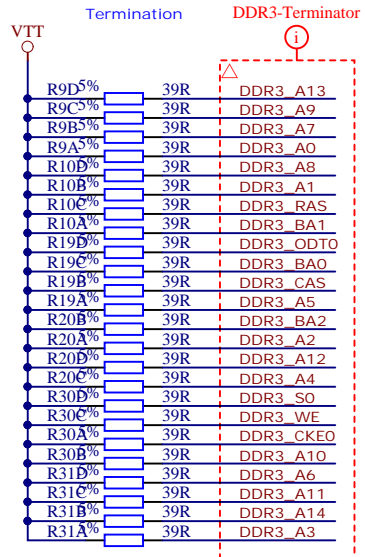
D

A

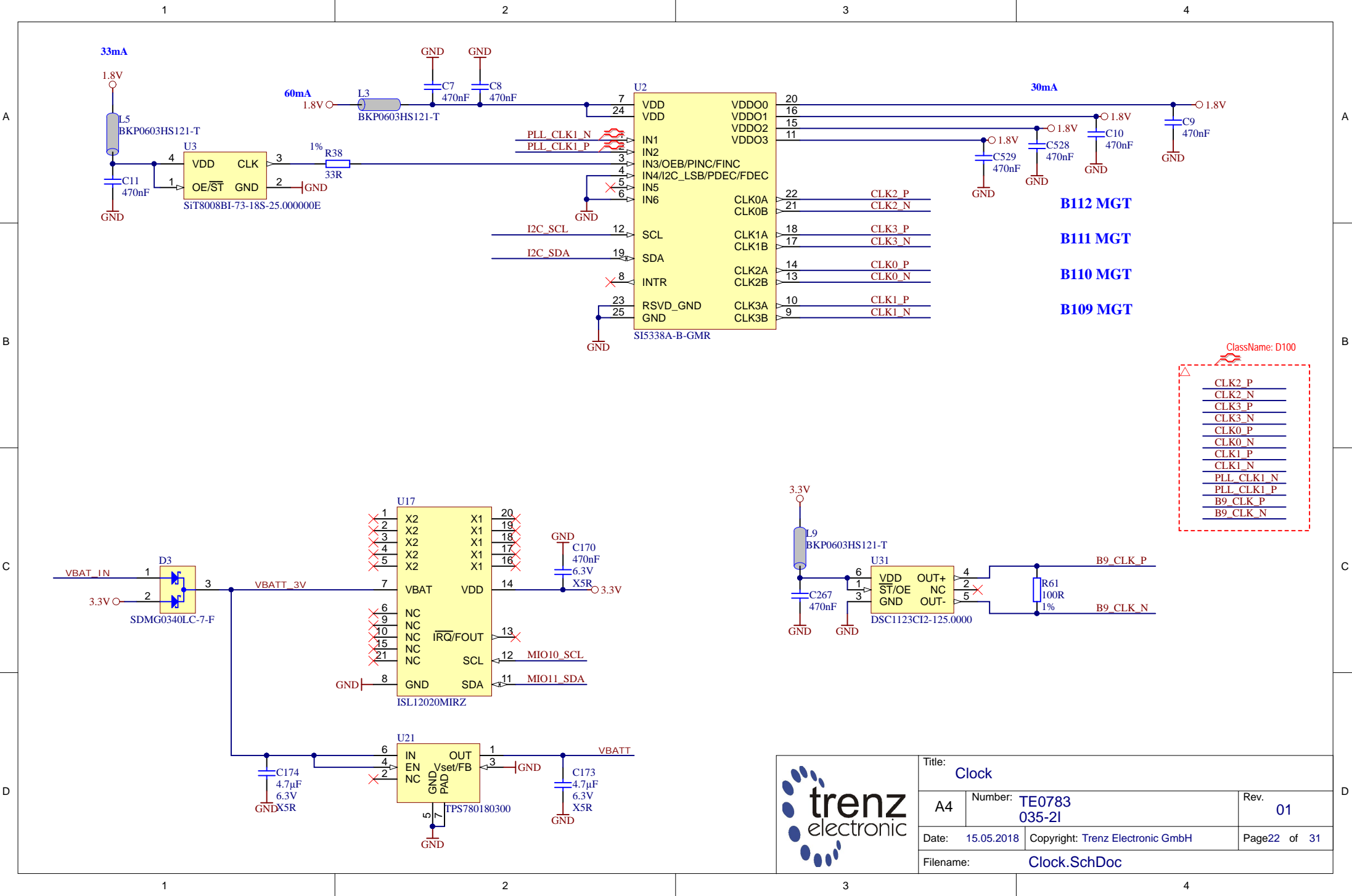
B

C

D



Title: DDR3 RAM PS		
A4	Number: TE0783 035-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 21 of 31
Filename: DDR3-RAM.SchDoc		



- ClassName: D100
- CLK2_P
 - CLK2_N
 - CLK3_P
 - CLK3_N
 - CLK0_P
 - CLK0_N
 - CLK1_P
 - CLK1_N
 - PLL_CLK1_N
 - PLL_CLK1_P
 - B9_CLK_P
 - B9_CLK_N



Title: Clock		
A4	Number: TE0783 035-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 22 of 31
Filename: Clock.SchDoc		

A

B

C

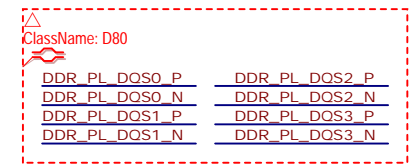
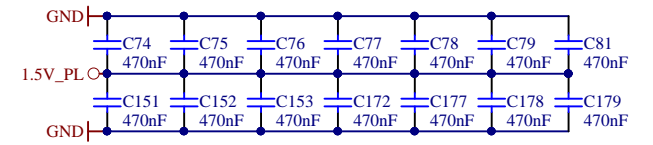
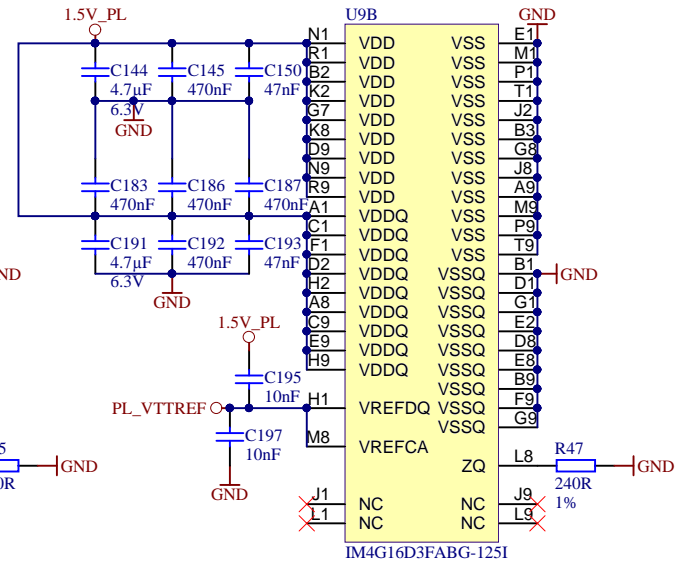
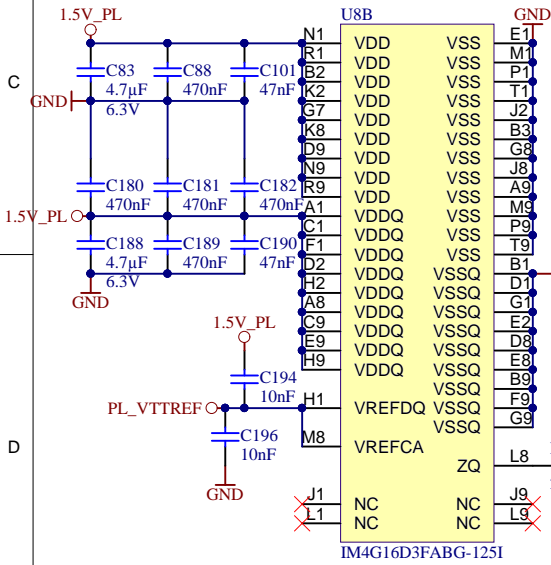
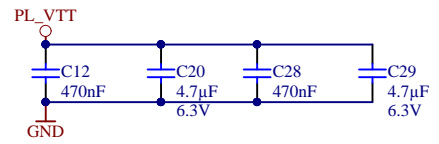
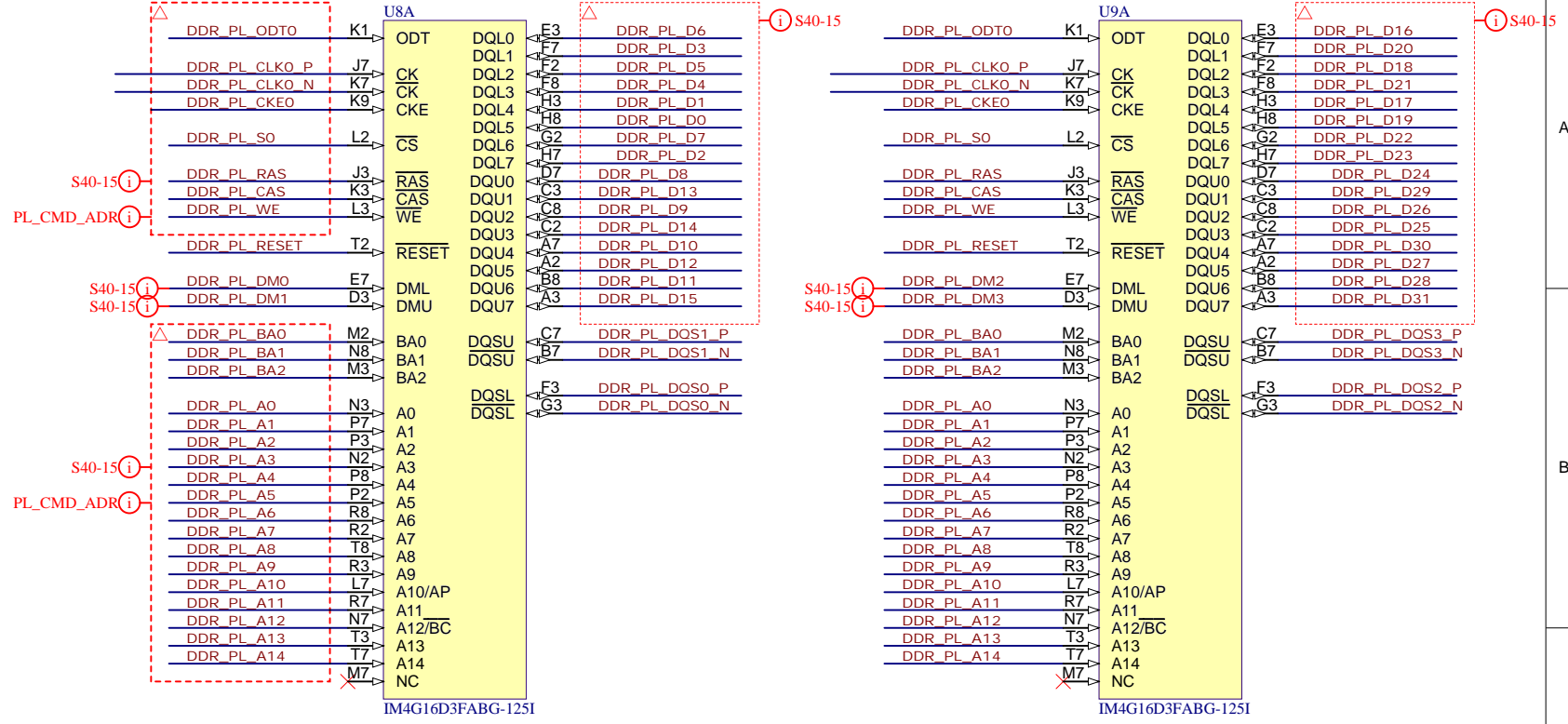
D

A

B

C

D



Title: DDR3 RAM PL		
A4	Number: TE0783 035-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 23 of 31
Filename: DDR3-RAM-PL1.SchDoc		

A

B

C

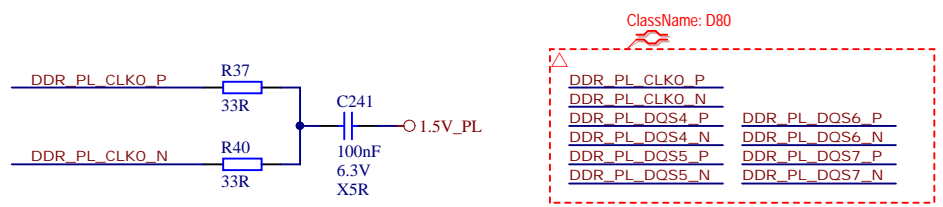
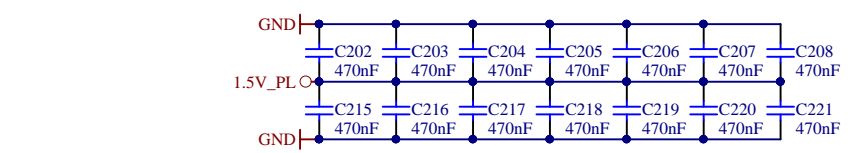
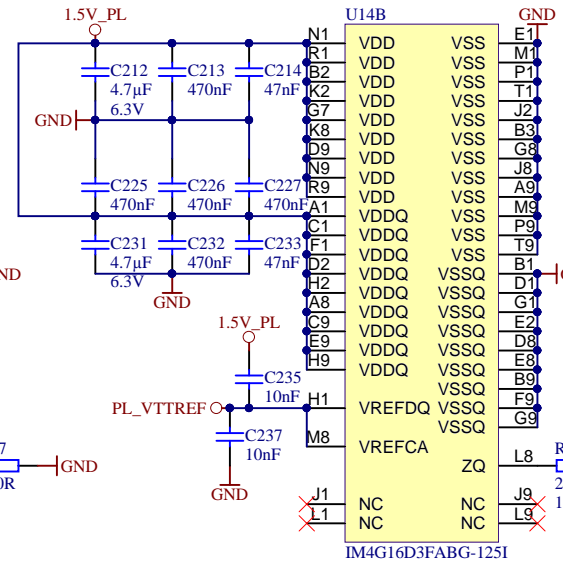
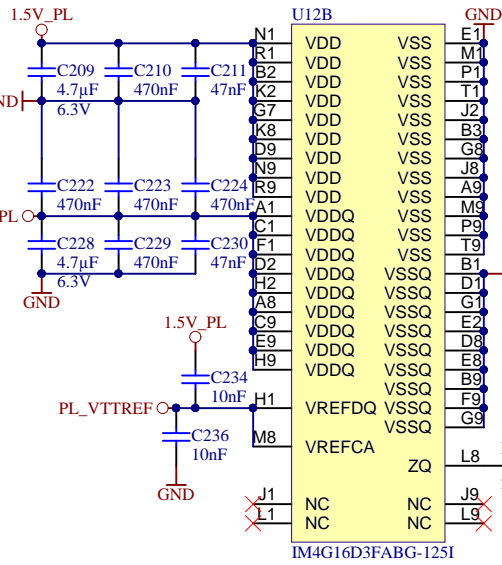
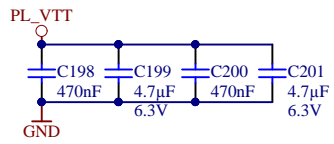
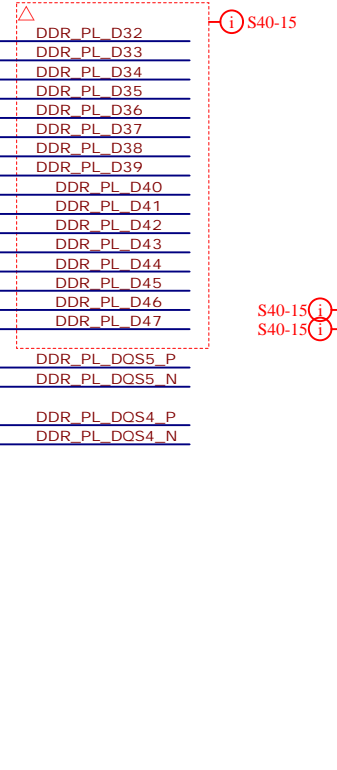
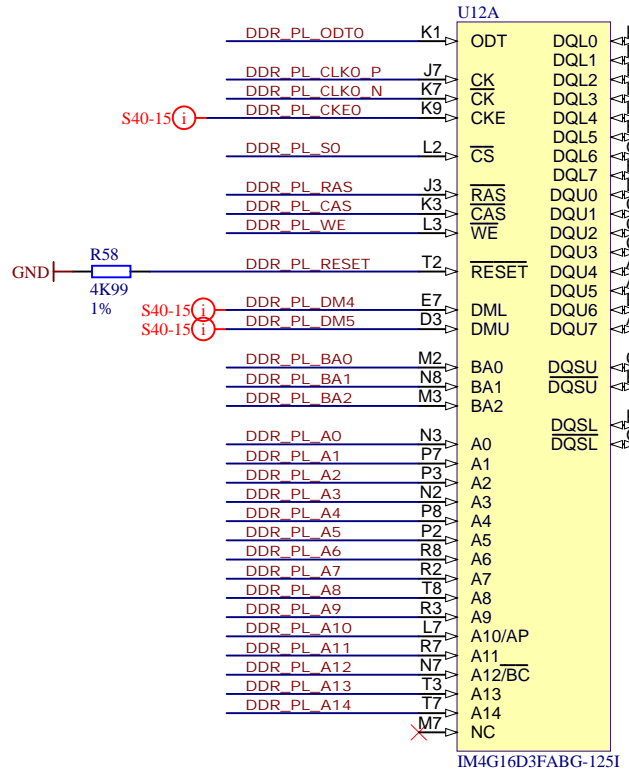
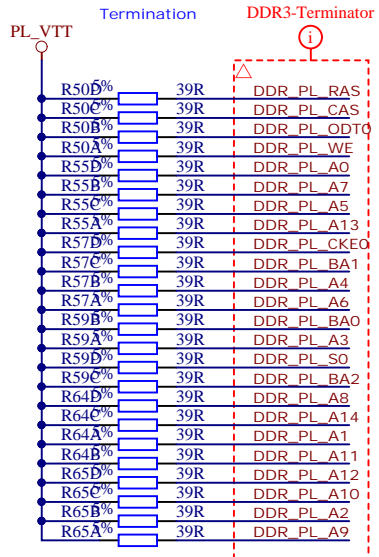
D

A

B

C

D



Place directly at the clock pins



Title: DDR3 RAM PL		
A4	Number: TE0783 035-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 24 of 31
Filename: DDR3-RAM-PL2.SchDoc		

A

B

C

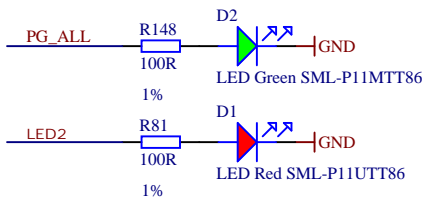
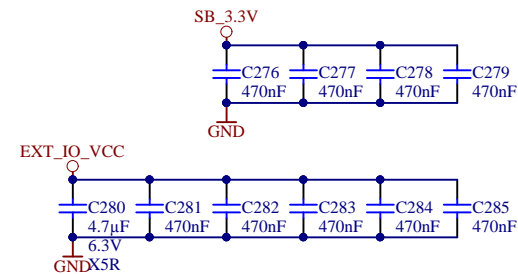
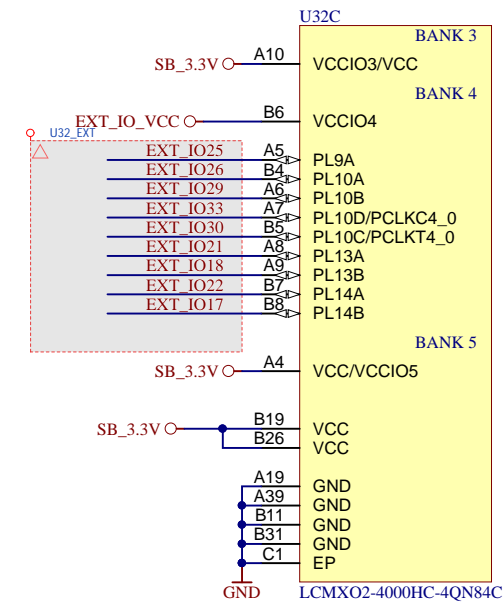
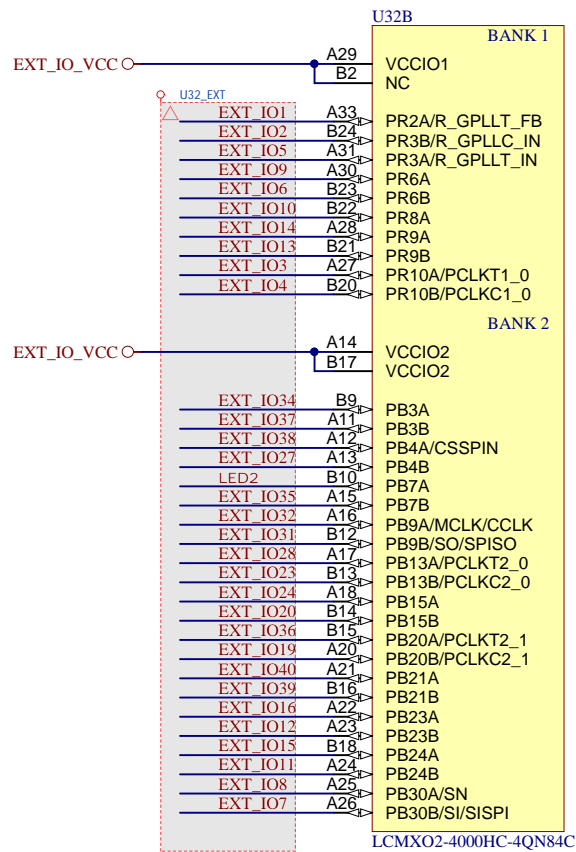
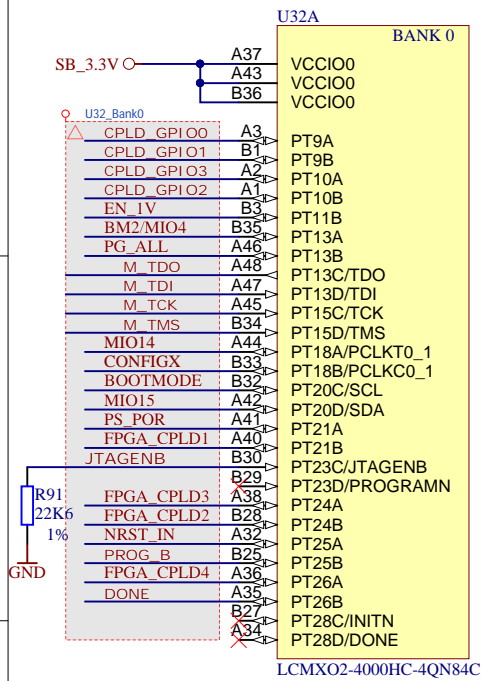
D

A

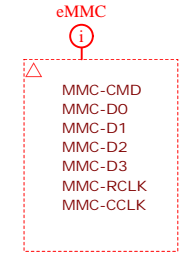
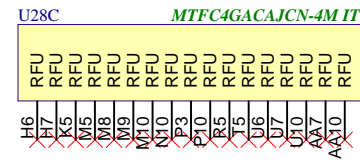
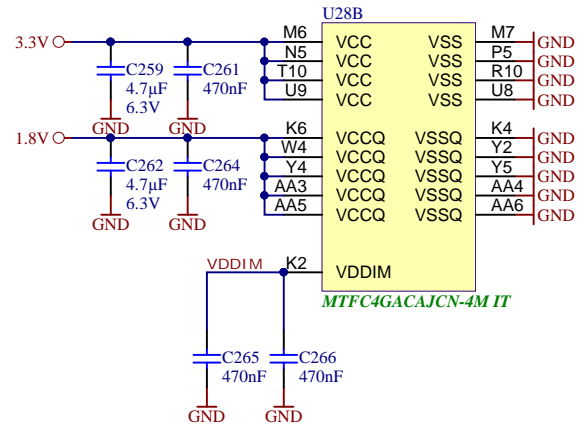
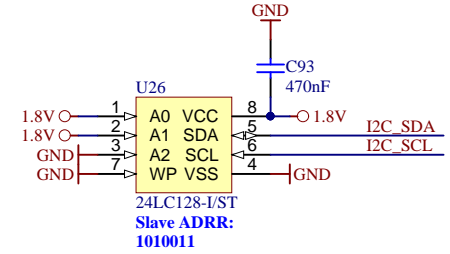
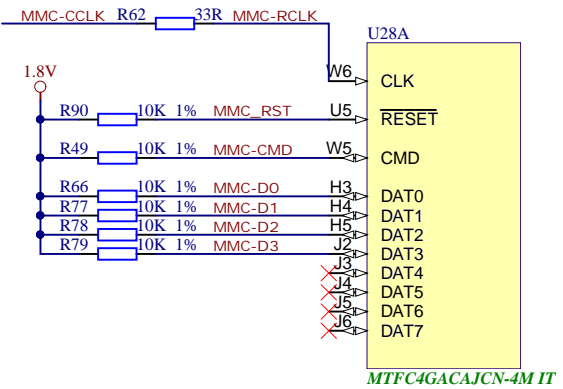
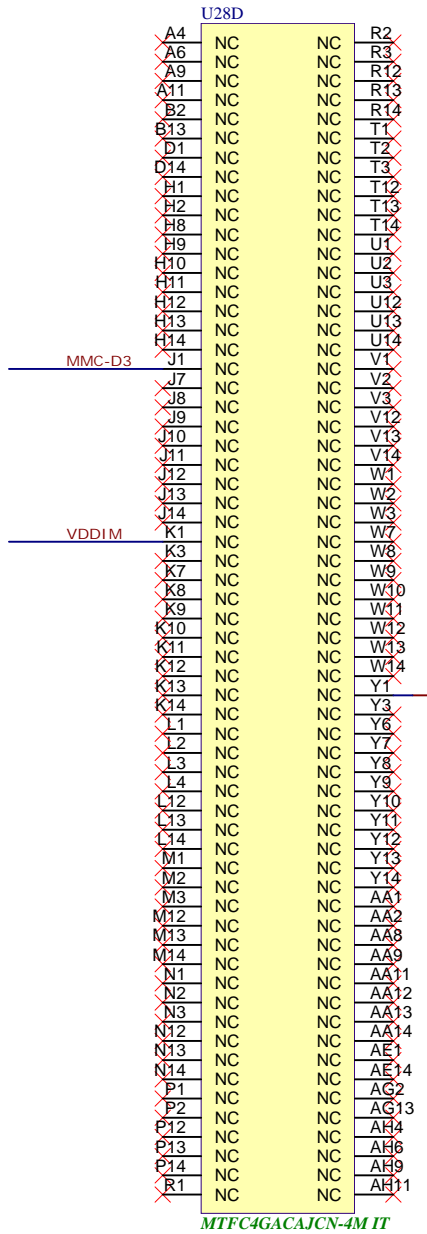
B

C

D



Title: CPLD		
A4	Number: TE0783 035-21	Rev. 01
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Filename: CPLD.SchDoc		



Title: eMMC		
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Filename: eMMC.SchDoc		

1

2

3

4

A

A

B

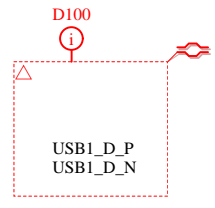
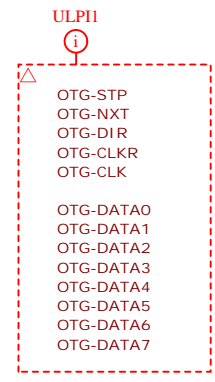
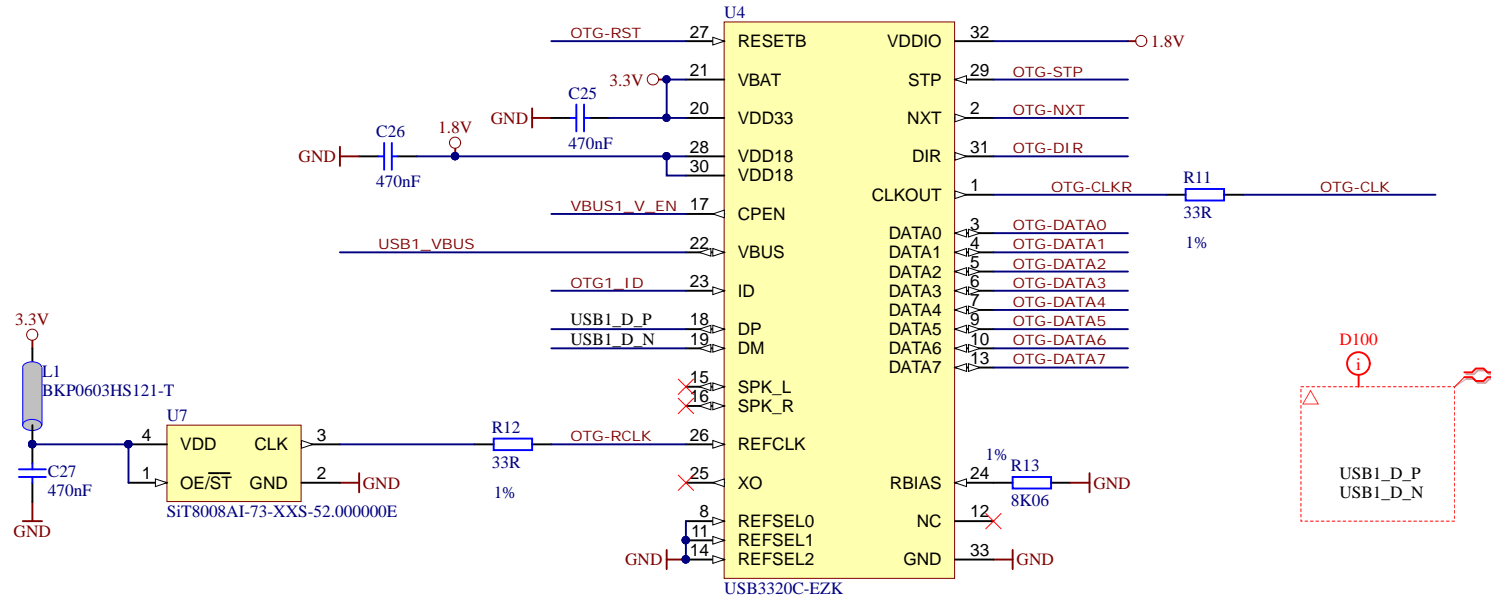
B

C

C

D

D



Title: USB-PHY		
A4	Number: TE0783 035-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 27 of 31
Filename: USB-PHY.SchDoc		

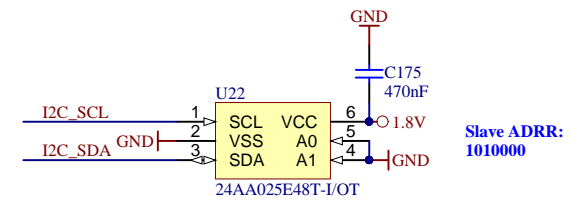
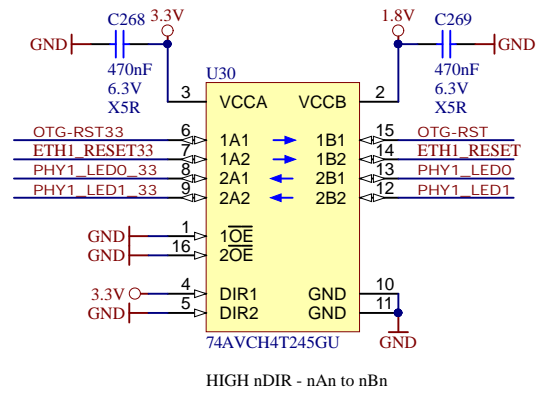
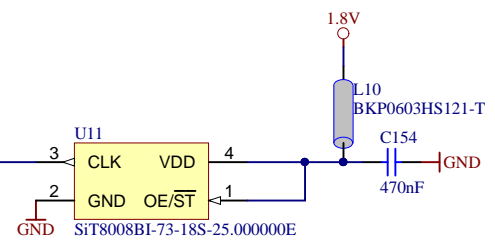
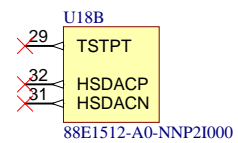
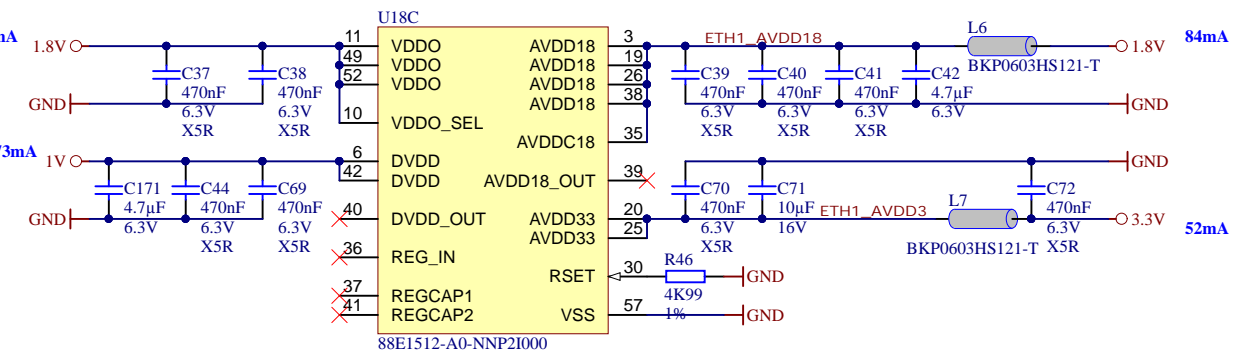
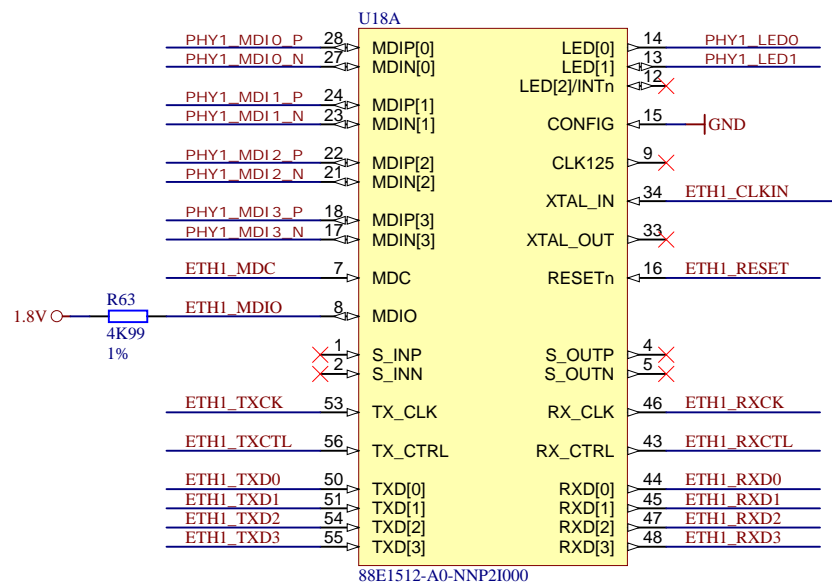
1

2

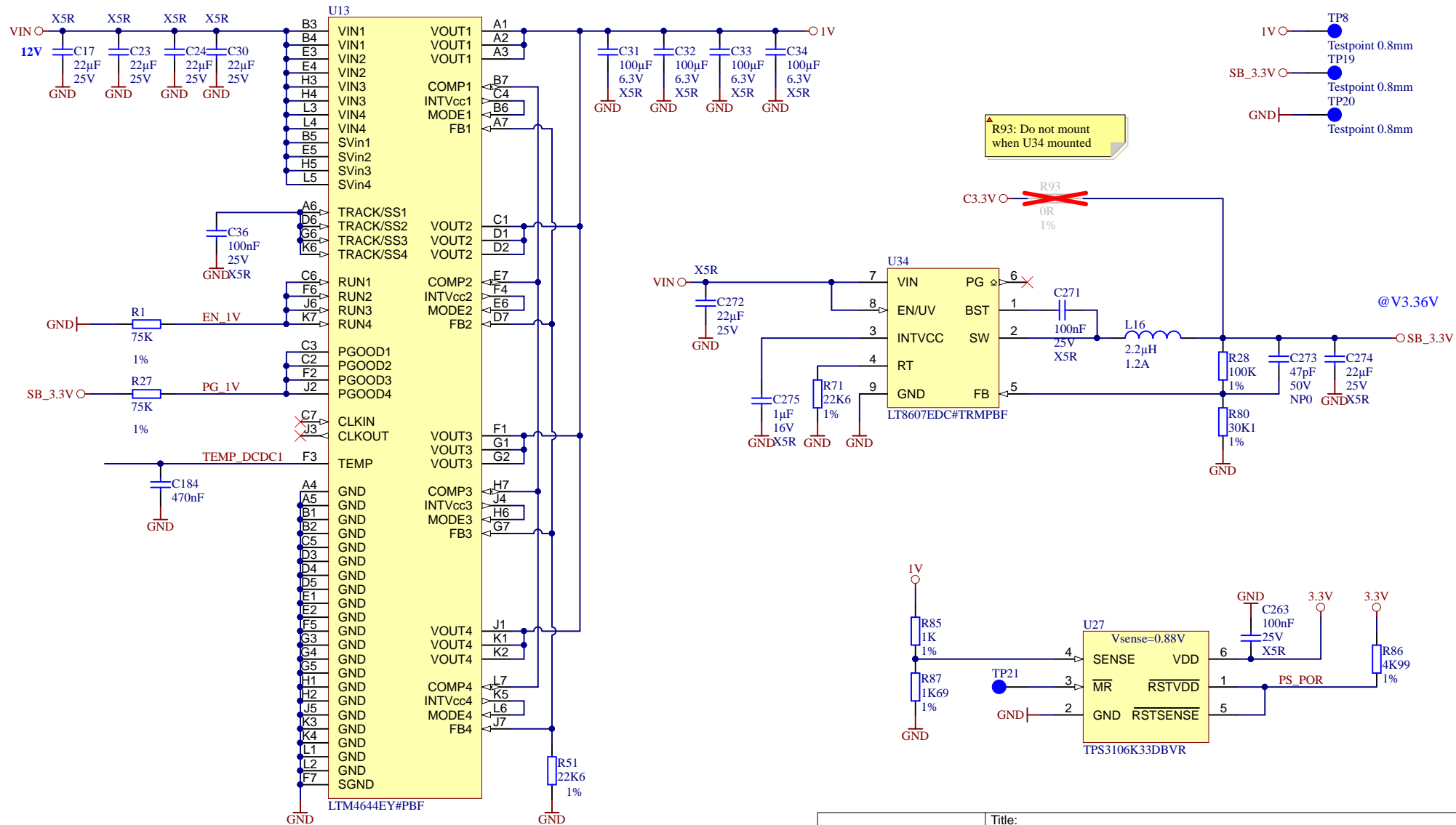
3

4

B9



Title: ETH_PHY1		
A4	Number: TE0783 035-21	Rev. 01
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Filename: ETH1.SchDoc		



	Title: POWER	
	A4	Number: TE0783 035-21
	Date: 15.05.2018	Copyright: Trenz Electronic GmbH
	Filename: POWER.SchDoc	Rev. 01

R93: Do not mount when U34 mounted

- 1V ○ TP8 Testpoint 0.8mm
- SB_3.3V ○ TP19 Testpoint 0.8mm
- GND TP20 Testpoint 0.8mm

@V3.36V

Vsense=0.88V

1

2

3

4

A

A

B

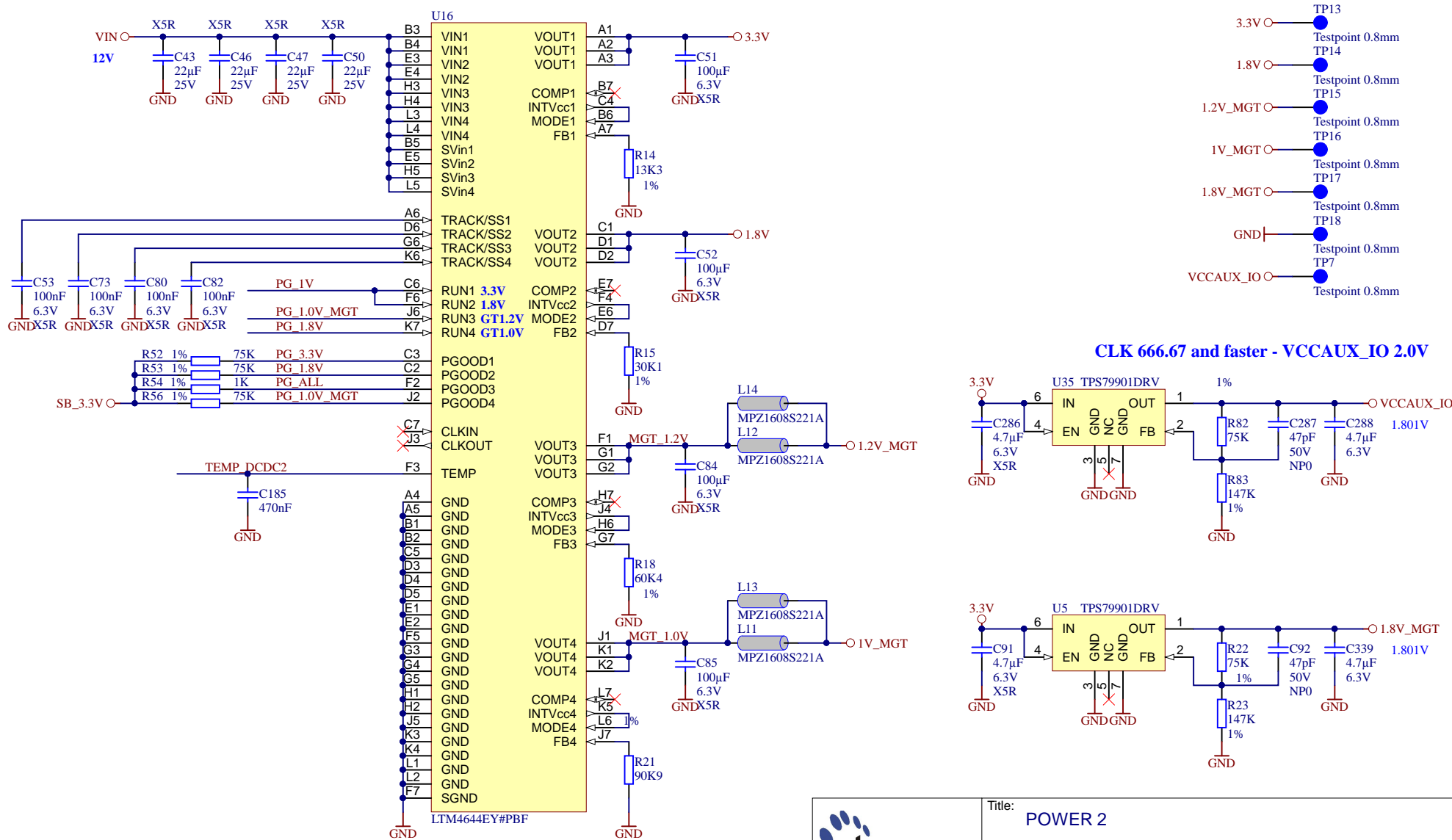
B

C

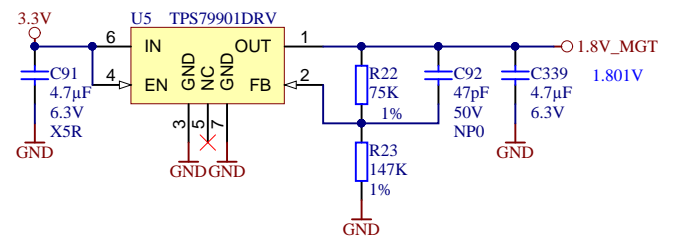
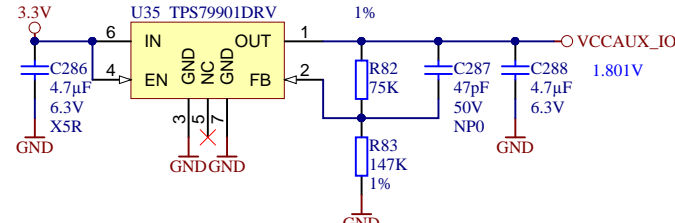
C


D

D



CLK 666.67 and faster - VCCAUX_IO 2.0V



			Title: POWER 2	
A4	Number: TE0783 035-21	Rev. 01		
Date:	15.05.2018	Copyright: Trenz Electronic GmbH	Page30 of 31	
Filename:	POWER2.SchDoc			

1

2

3

4

1

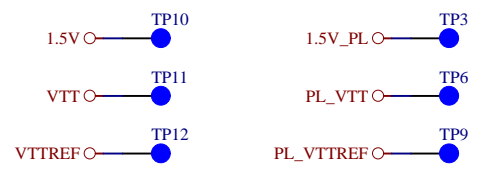
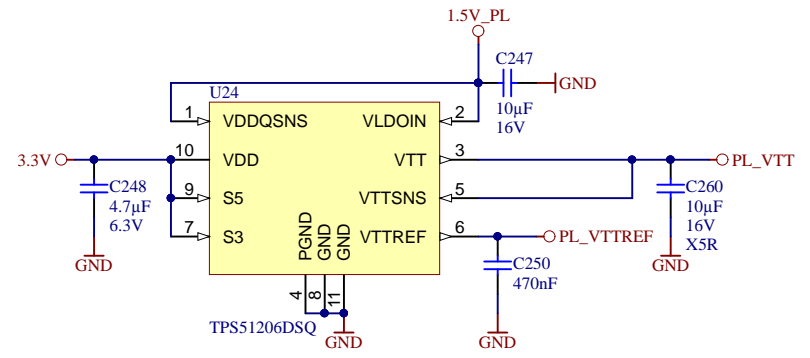
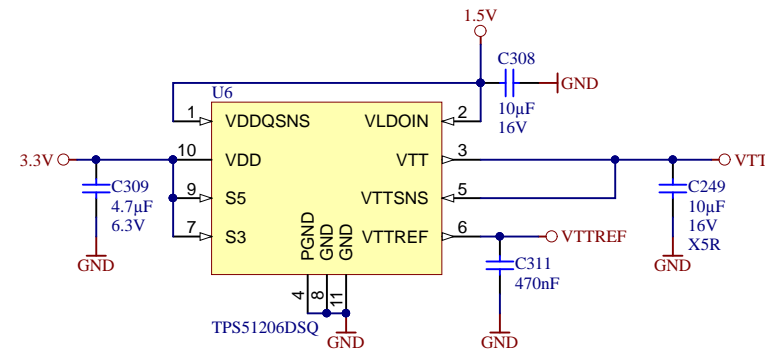
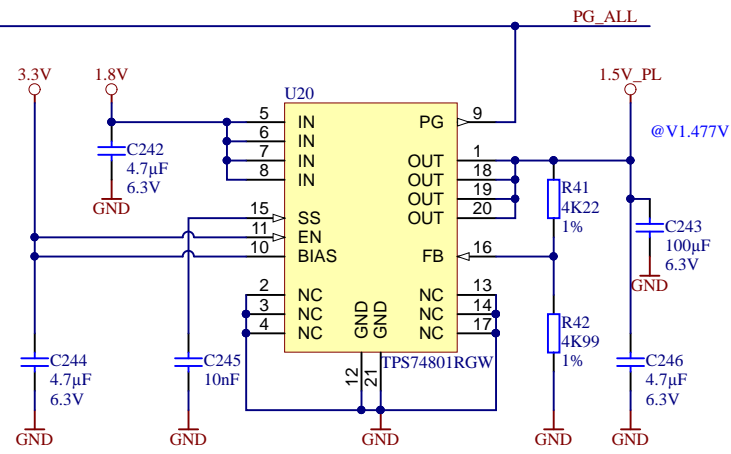
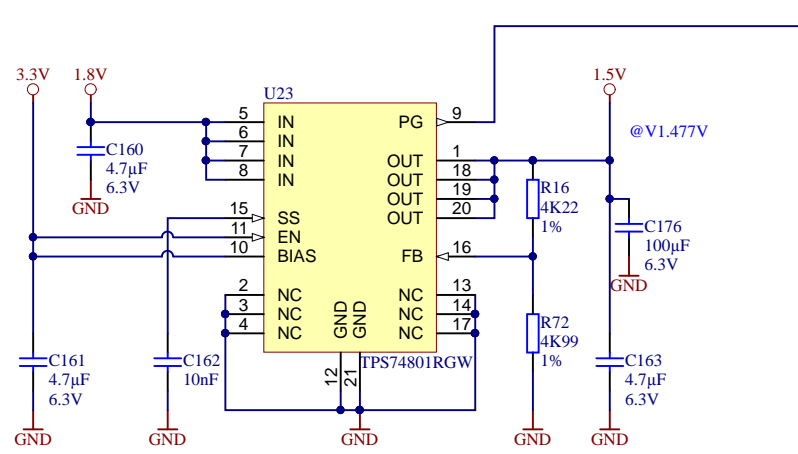
2

3

4

DDR3 PS

DDR3 PL



Title: POWER 2		
A4	Number: TE0783 035-21	Rev. 01
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Filename: POWER3.SchDoc		

1

2

3

4