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U_DDR3-RAM
DDR3-RAM.SchDoc

U_USB-PHY
USB-PHY.SchDoc

U_ETH1
ETH1.SchDoc

U_SOC
SOC.SchDoc

U_CPLD
CPLD.SchDoc

U_POWER2
POWER2.SchDoc

U_Clock
Clock.SchDoc

U_eMMC
eMMC.SchDoc

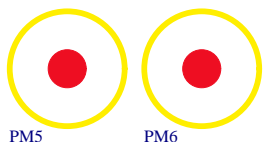
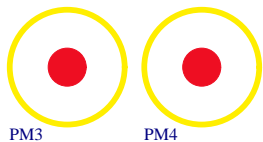
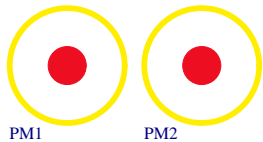
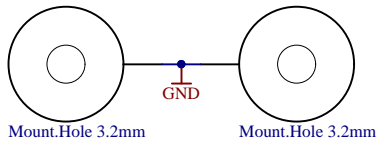
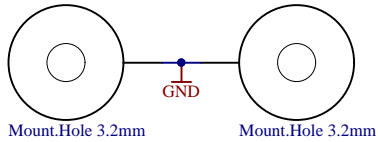
U_Connectors
Connectors.SchDoc

U_POWER
POWER.SchDoc

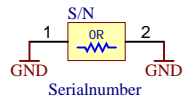
U_POWER3
POWER3.SchDoc

LOGO1
TE Logo PRINT Layer

LOGO PRINT



Serial
Serialnumber 6,3 x 6.3mm



Title: Overview		
A4	Number: TE0783 100-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page1 of 31
Filename: TE0783.SchDoc		

1

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A

A

B

B

C

C

D

D

1

2

3

4

A

A

U_HSMC_CONN_J1
HSMC_CONN_J1.SchDoc



U_HSMC_CONN_J2
HSMC_CONN_J2.SchDoc



U_HSMC_CONN_J3
HSMC_CONN_J3.SchDoc



B

B

C

C

D


D

1

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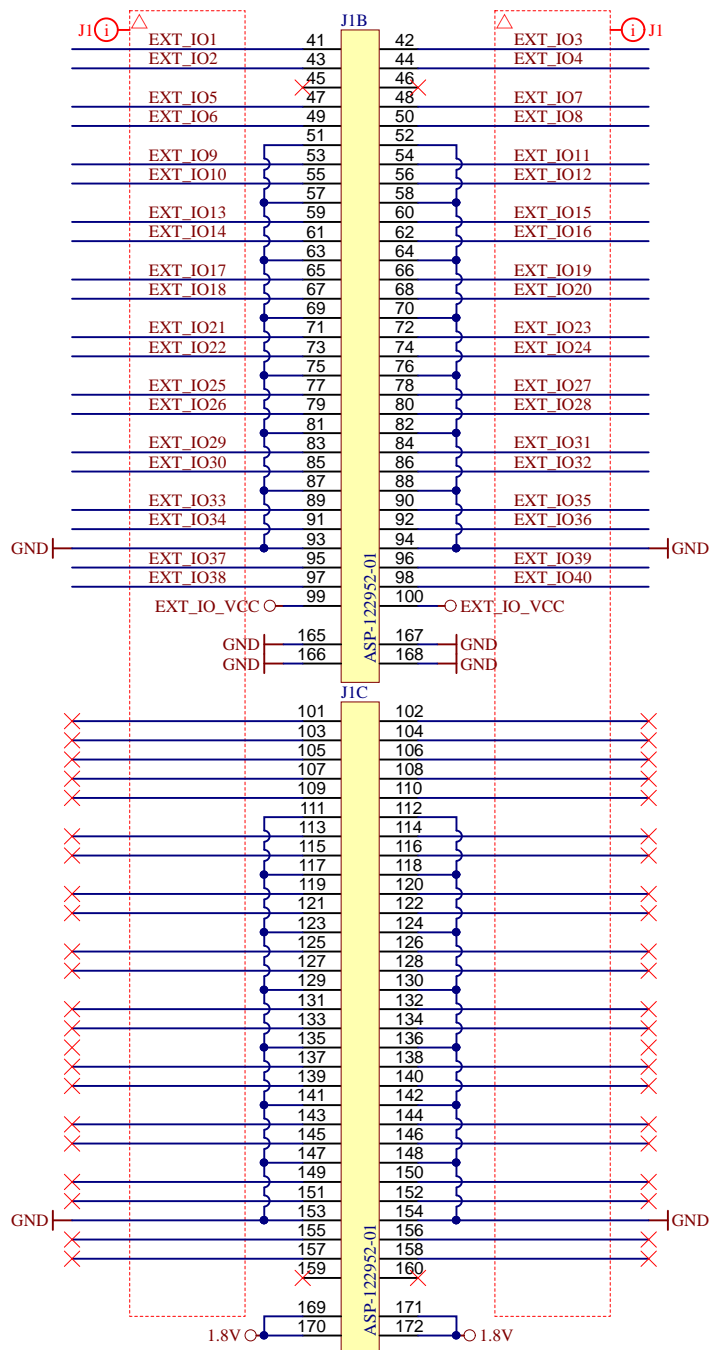
	Title: Connectors		
	A4	Number: TE0783 100-2I	Rev. 01
	Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 2 of 31
	Filename: Connectors.SchDoc		

1

2

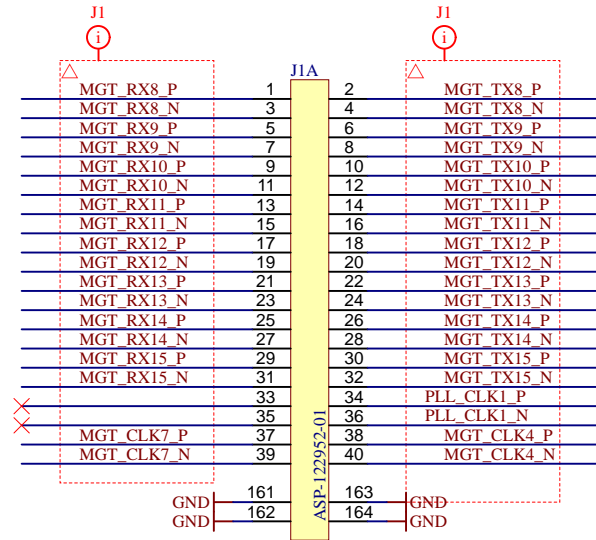
3

4



Next signals has different functionality in TE0782 and TEBT0782.

TE0782
 J1_TX20_N
 J1_TX20_P
 J1_TX21_N
 J1_TX21_P



Next signals has different functionality in TE0782 and TEBT0782.

TE0782
 J1_RX20_N
 J1_RX20_P



Title: HSMC_Connector_J1		
A4	Number: TE0783 100-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page3 of 31
Filename: HSMC_CONN_J1.SchDoc		

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A

A

B

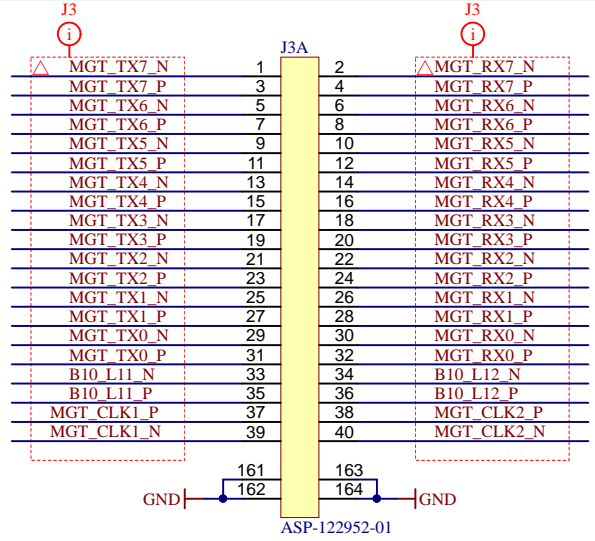
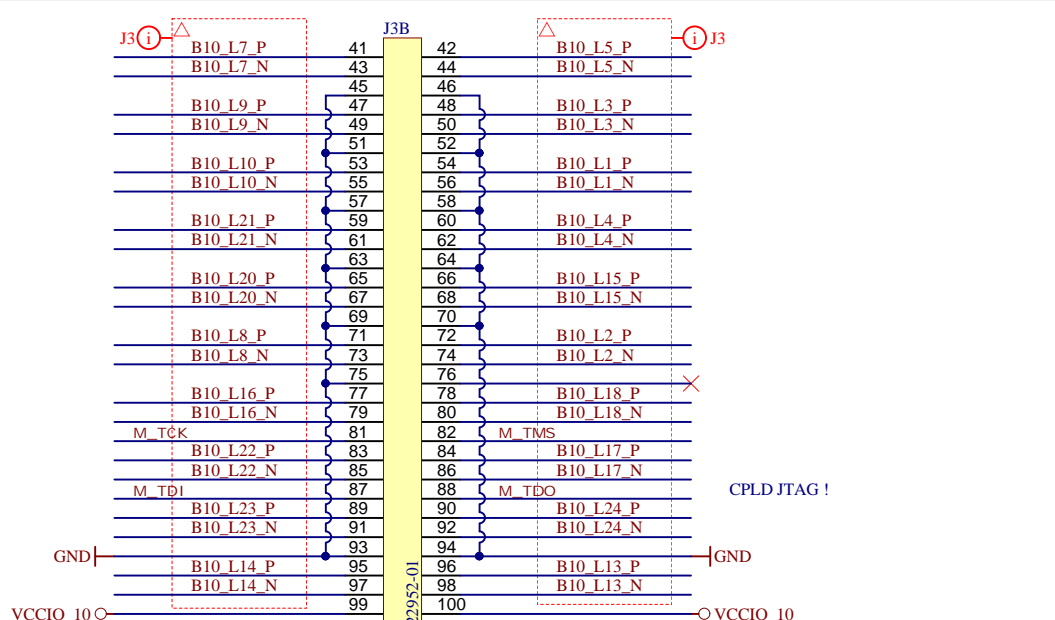
B

C

C

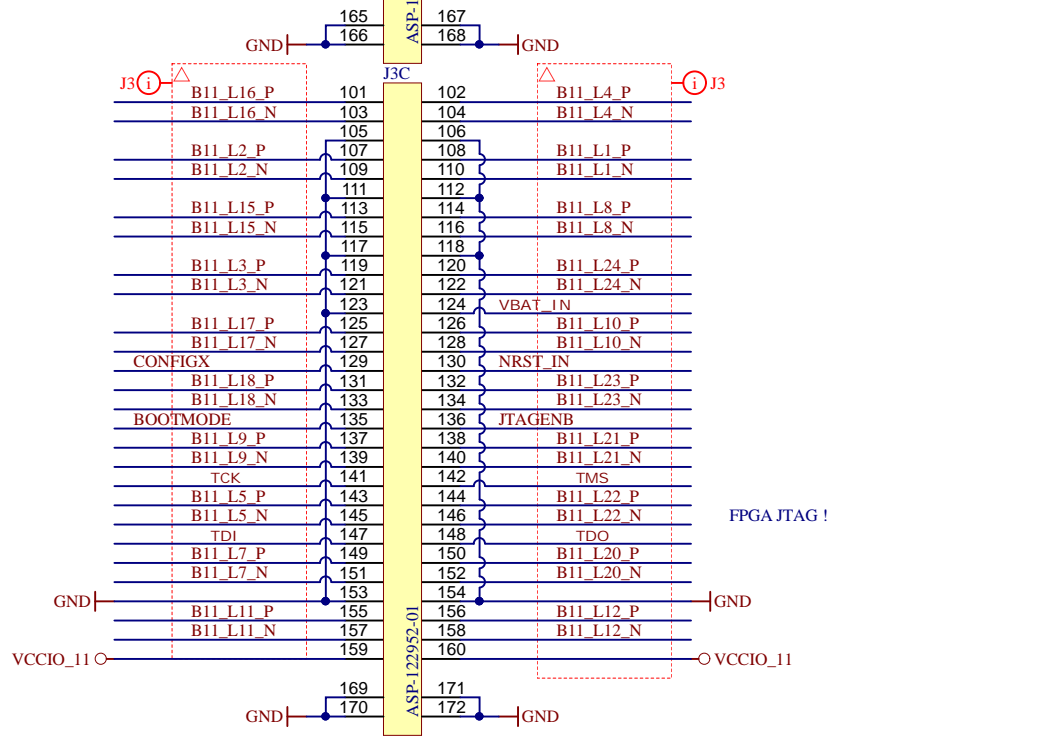
D

D



Next signals has different functionality in TE0782 and TEBT0782.

S15328_CLK1_P
S15328_CLK1_N



Title: HSMC_Connector_J3		
A4	Number: TE0783 100-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 4 of 31
Filename: HSMC_CONN_J3.SchDoc		

A

B

C

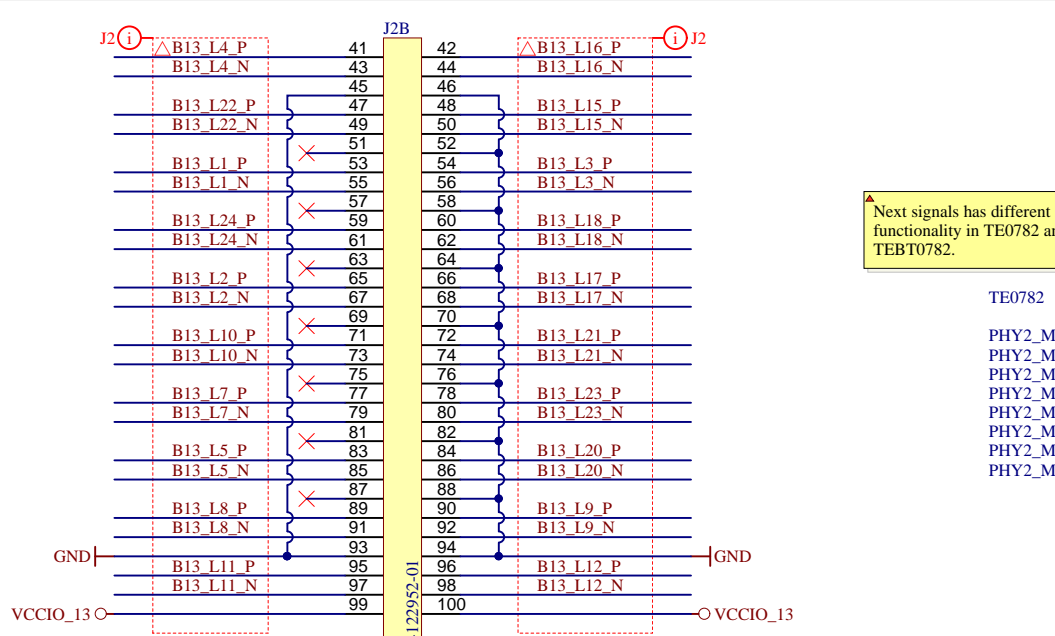
D

A

B

C

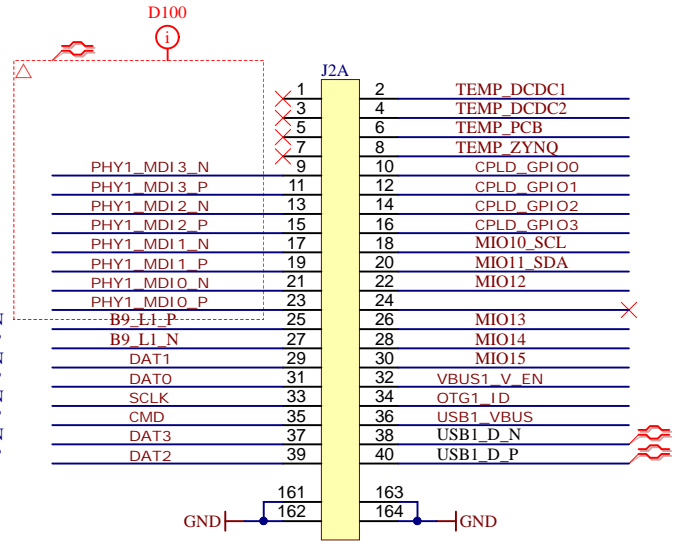
D



Next signals has different functionality in TE0782 and TEBT0782.

TE0782

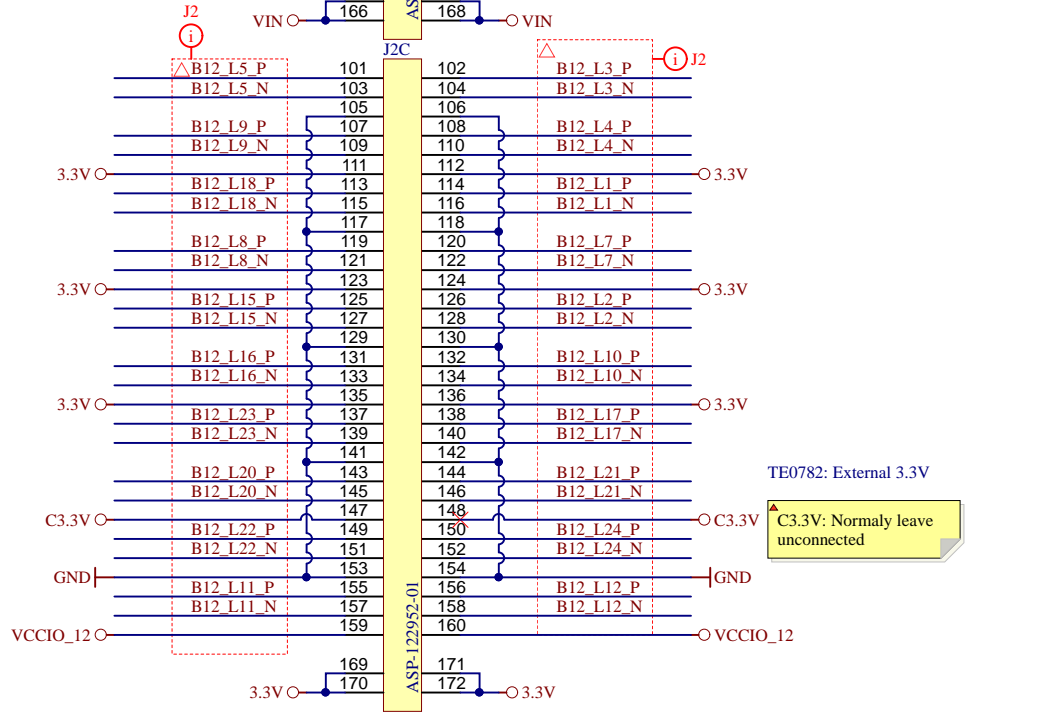
- PHY2_MDI3_N
- PHY2_MDI3_P
- PHY2_MDI2_N
- PHY2_MDI2_P
- PHY2_MDI1_N
- PHY2_MDI1_P
- PHY2_MDI0_N
- PHY2_MDI0_P



Next signals has different functionality in TE0782 and TEBT0782.

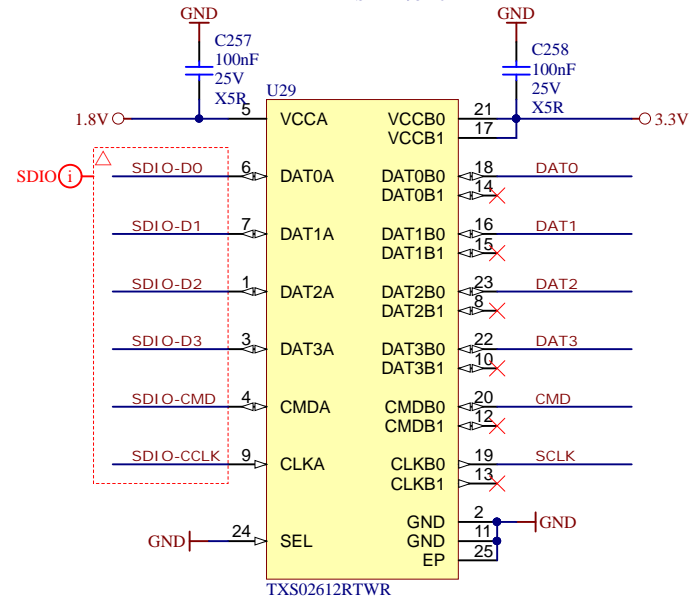
TE0782

- CPLD_GPIO4
- CPLD_GPIO5
- OTG2_ID
- USB2_VBUS
- USB2_D_N
- USB2_D_P
- VBUS2_V_EN



TE0782: External 3.3V

C3.3V: Normally leave unconnected



SDCARD

- DAT0
- DAT1
- DAT2
- DAT3
- CMD
- SCLK



Title: HSMC_Connector_J2		
A4	Number: TE0783 100-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page5 of 31
Filename: HSMC_CONN_J2.SchDoc		

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U_PS-DDR
PS-DDR.SchDoc



U_B9
B9.SchDoc



U_MIO-BANKS
MIO-BANKS.SchDoc



U_B10
B10.SchDoc



U_HP-BANKS
HP-BANKS.SchDoc



U_B11
B11.SchDoc



U_FPGA-MGT
FPGA-MGT.SchDoc



U_B12
B12.SchDoc



U_FPGA-CFG
FPGA-CFG.SchDoc



U_B13
B13.SchDoc



U_FPGA-PWR
FPGA-PWR.SchDoc



A

A

B


B

C

C

D

D

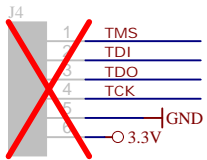
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	A4	Number: TE0783 100-2I	Rev. 01
	Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 6 of 31
	Filename: SOC.SchDoc		

1

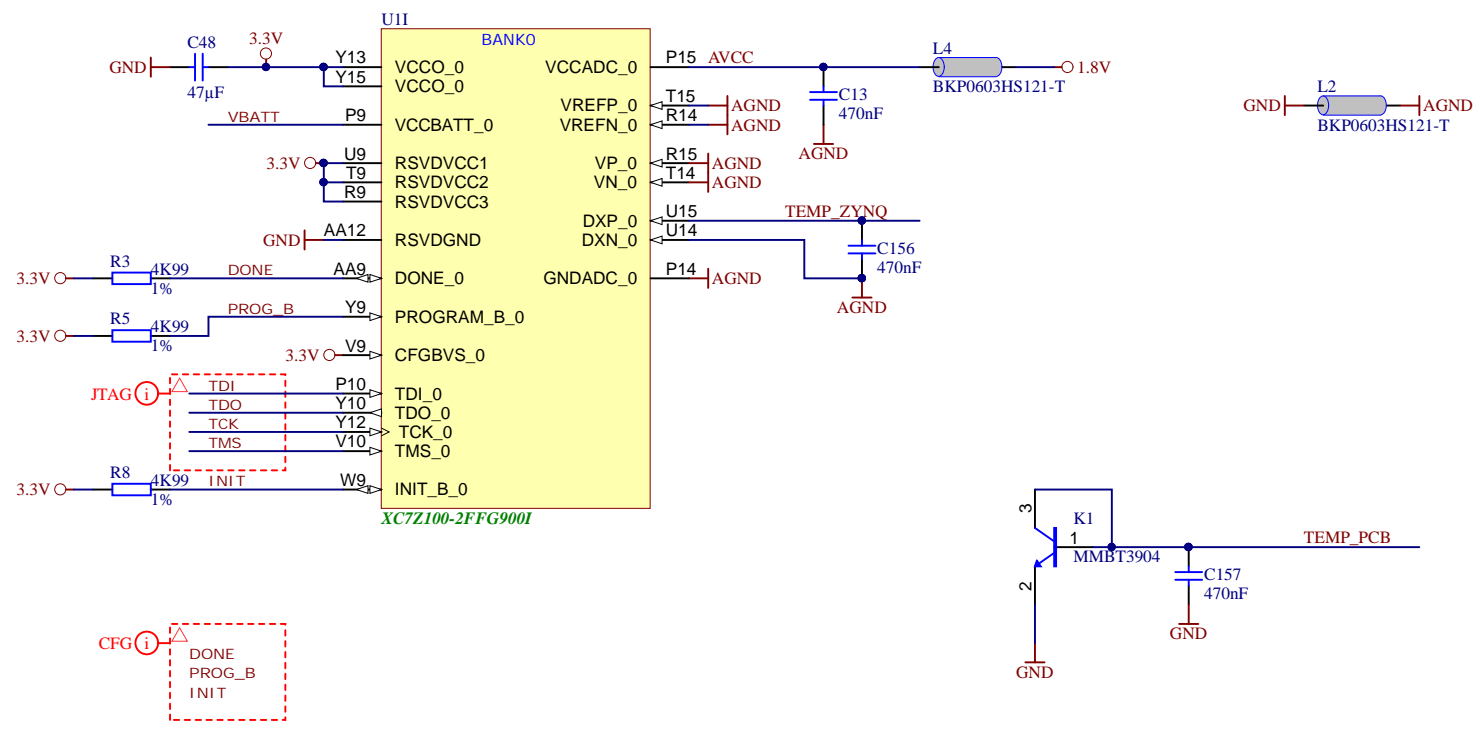
2

3

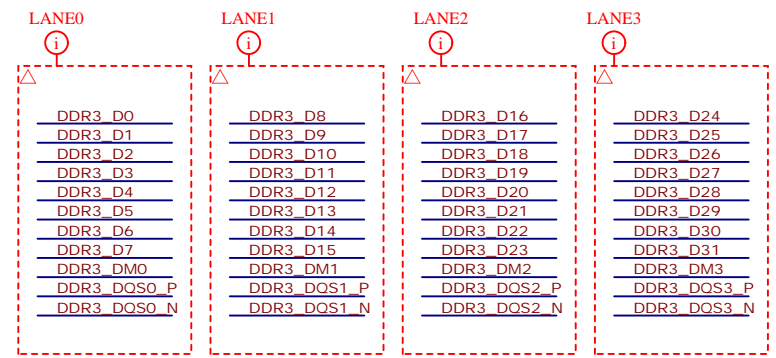
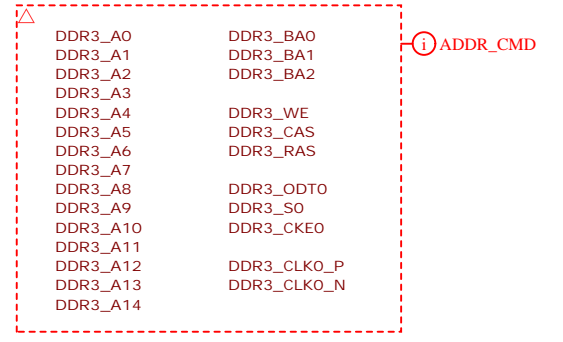
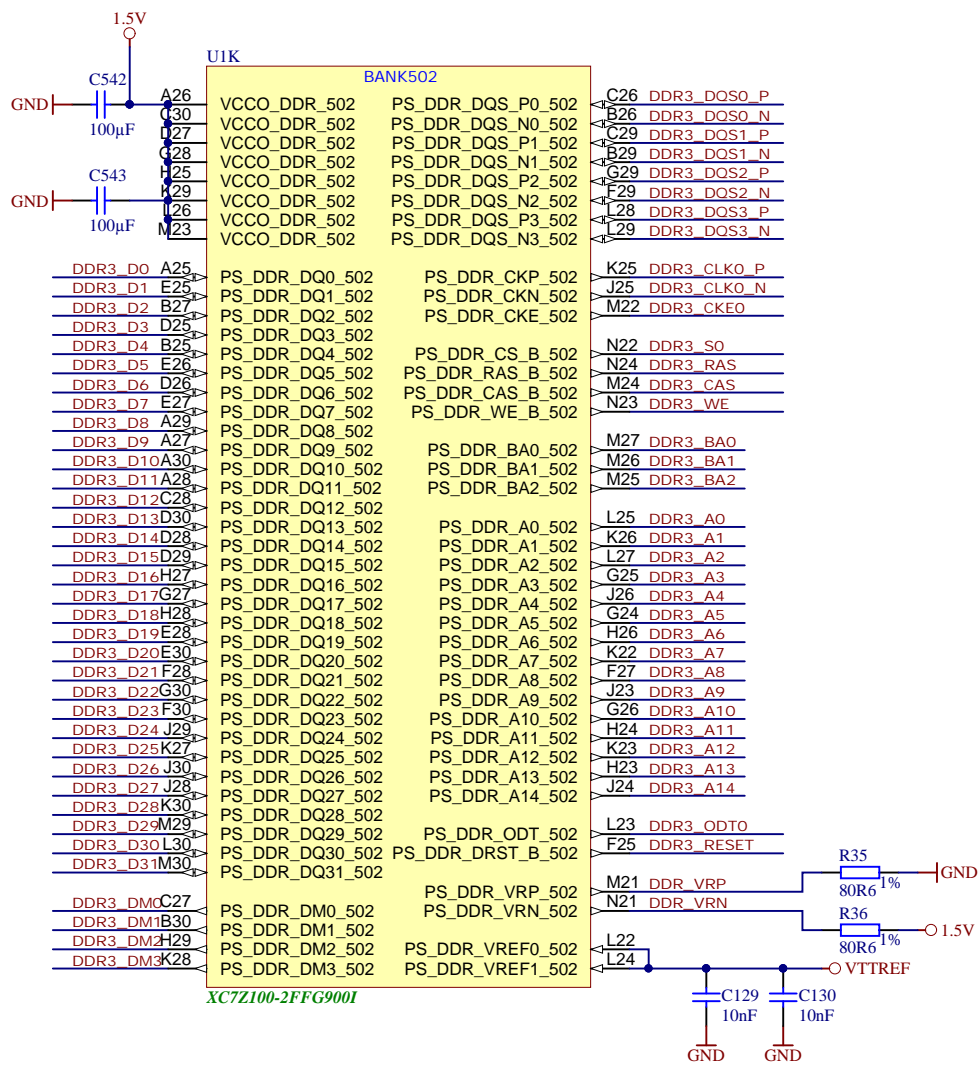
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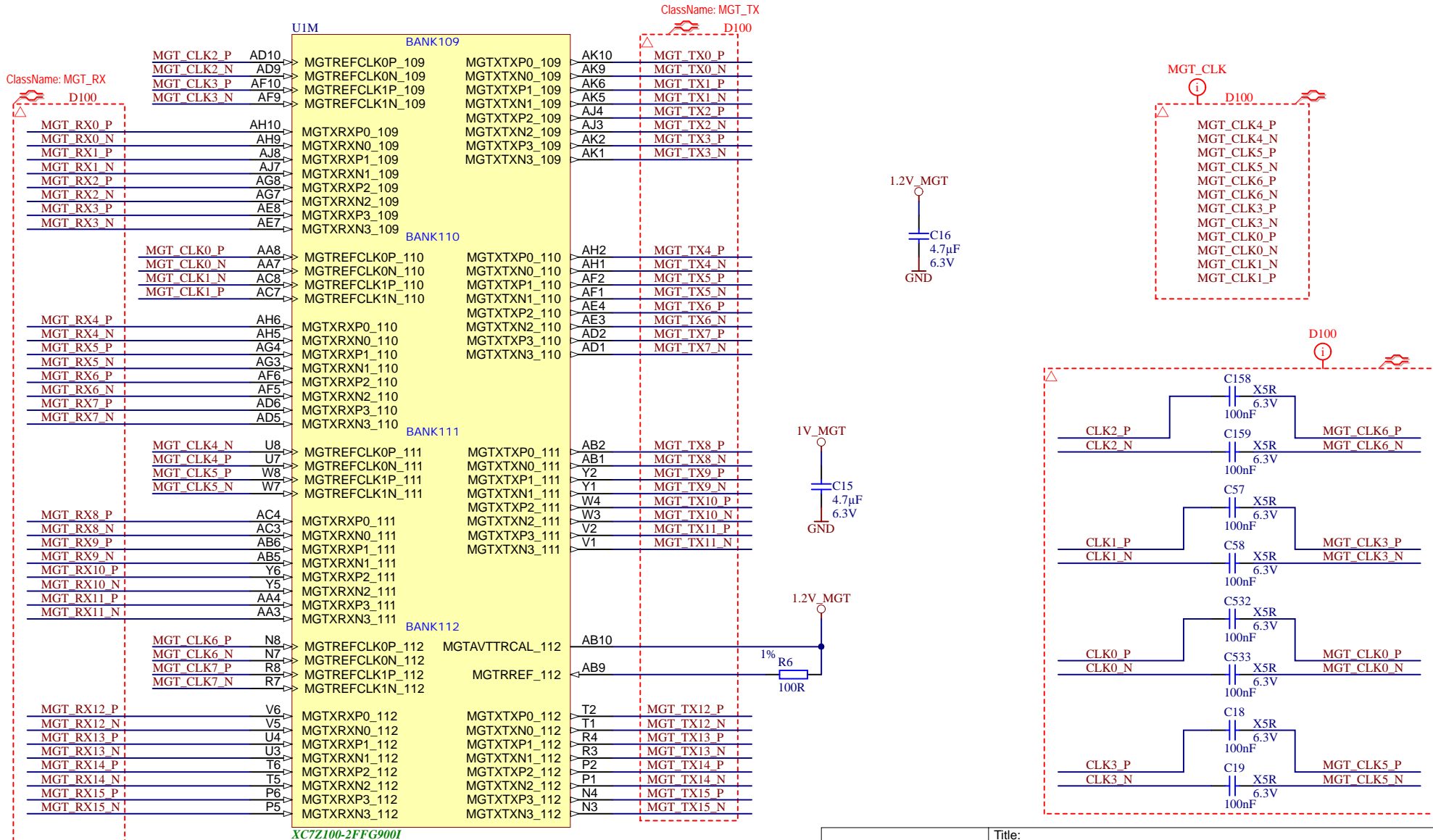
Placeholder 1 row 6 pin header



	Title: FPGA Configuration		
	A4	Nummer: TE0783 100-2I	Rev. 01
	Datum: 15.05.2018	Zeichner: Trenz Electronic GmbH	Blatt 7 von 31
	Filename: FPGA-CFG.SchDoc		



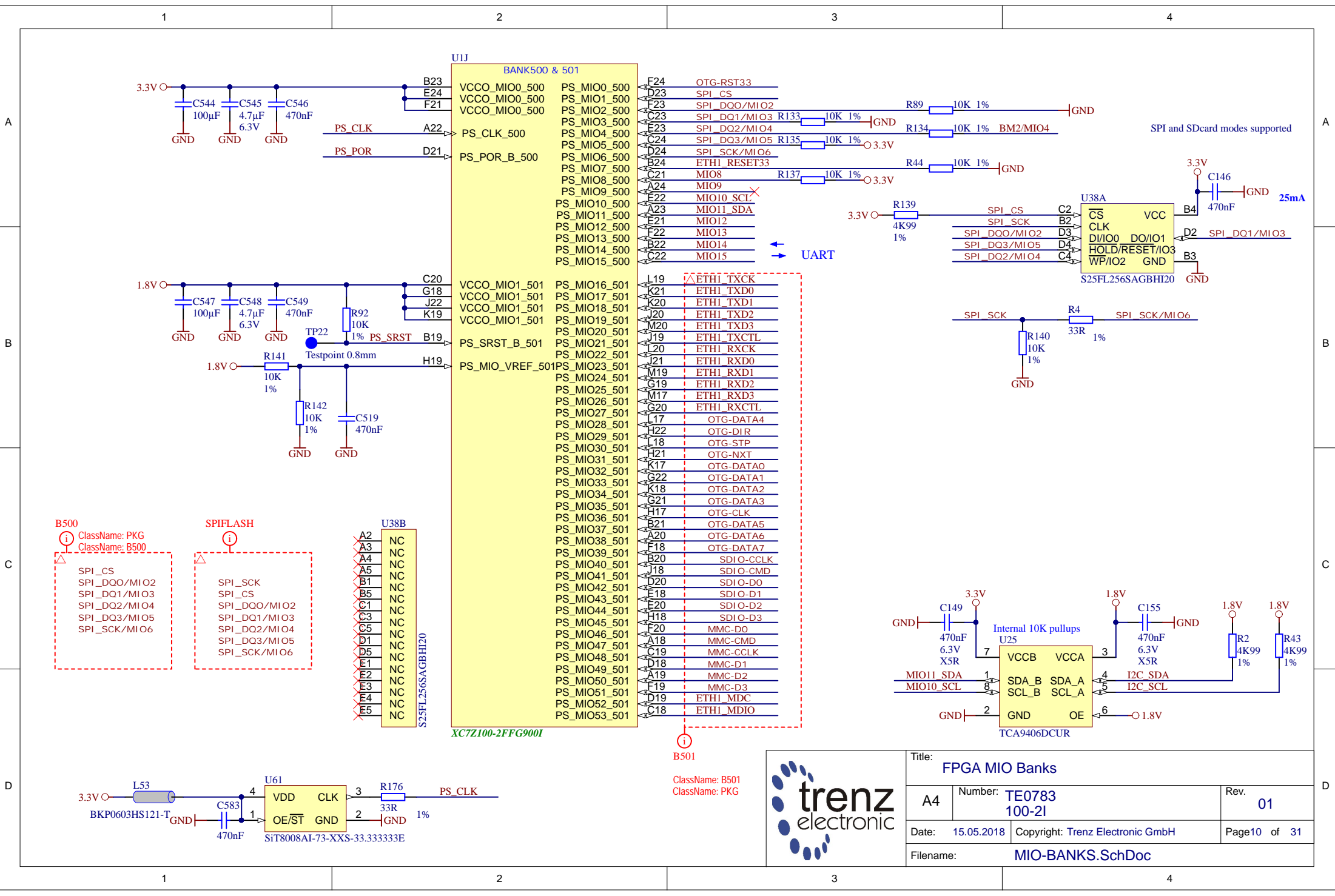
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A4	Number: TE0783 100-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 8 of 31
Filename: PS-DDR.SchDoc		



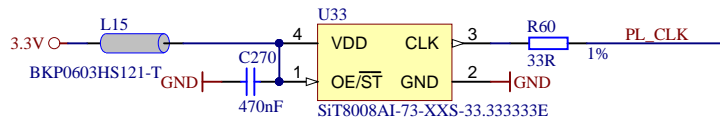
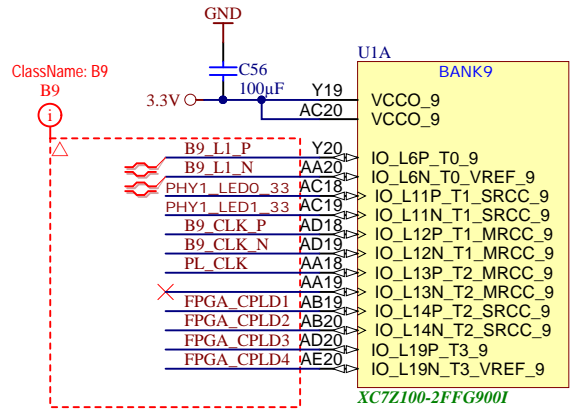

XC7Z100-2FFG9001



Title: FPGA MGT		
A4	Number: TE0783 100-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 9 of 31
Filename: FPGA-MGT.SchDoc		

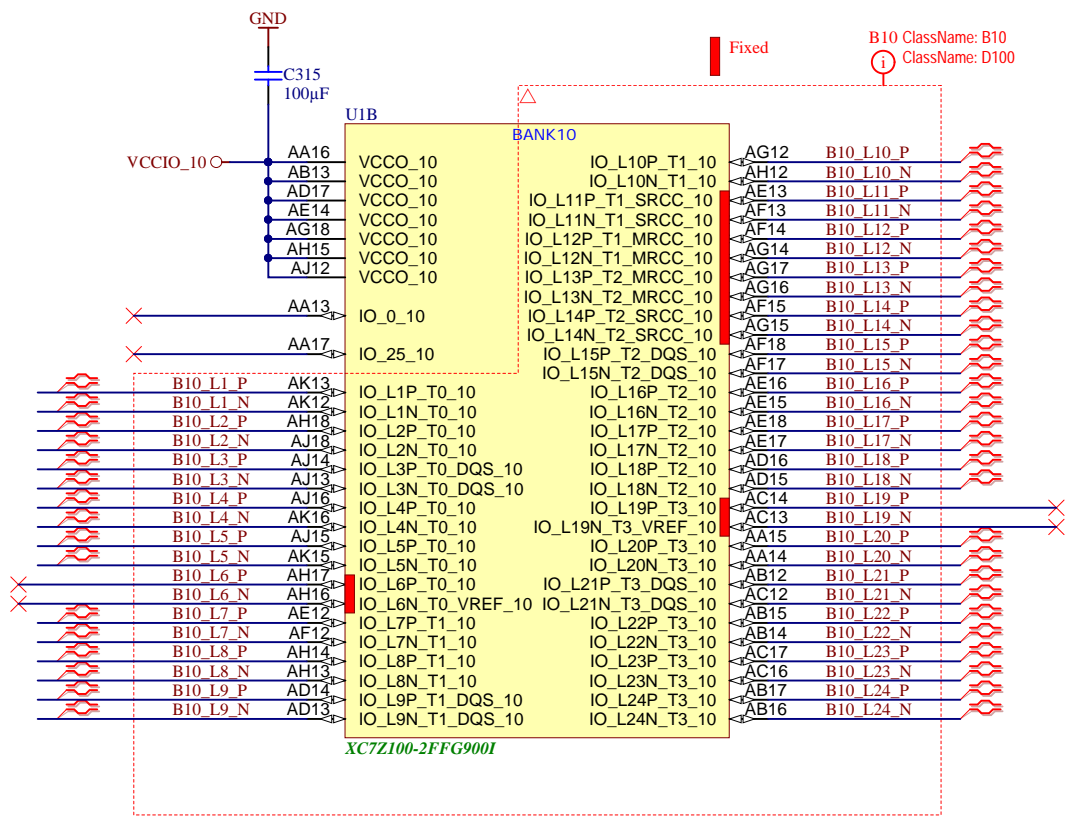


Title: FPGA MIO Banks			
A4	Number: TE0783 100-21	Rev. 01	
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 10 of 31	
Filename: MIO-BANKS.SchDoc			

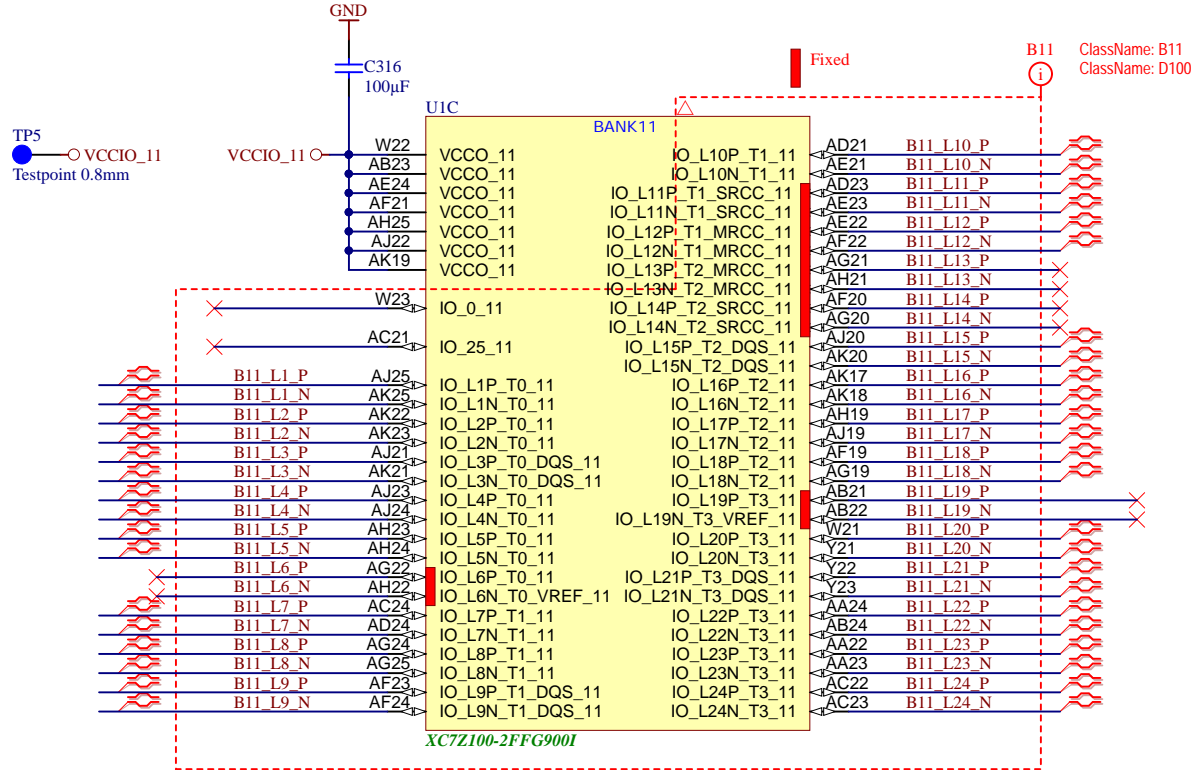




Title: FPGA B9		
A4	Number: TE0783 100-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 11 of 31
Filename: B9.SchDoc		


TP4
 ● VCCIO_10
 ○ Testpoint 0.8mm

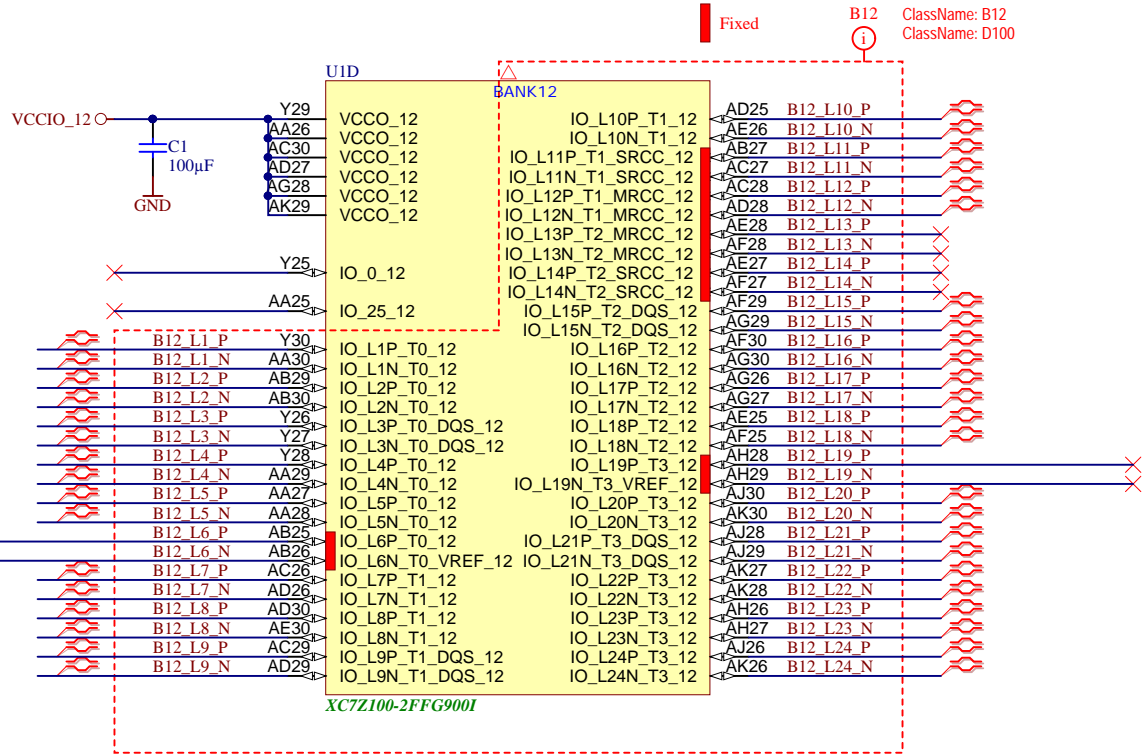


Title: FPGA B10		
A4	Number: TE0783 100-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 12 of 31
Filename: B10.SchDoc		



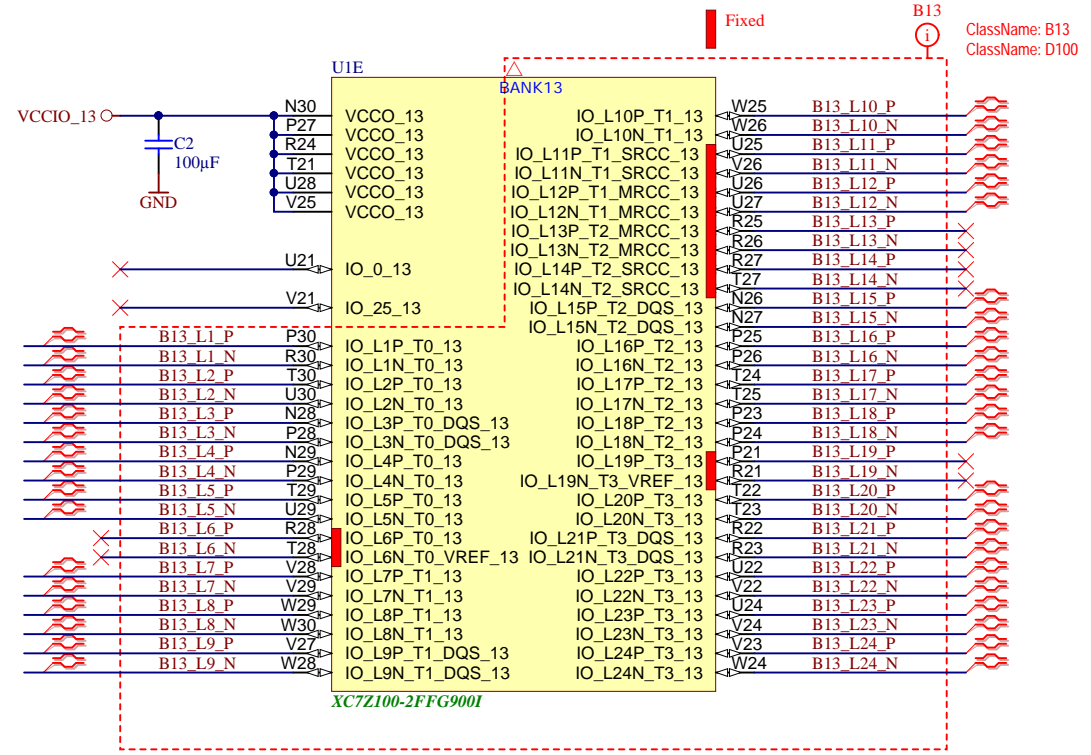
		Title: FPGA B11	
		A4	Number: TE0783 100-2I
Date: 15.05.2018		Copyright: Trenz Electronic GmbH	
Filename: B11.SchDoc		Page 13 of 31	

TP1
 VCCIO_12
 Testpoint 0.8mm



Title: FPGA B12		
A4	Number: TE0783 100-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 14 of 31
Filename: B12.SchDoc		

TP2
 ● ○ VCCIO_13
 Testpoint 0.8mm



Title: FPGA B13		
A4	Number: TE0783 100-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 15 of 31
Filename: B13.SchDoc		

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U_B33
B33.SchDoc



U_B34
B34.SchDoc



U_B35
B35.SchDoc



U_DDR3-RAM-PL1
DDR3-RAM-PL1.SchDoc



U_DDR3-RAM-PL2
DDR3-RAM-PL2.SchDoc



A

A

B

B

C

C

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D



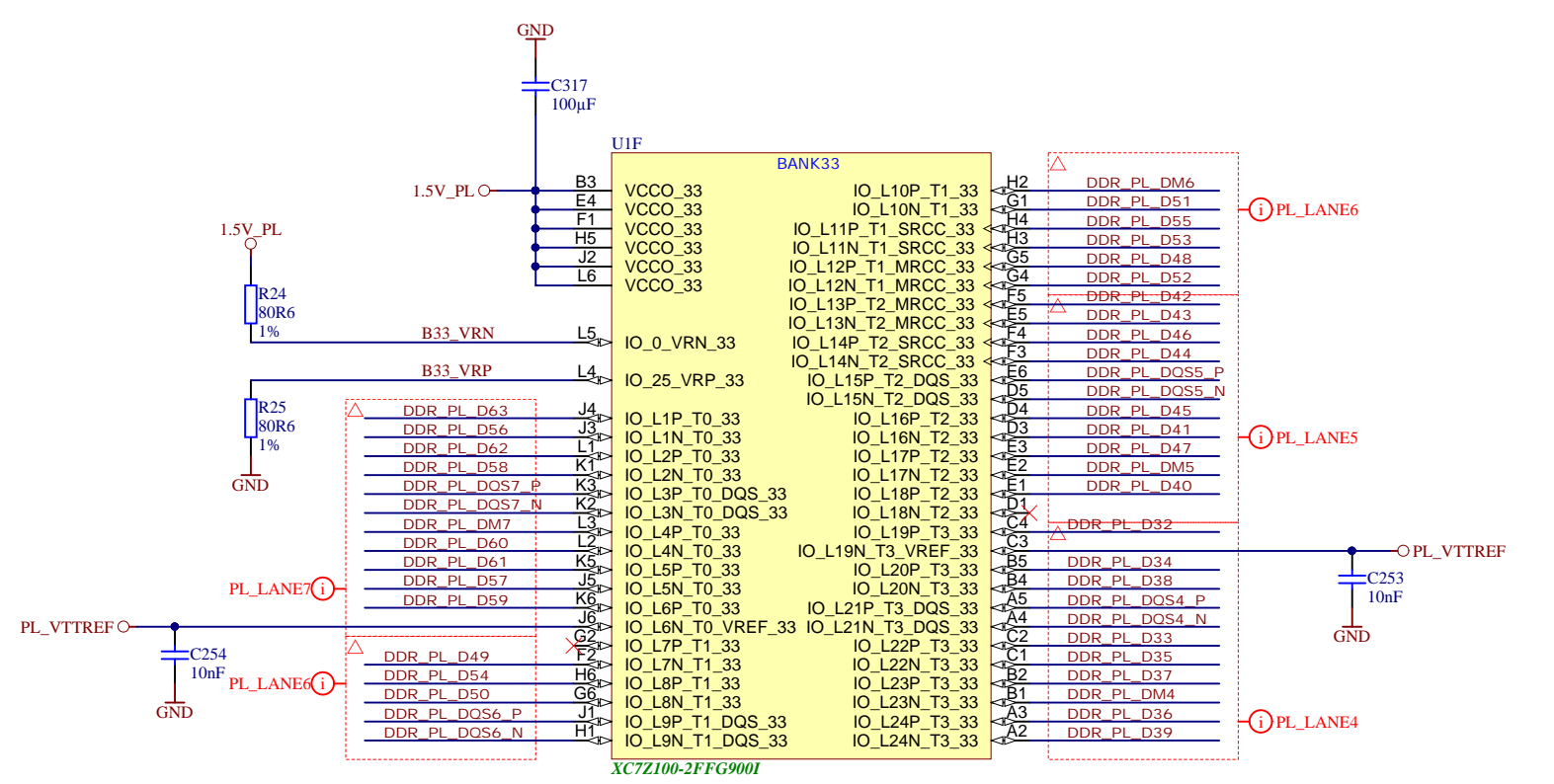
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A4	Number: TE0783 100-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 16 of 31
Filename: HP-BANKS.SchDoc		

1

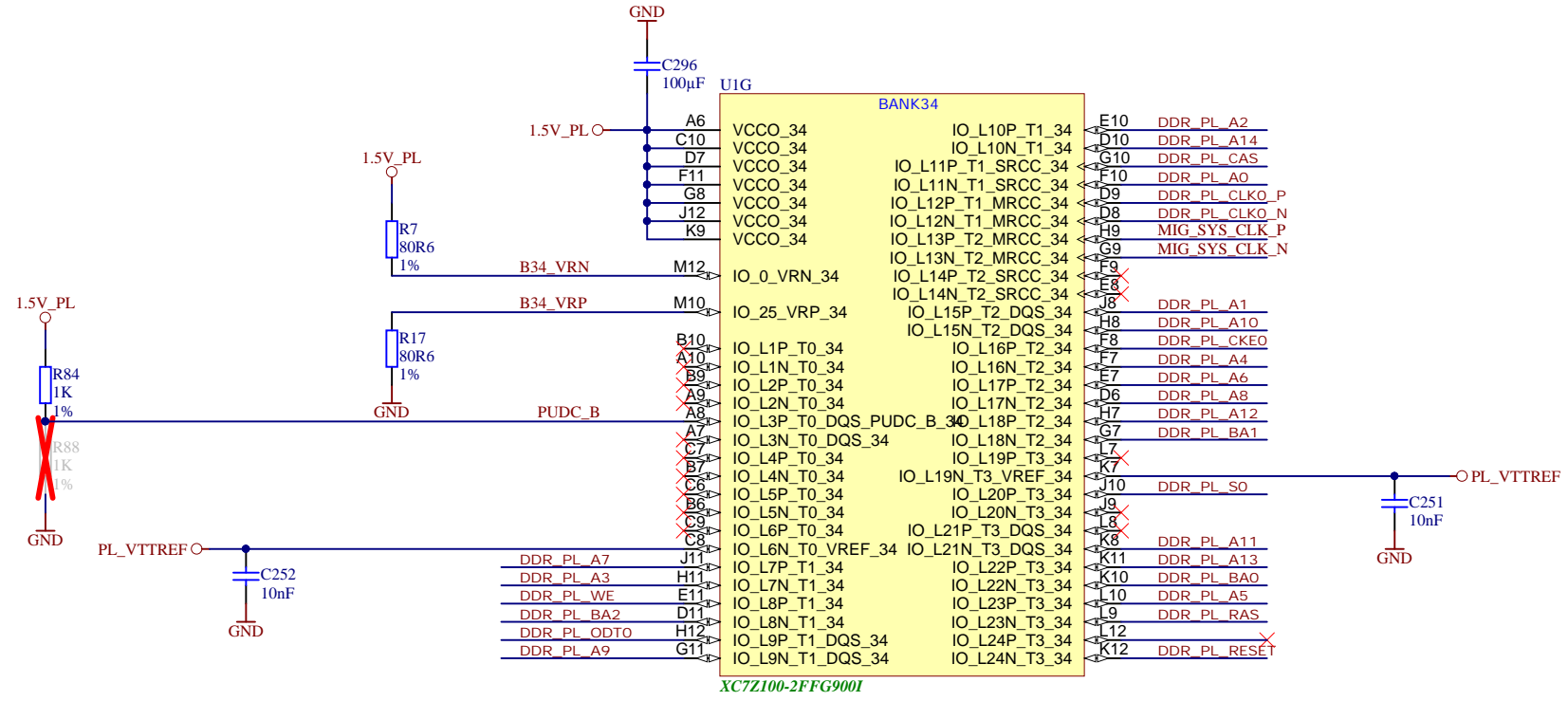
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3

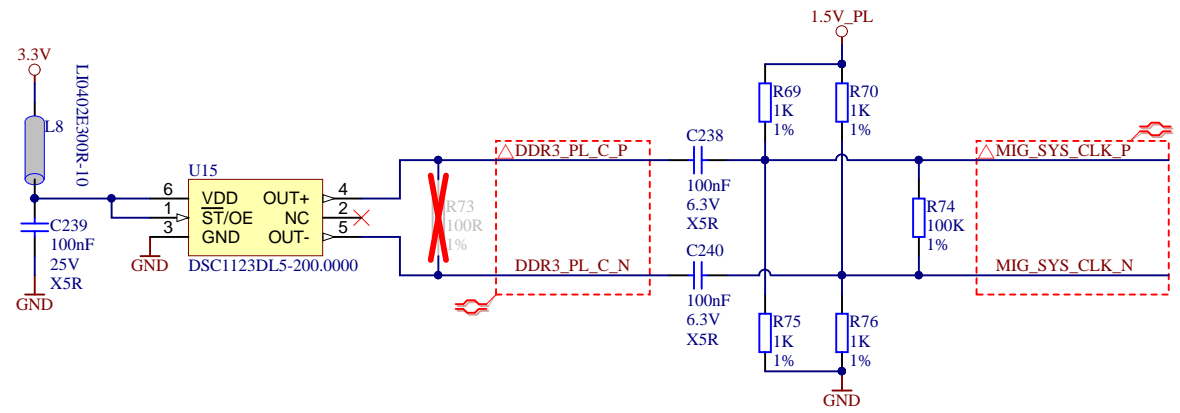
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	Title: FPGA B33		
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	Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 17 of 31
	Filename: B33.SchDoc		



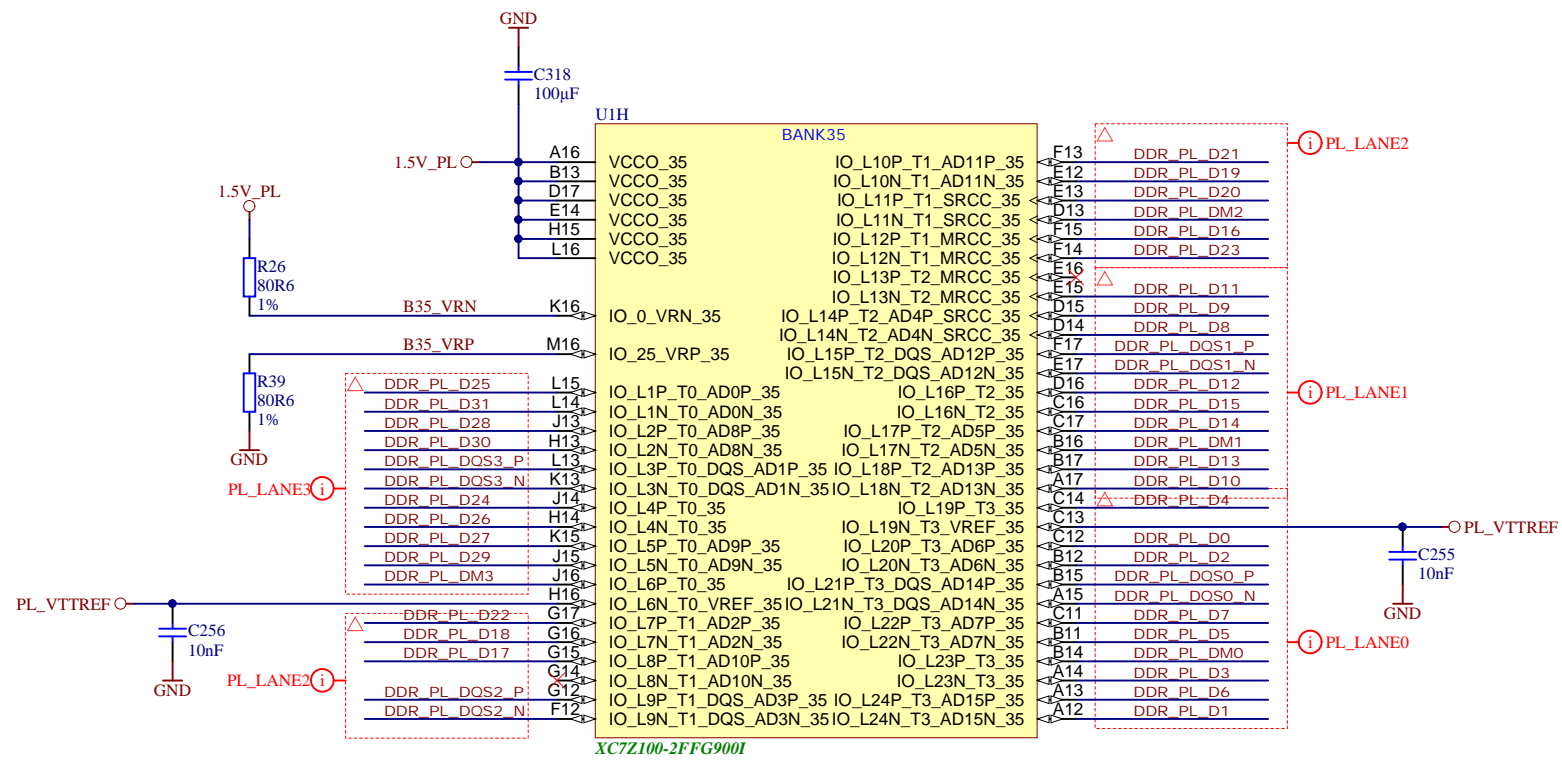
XC7Z100-2FFG900I



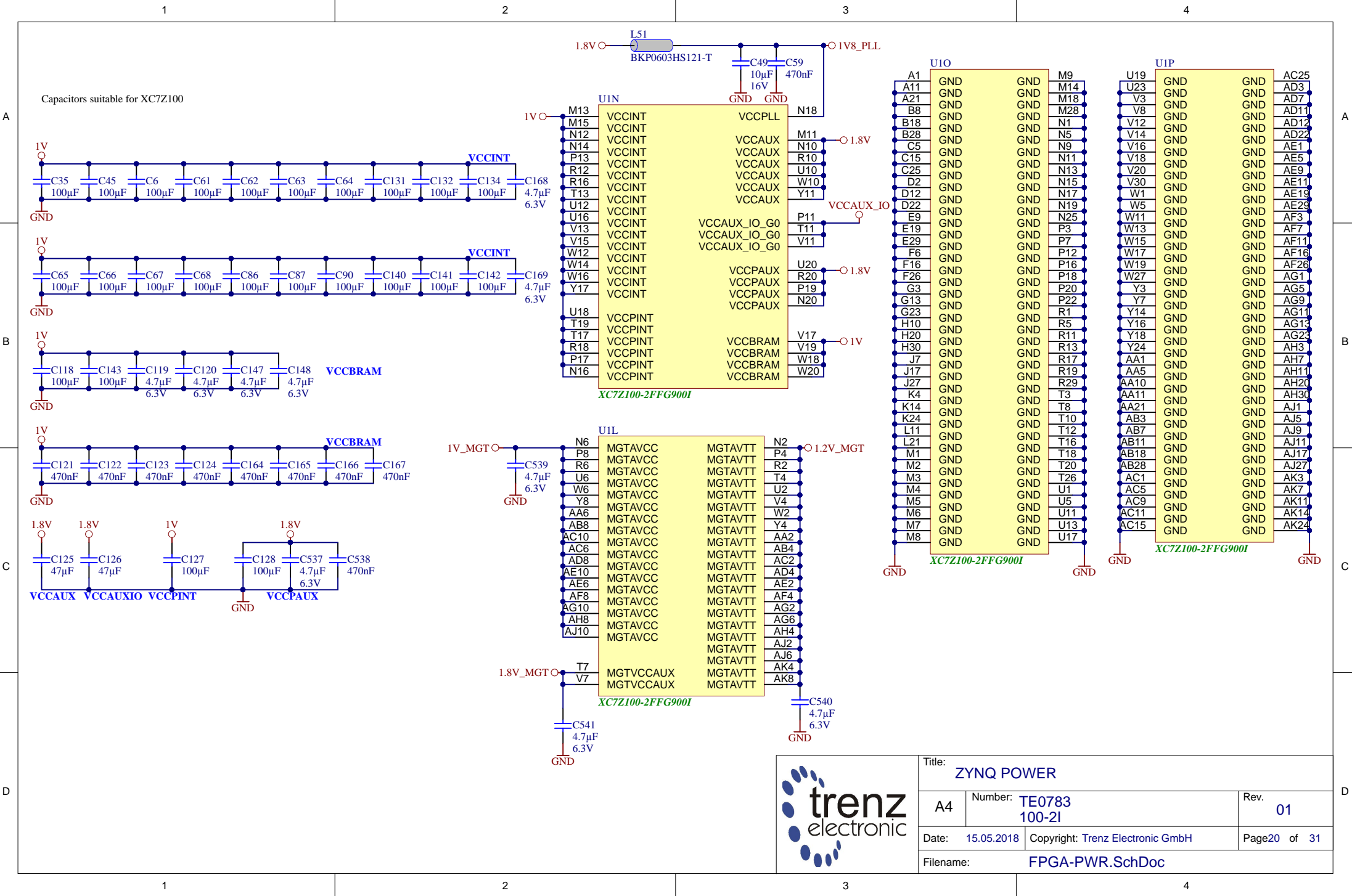
Check clock source. R74 100R changed to 100K



Title: FPGA B34		
A4	Number: TE0783 100-2I	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page18 of 31
Filename: B34.SchDoc		



	Title: FPGA B35		
	A4	Number: TE0783 100-2I	Rev. 01
	Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 19 of 31
	Filename: B35.SchDoc		



Title: ZYNQ POWER		
A4	Number: TE0783 100-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page20 of 31
Filename: FPGA-PWR.SchDoc		

A

A

B

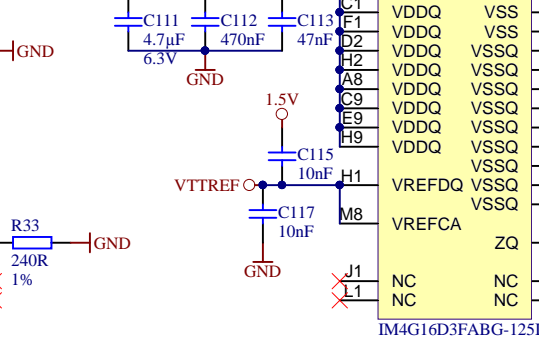
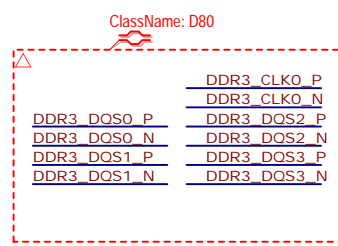
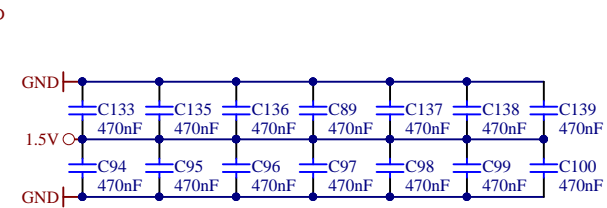
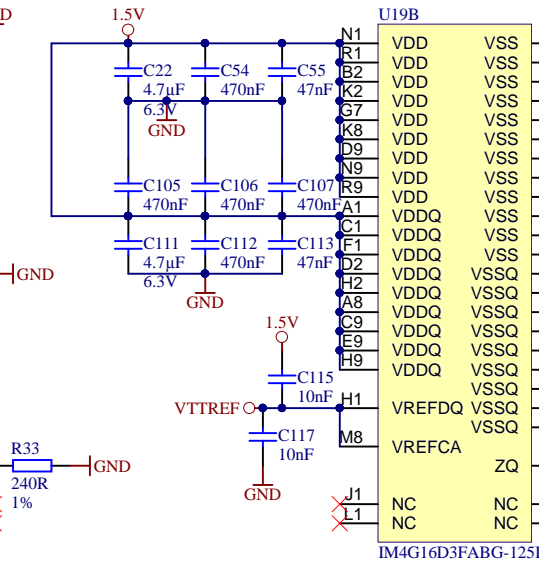
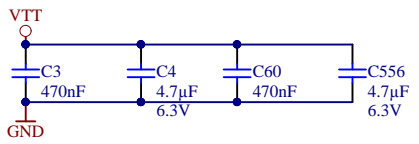
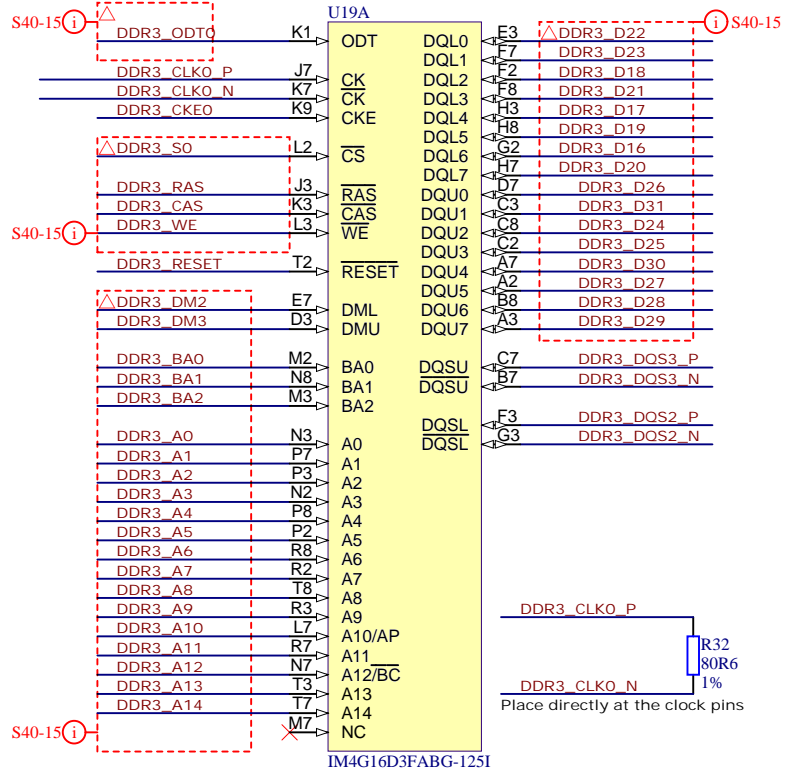
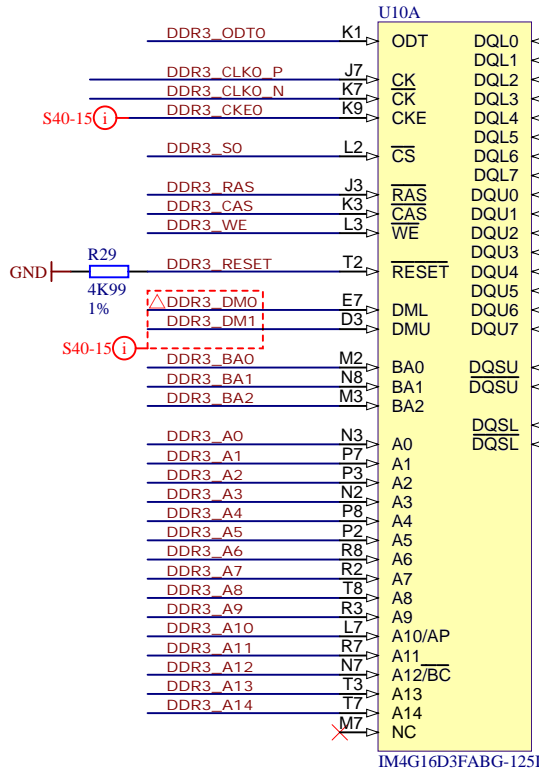
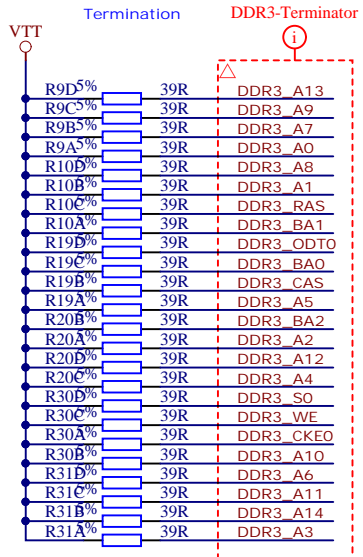
B

C

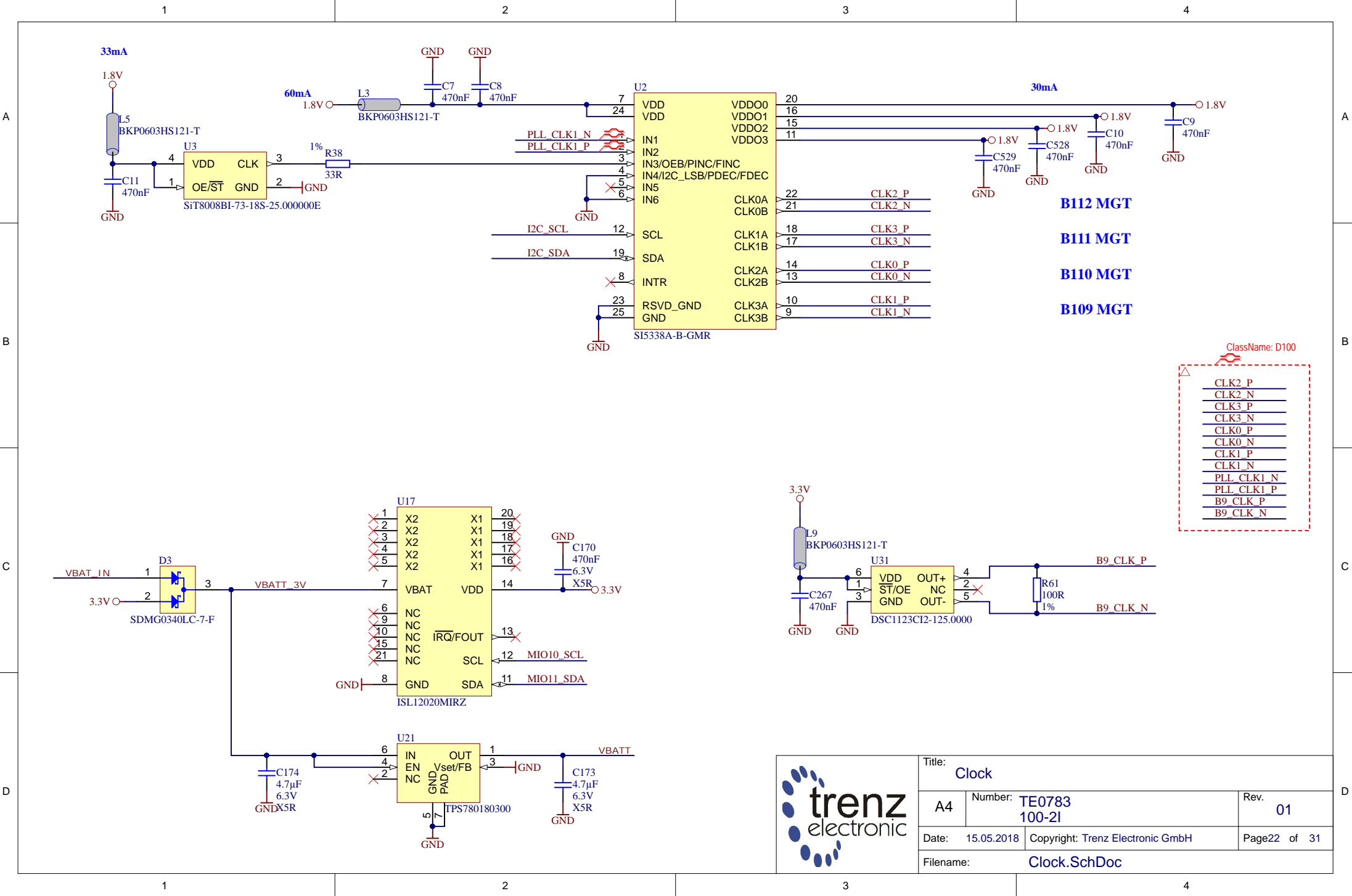
C

D

D



Title: DDR3 RAM PS		
A4	Number: TE0783 100-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 21 of 31
Filename: DDR3-RAM.SchDoc		



- ClassName: D100
- CLK2_P
 - CLK2_N
 - CLK3_P
 - CLK3_N
 - CLK0_P
 - CLK0_N
 - CLK1_P
 - CLK1_N
 - PLL_CLK1_N
 - PLL_CLK1_P
 - B9_CLK_P
 - B9_CLK_N



Title: Clock		
A4	Number: TE0783 100-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page22 of 31
Filename: Clock.SchDoc		

A

A

B

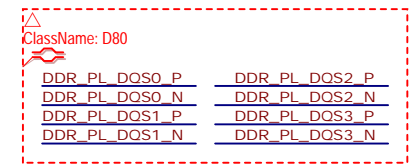
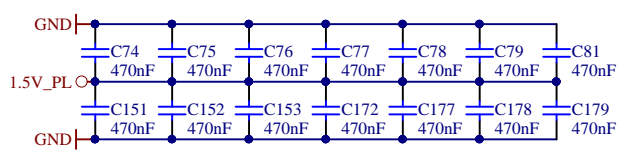
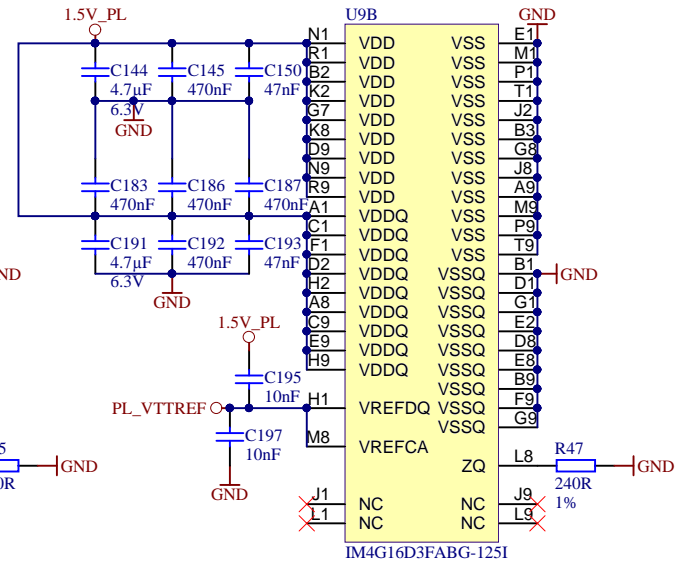
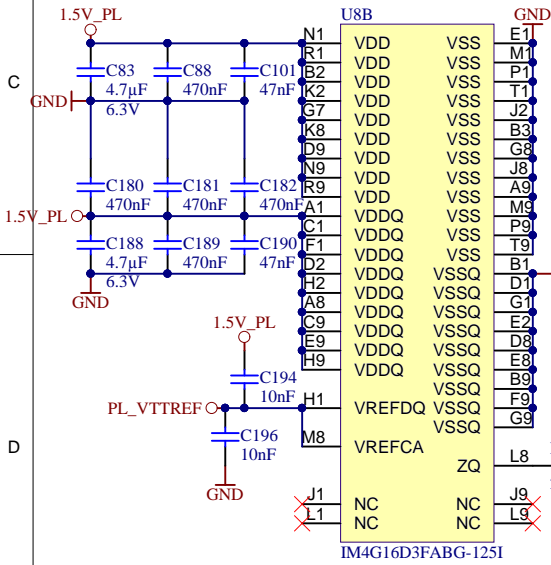
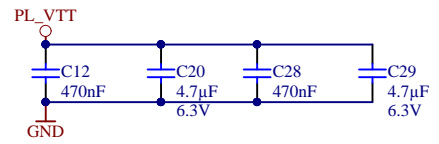
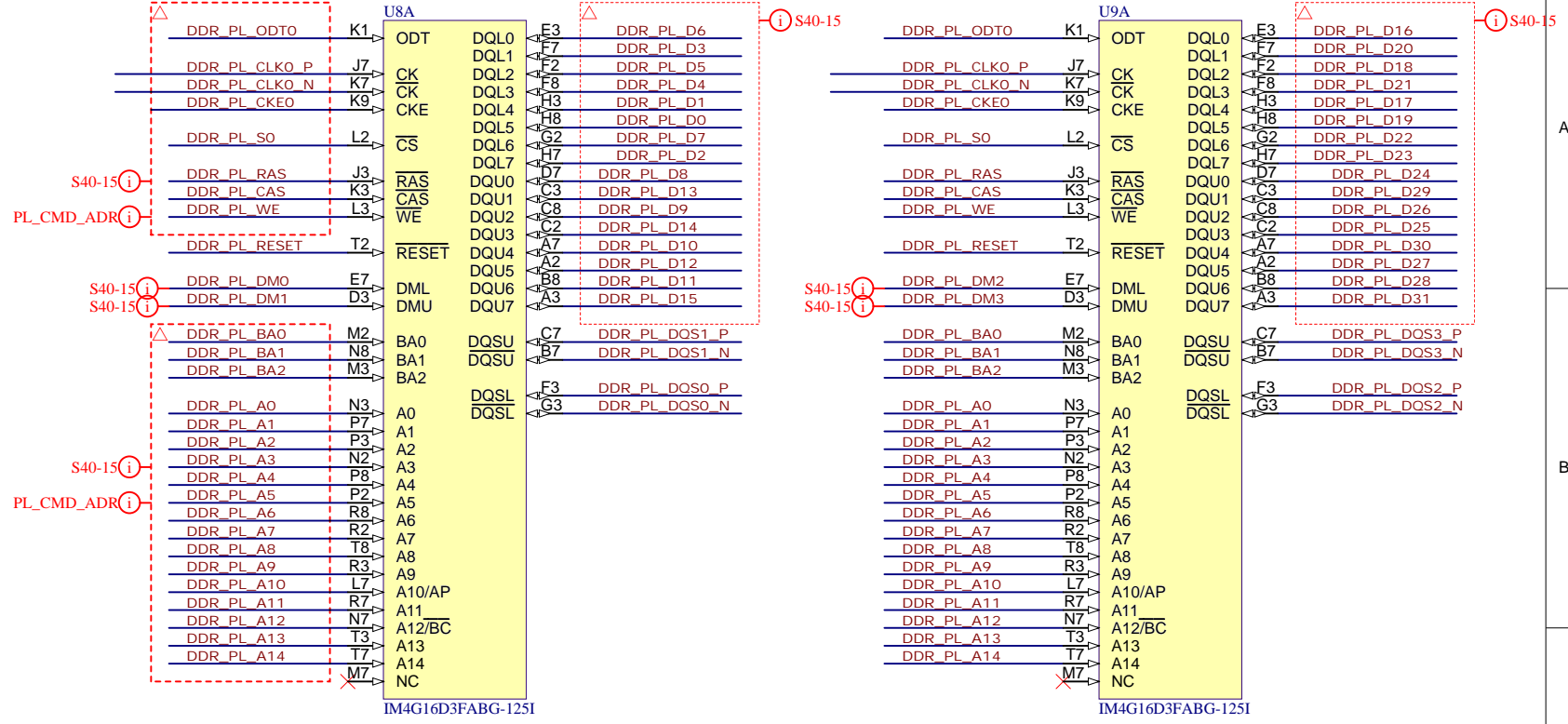
B

C

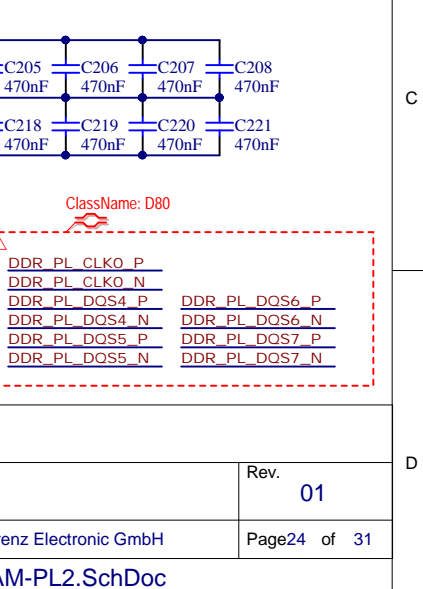
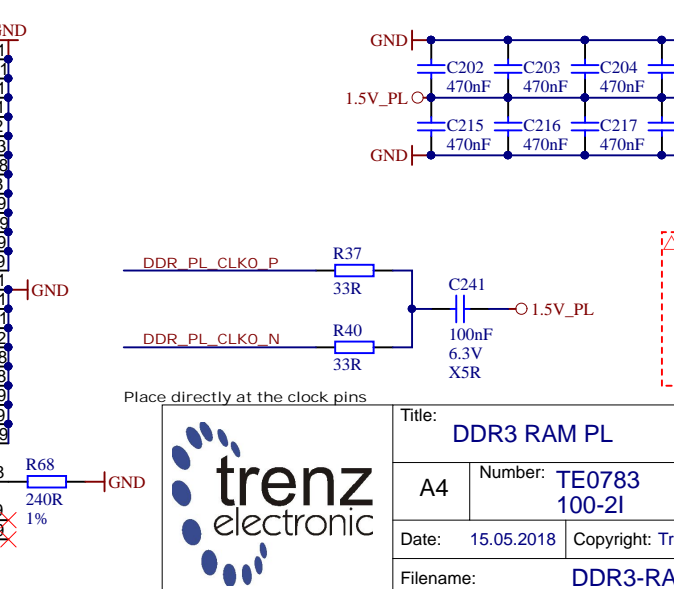
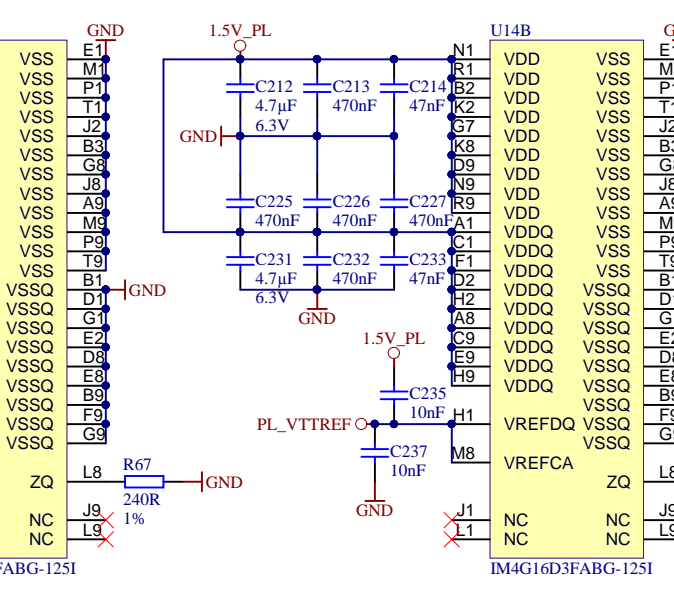
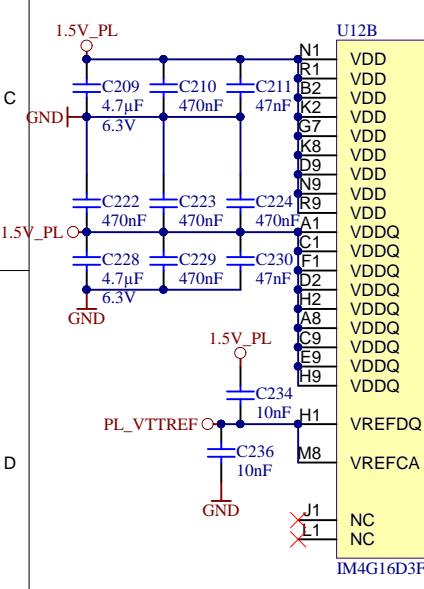
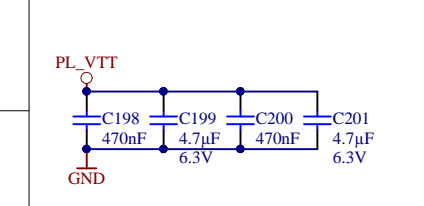
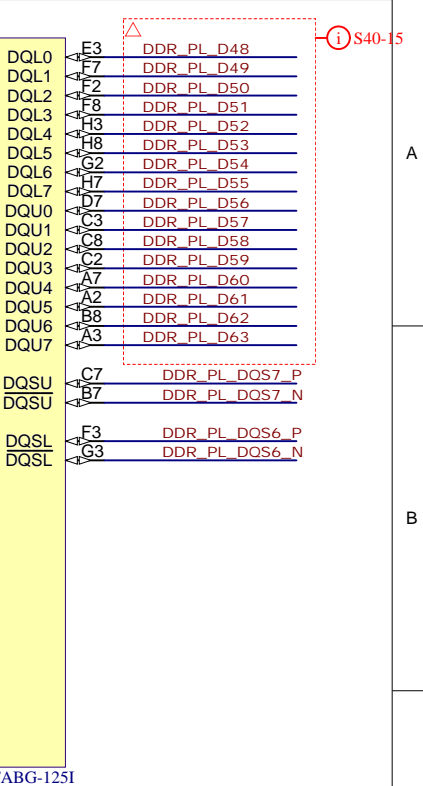
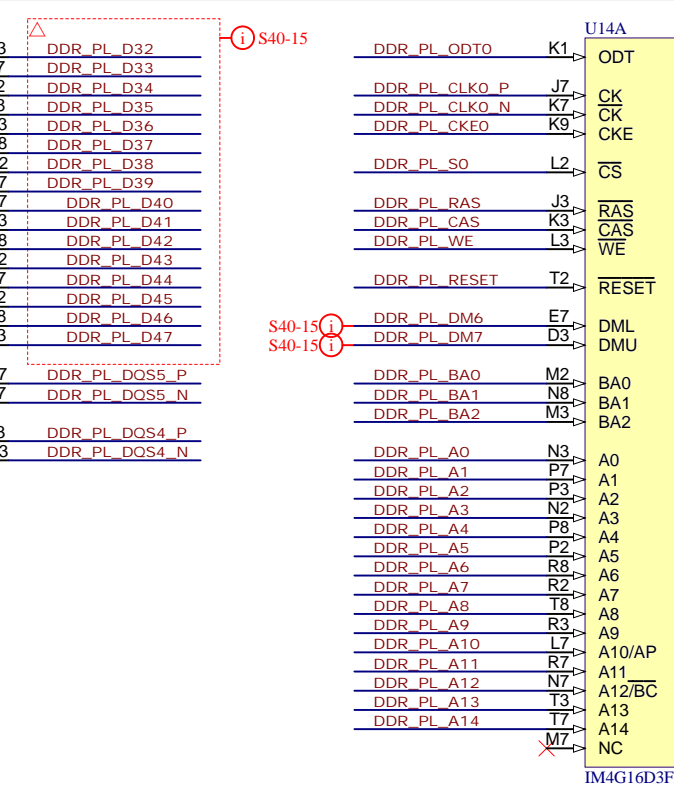
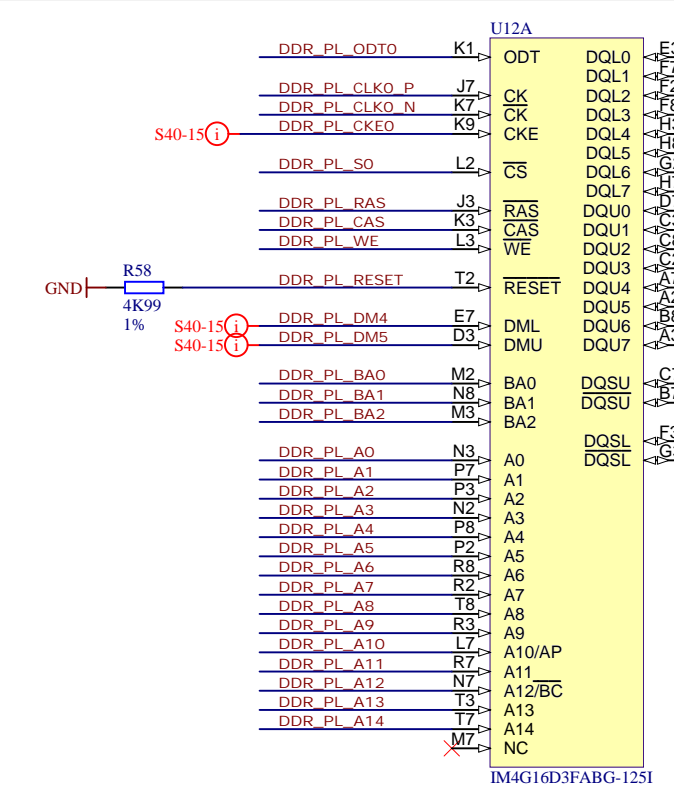
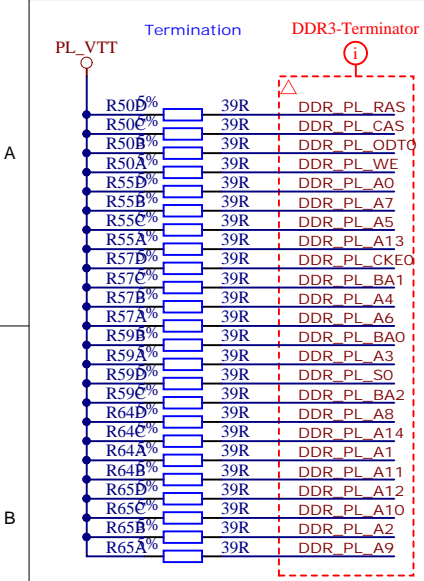
C

D

D



Title: DDR3 RAM PL		
A4	Number: TE0783 100-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 23 of 31
Filename: DDR3-RAM-PL1.SchDoc		



Title: DDR3 RAM PL		
A4	Number: TE0783 100-21	Rev. 01
Date: 15.05.2018	Copyright: Trenz Electronic GmbH	Page 24 of 31
Filename: DDR3-RAM-PL2.SchDoc		

A

B

C

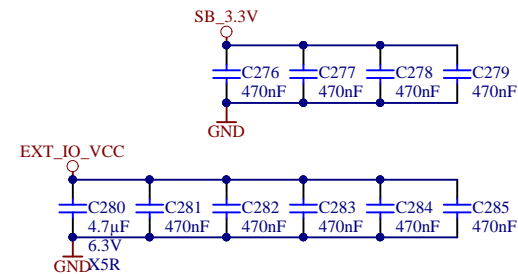
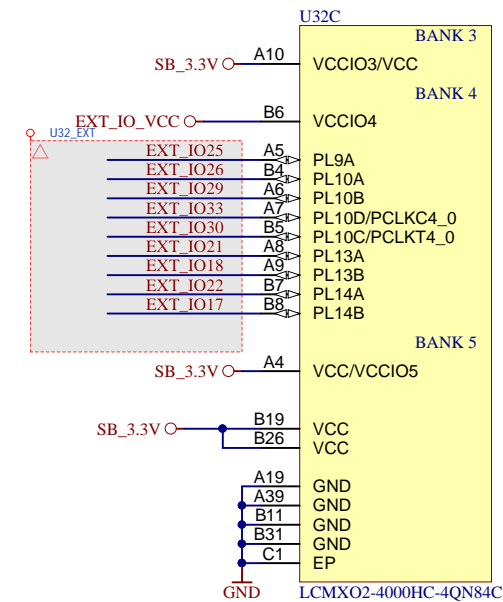
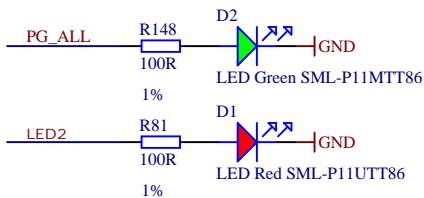
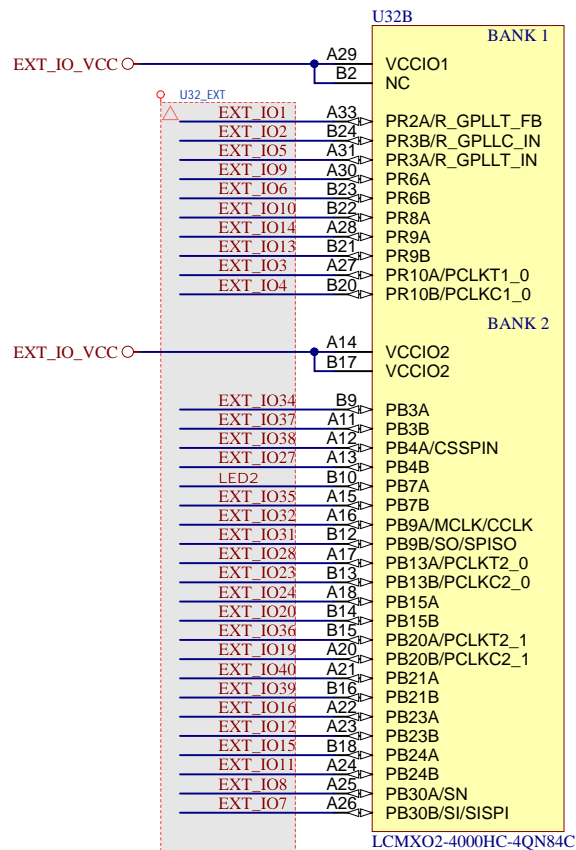
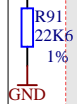
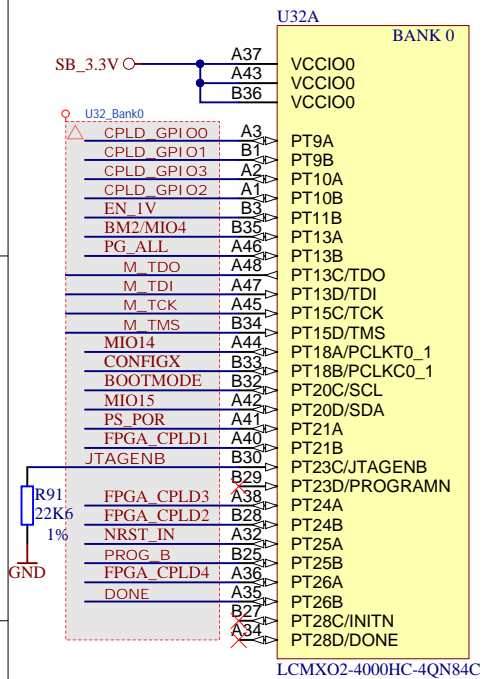
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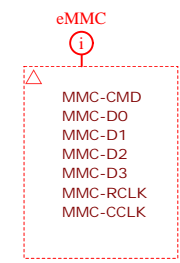
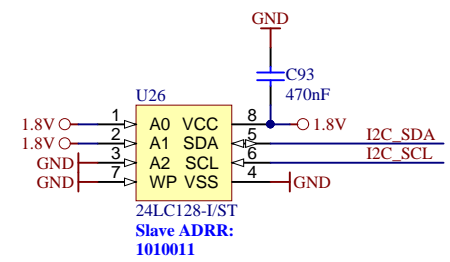
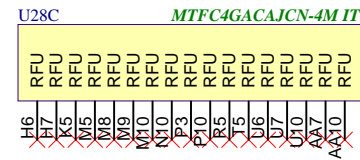
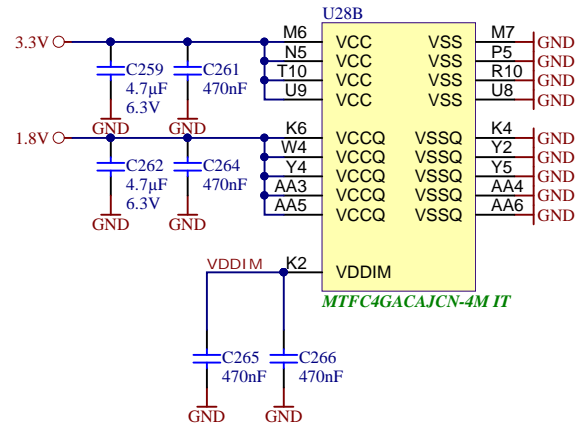
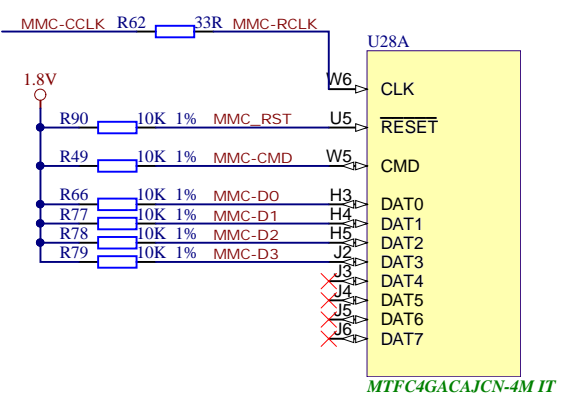
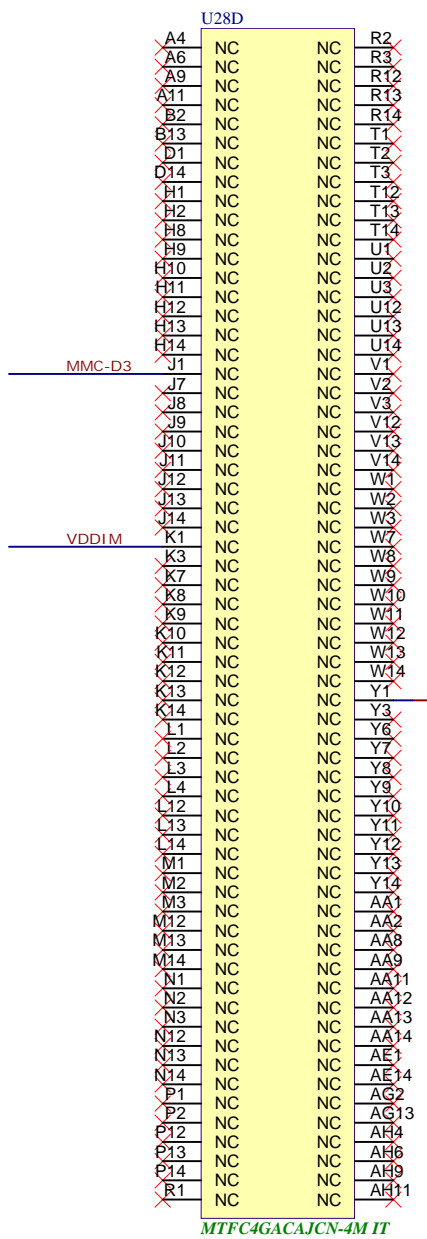
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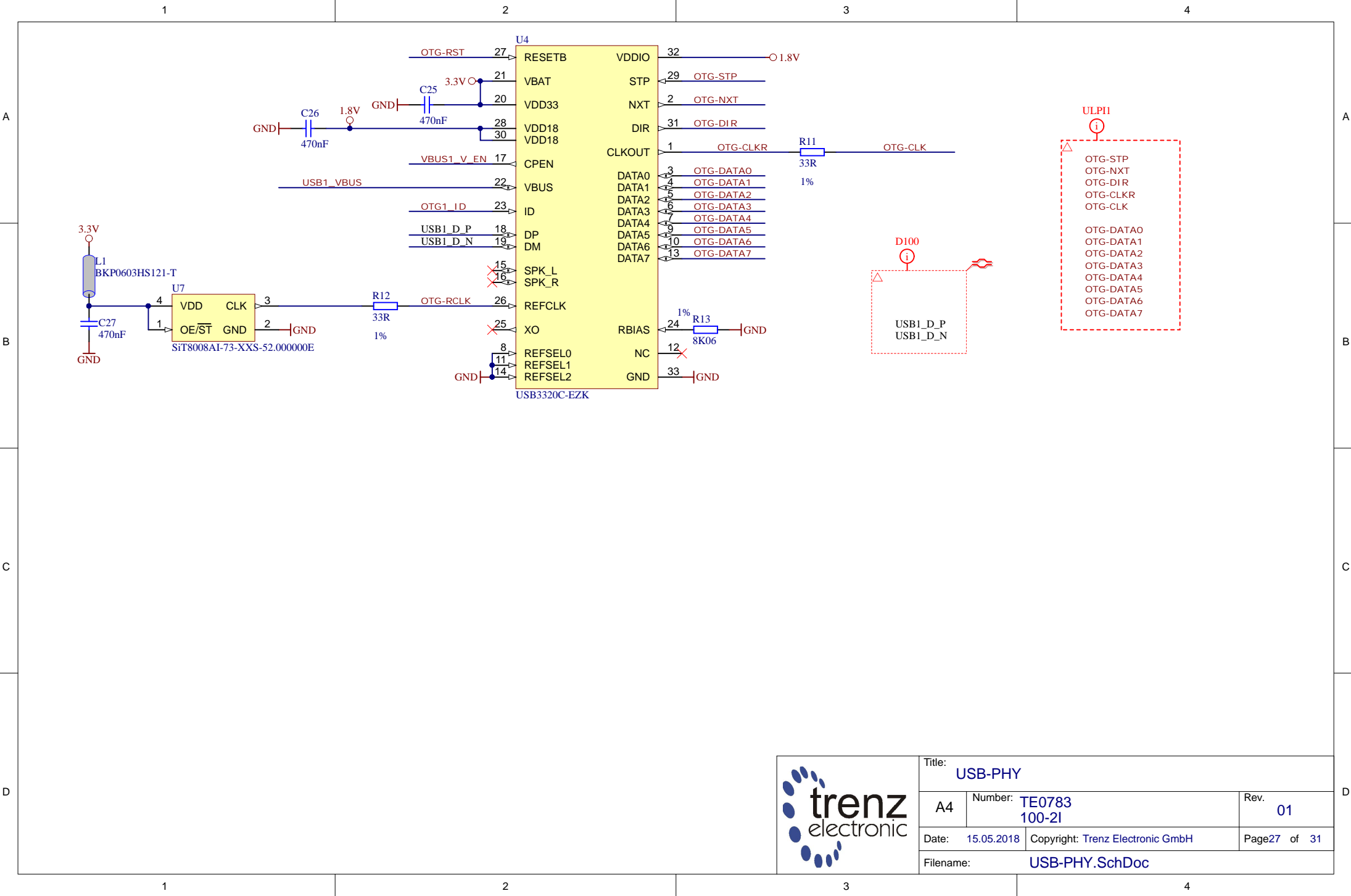
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Title: CPLD		
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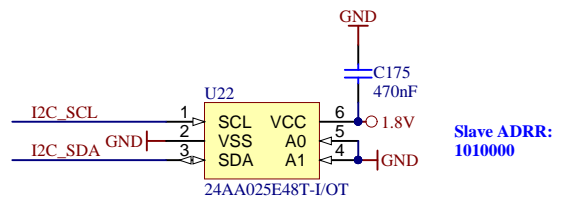
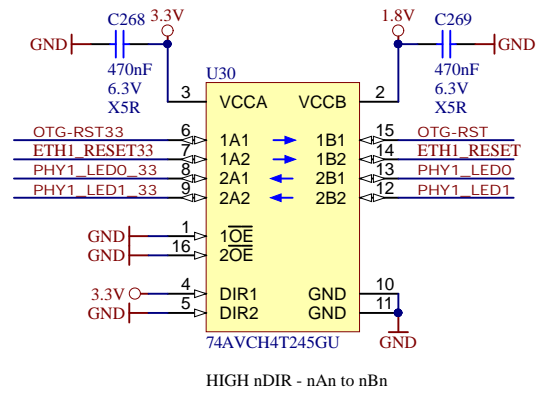
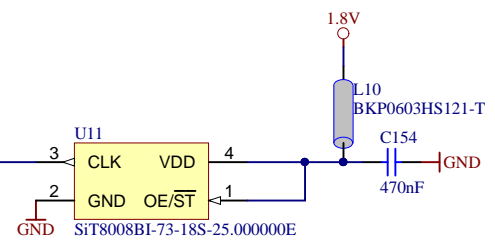
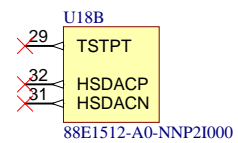
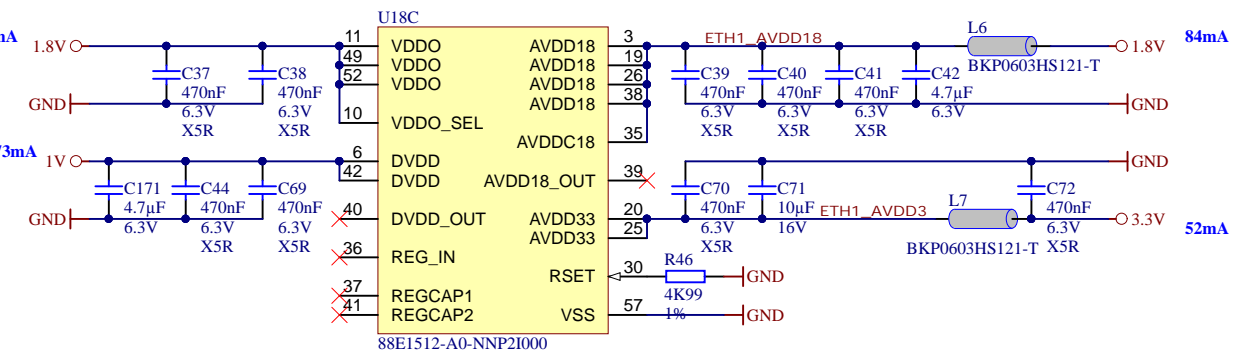
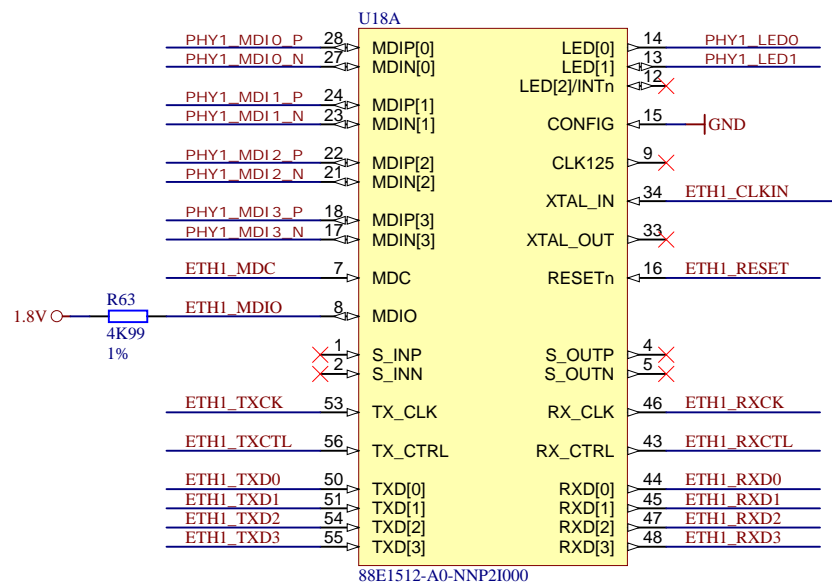


Title: eMMC		
A4	Number: TE0783 100-21	Rev. 01
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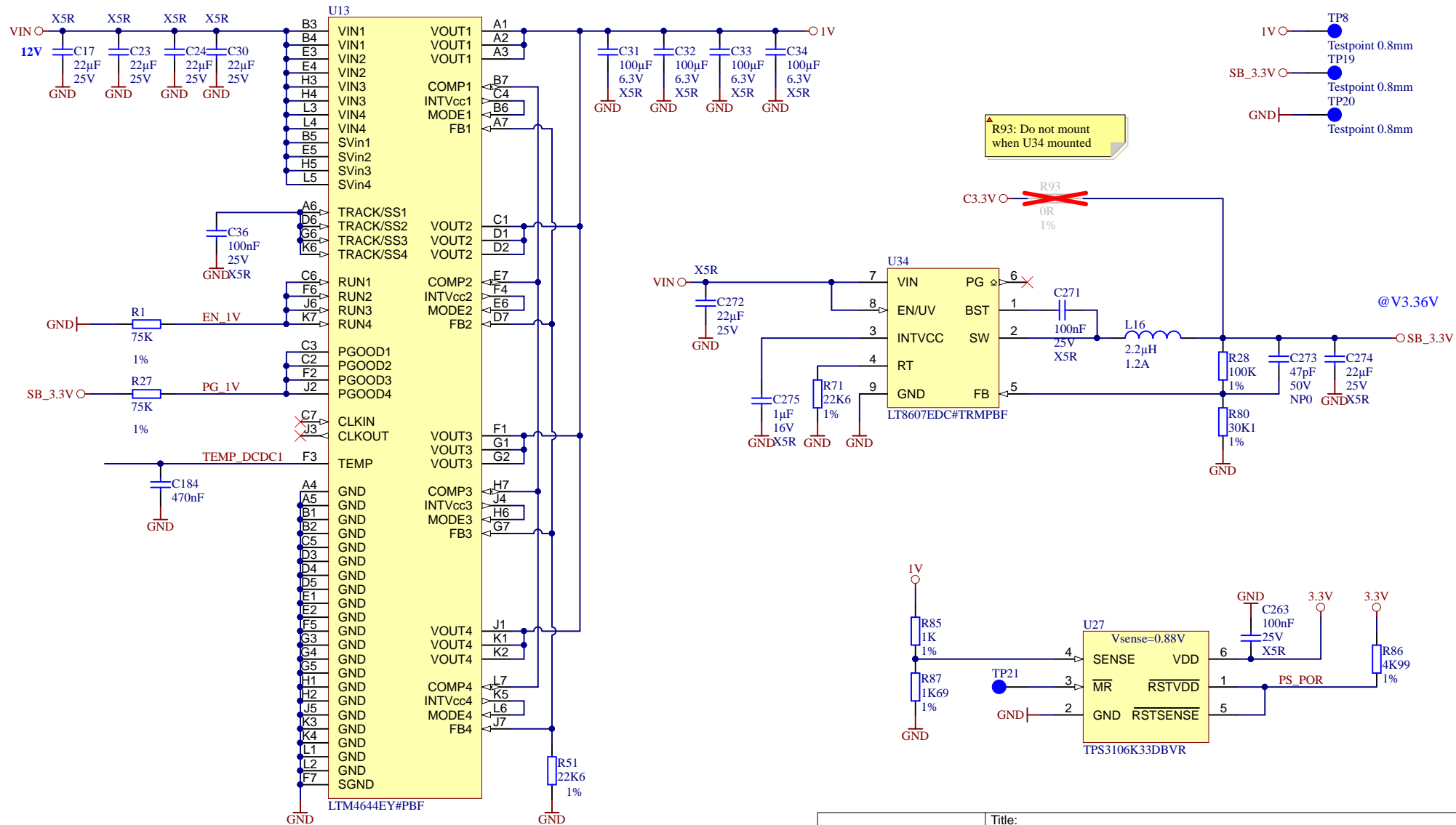


		Title: USB-PHY	
		A4	Number: TE0783 100-2I
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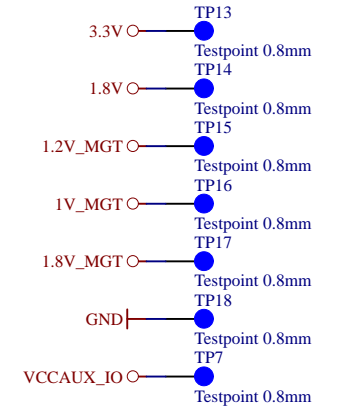
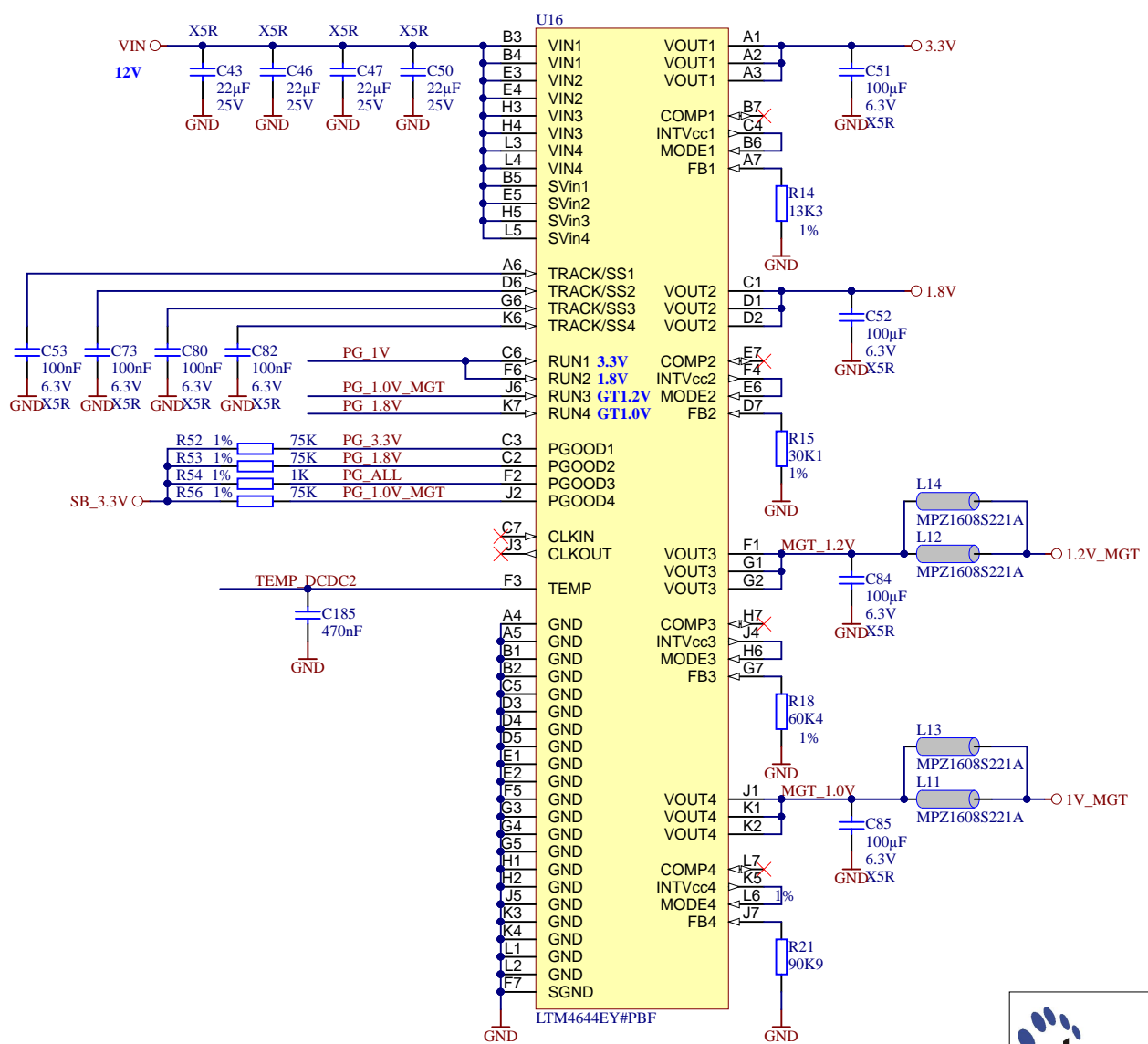
Title: ETH_PHY1		
A4	Number: TE0783 100-21	Rev. 01
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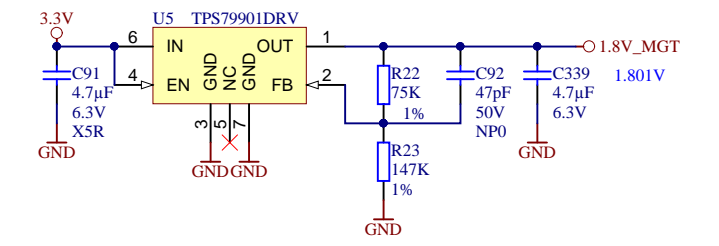
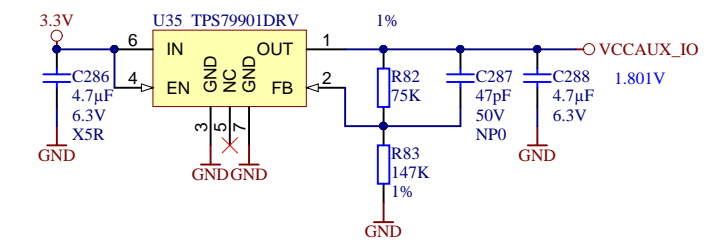
R93: Do not mount when U34 mounted


- 1V ○ TP8 Testpoint 0.8mm
- SB_3.3V ○ TP19 Testpoint 0.8mm
- GND TP20 Testpoint 0.8mm

	Title: POWER		
	A4	Number: TE0783 100-2I	Rev. 01
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CLK 666.67 and faster - VCCAUX_IO 2.0V



			Title: POWER 2	
			A4	Number: TE0783 100-21
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1

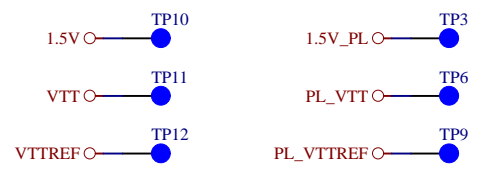
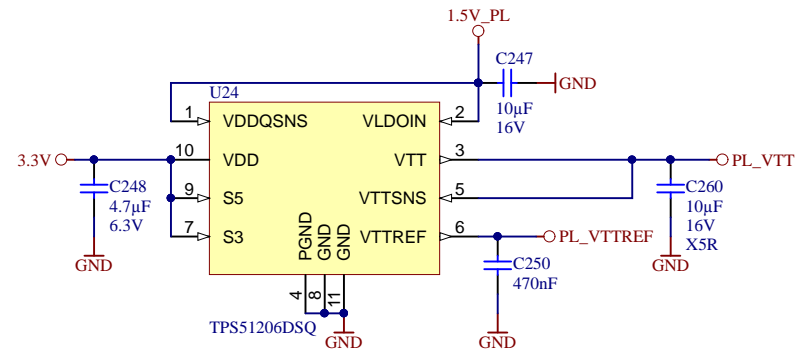
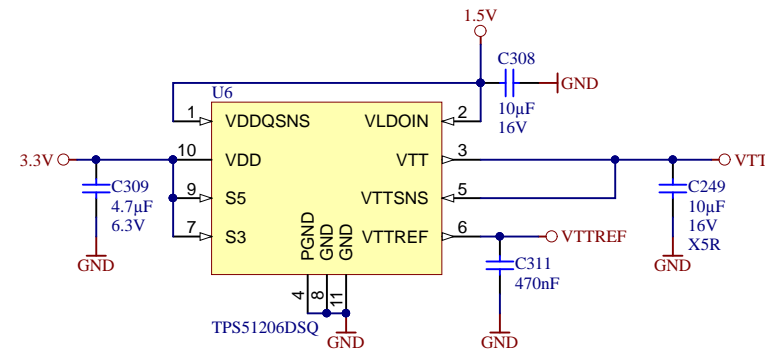
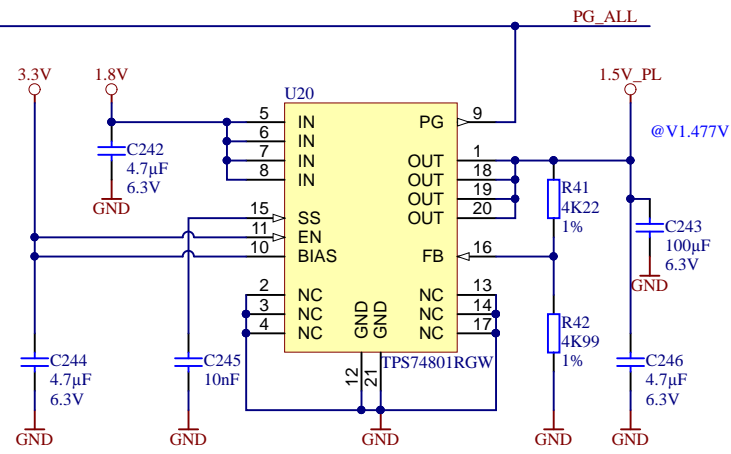
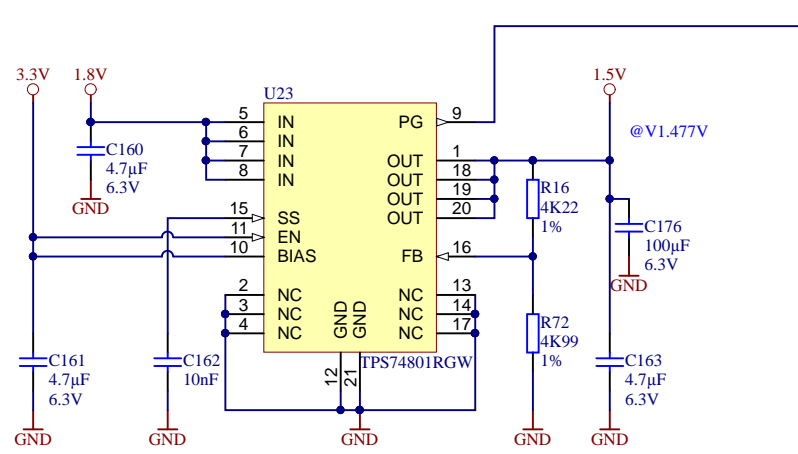
2

3

4

DDR3 PS

DDR3 PL



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1

2

3

4