

U_SOC
SOC.SchDoc

U_DDR3-RAM
DDR3-RAM.SchDoc

U_CPLD
CPLD.SchDoc

U_USB-PHY
USB-PHY.SchDoc

U_ETH1
ETH1.SchDoc

U_Clock
Clock.SchDoc

U_eMMC
eMMC.SchDoc

U_POWER2
POWER2.SchDoc

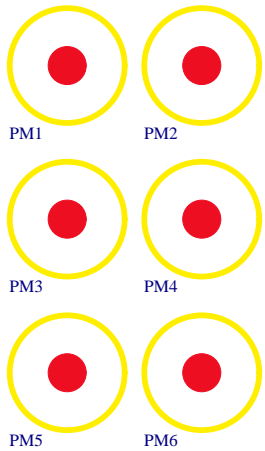
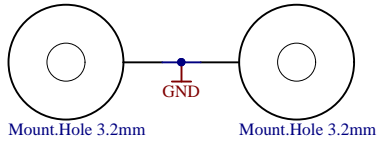
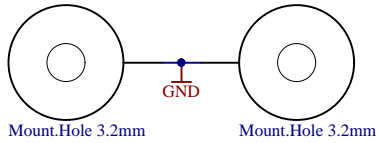
U_Connectors
Connectors.SchDoc

U_Rev_changes
Revision Changes.SchDoc

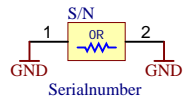
U_POWER
POWER.SchDoc

U_POWER3
POWER3.SchDoc

LOGO1
TE Logo PRINT Layer
LOGO PRINT



Serial
Serialnumber 6,3 x 6.3mm



Title: Overview		
A4	Number: TE0783 045-21	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page1 of 32
Filename: TE0783.SchDoc		

1

2

3

4

A

A

U_HSMC_CONN_J1
HSMC_CONN_J1.SchDoc



U_HSMC_CONN_J2
HSMC_CONN_J2.SchDoc



U_HSMC_CONN_J3
HSMC_CONN_J3.SchDoc



B

B

C

C

D


D

1

2

3

4

		Title: Connectors	
		A4	Number: TE0783 045-2I
Date: 13.07.2018		Copyright: Trenz Electronic GmbH	
Filename: Connectors.SchDoc		Page 2 of 32	

1

2

3

4

A

A

B

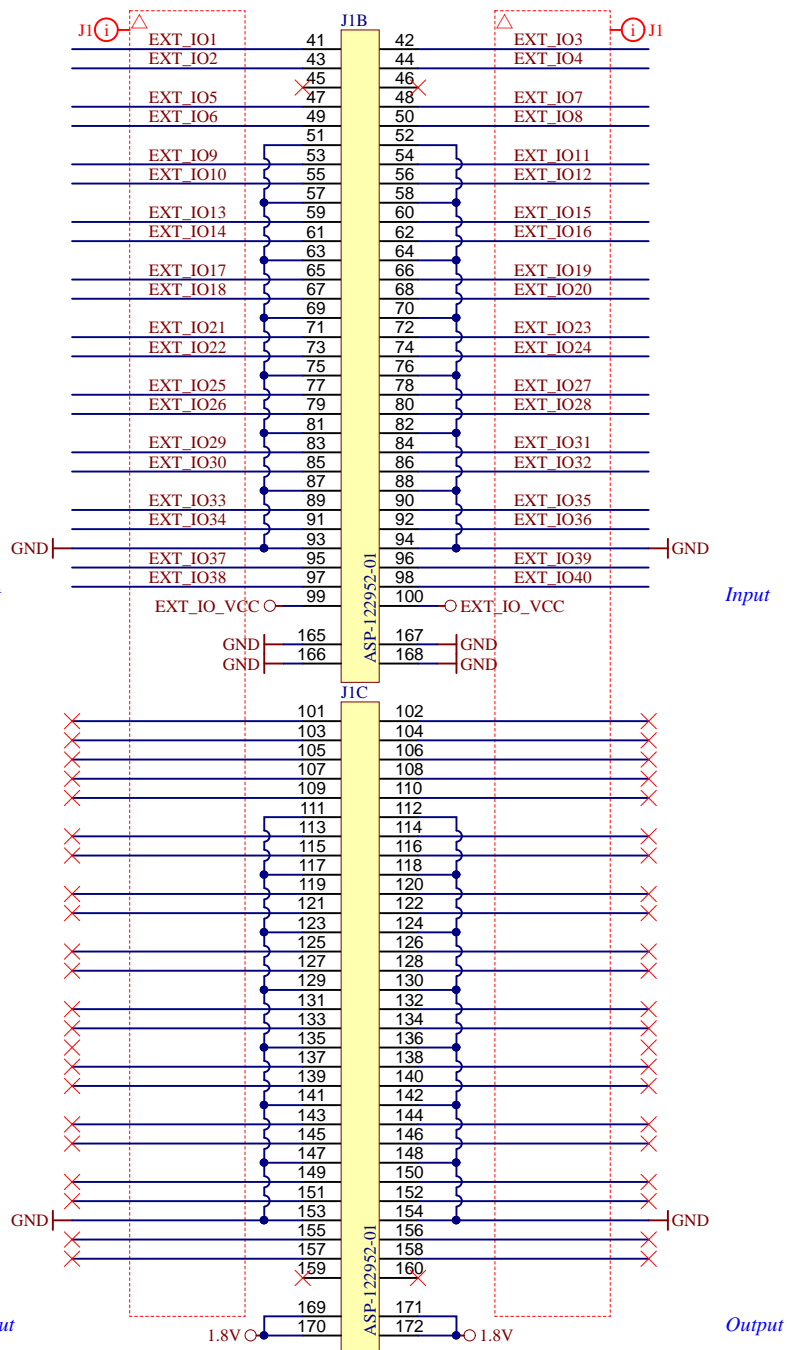
B

C

C

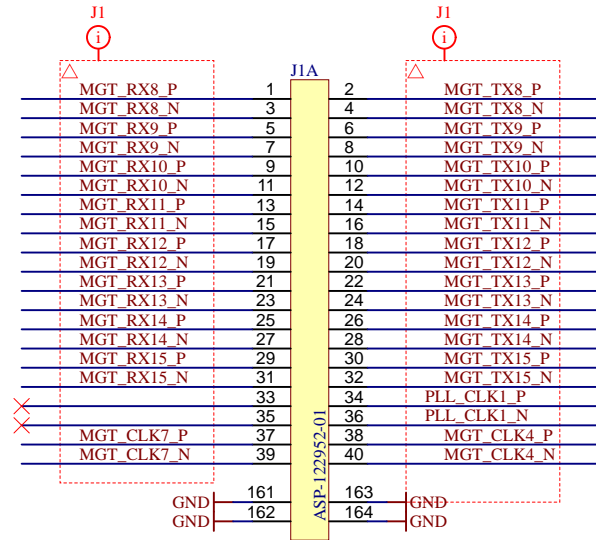
D

D



Next signals has different functionality in TE0782 and TEBT0782.

TE0782
 J1_TX20_N
 J1_TX20_P
 J1_TX21_N
 J1_TX21_P

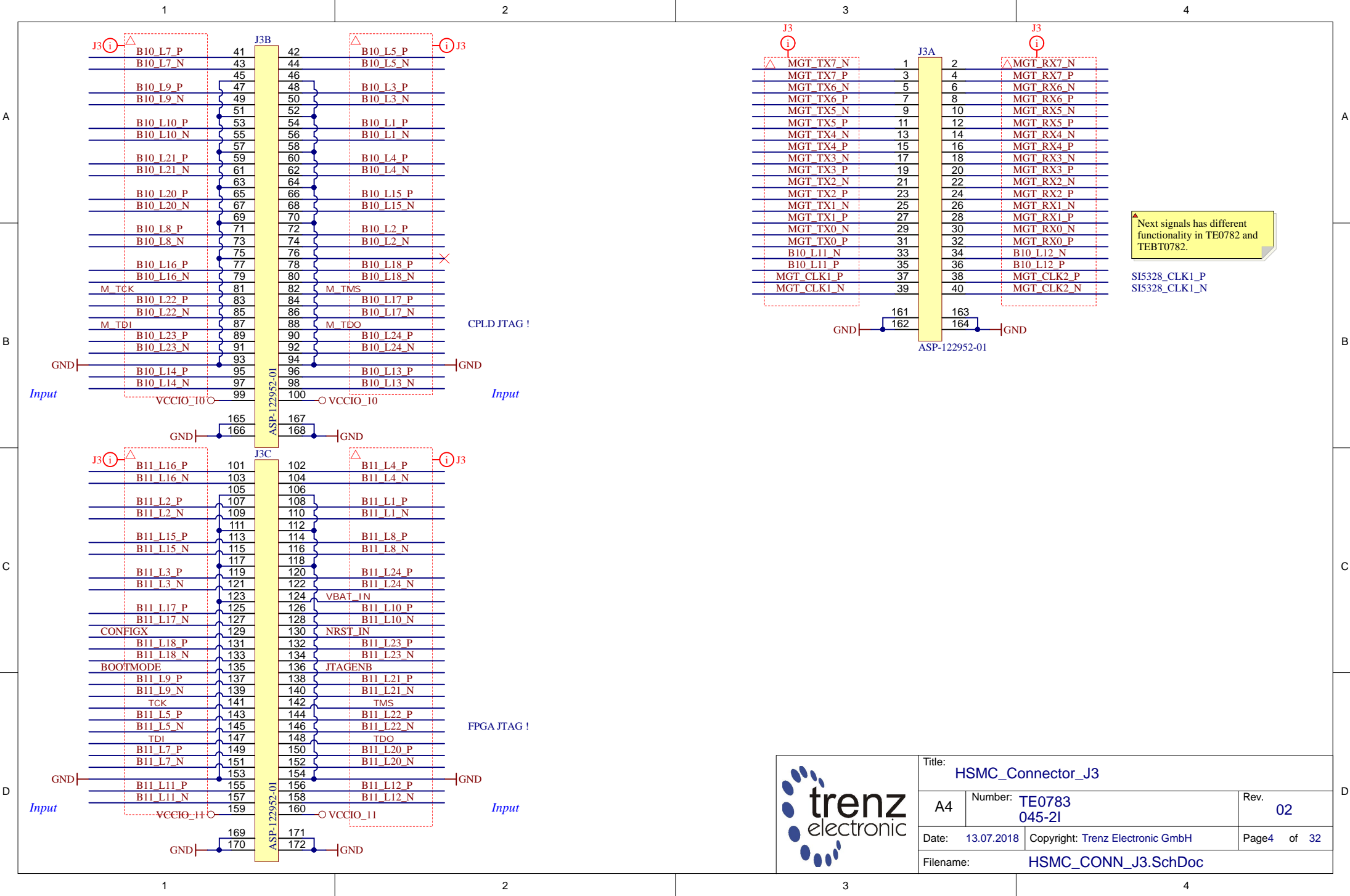


Next signals has different functionality in TE0782 and TEBT0782.

TE0782
 J1_RX20_N
 J1_RX20_P



Title: HSMC_Connector_J1		
A4	Number: TE0783 045-2I	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 3 of 32
Filename: HSMC_CONN_J1.SchDoc		



▲ Next signals has different functionality in TE0782 and TEBT0782.

S15328_CLK1_P
S15328_CLK1_N



Title: HSMC_Connector_J3		
A4	Number: TE0783 045-21	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page4 of 32
Filename: HSMC_CONN_J3.SchDoc		

A

B

C

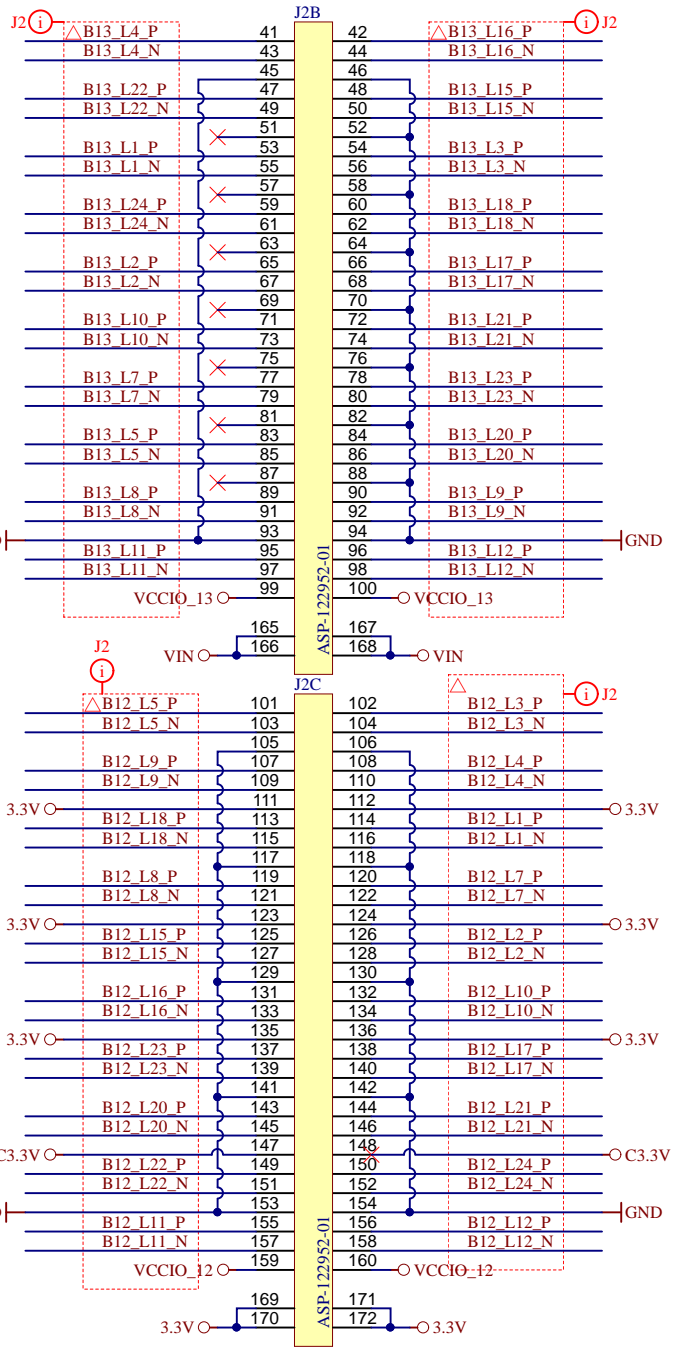
D

A

B

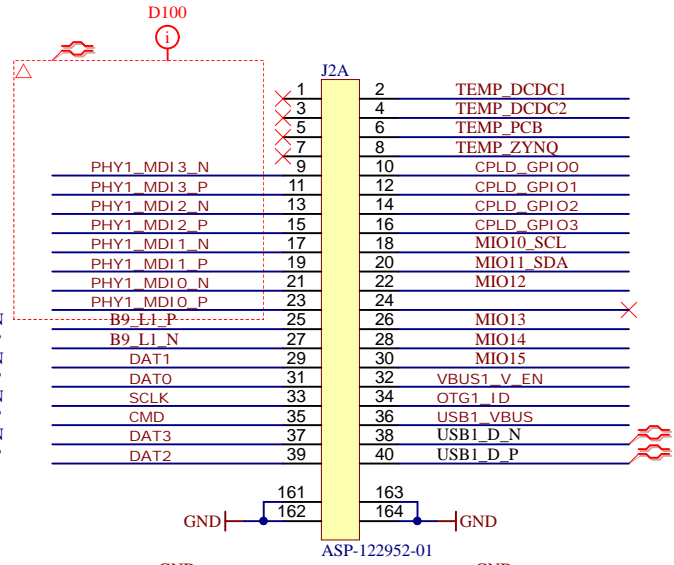
C

D



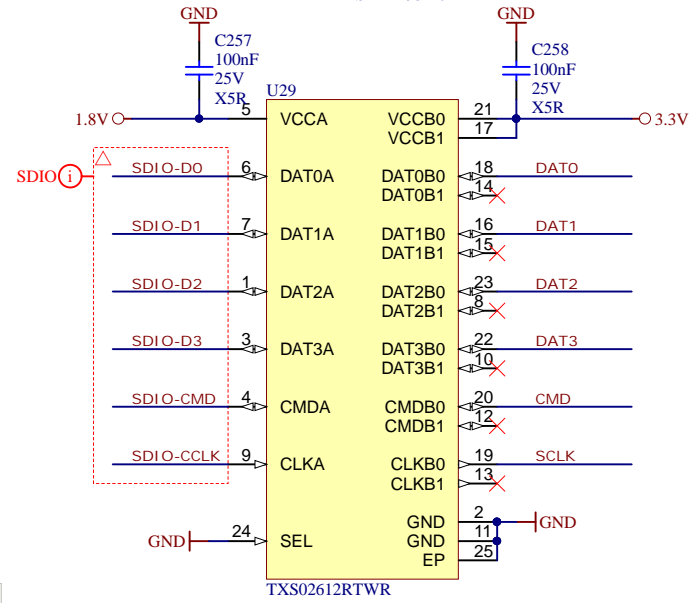
Next signals has different functionality in TE0782 and TEBT0782.

TE0782
 PHY2_MDI3_N
 PHY2_MDI3_P
 PHY2_MDI2_N
 PHY2_MDI2_P
 PHY2_MDI1_N
 PHY2_MDI1_P
 PHY2_MDI0_N
 PHY2_MDI0_P



Next signals has different functionality in TE0782 and TEBT0782.

TE0782
 CPLD_GPIO4
 CPLD_GPIO5
 OTG2_ID
 USB2_VBUS
 USB2_D_N
 USB2_D_P
 VBUS2_V_EN



SDCARD
 DAT0
 DAT1
 DAT2
 DAT3
 CMD
 SCLK

* - C3.3V: Normally leave unconnected



Title: HSMC_Connector_J2		
A4	Number: TE0783 045-21	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page5 of 32
Filename: HSMC_CONN_J2.SchDoc		

1

2

3

4

A

A

U_PS-DDR
PS-DDR.SchDoc



U_B9
B9.SchDoc



U_MIO-BANKS
MIO-BANKS.SchDoc



U_B10
B10.SchDoc



U_HP-BANKS
HP-BANKS.SchDoc



U_B11
B11.SchDoc



B

B

U_FPGA-MGT
FPGA-MGT.SchDoc



U_B12
B12.SchDoc



U_FPGA-CFG
FPGA-CFG.SchDoc



U_B13
B13.SchDoc



C

C

U_FPGA-PWR
FPGA-PWR.SchDoc



D

D



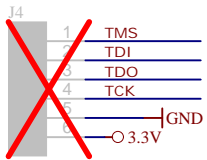
Title: SOC		
A4	Number: TE0783 045-2I	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 6 of 32
Filename: SOC.SchDoc		

1

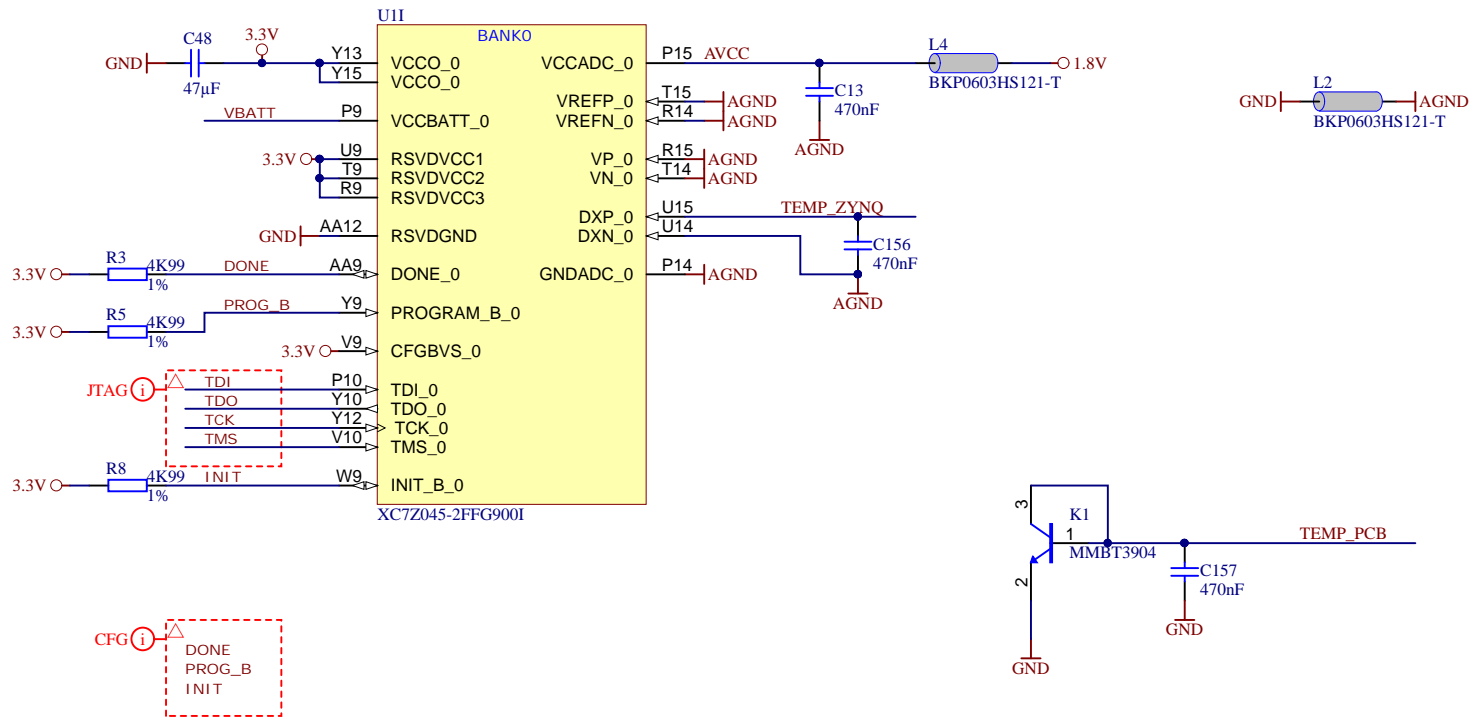
2

3

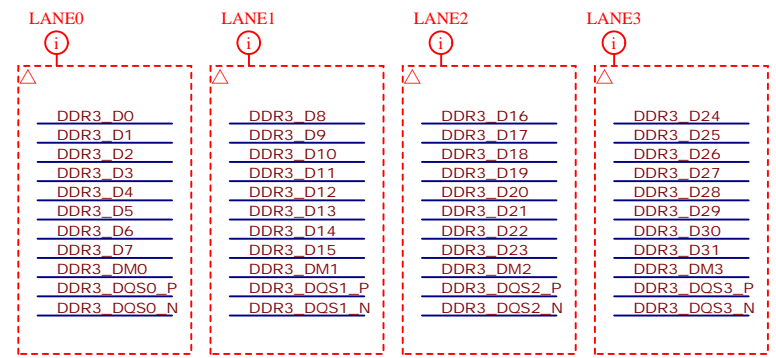
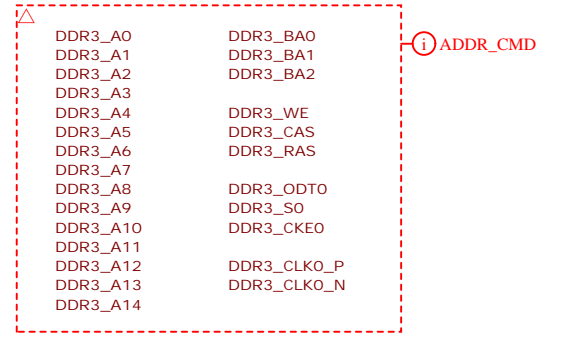
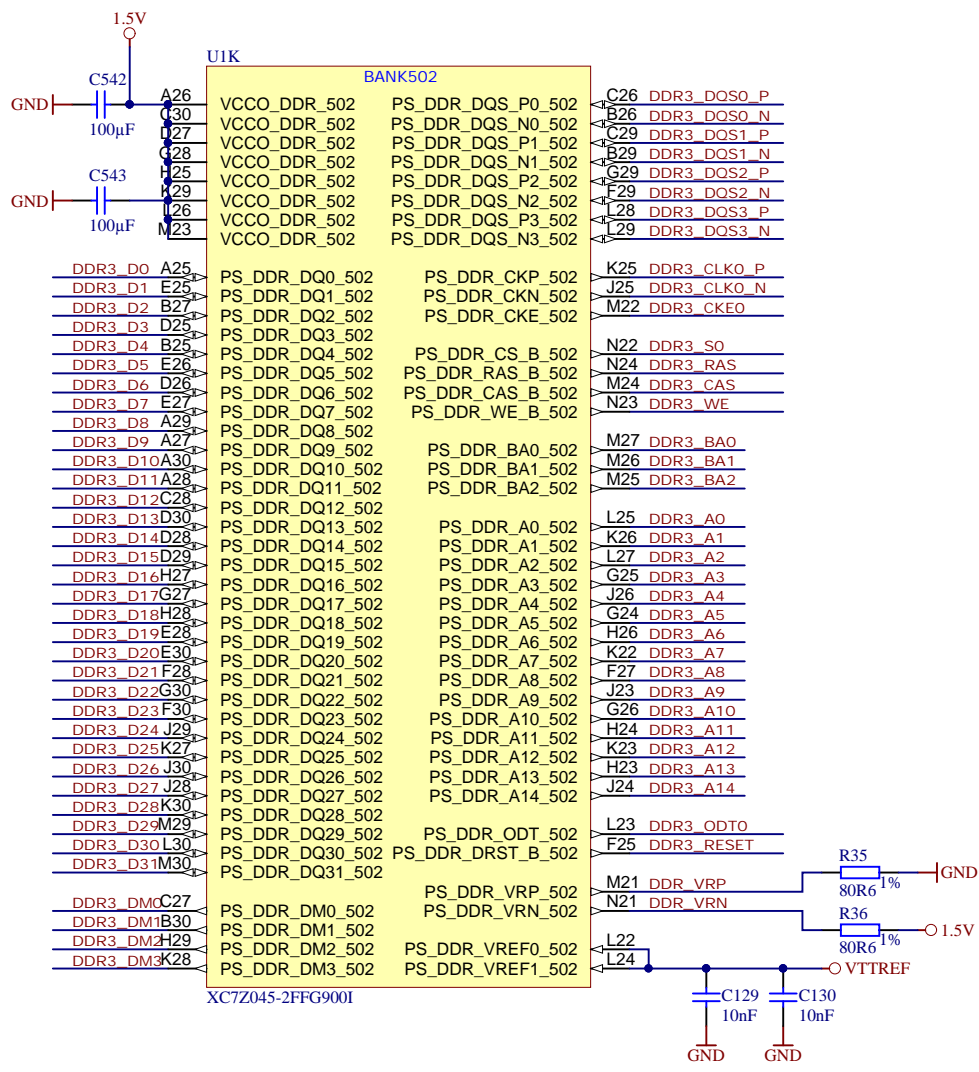
4



Placeholder 1 row 6 pin header



Title: FPGA Configuration		
A4	Nummer: TE0783 045-2I	Rev. 02
Datum: 13.07.2018	Zeichner: Trenz Electronic GmbH	Blatt 7 von 32
Filename: FPGA-CFG.SchDoc		



Title: FPGA DDR Banks		
A4	Number: TE0783 045-21	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 8 of 32
Filename: PS-DDR.SchDoc		

U1M

ClassName: MGT_TX

D100

BANK109

MGT_CLK2_P AD10
 MGT_CLK2_N AD9
 MGT_CLK3_P AF10
 MGT_CLK3_N AF9
 MGT_RX0_P AH10
 MGT_RX0_N AH9
 MGT_RX1_P AJ8
 MGT_RX1_N AJ7
 MGT_RX2_P AG8
 MGT_RX2_N AG7
 MGT_RX3_P AE8
 MGT_RX3_N AE7

MGT_XRP0_109
 MGT_XRN0_109
 MGT_XRP1_109
 MGT_XRN1_109
 MGT_XRP2_109
 MGT_XRN2_109
 MGT_XRP3_109
 MGT_XRN3_109

BANK110

MGT_CLK0_P AA8
 MGT_CLK0_N AA7
 MGT_CLK1_N AC8
 MGT_CLK1_P AC7
 MGT_RX4_P AH6
 MGT_RX4_N AH5
 MGT_RX5_P AG4
 MGT_RX5_N AG3
 MGT_RX6_P AF6
 MGT_RX6_N AF5
 MGT_RX7_P AD6
 MGT_RX7_N AD5

MGT_XRP0_110
 MGT_XRN0_110
 MGT_XRP1_110
 MGT_XRN1_110
 MGT_XRP2_110
 MGT_XRN2_110
 MGT_XRP3_110
 MGT_XRN3_110

BANK111

MGT_CLK4_N U8
 MGT_CLK4_P U7
 MGT_CLK5_P W8
 MGT_CLK5_N W7
 MGT_RX8_P AC4
 MGT_RX8_N AC3
 MGT_RX9_P AB6
 MGT_RX9_N AB5
 MGT_RX10_P Y6
 MGT_RX10_N Y5
 MGT_RX11_P AA4
 MGT_RX11_N AA3

MGT_XRP0_111
 MGT_XRN0_111
 MGT_XRP1_111
 MGT_XRN1_111
 MGT_XRP2_111
 MGT_XRN2_111
 MGT_XRP3_111
 MGT_XRN3_111

BANK112

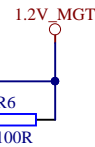
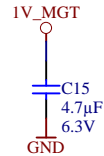
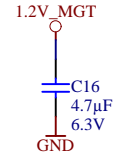
MGT_CLK6_P N8
 MGT_CLK6_N N7
 MGT_CLK7_P R8
 MGT_CLK7_N R7
 MGT_RX12_P V6
 MGT_RX12_N V5
 MGT_RX13_P U4
 MGT_RX13_N U3
 MGT_RX14_P T6
 MGT_RX14_N T5
 MGT_RX15_P P6
 MGT_RX15_N P5

MGT_XRP0_112
 MGT_XRN0_112
 MGT_XRP1_112
 MGT_XRN1_112
 MGT_XRP2_112
 MGT_XRN2_112
 MGT_XRP3_112
 MGT_XRN3_112

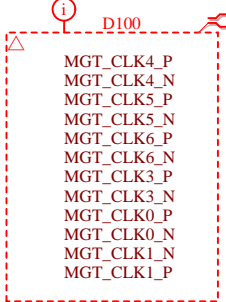
XC7Z045-2FFG9001

MGTXTXP0_109
 MGTXTXN0_109
 MGTXTXP1_109
 MGTXTXN1_109
 MGTXTXP2_109
 MGTXTXN2_109
 MGTXTXP3_109
 MGTXTXN3_109
 MGTXTXP0_110
 MGTXTXN0_110
 MGTXTXP1_110
 MGTXTXN1_110
 MGTXTXP2_110
 MGTXTXN2_110
 MGTXTXP3_110
 MGTXTXN3_110
 MGTXTXP0_111
 MGTXTXN0_111
 MGTXTXP1_111
 MGTXTXN1_111
 MGTXTXP2_111
 MGTXTXN2_111
 MGTXTXP3_111
 MGTXTXN3_111

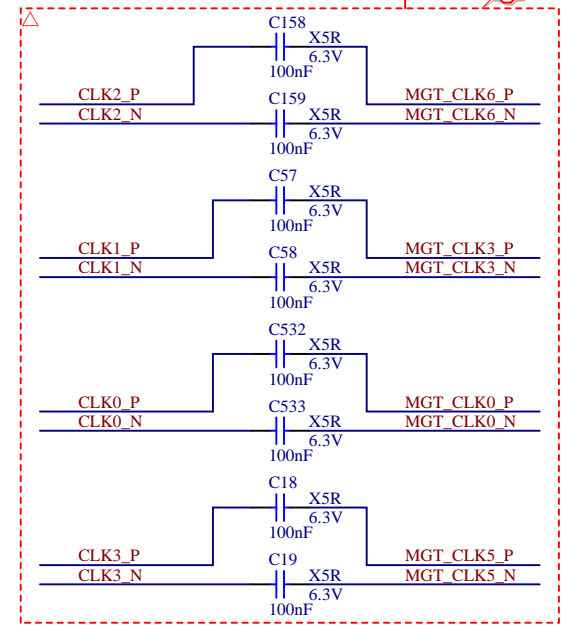
AK10 MGT_TX0_P
 AK9 MGT_TX0_N
 AK6 MGT_TX1_P
 AK5 MGT_TX1_N
 AJ4 MGT_TX2_P
 AJ3 MGT_TX2_N
 AK2 MGT_TX3_P
 AK1 MGT_TX3_N
 AH2 MGT_TX4_P
 AH1 MGT_TX4_N
 AF2 MGT_TX5_P
 AF1 MGT_TX5_N
 AE4 MGT_TX6_P
 AE3 MGT_TX6_N
 AD2 MGT_TX7_P
 AD1 MGT_TX7_N
 AB2 MGT_TX8_P
 AB1 MGT_TX8_N
 Y2 MGT_TX9_P
 Y1 MGT_TX9_N
 W4 MGT_TX10_P
 W3 MGT_TX10_N
 V2 MGT_TX11_P
 V1 MGT_TX11_N
 AB10 MGT_TX12_P
 AB9 MGT_TX12_N
 T2 MGT_TX12_P
 T1 MGT_TX12_N
 R4 MGT_TX13_P
 R3 MGT_TX13_N
 P2 MGT_TX14_P
 P1 MGT_TX14_N
 N4 MGT_TX15_P
 N3 MGT_TX15_N



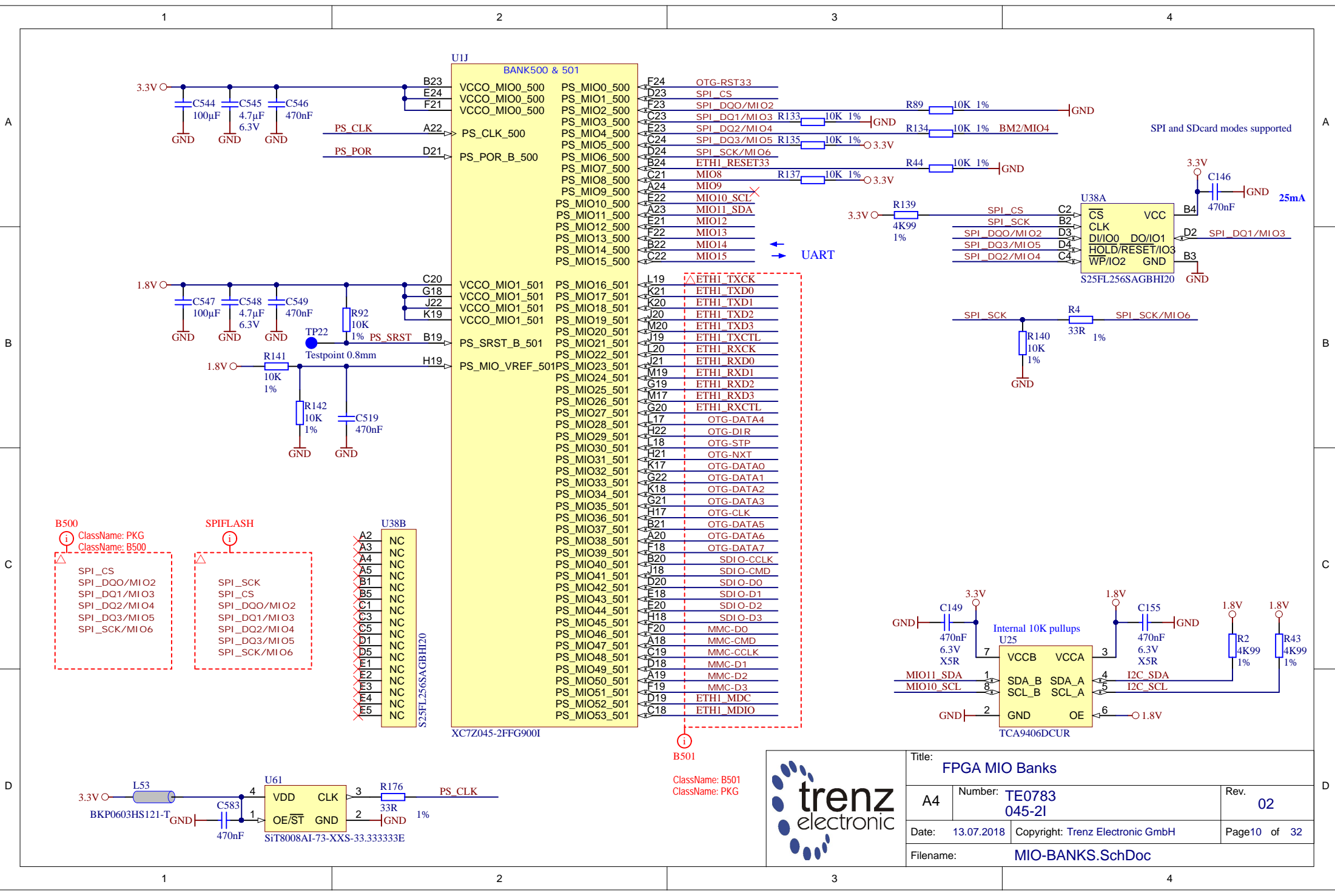
MGT_CLK



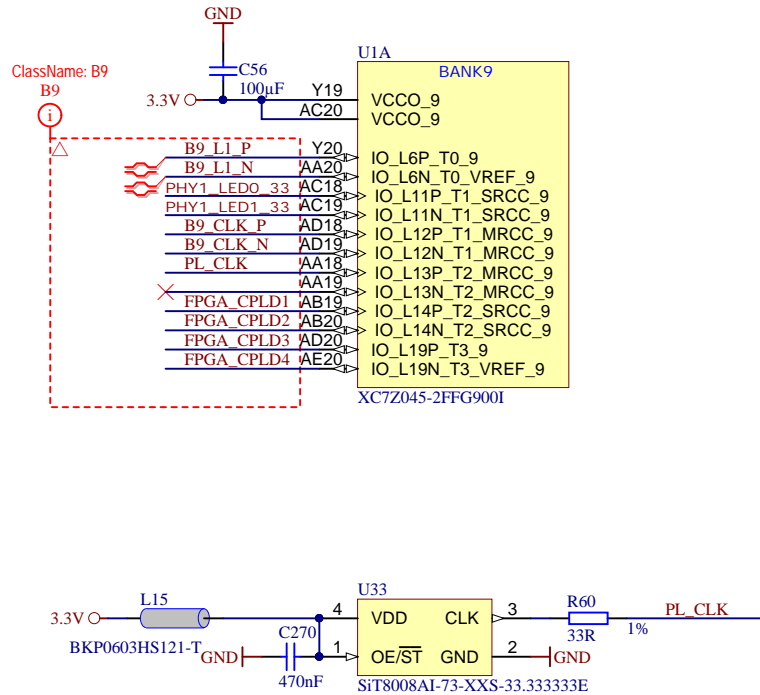
D100




Title: FPGA MGT		
A4	Number: TE0783 045-2I	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 9 of 32
Filename: FPGA-MGT.SchDoc		

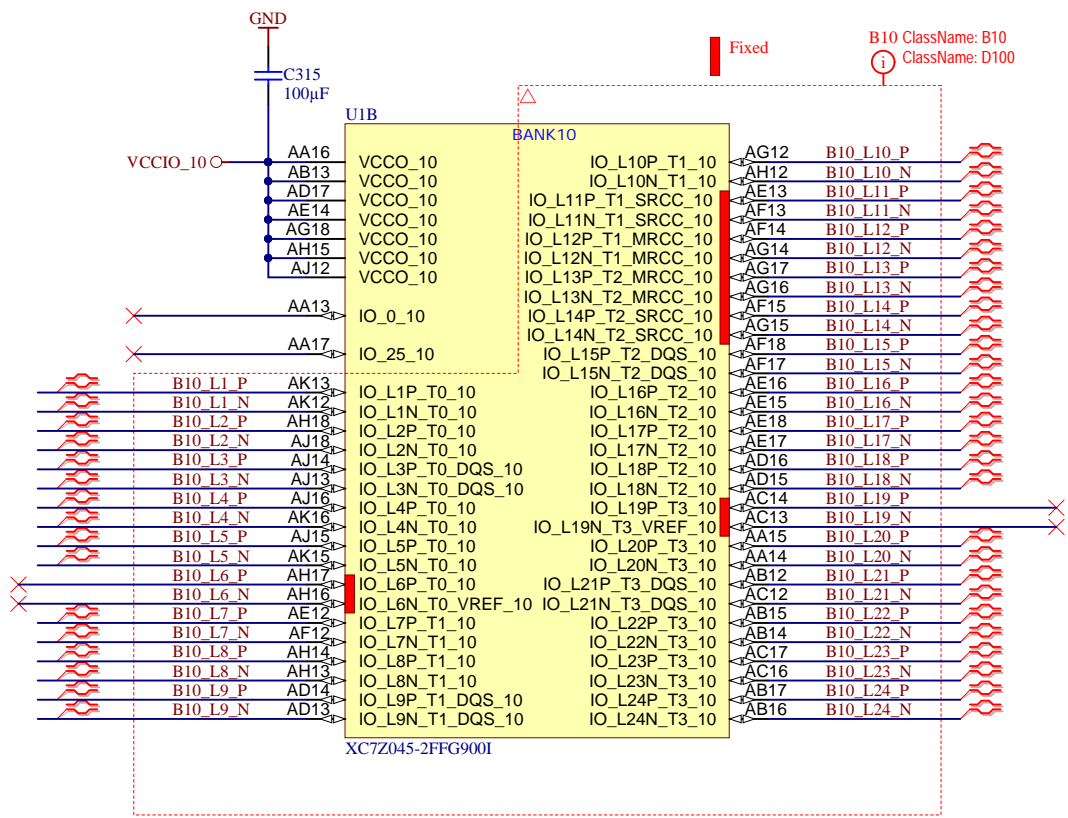


Title: FPGA MIO Banks		
A4	Number: TE0783 045-21	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 10 of 32
Filename: MIO-BANKS.SchDoc		



	Title: FPGA B9		
	A4	Number: TE0783 045-2I	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 11 of 32
	Filename: B9.SchDoc		

TP4
 ● VCCIO_10
 ○ Testpoint 0.8mm



Title: FPGA B10		
A4	Number: TE0783 045-2I	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 12 of 32
Filename: B10.SchDoc		

A

A

B

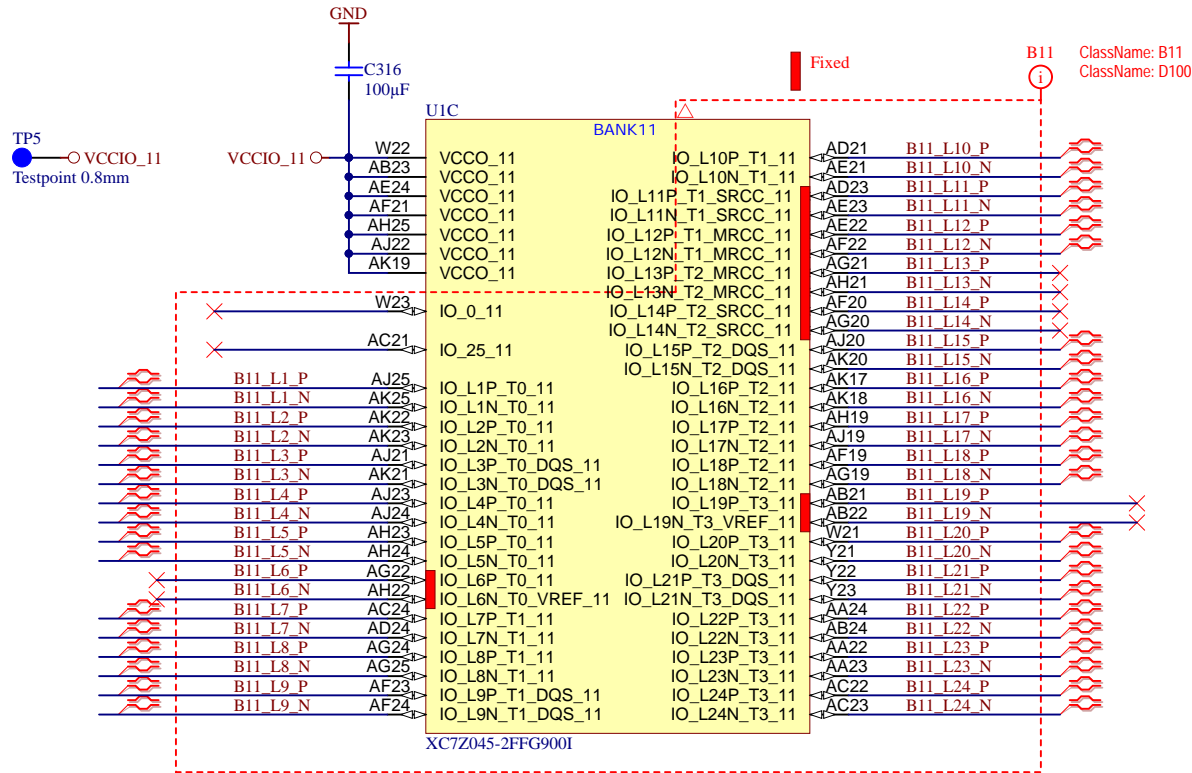
B


C


C

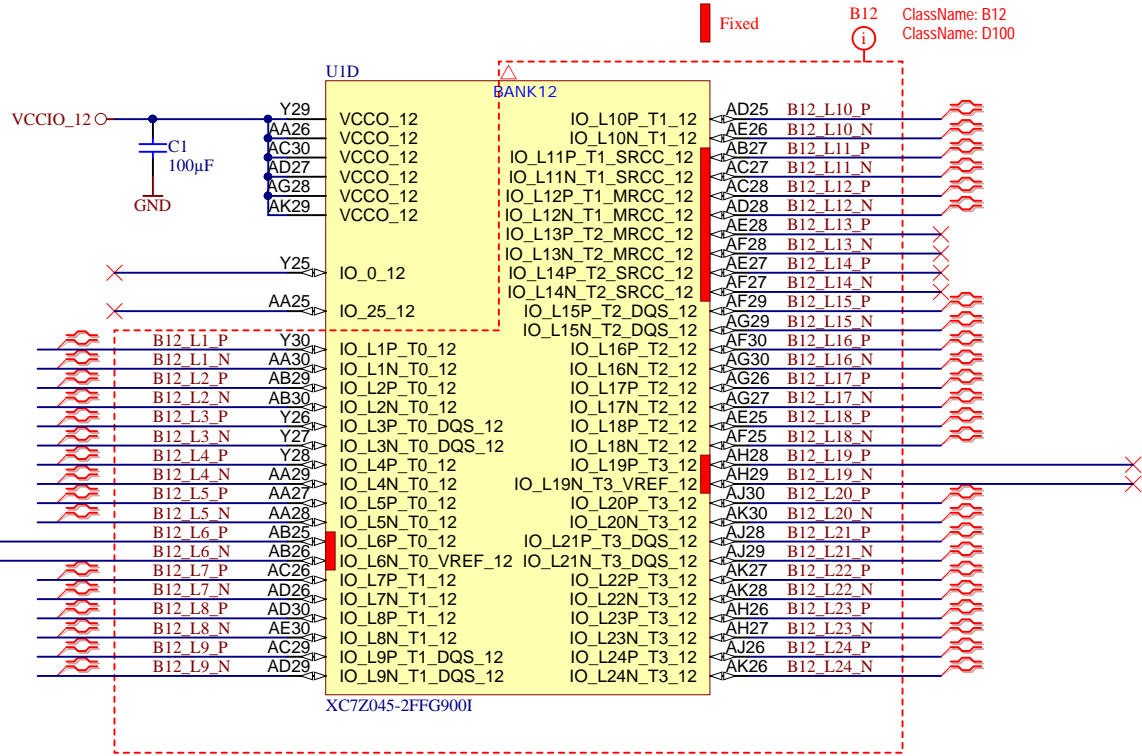
D

D



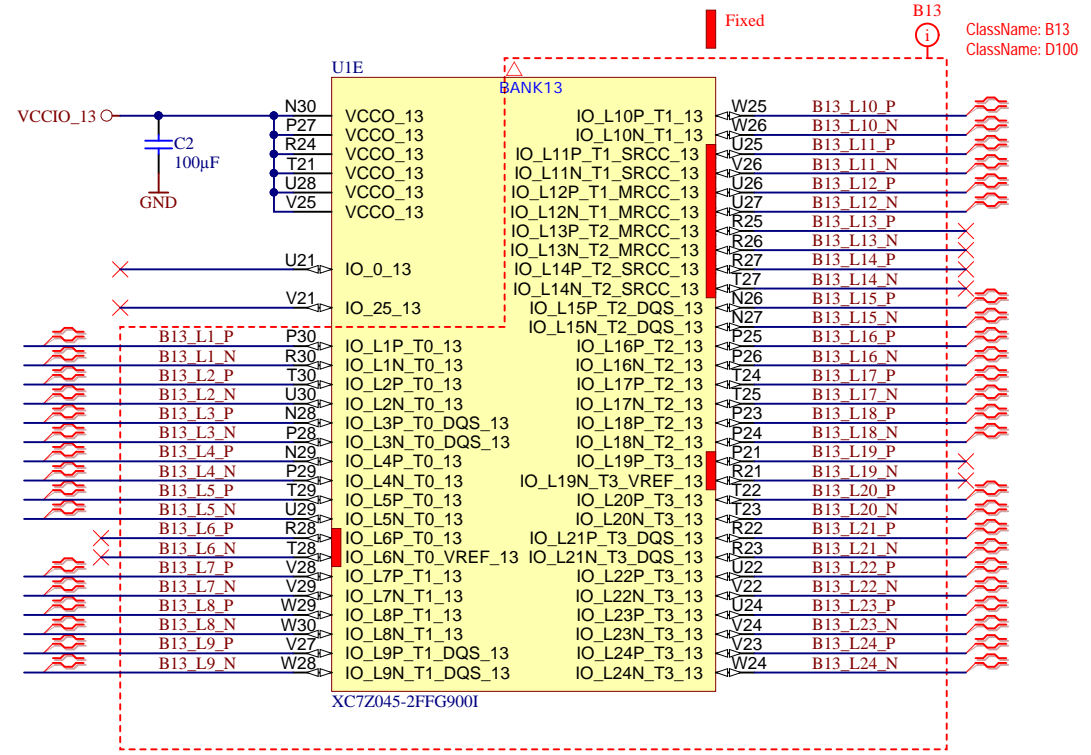
			Title: FPGA B11	
			A4	Number: TE0783 045-2I
Date: 13.07.2018		Copyright: Trenz Electronic GmbH		Page 13 of 32
Filename: B11.SchDoc				

TP1
 VCCIO_12
 Testpoint 0.8mm



Title: FPGA B12		
A4	Number: TE0783 045-2I	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 14 of 32
Filename: B12.SchDoc		

TP2
 ● ○ VCCIO_13
 Testpoint 0.8mm



Title: FPGA B13		
A4	Number: TE0783 045-2I	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 15 of 32
Filename: B13.SchDoc		

1

2

3

4

U_B33
B33.SchDoc



U_B34
B34.SchDoc



U_B35
B35.SchDoc



U_DDR3-RAM-PL1
DDR3-RAM-PL1.SchDoc



U_DDR3-RAM-PL2
DDR3-RAM-PL2.SchDoc



A

A

B

B

C

C

D

D



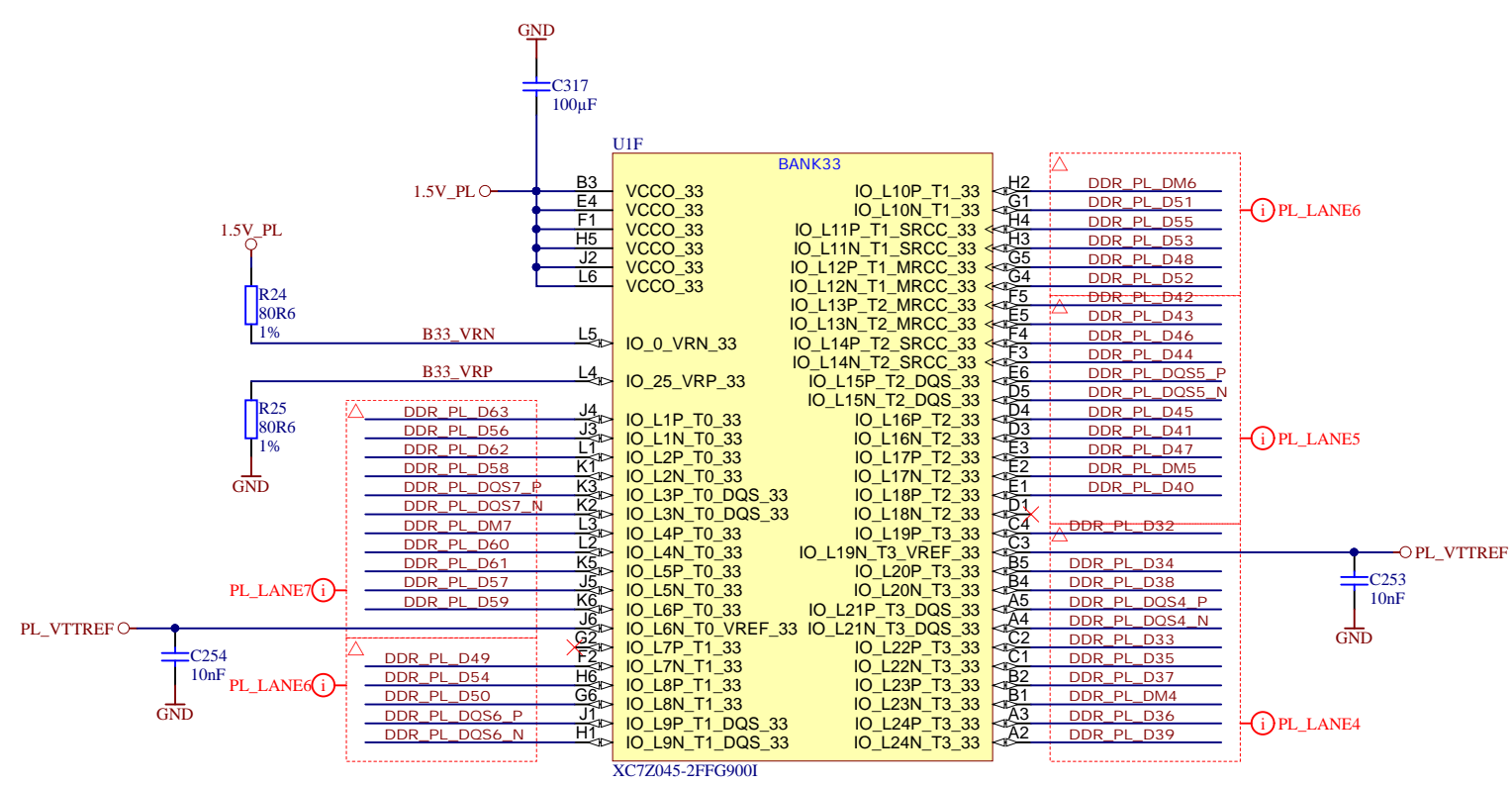
Title: FPGA HP Banks		
A4	Number: TE0783 045-2I	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 16 of 32
Filename: HP-BANKS.SchDoc		

1

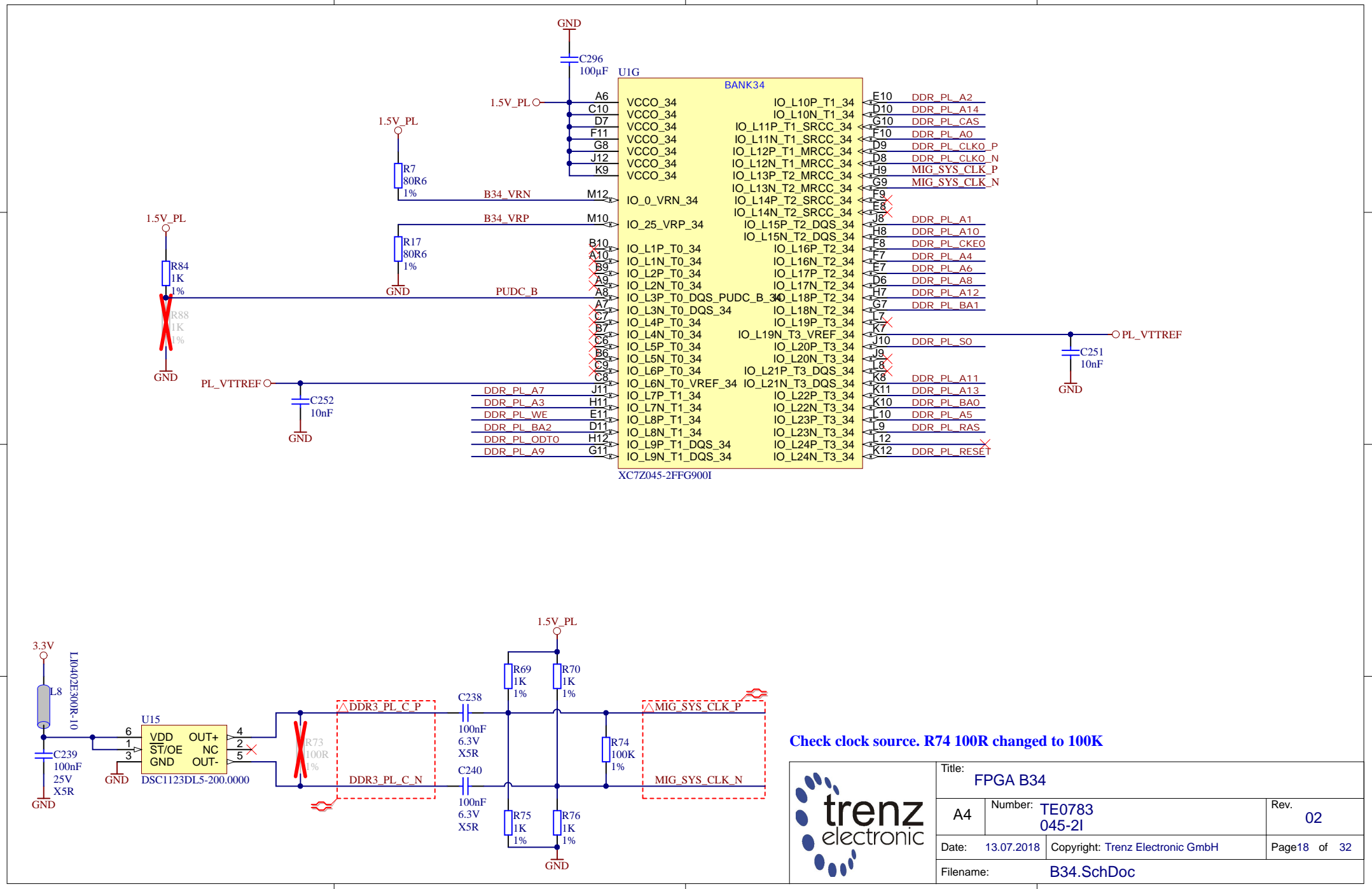
2

3

4



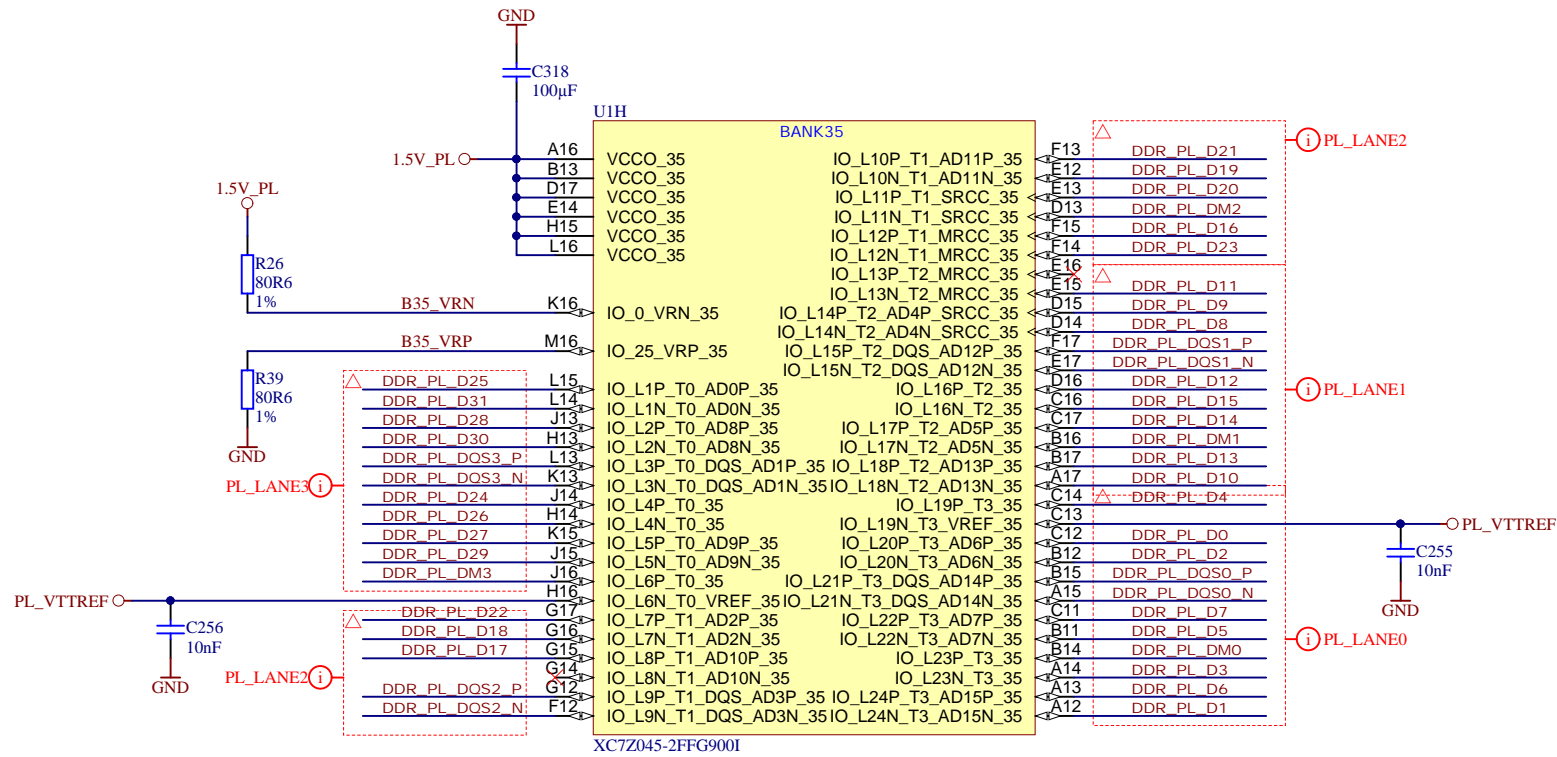
Title: FPGA B33		
A4	Number: TE0783 045-2I	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 17 of 32
Filename: B33.SchDoc		



Check clock source. R74 100R changed to 100K



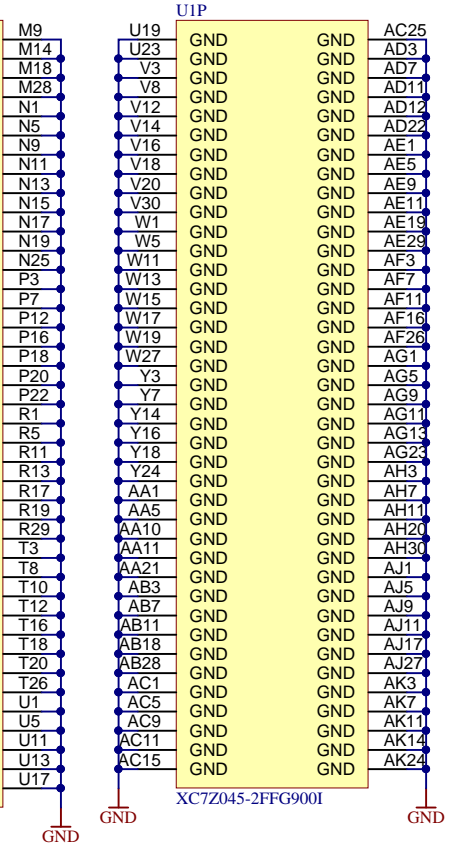
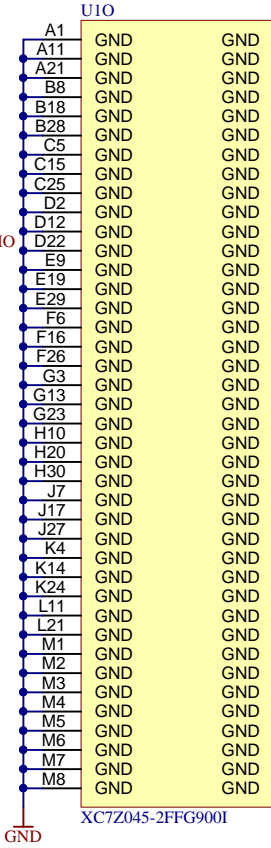
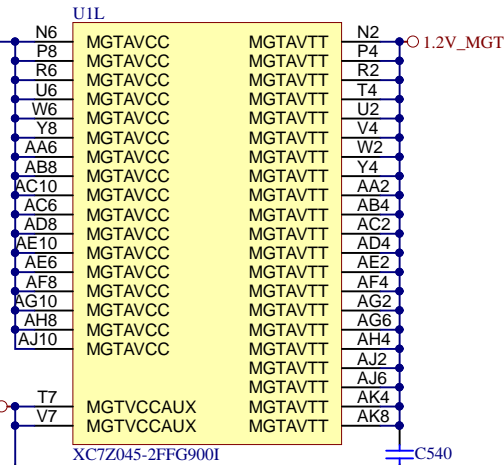
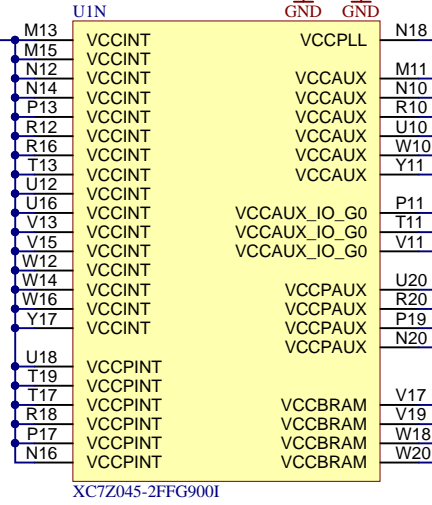
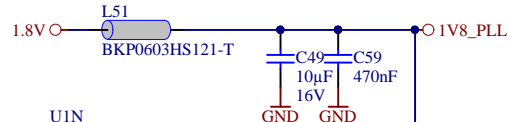
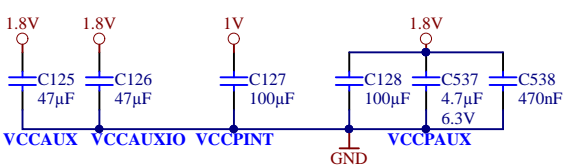
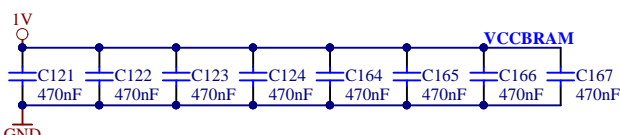
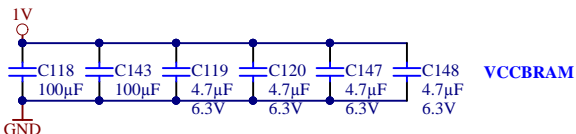
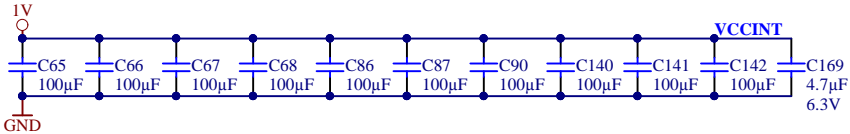
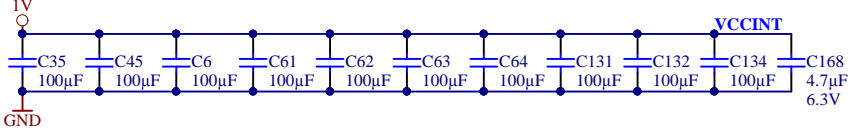
Title: FPGA B34		
A4	Number: TE0783 045-2I	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 18 of 32
Filename: B34.SchDoc		



XC7Z045-2FFG9001

	Title: FPGA B35		
	A4	Number: TE0783 045-2I	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 19 of 32
	Filename: B35.SchDoc		

Capacitors suitable for XC7Z100



Title: ZYNQ POWER		
A4	Number: TE0783 045-21	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page20 of 32
Filename: FPGA-PWR.SchDoc		

A

B

C

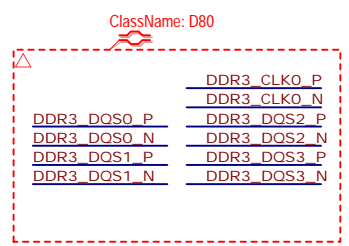
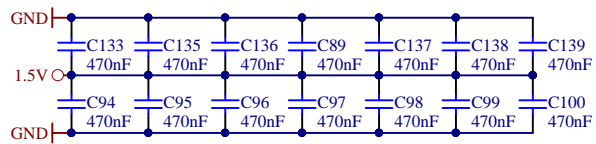
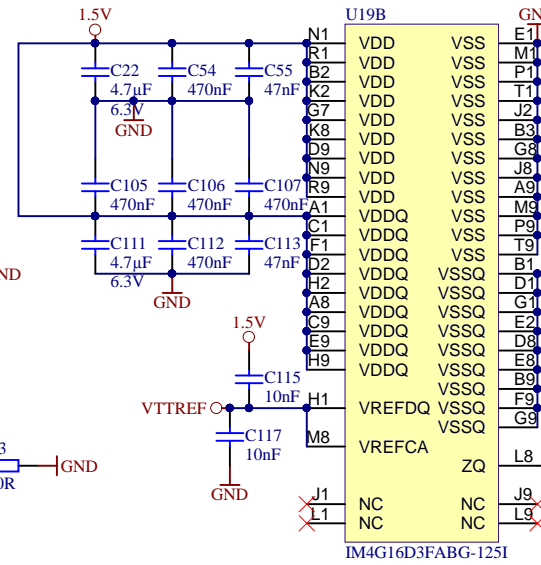
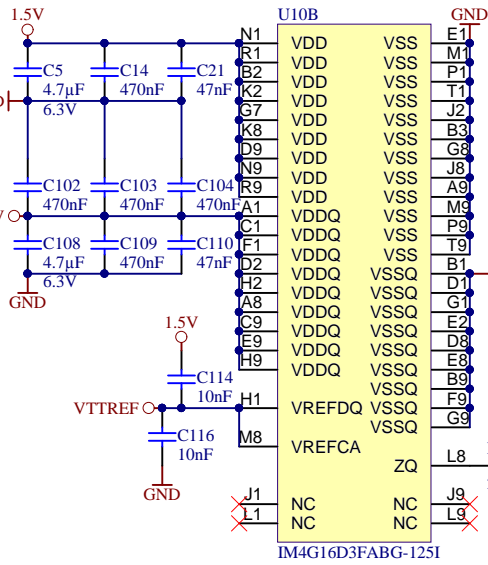
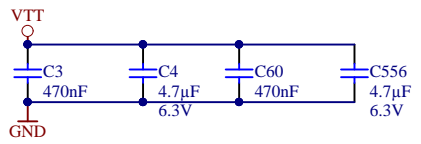
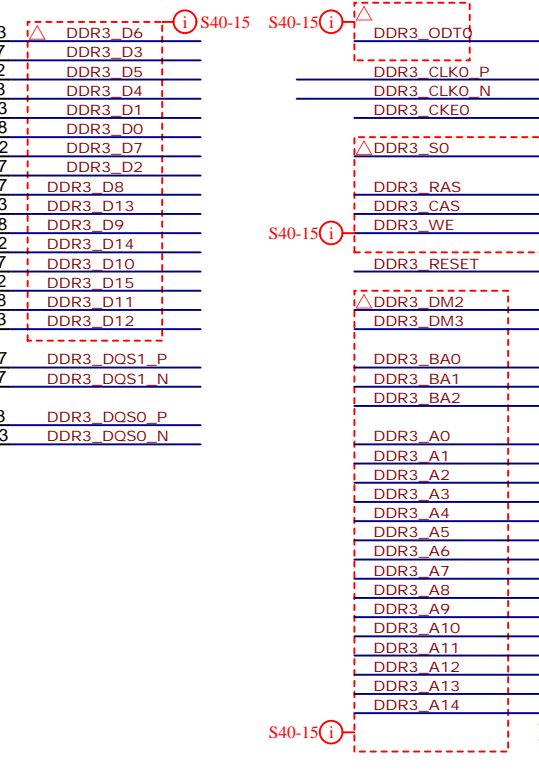
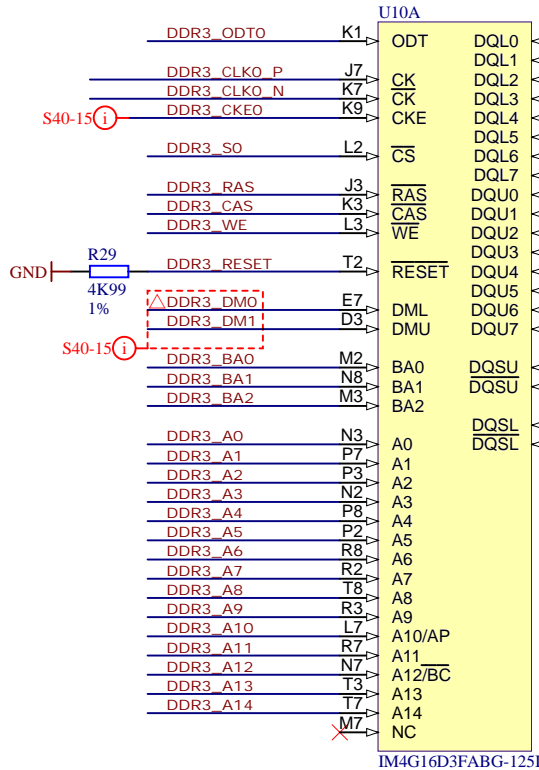
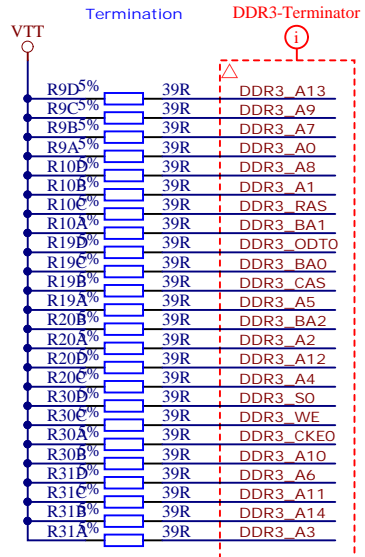
D

A

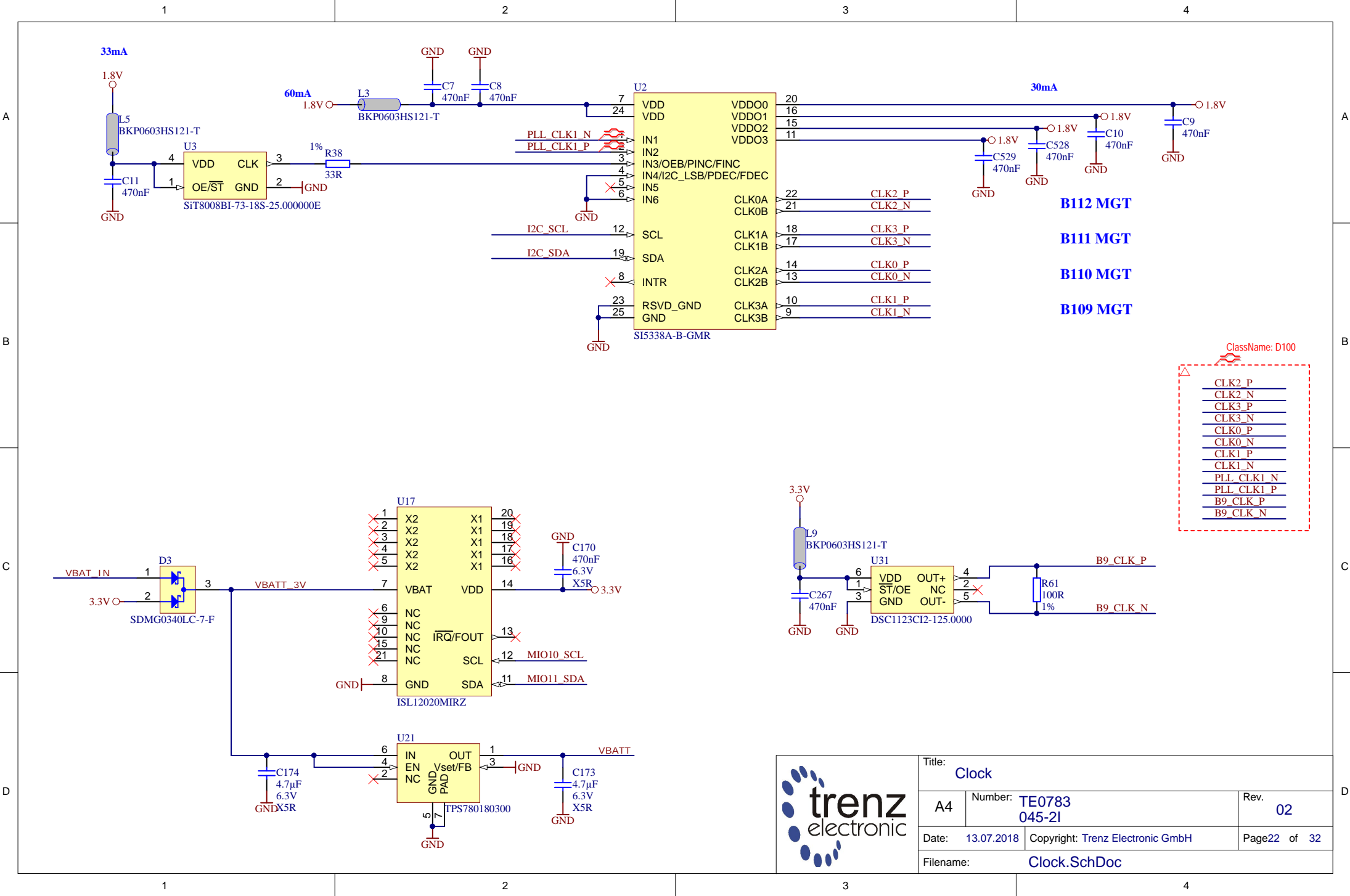
B

C

D



Title: DDR3 RAM PS		
A4	Number: TE0783 045-21	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 21 of 32
Filename: DDR3-RAM.SchDoc		



Title: Clock		
A4	Number: TE0783 045-21	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 22 of 32
Filename: Clock.SchDoc		

A

B

C

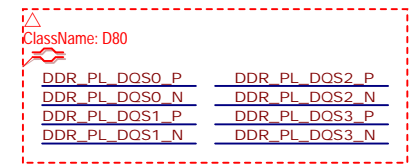
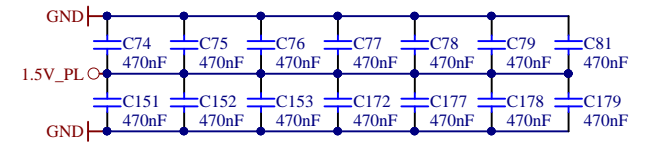
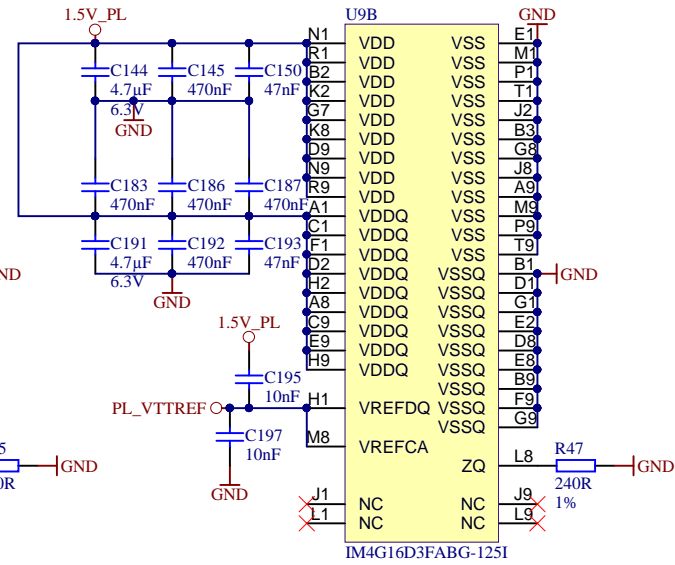
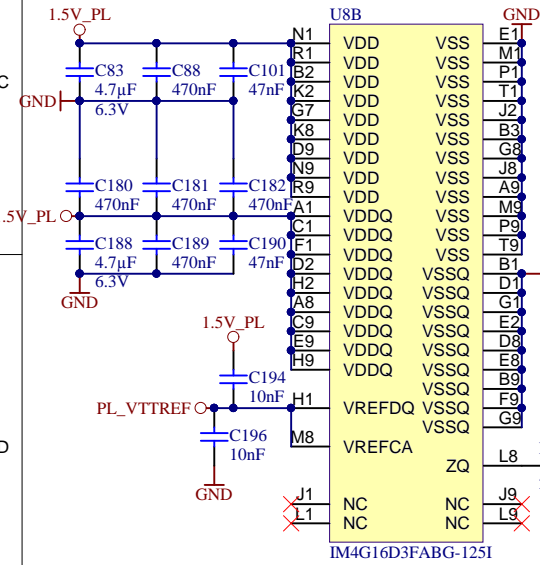
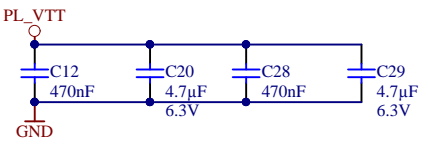
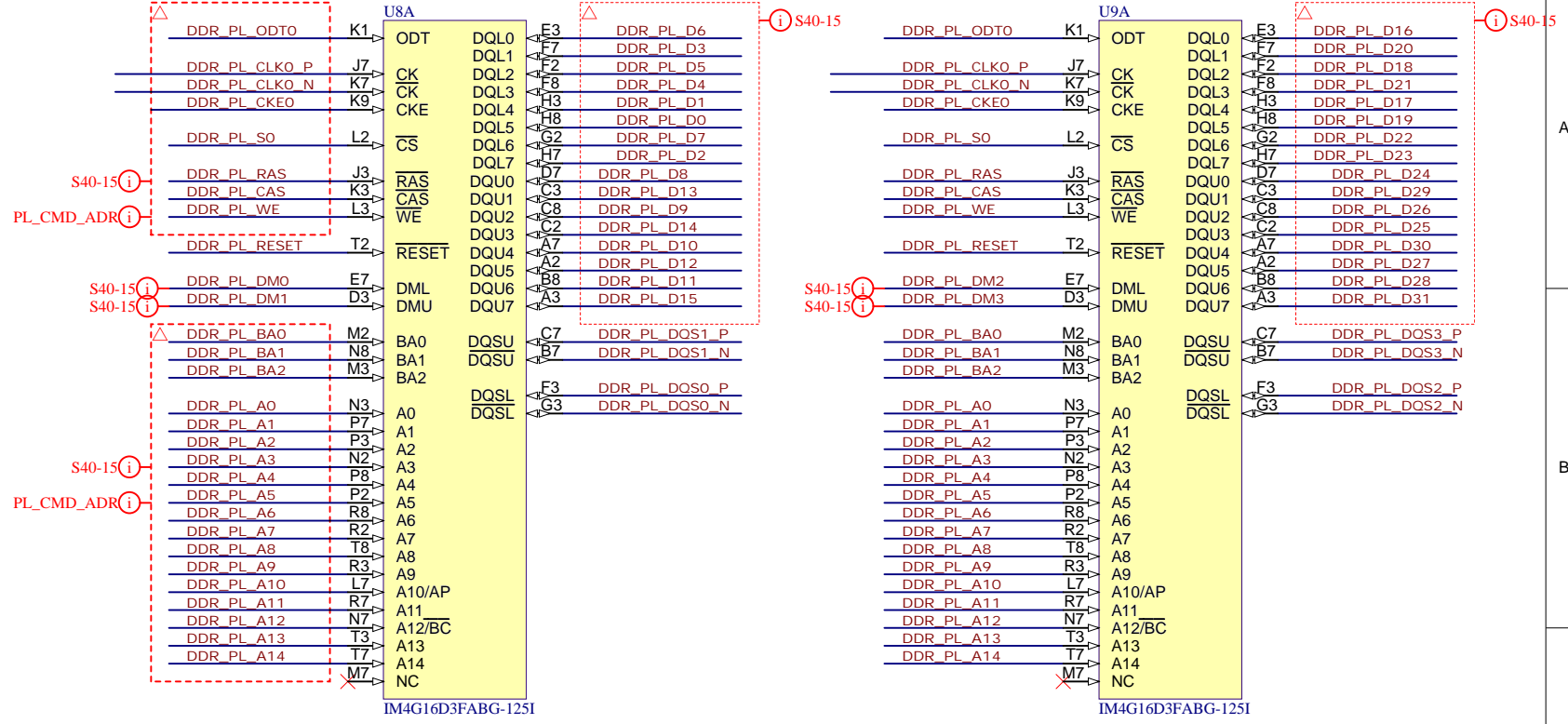
D

A

B

C

D



Title: DDR3 RAM PL		
A4	Number: TE0783 045-21	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 23 of 32
Filename: DDR3-RAM-PL1.SchDoc		

A

B

C

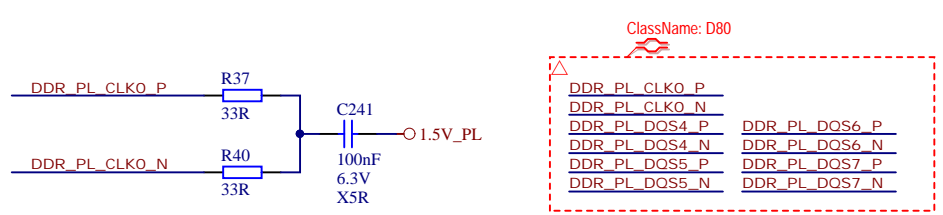
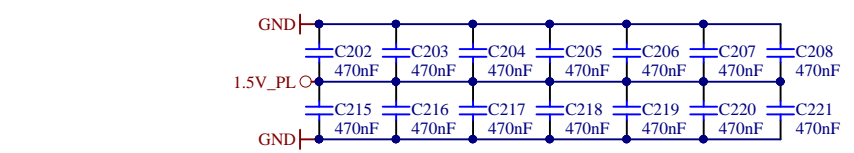
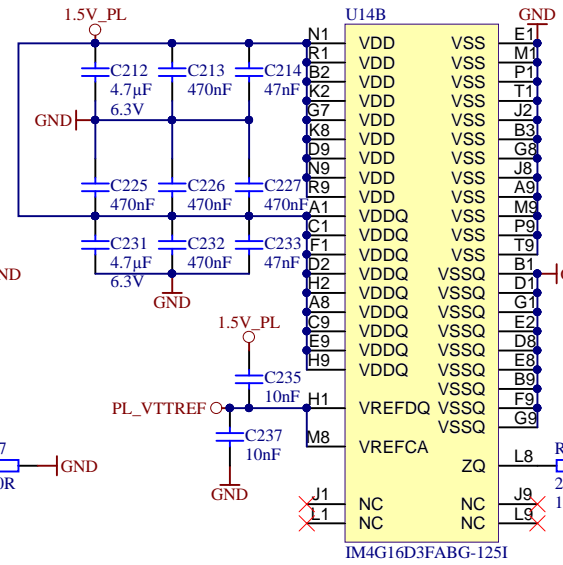
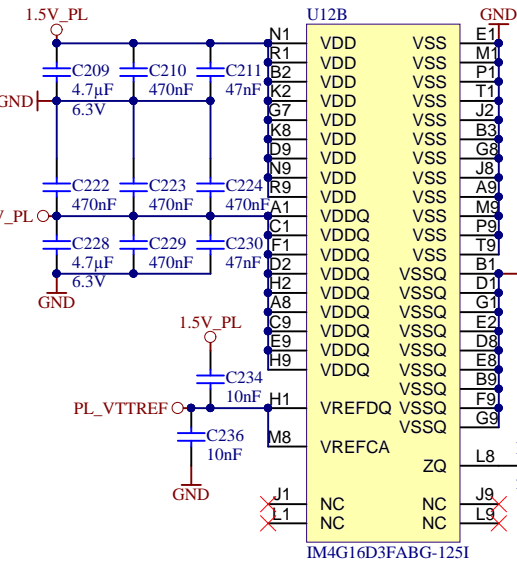
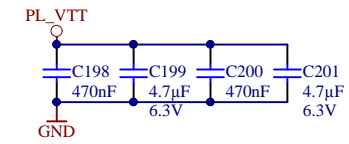
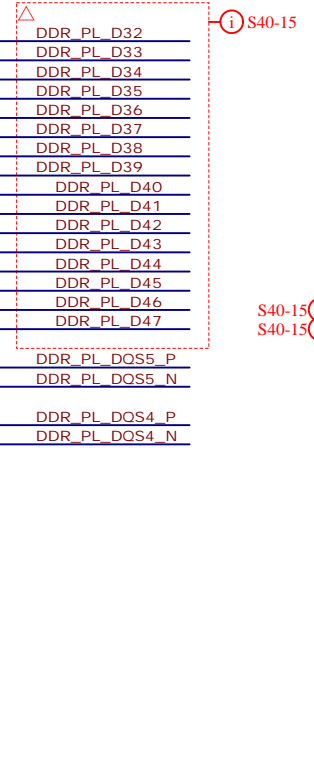
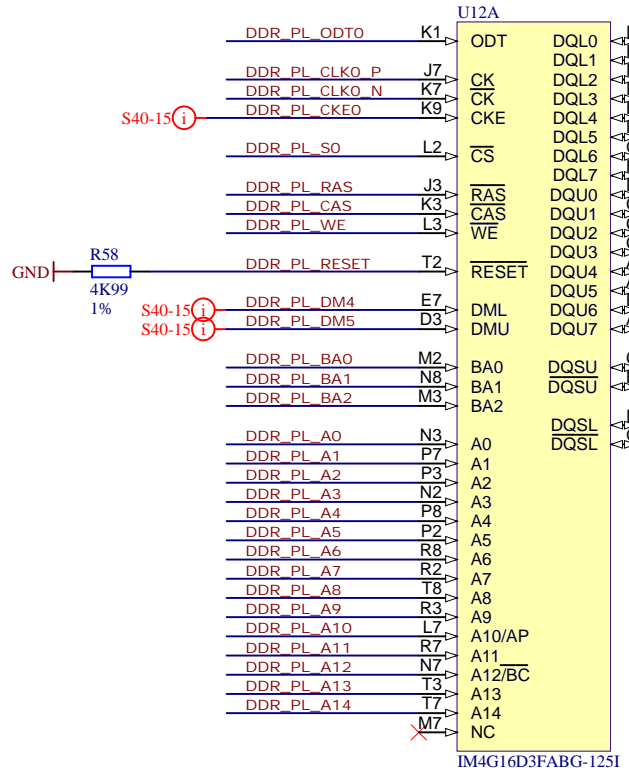
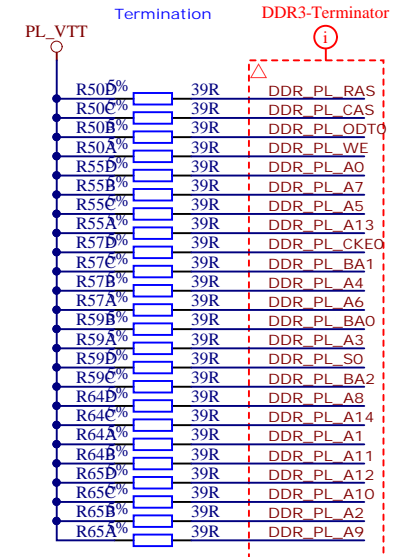
D

A

B

C

D



Title: DDR3 RAM PL		
A4	Number: TE0783 045-21	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 24 of 32
Filename: DDR3-RAM-PL2.SchDoc		

A

B

C

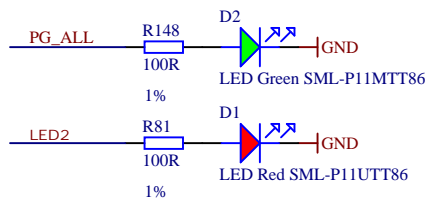
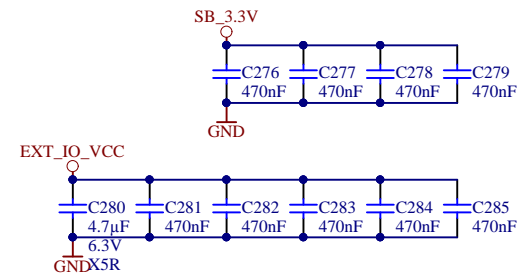
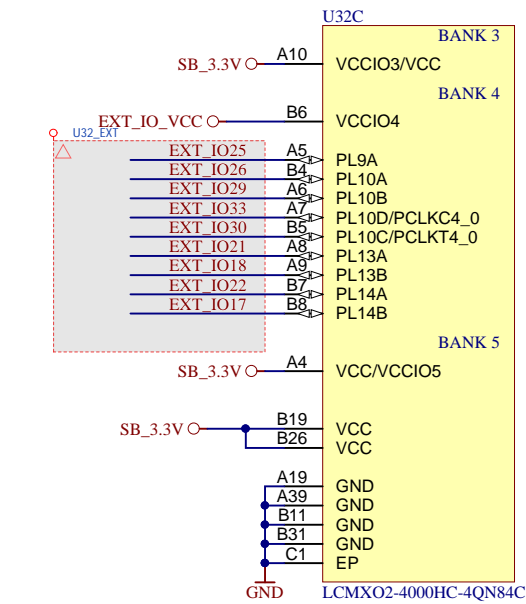
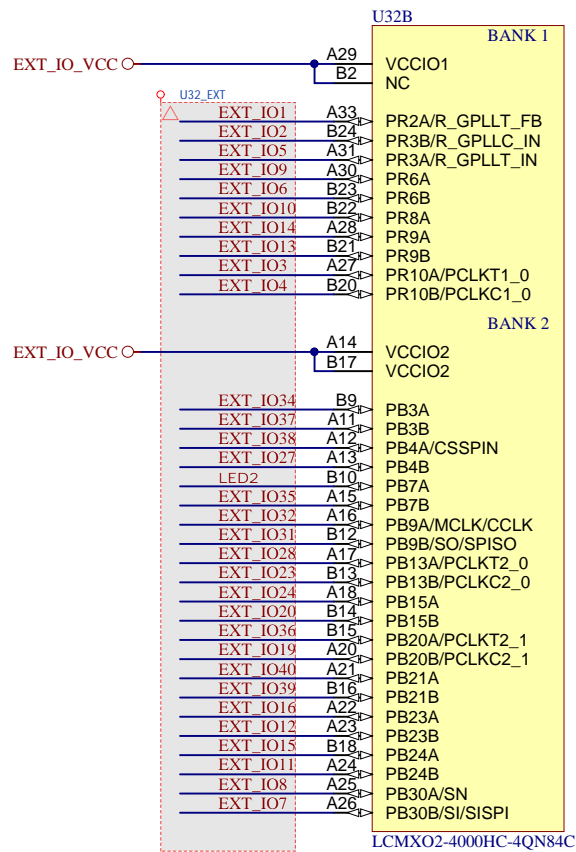
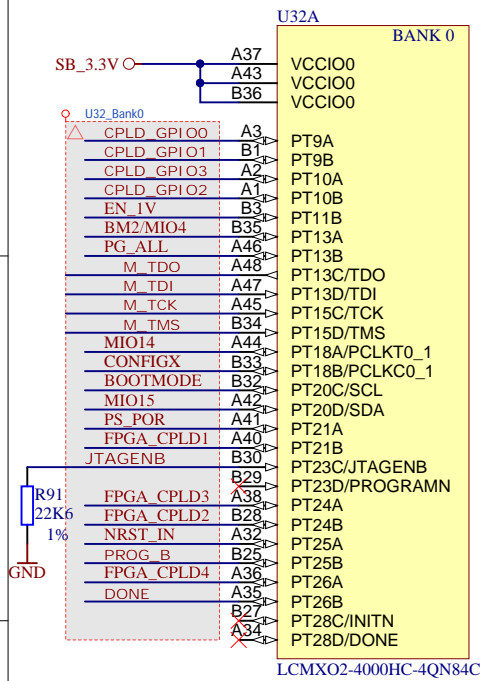
D

A

B

C

D



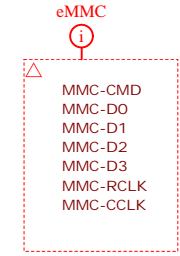
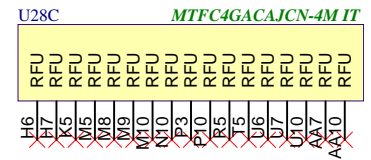
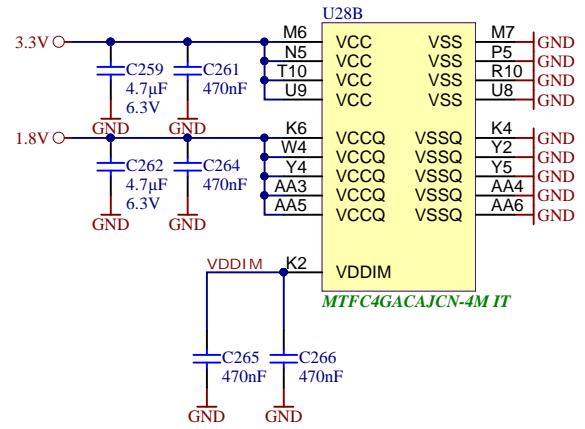
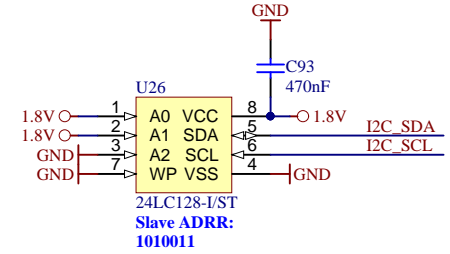
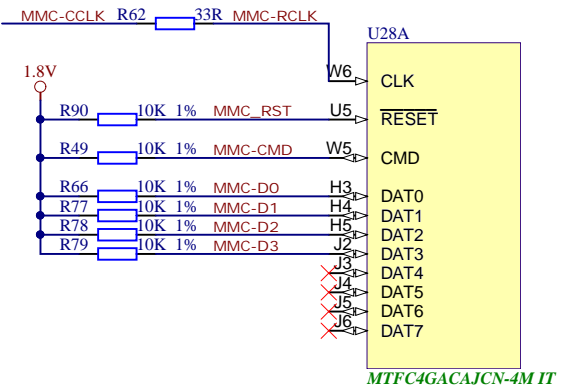
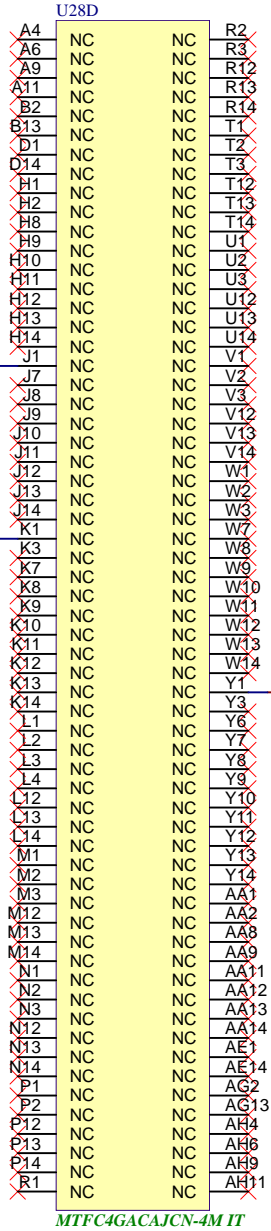
Title: CPLD		
A4	Number: TE0783 045-21	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 25 of 32
Filename: CPLD.SchDoc		

1

2

3

4



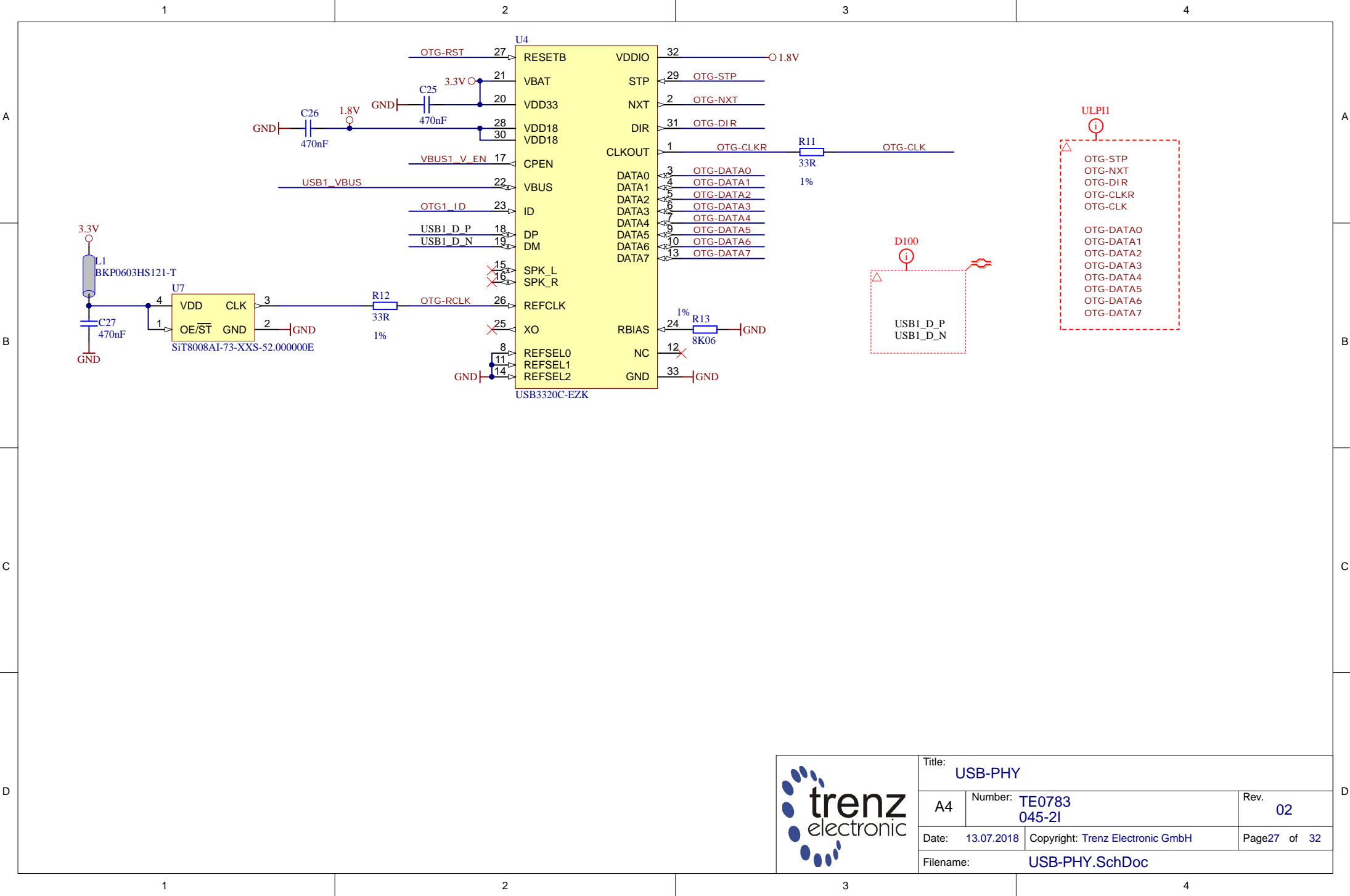
Title: eMMC		
A4	Number: TE0783 045-21	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page26 of 32
Filename: eMMC.SchDoc		


1

2

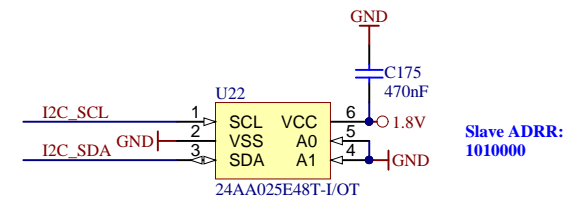
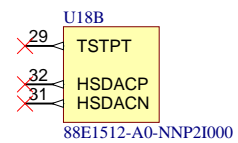
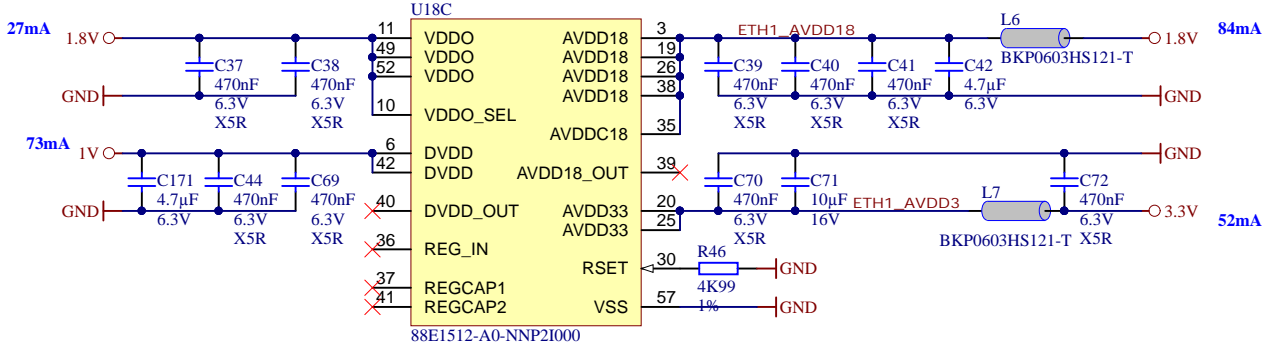
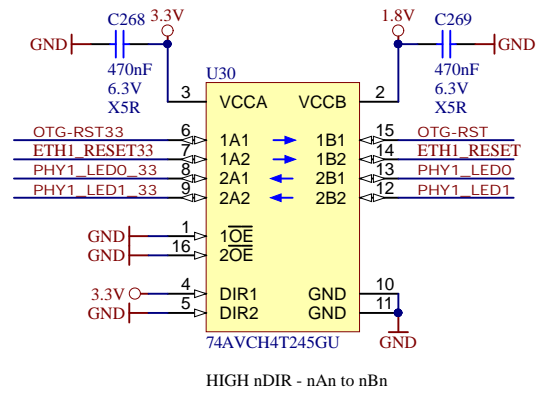
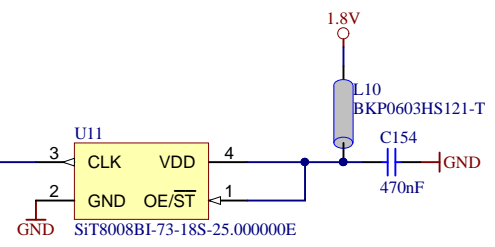
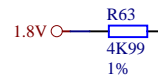
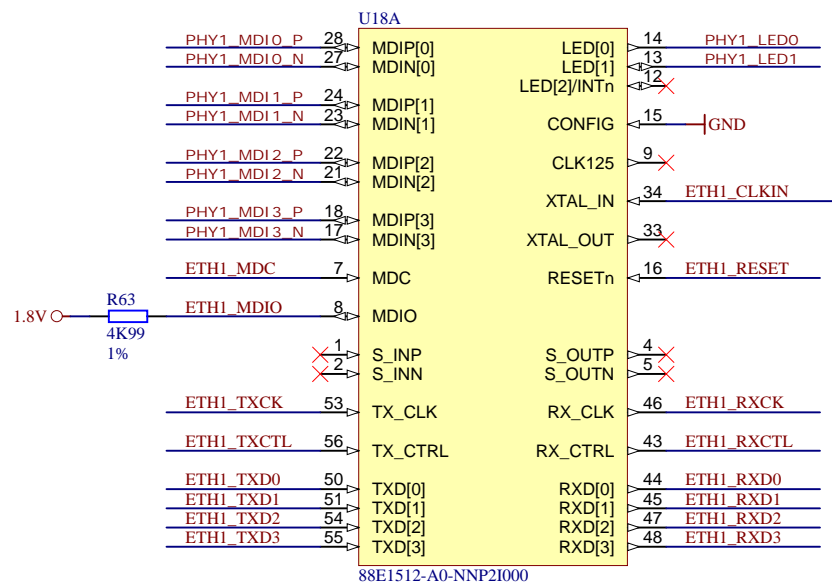
3

4

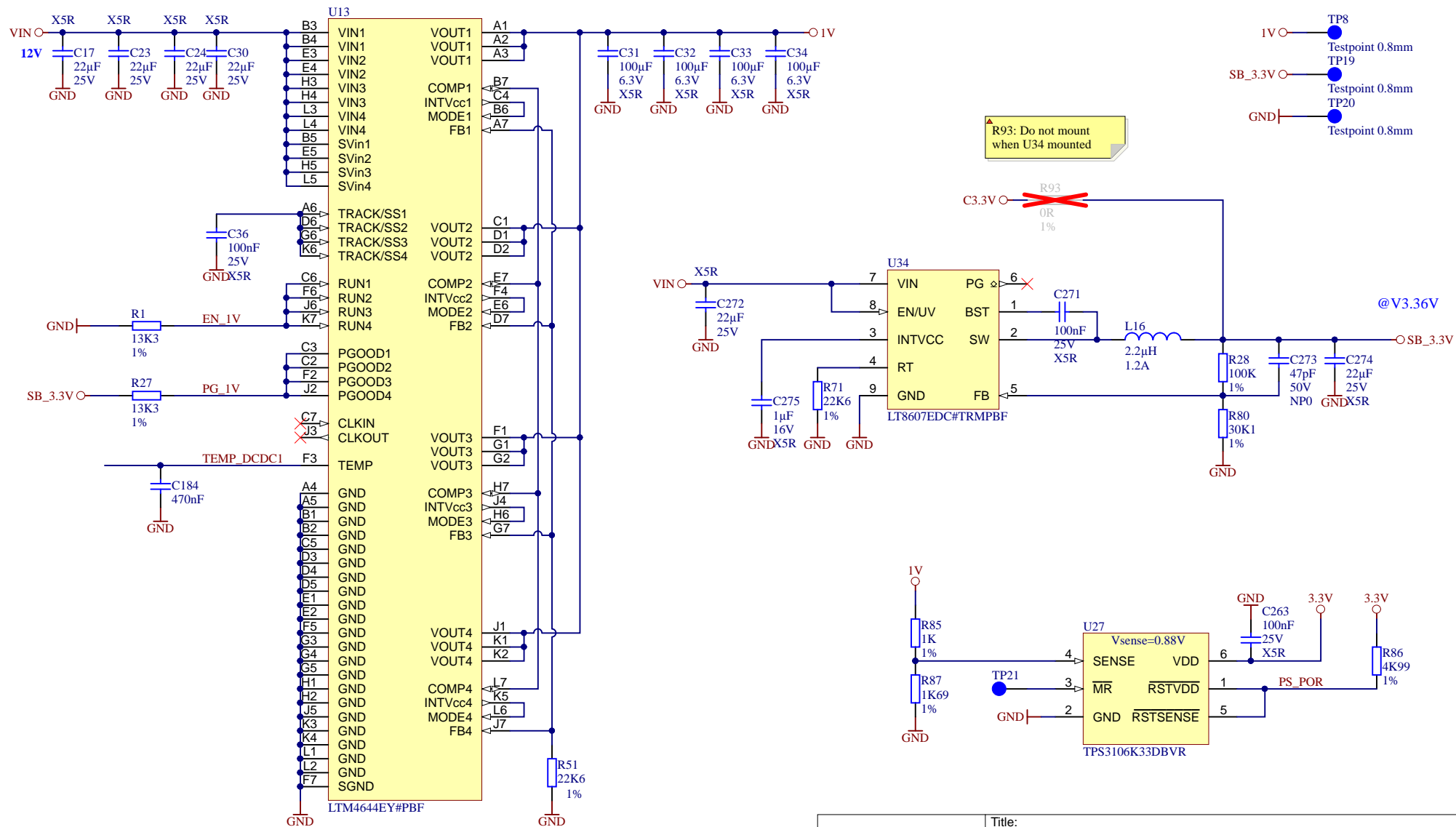


		Title: USB-PHY	
		A4	Number: TE0783 045-2I
Date: 13.07.2018		Copyright: Trenz Electronic GmbH	
Filename: USB-PHY.SchDoc		Page 27 of 32	

B9



Title: ETH_PHY1		
A4	Number: TE0783 045-21	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 28 of 32
Filename: ETH1.SchDoc		



	Title: POWER	
	A4	Number: TE0783 045-21
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH
	Filename: POWER.SchDoc	Rev. 02

R93: Do not mount when U34 mounted

- 1V ○ TP8 Testpoint 0.8mm
- SB_3.3V ○ TP19 Testpoint 0.8mm
- GND TP20 Testpoint 0.8mm

@V3.36V

Vsense=0.88V

1

2

3

4

1

2

3

4

A

A

B

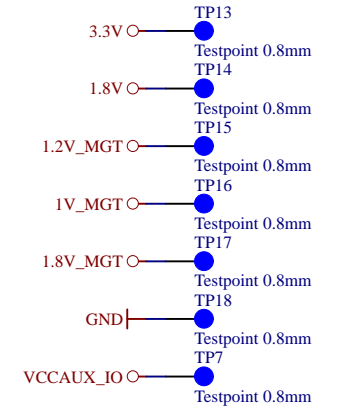
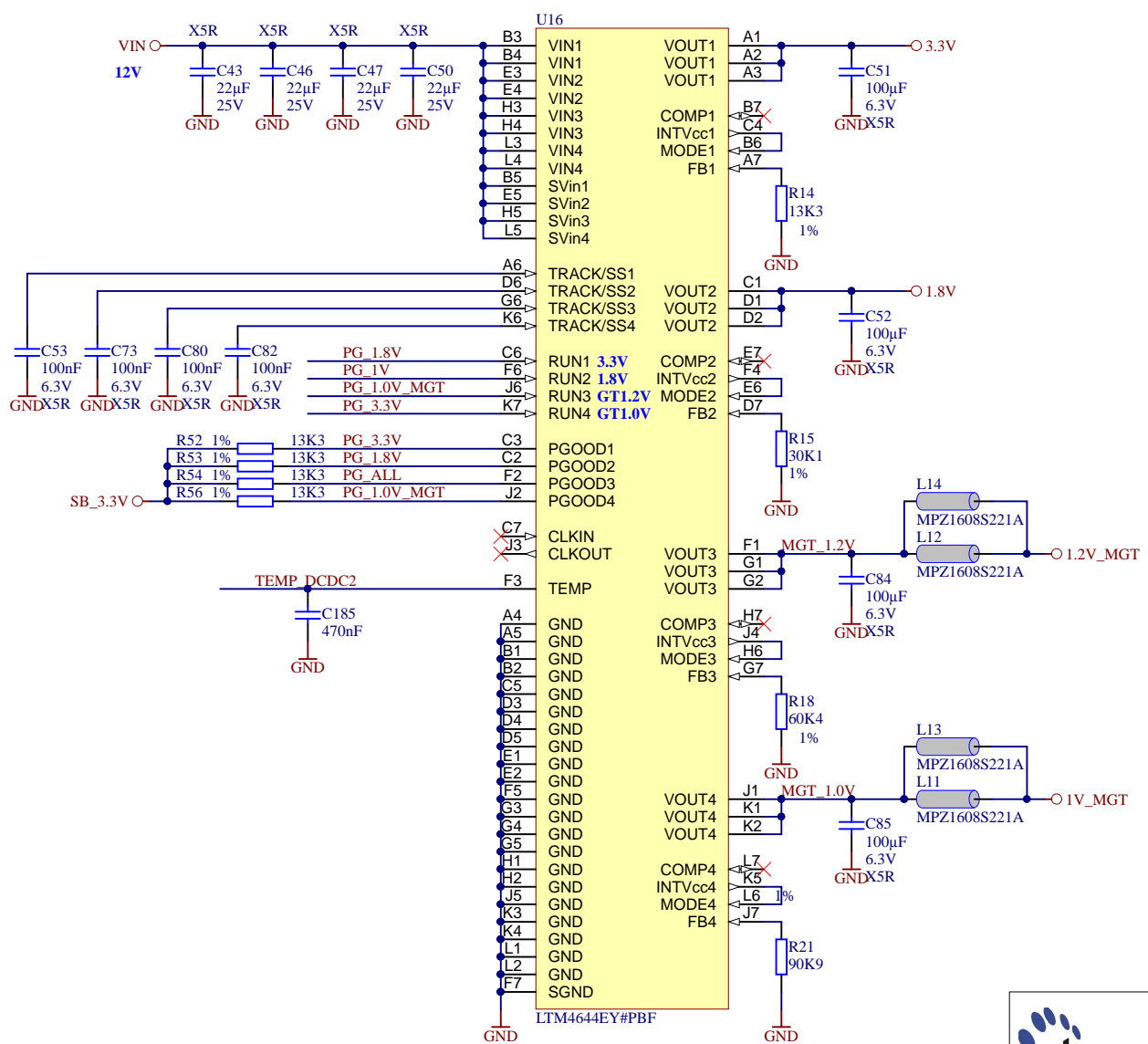
B

C

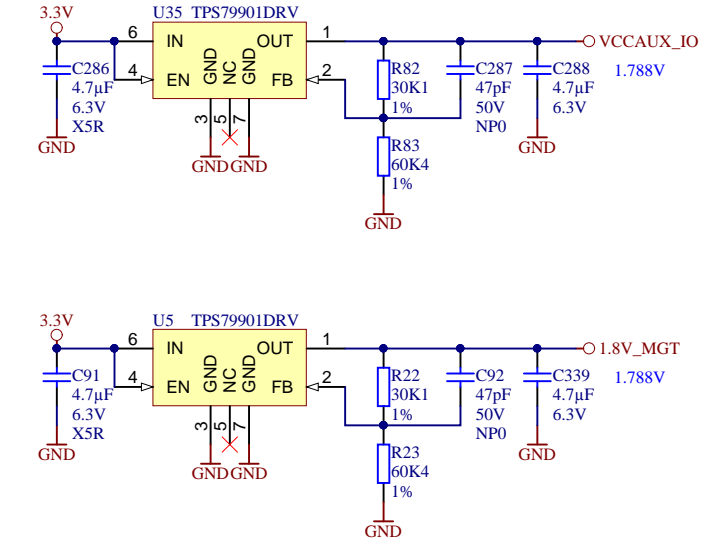
C


D

D



CLK 666.67 and faster - VCCAUX_IO 2.0V



			Title: POWER 2	
			A4	Number: TE0783 045-21
Date: 13.07.2018		Copyright: Trenz Electronic GmbH		Page30 of 32
Filename: POWER2.SchDoc				

1

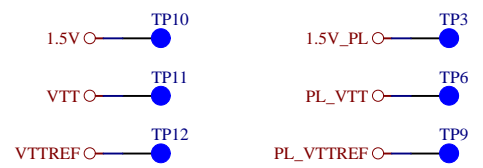
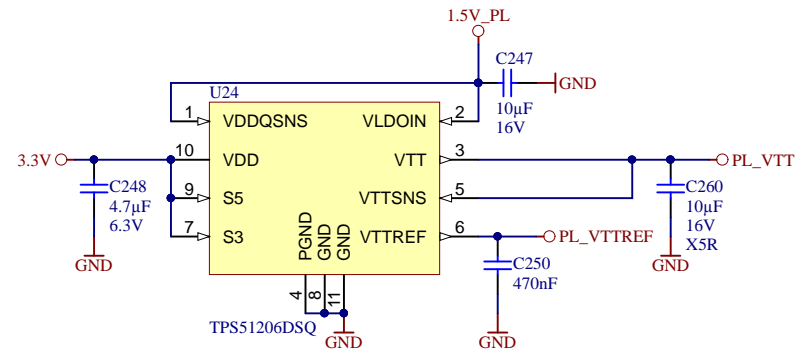
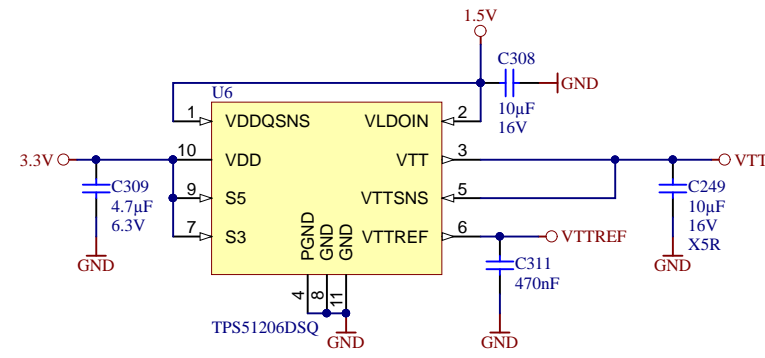
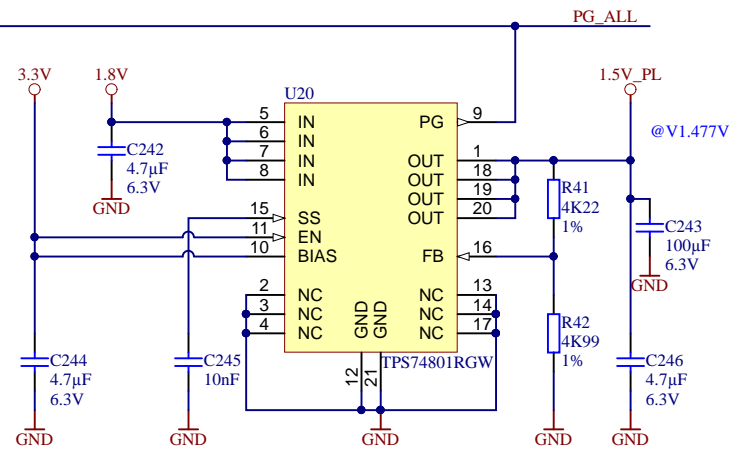
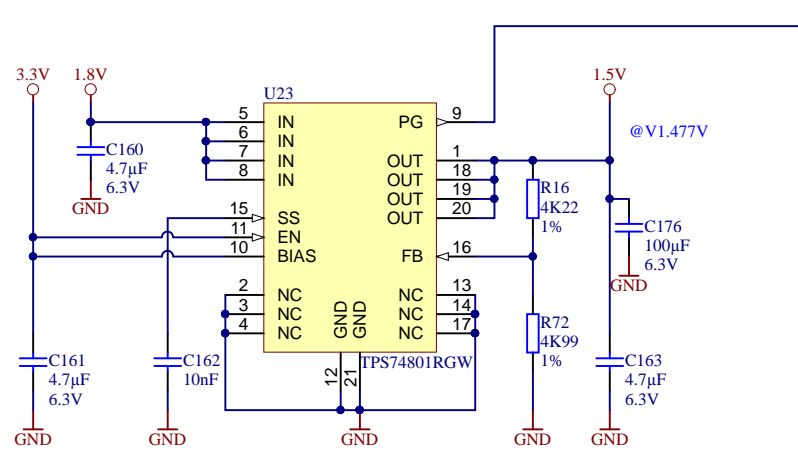
2

3

4

DDR3 PS

DDR3 PL



Title: POWER 2		
A4	Number: TE0783 045-21	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page31 of 32
Filename: POWER3.SchDoc		

1

2

3

4

1

2

3

4

REV. 02:

1) Changed power-up sequence: 3.3V next to 1.8V. MGT power domain next to 3.3V

A

A

B


B

C

C

D

D

		Title: Revision Changes	
		A4	Number: TE0783 045-2I
Date: 13.07.2018		Copyright: Trenz Electronic GmbH / TT	
Filename: Revision Changes.SchDoc		Page 32 of 32	

1

2

3

4