

U\_SOC  
SOC.SchDoc

U\_DDR3-RAM  
DDR3-RAM.SchDoc

U\_CPLD  
CPLD.SchDoc

U\_USB-PHY  
USB-PHY.SchDoc

U\_ETH1  
ETH1.SchDoc

U\_Clock  
Clock.SchDoc

U\_eMMC  
eMMC.SchDoc

U\_POWER2  
POWER2.SchDoc

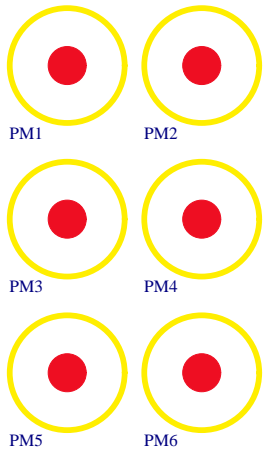
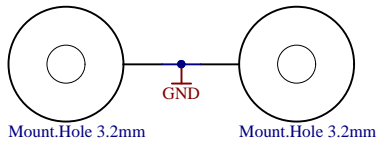
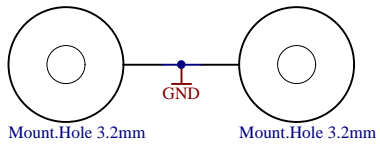
U\_Connectors  
Connectors.SchDoc

U\_Rev\_changes  
Revision Changes.SchDoc

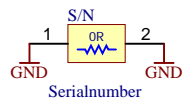
U\_POWER  
POWER.SchDoc

U\_POWER3  
POWER3.SchDoc

LOGO1  
TE Logo PRINT Layer  
LOGO PRINT



Serial  
Serialnumber 6,3 x 6.3mm



Title: <b>Overview</b>		
A4	Number: <b>TE0783 100-2I</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page1 of 32
Filename: <b>TE0783.SchDoc</b>		

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A

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U\_HSMC\_CONN\_J1  
HSMC\_CONN\_J1.SchDoc



U\_HSMC\_CONN\_J2  
HSMC\_CONN\_J2.SchDoc



U\_HSMC\_CONN\_J3  
HSMC\_CONN\_J3.SchDoc



B

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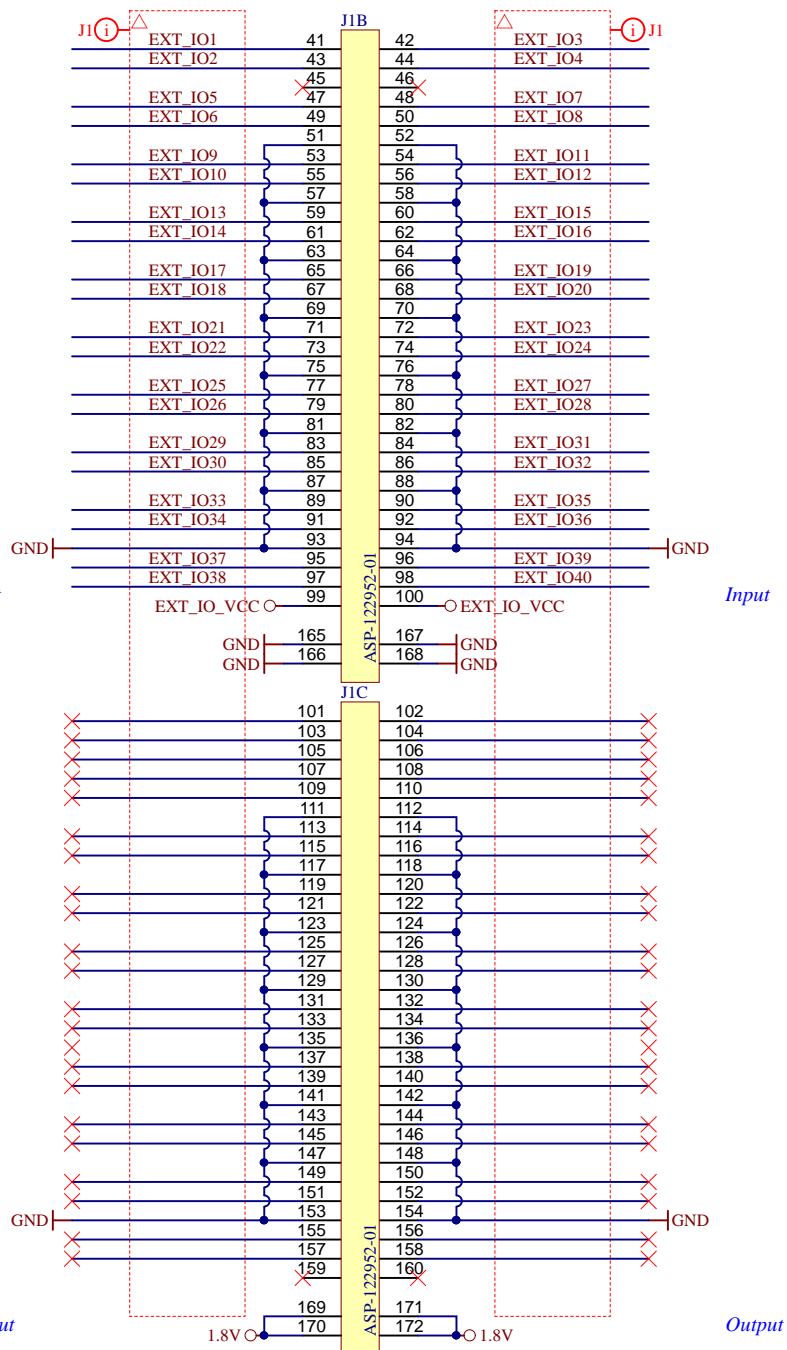
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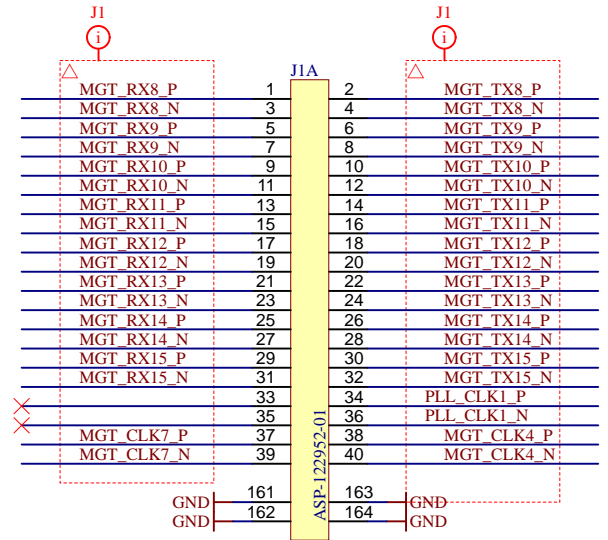
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			Title: <b>Connectors</b>		
			A4	Number: <b>TE0783 100-2I</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>		Copyright: <b>Trenz Electronic GmbH</b>		Page <b>2</b> of <b>32</b>	
Filename: <b>Connectors.SchDoc</b>					



Next signals has different functionality in TE0782 and TEBT0782.

TE0782  
 J1\_TX20\_N  
 J1\_TX20\_P  
 J1\_TX21\_N  
 J1\_TX21\_P

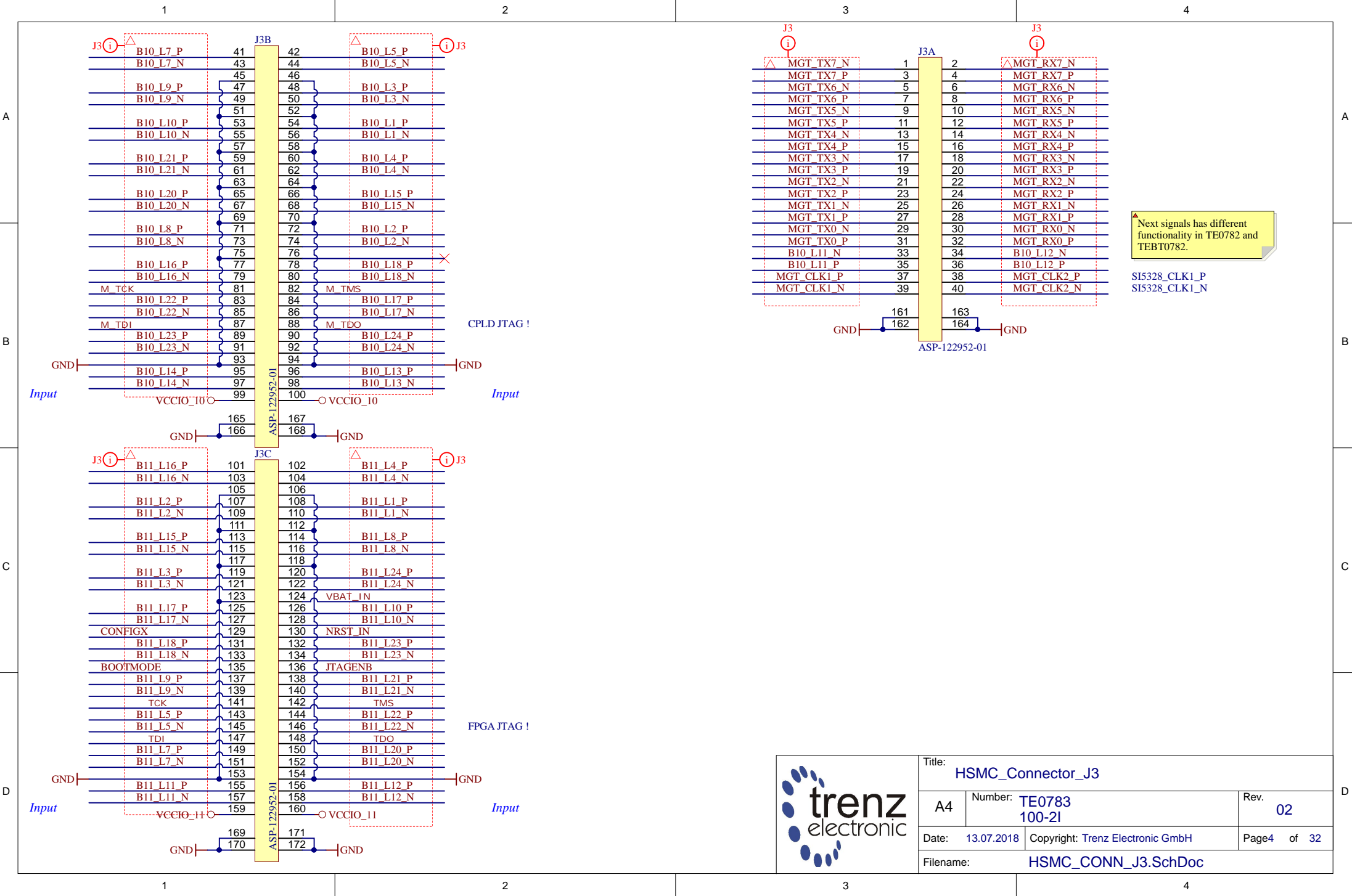


Next signals has different functionality in TE0782 and TEBT0782.

TE0782  
 J1\_RX20\_N  
 J1\_RX20\_P



Title: <b>HSMC_Connector_J1</b>		
A4	Number: <b>TE0783 100-21</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>3</b> of <b>32</b>
Filename: <b>HSMC_CONN_J1.SchDoc</b>		



▲ Next signals has different functionality in TE0782 and TEBT0782.

S15328\_CLK1\_P  
S15328\_CLK1\_N



Title: HSMC_Connector_J3		
A4	Number: TE0783 100-21	Rev. 02
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Filename: HSMC_CONN_J3.SchDoc		

A

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C

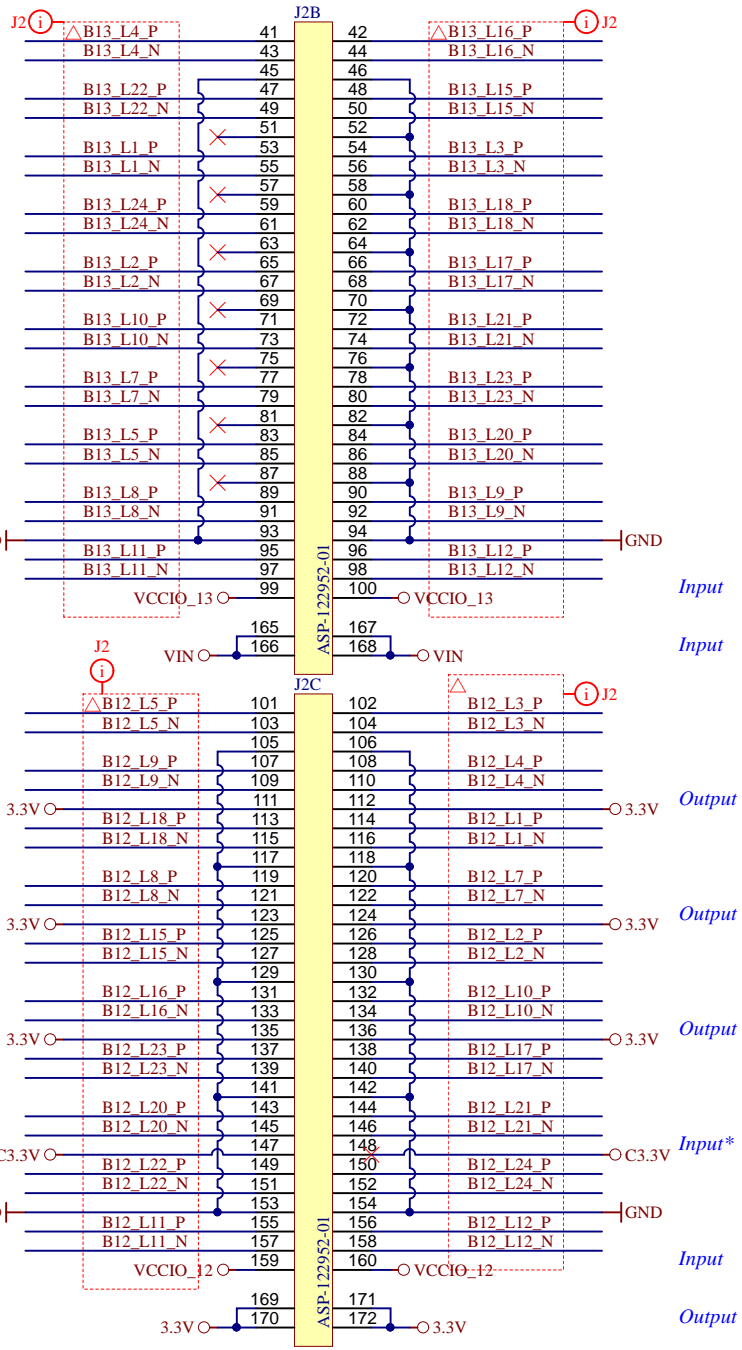
D

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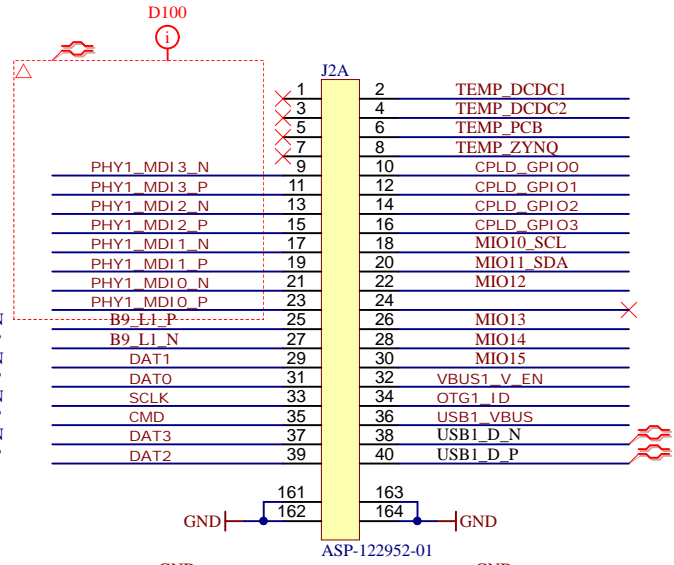
C

D



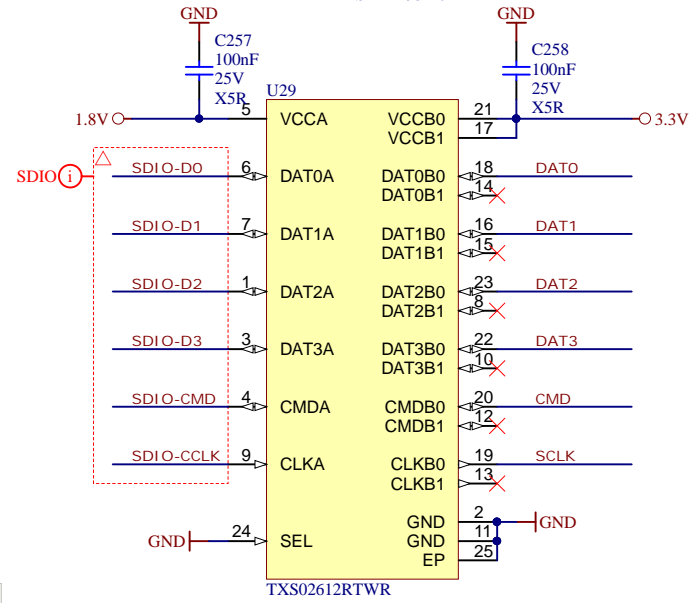
Next signals has different functionality in TE0782 and TEBT0782.

TE0782  
PHY2\_MDI3\_N  
PHY2\_MDI3\_P  
PHY2\_MDI2\_N  
PHY2\_MDI2\_P  
PHY2\_MDI1\_N  
PHY2\_MDI1\_P  
PHY2\_MDI0\_N  
PHY2\_MDI0\_P



Next signals has different functionality in TE0782 and TEBT0782.

TE0782  
CPLD\_GPIO4  
CPLD\_GPIO5  
OTG2\_ID  
USB2\_VBUS  
USB2\_D\_N  
USB2\_D\_P  
VBUS2\_V\_EN



SDCARD  
DAT0  
DAT1  
DAT2  
DAT3  
CMD  
SCLK

\* - C3.3V: Normally leave unconnected



Title: HSMC_Connector_J2		
A4	Number: TE0783 100-21	Rev. 02
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Filename: HSMC_CONN_J2.SchDoc		

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A

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U\_PS-DDR  
PS-DDR.SchDoc



U\_B9  
B9.SchDoc



U\_MIO-BANKS  
MIO-BANKS.SchDoc



U\_B10  
B10.SchDoc



U\_HP-BANKS  
HP-BANKS.SchDoc



U\_B11  
B11.SchDoc



B

B

U\_FPGA-MGT  
FPGA-MGT.SchDoc



U\_B12  
B12.SchDoc



U\_FPGA-CFG  
FPGA-CFG.SchDoc



U\_B13  
B13.SchDoc



C

C

U\_FPGA-PWR  
FPGA-PWR.SchDoc



D

D



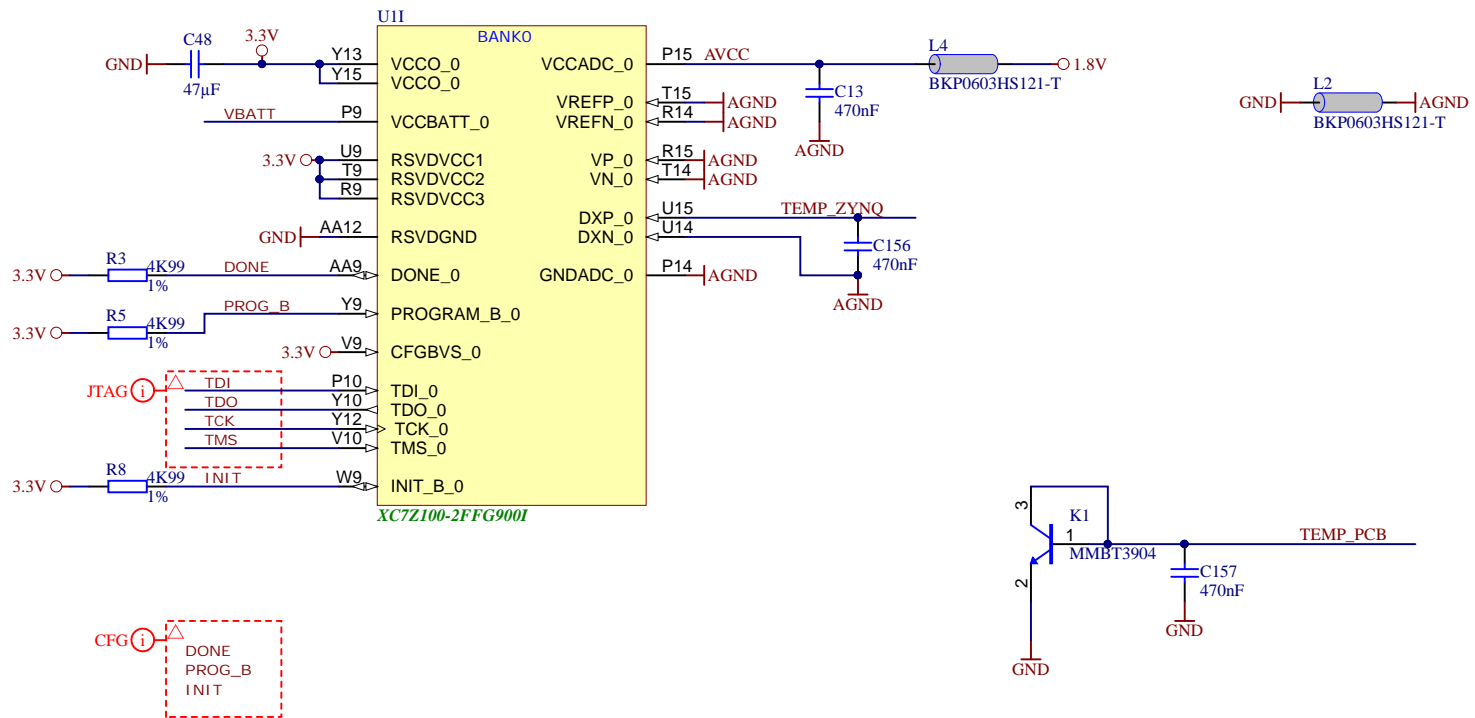
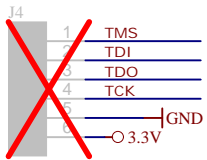
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A4	Number: <b>TE0783 100-2I</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>6</b> of <b>32</b>
Filename: <b>SOC.SchDoc</b>		

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	Title: <b>FPGA Configuration</b>		
	A4	Nummer: <b>TE0783 100-21</b>	Rev. <b>02</b>
	Datum: 13.07.2018	Zeichner: Trenz Electronic GmbH	Blatt 7 von 32
	Filename: <b>FPGA-CFG.SchDoc</b>		

A

A

B

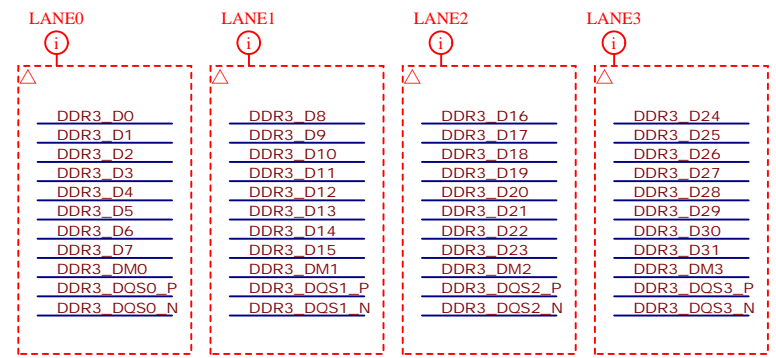
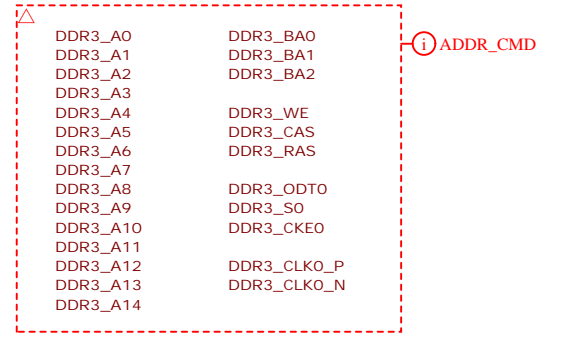
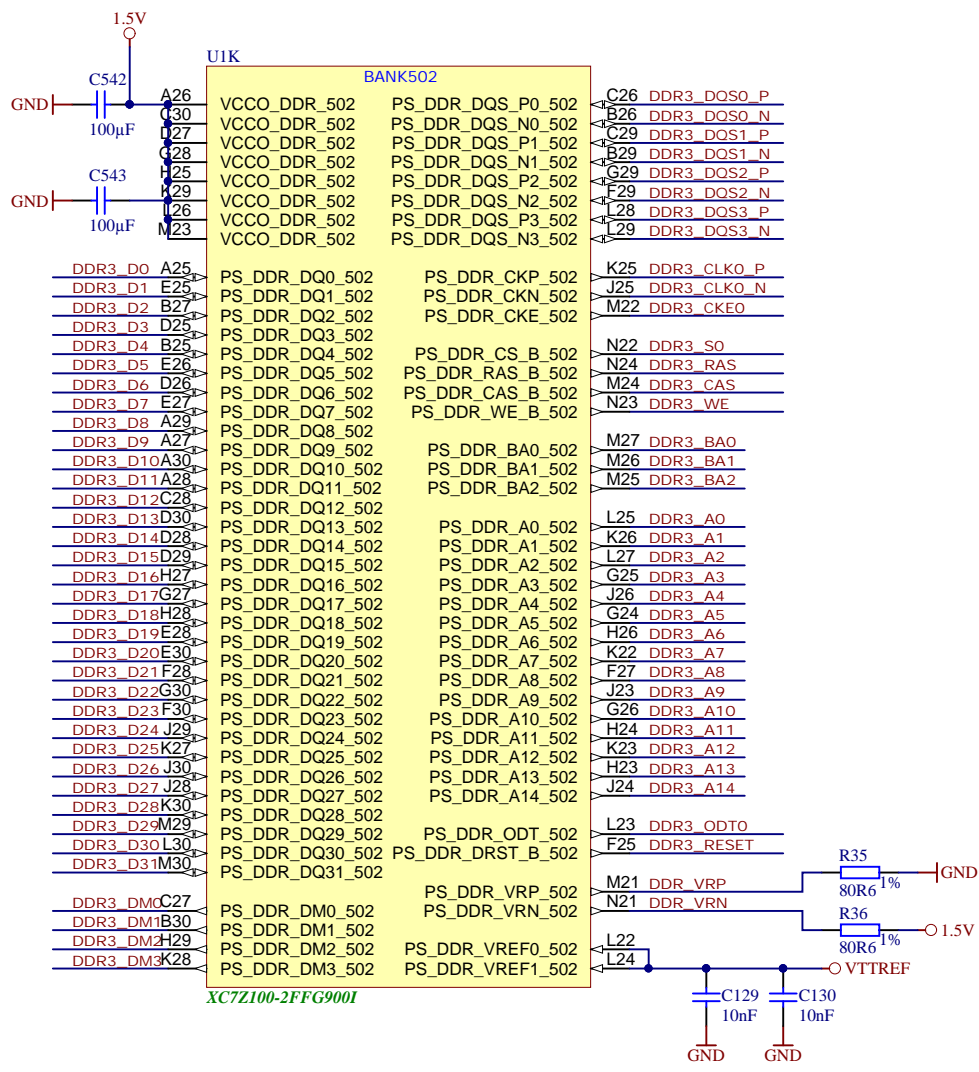
B

C

C

D

D



Title: <b>FPGA DDR Banks</b>		
A4	Number: <b>TE0783 100-21</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>8</b> of <b>32</b>
Filename: <b>PS-DDR.SchDoc</b>		



U1M

ClassName: MGT\_TX

D100

BANK109

MGT\_CLK2\_P AD10  
 MGT\_CLK2\_N AD9  
 MGT\_CLK3\_P AF10  
 MGT\_CLK3\_N AF9  
 MGTREFCLK0P\_109  
 MGTREFCLK0N\_109  
 MGTREFCLK1P\_109  
 MGTREFCLK1N\_109

MGTXTXP0\_109  
 MGTXTXN0\_109  
 MGTXTXP1\_109  
 MGTXTXN1\_109  
 MGTXRXP2\_109  
 MGTXTXN2\_109  
 MGTXTXP3\_109  
 MGTXTXN3\_109

AK10 MGT\_TX0\_P  
 AK9 MGT\_TX0\_N  
 AK6 MGT\_TX1\_P  
 AK5 MGT\_TX1\_N  
 AJ4 MGT\_TX2\_P  
 AJ3 MGT\_TX2\_N  
 AK2 MGT\_TX3\_P  
 AK1 MGT\_TX3\_N

BANK110

MGT\_CLK0\_P AA8  
 MGT\_CLK0\_N AA7  
 MGT\_CLK1\_N AC8  
 MGT\_CLK1\_P AC7  
 MGTREFCLK0P\_110  
 MGTREFCLK0N\_110  
 MGTREFCLK1P\_110  
 MGTREFCLK1N\_110

MGTXTXP0\_110  
 MGTXTXN0\_110  
 MGTXTXP1\_110  
 MGTXTXN1\_110  
 MGTXTXP2\_110  
 MGTXTXN2\_110  
 MGTXTXP3\_110  
 MGTXTXN3\_110

AH2 MGT\_TX4\_P  
 AH1 MGT\_TX4\_N  
 AF2 MGT\_TX5\_P  
 AF1 MGT\_TX5\_N  
 AE4 MGT\_TX6\_P  
 AE3 MGT\_TX6\_N  
 AD2 MGT\_TX7\_P  
 AD1 MGT\_TX7\_N

BANK111

MGT\_CLK4\_N U8  
 MGT\_CLK4\_P U7  
 MGT\_CLK5\_P W8  
 MGT\_CLK5\_N W7  
 MGTREFCLK0P\_111  
 MGTREFCLK0N\_111  
 MGTREFCLK1P\_111  
 MGTREFCLK1N\_111

MGTXTXP0\_111  
 MGTXTXN0\_111  
 MGTXTXP1\_111  
 MGTXTXN1\_111  
 MGTXTXP2\_111  
 MGTXTXN2\_111  
 MGTXTXP3\_111  
 MGTXTXN3\_111

AB2 MGT\_TX8\_P  
 AB1 MGT\_TX8\_N  
 Y2 MGT\_TX9\_P  
 Y1 MGT\_TX9\_N  
 W4 MGT\_TX10\_P  
 W3 MGT\_TX10\_N  
 V2 MGT\_TX11\_P  
 V1 MGT\_TX11\_N

BANK112

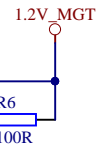
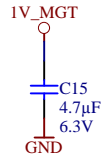
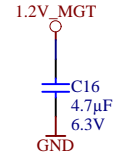
MGT\_CLK6\_P N8  
 MGT\_CLK6\_N N7  
 MGT\_CLK7\_P R8  
 MGT\_CLK7\_N R7  
 MGTREFCLK0P\_112  
 MGTREFCLK0N\_112  
 MGTREFCLK1P\_112  
 MGTREFCLK1N\_112

MGTAVTTRCAL\_112  
 MGTRREF\_112

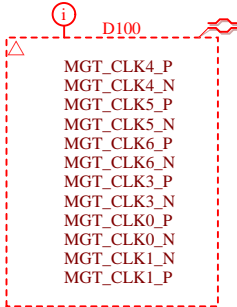
AB10  
 AB9

ClassName: MGT\_RX  
 D100  
 MGT\_RX0\_P AH10  
 MGT\_RX0\_N AH9  
 MGT\_RX1\_P AJ8  
 MGT\_RX1\_N AJ7  
 MGT\_RX2\_P AG8  
 MGT\_RX2\_N AG7  
 MGT\_RX3\_P AE8  
 MGT\_RX3\_N AE7  
 MGT\_RX4\_P AH6  
 MGT\_RX4\_N AH5  
 MGT\_RX5\_P AG4  
 MGT\_RX5\_N AG3  
 MGT\_RX6\_P AF6  
 MGT\_RX6\_N AF5  
 MGT\_RX7\_P AD6  
 MGT\_RX7\_N AD5  
 MGT\_RX8\_P AC4  
 MGT\_RX8\_N AC3  
 MGT\_RX9\_P AB6  
 MGT\_RX9\_N AB5  
 MGT\_RX10\_P Y6  
 MGT\_RX10\_N Y5  
 MGT\_RX11\_P AA4  
 MGT\_RX11\_N AA3  
 MGT\_RX12\_P V6  
 MGT\_RX12\_N V5  
 MGT\_RX13\_P U4  
 MGT\_RX13\_N U3  
 MGT\_RX14\_P T6  
 MGT\_RX14\_N T5  
 MGT\_RX15\_P P6  
 MGT\_RX15\_N P5

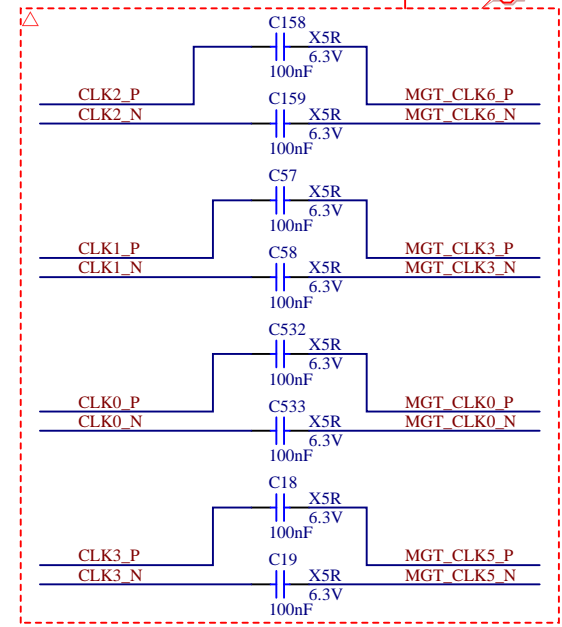
XC7Z100-2FFG9001



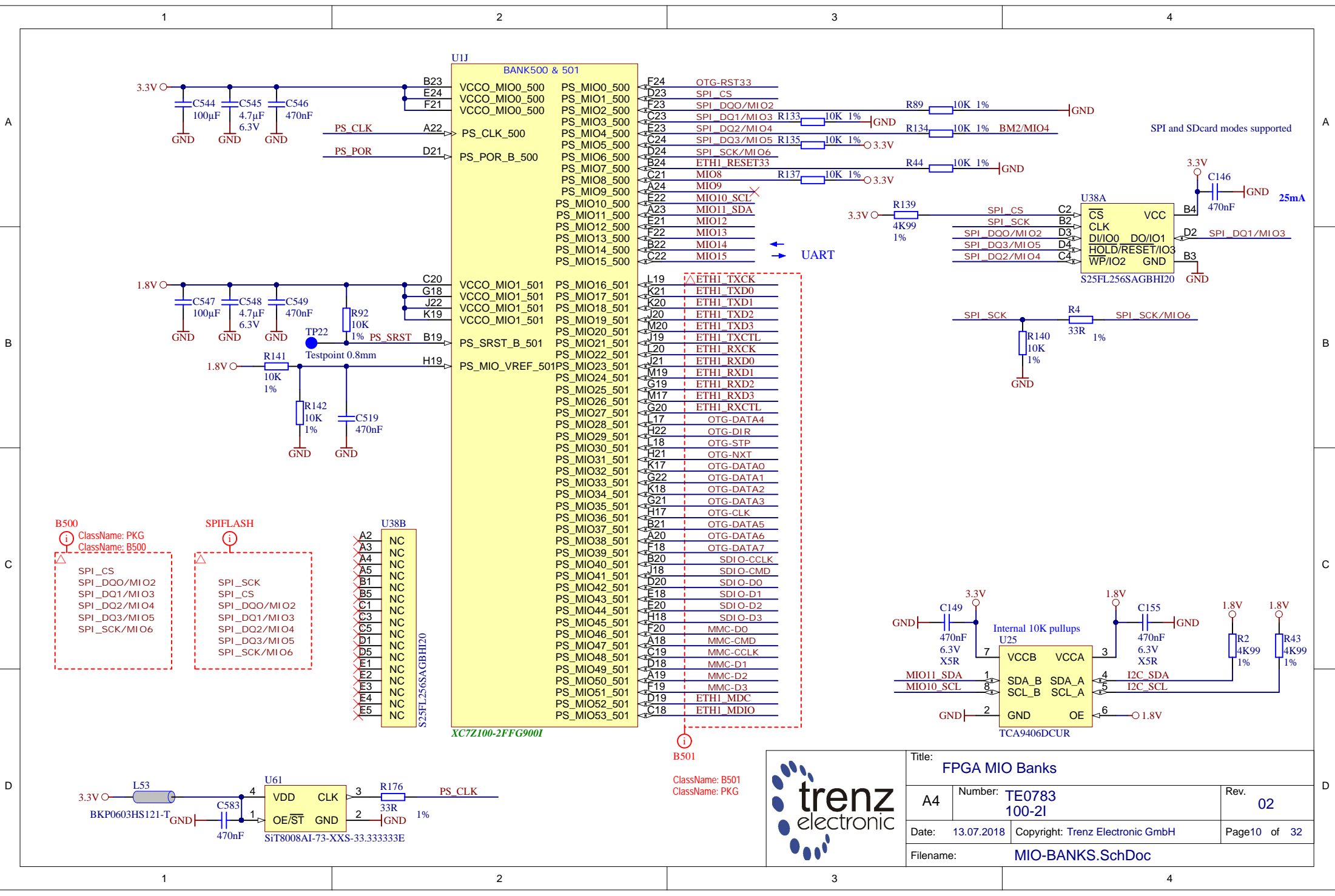
MGT\_CLK



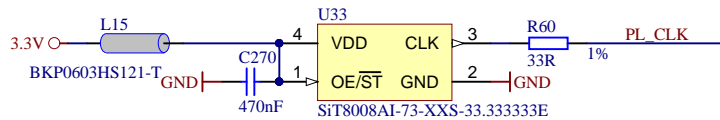
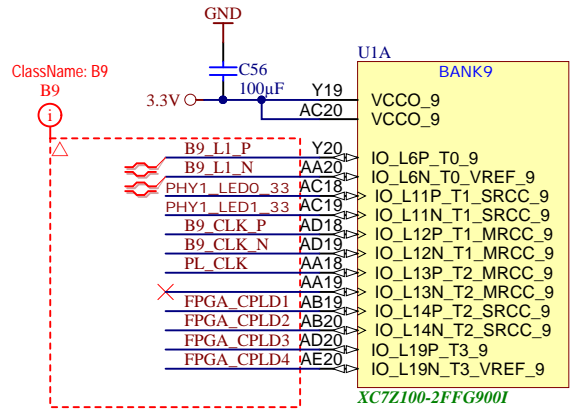
D100



Title: <b>FPGA MGT</b>		
A4	Number: <b>TE0783 100-21</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>9</b> of <b>32</b>
Filename: <b>FPGA-MGT.SchDoc</b>		

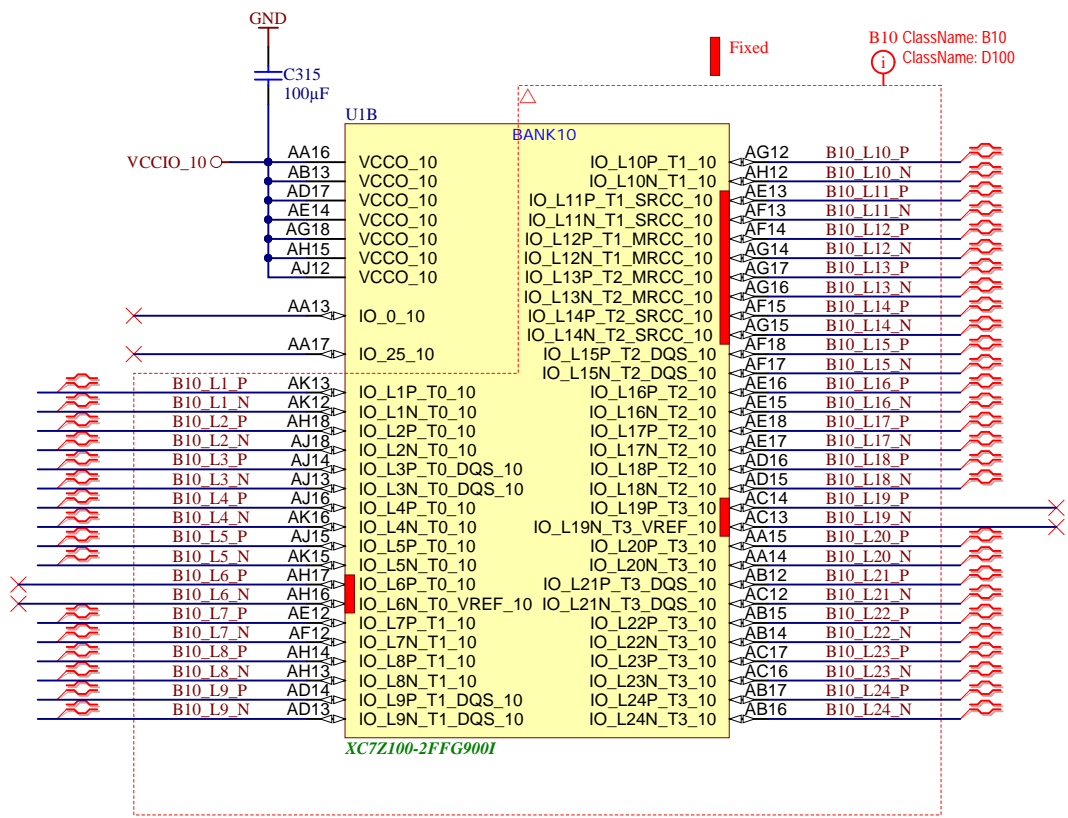


Title: <b>FPGA MIO Banks</b>		
A4	Number: <b>TE0783 100-21</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>10</b> of <b>32</b>
Filename: <b>MIO-BANKS.SchDoc</b>		



Title: <b>FPGA B9</b>		
A4	Number: <b>TE0783 100-2I</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>11</b> of <b>32</b>
Filename: <b>B9.SchDoc</b>		

TP4  
 ● VCCIO\_10  
 ○ Testpoint 0.8mm



Title: <b>FPGA B10</b>		
A4	Number: <b>TE0783 100-2I</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>12</b> of <b>32</b>
Filename: <b>B10.SchDoc</b>		

A

A

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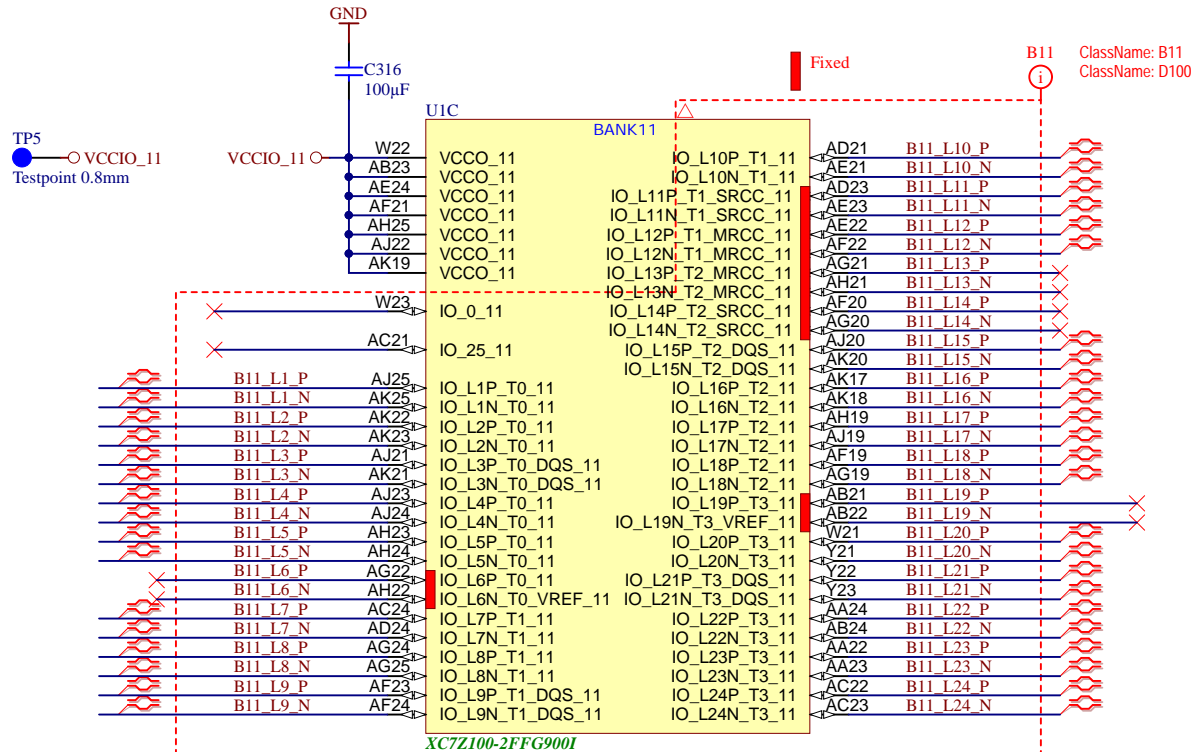
B


C


C

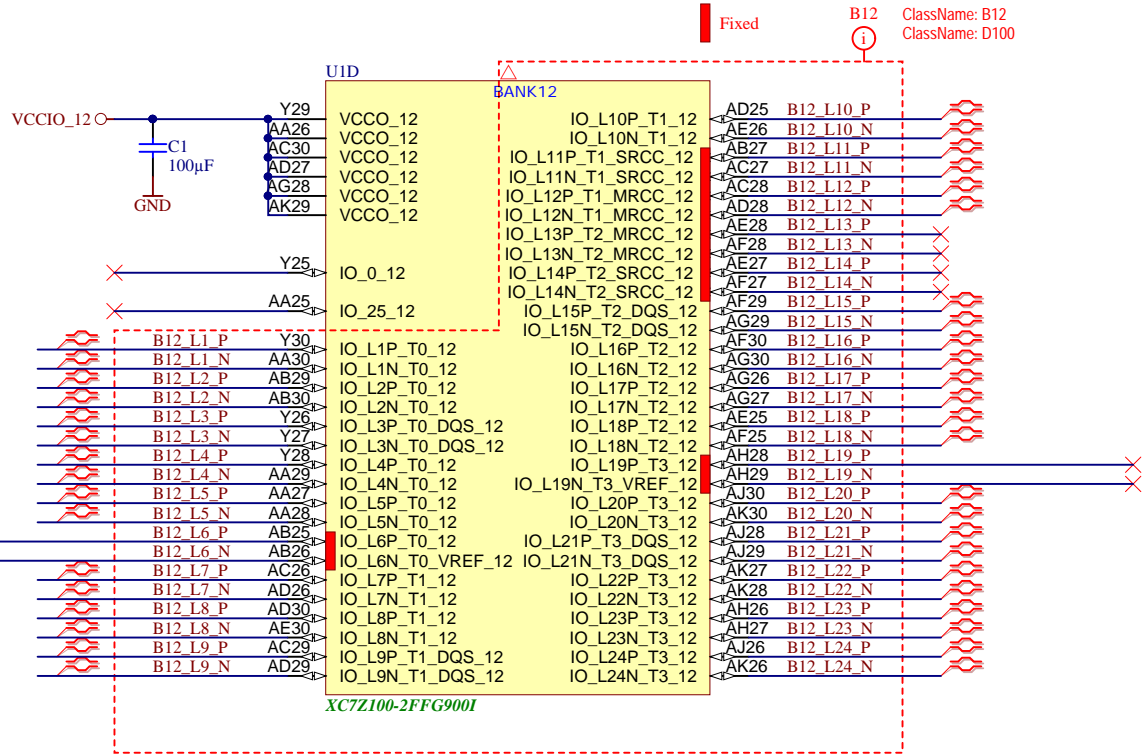
D

D

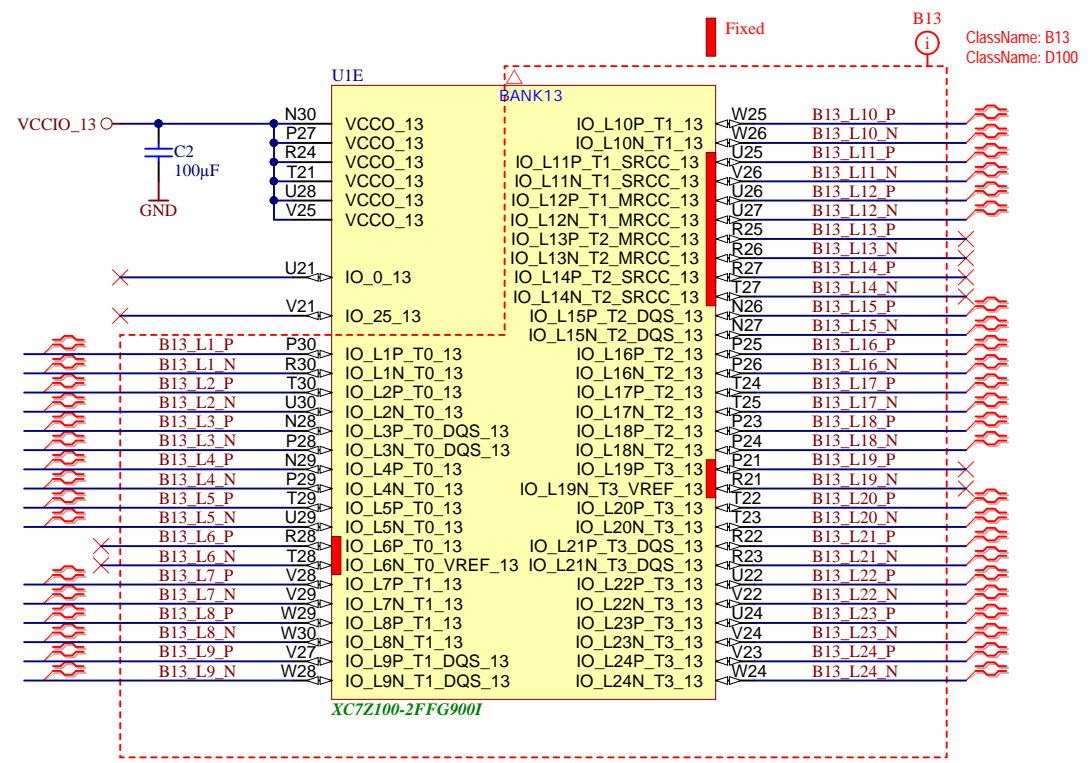
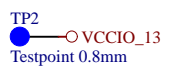


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			A4	Number: <b>TE0783 100-2I</b>
Date: <b>13.07.2018</b>		Copyright: <b>Trenz Electronic GmbH</b>		Page <b>13</b> of <b>32</b>
Filename: <b>B11.SchDoc</b>				

TP1  
 VCCIO\_12  
 Testpoint 0.8mm



Title: FPGA B12		
A4	Number: TE0783 100-21	Rev. 02
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Filename: B12.SchDoc		



	Title: <b>FPGA B13</b>		
	A4	Number: <b>TE0783 100-2I</b>	Rev. <b>02</b>
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	Filename: <b>B13.SchDoc</b>		

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U\_B33  
B33.SchDoc



U\_B34  
B34.SchDoc



U\_B35  
B35.SchDoc



U\_DDR3-RAM-PL1  
DDR3-RAM-PL1.SchDoc



U\_DDR3-RAM-PL2  
DDR3-RAM-PL2.SchDoc



A

A

B

B

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C

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Title: <b>FPGA HP Banks</b>		
A4	Number: <b>TE0783 100-2I</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>16</b> of <b>32</b>
Filename: <b>HP-BANKS.SchDoc</b>		

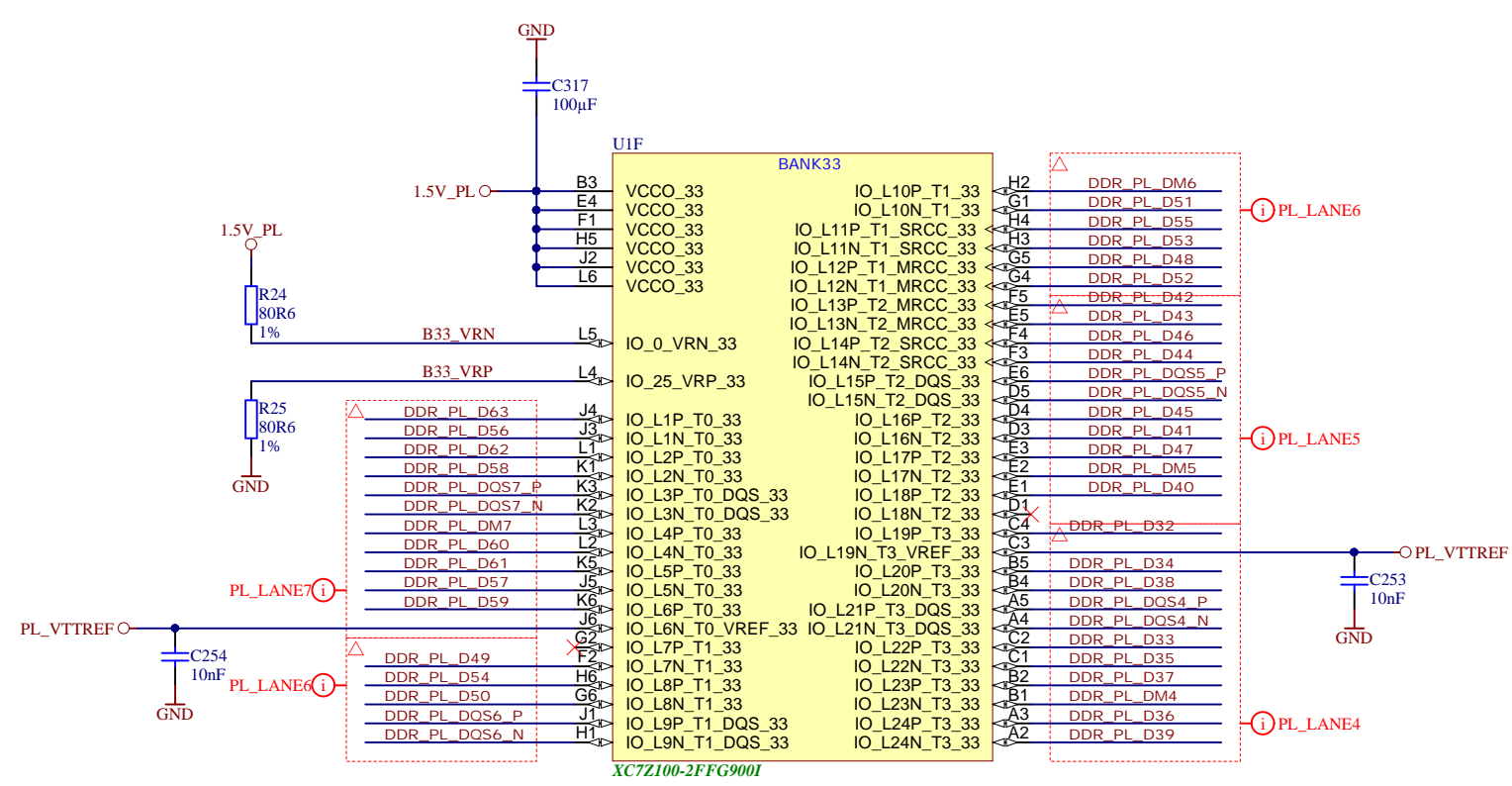

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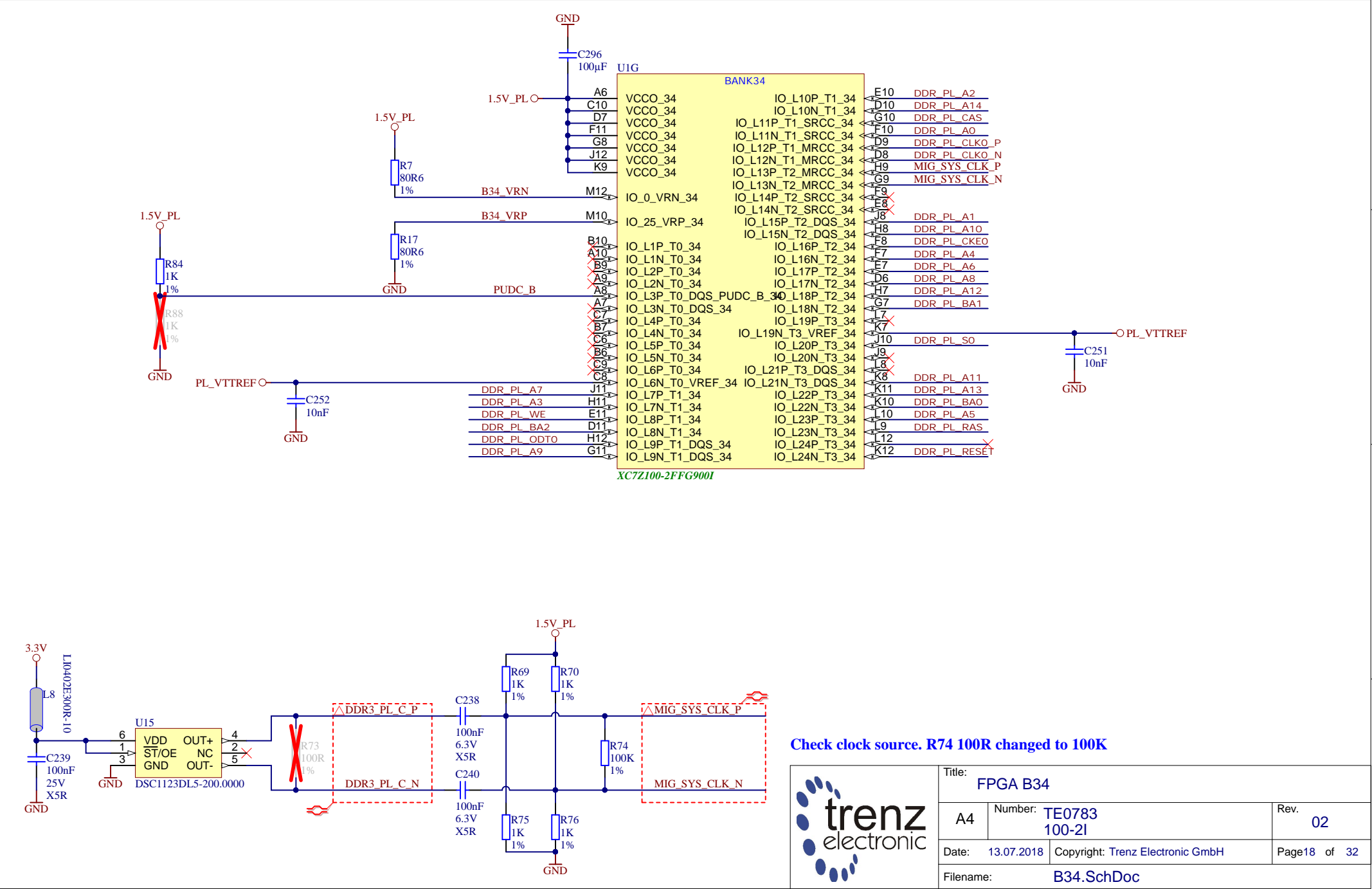
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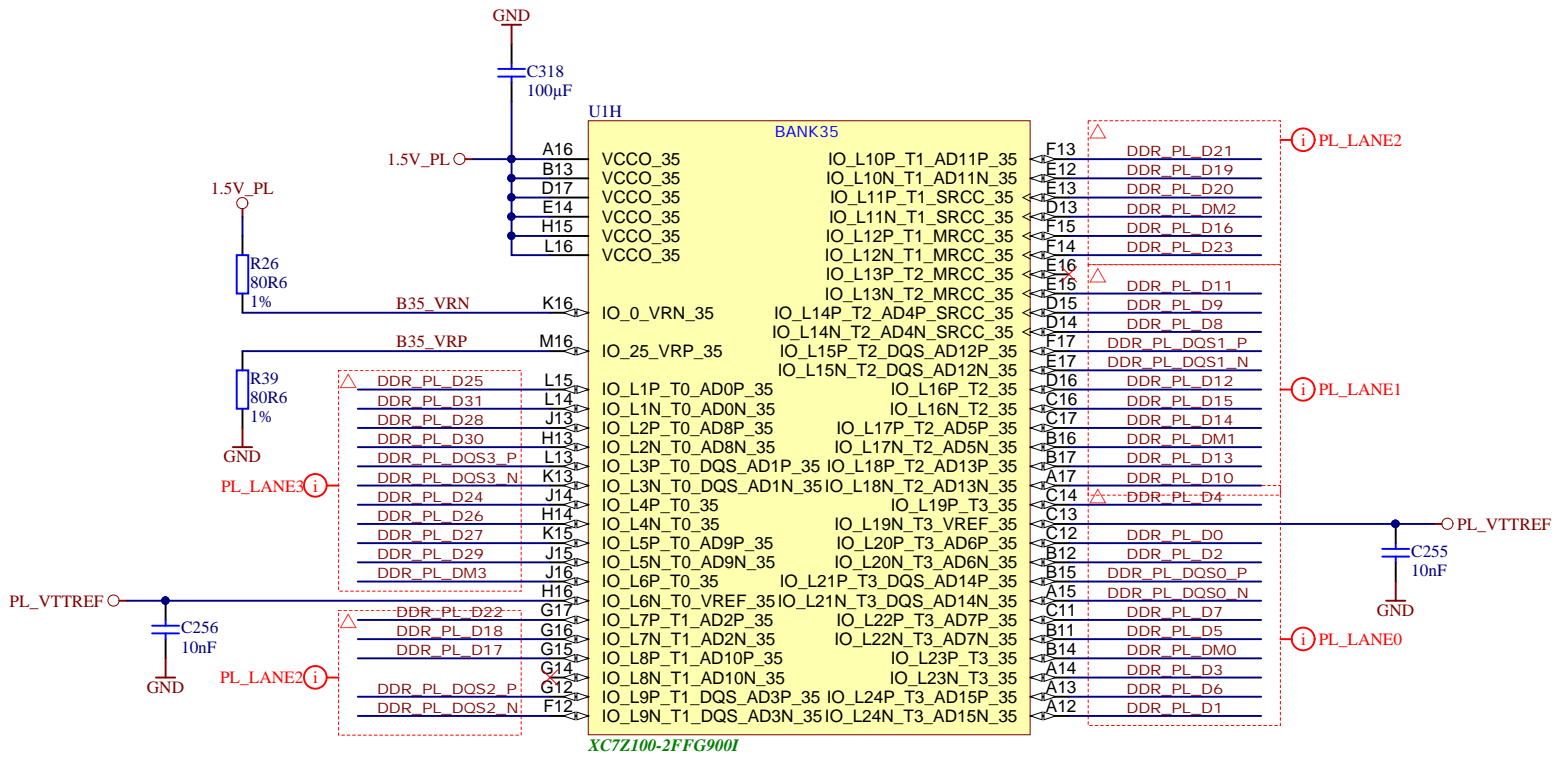



Title: <b>FPGA B33</b>		
A4	Number: <b>TE0783 100-2I</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>17</b> of <b>32</b>
Filename: <b>B33.SchDoc</b>		




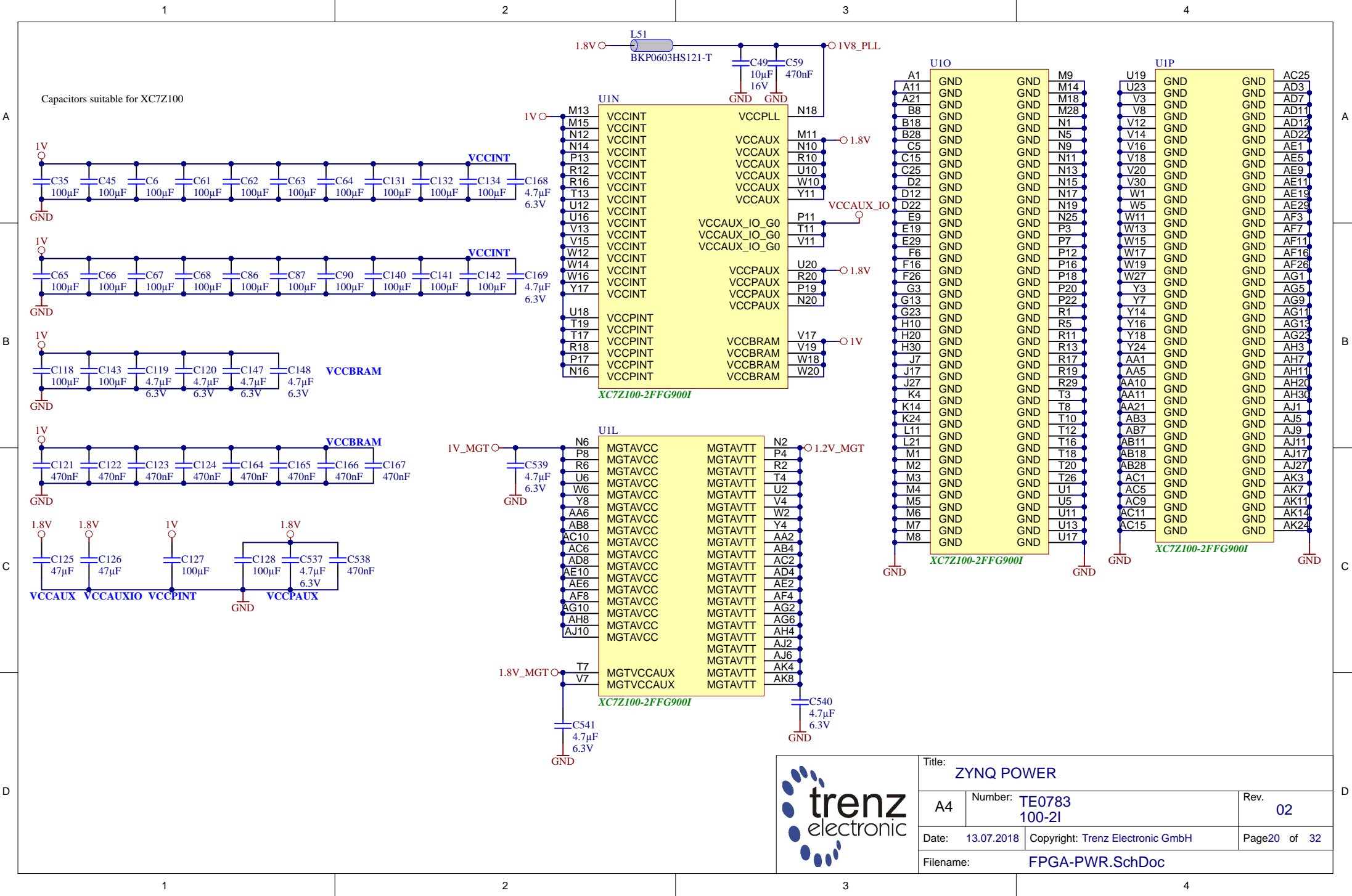
Check clock source. R74 100R changed to 100K

			Title: <b>FPGA B34</b>	
			A4	Number: <b>TE0783 100-2I</b>
Date: <b>13.07.2018</b>		Copyright: <b>Trenz Electronic GmbH</b>		Page <b>18</b> of <b>32</b>
Filename: <b>B34.SchDoc</b>				



XC7Z100-2FFG9001

	Title: <b>FPGA B35</b>		
	A4	Number: <b>TE0783 100-2I</b>	Rev. <b>02</b>
	Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>19</b> of <b>32</b>
	Filename: <b>B35.SchDoc</b>		



Title: ZYNQ POWER		
A4	Number: TE0783 100-21	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page20 of 32
Filename: FPGA-PWR.SchDoc		

A

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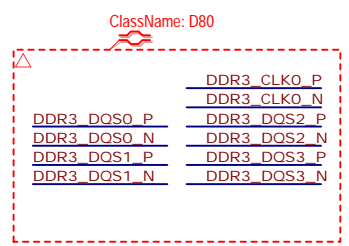
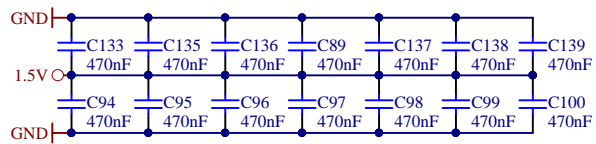
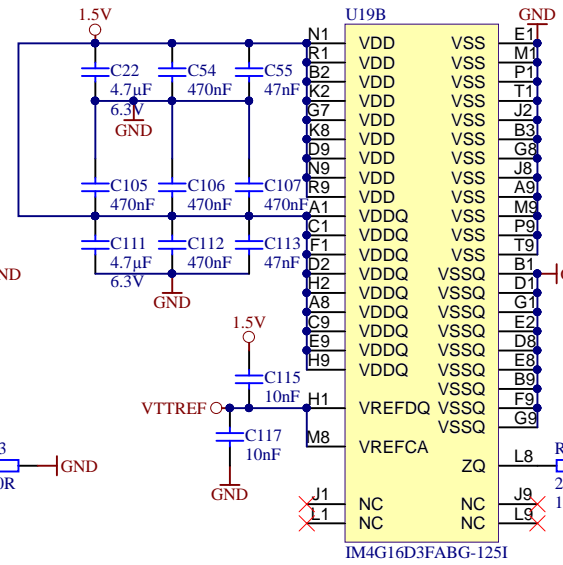
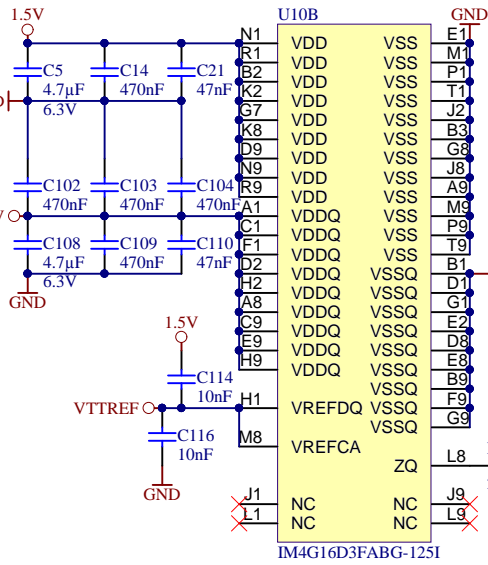
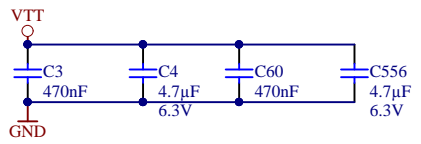
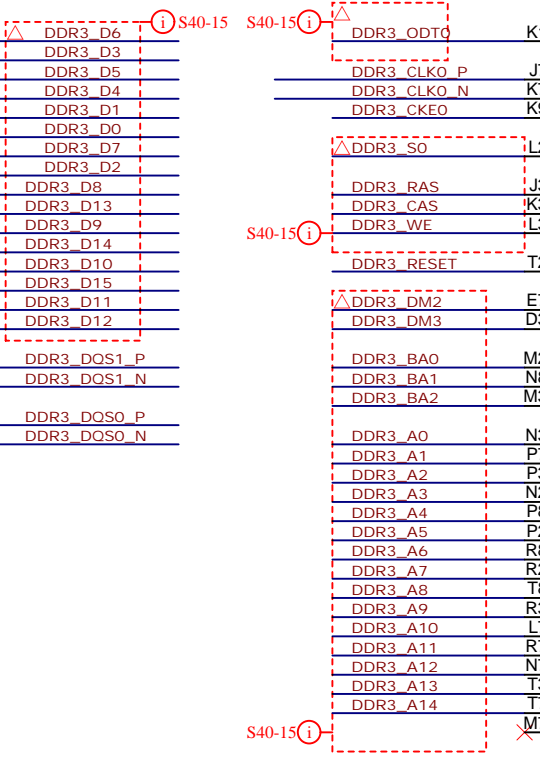
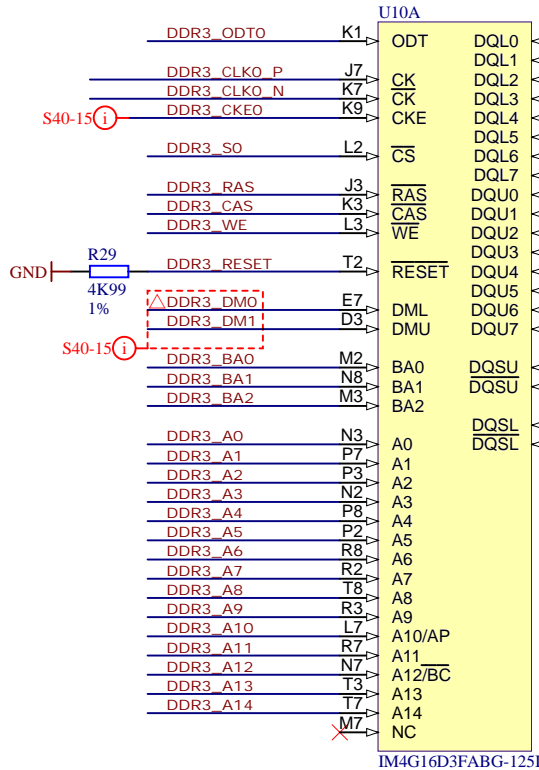
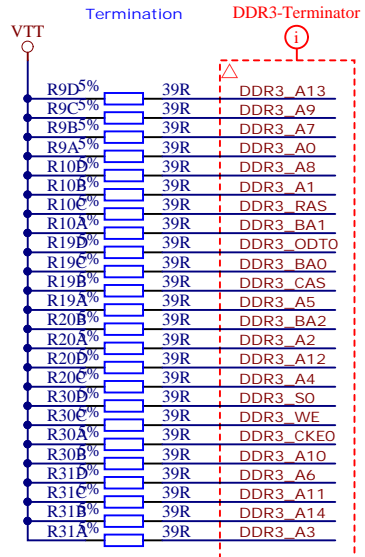
D

A

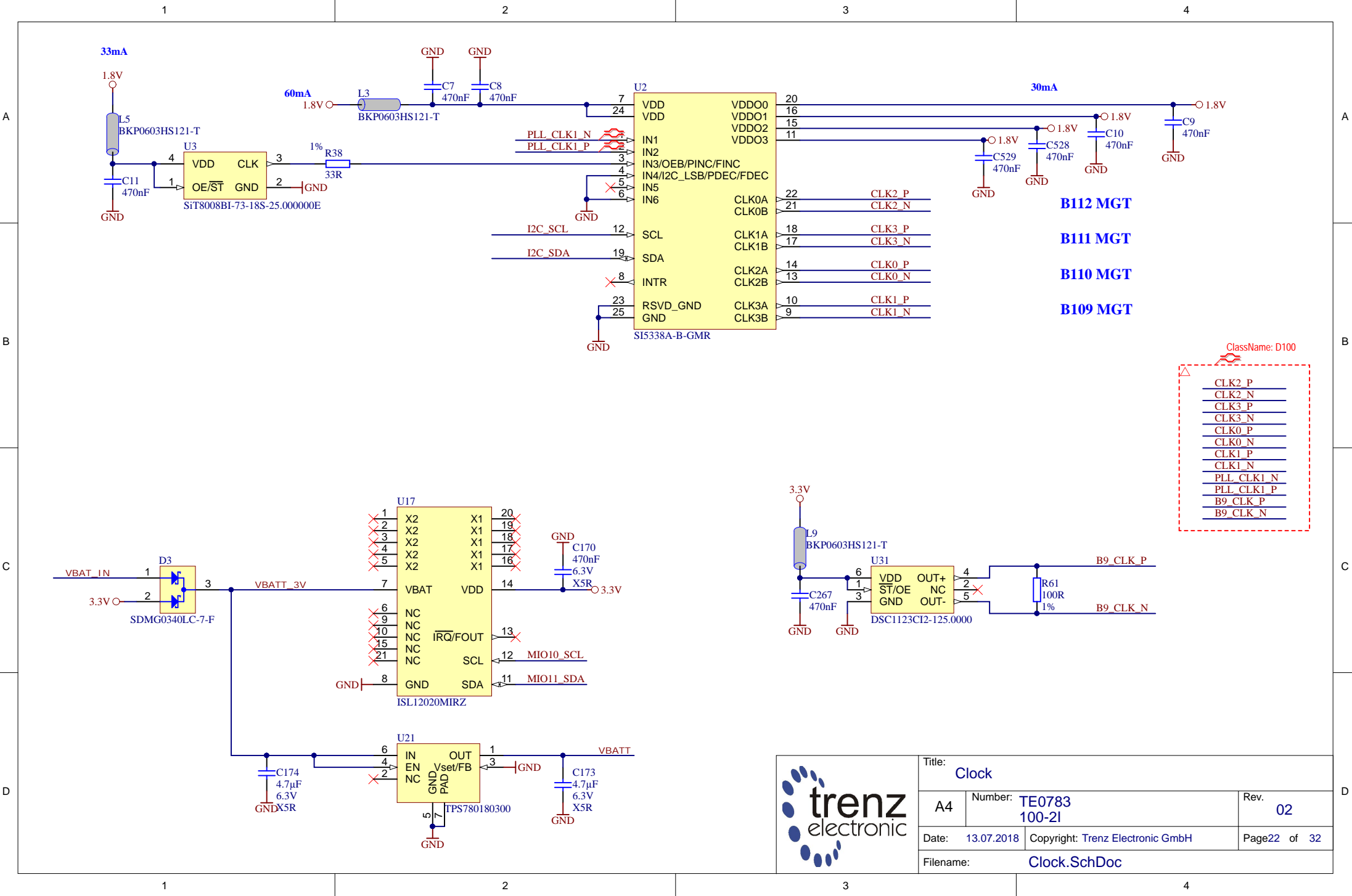
B

C

D



Title: <b>DDR3 RAM PS</b>		
A4	Number: <b>TE0783 100-21</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>21</b> of <b>32</b>
Filename: <b>DDR3-RAM.SchDoc</b>		



Title: Clock		
A4	Number: TE0783 100-21	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page22 of 32
Filename: Clock.SchDoc		

A

A

B

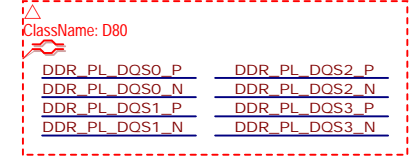
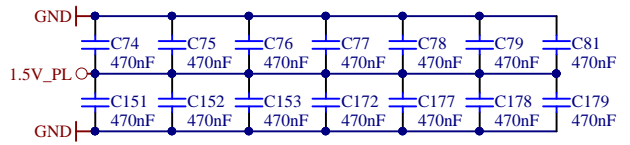
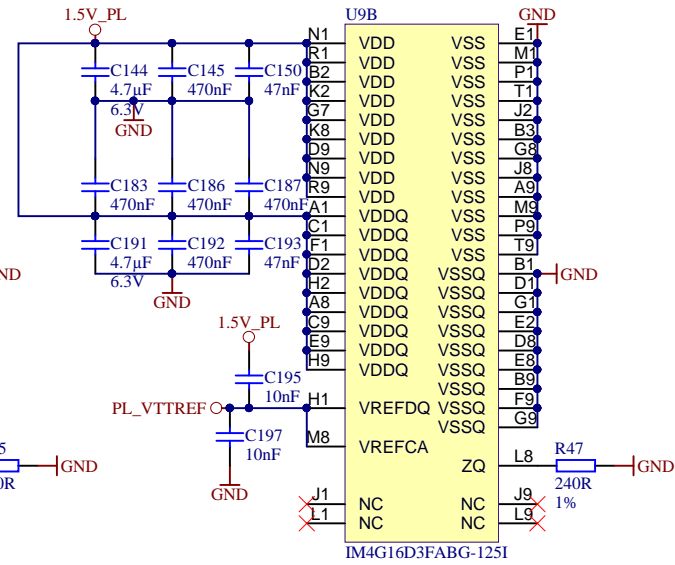
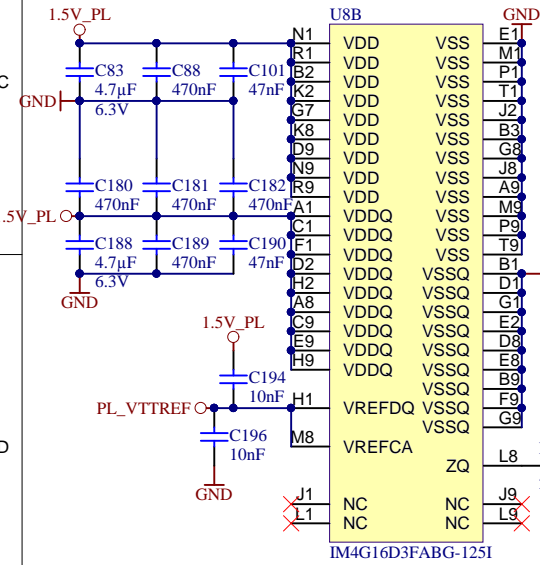
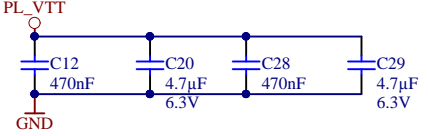
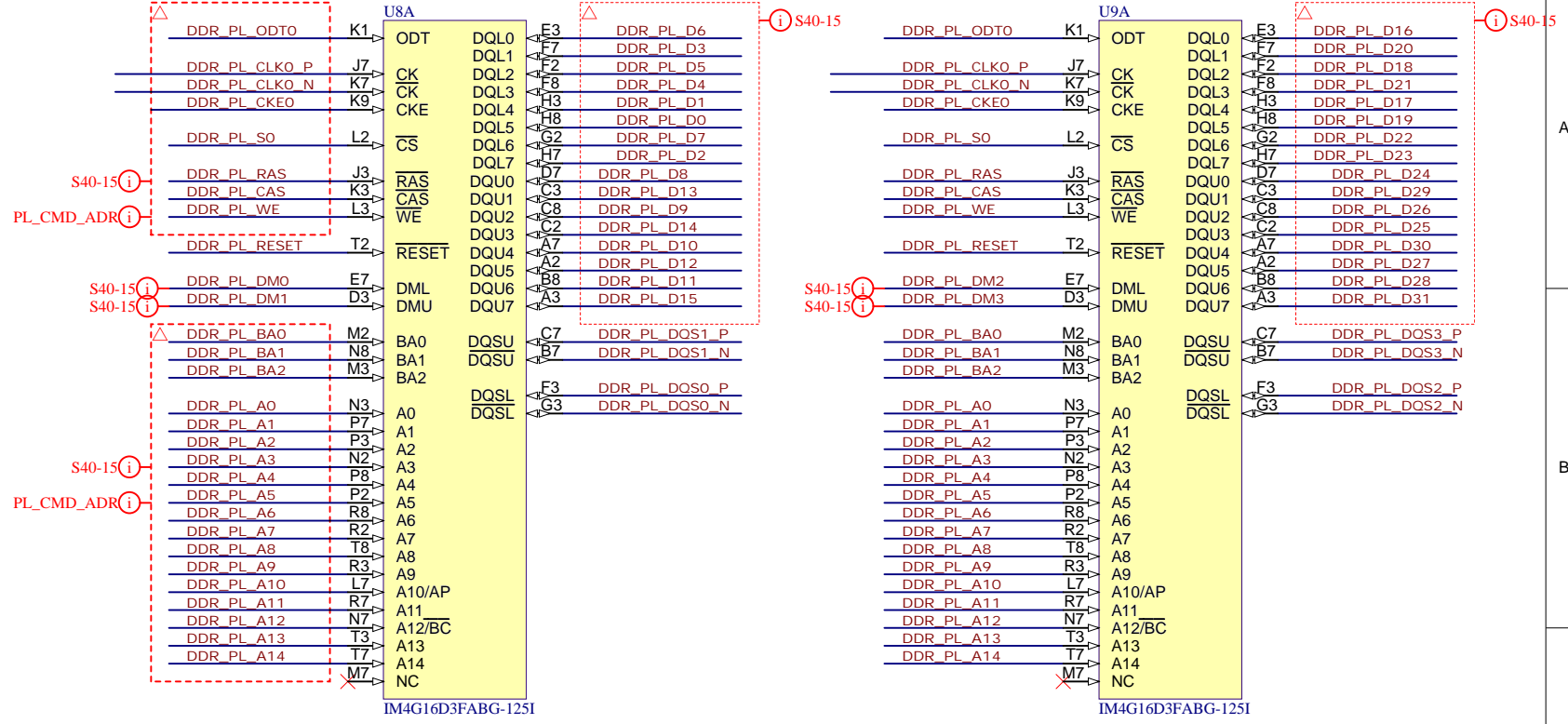
B

C

C

D

D



Title: <b>DDR3 RAM PL</b>		
A4	Number: <b>TE0783 100-21</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>23</b> of <b>32</b>
Filename: <b>DDR3-RAM-PL1.SchDoc</b>		

A

B

C

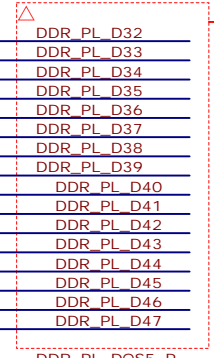
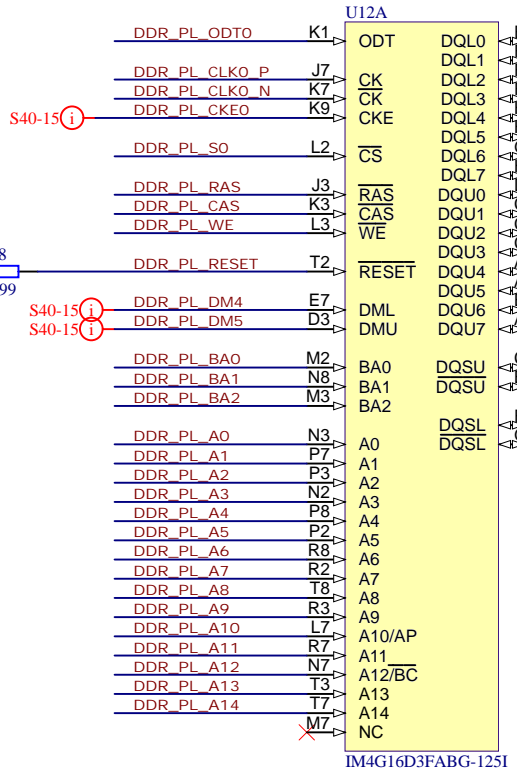
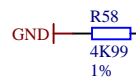
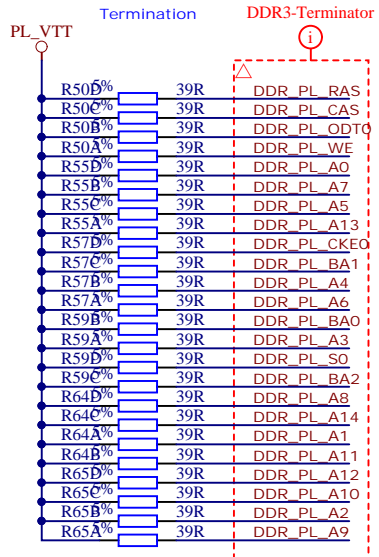
D

A

B

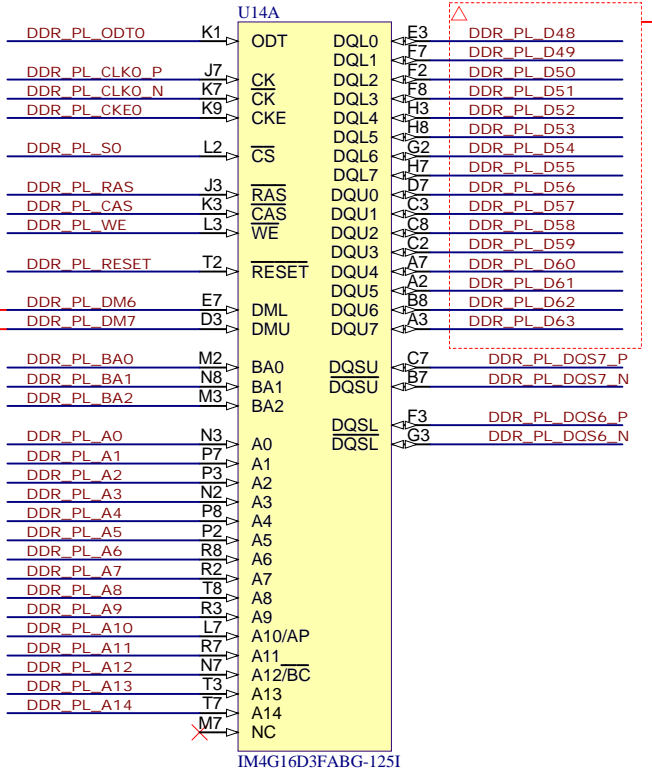
C

D



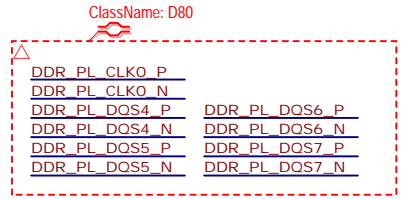
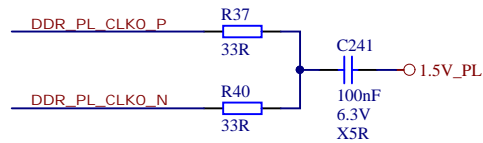
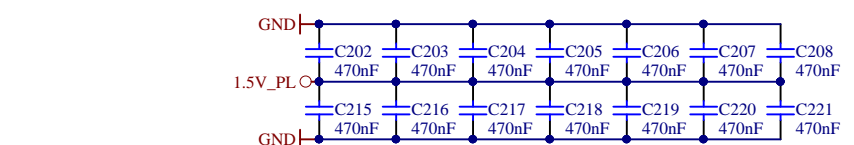
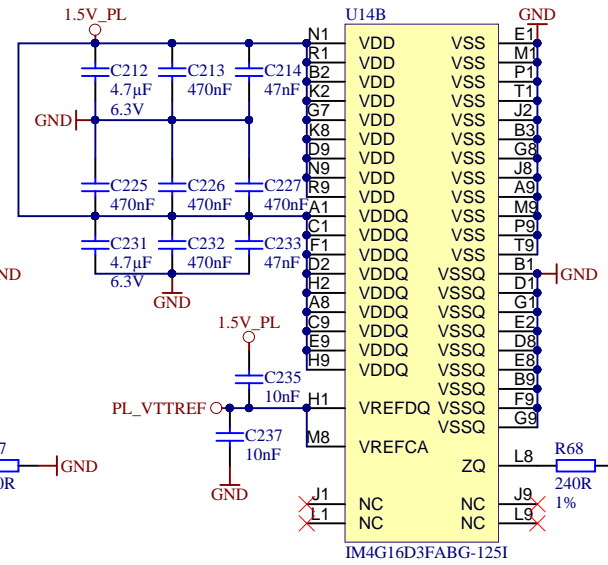
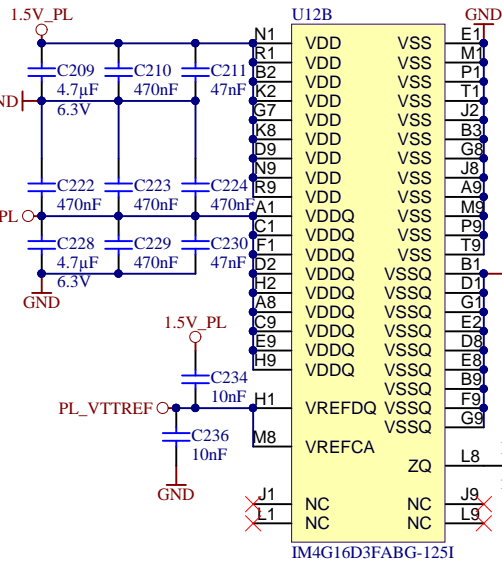
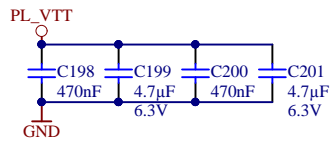
S40-15

S40-15



S40-15

S40-15



Place directly at the clock pins



Title: <b>DDR3 RAM PL</b>		
A4	Number: <b>TE0783 100-21</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>24</b> of <b>32</b>
Filename: <b>DDR3-RAM-PL2.SchDoc</b>		



A

B

C

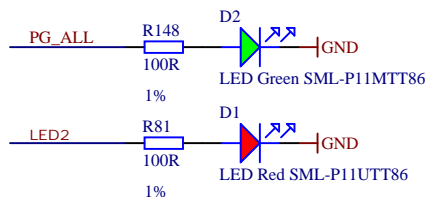
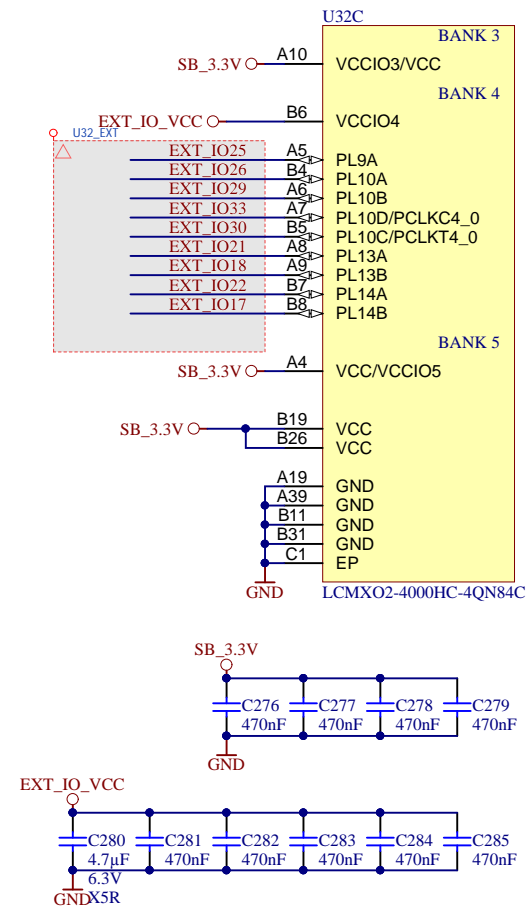
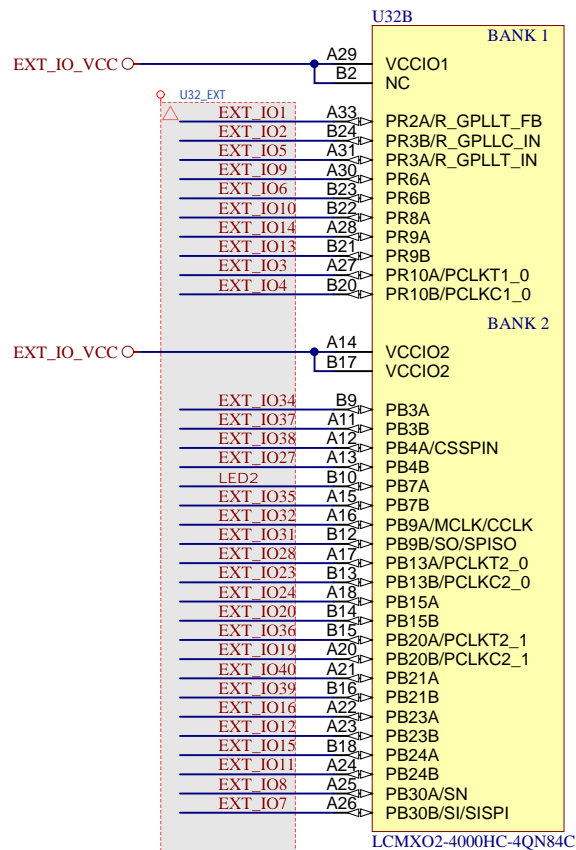
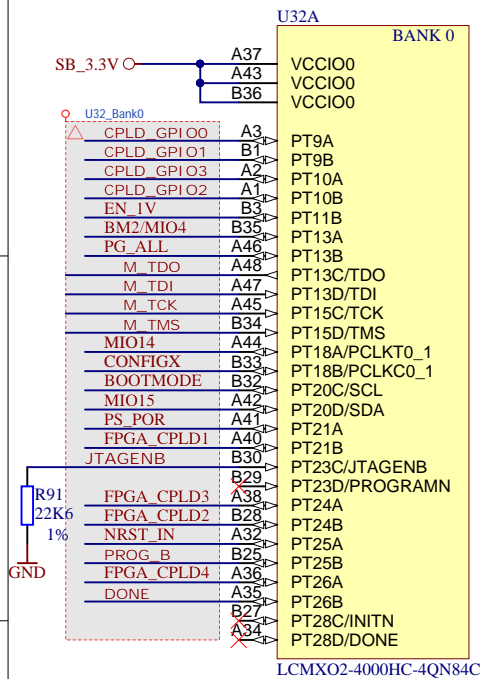
D

A

B

C

D



Title: CPLD		
A4	Number: TE0783 100-21	Rev. 02
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Filename: CPLD.SchDoc		

A

B

C

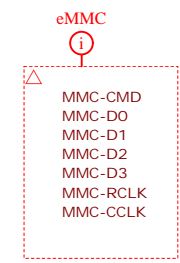
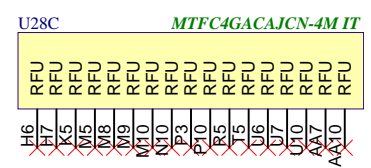
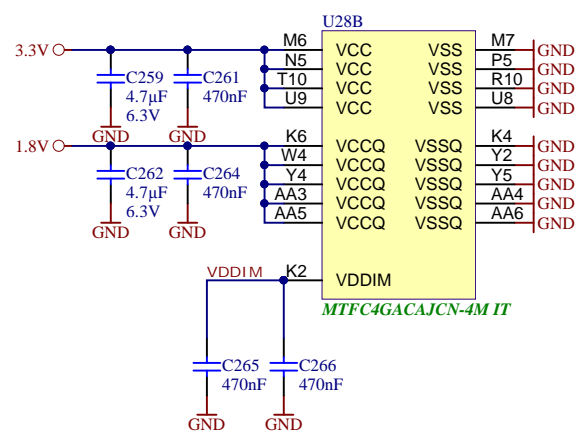
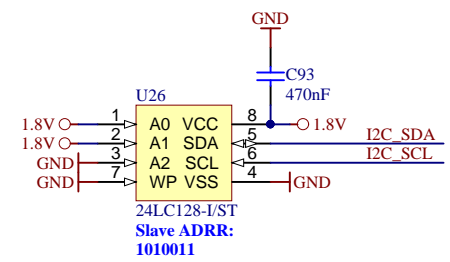
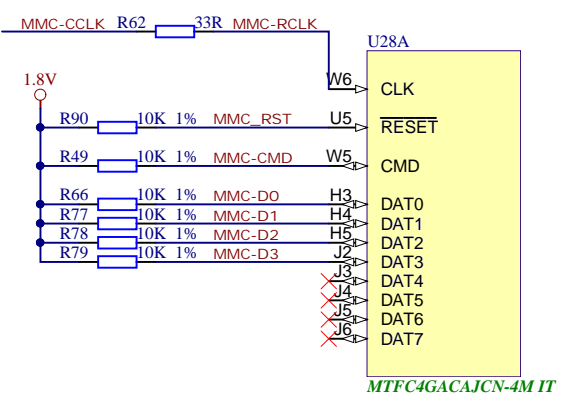
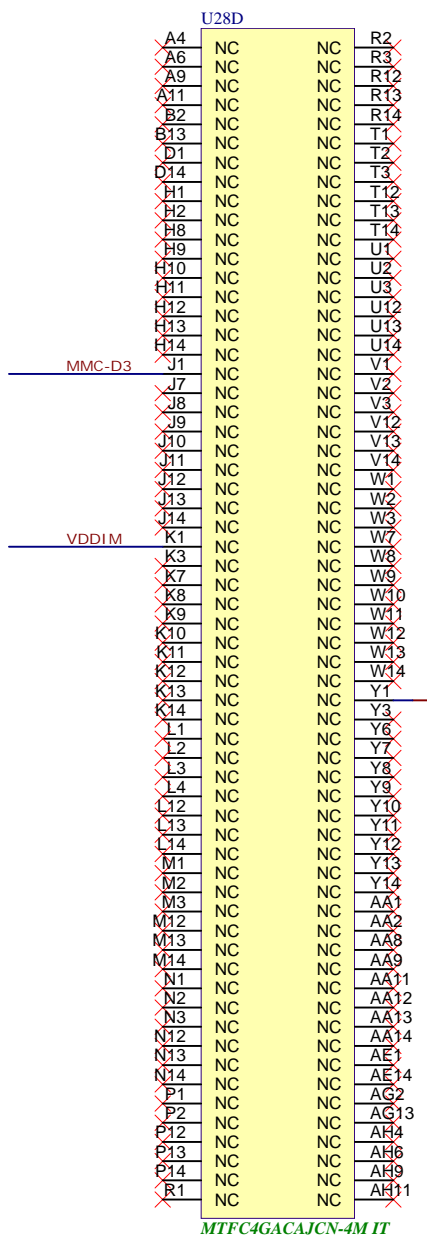
D

A

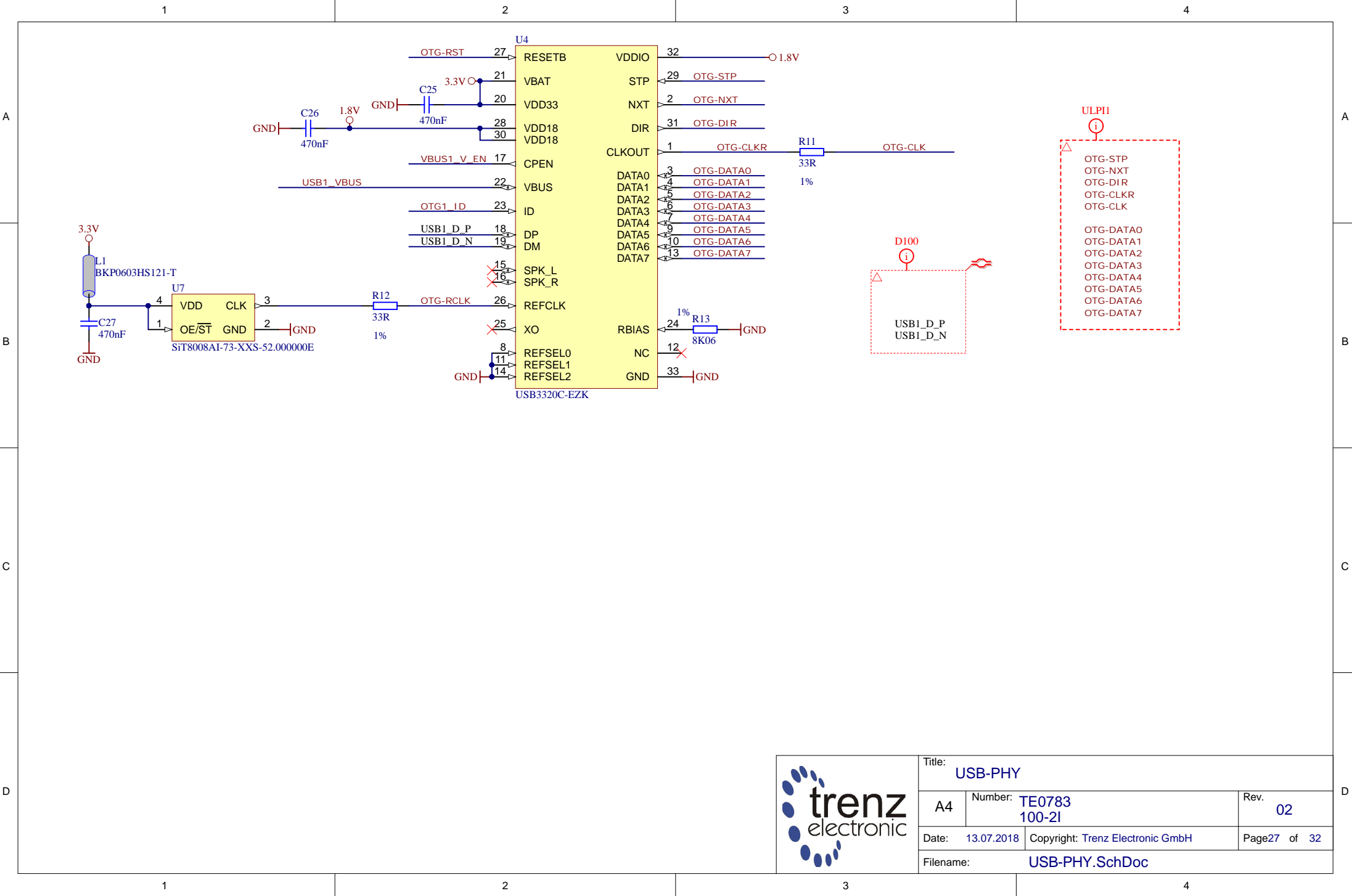
B


C

D

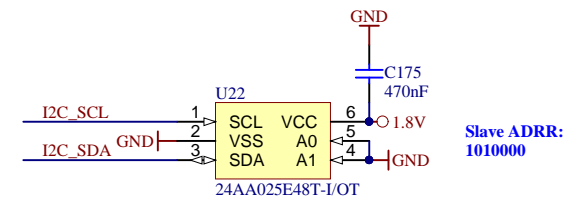
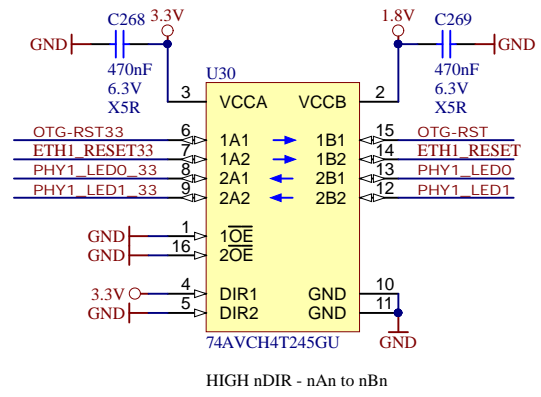
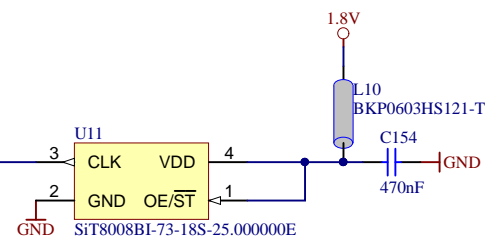
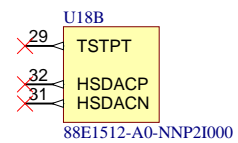
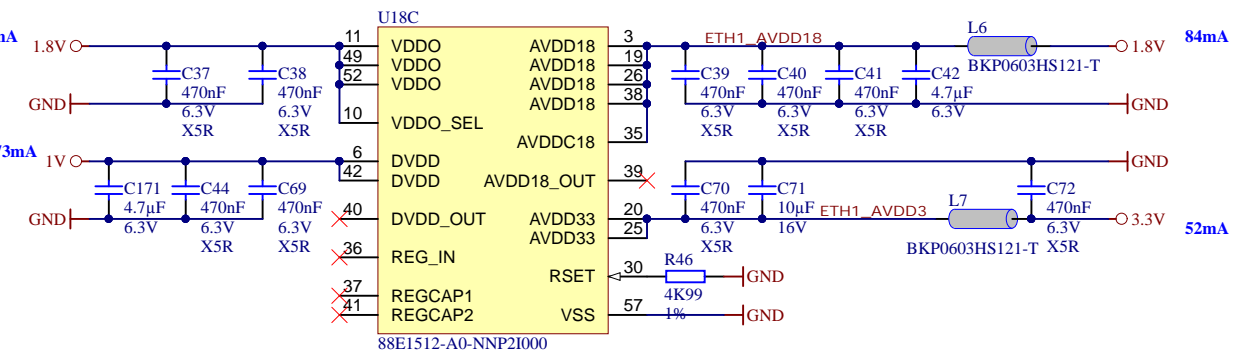
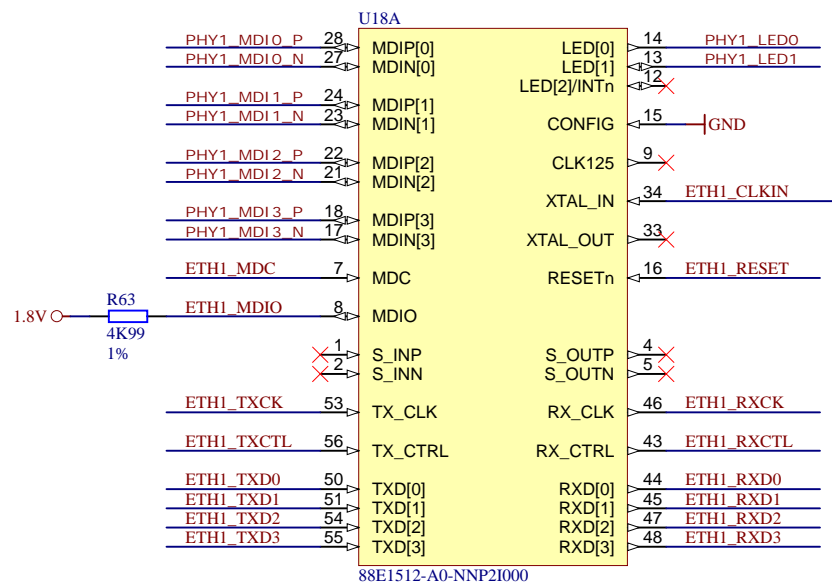


Title: eMMC		
A4	Number: TE0783 100-21	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 26 of 32
Filename: eMMC.SchDoc		

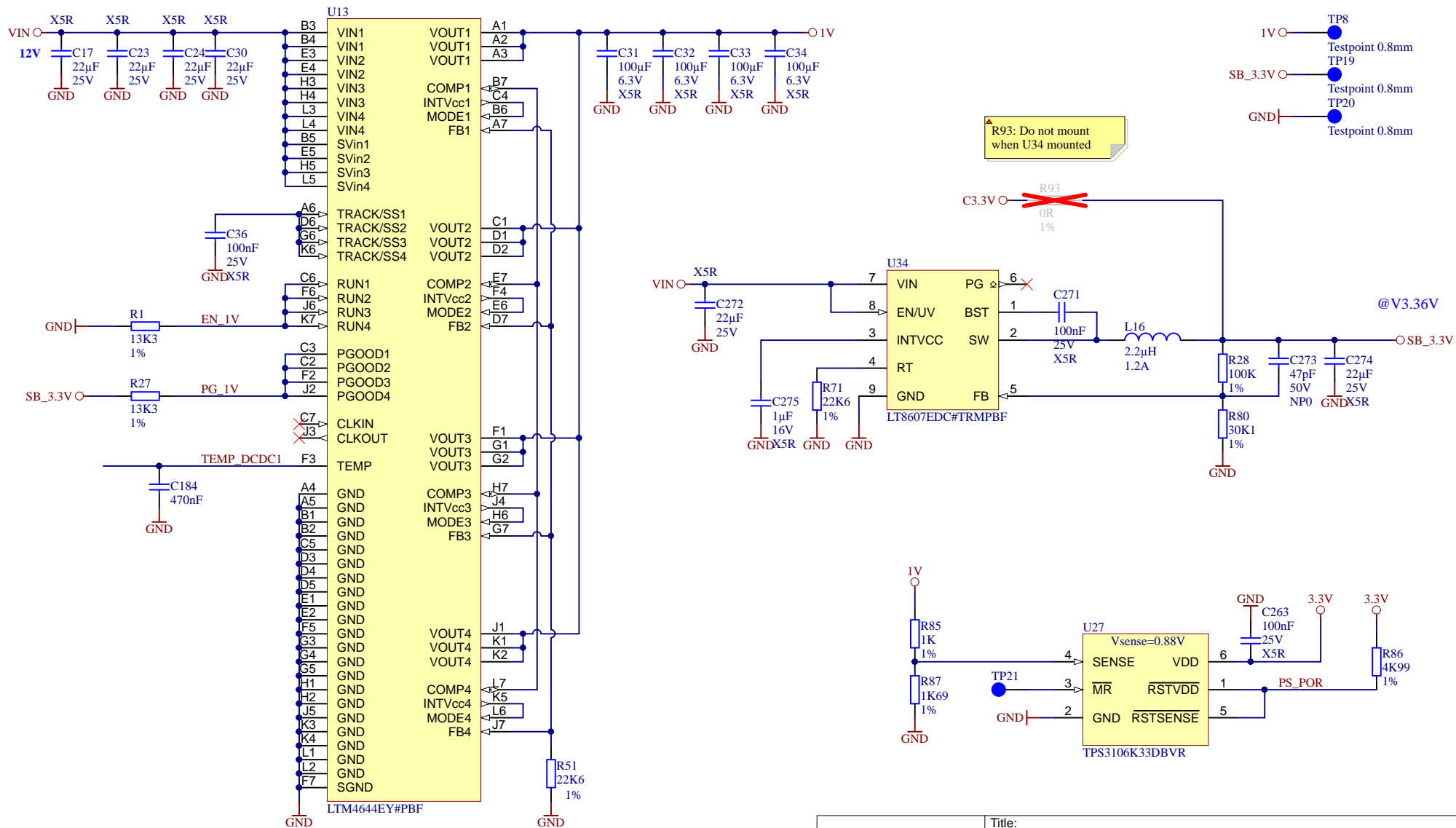



		Title: <b>USB-PHY</b>	
		A4	Number: <b>TE0783 100-2I</b>
Date: <b>13.07.2018</b>		Copyright: <b>Trenz Electronic GmbH</b>	
Filename: <b>USB-PHY.SchDoc</b>		Page <b>27</b> of <b>32</b>	

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Title: ETH_PHY1		
A4	Number: TE0783 100-21	Rev. 02
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Filename: ETH1.SchDoc		



			Title: <b>POWER</b>	
			A4	Number: <b>TE0783 100-21</b>
Date: <b>13.07.2018</b>		Copyright: <b>Trenz Electronic GmbH</b>		Page <b>29</b> of <b>32</b>
Filename: <b>POWER.SchDoc</b>				

1

2

3

4

A

A

B

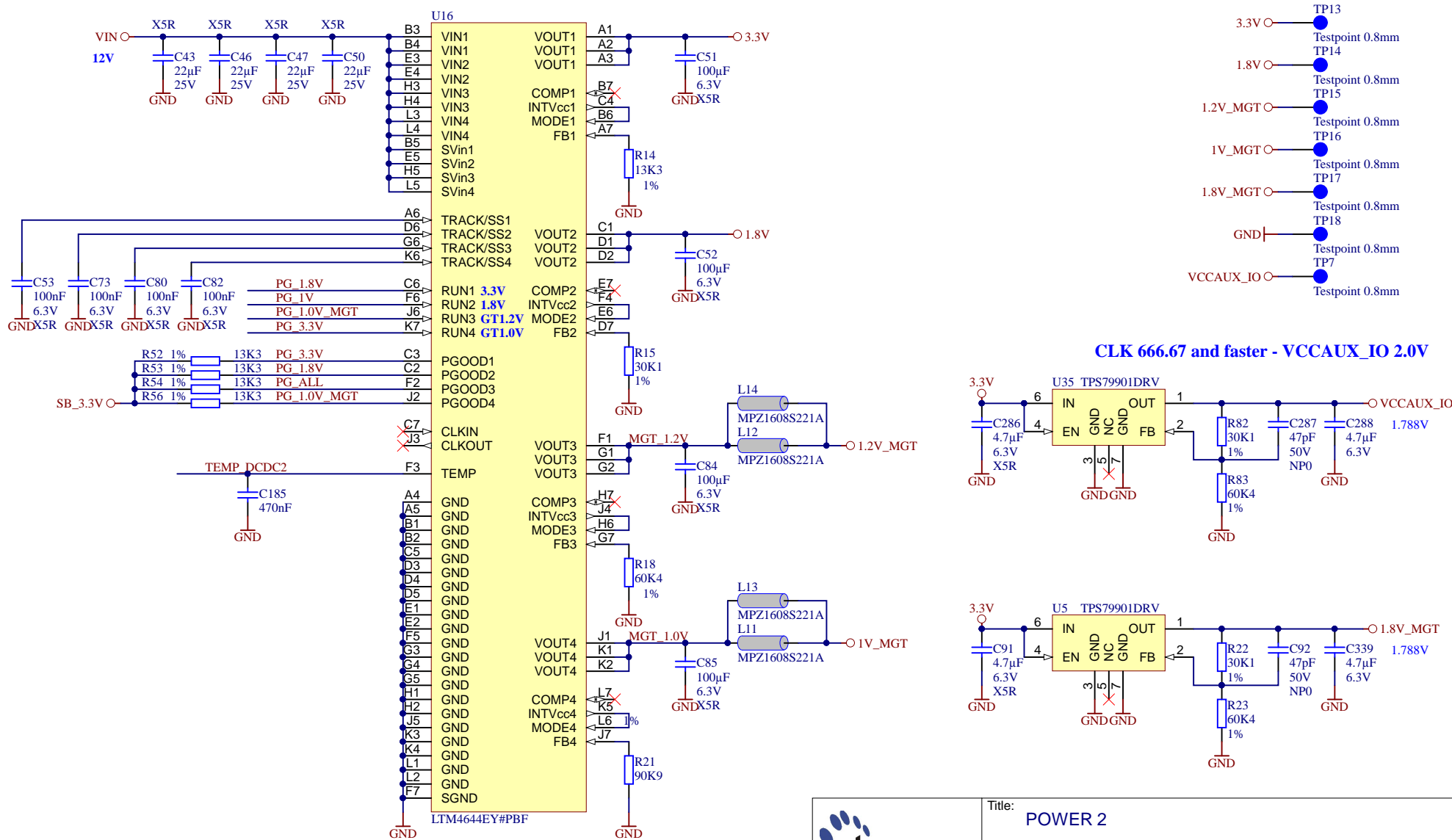
B

C


C

D

D



CLK 666.67 and faster - VCCAUX\_IO 2.0V

			Title: <b>POWER 2</b>	
			A4	Number: <b>TE0783 100-21</b>
Date: 13.07.2018		Copyright: Trenz Electronic GmbH		Page 30 of 32
Filename: <b>POWER2.SchDoc</b>				

1

2

3

4

1

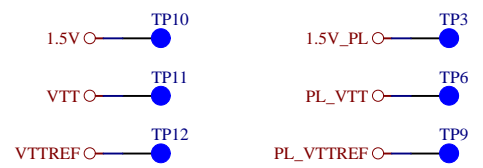
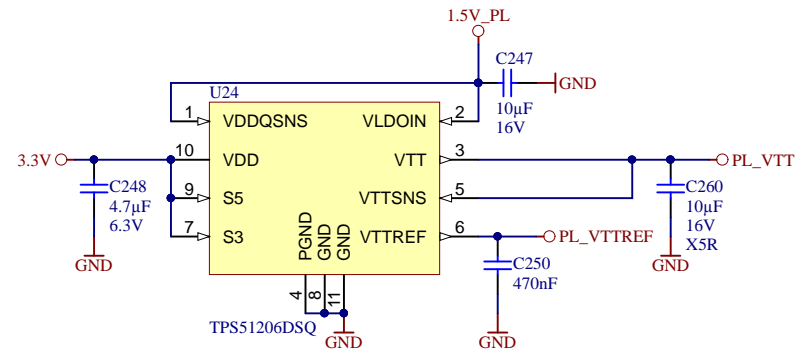
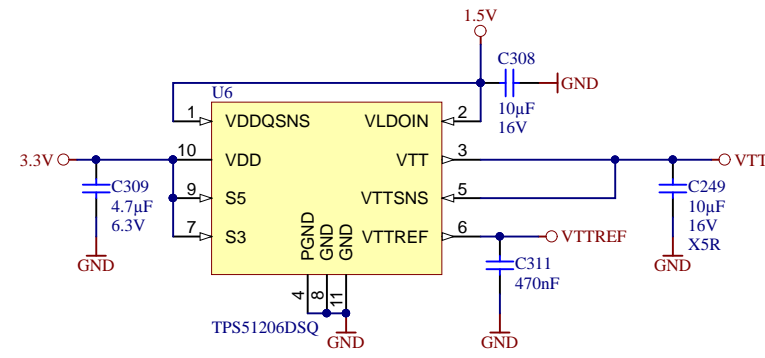
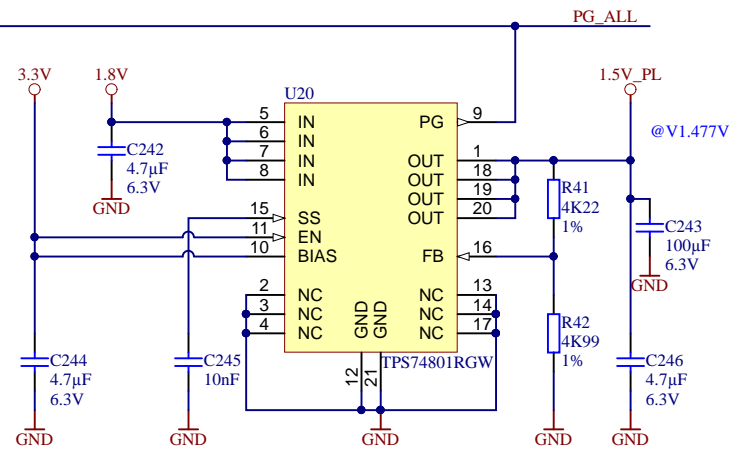
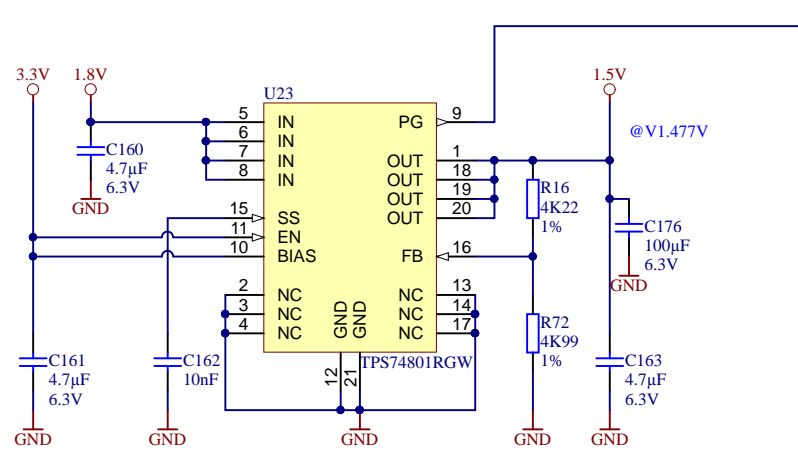
2

3

4

### DDR3 PS

### DDR3 PL



Title: <b>POWER 2</b>		
A4	Number: <b>TE0783 100-21</b>	Rev. <b>02</b>
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Filename: <b>POWER3.SchDoc</b>		

1

2

3

4

1

2

3

4

REV. 02:

1) Changed power-up sequence: 3.3V next to 1.8V. MGT power domain next to 3.3V

A

A

B


B

C

C

D

D

	Title: Revision Changes		
	A4	Number: TE0783 100-2I	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH / TT	Page 32 of 32
	Filename: Revision Changes.SchDoc		

1

2

3

4