

U_SOC
SOC.SchDoc

U_DDR3-RAM
DDR3-RAM.SchDoc

U_CPLD
CPLD.SchDoc

U_USB-PHY
USB-PHY.SchDoc

U_ETH1
ETH1.SchDoc

U_Clock
Clock.SchDoc

U_eMMC
eMMC.SchDoc

U_POWER2
POWER2.SchDoc

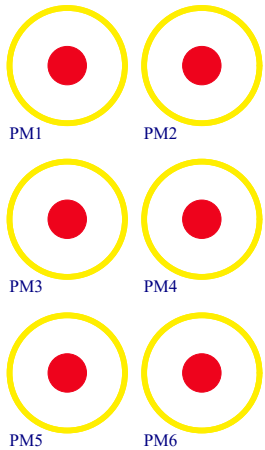
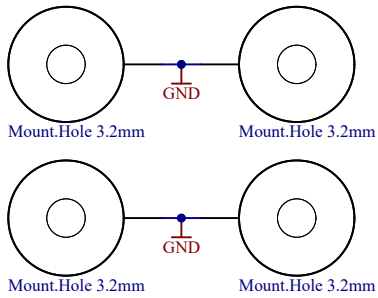
U_Connectors
Connectors.SchDoc

U_Rev_changes
Revision Changes.SchDoc

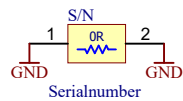
U_POWER
POWER.SchDoc

U_POWER3
POWER3.SchDoc

LOGO1
TE Logo PRINT Layer
LOGO PRINT



Serial
Serialnumber 6,3 x 6.3mm



Assembly variant	92133HA
Created by	RM
Modified by	RM
Modified at	2021-03-26
SVN Revision	



Title: Overview		
A4	Number: TE0783 92133HA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page1 of 32
Filename: TE0783.SchDoc		

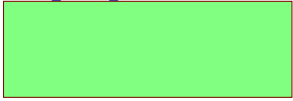
1

2

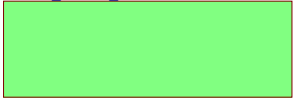
3

4

U_HSMC_CONN_J1
HSMC_CONN J1.SchDoc



U_HSMC_CONN_J2
HSMC_CONN J2.SchDoc



U_HSMC_CONN_J3
HSMC_CONN J3.SchDoc



A

A

B


B

C

C

D

D

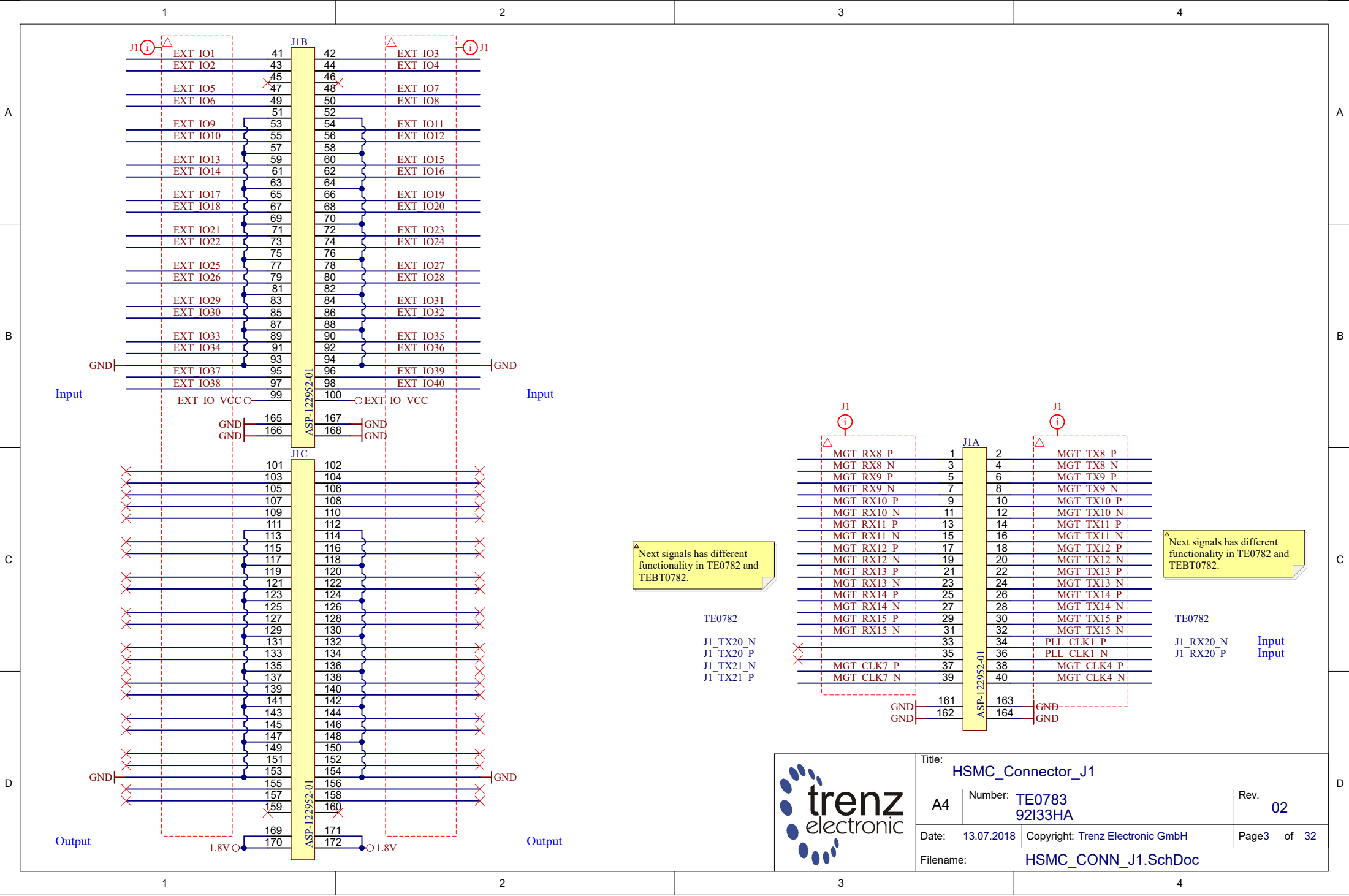
			Title: Connectors		
			A4	Number: TE0783 92I33HA	Rev. 02
Date: 13.07.2018		Copyright: Trenz Electronic GmbH		Page 2 of 32	
Filename: Connectors.SchDoc					

1

2

3

4



Next signals has different functionality in TE0782 and TEBT0782.

TE0782

- J1_TX20_N
- J1_TX20_P
- J1_TX21_N
- J1_TX21_P

Next signals has different functionality in TE0782 and TEBT0782.

TE0782

- J1_RX20_N
- J1_RX20_P

Input
Input



Title: HSMC_Connector_J1		
A4	Number: TE0783 92I33HA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page3 of 32
Filename: HSMC_CONN_J1.SchDoc		

1

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4

A

A

B

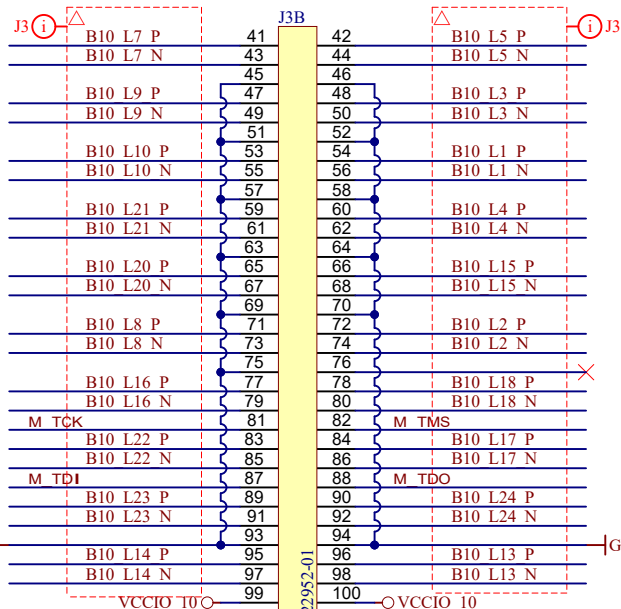
B

C

C

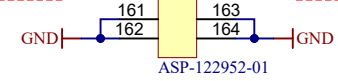
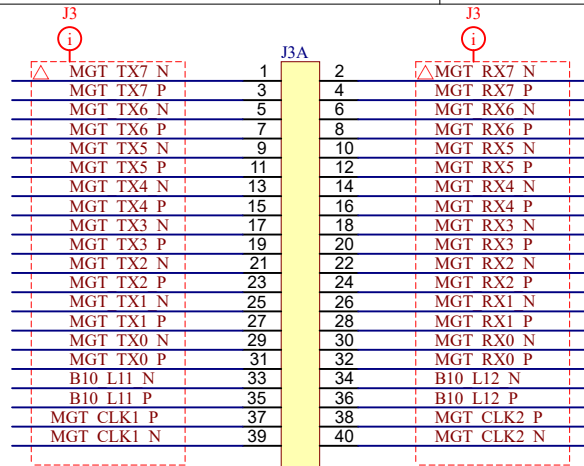
D

D



CPLD JTAG !

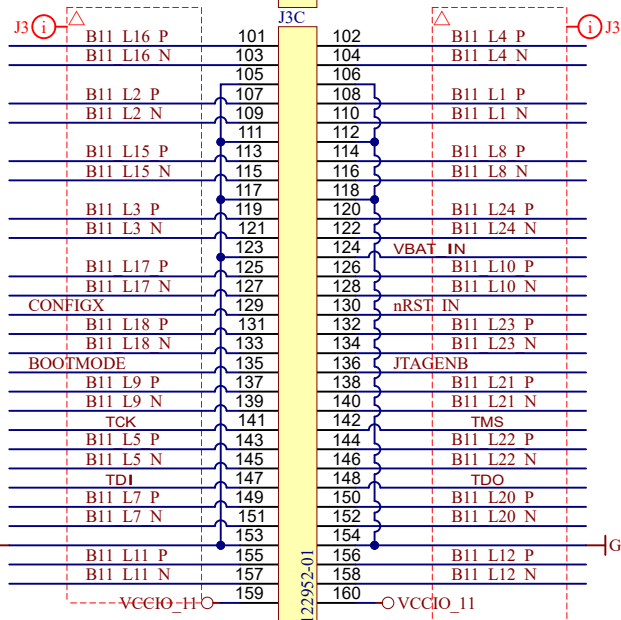
Input



ASP-122952-01

Next signals has different functionality in TE0782 and TEBT0782.

S15328_CLK1_P
S15328_CLK1_N



FPGA JTAG !

Input



Title: HSMC_Connector_J3		
A4	Number: TE0783 92I33HA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page4 of 32
Filename: HSMC_CONN_J3.SchDoc		

1

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4

A

A

B

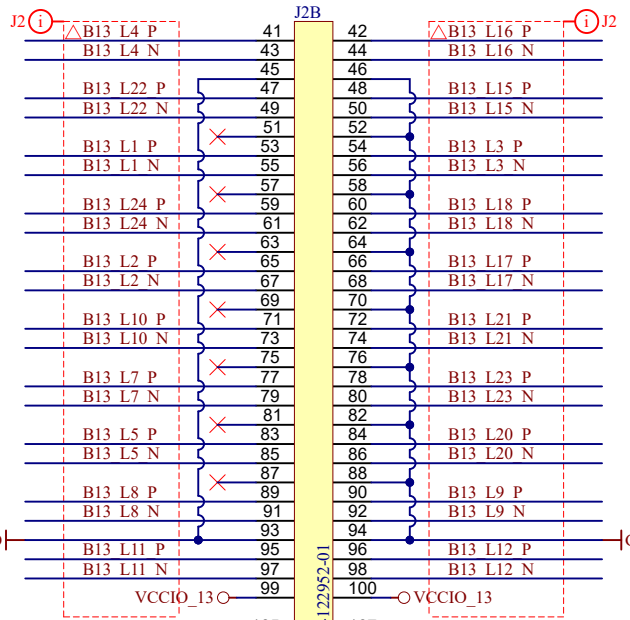
B

C

C

D

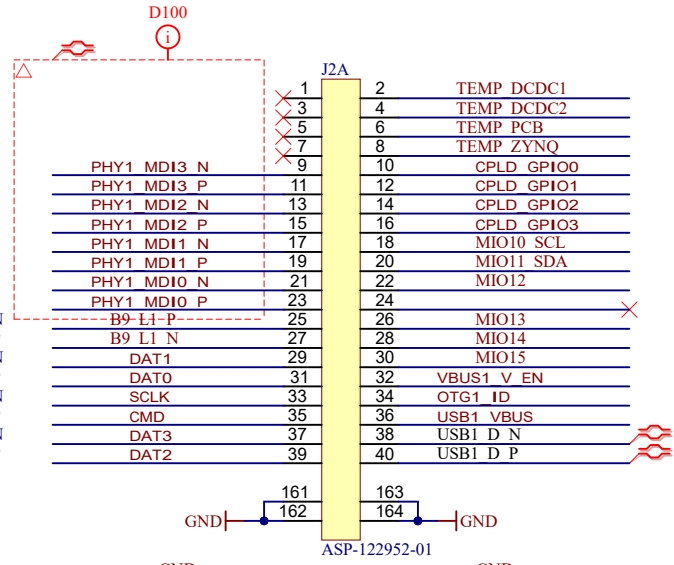
D



Next signals has different functionality in TE0782 and TEBT0782.

TE0782

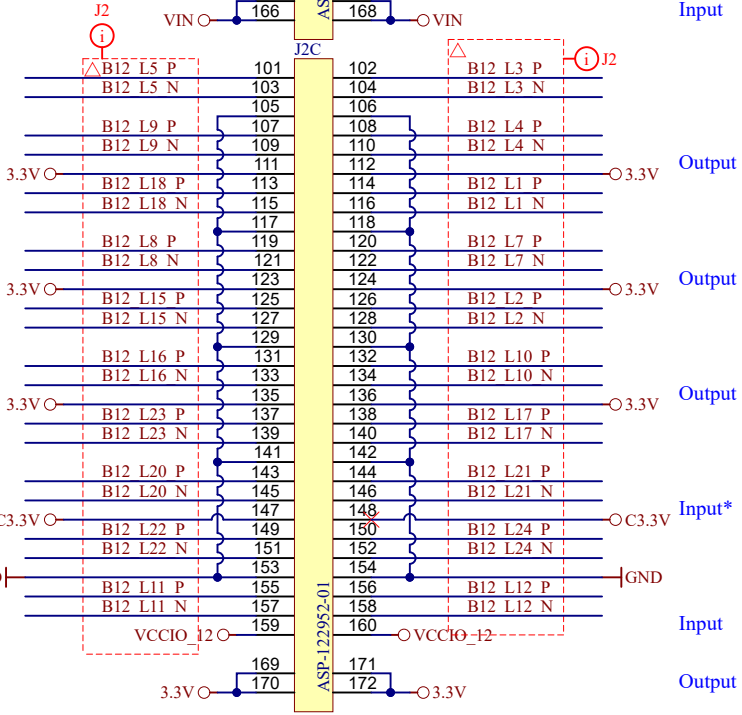
- PHY2_MDI3_N
- PHY2_MDI3_P
- PHY2_MDI2_N
- PHY2_MDI2_P
- PHY2_MDI1_N
- PHY2_MDI1_P
- PHY2_MDI0_N
- PHY2_MDI0_P



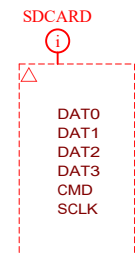
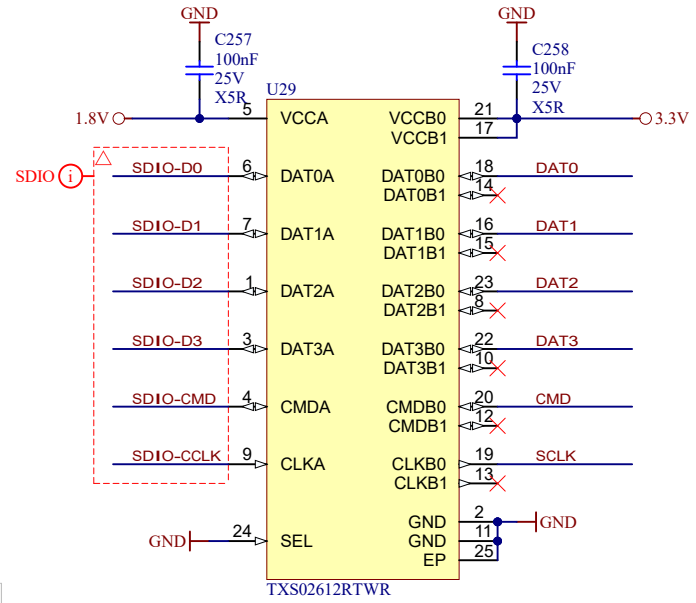
Next signals has different functionality in TE0782 and TEBT0782.

TE0782

- CPLD_GPIO4
- CPLD_GPIO5
- OTG2_ID
- USB2_VBUS
- USB2_D_N
- USB2_D_P
- VBUS2_V_EN



* - C3.3V: Normally leave unconnected



Title: HSMC_Connector_J2		
A4	Number: TE0783 92I33HA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page5 of 32
Filename: HSMC_CONN_J2.SchDoc		

1

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U_PS-DDR
PS-DDR.SchDoc



U_B9
B9.SchDoc



U_MIO-BANKS
MIO-BANKS.SchDoc



U_B10
B10.SchDoc



U_HP-BANKS
HP-BANKS.SchDoc



U_B11
B11.SchDoc



U_FPGA-MGT
FPGA-MGT.SchDoc



U_B12
B12.SchDoc



U_FPGA-CFG
FPGA-CFG.SchDoc



U_B13
B13.SchDoc



U_FPGA-PWR
FPGA-PWR.SchDoc



A

A

B


B

C

C

D

D

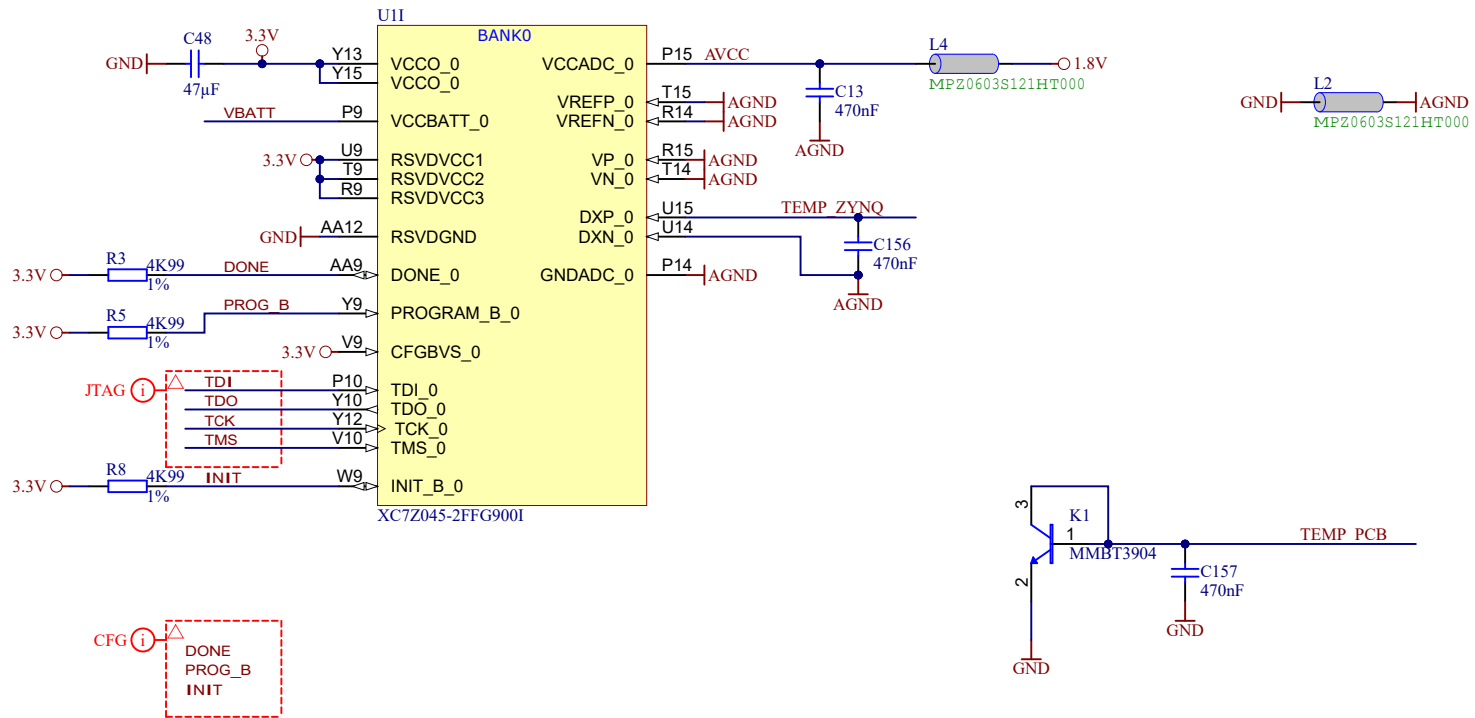
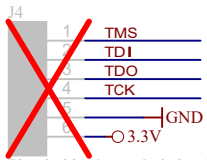
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			A4	Number: TE0783 92I33HA	Rev. 02
Date: 13.07.2018		Copyright: Trenz Electronic GmbH		Page6 of 32	
Filename: SOC.SchDoc					


1

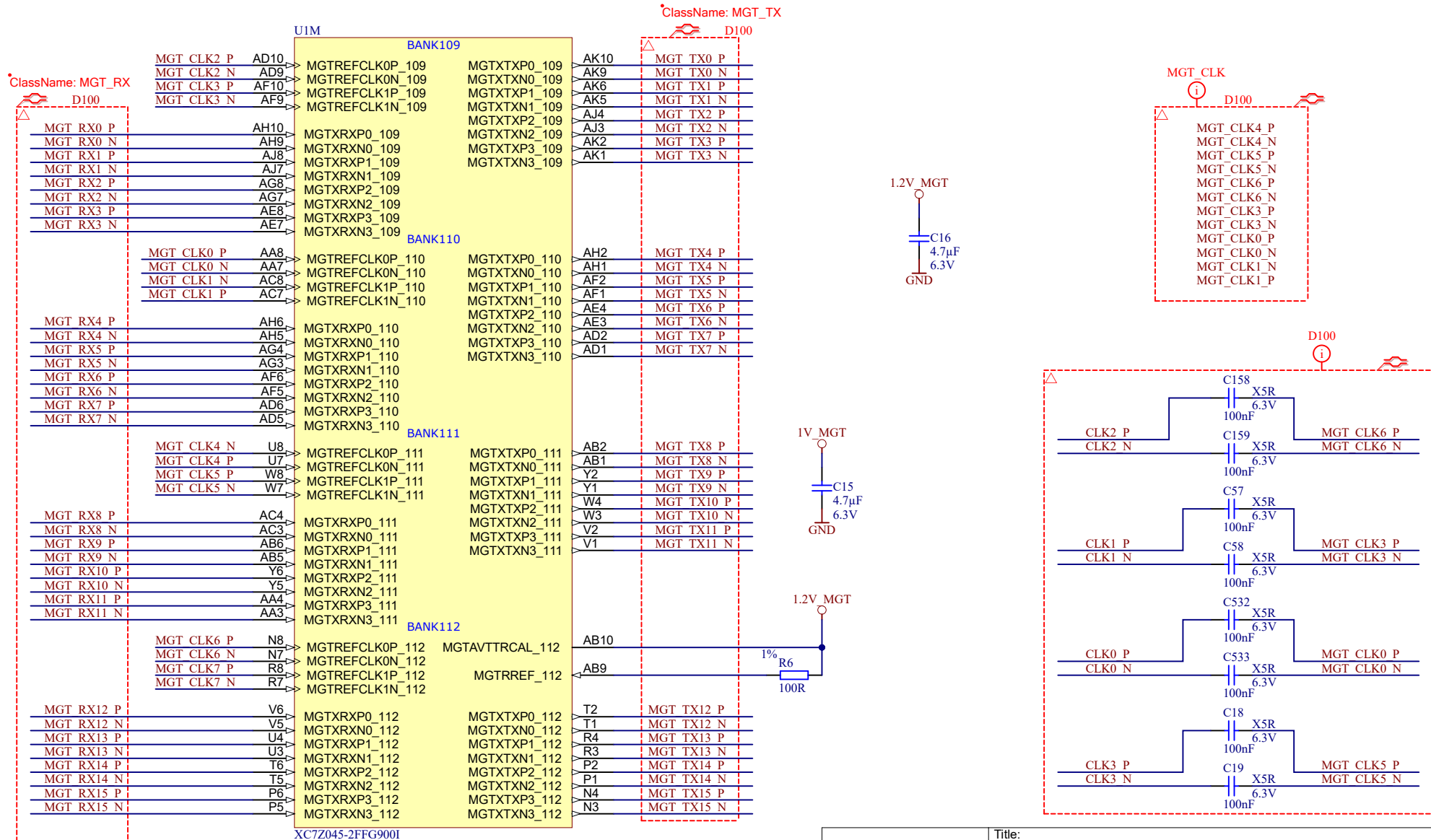
2


3

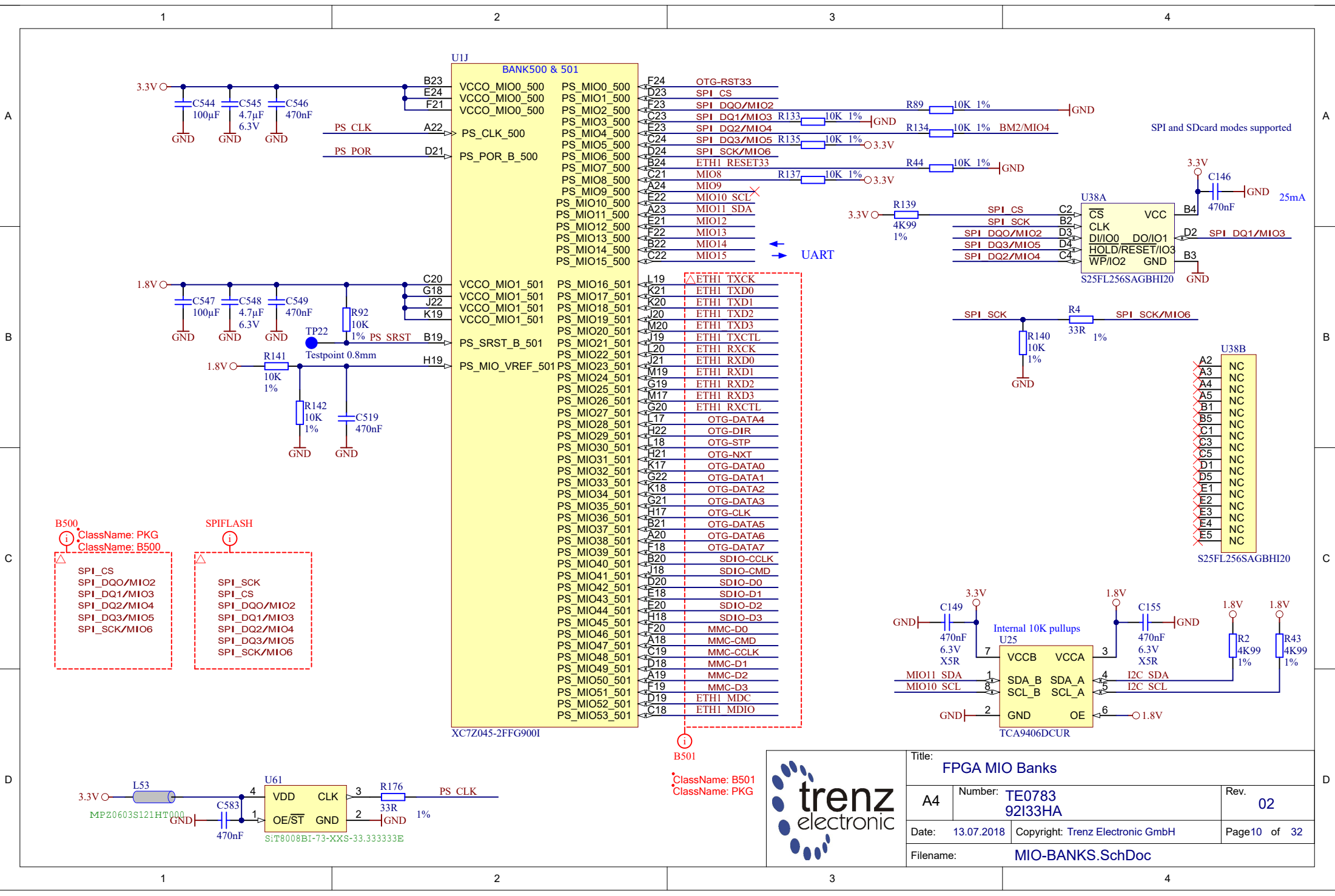
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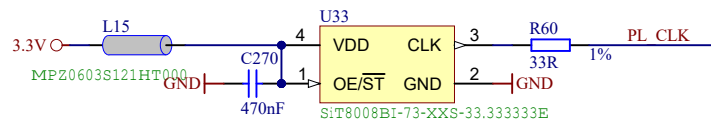
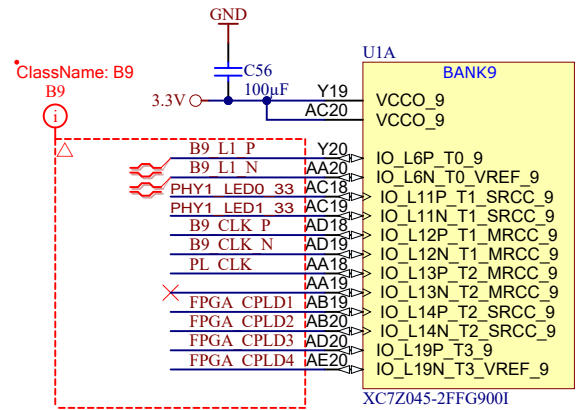
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			A4	Nummer: TE0783 92I33HA Rev. 02
Datum: 13.07.2018		Zeichner: Trenz Electronic GmbH		Blatt 7 von 32
Filename: FPGA-CFG.SchDoc				




			Title: FPGA MGT	
			A4	Number: TE0783 92I33HA
Date: 13.07.2018		Copyright: Trenz Electronic GmbH		Page 9 of 32
Filename: FPGA-MGT.SchDoc				

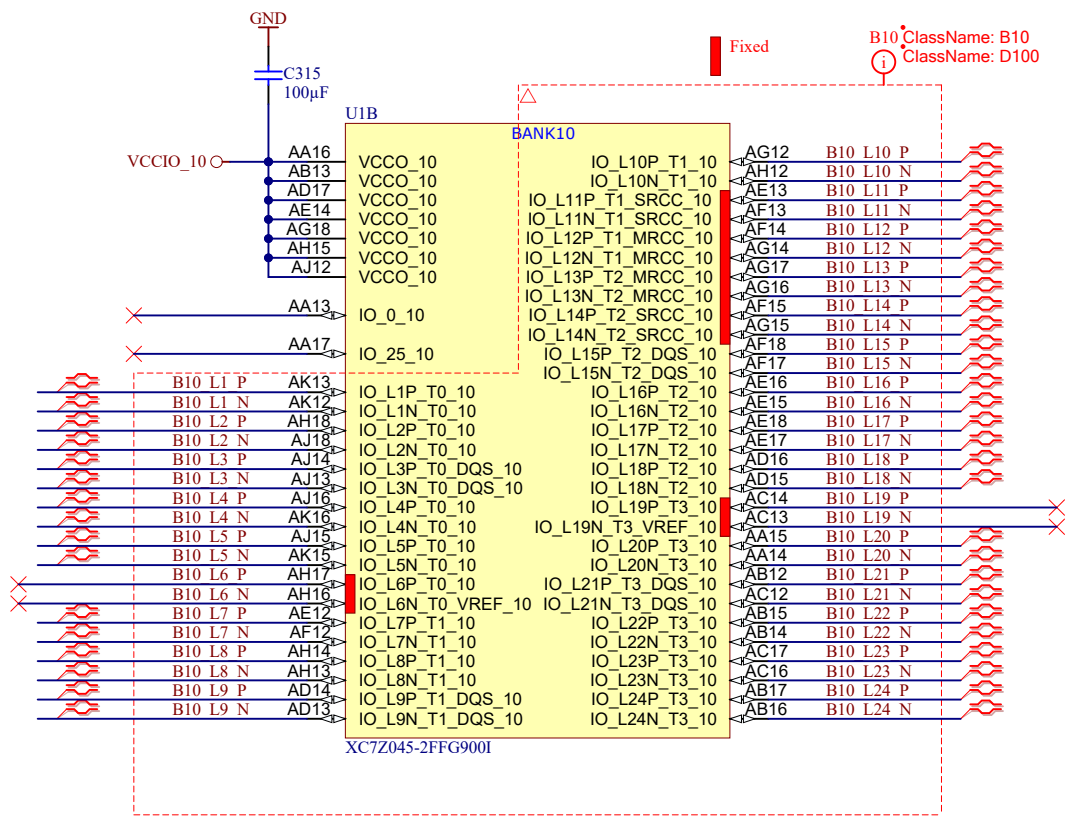


Title: FPGA MIO Banks		
A4	Number: TE0783 92133HA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 10 of 32
Filename: MIO-BANKS.SchDoc		

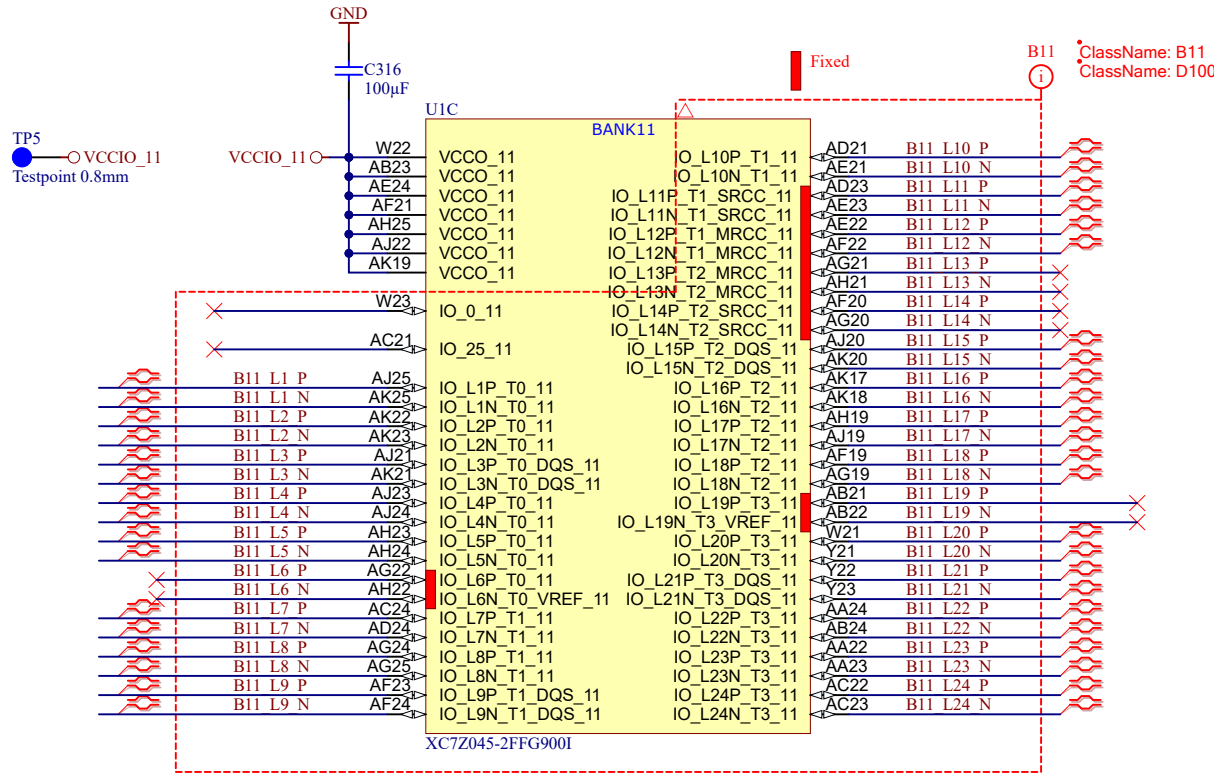


		Title: FPGA B9	
		A4	Number: TE0783 92I33HA
Date: 13.07.2018		Copyright: Trenz Electronic GmbH	
Page 11 of 32		Filename: B9.SchDoc	


TP4
 ● VCCIO_10
 Testpoint 0.8mm

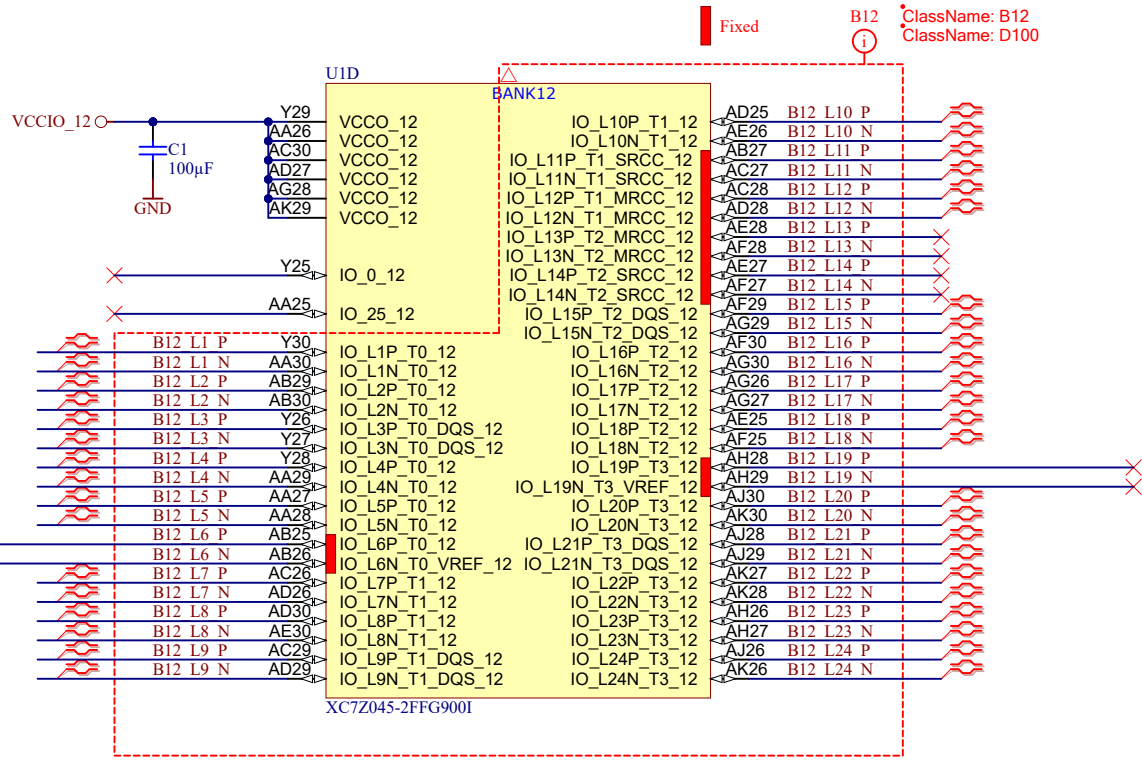


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Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 12 of 32
Filename: B10.SchDoc		

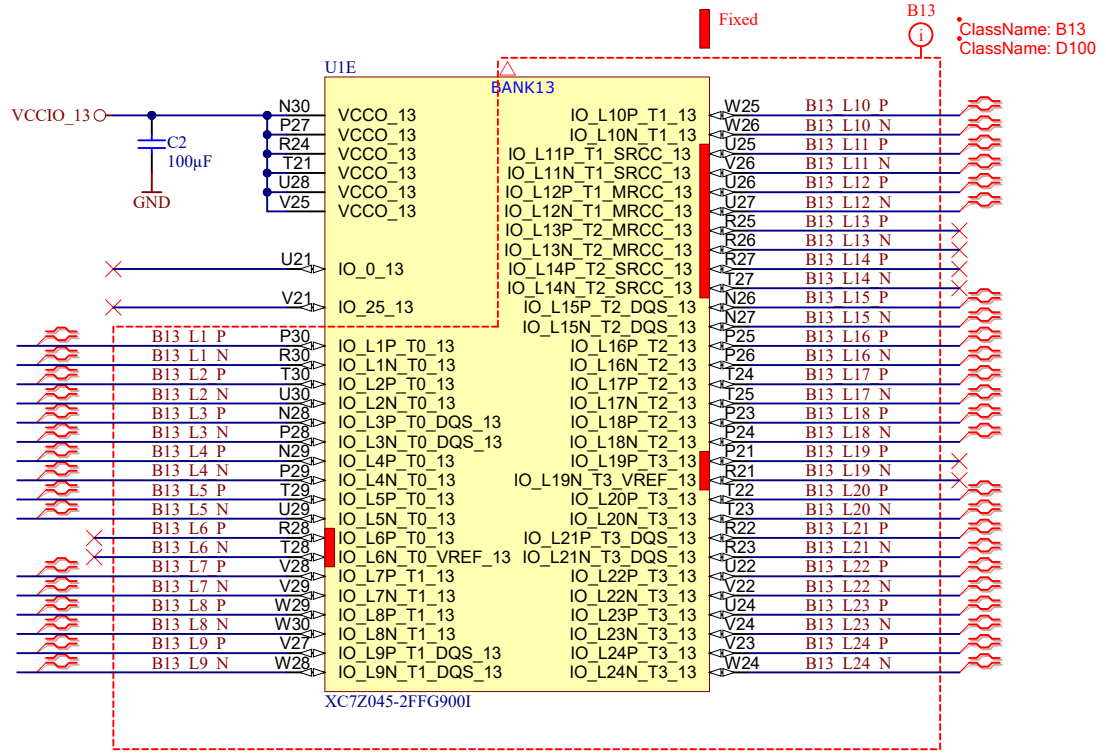
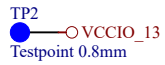


	Title: FPGA B11		
	A4	Number: TE0783 92I33HA	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 13 of 32
	Filename: B11.SchDoc		

TP1
 VCCIO_12
 Testpoint 0.8mm



Title: FPGA B12		
A4	Number: TE0783 92I33HA	Rev. 02
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Filename: B12.SchDoc		



	Title: FPGA B13		
	A4	Number: TE0783 92I33HA	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 15 of 32
	Filename: B13.SchDoc		

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U_B33
B33.SchDoc



U_B34
B34.SchDoc



U_B35
B35.SchDoc



U_DDR3-RAM-PL1
DDR3-RAM-PL1.SchDoc



U_DDR3-RAM-PL2
DDR3-RAM-PL2.SchDoc



A

A

B

B

C

C

D

D



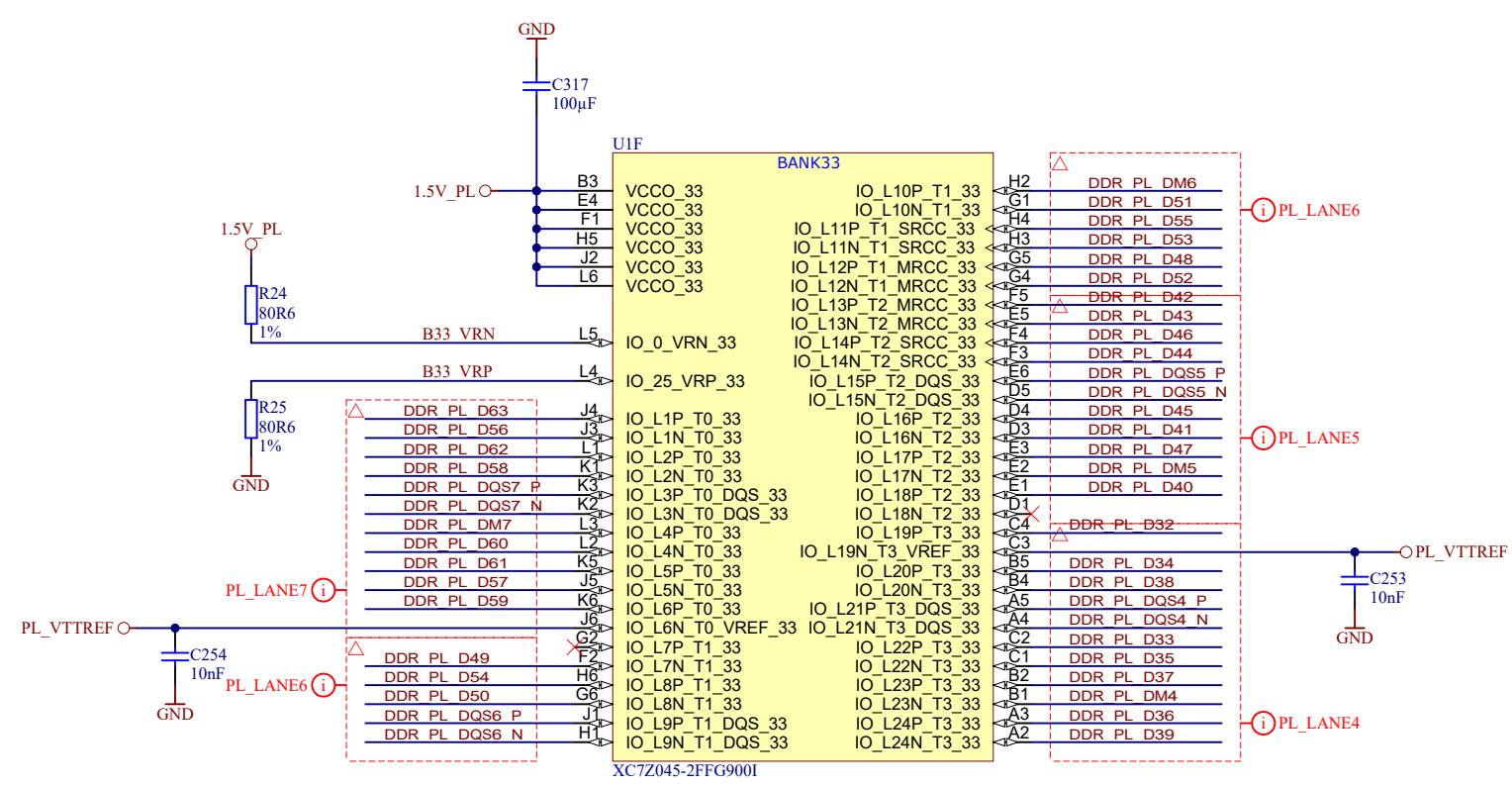
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A4	Number: TE0783 92I33HA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 16 of 32
Filename: HP-BANKS.SchDoc		


1

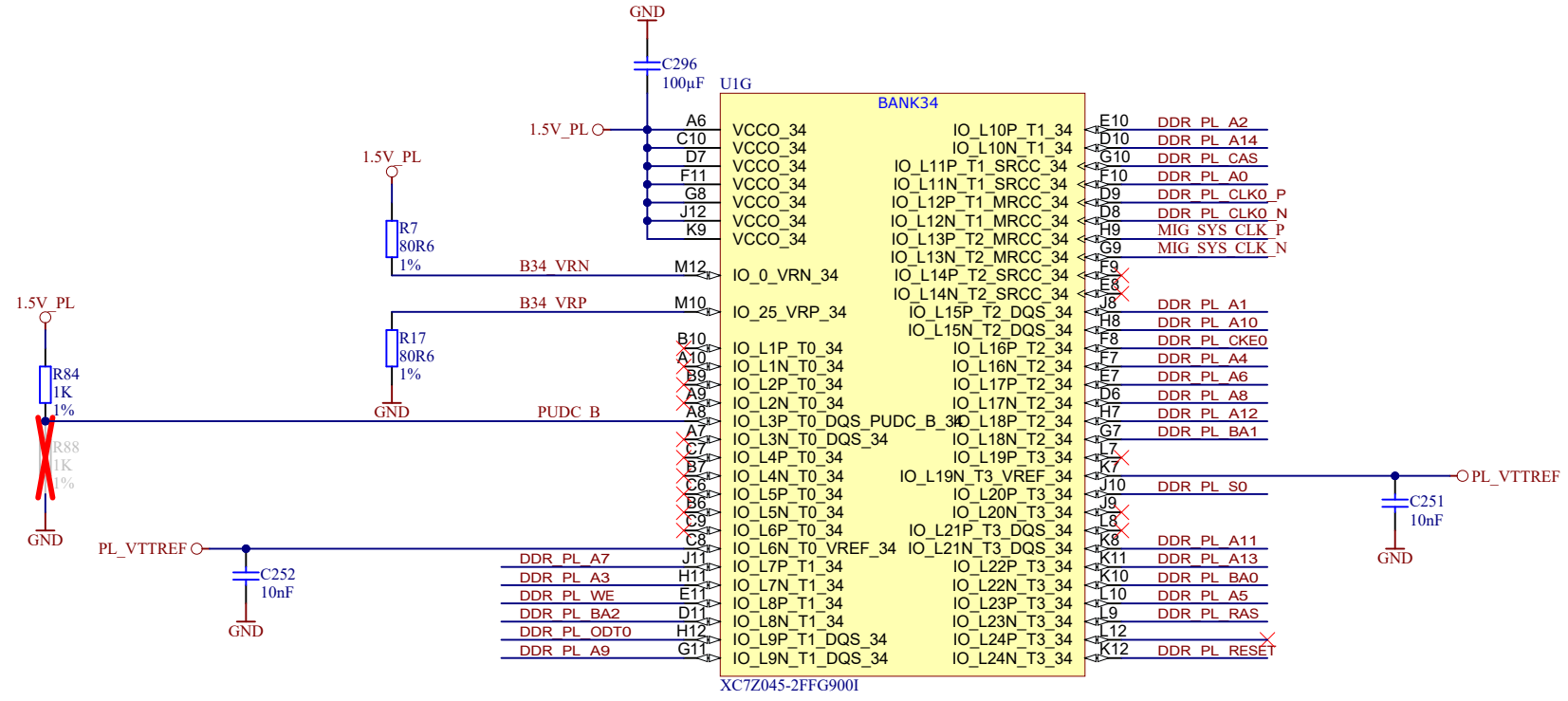
2

3

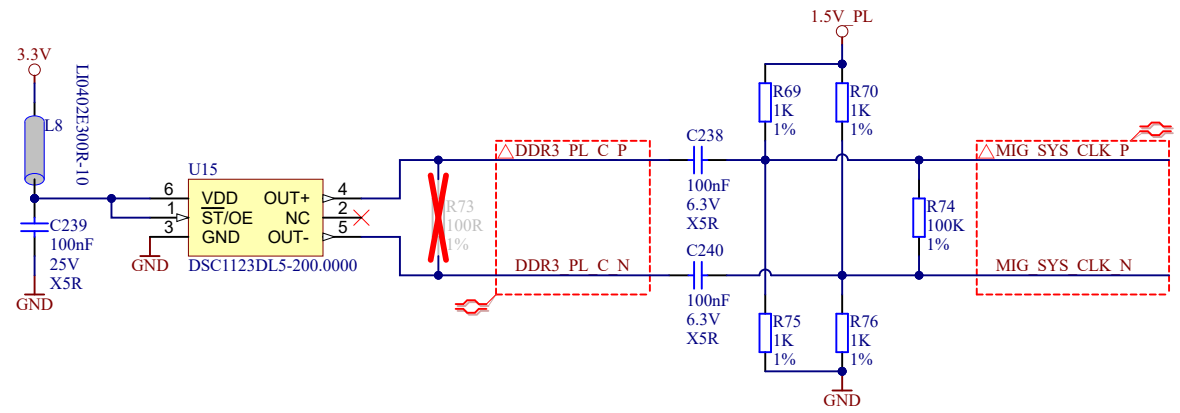
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			Title: FPGA B33	
			A4	Number: TE0783 92I33HA
Date: 13.07.2018		Copyright: Trenz Electronic GmbH		Page 17 of 32
Filename: B33.SchDoc				



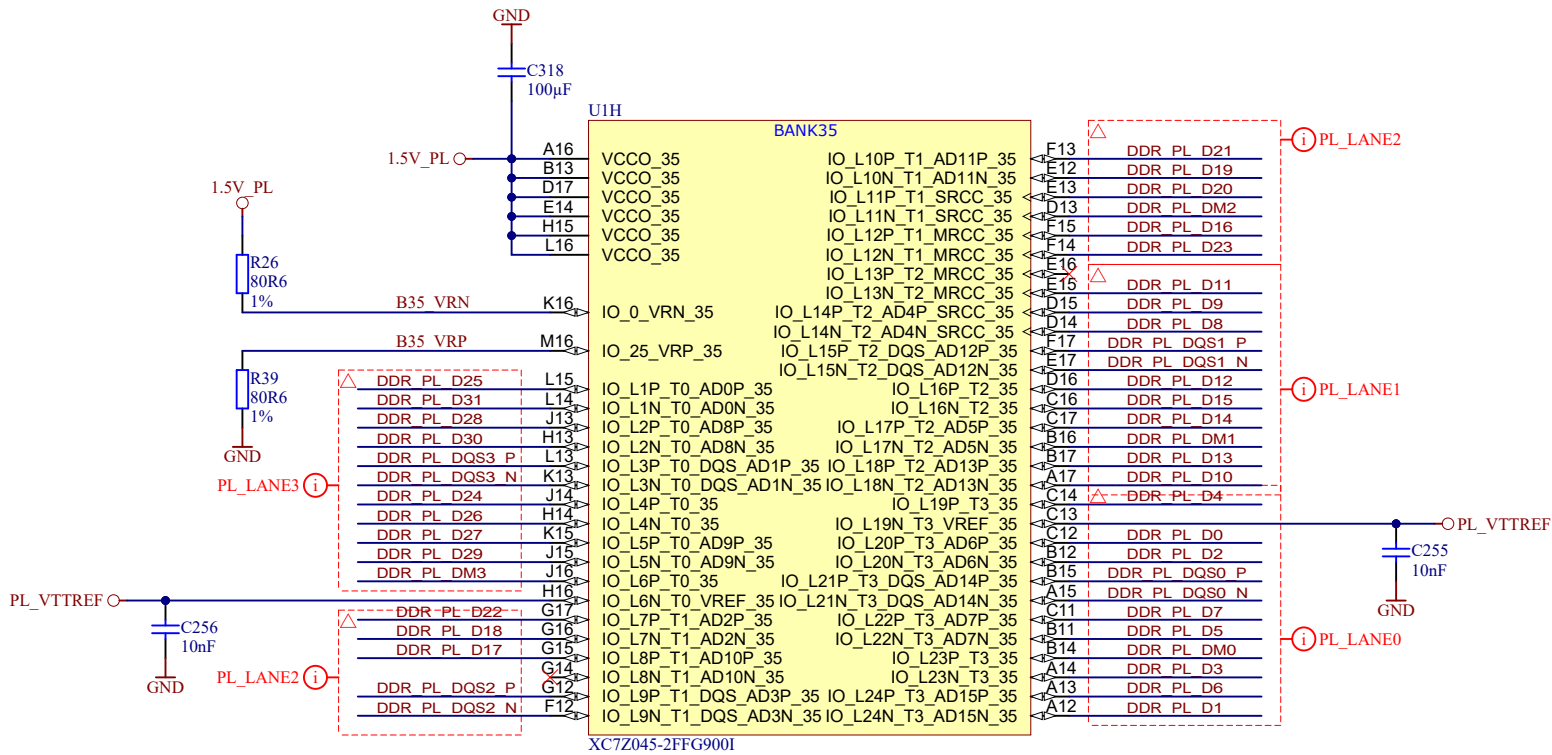
XC7Z045-2FFG900I



Check clock source. R74 100R changed to 100K



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Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 18 of 32
Filename: B34.SchDoc		

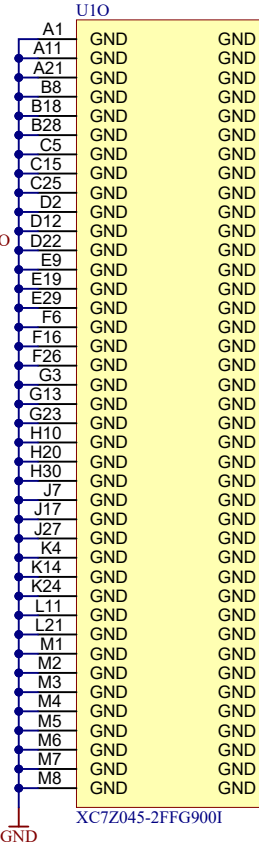
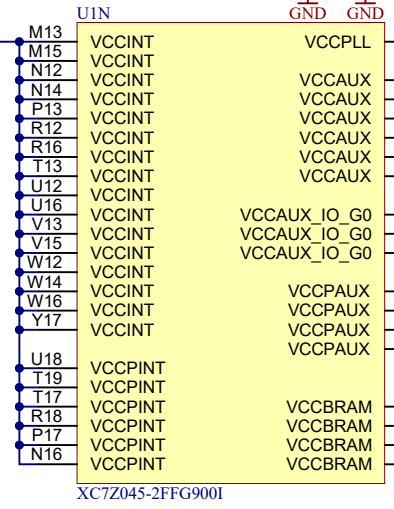
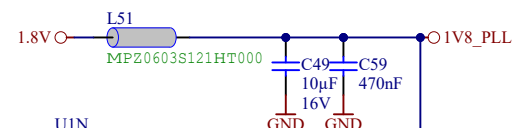
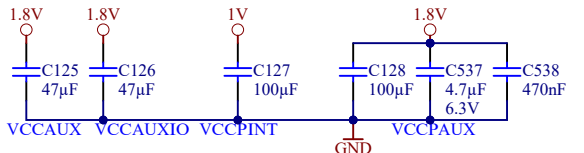
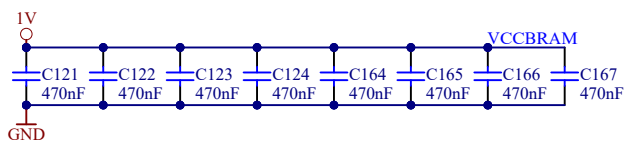
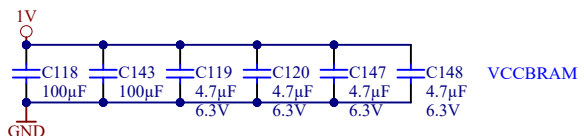
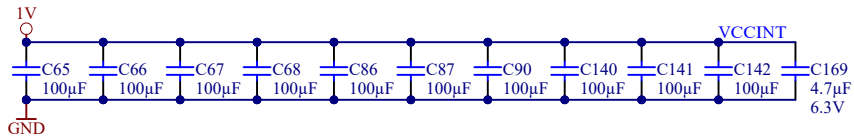
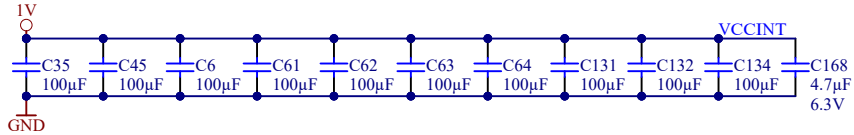


XC7Z045-2FFG9001



Title: FPGA B35		
A4	Number: TE0783 92I33HA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 19 of 32
Filename: B35.SchDoc		

Capacitors suitable for XC7Z100



Title: ZYNQ POWER		
A4	Number: TE0783 92I33HA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page20 of 32
Filename: FPGA-PWR.SchDoc		

A

A

B

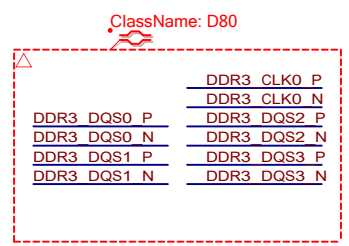
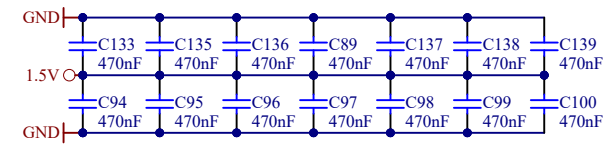
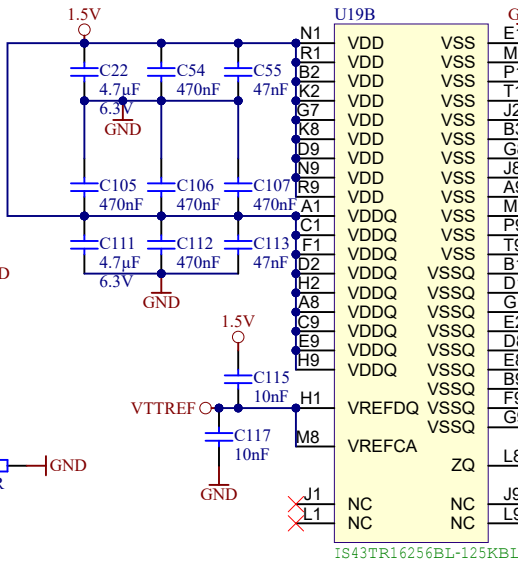
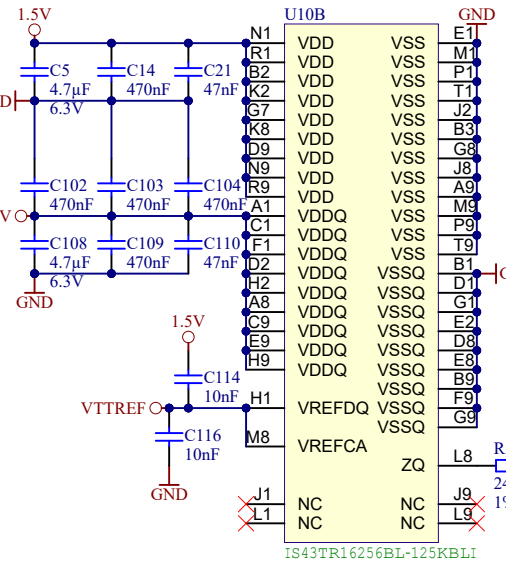
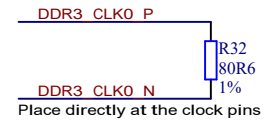
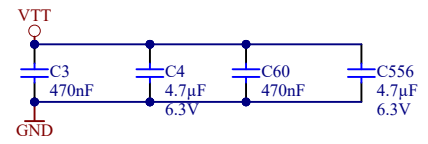
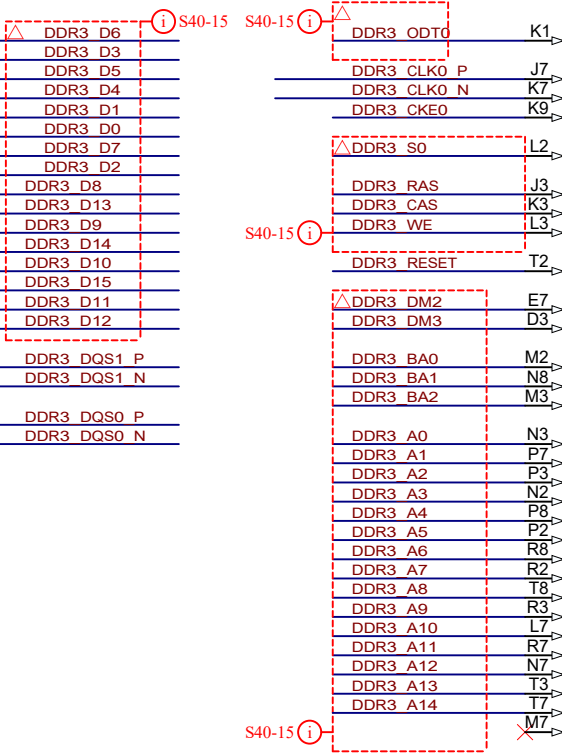
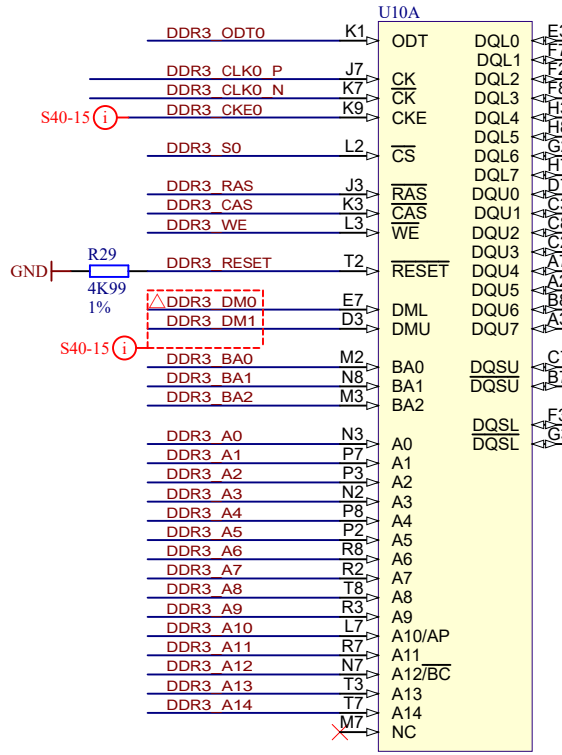
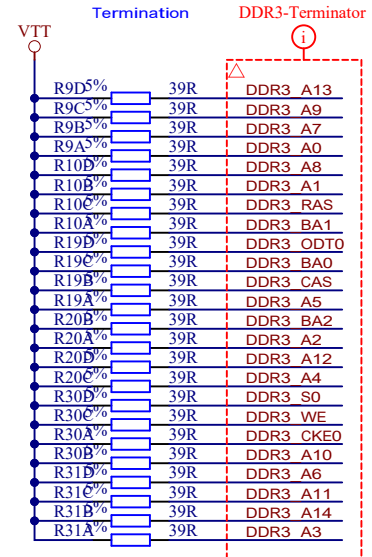
B

C

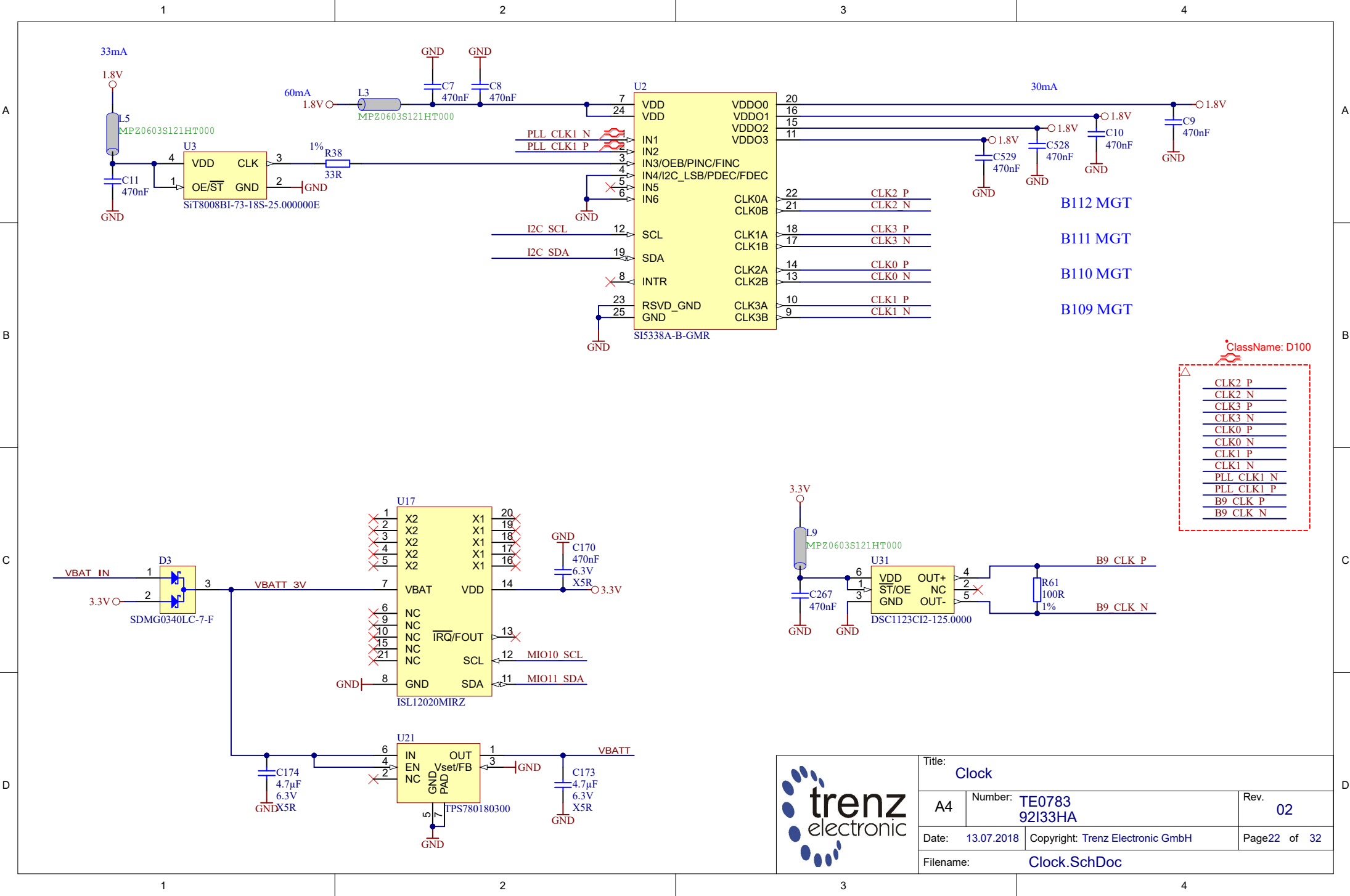
C

D

D




Title: DDR3 RAM PS		
A4	Number: TE0783 92I33HA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 21 of 32
Filename: DDR3-RAM.SchDoc		



ClassName: D100

CLK2 P
CLK2 N
CLK3 P
CLK3 N
CLK0 P
CLK0 N
CLK1 P
CLK1 N
PLL CLK1 N
PLL CLK1 P
B9 CLK P
B9 CLK N



Title: Clock		
A4	Number: TE0783 92I33HA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 22 of 32
Filename: Clock.SchDoc		

A

A

B

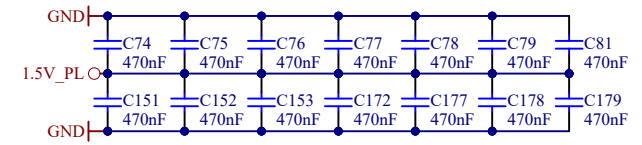
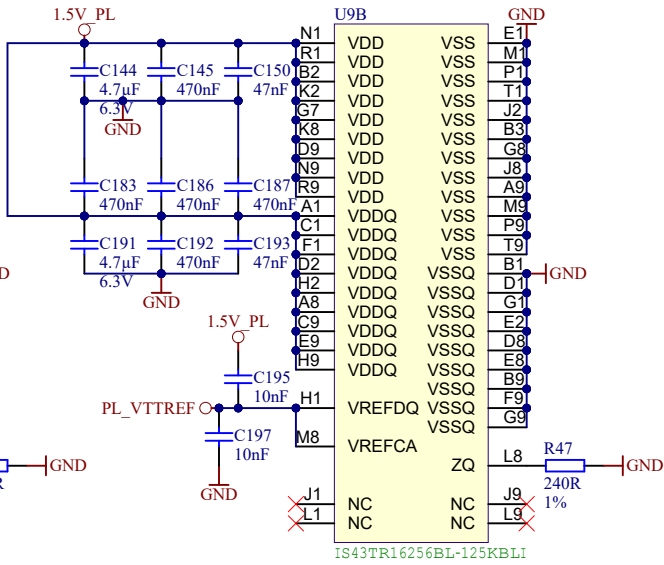
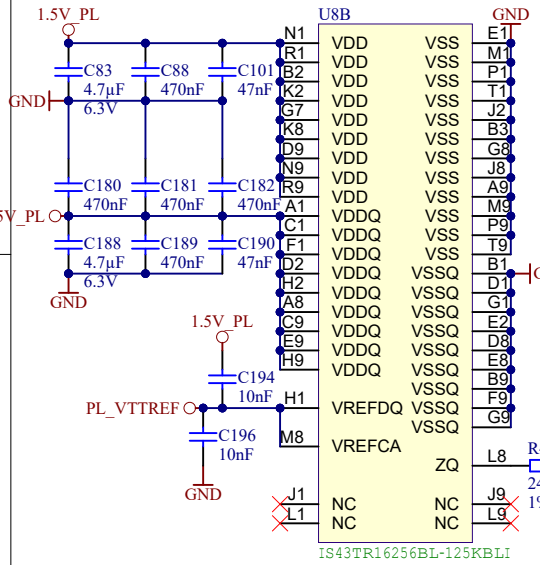
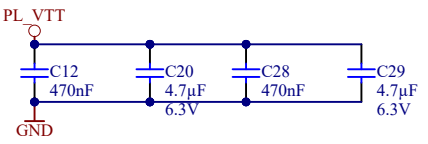
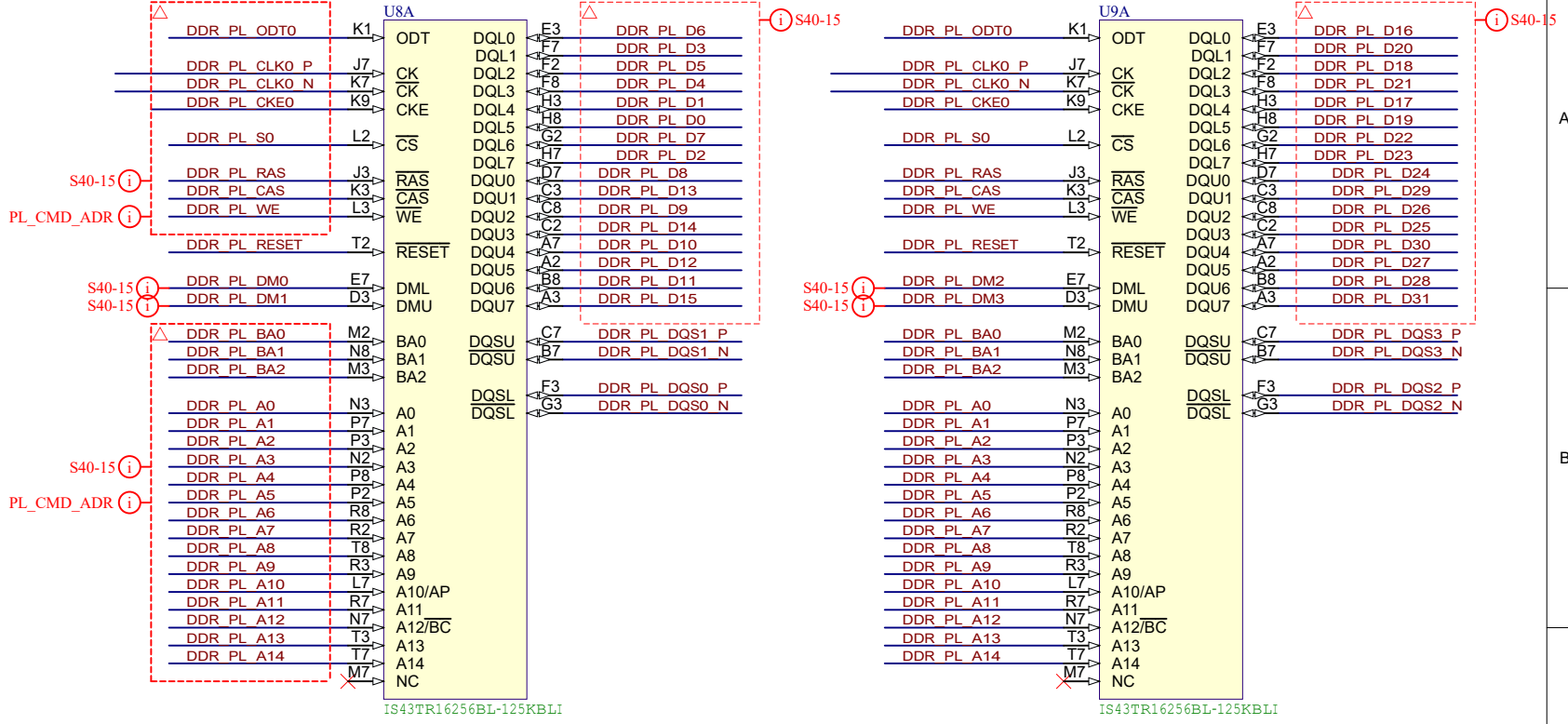
B

C

C

D

D

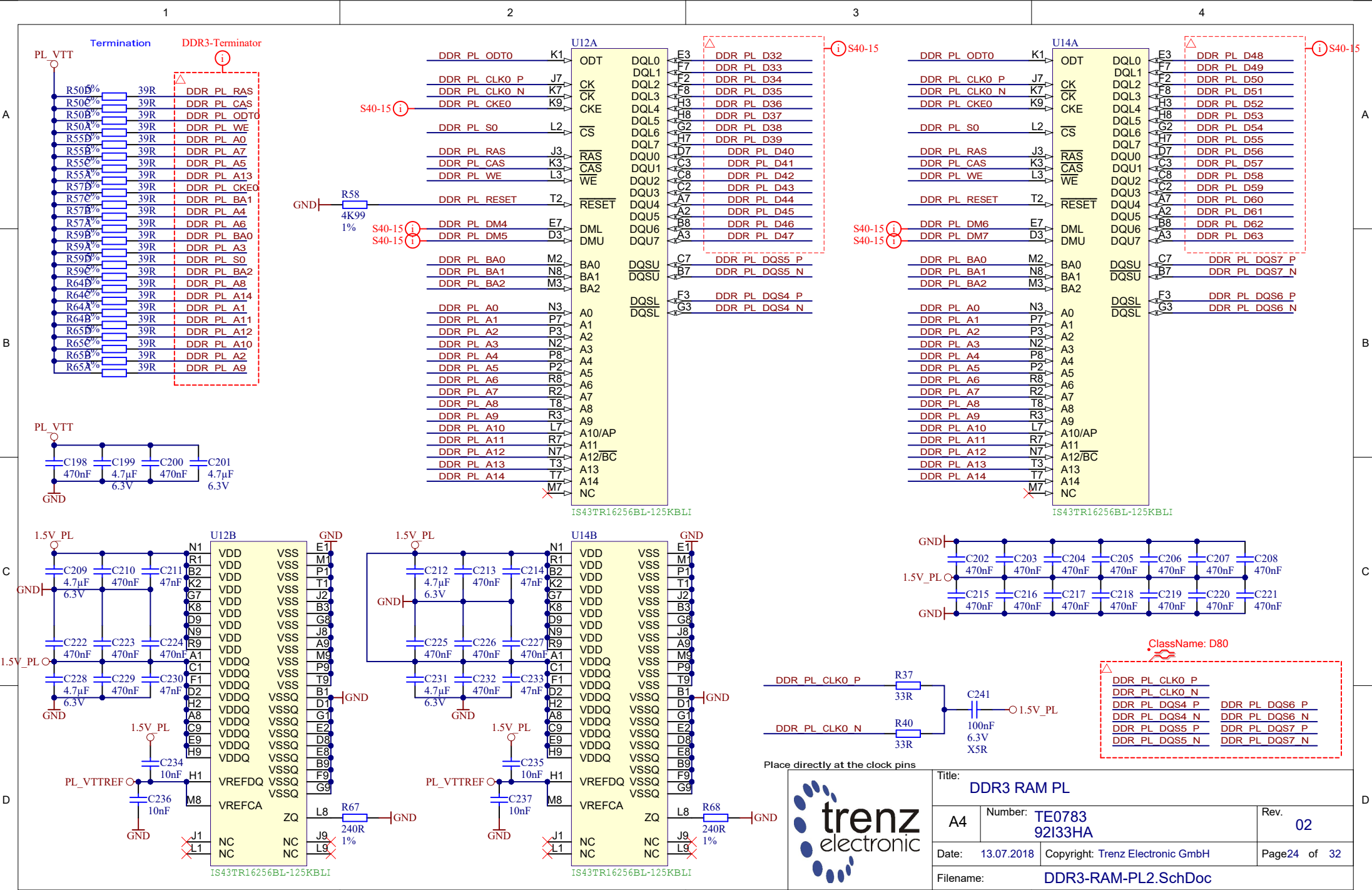


ClassName: D80

DDR PL DQS0 P	DDR PL DQS2 P
DDR PL DQS0 N	DDR PL DQS2 N
DDR PL DQS1 P	DDR PL DQS3 P
DDR PL DQS1 N	DDR PL DQS3 N



Title: DDR3 RAM PL		
A4	Number: TE0783 92133HA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 23 of 32
Filename: DDR3-RAM-PL1.SchDoc		



Title: DDR3 RAM PL		
A4	Number: TE0783 92133HA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 24 of 32
Filename: DDR3-RAM-PL2.SchDoc		

ClassName: D80	
DDR PL CLK0 P	DDR PL DQ56 P
DDR PL CLK0 N	DDR PL DQ57 P
DDR PL DQS4 P	DDR PL DQS6 P
DDR PL DQS4 N	DDR PL DQS7 P
DDR PL DQS5 P	DDR PL DQS7 N
DDR PL DQS5 N	DDR PL DQS6 N

A

B

C

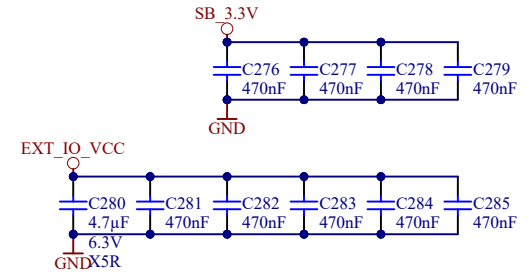
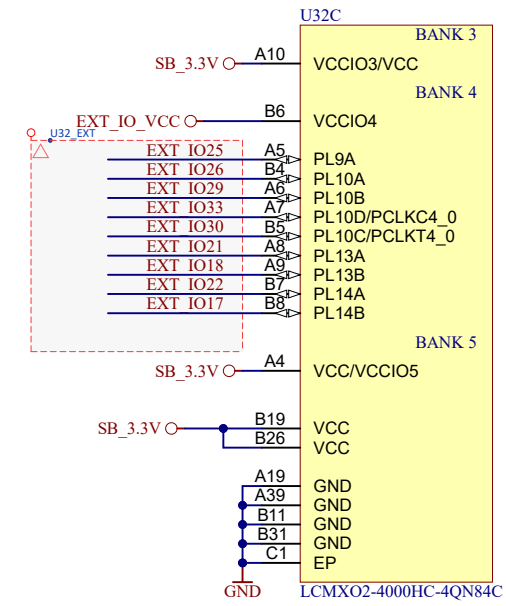
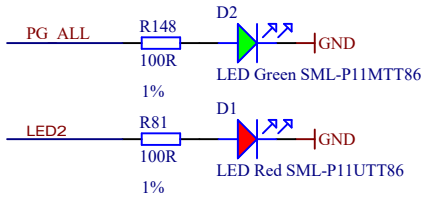
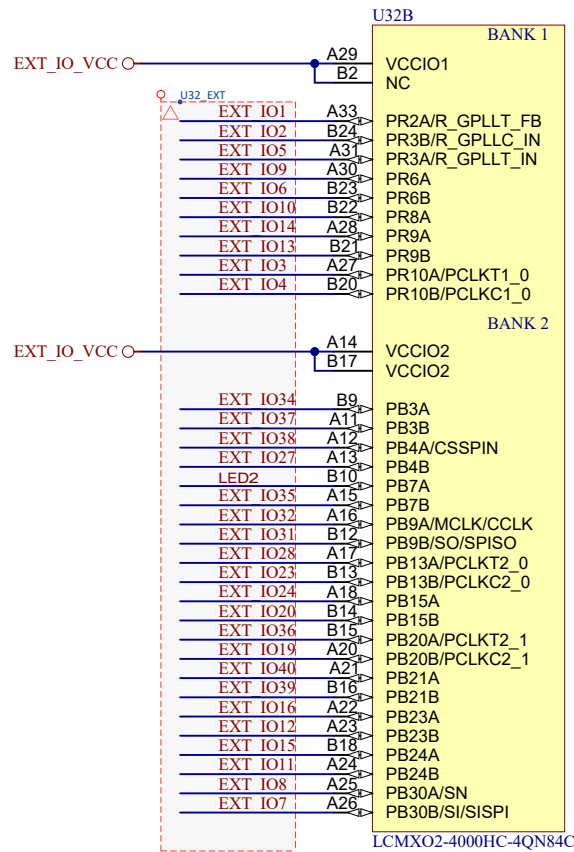
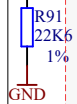
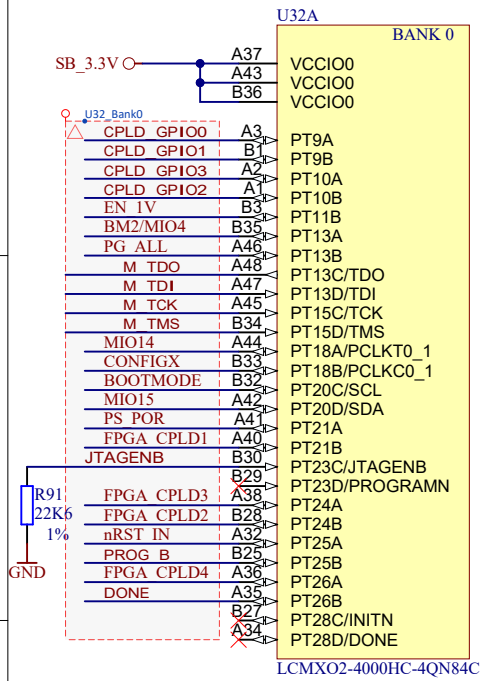
D

A

B

C

D



Title: CPLD			
A4	Number: TE0783 92I33HA	Rev. 02	
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Filename: CPLD.SchDoc			

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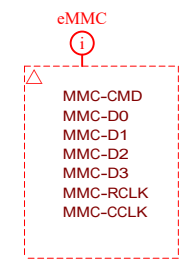
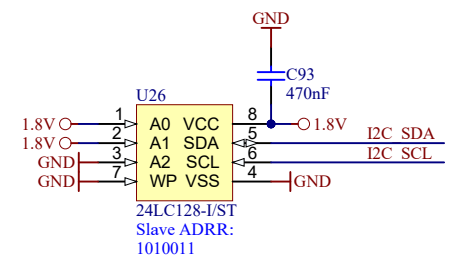
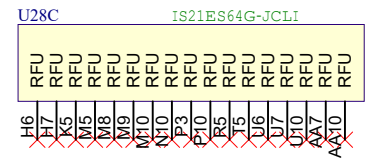
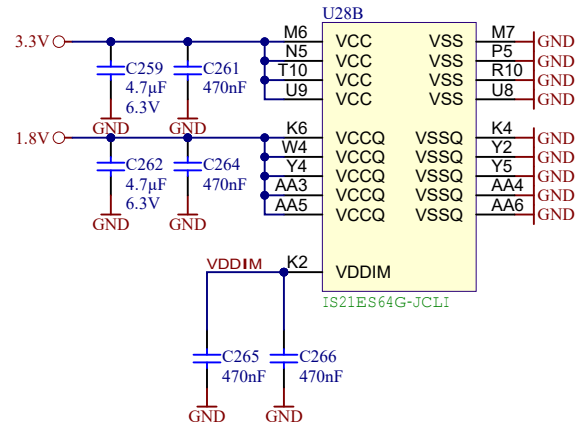
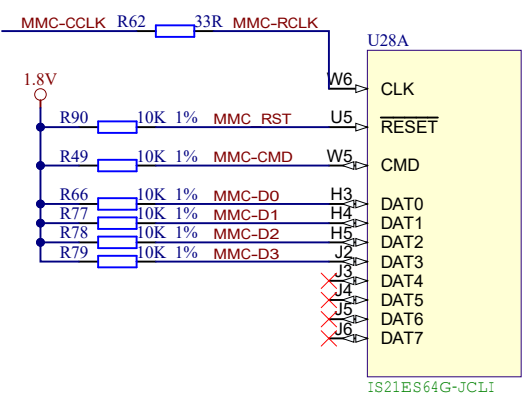
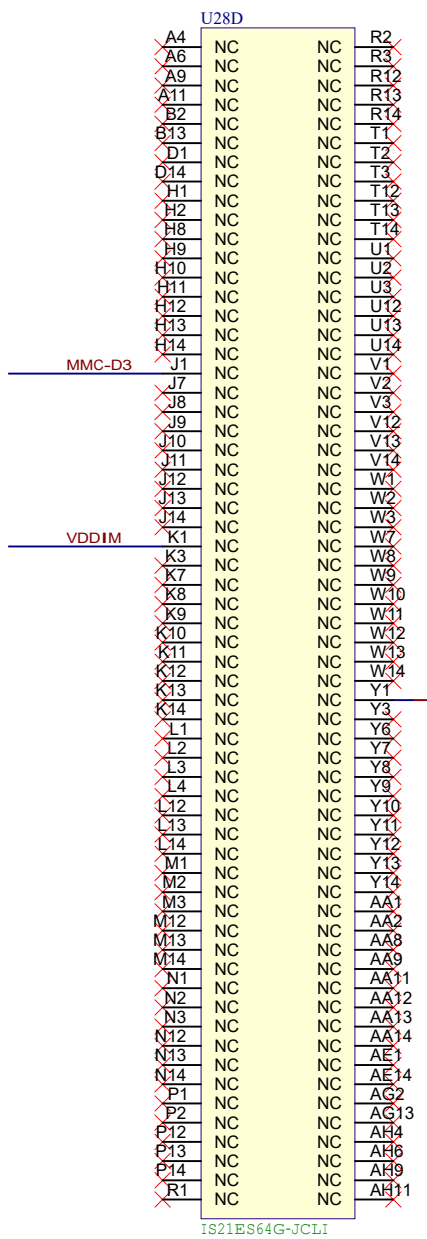
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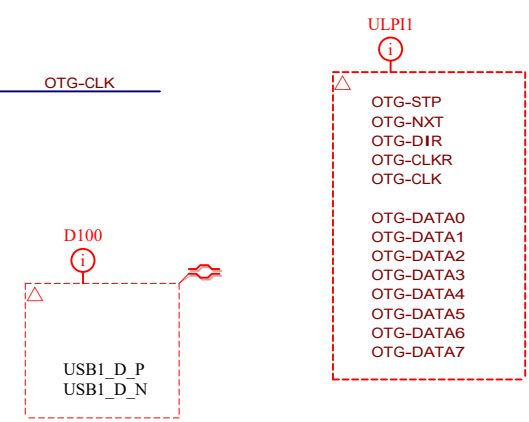
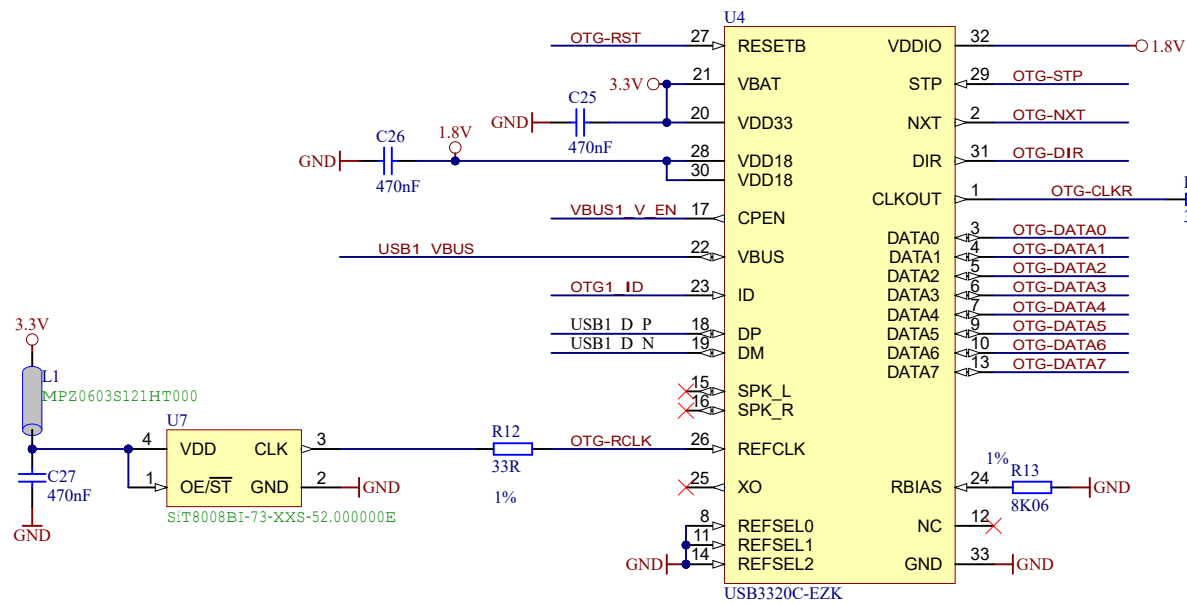
Title: eMMC		
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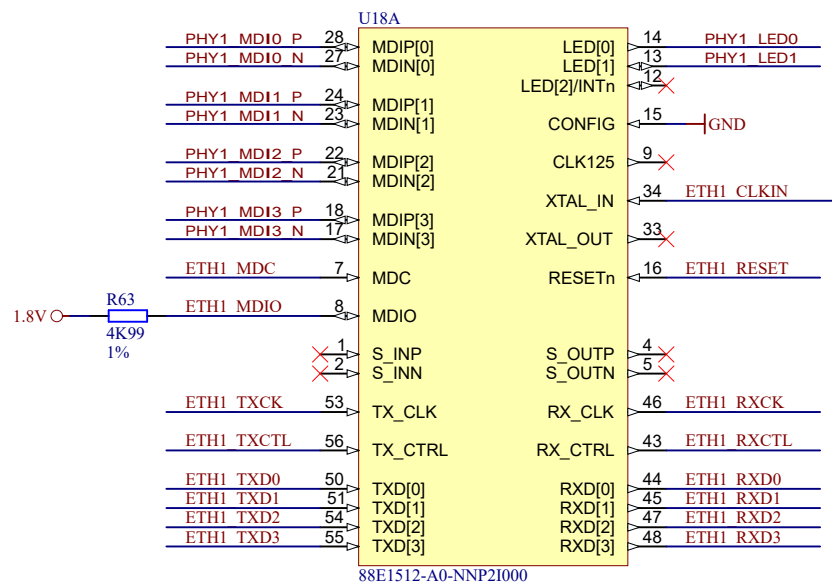
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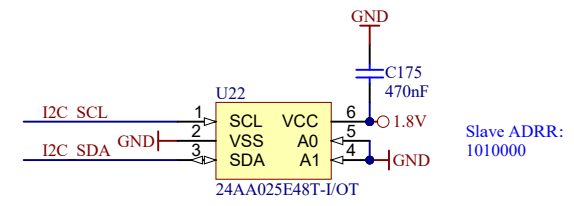
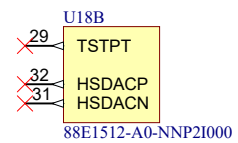
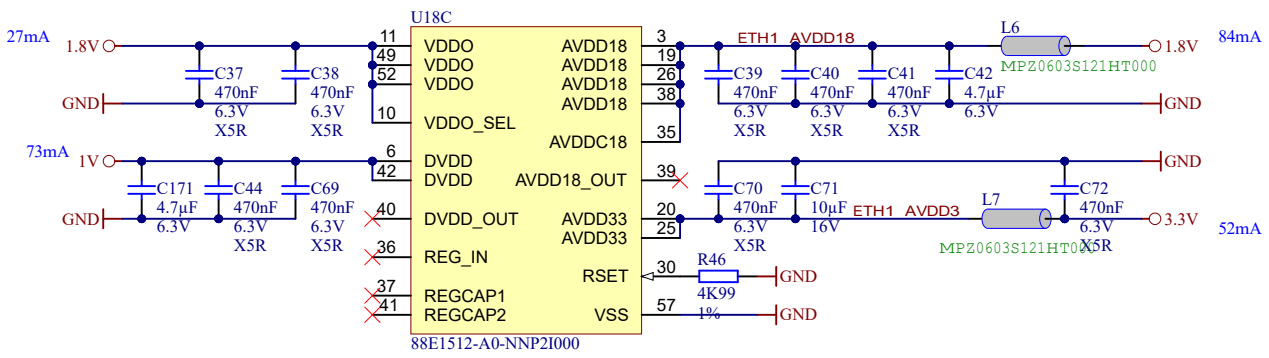
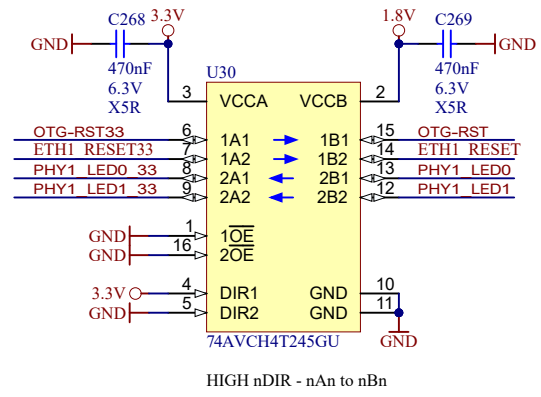
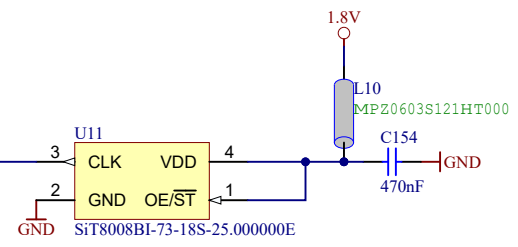
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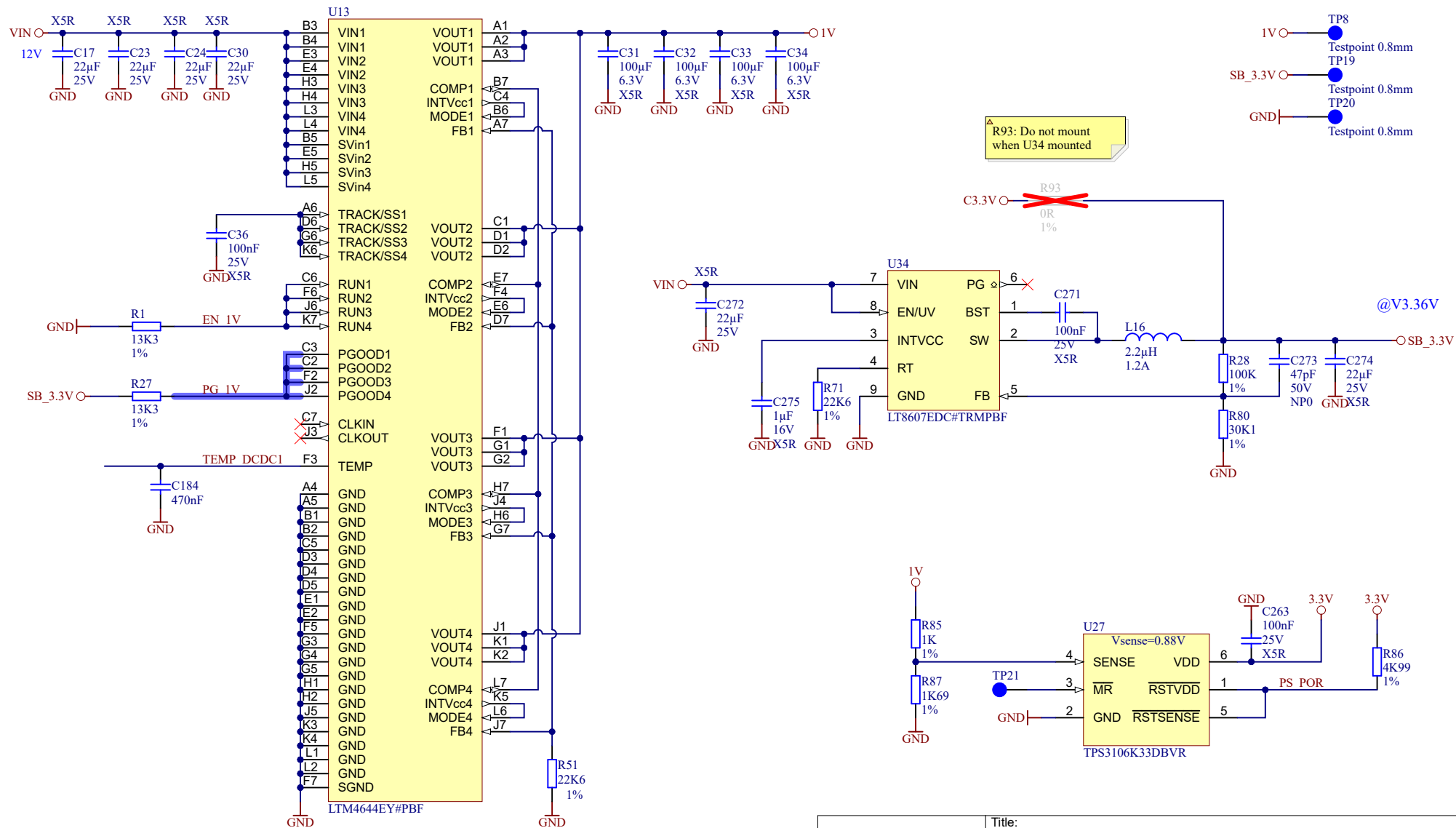
	Title: USB-PHY		
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B9



Title: ETH_PHY1		
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Filename: ETH1.SchDoc		

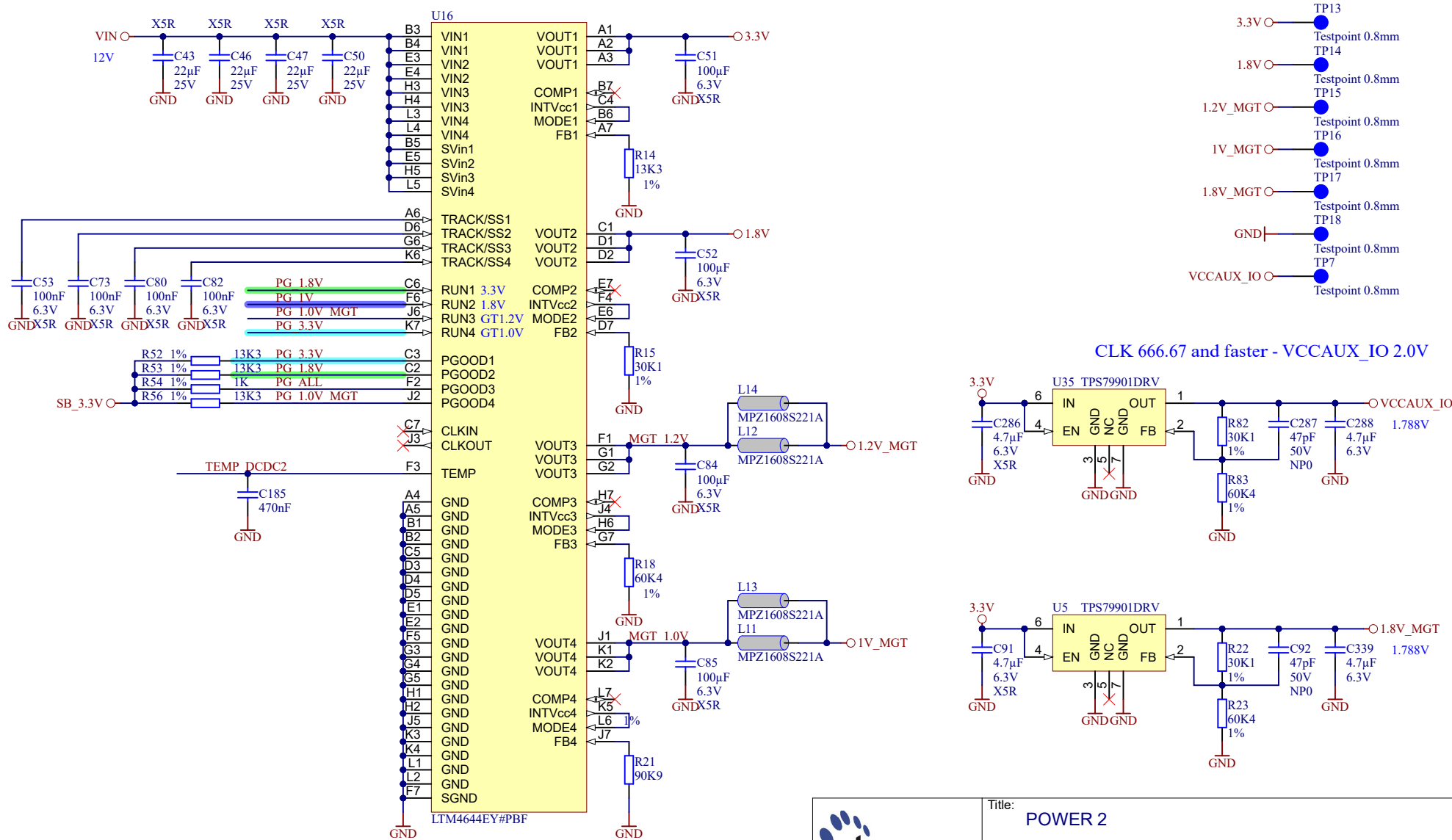


R93: Do not mount when U34 mounted

- 1V ○ TP8 Testpoint 0.8mm
- SB_3.3V ○ TP19 Testpoint 0.8mm
- GND ○ TP20 Testpoint 0.8mm



Title: POWER		
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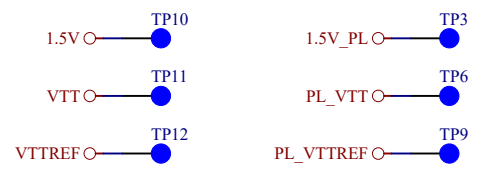
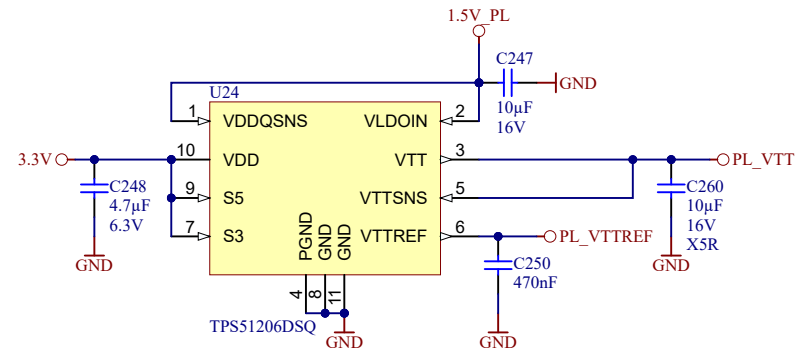
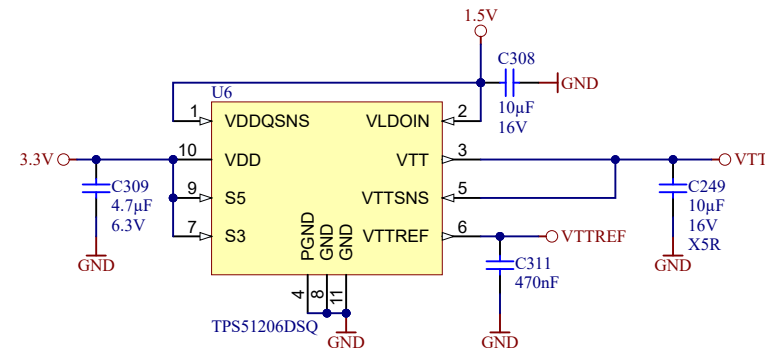
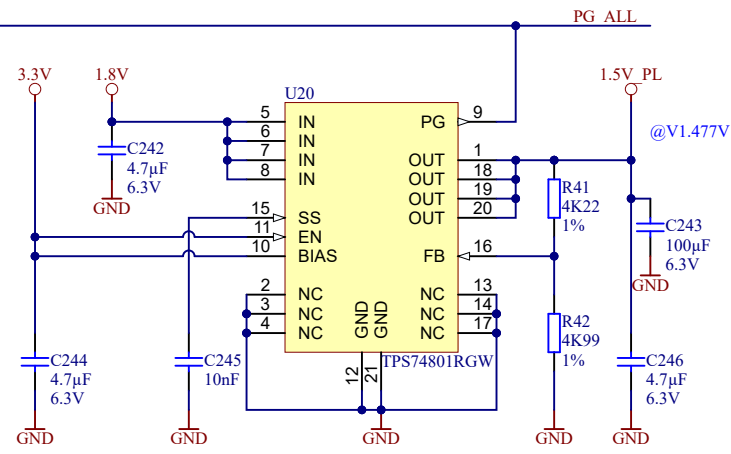
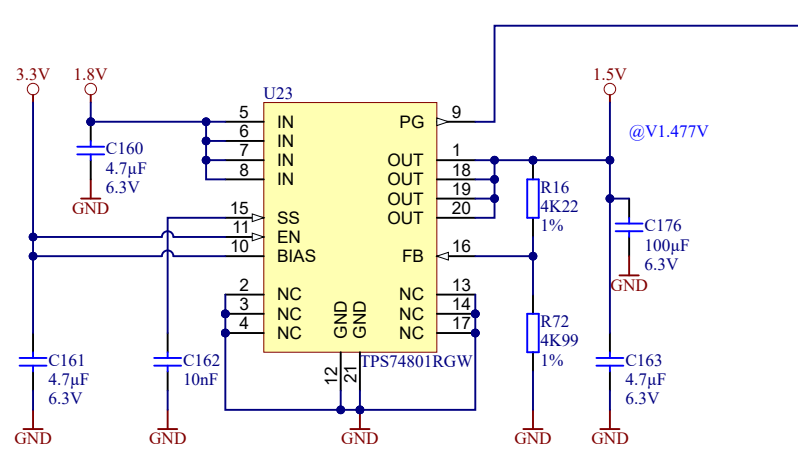


CLK 666.67 and faster - VCCAUX_IO 2.0V

			Title: POWER 2	
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DDR3 PS

DDR3 PL



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REV. 02:

1) Changed power-up sequence: 3.3V next to 1.8V. MGT power domain next to 3.3V

A

A

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B

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C

D

D

	Title: Revision Changes		
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