U_SOC
SOC.SchDoc

U_DDR3-RAM
DDR3-RAM.SchDoc

U_CPLD
CPLD.SchDoc

U_USB-PHY
USB-PHY.SchDoc

U_ETH1
ETH1.SchDoc

U_Clock
Clock.SchDoc

U_eMMC
eMMC.SchDoc

U_POWER2
POWER2.SchDoc

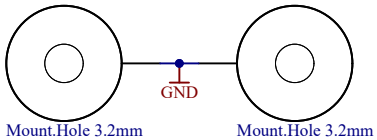
U_Connectors
Connectors.SchDoc

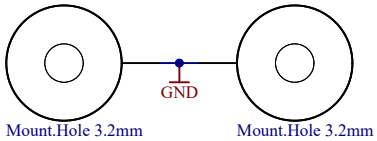
U_Rev_changes
Revision Changes.SchDoc

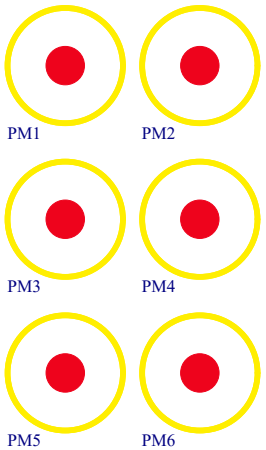
U_POWER
POWER.SchDoc

U_POWER3
POWER3.SchDoc

LOGO1
TE Logo PRINT Layer
LOGO PRINT







Serial
Serial
Serialnumber 6,3 x 6.3mm

Assembly variant	92I33MA
Created by	MR
Modified by	MR
Modified at	2021-09-09
SVN Revision	8604

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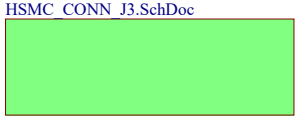
Title: Overview		
A4	Number: TE0783 92I33MA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page1 of 32
Filename: TE0783.SchDoc		

U_HSMC_CONN_J1
HSMC_CONN_J1.SchDoc

U_HSMC_CONN_J2
HSMC_CONN_J2.SchDoc

U_HSMC_CONN_J3
HSMC_CONN_J3.SchDoc



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Title: Connectors			
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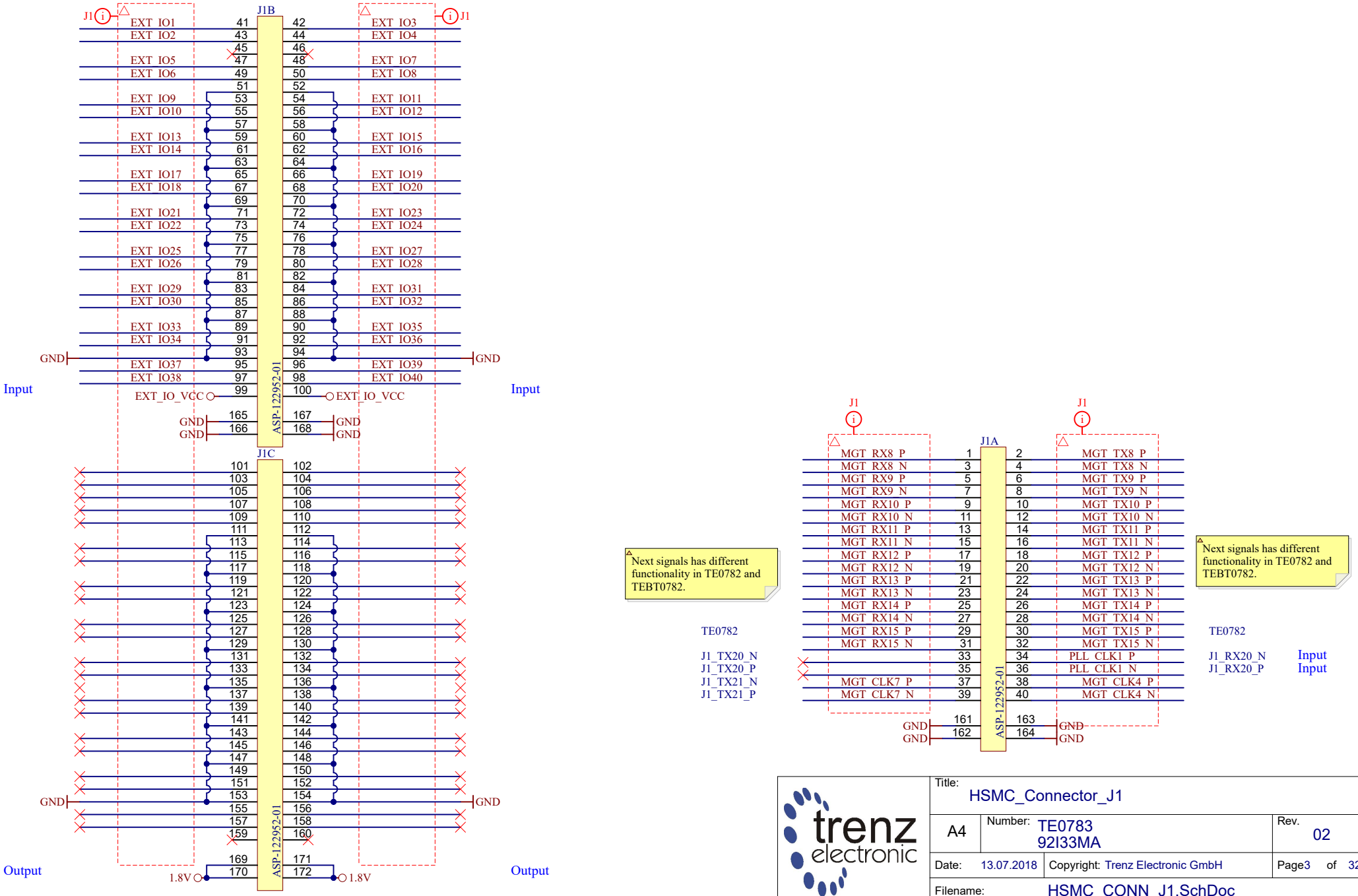
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page2 of 32
Filename: Connectors.SchDoc			



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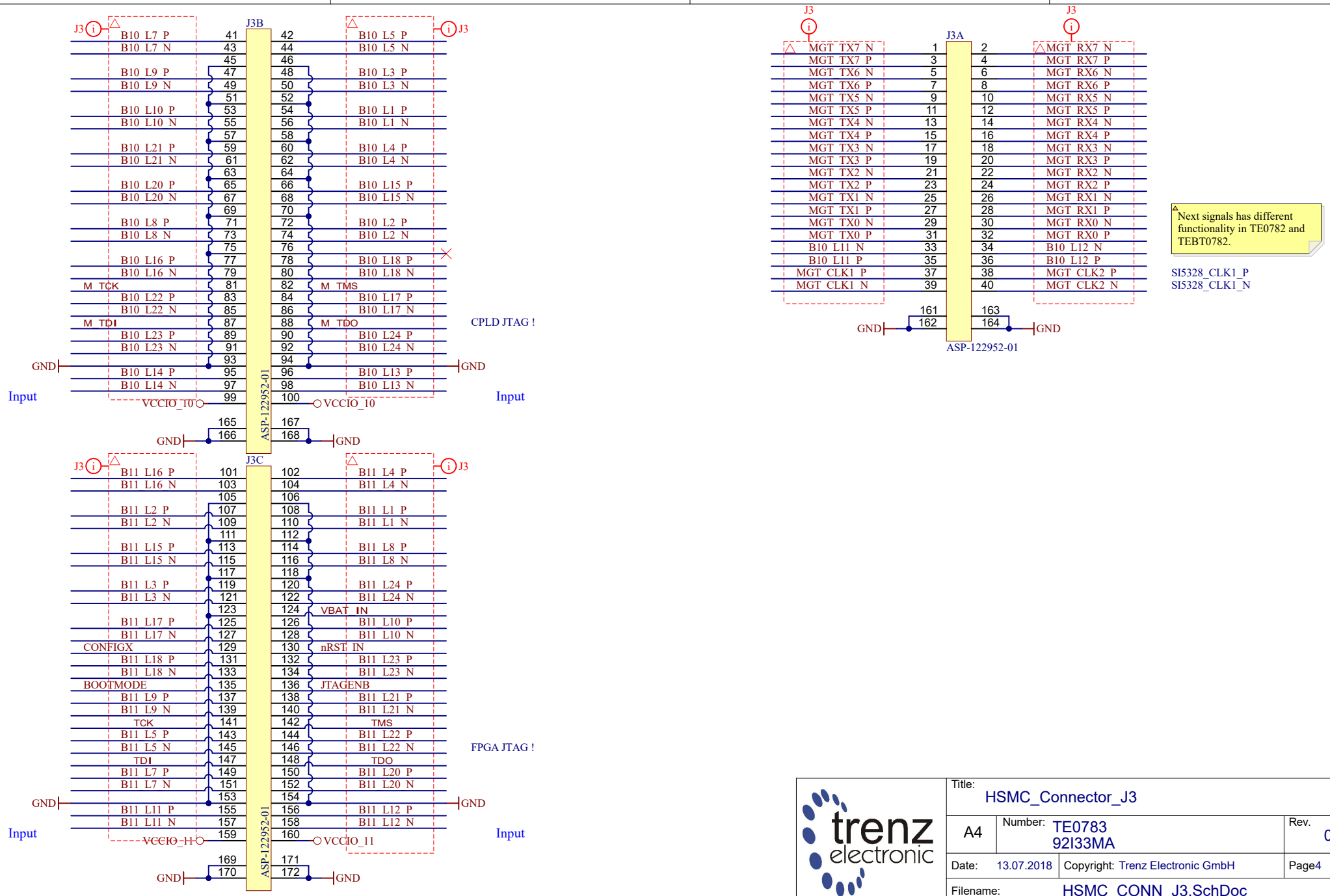
A4	Number: TE0783 92I33MA		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page3 of 32
Filename: HSMC_CONN_J1.SchDoc			


J3B
J3
B10_L7_P 41 42 B10_L5_P
B10_L7_N 43 44 B10_L5_N
45 46
B10_L9_P 47 48 B10_L3_P
B10_L9_N 49 50 B10_L3_N
51 52
B10_L10_P 53 54 B10_L1_P
B10_L10_N 55 56 B10_L1_N
57 58
B10_L21_P 59 60 B10_L4_P
B10_L21_N 61 62 B10_L4_N
63 64
B10_L20_P 65 66 B10_L15_P
B10_L20_N 67 68 B10_L15_N
69 70
B10_L8_P 71 72 B10_L2_P
B10_L8_N 73 74 B10_L2_N
75 76
B10_L16_P 77 78 B10_L18_P
B10_L16_N 79 80 B10_L18_N
M_TCK 81 82 M_TMS
B10_L22_P 83 84 B10_L17_P
B10_L22_N 85 86 B10_L17_N
M_TDI 87 88 M_TDO
B10_L23_P 89 90 B10_L24_P
B10_L23_N 91 92 B10_L24_N
93 94
GND 95 96 GND
B10_L14_P 97 98 B10_L13_P
B10_L14_N 99 100 B10_L13_N
VCCIO_10 VCCIO_10
165 167
GND 166 168 GND
ASP-122952-01
CPLD JTAG !
Input
Input
J3C
J3
B11_L16_P 101 102 B11_L4_P
B11_L16_N 103 104 B11_L4_N
105 106
B11_L2_P 107 108 B11_L1_P
B11_L2_N 109 110 B11_L1_N
111 112
B11_L15_P 113 114 B11_L8_P
B11_L15_N 115 116 B11_L8_N
117 118
B11_L3_P 119 120 B11_L24_P
B11_L3_N 121 122 B11_L24_N
123 124 VBAT_IN
B11_L17_P 125 126 B11_L10_P
B11_L17_N 127 128 B11_L10_N
CONFIGX 129 130 nRST_IN
B11_L18_P 131 132 B11_L23_P
B11_L18_N 133 134 B11_L23_N
BOOTMODE 135 136 JTAGENB
B11_L9_P 137 138 B11_L21_P
B11_L9_N 139 140 B11_L21_N
TCK 141 142 TMS
B11_L5_P 143 144 B11_L22_P
B11_L5_N 145 146 B11_L22_N
TDI 147 148 TDO
B11_L7_P 149 150 B11_L20_P
B11_L7_N 151 152 B11_L20_N
153 154
GND 155 156 GND
B11_L11_P 157 158 B11_L12_P
B11_L11_N 159 160 B11_L12_N
VCCIO_11 VCCIO_11
169 171
GND 170 172 GND
ASP-122952-01
FPGA JTAG !
Input
Input
J3
J3A
J3
MGT_TX7_N 1 2 MGT_RX7_N
MGT_TX7_P 3 4 MGT_RX7_P
MGT_TX6_N 5 6 MGT_RX6_N
MGT_TX6_P 7 8 MGT_RX6_P
MGT_TX5_N 9 10 MGT_RX5_N
MGT_TX5_P 11 12 MGT_RX5_P
MGT_TX4_N 13 14 MGT_RX4_N
MGT_TX4_P 15 16 MGT_RX4_P
MGT_TX3_N 17 18 MGT_RX3_N
MGT_TX3_P 19 20 MGT_RX3_P
MGT_TX2_N 21 22 MGT_RX2_N
MGT_TX2_P 23 24 MGT_RX2_P
MGT_TX1_N 25 26 MGT_RX1_N
MGT_TX1_P 27 28 MGT_RX1_P
MGT_TX0_N 29 30 MGT_RX0_N
MGT_TX0_P 31 32 MGT_RX0_P
B10_L11_N 33 34 B10_L12_N
B10_L11_P 35 36 B10_L12_P
MGT_CLK1_P 37 38 MGT_CLK2_P
MGT_CLK1_N 39 40 MGT_CLK2_N
161 163
GND 162 164 GND
ASP-122952-01
Next signals has different functionality in TE0782 and TEBT0782.
SI5328_CLK1_P
SI5328_CLK1_N
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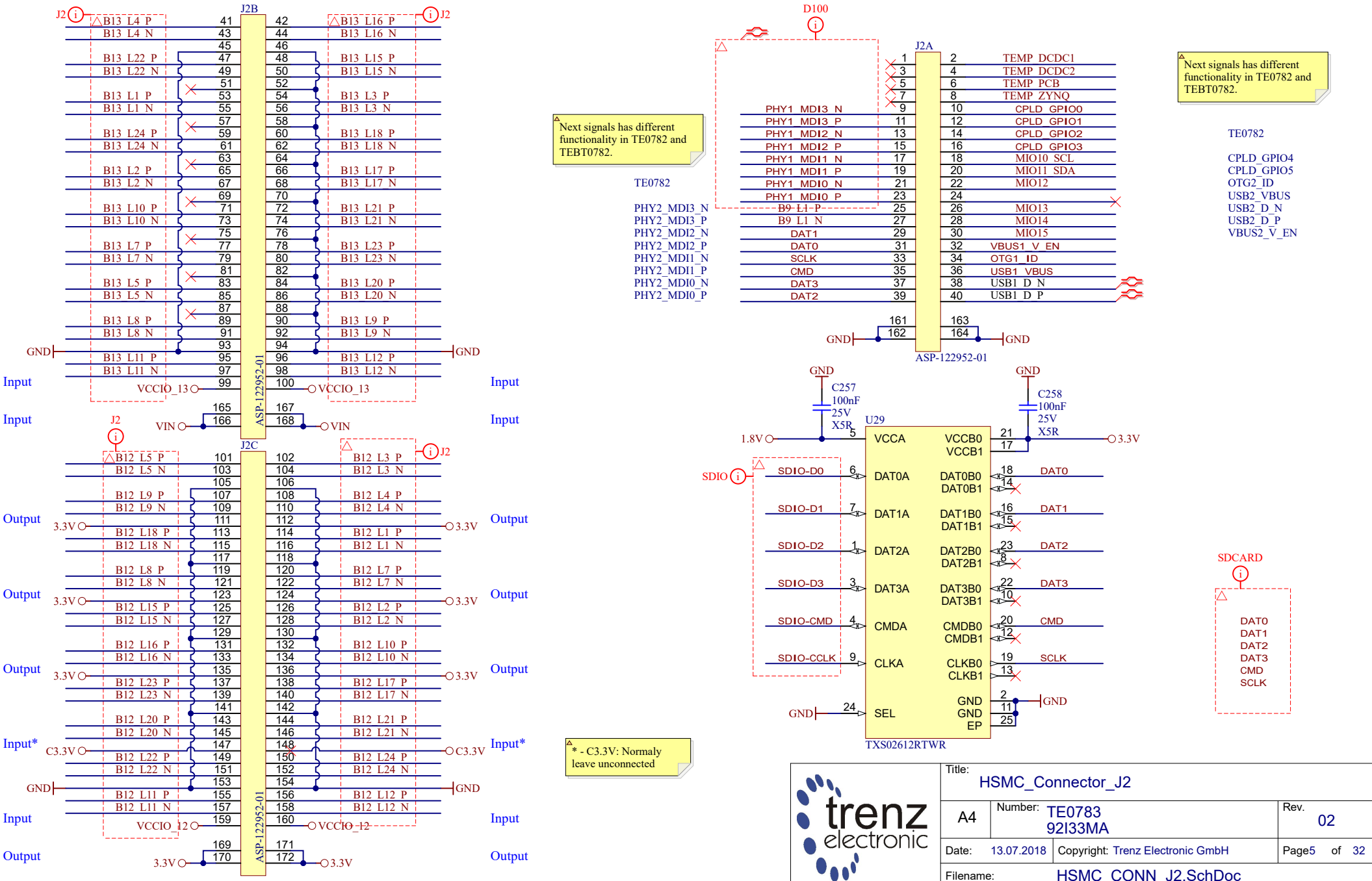
Title: HSMC_Connector_J3
A4
Number: TE0783 92I33MA
Rev. 02
Date: 13.07.2018
Copyright: Trenz Electronic GmbH
Page4 of 32
Filename: HSMC_CONN_J3.SchDoc


J2B
J2C
ASP-122952-01
B13_L4_P
B13_L4_N
B13_L22_P
B13_L22_N
B13_L1_P
B13_L1_N
B13_L24_P
B13_L24_N
B13_L2_P
B13_L2_N
B13_L10_P
B13_L10_N
B13_L7_P
B13_L7_N
B13_L5_P
B13_L5_N
B13_L8_P
B13_L8_N
B13_L11_P
B13_L11_N
B13_L16_P
B13_L16_N
B13_L15_P
B13_L15_N
B13_L3_P
B13_L3_N
B13_L18_P
B13_L18_N
B13_L17_P
B13_L17_N
B13_L21_P
B13_L21_N
B13_L23_P
B13_L23_N
B13_L20_P
B13_L20_N
B13_L9_P
B13_L9_N
B13_L12_P
B13_L12_N
B12_L5_P
B12_L5_N
B12_L9_P
B12_L9_N
B12_L18_P
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B12_L8_P
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B12_L16_P
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B12_L23_P
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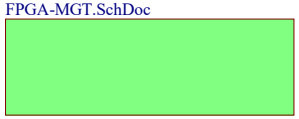
B12_L20_N
B12_L22_P
B12_L22_N
B12_L11_P
B12_L11_N
B12_L3_P
B12_L3_N
B12_L4_P
B12_L4_N
B12_L1_P
B12_L1_N
B12_L7_P
B12_L7_N
B12_L2_P
B12_L2_N
B12_L10_P
B12_L10_N
B12_L17_P
B12_L17_N
B12_L21_P
B12_L21_N
B12_L24_P
B12_L24_N
B12_L12_P
B12_L12_N
GND
VCCIO_13
VCCIO_12
VIN
3.3V
C3.3V
Input
Output
Input*
J2
Next signals has different functionality in TE0782 and TEBT0782.
TE0782
PHY2_MDI3_N
PHY2_MDI3_P
PHY2_MDI2_N
PHY2_MDI2_P
PHY2_MDI1_N
PHY2_MDI1_P
PHY2_MDI0_N
PHY2_MDI0_P
D100
J2A
PHY1_MDI3_N
PHY1_MDI3_P
PHY1_MDI2_N
PHY1_MDI2_P
PHY1_MDI1_N
PHY1_MDI1_P
PHY1_MDI0_N
PHY1_MDI0_P
B9_L1_P
B9_L1_N
DAT1
DAT0
SCLK
CMD
DAT3
DAT2
TEMP_DCDC1
TEMP_DCDC2
TEMP_PCB
TEMP_ZYNQ
CPLD_GPIO0
CPLD_GPIO1
CPLD_GPIO2
CPLD_GPIO3
MIO10_SCL
MIO11_SDA
MIO12
MIO13
MIO14
MIO15
VBUS1_V_EN
OTG1_ID
USB1_VBUS
USB1_D_N
USB1_D_P
Next signals has different functionality in TE0782 and TEBT0782.
TE0782
CPLD_GPIO4
CPLD_GPIO5
OTG2_ID
USB2_VBUS
USB2_D_N
USB2_D_P
VBUS2_V_EN
C257
100nF
25V
X5R
C258
100nF
25V
X5R
1.8V
U29
VCCA
VCCB0
VCCB1
DAT0A
DAT0B0
DAT0B1
DAT1A
DAT1B0
DAT1B1
DAT2A
DAT2B0
DAT2B1
DAT3A
DAT3B0
DAT3B1
CMDA
CMDB0
CMDB1
CLKA
CLKB0
CLKB1
SEL
GND
EP
SDIO-D0
SDIO-D1
SDIO-D2
SDIO-D3
SDIO-CMD
SDIO-CCLK
SDIO
DAT0
DAT1
DAT2
DAT3
CMD
SCLK
TXS02612RTWR
SDCARD
* - C3.3V: Normaly leave unconnected
trenz electronic
Title: HSMC_Connector_J2
A4
Number: TE0783 92I33MA
Rev. 02
Date: 13.07.2018
Copyright: Trenz Electronic GmbH
Page5 of 32
Filename: HSMC_CONN_J2.SchDoc

U_PS-DDR
PS-DDR.SchDoc

U_MIO-BANKS
MIO-BANKS.SchDoc

U_HP-BANKS
HP-BANKS.SchDoc

U_FPGA-MGT
FPGA-MGT.SchDoc



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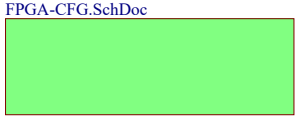
FPGA-CFG.SchDoc



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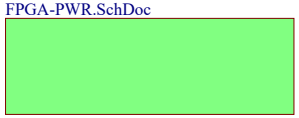
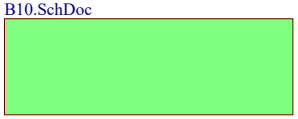
FPGA-PWR.SchDoc



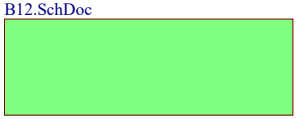
U_B9
B9.SchDoc

U_B10
B10.SchDoc



U_B11
B11.SchDoc

U_B12
B12.SchDoc



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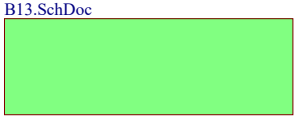
B13.SchDoc



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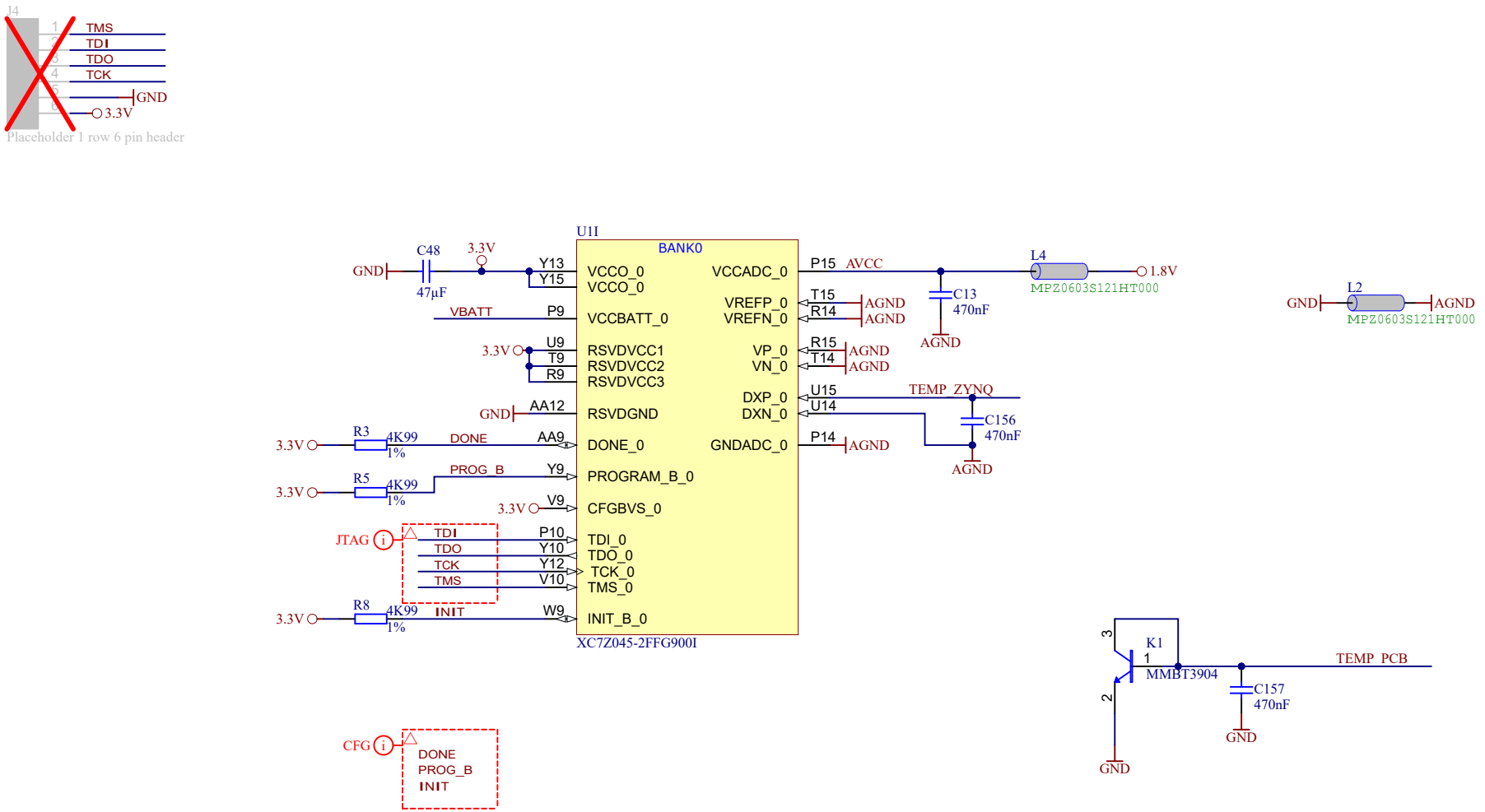
A4	Number: TE0783 92I33MA		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page6 of 32
Filename: SOC.SchDoc			



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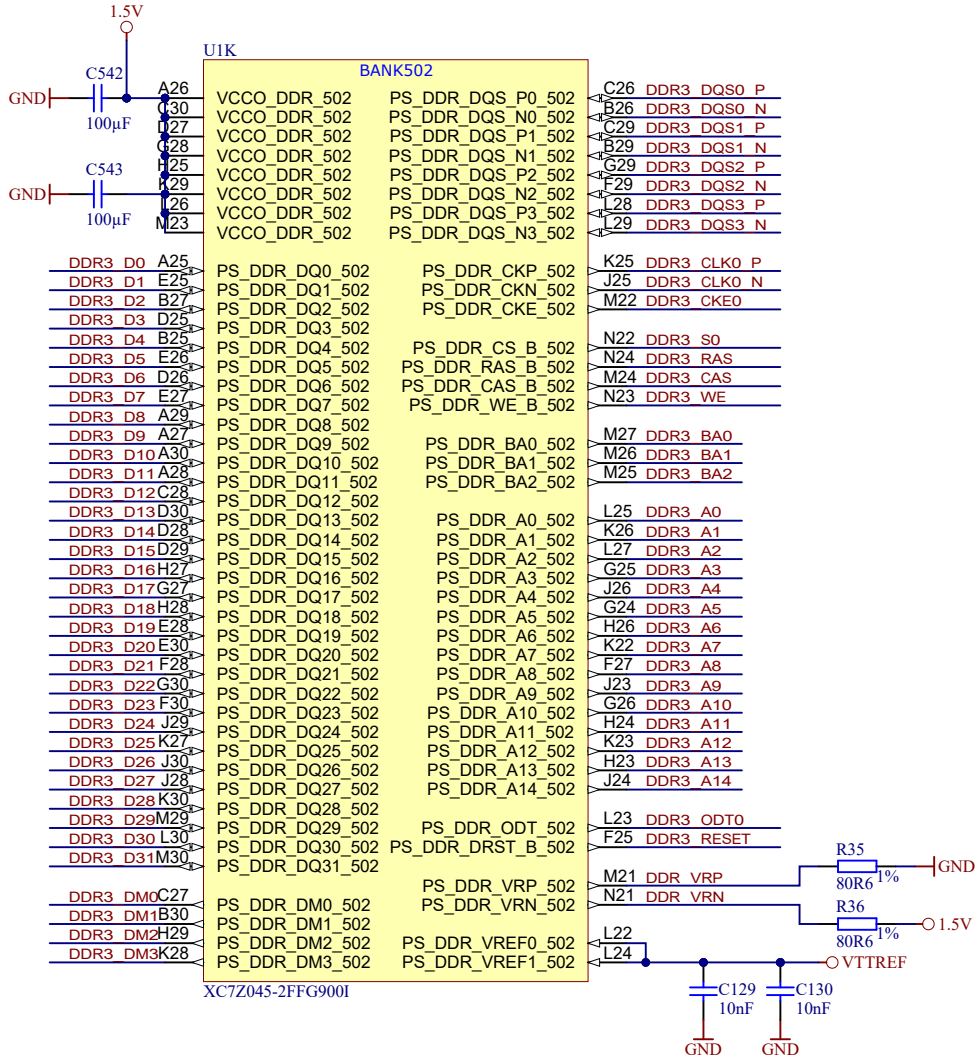
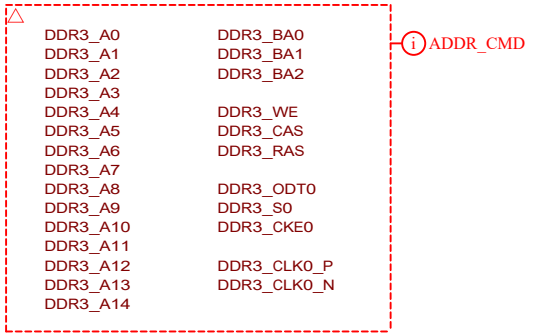
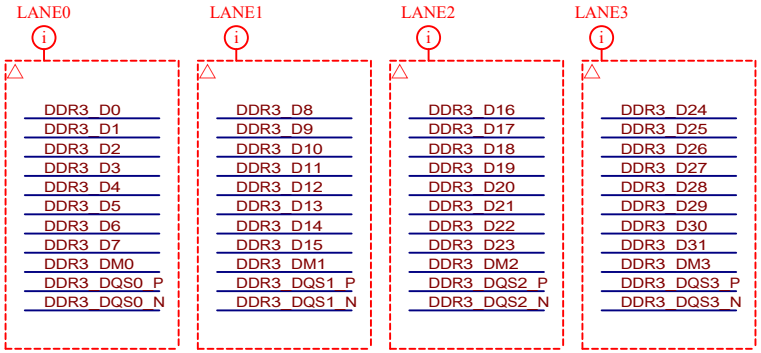
Datum: 13.07.2018	Zeichner: Trenz Electronic GmbH		Blatt 7 von 32
Filename: FPGA-CFG.SchDoc			







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Title: FPGA DDR Banks			
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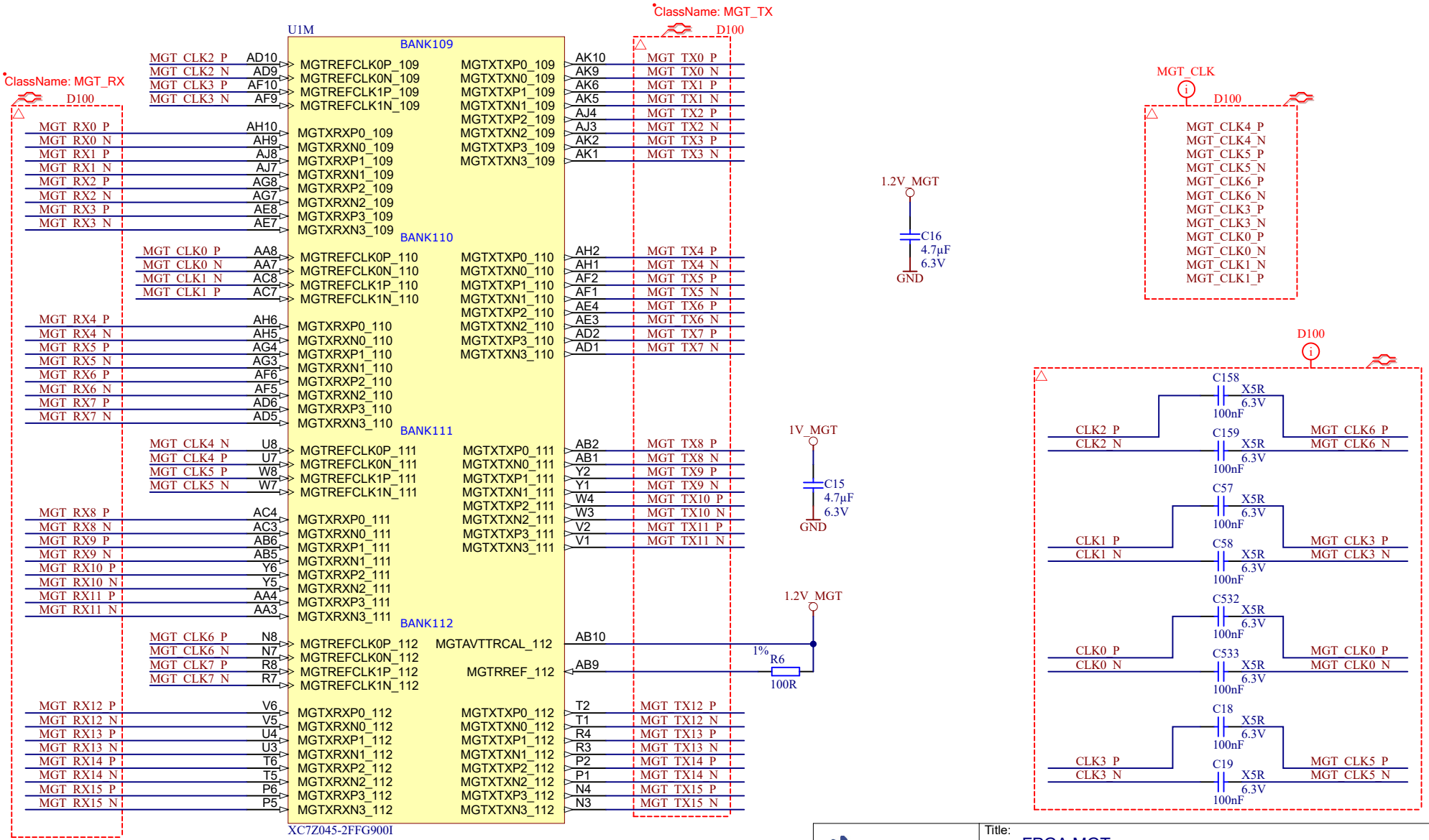
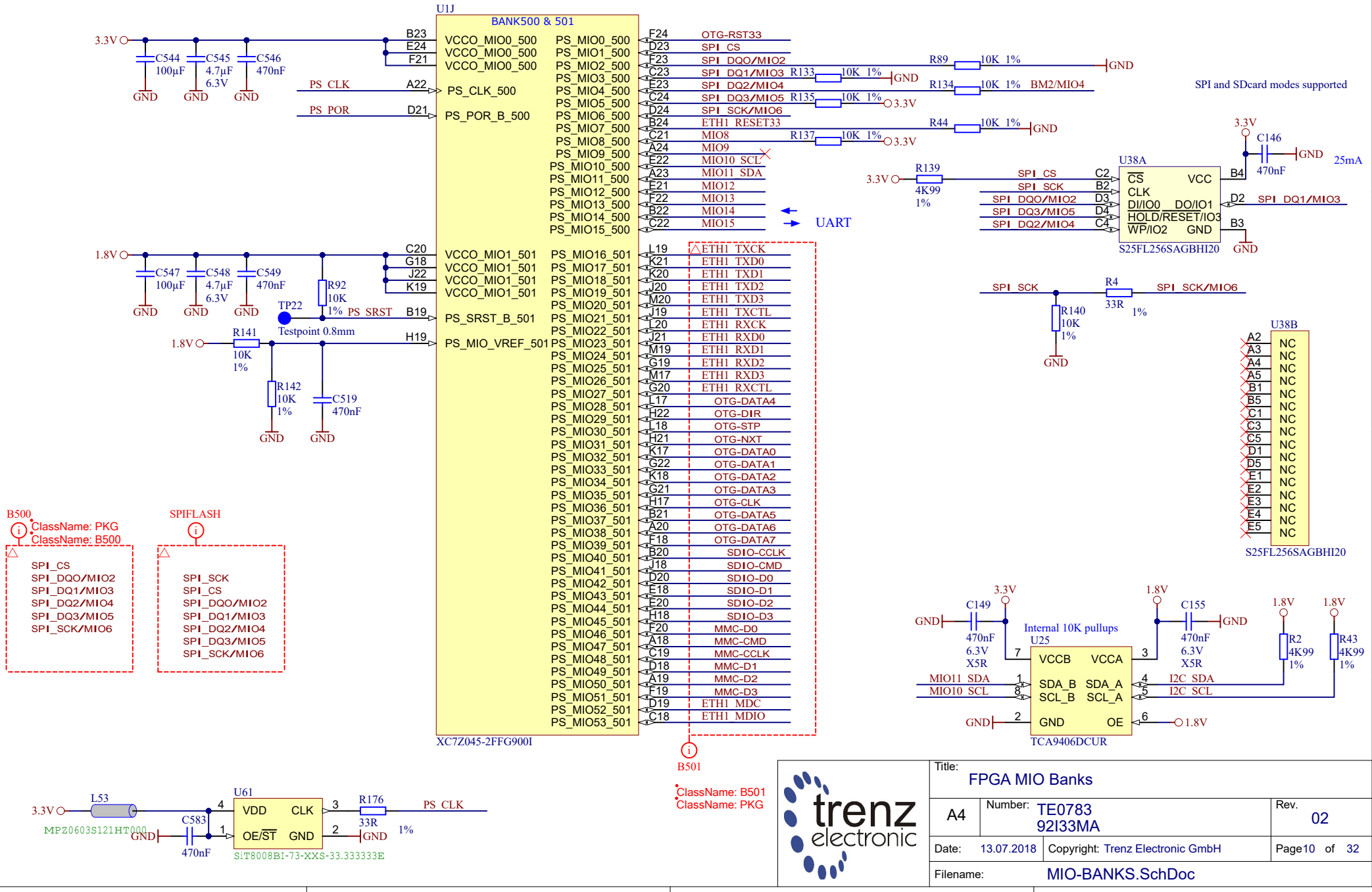
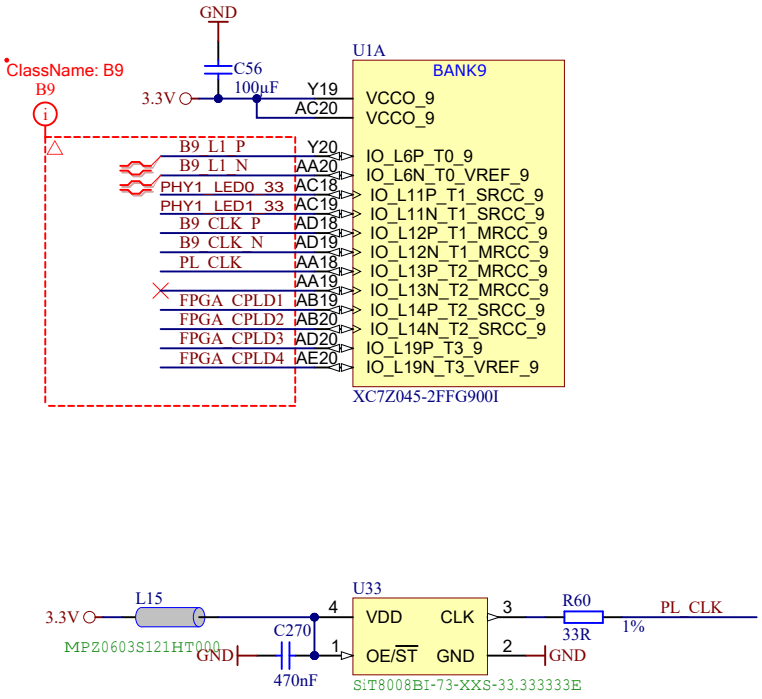
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page8 of 32
Filename: PS-DDR.SchDoc			



trenz electronic	Title: FPGA MGT		
A4	Number: TE0783 92I33MA		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page9 of 32
Filename: FPGA-MGT.SchDoc			


U1J
BANK500 & 501
XC7Z045-2FFG900I
PS_CLK
PS_POR
PS_SRST_B_501
PS_MIO_VREF_501
TP22
Testpoint 0.8mm
SPI and SDcard modes supported
UART
U38A
S25FL256SAGBHI20
U38B
B500
ClassName: PKG
ClassName: B500
SPI_CS
SPI_DQO/MIO2
SPI_DQ1/MIO3
SPI_DQ2/MIO4
SPI_DQ3/MIO5
SPI_SCK/MIO6
SPIFLASH
SPI_SCK
SPI_CS
SPI_DQO/MIO2
SPI_DQ1/MIO3
SPI_DQ2/MIO4
SPI_DQ3/MIO5
SPI_SCK/MIO6
B501
ClassName: B501
ClassName: PKG
Internal 10K pullups
U25
TCA9406DCUR
L53
MPZ0603S121HT000
U61
SiT8008BI-73-XXS-33.333333E
Title: FPGA MIO Banks
A4
Number: TE0783 92I33MA
Rev. 02
Date: 13.07.2018
Copyright: Trenz Electronic GmbH
Page10 of 32
Filename: MIO-BANKS.SchDoc



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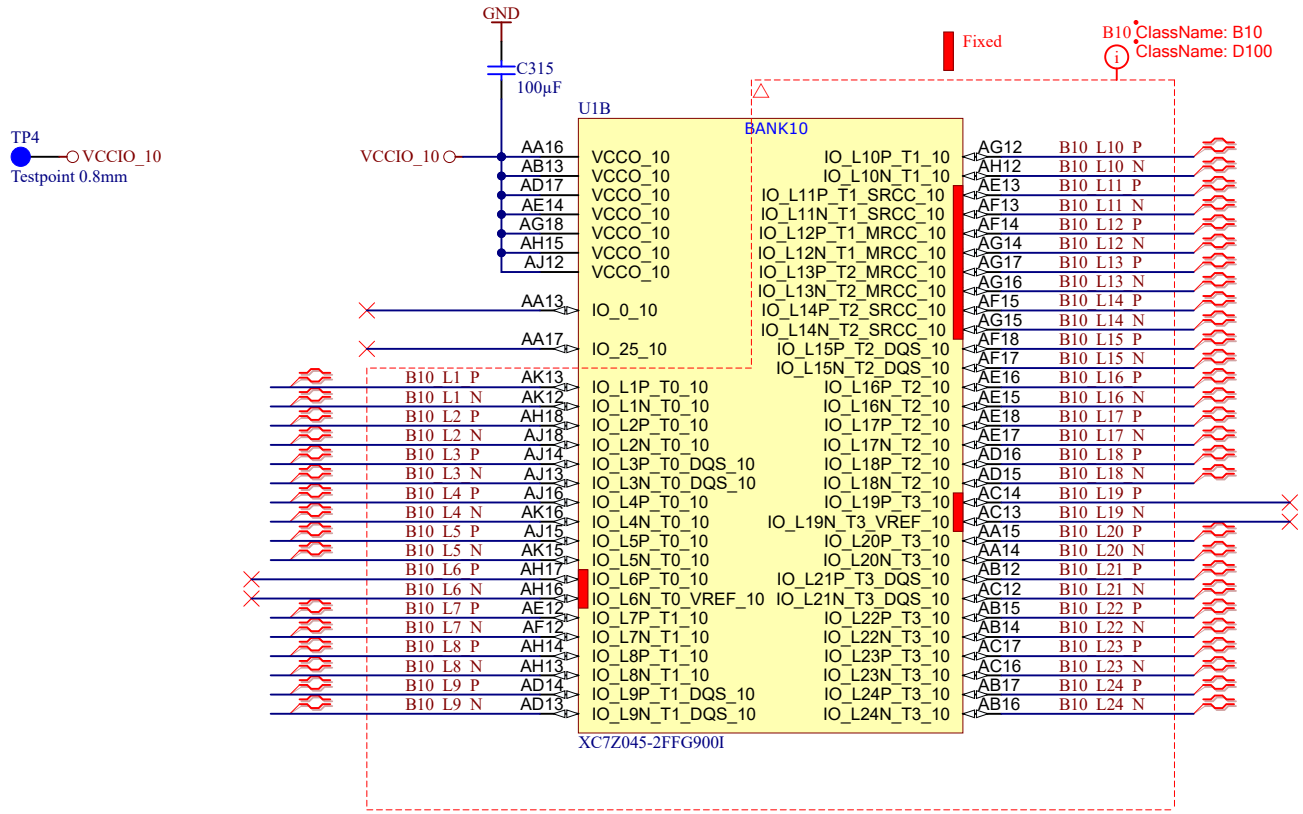
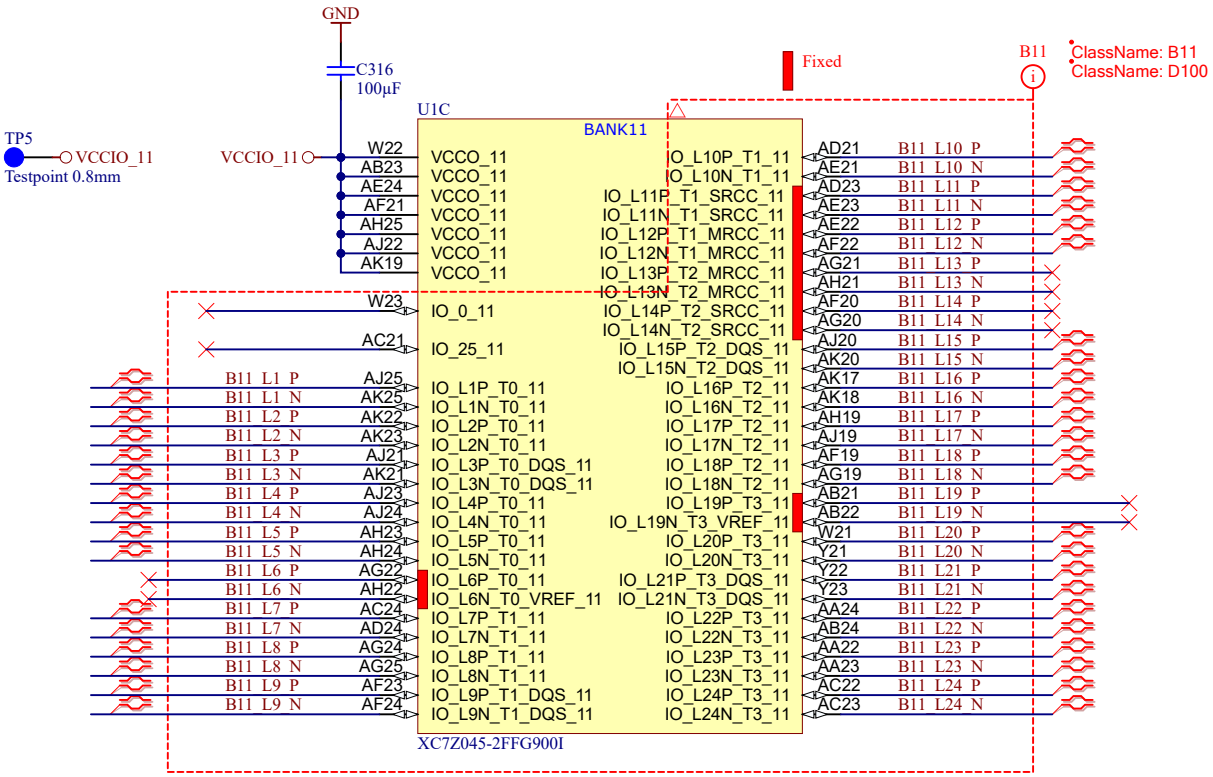
Title: FPGA B9		
A4	Number: TE0783 92I33MA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 11 of 32
Filename: B9.SchDoc		



trenz electronic	Title: FPGA B10		
	A4	Number: TE0783 92I33MA	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 12 of 32
	Filename: B10.SchDoc		



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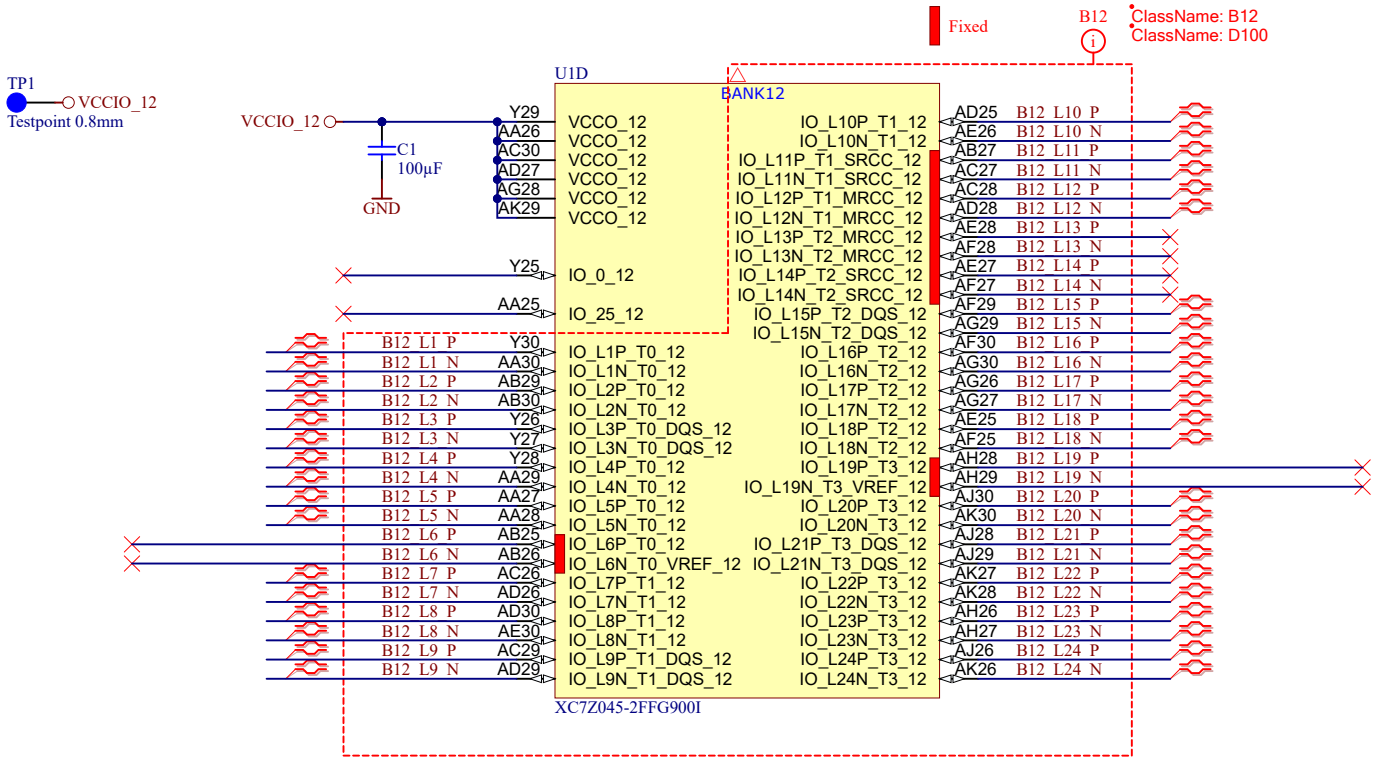
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page 13 of 32
Filename: B11.SchDoc			



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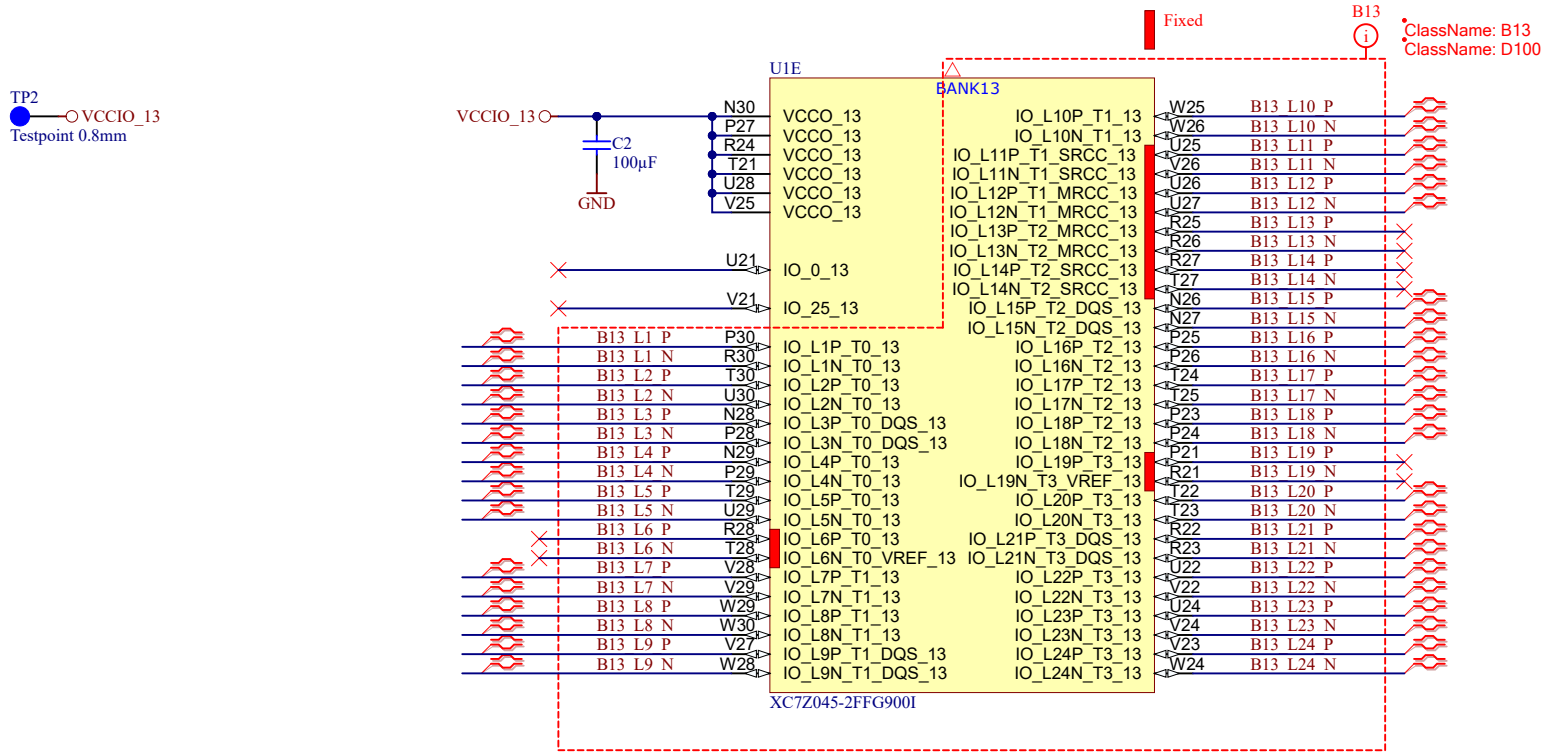
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page 14 of 32
Filename: B12.SchDoc			



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Title: FPGA B13		
A4	Number: TE0783 92I33MA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 15 of 32
Filename: B13.SchDoc		

U_B33
B33.SchDoc

U_B34
B34.SchDoc

U_B35
B35.SchDoc

U_DDR3-RAM-PL1
DDR3-RAM-PL1.SchDoc

U_DDR3-RAM-PL2
DDR3-RAM-PL2.SchDoc

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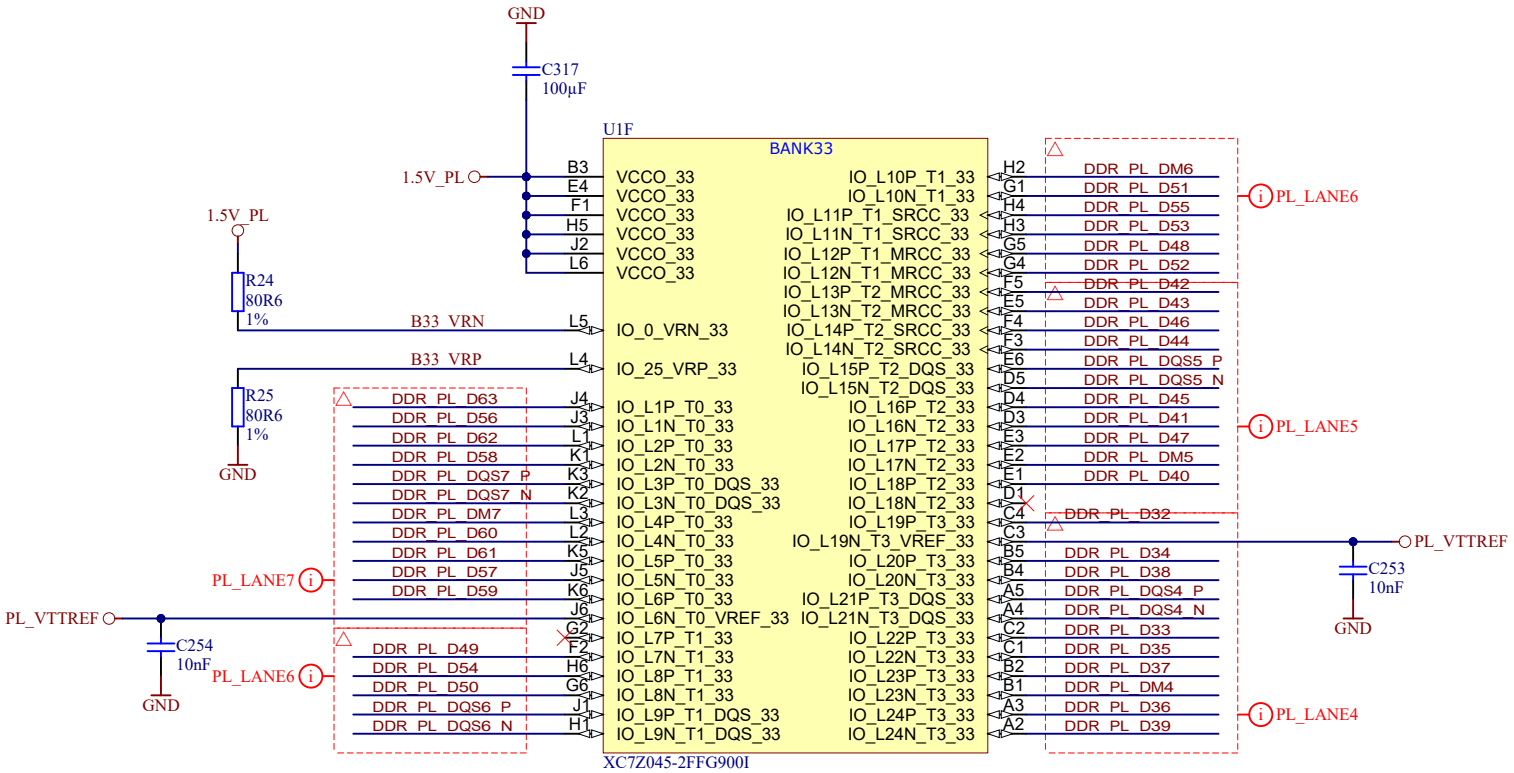
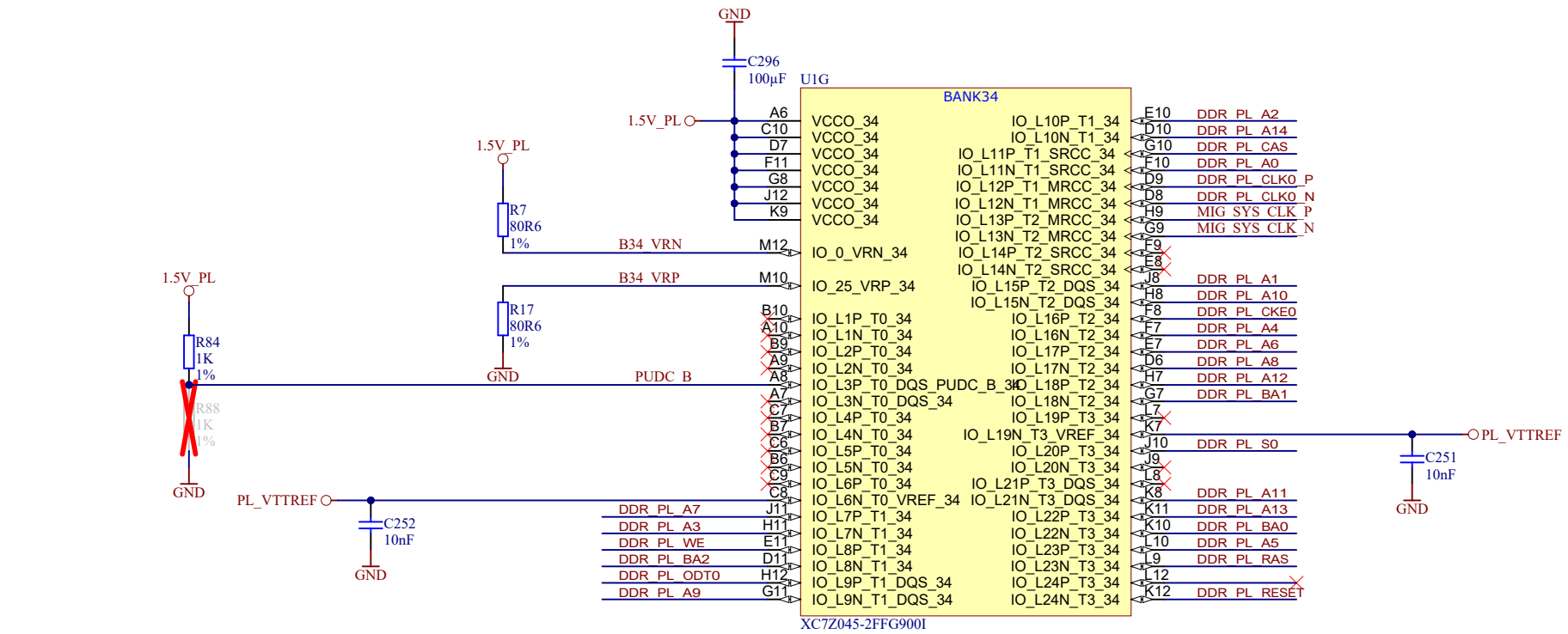
Title: FPGA HP Banks		
A4	Number: TE0783 92I33MA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 16 of 32
Filename: HP-BANKS.SchDoc		



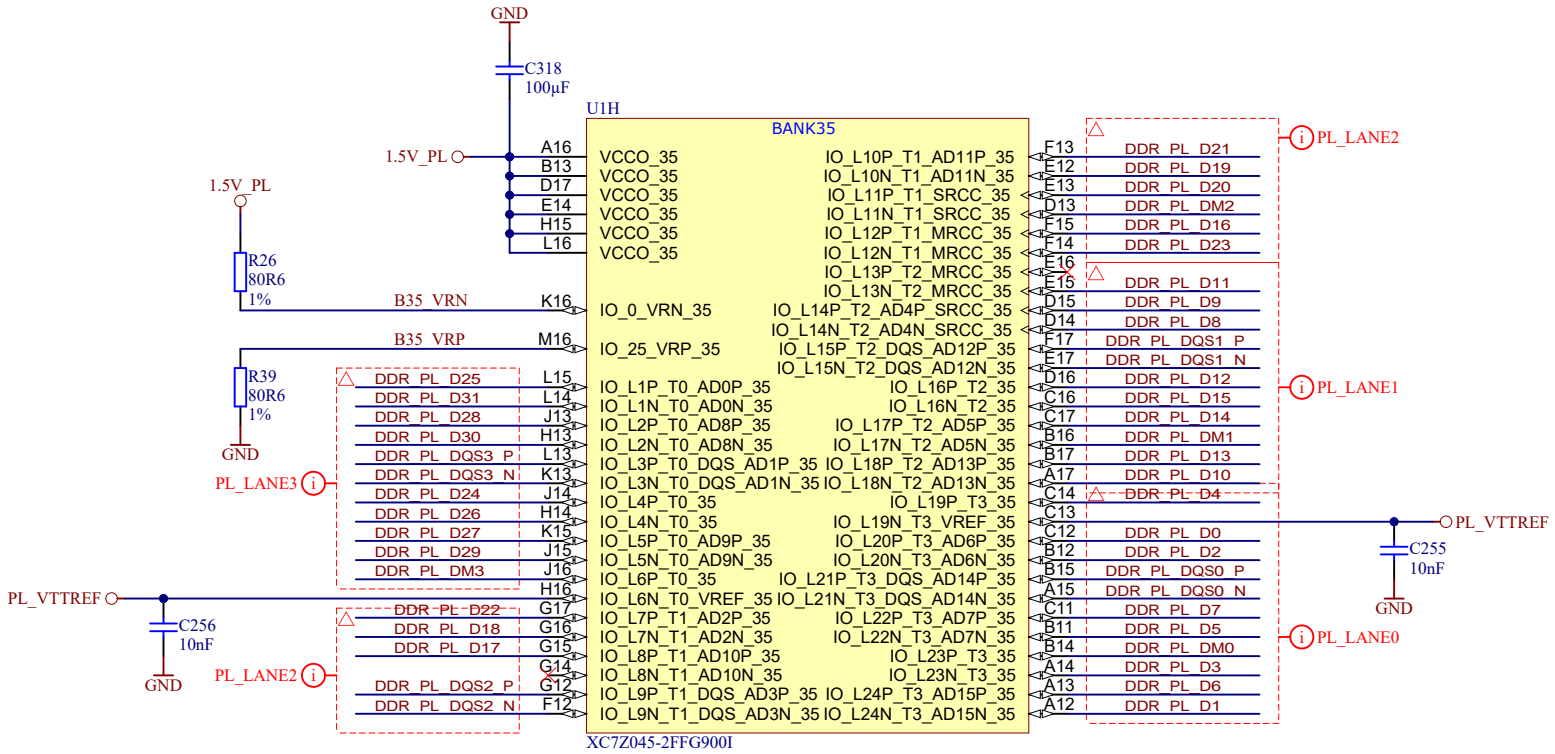
trenz electronic	Title: FPGA B33		
A4	Number: TE0783 92I33MA		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page 17 of 32
Filename: B33.SchDoc			



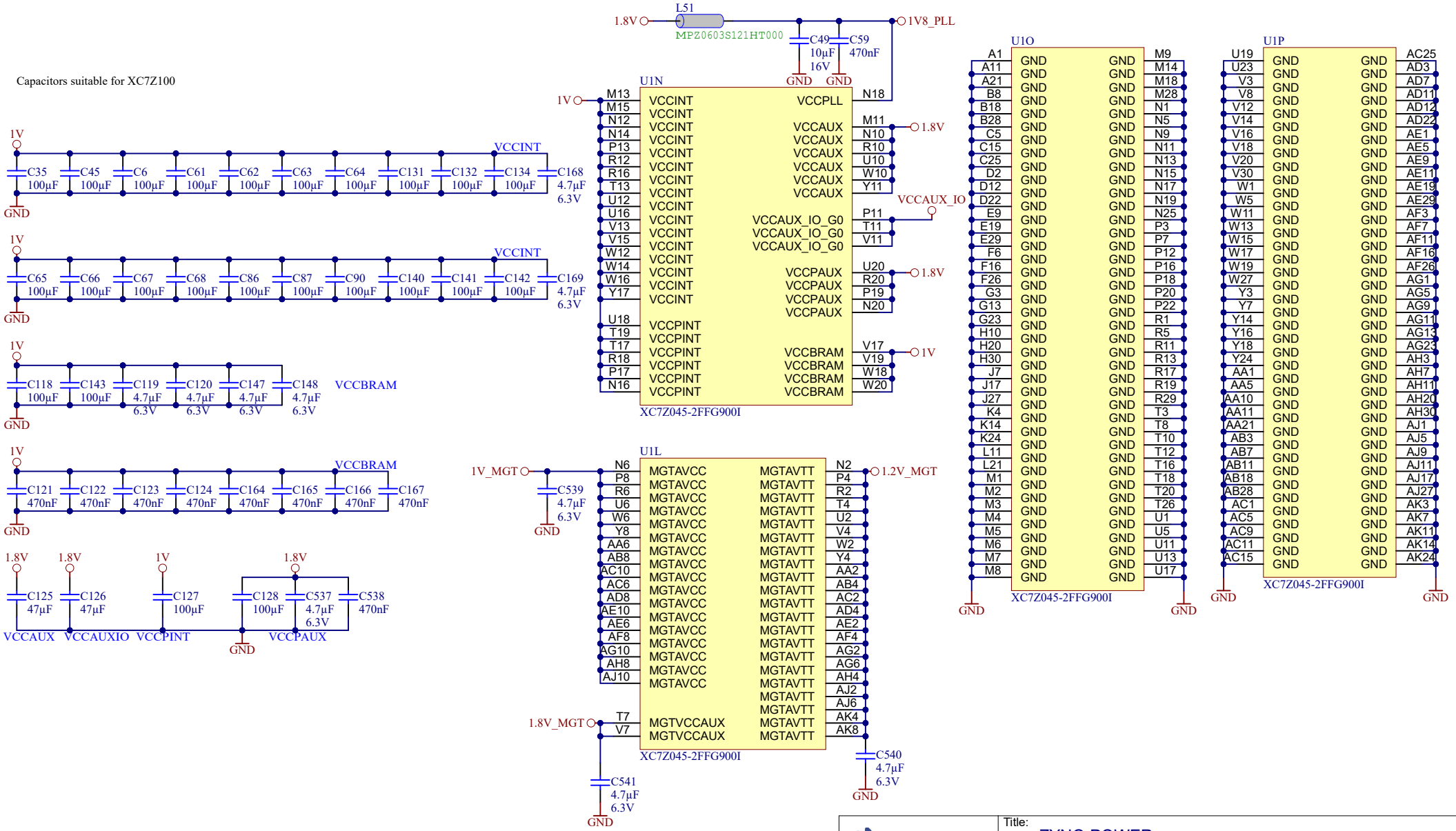
Check clock source. R74 100R changed to 100K

trenz electronic

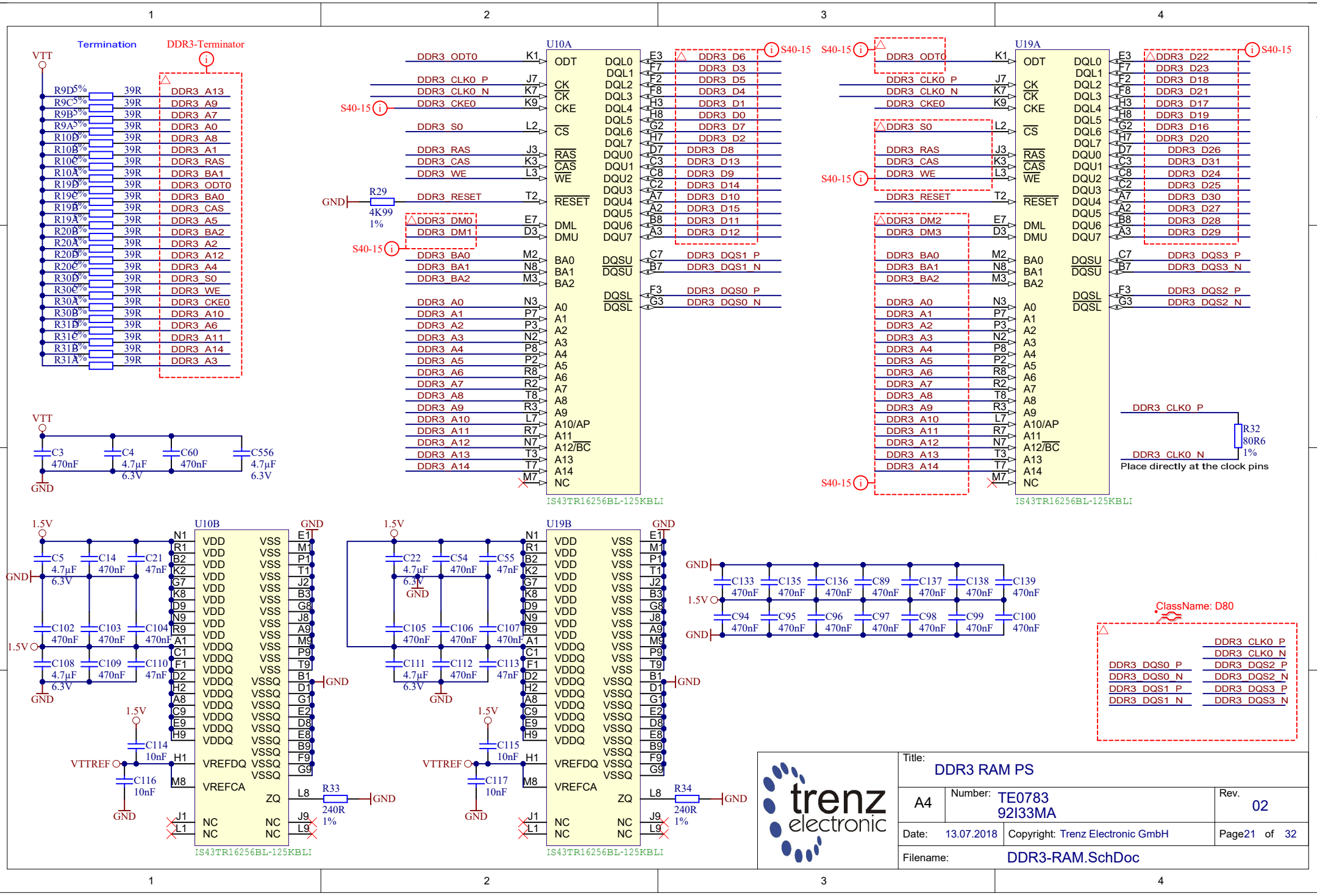
Title: FPGA B34			
A4	Number: TE0783 92I33MA		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page 18 of 32
Filename: B34.SchDoc			

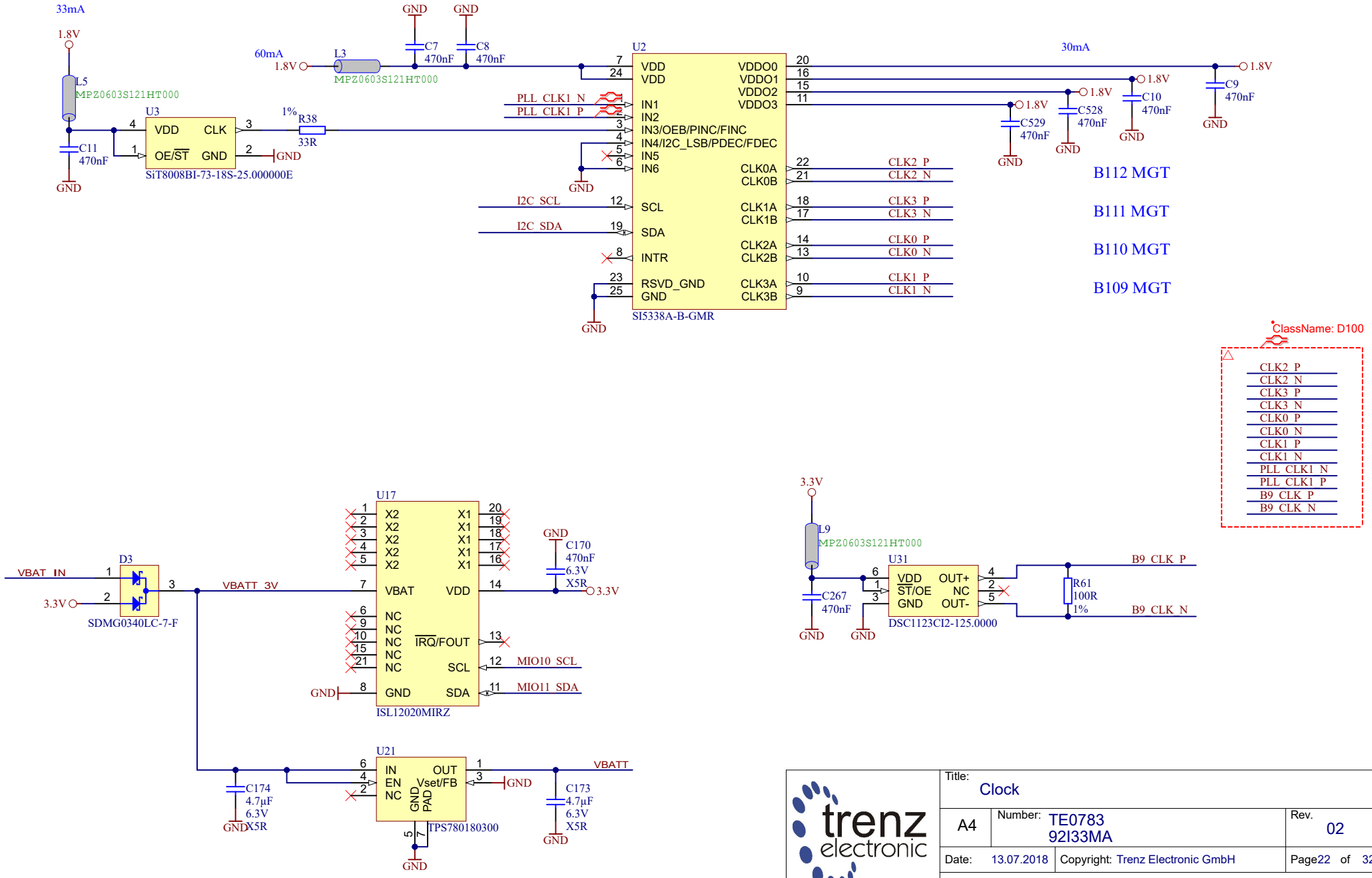


trenz electronic	Title: FPGA B35		
	A4	Number: TE0783 92I33MA	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 19 of 32
	Filename: B35.SchDoc		

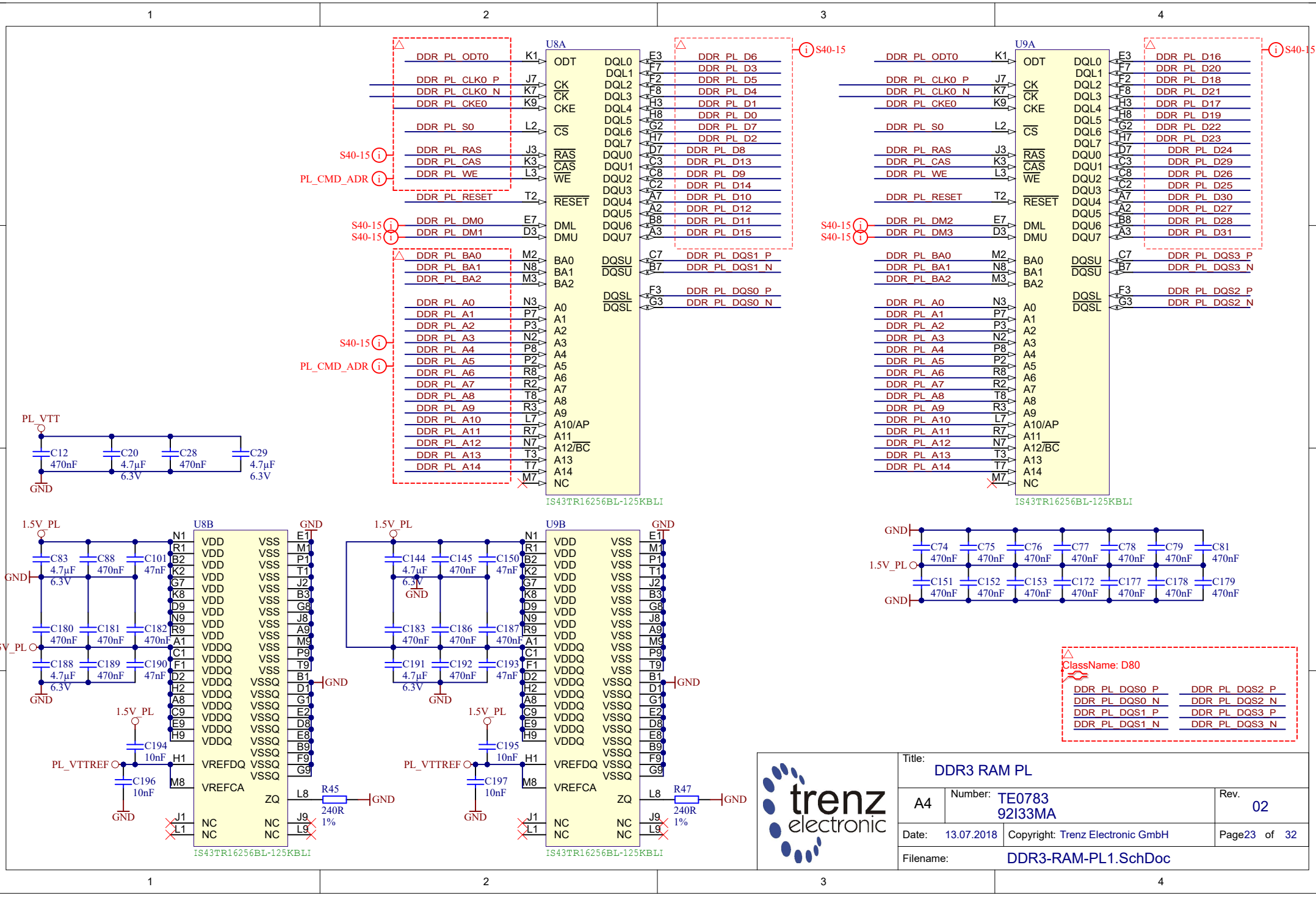


Title: ZYNQ POWER			
A4	Number: TE0783 92I33MA		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page20 of 32
Filename: FPGA-PWR.SchDoc			


Termination
DDR3-Terminator
VTT
R9D 5% 39R DDR3_A13
R9C 5% 39R DDR3_A9
R9B 5% 39R DDR3_A7
R9A 5% 39R DDR3_A0
R10D 5% 39R DDR3_A8
R10B 5% 39R DDR3_A1
R10C 5% 39R DDR3_RAS
R10A 5% 39R DDR3_BA1
R19D 5% 39R DDR3_ODT0
R19C 5% 39R DDR3_BA0
R19B 5% 39R DDR3_CAS
R19A 5% 39R DDR3_A5
R20B 5% 39R DDR3_BA2
R20A 5% 39R DDR3_A2
R20D 5% 39R DDR3_A12
R20C 5% 39R DDR3_A4
R30D 5% 39R DDR3_S0
R30C 5% 39R DDR3_WE
R30A 5% 39R DDR3_CKE0
R30B 5% 39R DDR3_A10
R31D 5% 39R DDR3_A6
R31C 5% 39R DDR3_A11
R31B 5% 39R DDR3_A14
R31A 5% 39R DDR3_A3
VTT
C3 470nF
C4 4.7µF 6.3V
C60 470nF
C556 4.7µF 6.3V
GND
U10A
DDR3_ODT0 K1 ODT
DDR3_CLK0_P J7 CK
DDR3_CLK0_N K7 CK
DDR3_CKE0 K9 CKE
S40-15
DDR3_S0 L2 CS
DDR3_RAS J3 RAS
DDR3_CAS K3 CAS
DDR3_WE L3 WE
GND R29 4K99 1%
DDR3_RESET T2 RESET
DDR3_DM0 E7 DML
DDR3_DM1 D3 DMU
S40-15
DDR3_BA0 M2 BA0
DDR3_BA1 N8 BA1
DDR3_BA2 M3 BA2
DDR3_A0 N3 A0
DDR3_A1 P7 A1
DDR3_A2 P3 A2
DDR3_A3 N2 A3
DDR3_A4 P8 A4
DDR3_A5 P2 A5
DDR3_A6 R8 A6
DDR3_A7 R2 A7
DDR3_A8 T8 A8
DDR3_A9 R3 A9
DDR3_A10 L7 A10/AP
DDR3_A11 R7 A11
DDR3_A12 N7 A12/BC
DDR3_A13 T3 A13
DDR3_A14 T7 A14
M7 NC
DQL0 DQL1 DQL2 DQL3 DQL4 DQL5 DQL6 DQL7 DQU0 DQU1 DQU2 DQU3 DQU4 DQU5 DQU6 DQU7
DQSU DQSU
DQSL DQSL
E3 DDR3_D6
F7 DDR3_D3
F2 DDR3_D5
F8 DDR3_D4
H3 DDR3_D1
H8 DDR3_D0
G2 DDR3_D7
H7 DDR3_D2
D7 DDR3_D8
C3 DDR3_D13
C8 DDR3_D9
C2 DDR3_D14
A7 DDR3_D10
A2 DDR3_D15
B8 DDR3_D11
A3 DDR3_D12
C7 DDR3_DQS1_P
B7 DDR3_DQS1_N
F3 DDR3_DQS0_P
G3 DDR3_DQS0_N
S40-15
IS43TR16256BL-125KBLI
U19A
S40-15
DDR3_ODT0 K1 ODT
DDR3_CLK0_P J7 CK
DDR3_CLK0_N K7 CK
DDR3_CKE0 K9 CKE
DDR3_S0 L2 CS
DDR3_RAS J3 RAS
DDR3_CAS K3 CAS
DDR3_WE L3 WE
S40-15
DDR3_RESET T2 RESET
DDR3_DM2 E7 DML
DDR3_DM3 D3 DMU
DDR3_BA0 M2 BA0
DDR3_BA1 N8 BA1
DDR3_BA2 M3 BA2
DDR3_A0 N3 A0
DDR3_A1 P7 A1
DDR3_A2 P3 A2
DDR3_A3 N2 A3
DDR3_A4 P8 A4
DDR3_A5 P2 A5
DDR3_A6 R8 A6
DDR3_A7 R2 A7
DDR3_A8 T8 A8
DDR3_A9 R3 A9
DDR3_A10 L7 A10/AP
DDR3_A11 R7 A11
DDR3_A12 N7 A12/BC
DDR3_A13 T3 A13
DDR3_A14 T7 A14
M7 NC
S40-15
DQL0 DQL1 DQL2 DQL3 DQL4 DQL5 DQL6 DQL7 DQU0 DQU1 DQU2 DQU3 DQU4 DQU5 DQU6 DQU7
DQSU DQSU
DQSL DQSL
E3 DDR3_D22
F7 DDR3_D23
F2 DDR3_D18
F8 DDR3_D21
H3 DDR3_D17
H8 DDR3_D19
G2 DDR3_D16
H7 DDR3_D20
D7 DDR3_D26
C3 DDR3_D31
C8 DDR3_D24
C2 DDR3_D25
A7 DDR3_D30
A2 DDR3_D27
B8 DDR3_D28
A3 DDR3_D29
C7 DDR3_DQS3_P
B7 DDR3_DQS3_N
F3 DDR3_DQS2_P
G3 DDR3_DQS2_N
S40-15
IS43TR16256BL-125KBLI
DDR3_CLK0_P
R32 80R6 1%
DDR3_CLK0_N
Place directly at the clock pins
1.5V
GND
U10B
C5 4.7µF 6.3V
C14 470nF
C21 47nF
C102 470nF
C103 470nF
C104 470nF
C108 4.7µF 6.3V
C109 470nF
C110 47nF
C114 10nF
C116 10nF
VTTREF
VDD VSS
VDDQ VSSQ
VREFDQ
VREFCA
ZQ
NC NC
R33 240R 1%
IS43TR16256BL-125KBLI
U19B
C22 4.7µF 6.3V
C54 470nF
C55 47nF
C105 470nF
C106 470nF
C107 470nF
C111 4.7µF 6.3V
C112 470nF
C113 47nF
C115 10nF
C117 10nF
R34 240R 1%
IS43TR16256BL-125KBLI
C133 470nF
C135 470nF
C136 470nF
C89 470nF
C137 470nF
C138 470nF
C139 470nF
C94 470nF
C95 470nF
C96 470nF
C97 470nF
C98 470nF
C99 470nF
C100 470nF
ClassName: D80
DDR3_DQS0_P
DDR3_DQS0_N
DDR3_DQS1_P
DDR3_DQS1_N
DDR3_CLK0_P
DDR3_CLK0_N
DDR3_DQS2_P
DDR3_DQS2_N
DDR3_DQS3_P
DDR3_DQS3_N
trenz electronic
Title: DDR3 RAM PS
A4
Number: TE0783 92I33MA
Rev. 02
Date: 13.07.2018
Copyright: Trenz Electronic GmbH
Page21 of 32
Filename: DDR3-RAM.SchDoc



Title: Clock			
A4	Number: TE0783 92I33MA		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page22 of 32
Filename: Clock.SchDoc			


U8A
U9A
U8B
U9B
IS43TR16256BL-125KBLI
DDR_PL_ODT0
DDR_PL_CLK0_P
DDR_PL_CLK0_N
DDR_PL_CKE0
DDR_PL_S0
DDR_PL_RAS
DDR_PL_CAS
DDR_PL_WE
DDR_PL_RESET
DDR_PL_DM0
DDR_PL_DM1
DDR_PL_DM2
DDR_PL_DM3
DDR_PL_BA0
DDR_PL_BA1
DDR_PL_BA2
DDR_PL_A0
DDR_PL_A1
DDR_PL_A2
DDR_PL_A3
DDR_PL_A4
DDR_PL_A5
DDR_PL_A6
DDR_PL_A7
DDR_PL_A8
DDR_PL_A9
DDR_PL_A10
DDR_PL_A11
DDR_PL_A12
DDR_PL_A13
DDR_PL_A14
S40-15
PL_CMD_ADR
PL_VTT
GND
1.5V_PL
PL_VTTREF
R45
R47
240R
1%
ClassName: D80
DDR_PL_DQS0_P
DDR_PL_DQS0_N
DDR_PL_DQS1_P
DDR_PL_DQS1_N
DDR_PL_DQS2_P
DDR_PL_DQS2_N
DDR_PL_DQS3_P
DDR_PL_DQS3_N
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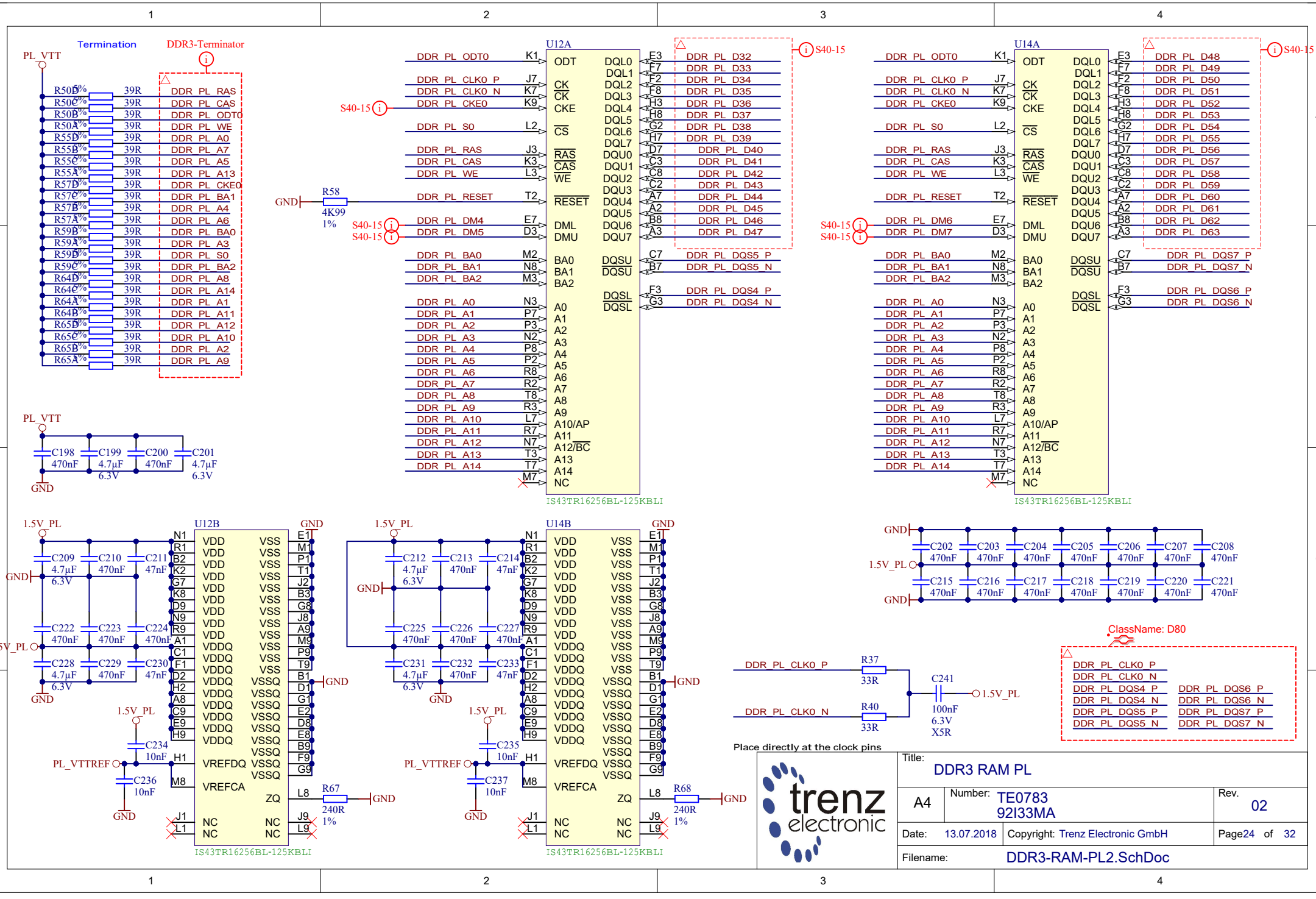
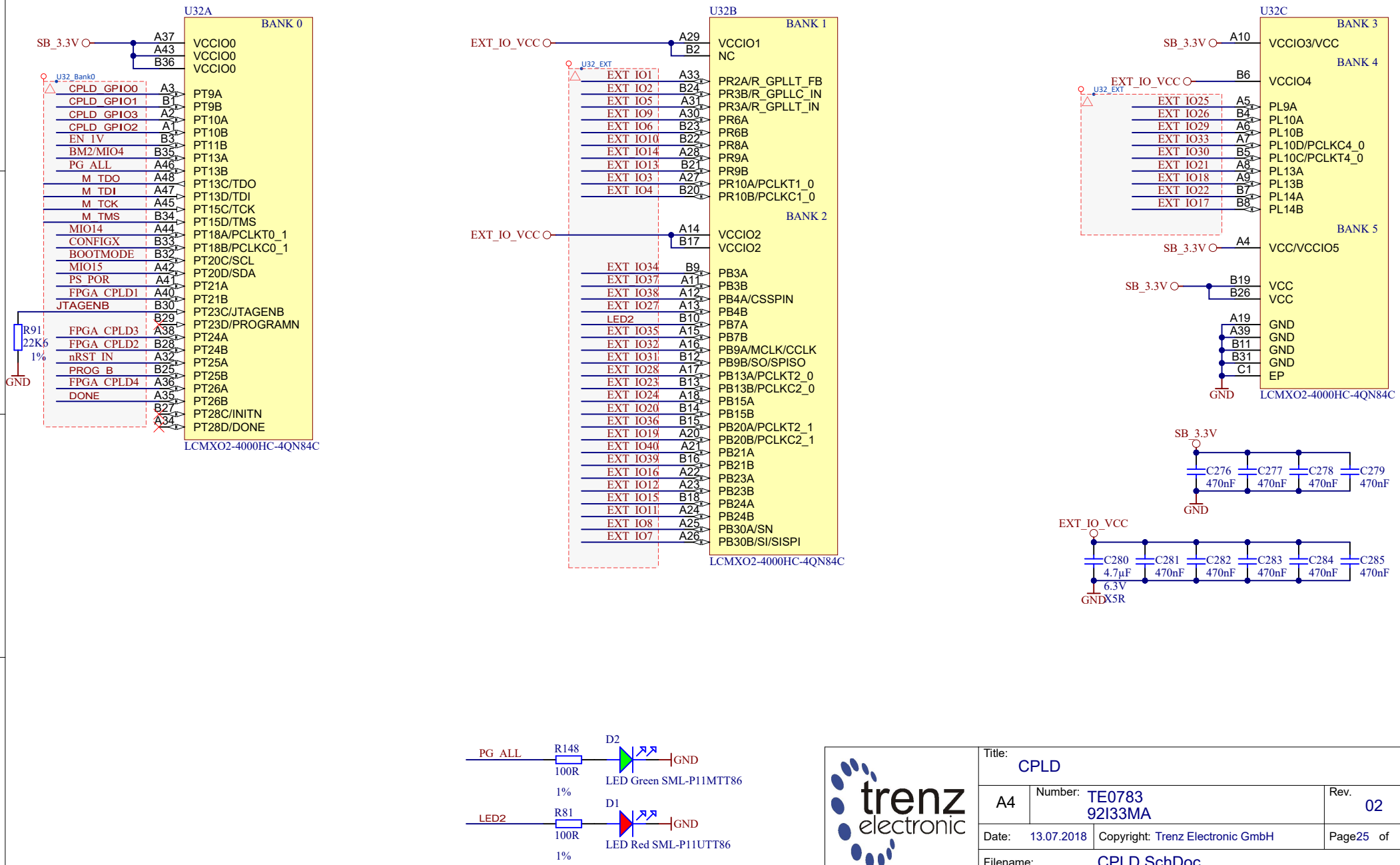
Title: DDR3 RAM PL
A4
Number: TE0783 92I33MA
Rev. 02
Date: 13.07.2018
Copyright: Trenz Electronic GmbH
Page23 of 32
Filename: DDR3-RAM-PL1.SchDoc


Termination
DDR3-Terminator
PL_VTT
R50D 39R DDR_PL_RAS
R50C 39R DDR_PL_CAS
R50B 39R DDR_PL_ODT0
R50A 39R DDR_PL_WE
R55D 39R DDR_PL_A0
R55B 39R DDR_PL_A7
R55C 39R DDR_PL_A5
R55A 39R DDR_PL_A13
R57D 39R DDR_PL_CKE0
R57C 39R DDR_PL_BA1
R57B 39R DDR_PL_A4
R57A 39R DDR_PL_A6
R59B 39R DDR_PL_BA0
R59A 39R DDR_PL_A3
R59D 39R DDR_PL_S0
R59C 39R DDR_PL_BA2
R64D 39R DDR_PL_A8
R64C 39R DDR_PL_A14
R64A 39R DDR_PL_A1
R64B 39R DDR_PL_A11
R65D 39R DDR_PL_A12
R65C 39R DDR_PL_A10
R65B 39R DDR_PL_A2
R65A 39R DDR_PL_A9
PL_VTT
C198 470nF
C199 4.7µF 6.3V
C200 470nF
C201 4.7µF 6.3V
GND
U12A
DDR_PL_ODT0 K1 ODT
DDR_PL_CLK0_P J7 CK
DDR_PL_CLK0_N K7 CK
DDR_PL_CKE0 K9 CKE
S40-15
DDR_PL_S0 L2 CS
DDR_PL_RAS J3 RAS
DDR_PL_CAS K3 CAS
DDR_PL_WE L3 WE
DDR_PL_RESET T2 RESET
R58 4K99 1%
GND
DDR_PL_DM4 E7 DML
DDR_PL_DM5 D3 DMU
DDR_PL_BA0 M2 BA0
DDR_PL_BA1 N8 BA1
DDR_PL_BA2 M3 BA2
DDR_PL_A0 N3 A0
DDR_PL_A1 P7 A1
DDR_PL_A2 P3 A2
DDR_PL_A3 N2 A3
DDR_PL_A4 P8 A4
DDR_PL_A5 P2 A5
DDR_PL_A6 R8 A6
DDR_PL_A7 R2 A7
DDR_PL_A8 T8 A8
DDR_PL_A9 R3 A9
DDR_PL_A10 L7 A10/AP
DDR_PL_A11 R7 A11
DDR_PL_A12 N7 A12/BC
DDR_PL_A13 T3 A13
DDR_PL_A14 T7 A14
M7 NC
DQL0 E3 DDR_PL_D32
DQL1 F7 DDR_PL_D33
DQL2 F2 DDR_PL_D34
DQL3 F8 DDR_PL_D35
DQL4 H3 DDR_PL_D36
DQL5 H8 DDR_PL_D37
DQL6 G2 DDR_PL_D38
DQL7 H7 DDR_PL_D39
DQU0 D7 DDR_PL_D40
DQU1 C3 DDR_PL_D41
DQU2 C8 DDR_PL_D42
DQU3 C2 DDR_PL_D43
DQU4 A7 DDR_PL_D44
DQU5 A2 DDR_PL_D45
DQU6 B8 DDR_PL_D46
DQU7 A3 DDR_PL_D47
DQSU C7 DDR_PL_DQS5_P
DQSU B7 DDR_PL_DQS5_N
DQSL F3 DDR_PL_DQS4_P
DQSL G3 DDR_PL_DQS4_N
S40-15
IS43TR16256BL-125KBLI
U14A
DDR_PL_ODT0 K1 ODT
DDR_PL_CLK0_P J7 CK
DDR_PL_CLK0_N K7 CK
DDR_PL_CKE0 K9 CKE
DDR_PL_S0 L2 CS
DDR_PL_RAS J3 RAS
DDR_PL_CAS K3 CAS
DDR_PL_WE L3 WE
DDR_PL_RESET T2 RESET
S40-15
DDR_PL_DM6 E7 DML
DDR_PL_DM7 D3 DMU
DDR_PL_BA0 M2 BA0
DDR_PL_BA1 N8 BA1
DDR_PL_BA2 M3 BA2
DDR_PL_A0 N3 A0
DDR_PL_A1 P7 A1
DDR_PL_A2 P3 A2
DDR_PL_A3 N2 A3
DDR_PL_A4 P8 A4
DDR_PL_A5 P2 A5
DDR_PL_A6 R8 A6
DDR_PL_A7 R2 A7
DDR_PL_A8 T8 A8
DDR_PL_A9 R3 A9
DDR_PL_A10 L7 A10/AP
DDR_PL_A11 R7 A11
DDR_PL_A12 N7 A12/BC
DDR_PL_A13 T3 A13
DDR_PL_A14 T7 A14
M7 NC
DQL0 E3 DDR_PL_D48
DQL1 F7 DDR_PL_D49
DQL2 F2 DDR_PL_D50
DQL3 F8 DDR_PL_D51
DQL4 H3 DDR_PL_D52
DQL5 H8 DDR_PL_D53
DQL6 G2 DDR_PL_D54
DQL7 H7 DDR_PL_D55
DQU0 D7 DDR_PL_D56
DQU1 C3 DDR_PL_D57
DQU2 C8 DDR_PL_D58
DQU3 C2 DDR_PL_D59
DQU4 A7 DDR_PL_D60
DQU5 A2 DDR_PL_D61
DQU6 B8 DDR_PL_D62
DQU7 A3 DDR_PL_D63
DQSU C7 DDR_PL_DQS7_P
DQSU B7 DDR_PL_DQS7_N
DQSL F3 DDR_PL_DQS6_P
DQSL G3 DDR_PL_DQS6_N
S40-15
IS43TR16256BL-125KBLI
1.5V_PL
C209 4.7µF 6.3V
C210 470nF
C211 47nF
C222 470nF
C223 470nF
C224 470nF
C228 4.7µF 6.3V
C229 470nF
C230 47nF
GND
U12B
VDD N1 R1 B2 K2 G7 K8 D9 N9 R9 A1 C1 F1 D2 H2 A8 C9 E9 H9
VDDQ C1 F1 D2 H2 A8 C9 E9 H9
VSS E1 M1 P1 T1 J2 B3 G8 J8 A9 M9 P9 T9 B1 D1 G1 E2 D8 E8 B9 F9 G9
VSSQ B1 D1 G1 E2 D8 E8 B9 F9 G9
GND
1.5V_PL
C234 10nF
PL_VTTREF
C236 10nF
GND
VREFDQ H1
VREFCA M8
ZQ L8
R67 240R 1%
GND
NC J1 L1
NC J9 L9
IS43TR16256BL-125KBLI
1.5V_PL
C212 4.7µF 6.3V
C213 470nF
C214 47nF
C225 470nF
C226 470nF
C227 470nF
C231 4.7µF 6.3V
C232 470nF
C233 47nF
GND
U14B
VDD N1 R1 B2 K2 G7 K8 D9 N9 R9 A1 C1 F1 D2 H2 A8 C9 E9 H9
VDDQ C1 F1 D2 H2 A8 C9 E9 H9
VSS E1 M1 P1 T1 J2 B3 G8 J8 A9 M9 P9 T9 B1 D1 G1 E2 D8 E8 B9 F9 G9
VSSQ B1 D1 G1 E2 D8 E8 B9 F9 G9
GND
1.5V_PL
C235 10nF
PL_VTTREF
C237 10nF
GND
VREFDQ H1
VREFCA M8
ZQ L8
R68 240R 1%
GND
NC J1 L1
NC J9 L9
IS43TR16256BL-125KBLI
GND
1.5V_PL
C202 470nF
C203 470nF
C204 470nF
C205 470nF
C206 470nF
C207 470nF
C208 470nF
C215 470nF
C216 470nF
C217 470nF
C218 470nF
C219 470nF
C220 470nF
C221 470nF
GND
DDR_PL_CLK0_P
DDR_PL_CLK0_N
R37 33R
R40 33R
C241 100nF 6.3V X5R
1.5V_PL
Place directly at the clock pins
ClassName: D80
DDR_PL_CLK0_P
DDR_PL_CLK0_N
DDR_PL_DQS4_P
DDR_PL_DQS4_N
DDR_PL_DQS5_P
DDR_PL_DQS5_N
DDR_PL_DQS6_P
DDR_PL_DQS6_N
DDR_PL_DQS7_P
DDR_PL_DQS7_N
trenz electronic
Title: DDR3 RAM PL
A4
Number: TE0783 92I33MA
Rev. 02
Date: 13.07.2018
Copyright: Trenz Electronic GmbH
Page24 of 32
Filename: DDR3-RAM-PL2.SchDoc



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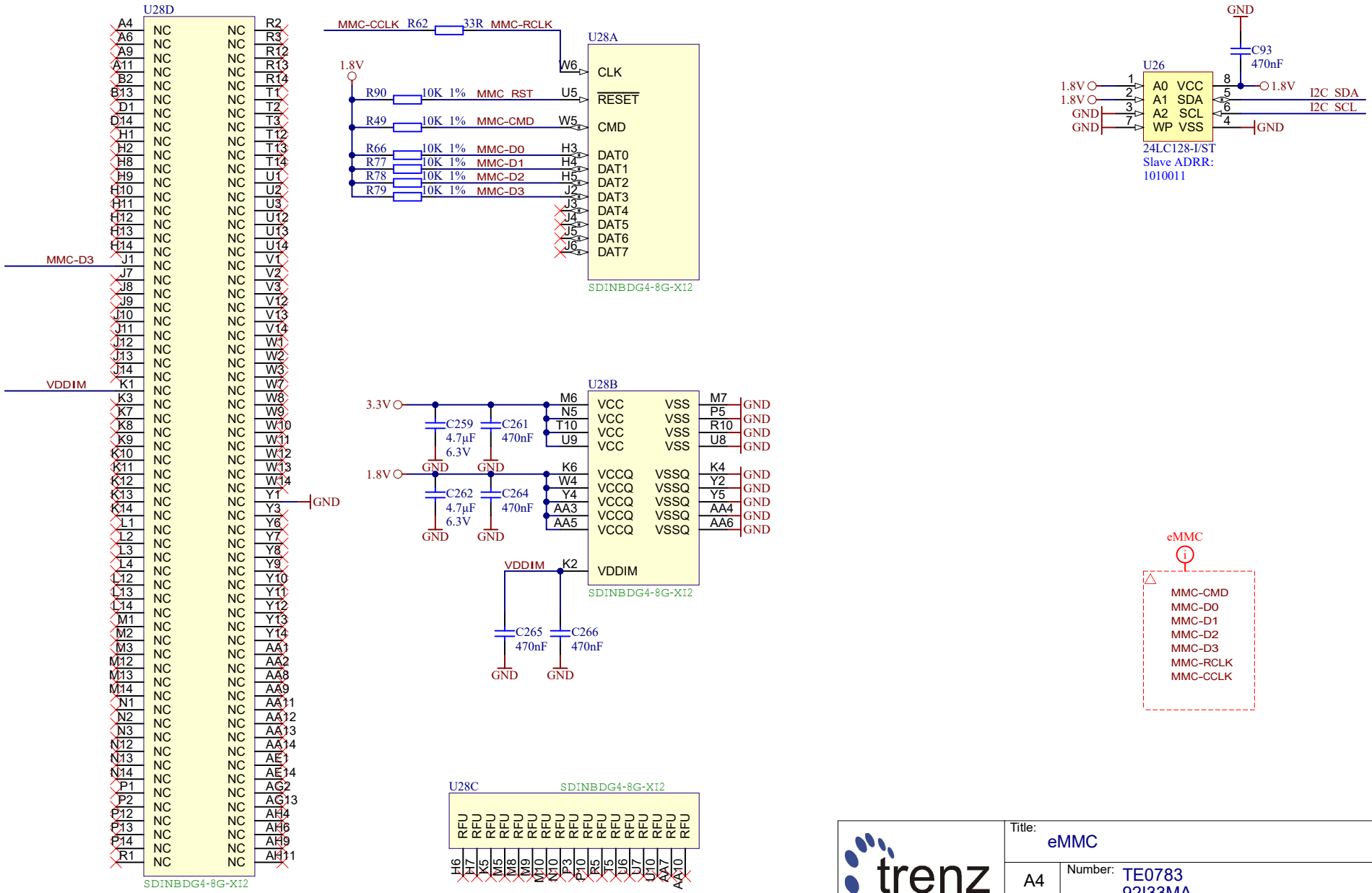
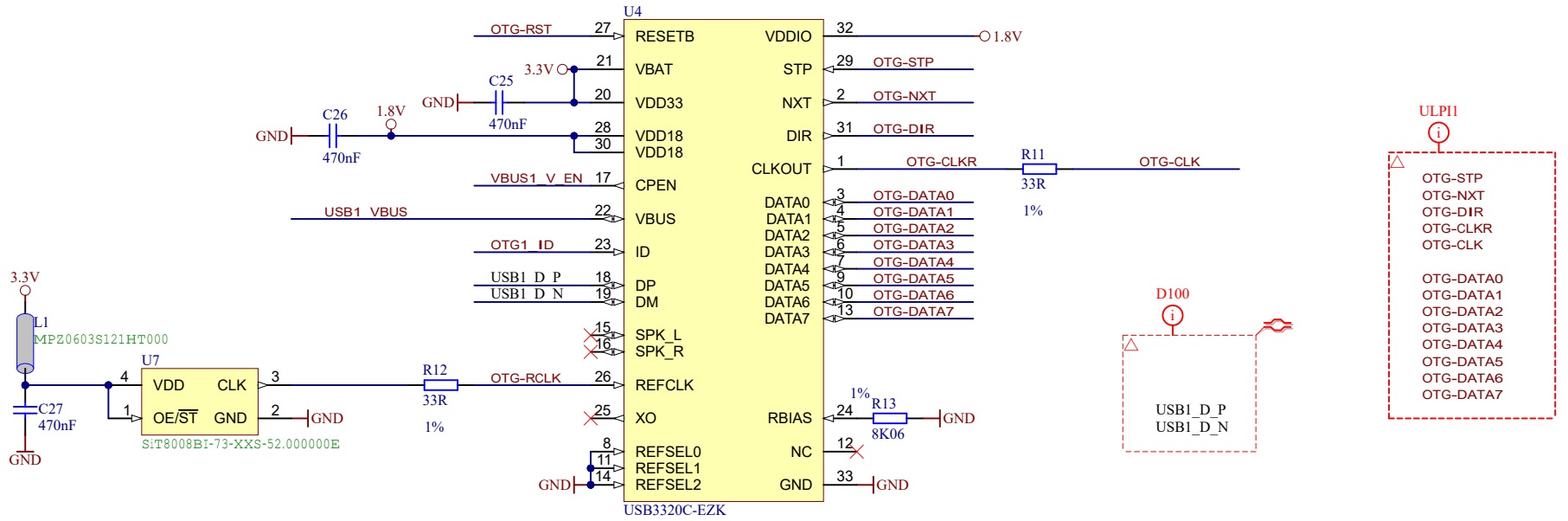
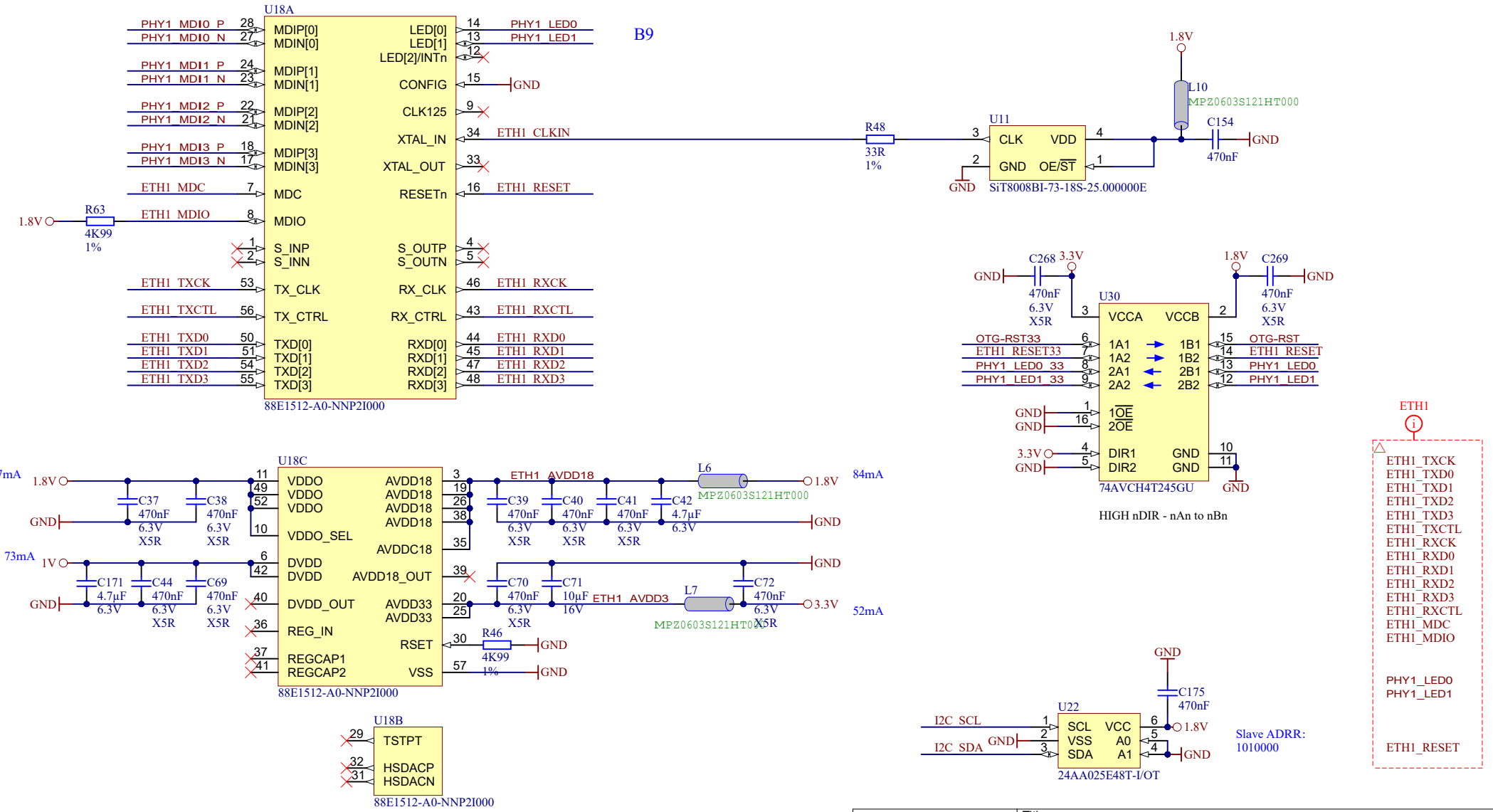
Title: CPLD			
A4	Number: TE0783 92I33MA		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page25 of 32
Filename: CPLD.SchDoc			



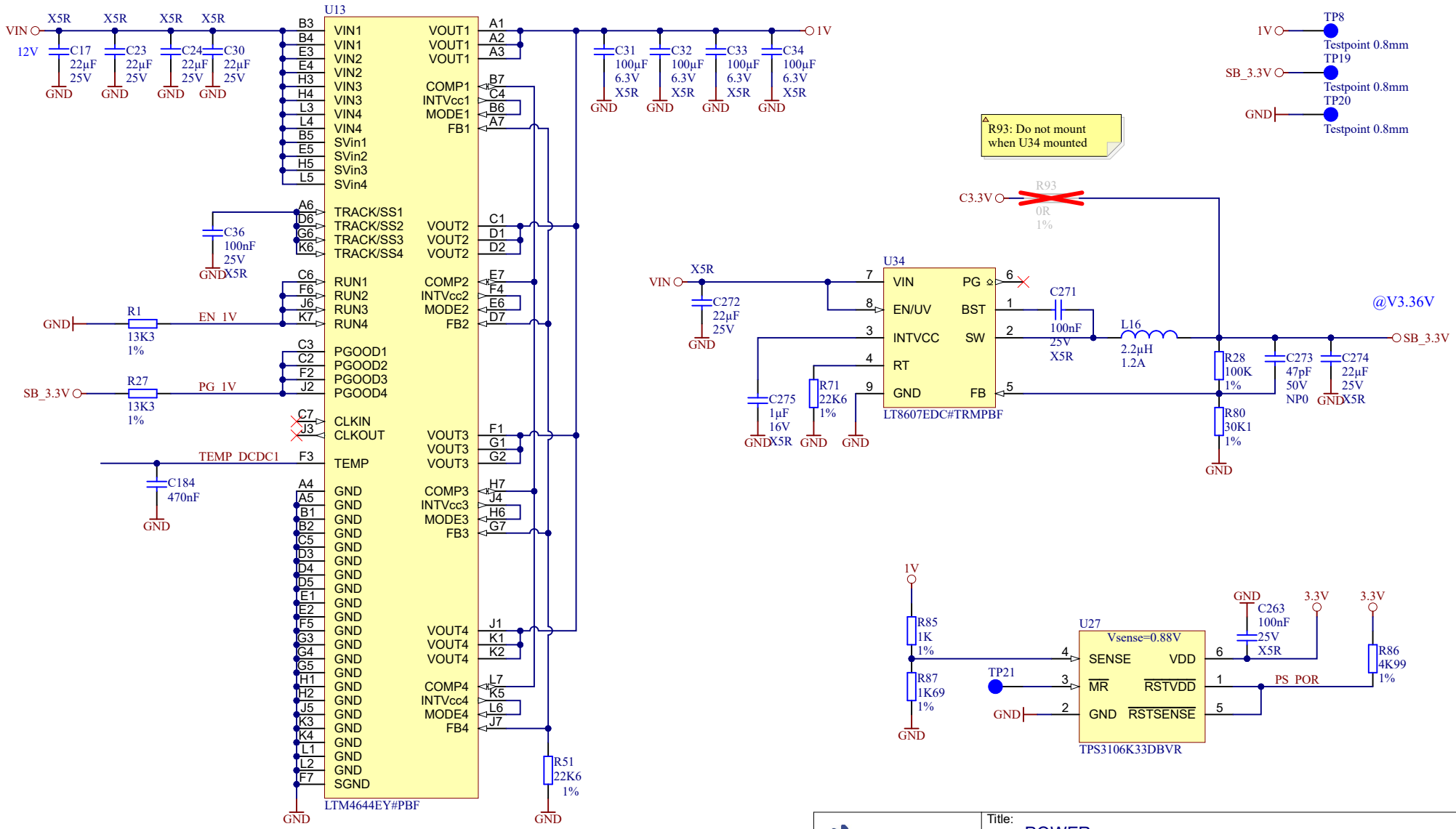
Title:	eMMC		
A4	Number: TE0783 92I33MA		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page26 of 32
Filename:	eMMC.SchDoc		



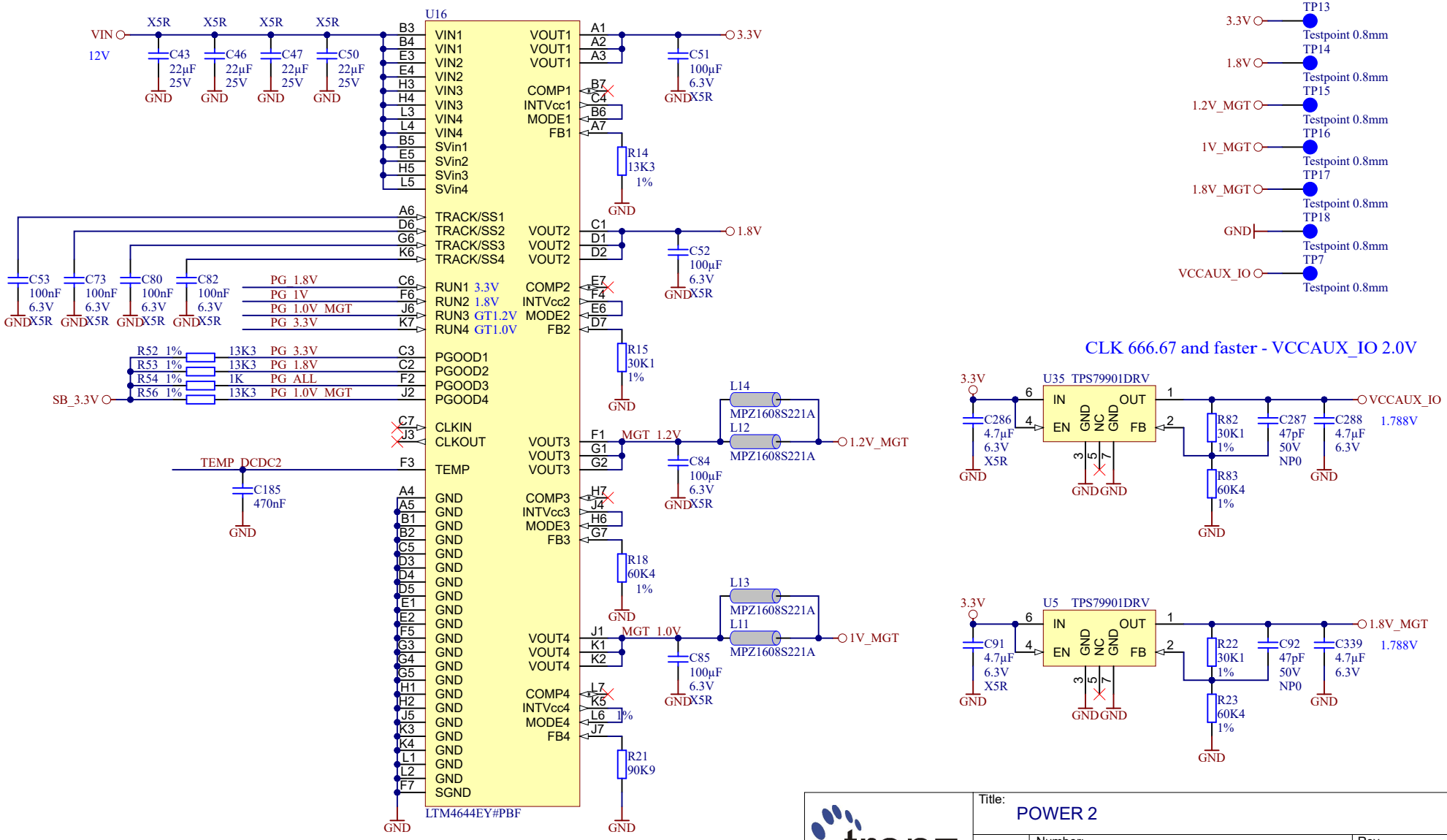
trenz electronic	Title: USB-PHY		
	A4	Number: TE0783 92I33MA	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page27 of 32
	Filename: USB-PHY.SchDoc		



Title: ETH_PHY1			
A4	Number: TE0783 92I33MA		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page28 of 32
Filename: ETH1.SchDoc			

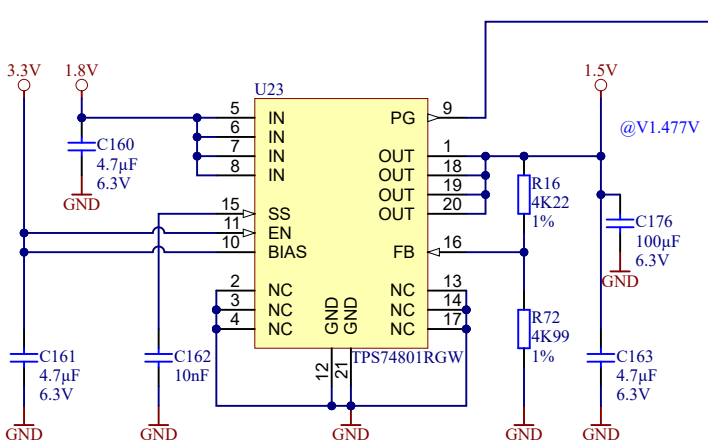


trenz electronic	Title: POWER		
	A4	Number: TE0783 92I33MA	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page29 of 32
	Filename: POWER.SchDoc		

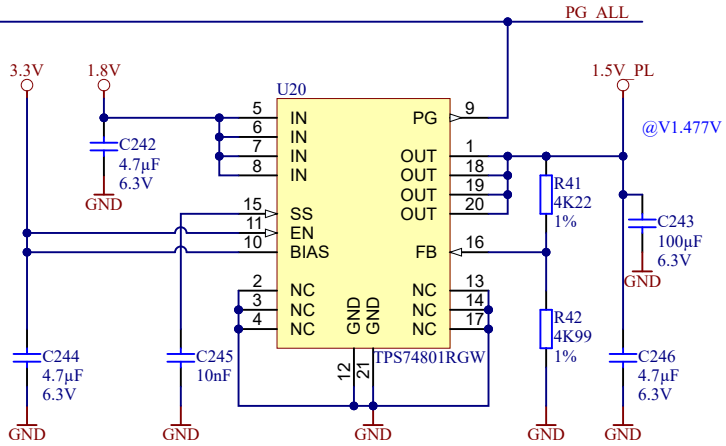


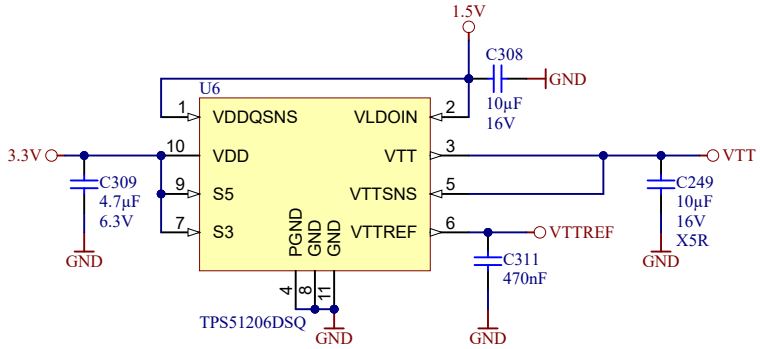
Title: POWER 2			
A4	Number: TE0783 92I33MA		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page30 of 32
Filename: POWER2.SchDoc			

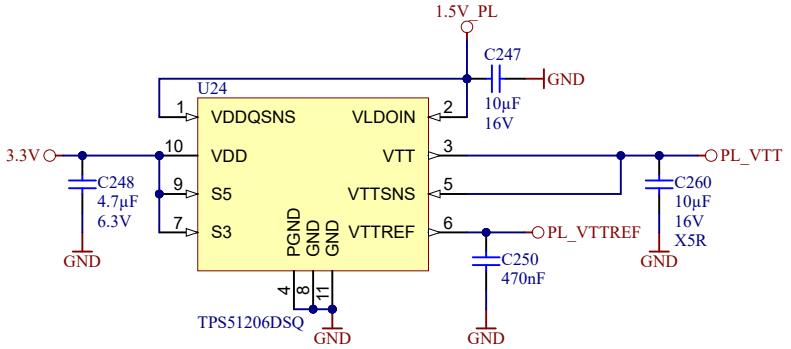
DDR3 PS

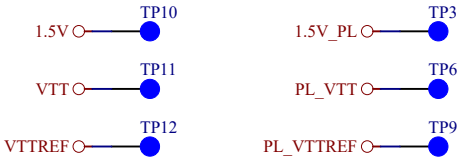


DDR3 PL









Title: POWER 2			
A4	Number: TE0783 92I33MA		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page31 of 32
Filename: POWER3.SchDoc			

REV. 02:

1) Changed power-up sequence: 3.3V next to 1.8V. MGT power domain next to 3.3V

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	A4	Number: TE0783 92I33MA	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH / TT	Page32 of 32
	Filename: Revision Changes.SchDoc		