

U\_SOC  
SOC.SchDoc

U\_DDR3-RAM  
DDR3-RAM.SchDoc

U\_CPLD  
CPLD.SchDoc

U\_USB-PHY  
USB-PHY.SchDoc

U\_ETH1  
ETH1.SchDoc

U\_Clock  
Clock.SchDoc

U\_eMMC  
eMMC.SchDoc

U\_POWER2  
POWER2.SchDoc

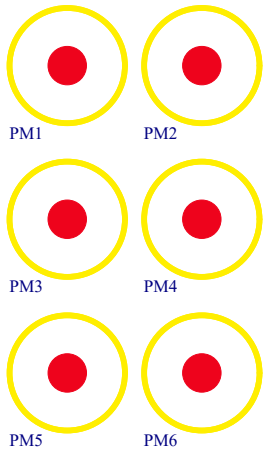
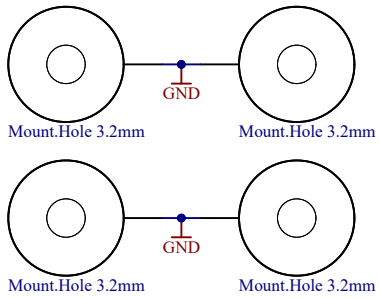
U\_Connectors  
Connectors.SchDoc

U\_Rev\_changes  
Revision Changes.SchDoc

U\_POWER  
POWER.SchDoc

U\_POWER3  
POWER3.SchDoc


LOGO1  
TE Logo PRINT Layer  
LOGO PRINT



Serial  
Serialnumber 6,3 x 6.3mm



Assembly variant	92135PA
Created by	MR
Modified by	MR
Modified at	2021-08-18
SVN Revision	8604

			Title: Overview	
			A4	Number: TE0783 92135PA
Date: 13.07.2018		Copyright: Trenz Electronic GmbH		Page1 of 32
Filename: TE0783.SchDoc				

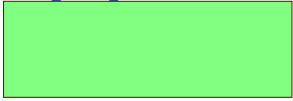
1

2

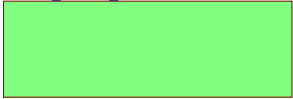
3

4

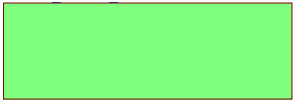
U\_HSMC\_CONN\_J1  
HSMC\_CONN\_J1.SchDoc



U\_HSMC\_CONN\_J2  
HSMC\_CONN\_J2.SchDoc



U\_HSMC\_CONN\_J3  
HSMC\_CONN\_J3.SchDoc



A

A

B


B

C

C

D

D

			Title: <b>Connectors</b>		
			A4	Number: <b>TE0783 92I35PA</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>		Copyright: <b>Trenz Electronic GmbH</b>		Page <b>2</b> of <b>32</b>	
Filename: <b>Connectors.SchDoc</b>					

1

2

3

4

1

2

3

4

A

A

B

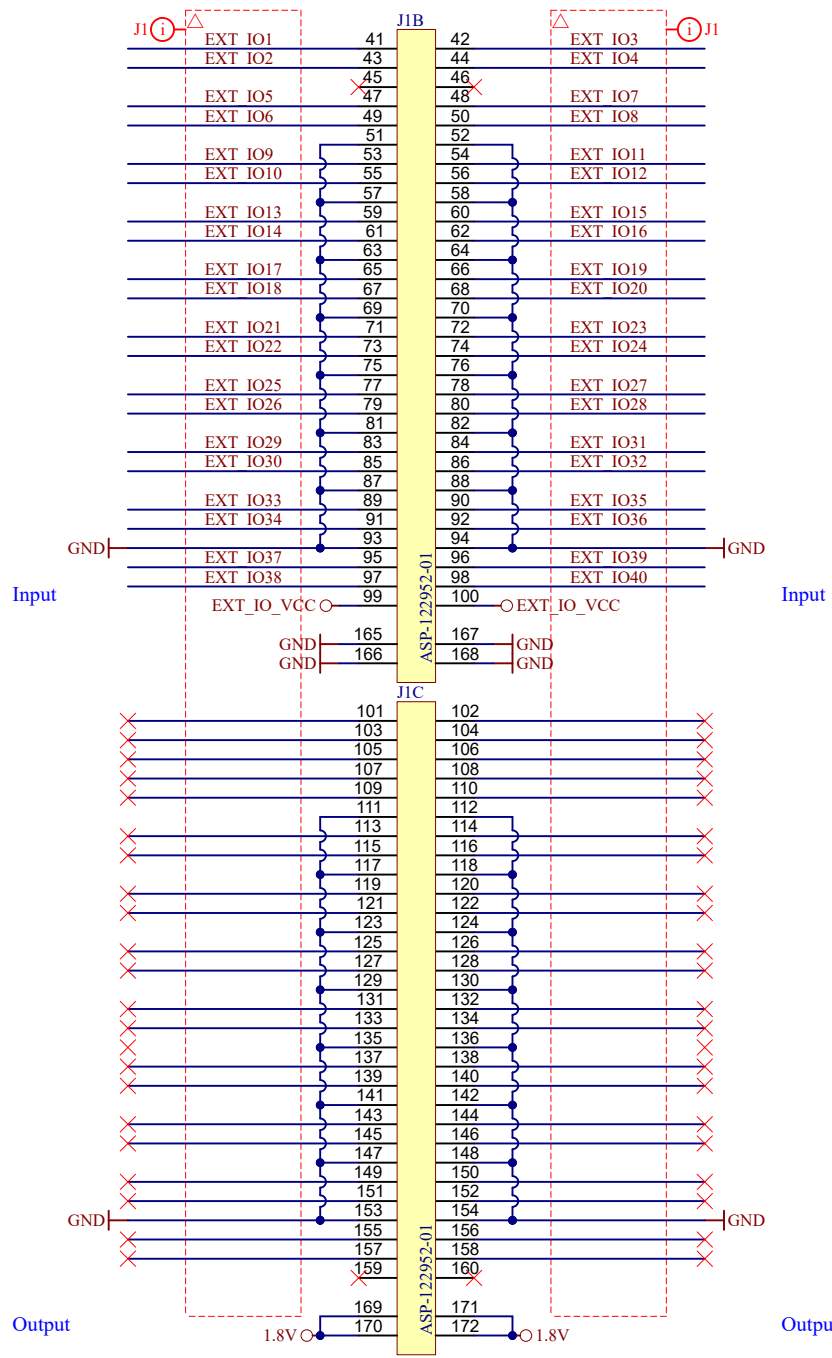
B

C

C

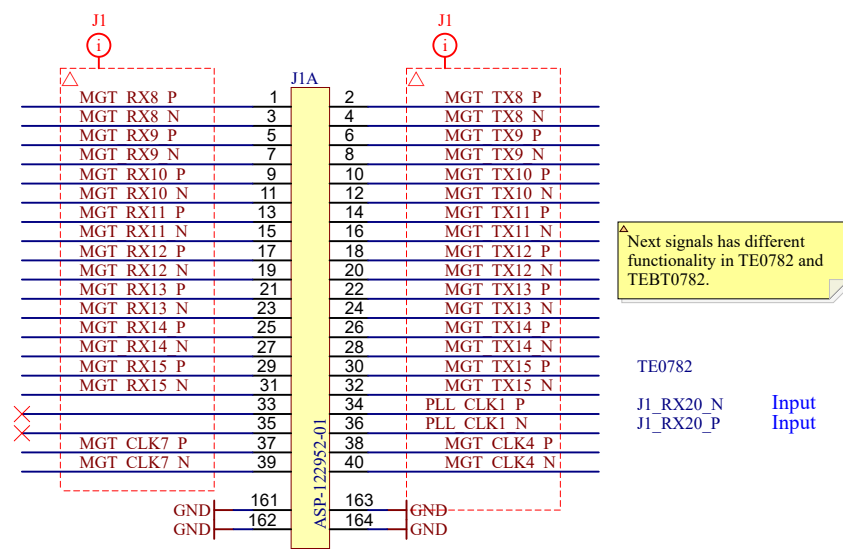
D

D



Next signals has different functionality in TE0782 and TEBT0782.

TE0782  
J1\_TX20\_N  
J1\_TX20\_P  
J1\_TX21\_N  
J1\_TX21\_P



Next signals has different functionality in TE0782 and TEBT0782.

TE0782  
J1\_RX20\_N  
J1\_RX20\_P



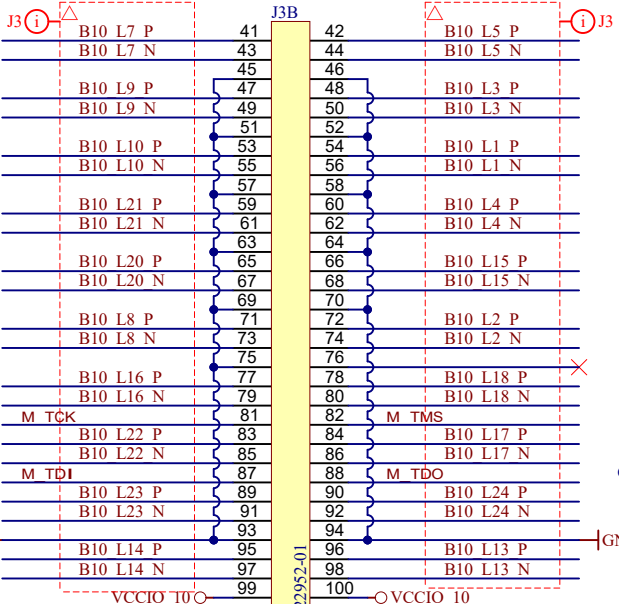
Title: HSMC_Connector_J1		
A4	Number: TE0783 92I35PA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page3 of 32
Filename: HSMC_CONN_J1.SchDoc		

1

2

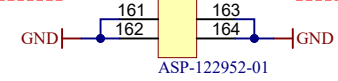
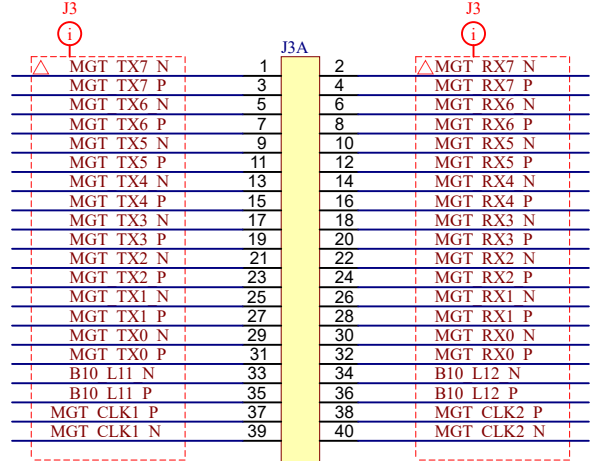
3

4



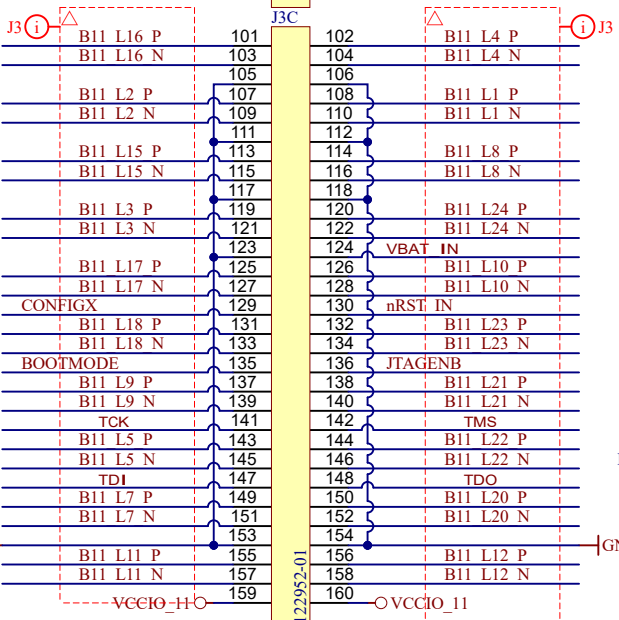
CPLD JTAG !

Input



Next signals has different functionality in TE0782 and TEBT0782.

S15328\_CLK1\_P  
S15328\_CLK1\_N



FPGA JTAG !

Input



Title: HSMC_Connector_J3		
A4	Number: TE0783 92135PA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page4 of 32
Filename: HSMC_CONN_J3.SchDoc		

A

B

C

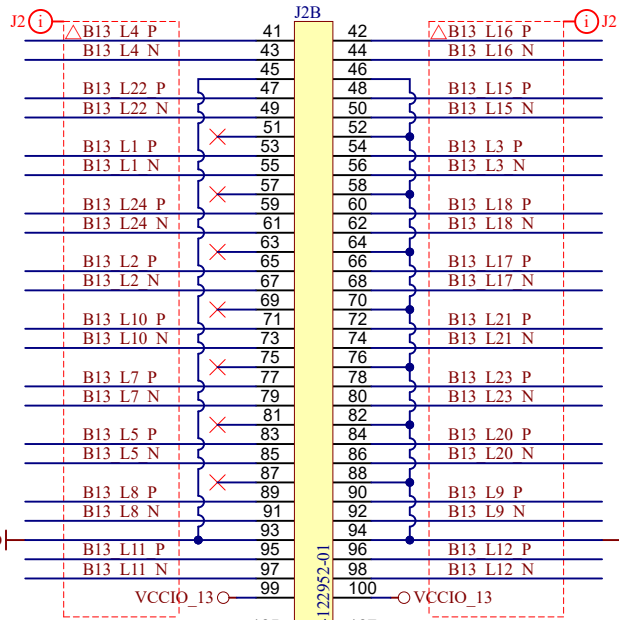
D

A

B

C

D



Input

Input

Output

Output

Output

Input\*

Input

Output

Input

Input

Output

Output

Output

Input\*

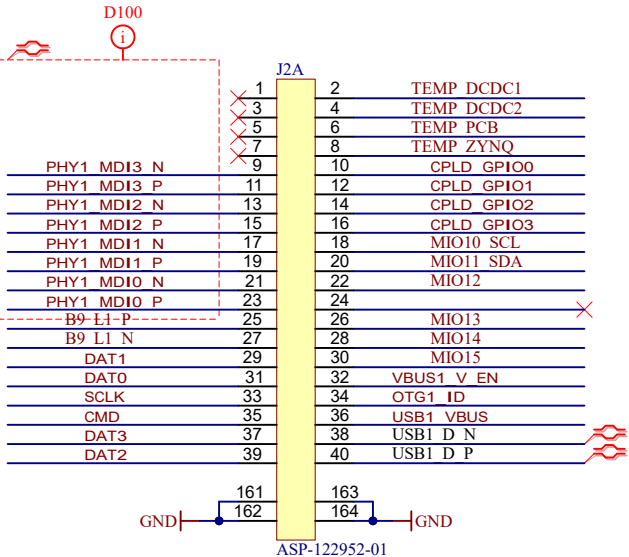
Input

Output

Next signals has different functionality in TE0782 and TEBT0782.

TE0782

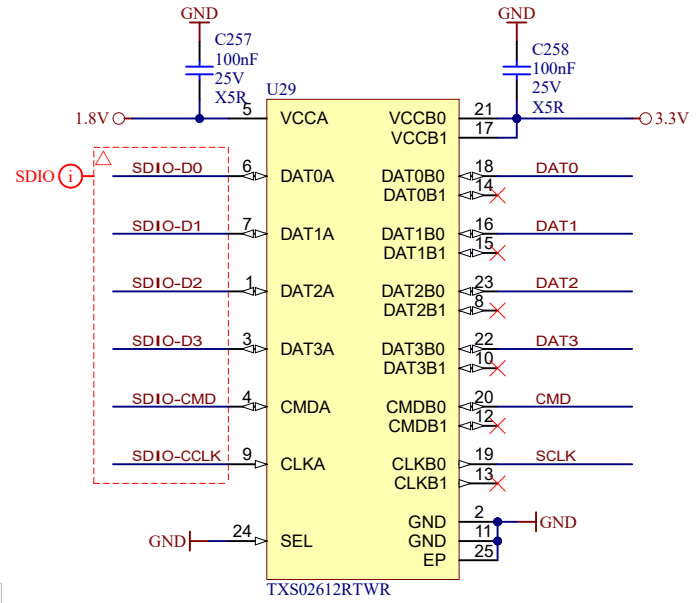
- PHY2\_MD13\_N
- PHY2\_MD13\_P
- PHY2\_MD12\_N
- PHY2\_MD12\_P
- PHY2\_MD11\_N
- PHY2\_MD11\_P
- PHY2\_MD10\_N
- PHY2\_MD10\_P



Next signals has different functionality in TE0782 and TEBT0782.

TE0782

- CPLD\_GPIO4
- CPLD\_GPIO5
- OTG2\_ID
- USB2\_VBUS
- USB2\_D\_N
- USB2\_D\_P
- VBUS2\_V\_EN



SDCARD

- DAT0
- DAT1
- DAT2
- DAT3
- CMD
- SCLK

\* - C3.3V: Normally leave unconnected



Title: HSMC_Connector_J2		
A4	Number: TE0783 92135PA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page5 of 32
Filename: HSMC_CONN_J2.SchDoc		

1

2

3

4

U\_PS-DDR  
PS-DDR.SchDoc



U\_B9  
B9.SchDoc



U\_MIO-BANKS  
MIO-BANKS.SchDoc



U\_B10  
B10.SchDoc



U\_HP-BANKS  
HP-BANKS.SchDoc



U\_B11  
B11.SchDoc



U\_FPGA-MGT  
FPGA-MGT.SchDoc



U\_B12  
B12.SchDoc



U\_FPGA-CFG  
FPGA-CFG.SchDoc



U\_B13  
B13.SchDoc



U\_FPGA-PWR  
FPGA-PWR.SchDoc



A

A

B


B

C

C

D

D

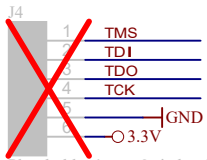
			Title: SOC		
			A4	Number: TE0783 92135PA	Rev. 02
Date: 13.07.2018		Copyright: Trenz Electronic GmbH		Page6 of 32	
Filename: SOC.SchDoc					

1

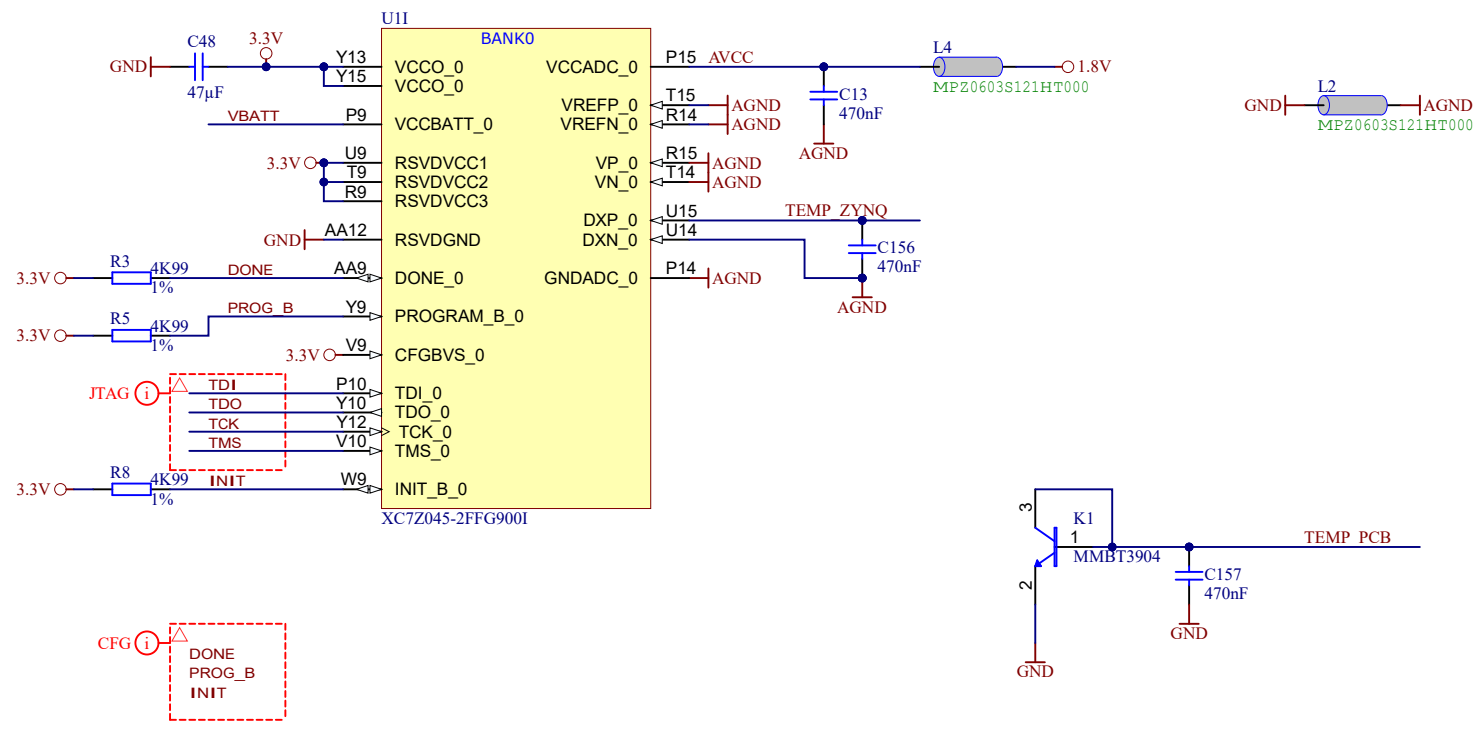
2

3

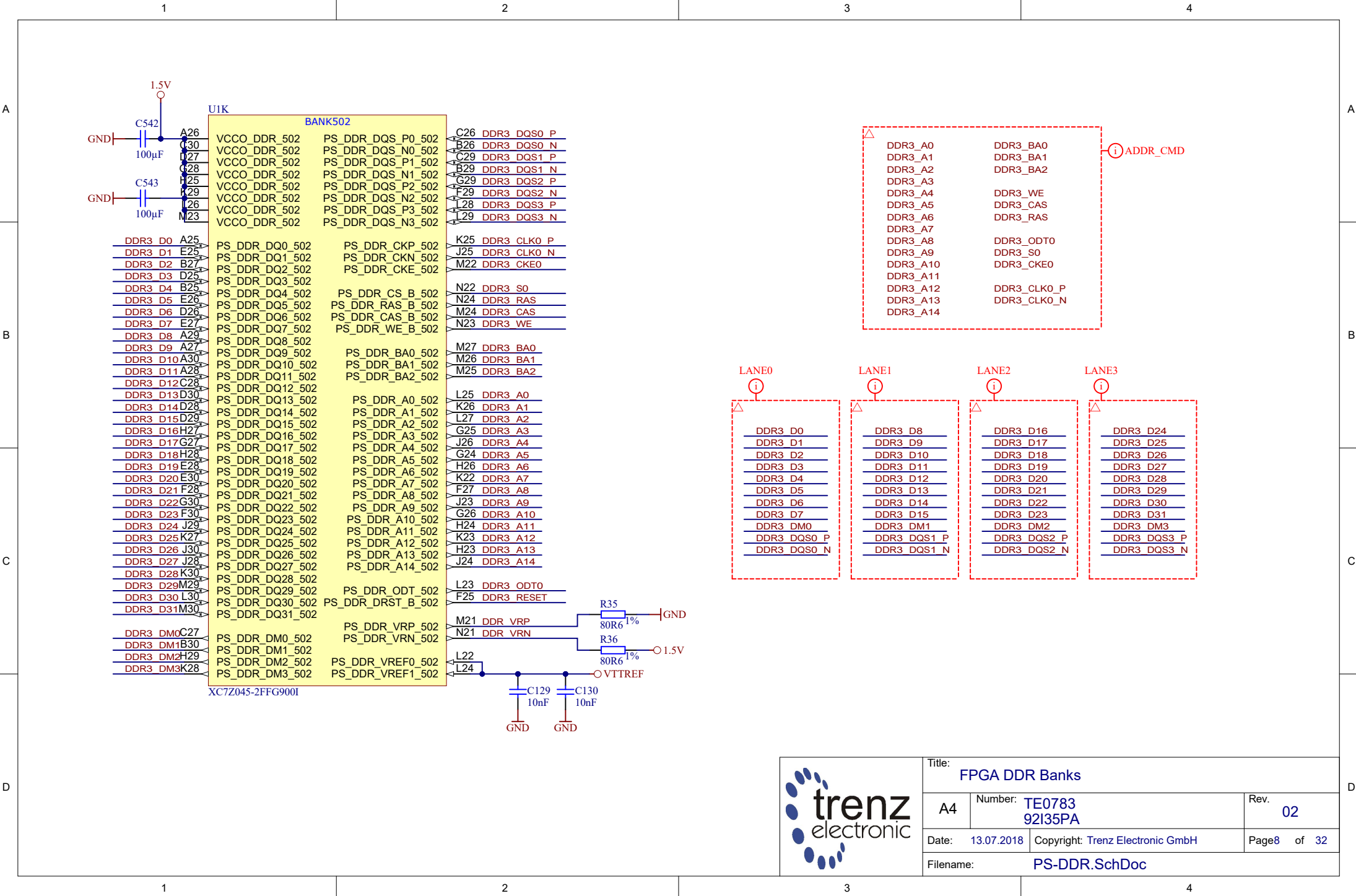
4



Placeholder 1 row 6 pin header

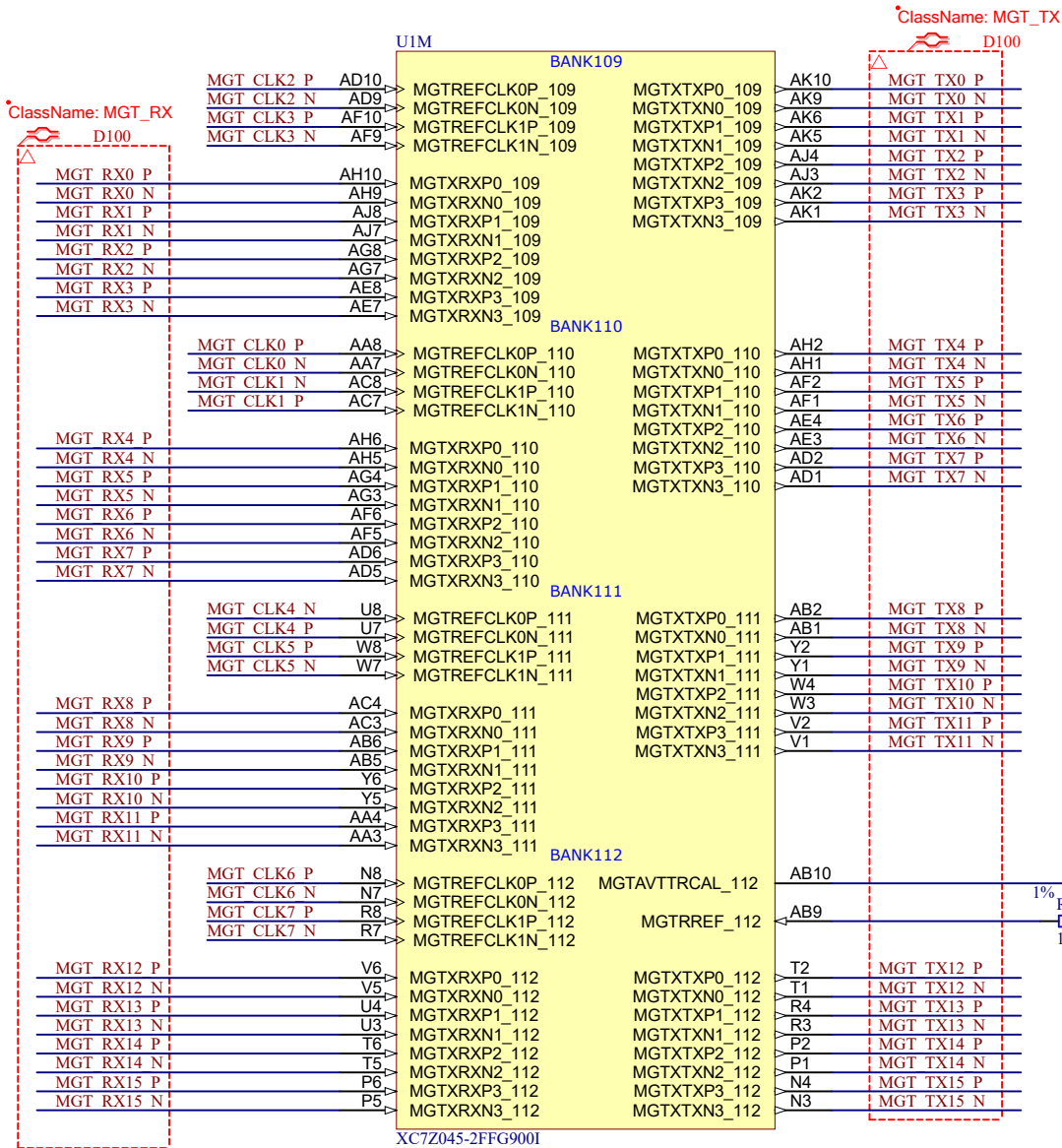


Title: <b>FPGA Configuration</b>		
A4	Nummer: <b>TE0783 92I35PA</b>	Rev. <b>02</b>
Datum: <b>13.07.2018</b>	Zeichner: <b>Trenz Electronic GmbH</b>	Blatt <b>7</b> von <b>32</b>
Filename: <b>FPGA-CFG.SchDoc</b>		

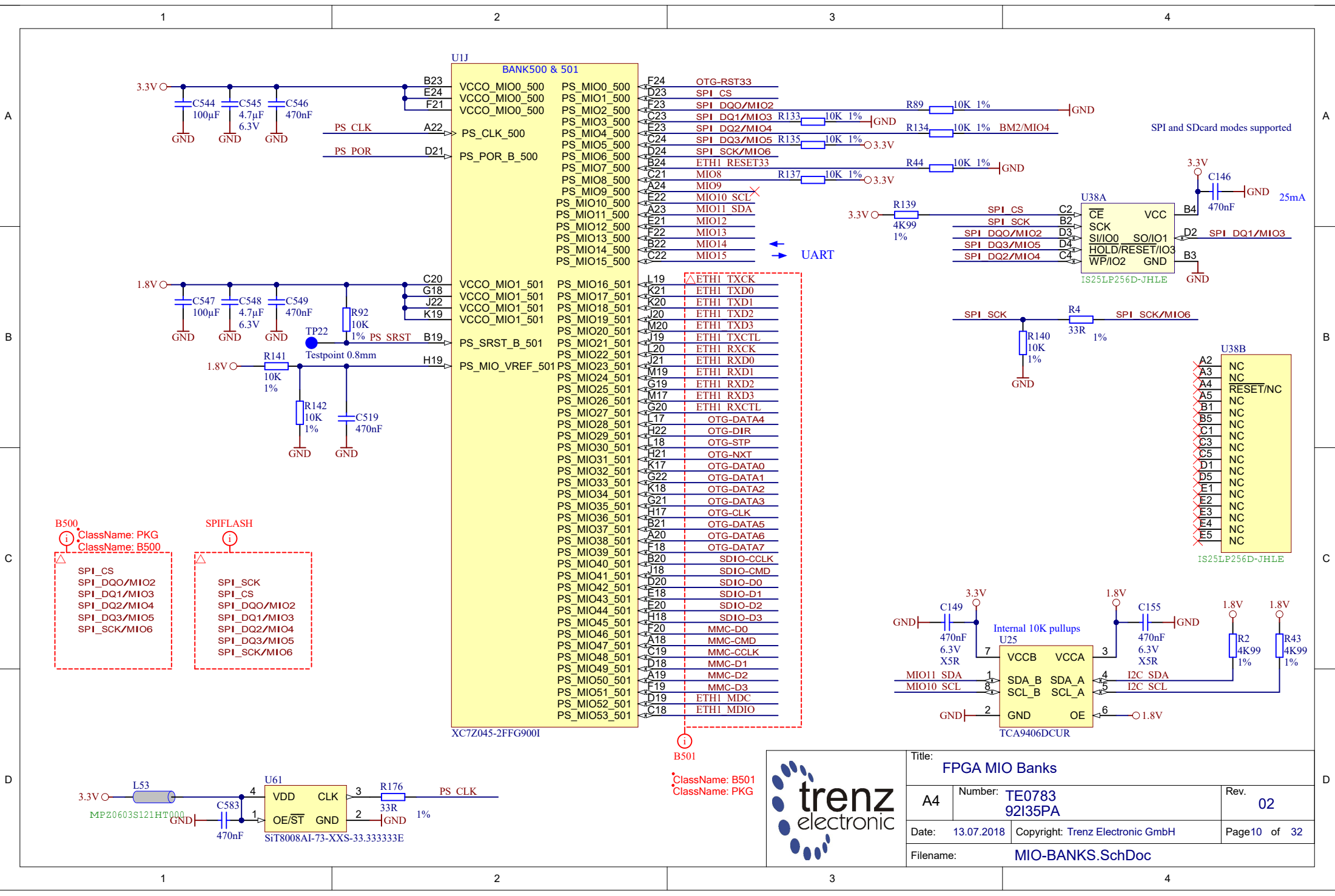


Title: <b>FPGA DDR Banks</b>		
A4	Number: <b>TE0783 92I35PA</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>8</b> of <b>32</b>
Filename: <b>PS-DDR.SchDoc</b>		

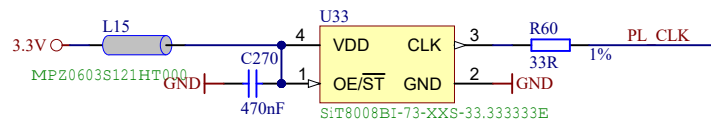
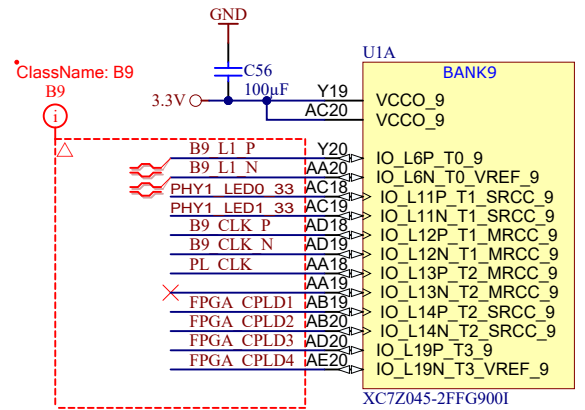





Title: <b>FPGA MGT</b>		
A4	Number: <b>TE0783 92135PA</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>9</b> of <b>32</b>
Filename: <b>FPGA-MGT.SchDoc</b>		

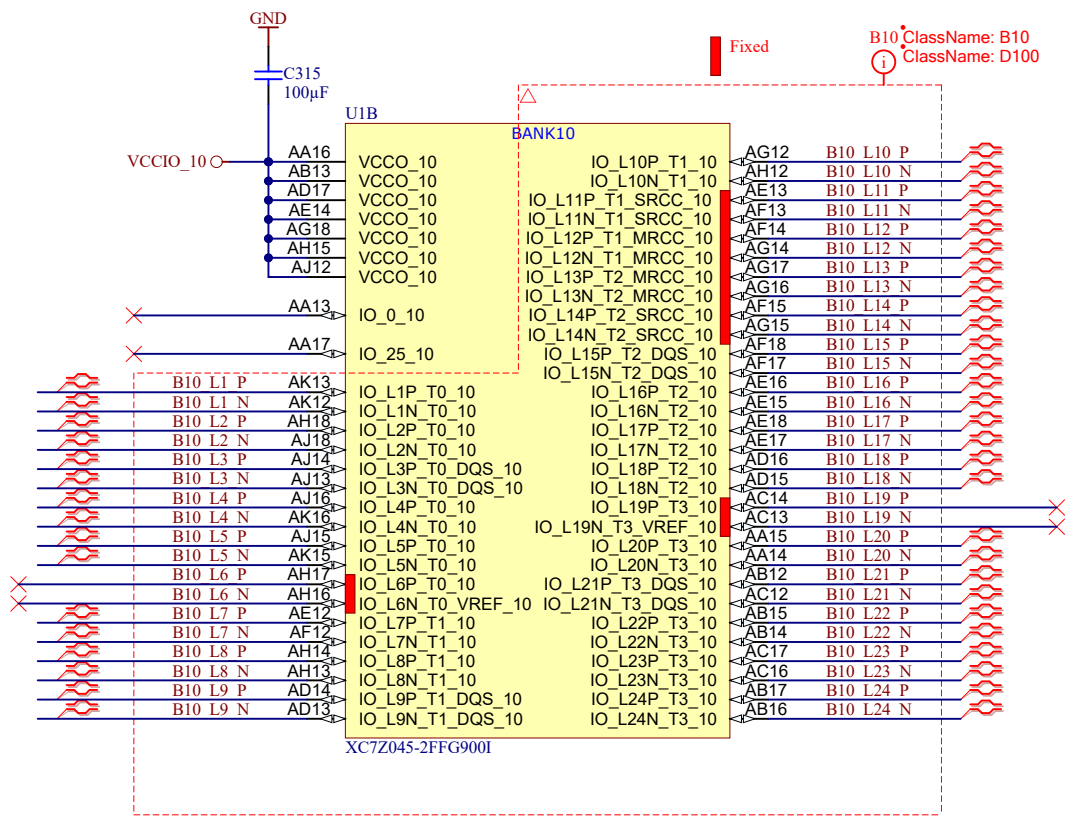


Title: <b>FPGA MIO Banks</b>		
A4	Number: <b>TE0783 92135PA</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>10</b> of <b>32</b>
Filename: <b>MIO-BANKS.SchDoc</b>		

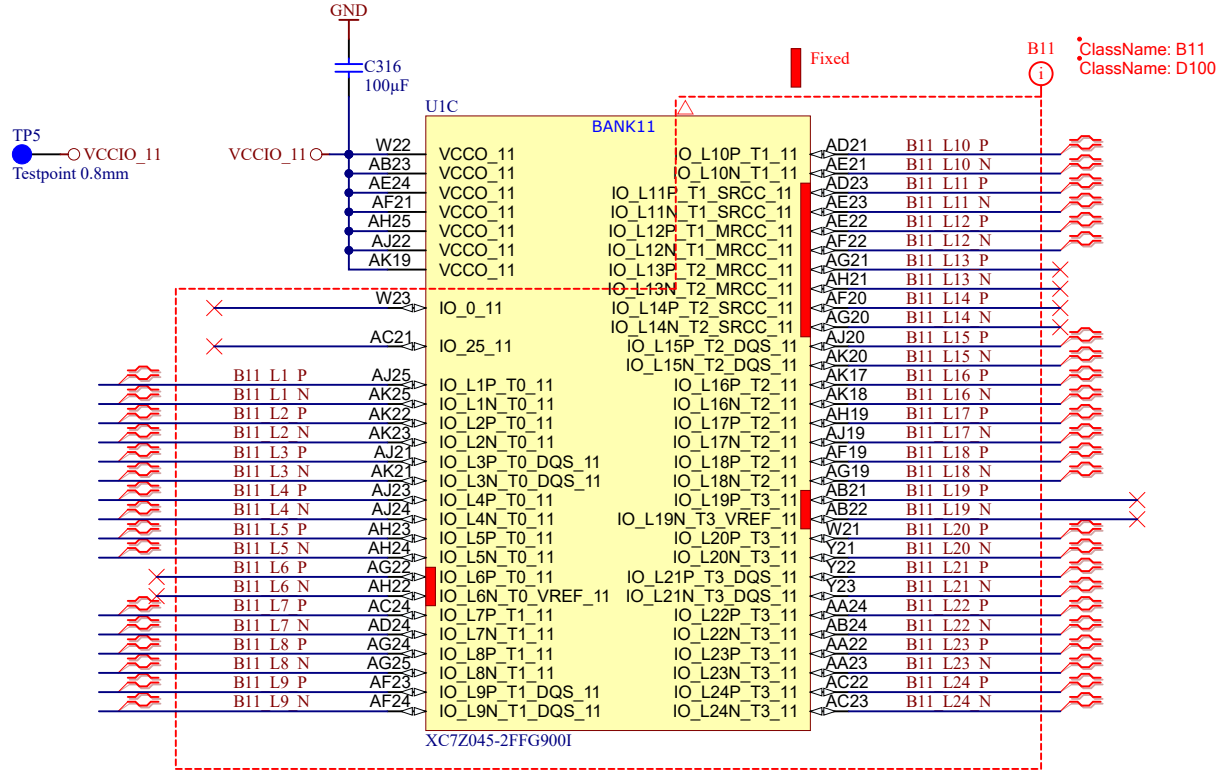


		Title: FPGA B9	
		A4	Number: TE0783 92I35PA
Date: 13.07.2018		Copyright: Trenz Electronic GmbH	
Page 11 of 32		Filename: B9.SchDoc	

TP4  
 ●—○ VCCIO\_10  
 Testpoint 0.8mm



Title: <b>FPGA B10</b>		
A4	Number: <b>TE0783 92I35PA</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>12</b> of <b>32</b>
Filename: <b>B10.SchDoc</b>		



	Title: <b>FPGA B11</b>		
	A4	Number: <b>TE0783 92I35PA</b>	Rev. <b>02</b>
	Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>13</b> of <b>32</b>
	Filename: <b>B11.SchDoc</b>		

A

A

B


B

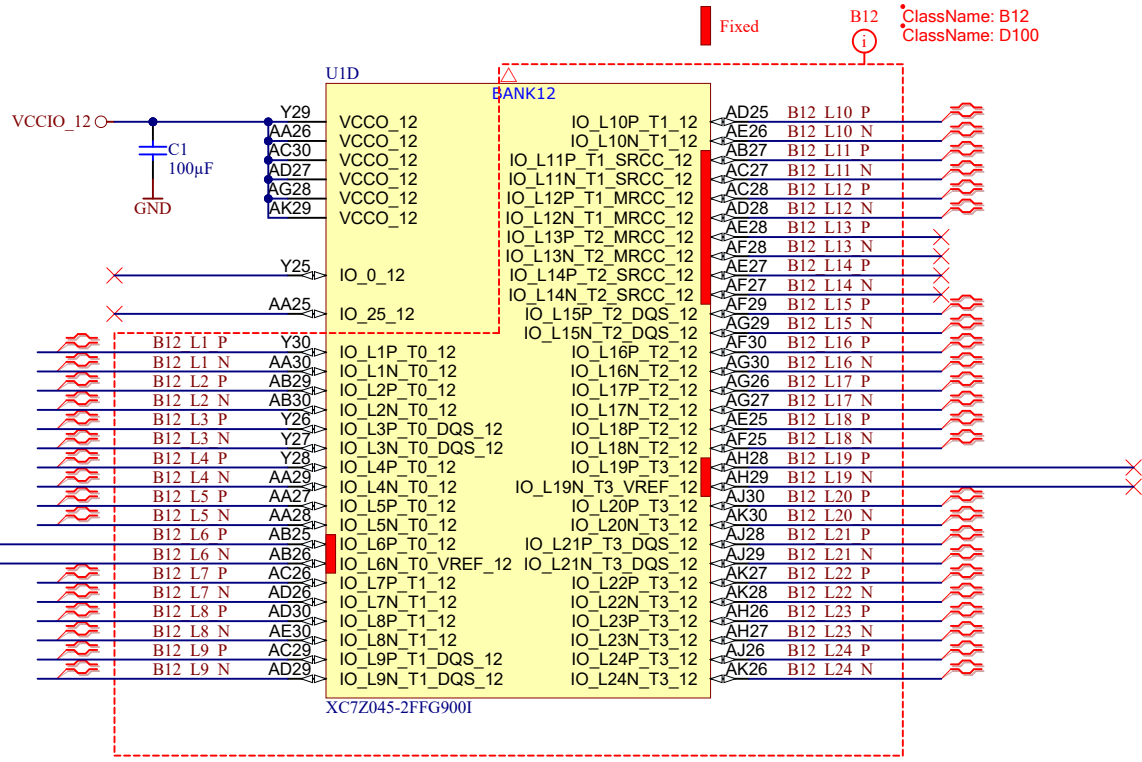
C

C


D

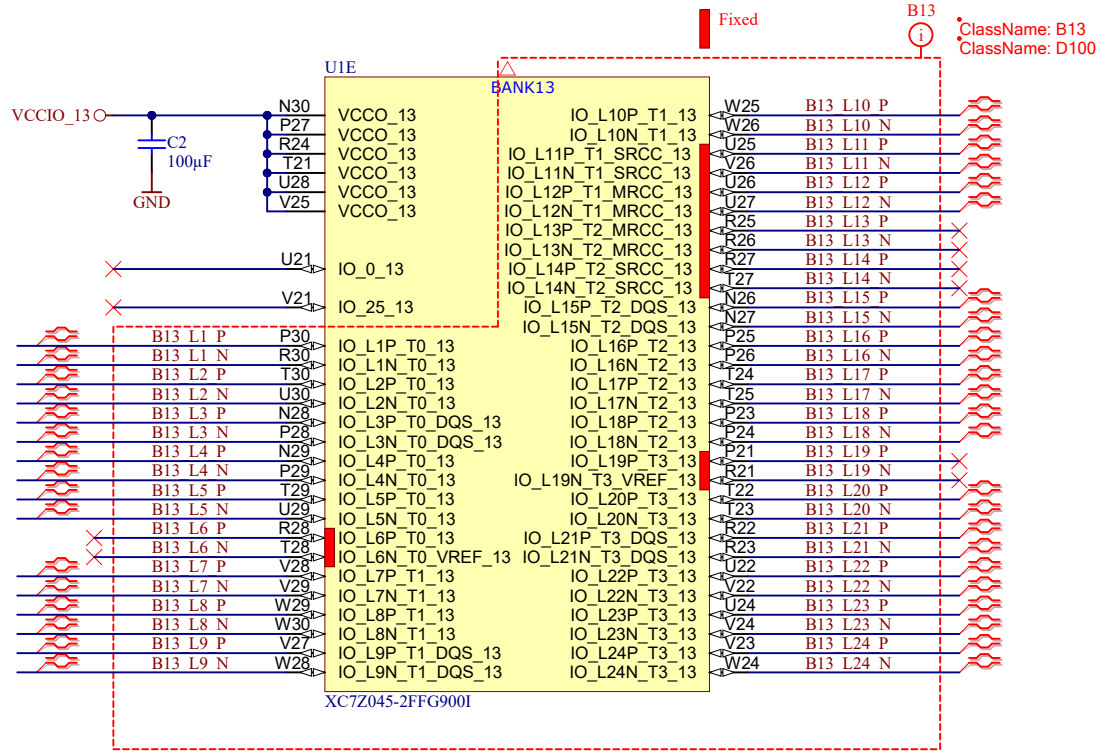
D

TP1  
 VCCIO\_12  
 Testpoint 0.8mm



Title: <b>FPGA B12</b>		
A4	Number: <b>TE0783 92135PA</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>14</b> of <b>32</b>
Filename: <b>B12.SchDoc</b>		

TP2  
 VCCIO\_13  
 Testpoint 0.8mm



Title: <b>FPGA B13</b>		
A4	Number: <b>TE0783 92135PA</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>15</b> of <b>32</b>
Filename: <b>B13.SchDoc</b>		

1

2

3

4

U\_B33  
B33.SchDoc



U\_B34  
B34.SchDoc



U\_B35  
B35.SchDoc



U\_DDR3-RAM-PL1  
DDR3-RAM-PL1.SchDoc



U\_DDR3-RAM-PL2  
DDR3-RAM-PL2.SchDoc



A

A

B


B

C

C

D

D

	Title: <b>FPGA HP Banks</b>		
	A4	Number: <b>TE0783 92I35PA</b>	Rev. <b>02</b>
	Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>16</b> of <b>32</b>
	Filename: <b>HP-BANKS.SchDoc</b>		

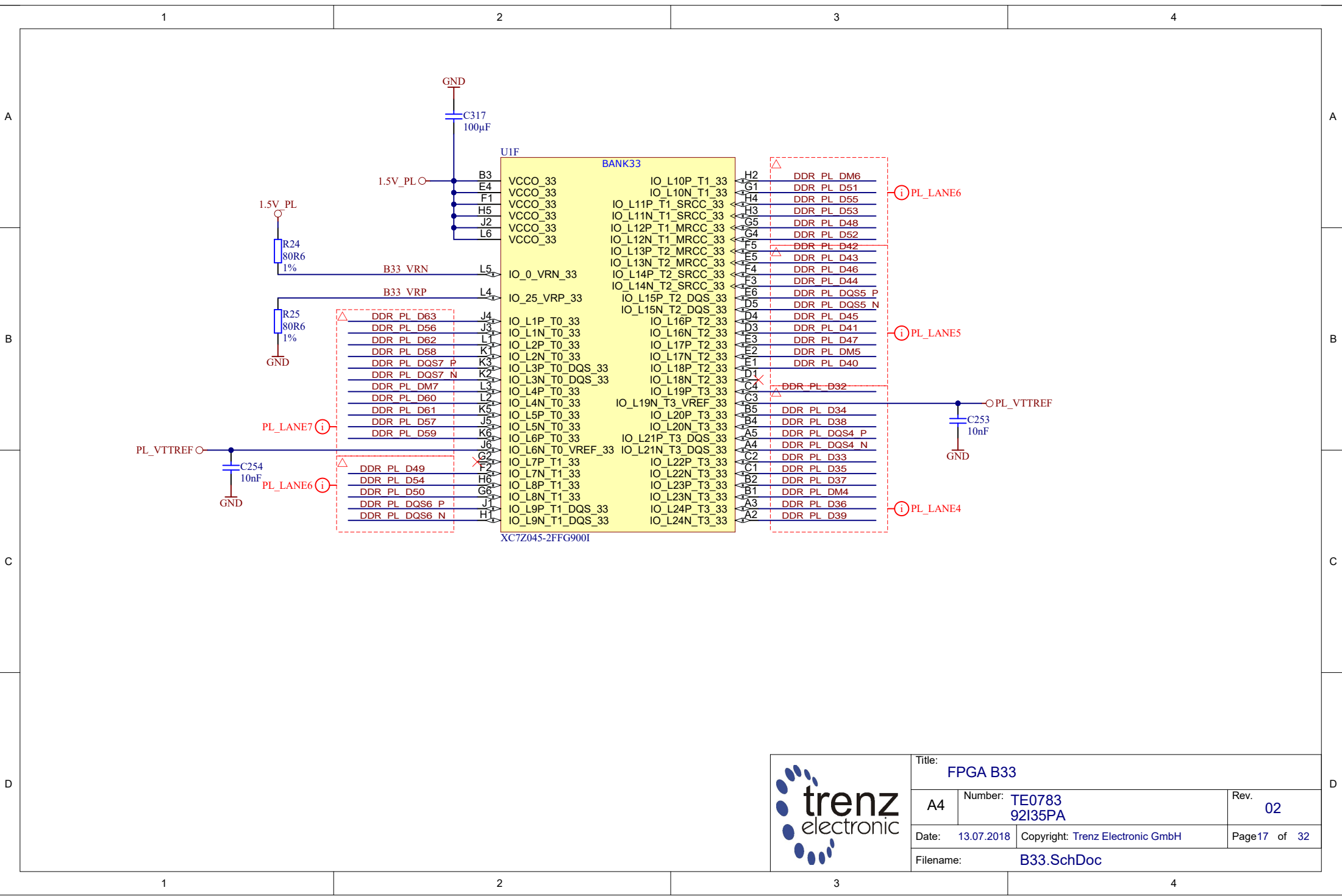
1

2

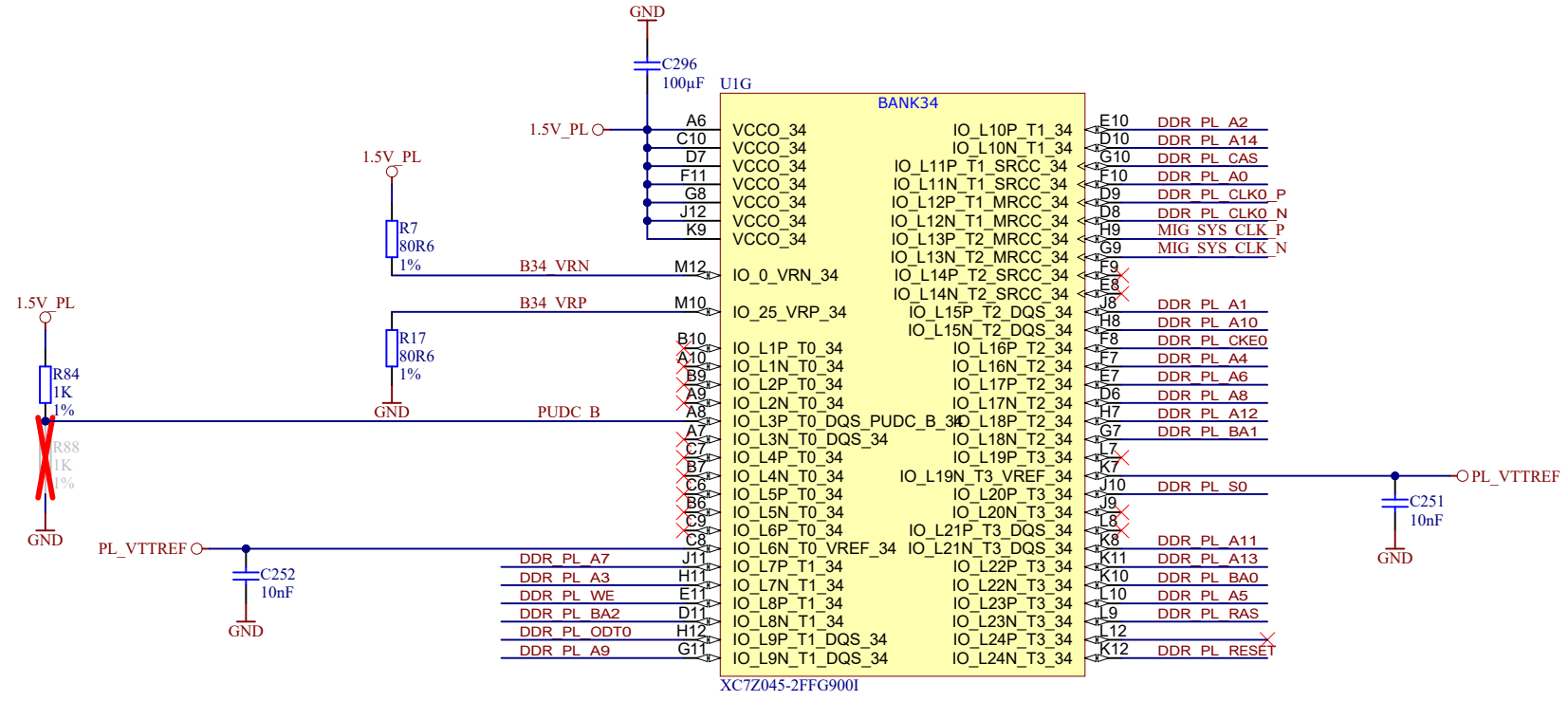
3

4

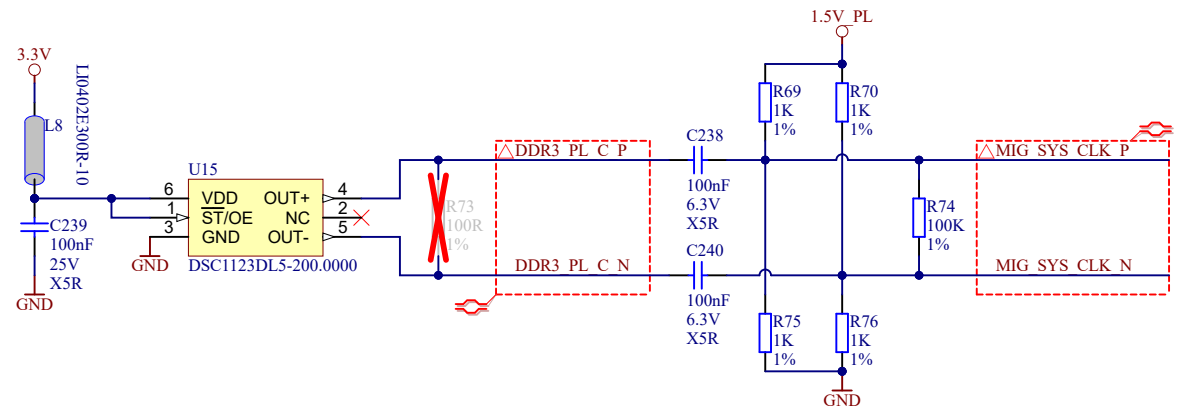




	Title: <b>FPGA B33</b>		
	A4	Number: <b>TE0783 92135PA</b>	Rev. <b>02</b>
	Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>17</b> of <b>32</b>
	Filename: <b>B33.SchDoc</b>		



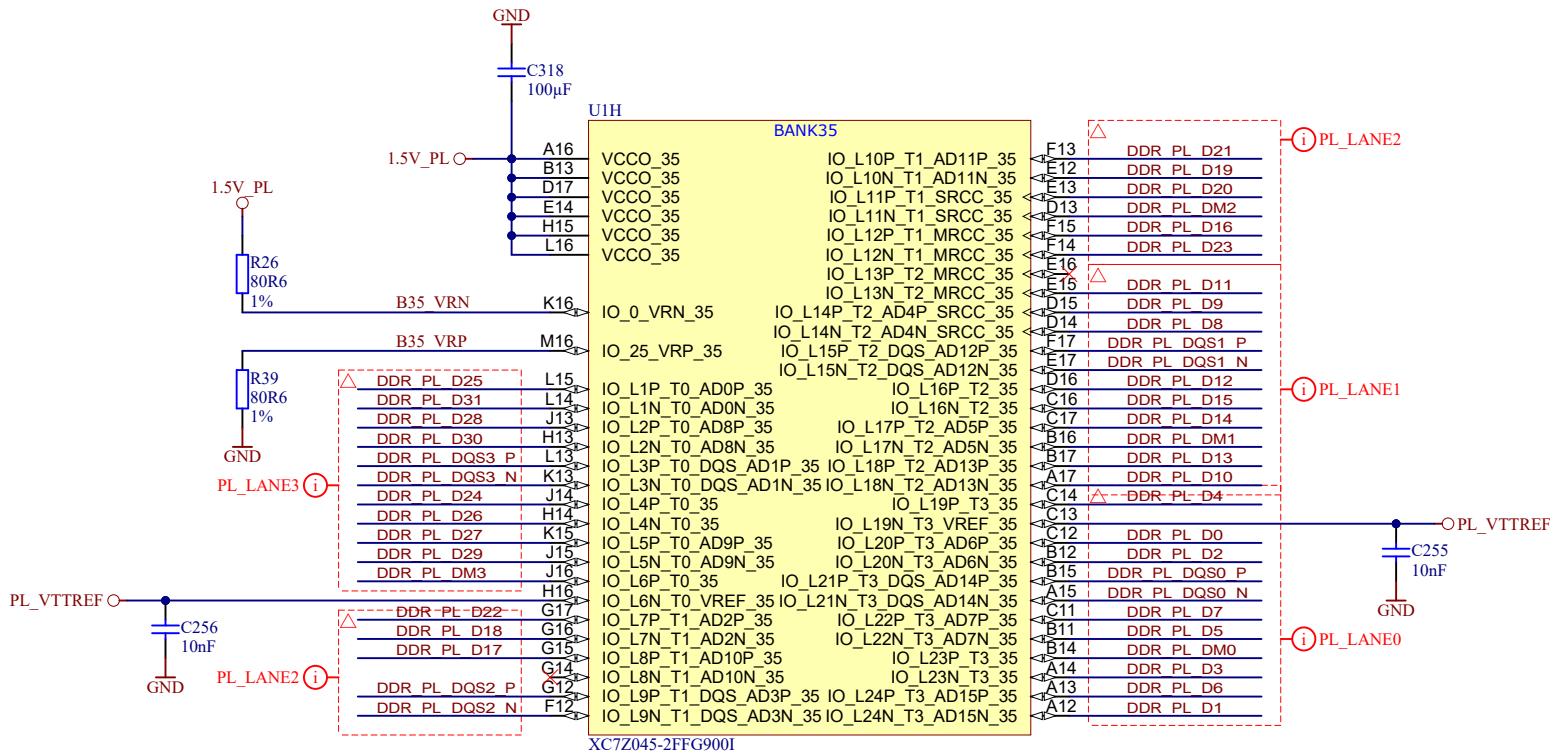

XC7Z045-2FFG900I



Check clock source. R74 100R changed to 100K

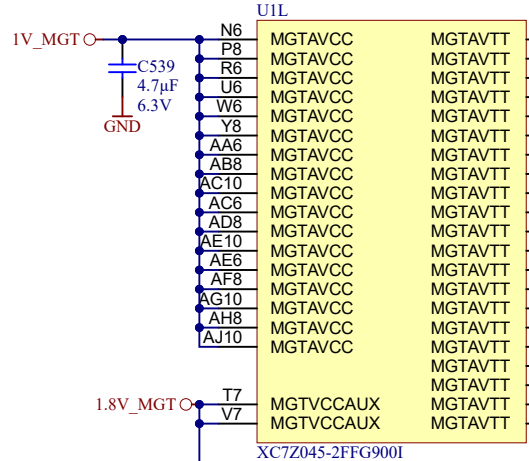
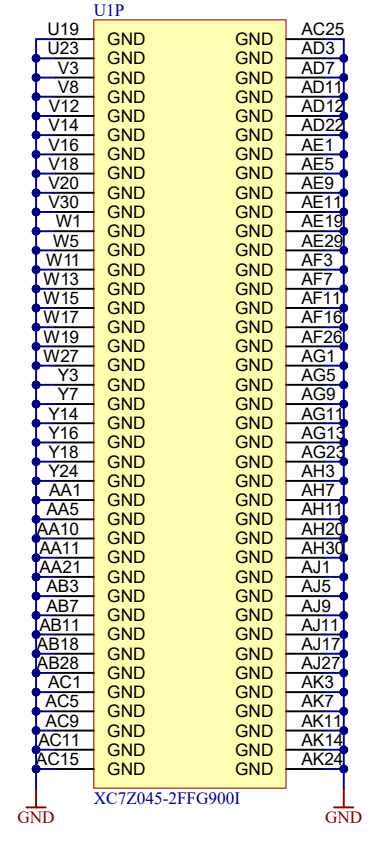
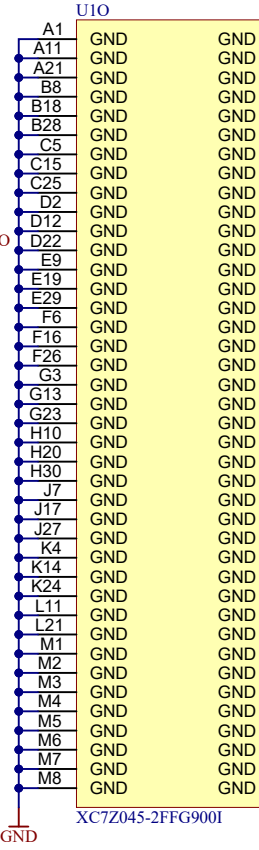
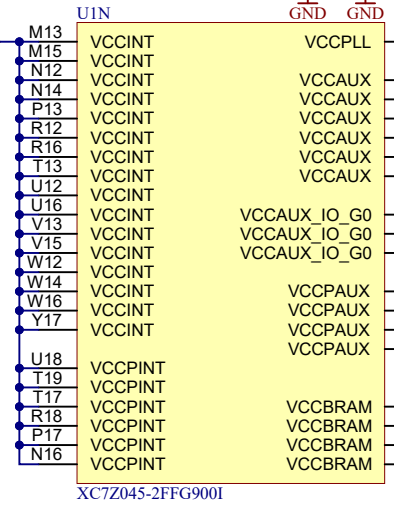
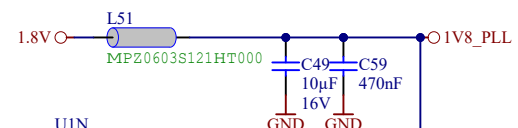
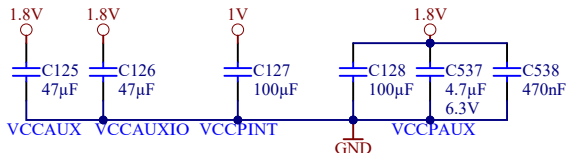
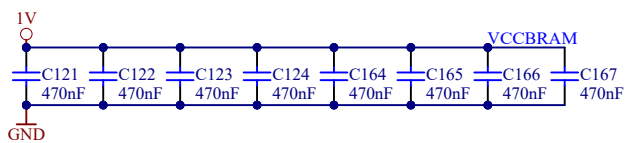
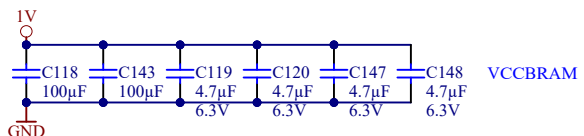
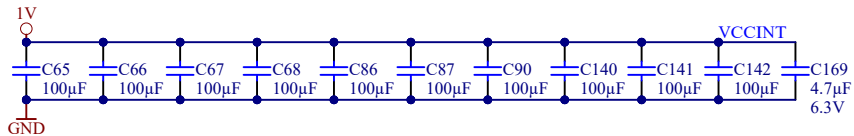
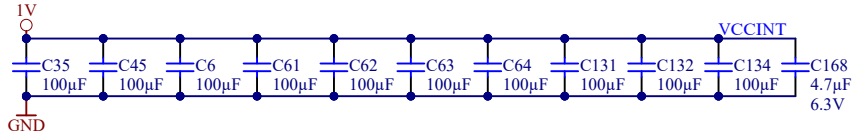


Title: <b>FPGA B34</b>		
A4	Number: <b>TE0783 92135PA</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>18</b> of <b>32</b>
Filename: <b>B34.SchDoc</b>		

Title: <b>FPGA B35</b>		
A4	Number: <b>TE0783 92135PA</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>19</b> of <b>32</b>
Filename: <b>B35.SchDoc</b>		

Capacitors suitable for XC7Z100



Title: ZYNQ POWER		
A4	Number: TE0783 92135PA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page20 of 32
Filename: FPGA-PWR.SchDoc		

A

A

B

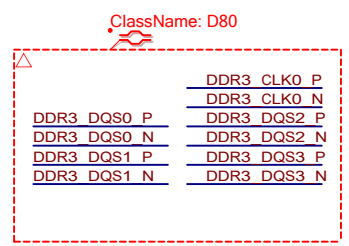
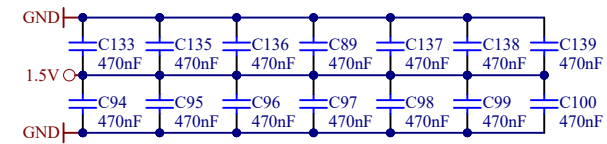
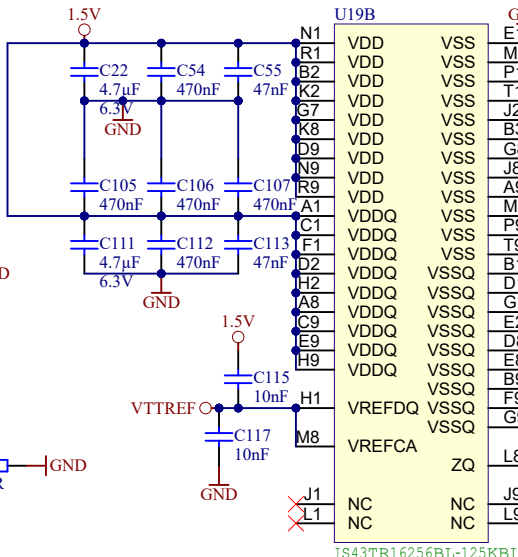
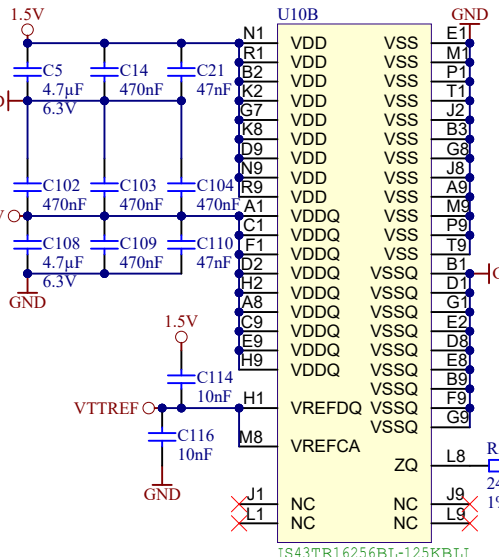
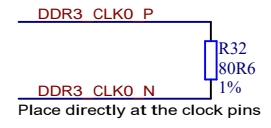
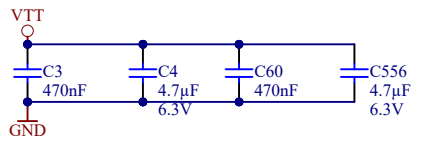
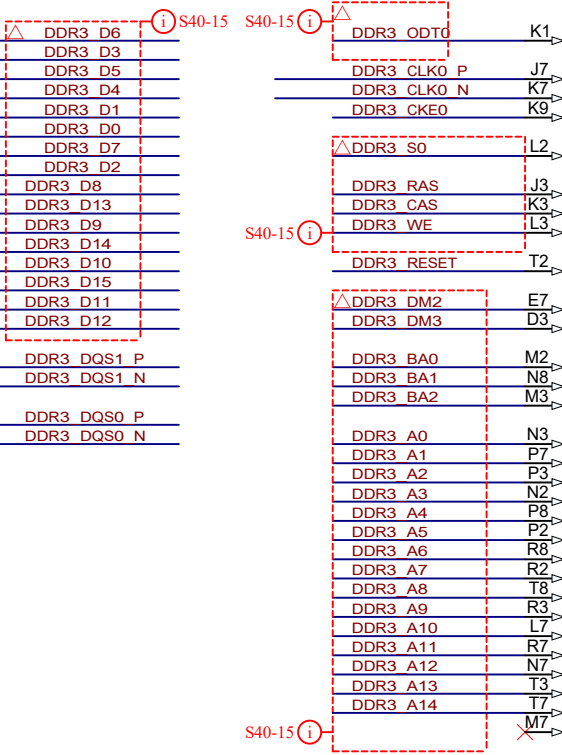
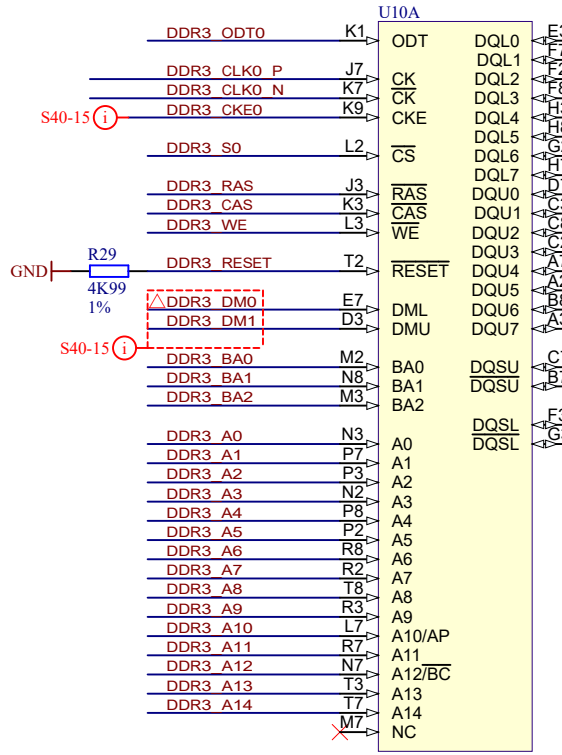
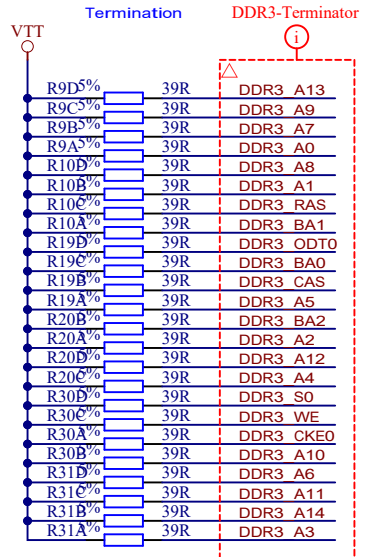
B

C

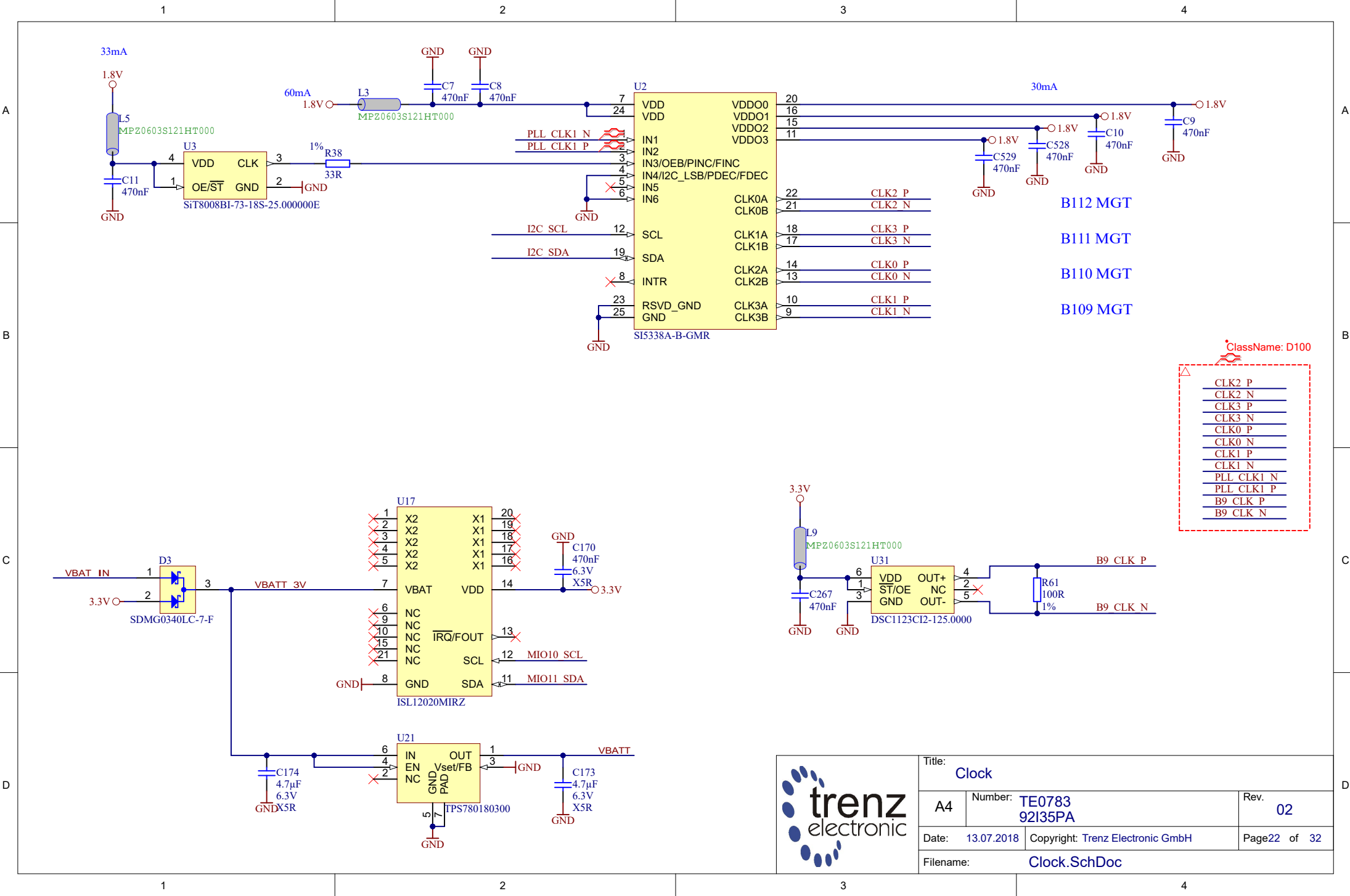

C

D

D



Title: <b>DDR3 RAM PS</b>		
A4	Number: <b>TE0783 92135PA</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>21</b> of <b>32</b>
Filename: <b>DDR3-RAM.SchDoc</b>		

Title: <b>Clock</b>		
A4	Number: <b>TE0783 92135PA</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>22</b> of <b>32</b>
Filename: <b>Clock.SchDoc</b>		

1

2

3

4

A

A

B

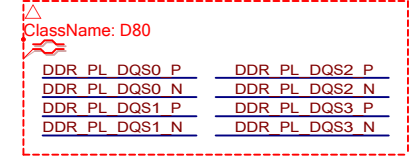
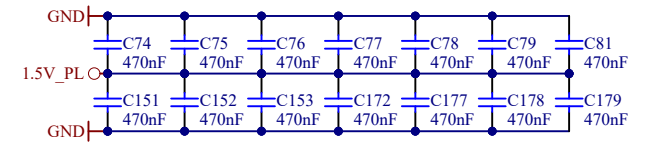
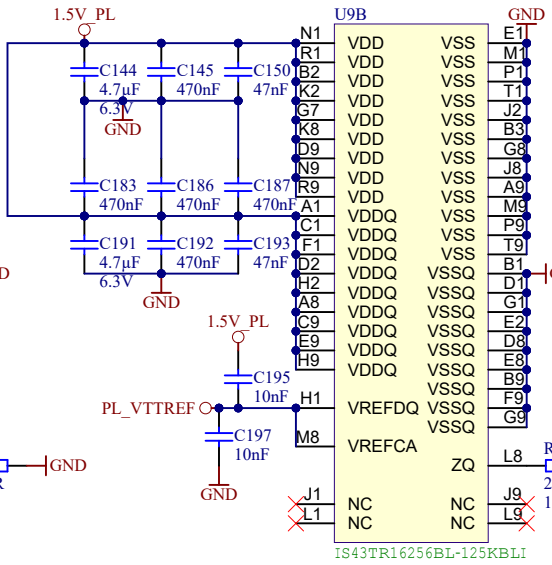
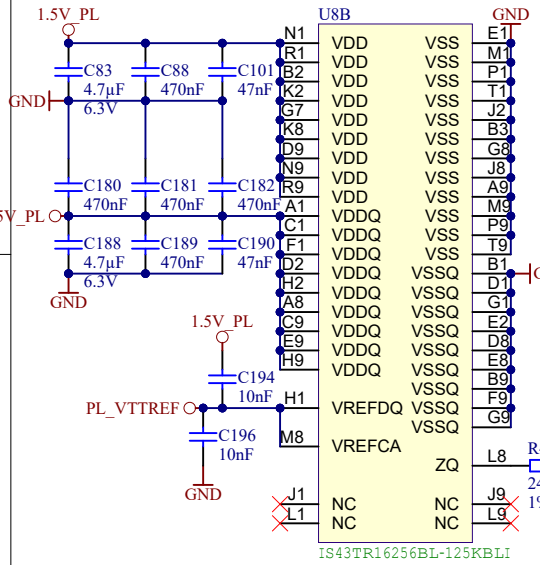
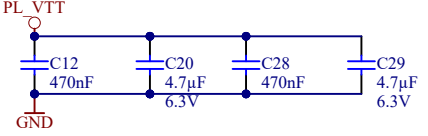
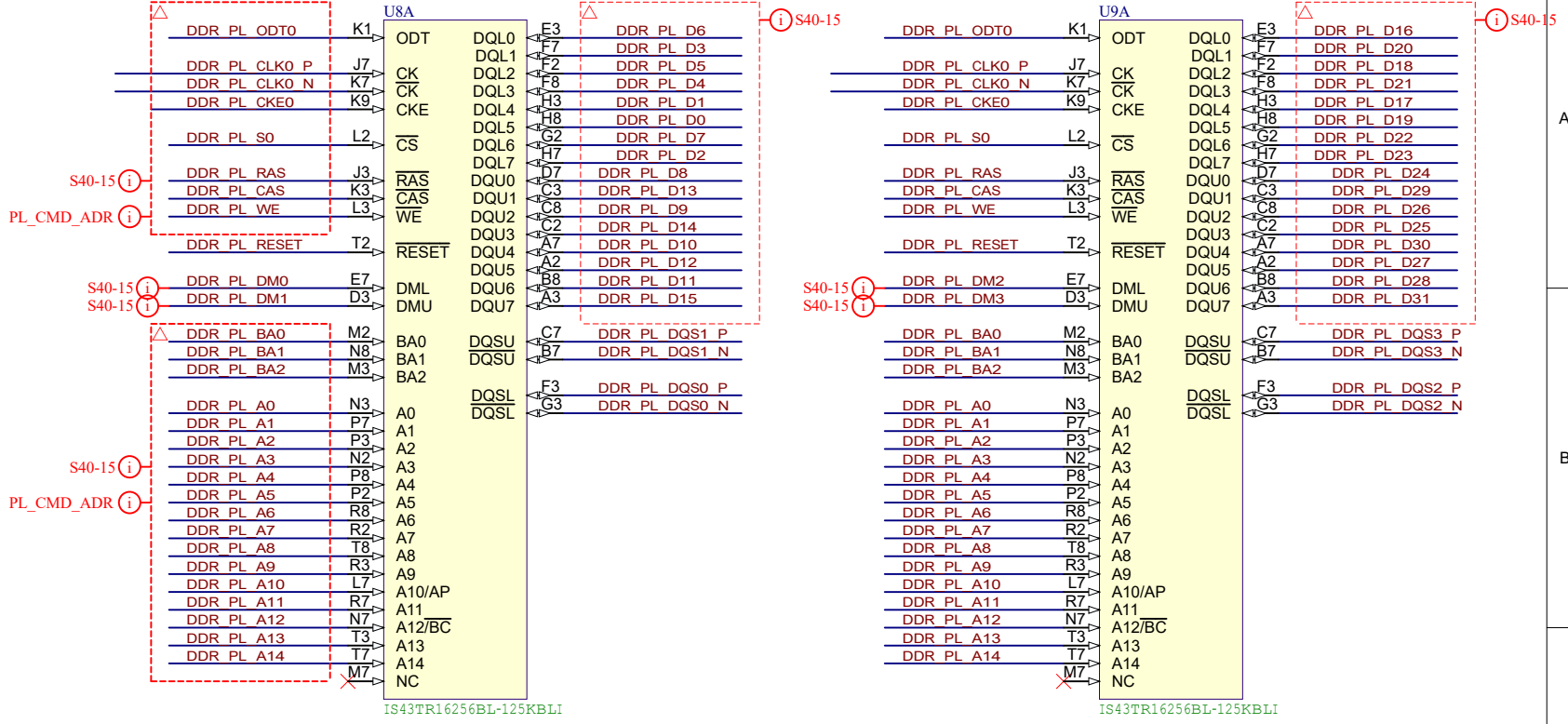
B

C

C

D

D



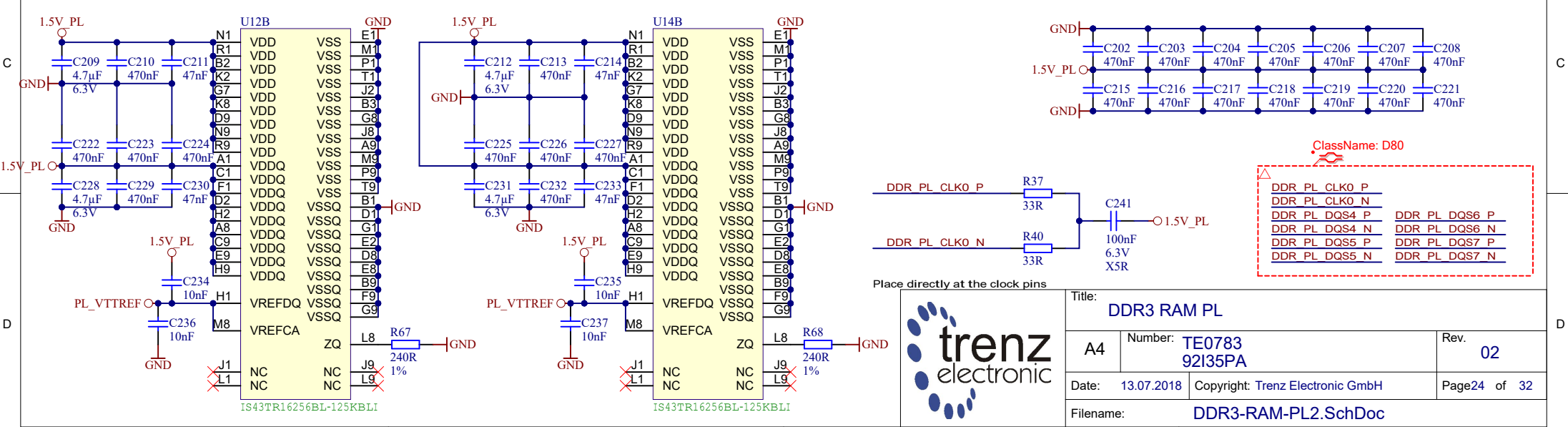
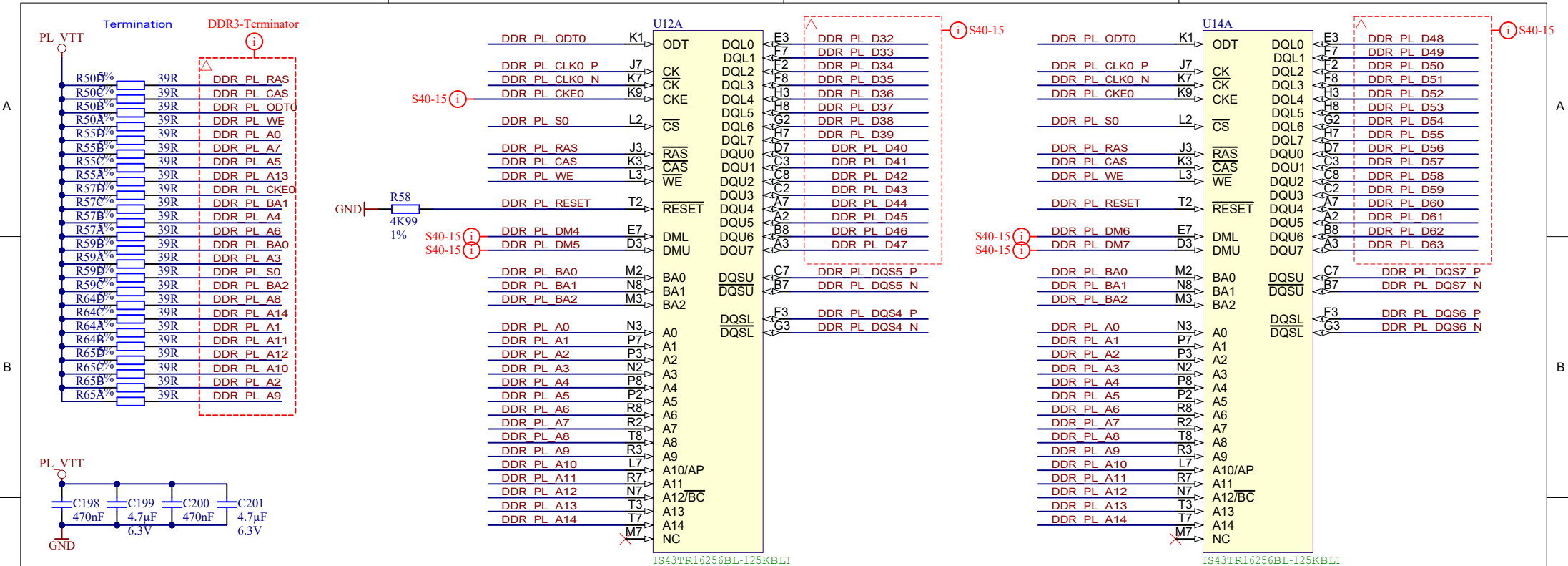
Title: <b>DDR3 RAM PL</b>		
A4	Number: <b>TE0783 92I35PA</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>23</b> of <b>32</b>
Filename: <b>DDR3-RAM-PL1.SchDoc</b>		

1

2

3

4



Title: <b>DDR3 RAM PL</b>		
A4	Number: <b>TE0783 92135PA</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>24</b> of <b>32</b>
Filename: <b>DDR3-RAM-PL2.SchDoc</b>		



A

B

C

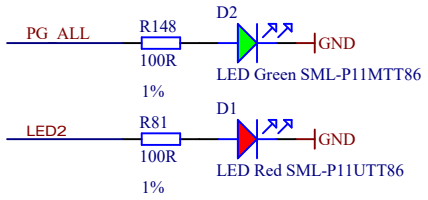
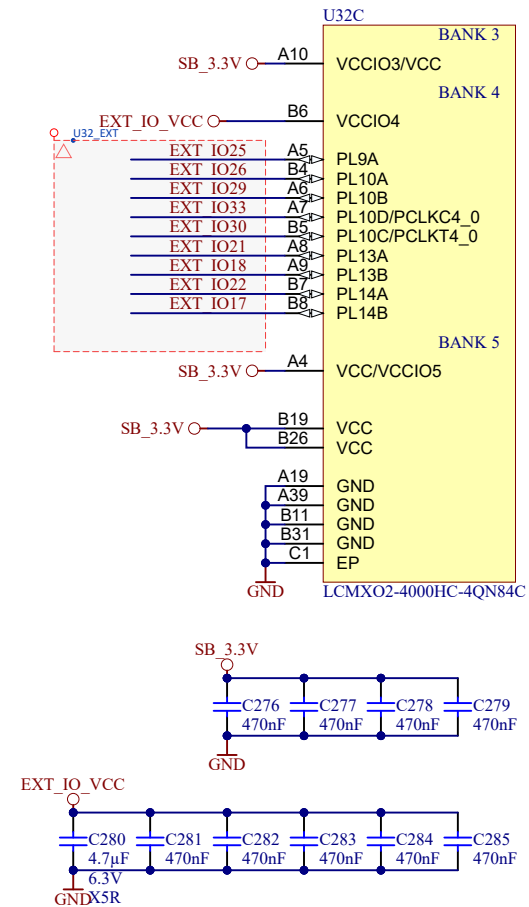
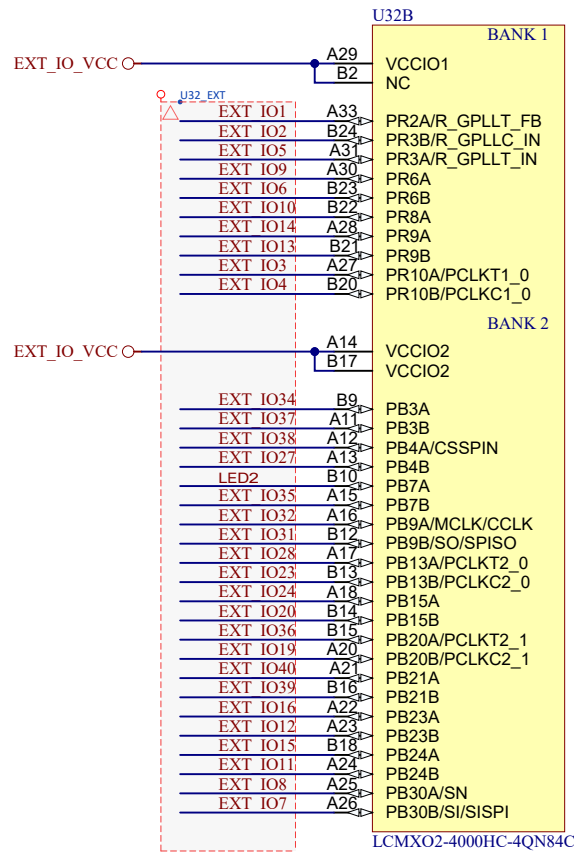
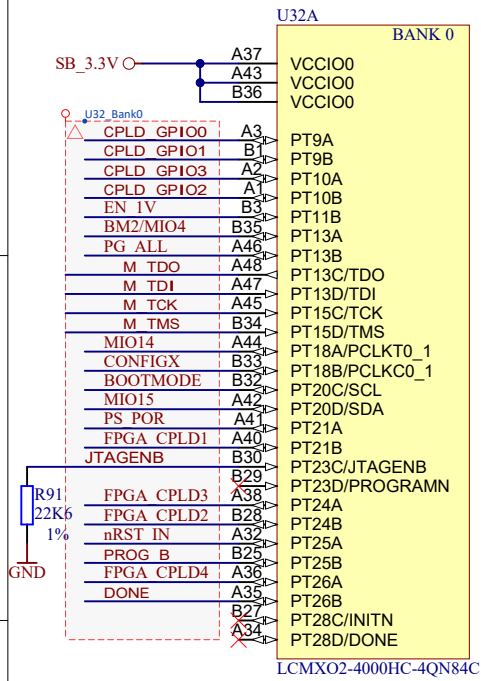
D

A

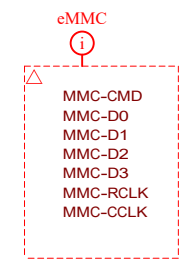
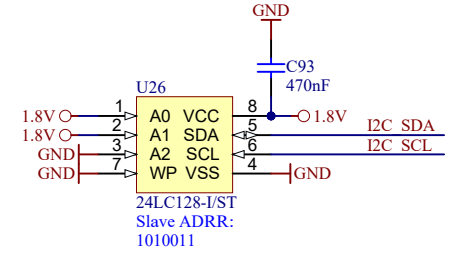
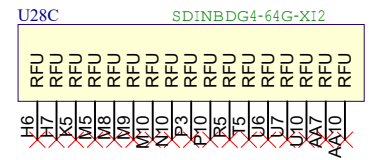
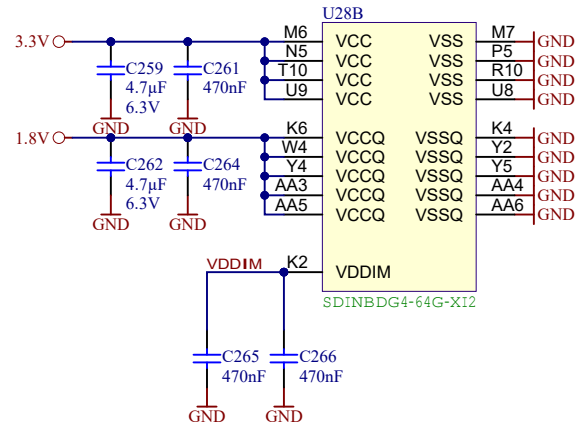
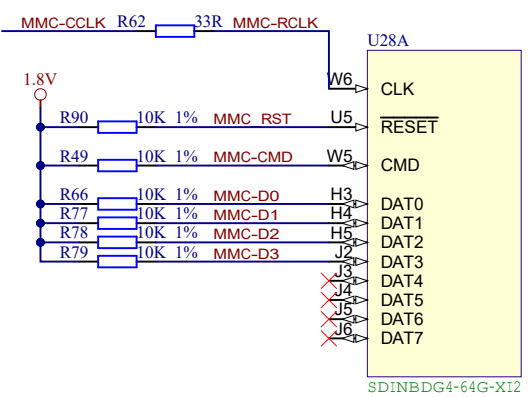
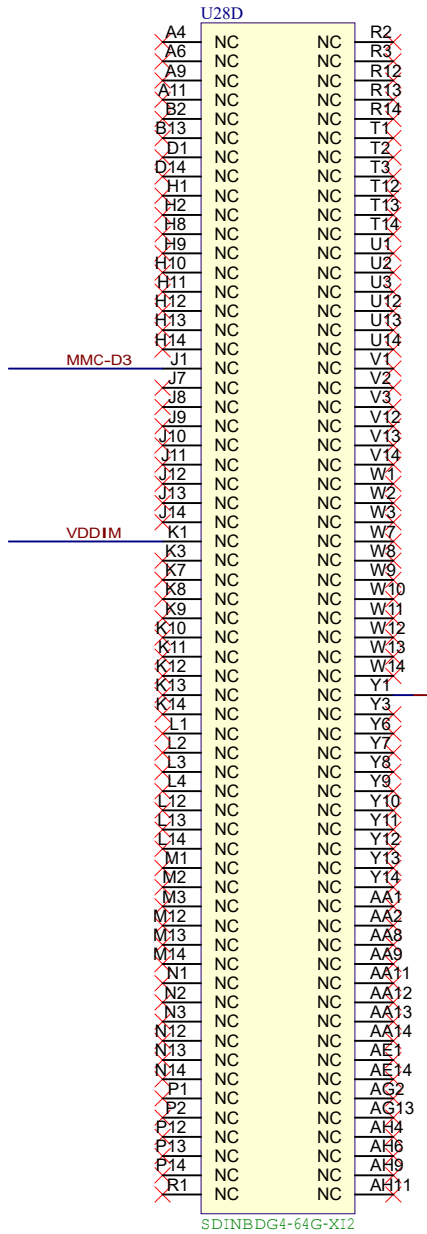
B

C

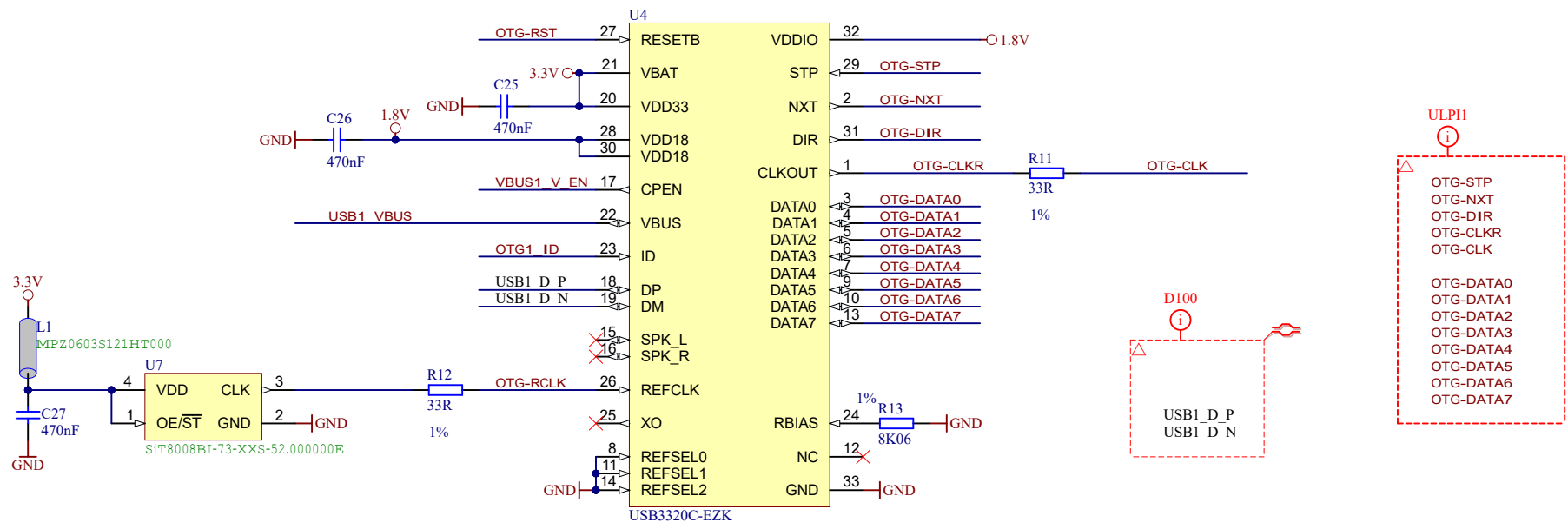
D




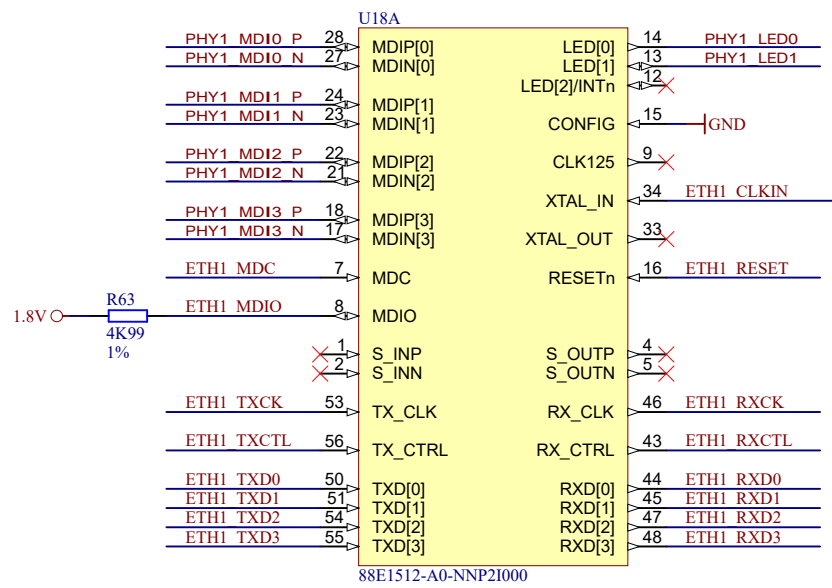
Title: CPLD		
A4	Number: TE0783 92135PA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 25 of 32
Filename: CPLD.SchDoc		



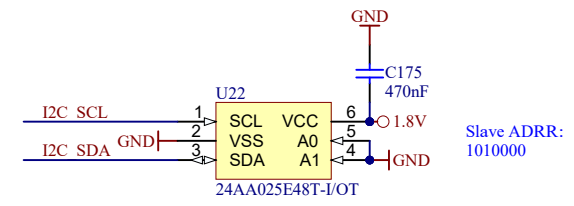
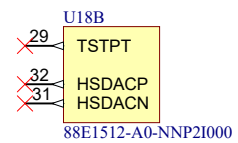
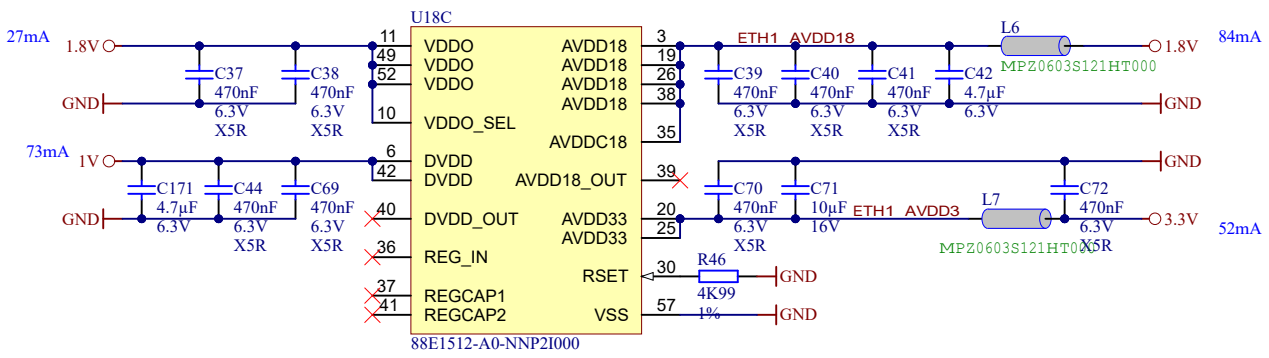
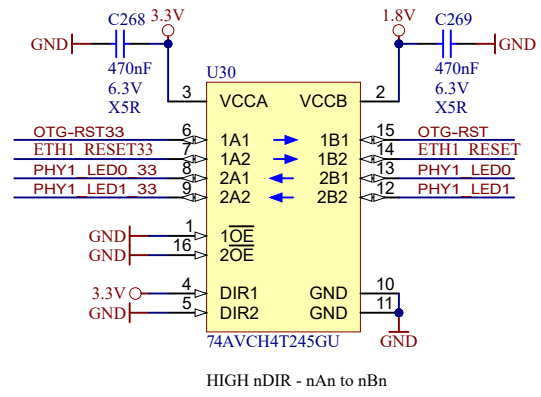
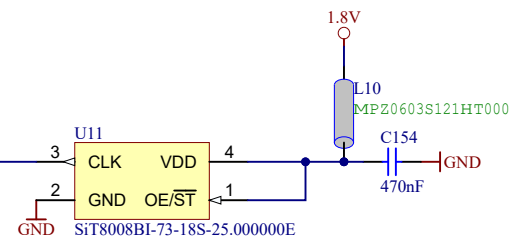
Title: eMMC		
A4	Number: TE0783 92135PA	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page 26 of 32
Filename: eMMC.SchDoc		



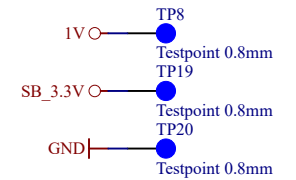
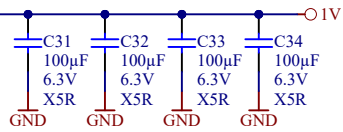
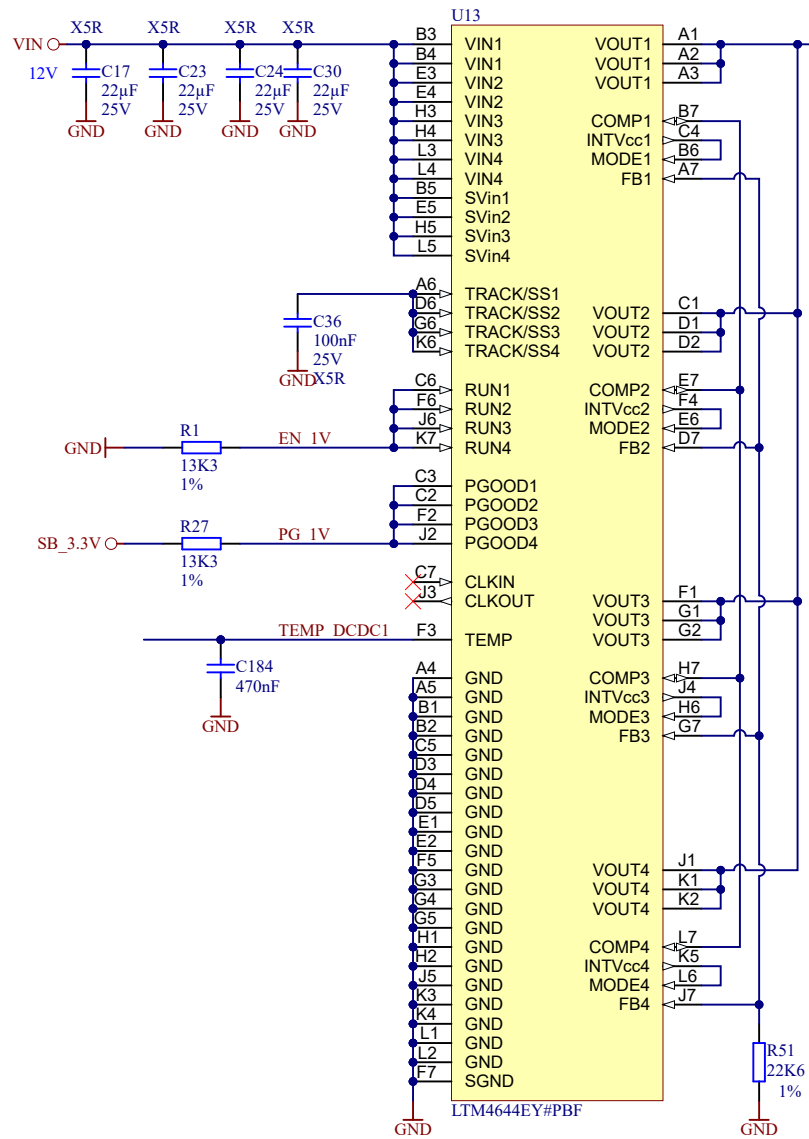
			Title: USB-PHY	
			A4	Number: TE0783 92135PA
Date: 13.07.2018		Copyright: Trenz Electronic GmbH		Page 27 of 32
Filename: USB-PHY.SchDoc				



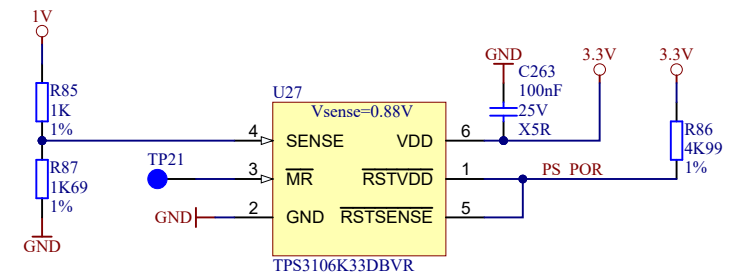
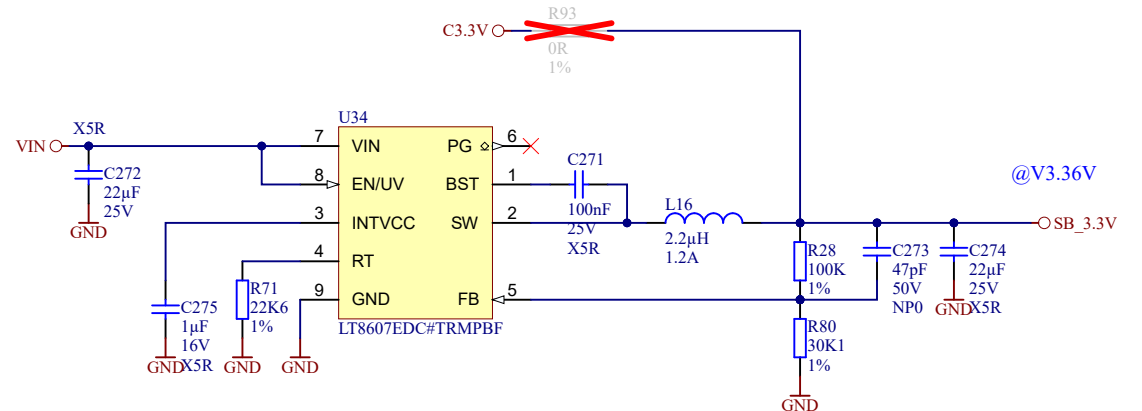
B9



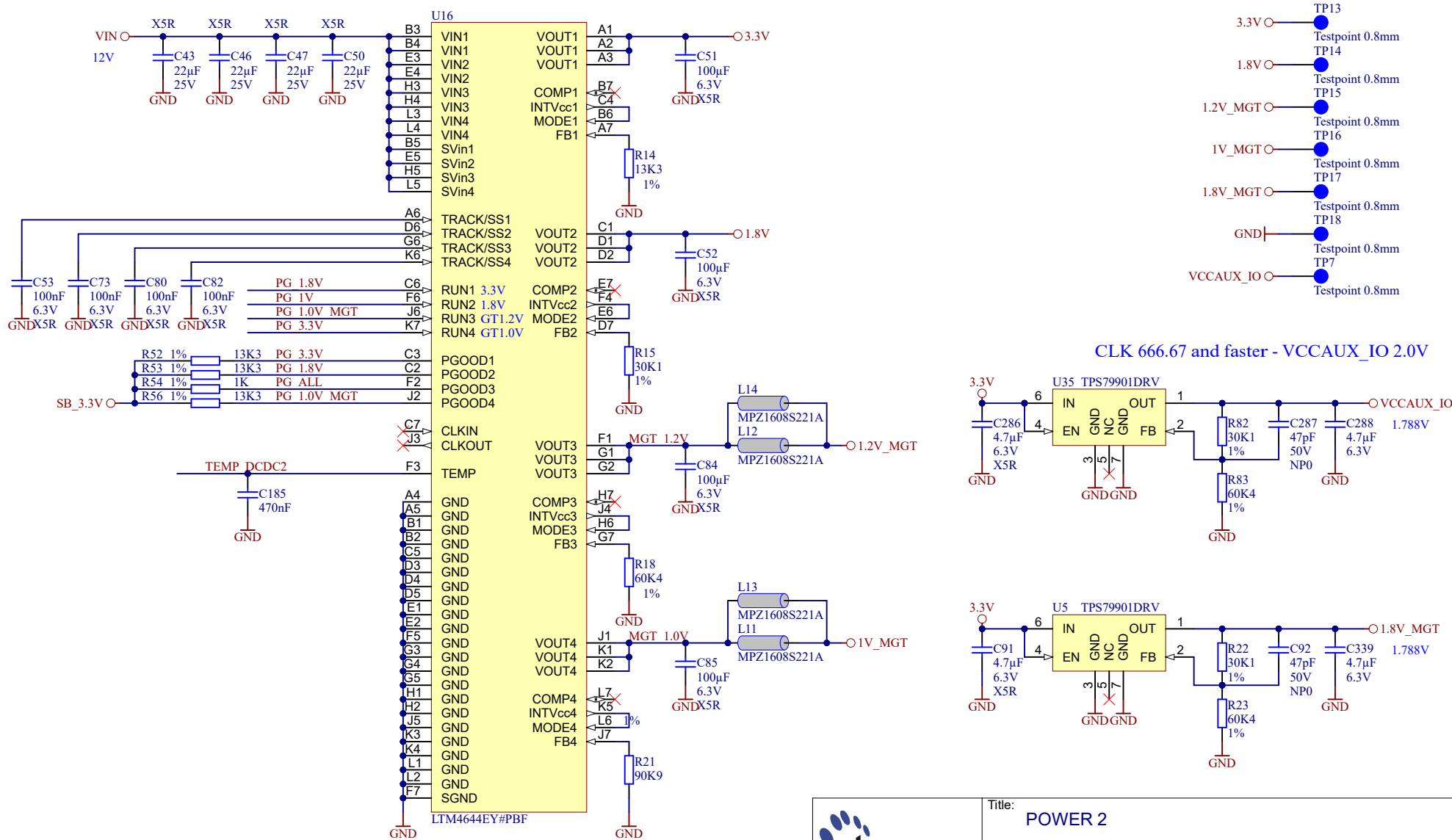
Title: <b>ETH_PHY1</b>		
A4	Number: <b>TE0783 92135PA</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>28</b> of <b>32</b>
Filename: <b>ETH1.SchDoc</b>		



R93: Do not mount when U34 mounted

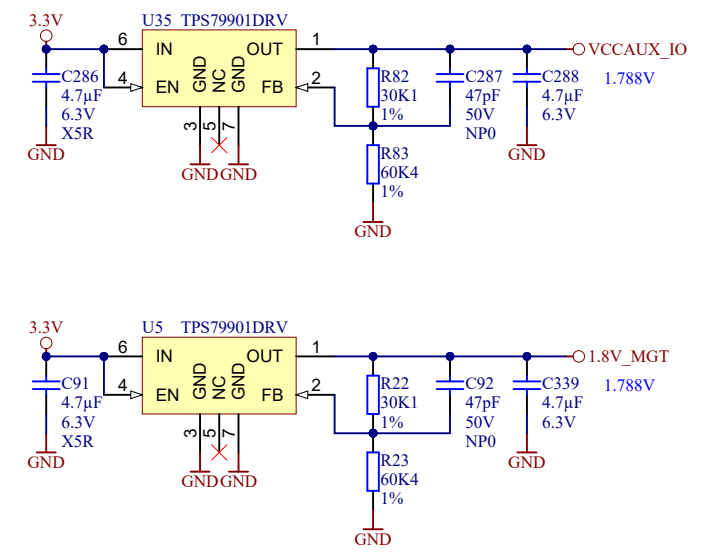


Title: <b>POWER</b>		
A4	Number: <b>TE0783 92I35PA</b>	Rev. <b>02</b>
Date: <b>13.07.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>29</b> of <b>32</b>
Filename: <b>POWER.SchDoc</b>		



- TP13 3.3V Testpoint 0.8mm
- TP14 1.8V Testpoint 0.8mm
- TP15 1.2V\_MGT Testpoint 0.8mm
- TP16 1V\_MGT Testpoint 0.8mm
- TP17 1.8V\_MGT Testpoint 0.8mm
- TP18 GND Testpoint 0.8mm
- TP7 VCCAUX\_IO Testpoint 0.8mm

CLK 666.67 and faster - VCCAUX\_IO 2.0V



		Title: POWER 2	
		A4	Number: TE0783 92I35PA
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Rev. 02	
Filename: POWER2.SchDoc		Page 30 of 32	

1

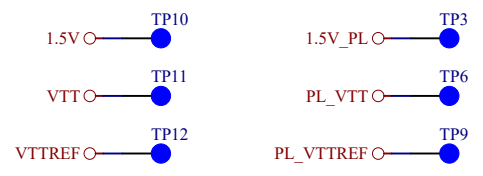
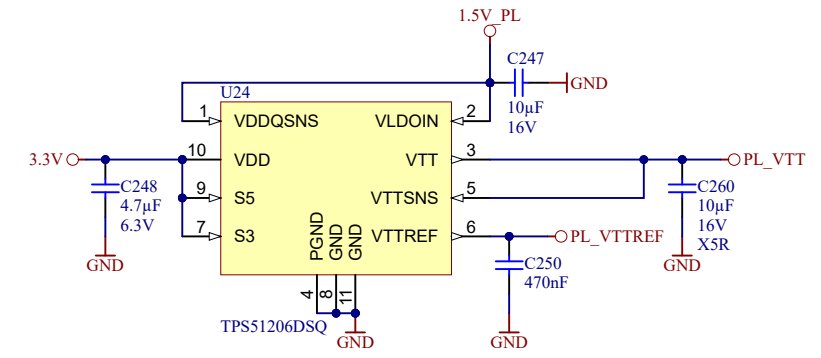
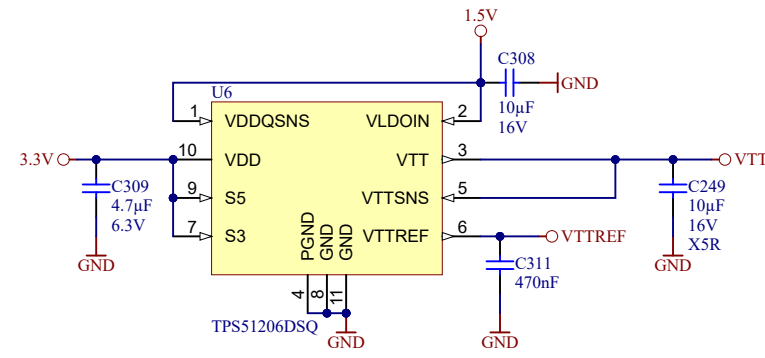
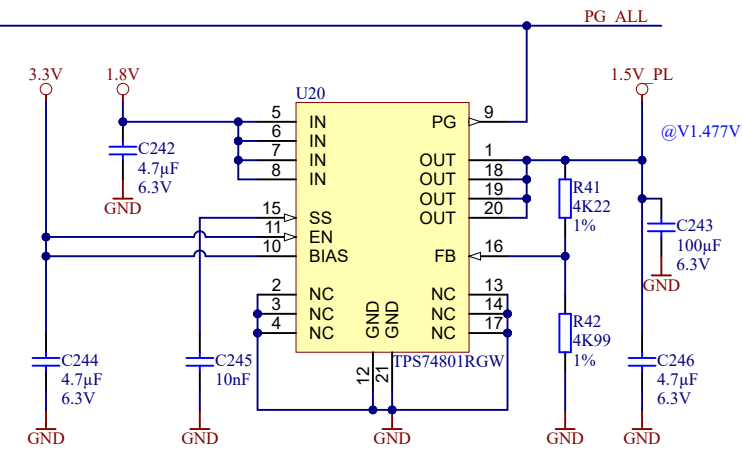
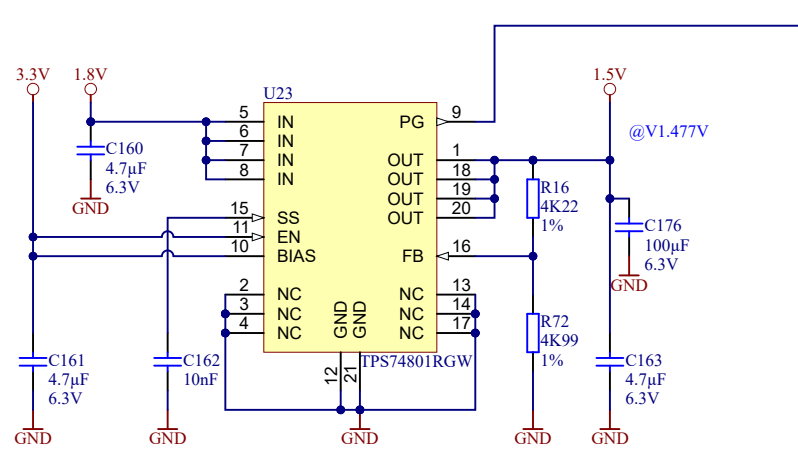
2

3

4

### DDR3 PS

### DDR3 PL



	Title: <b>POWER 2</b>	
	A4	Number: <b>TE0783 92135PA</b>
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH
	Rev. <b>02</b>	Page 31 of 32
Filename: <b>POWER3.SchDoc</b>		

1

2

3

4

1

2

3

4

REV. 02:

1) Changed power-up sequence: 3.3V next to 1.8V. MGT power domain next to 3.3V

A

A

B


B

C

C

D

D

	Title: Revision Changes		
	A4	Number: TE0783 92I35PA	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH / TT	Page 32 of 32
	Filename: Revision Changes.SchDoc		

1

2

3

4