U_SOC
SOC.SchDoc

U_DDR3-RAM
DDR3-RAM.SchDoc

U_CPLD
CPLD.SchDoc

U_USB-PHY
USB-PHY.SchDoc

U_ETH1
ETH1.SchDoc

U_Clock
Clock.SchDoc

U_eMMC
eMMC.SchDoc

U_POWER2
POWER2.SchDoc

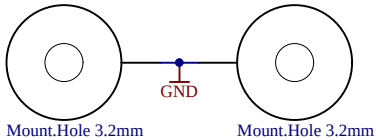
U_Connectors
Connectors.SchDoc

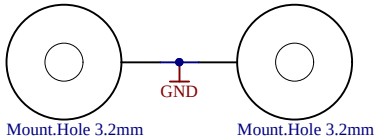
U_Rev_changes
Revision Changes.SchDoc

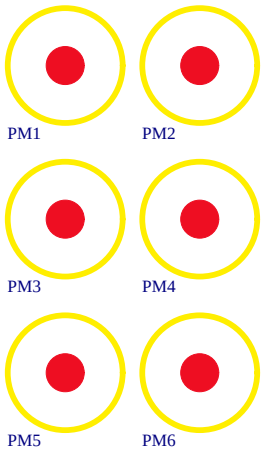
U_POWER
POWER.SchDoc

U_POWER3
POWER3.SchDoc

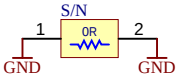
LOGO1
TE Logo PRINT Layer
LOGO PRINT







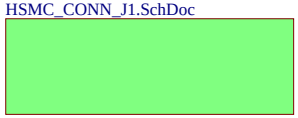
Serial
Serial
Serialnumber 6,3 x 6.3mm



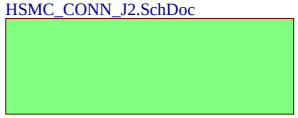
trenz electronic

Title: Overview		
A4	Number: TE0783 Default	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page1 of 32
Filename: TE0783.SchDoc		

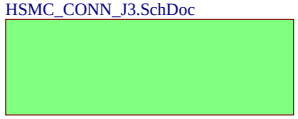
U_HSMC_CONN_J1
HSMC_CONN_J1.SchDoc



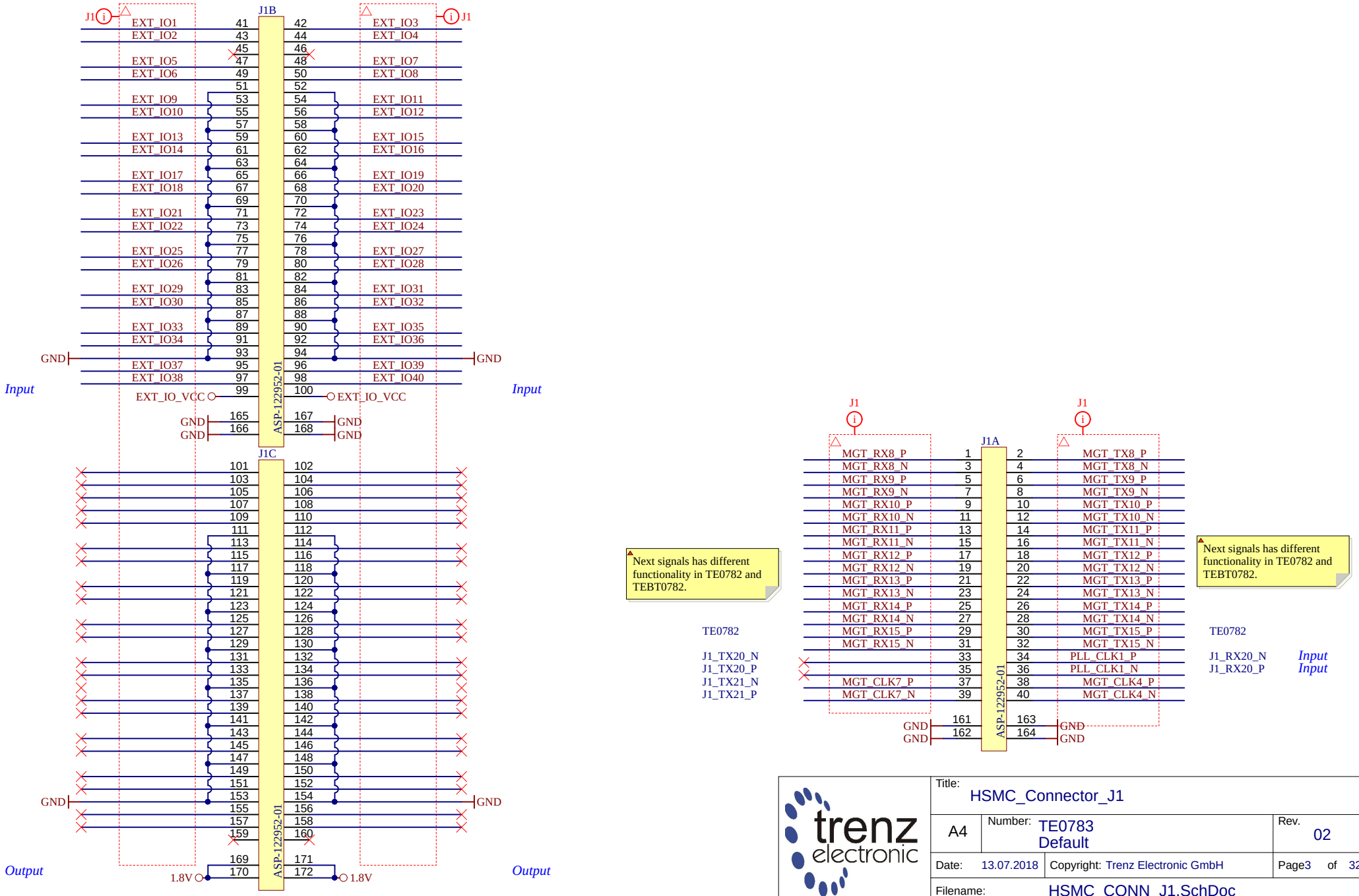
U_HSMC_CONN_J2
HSMC_CONN_J2.SchDoc



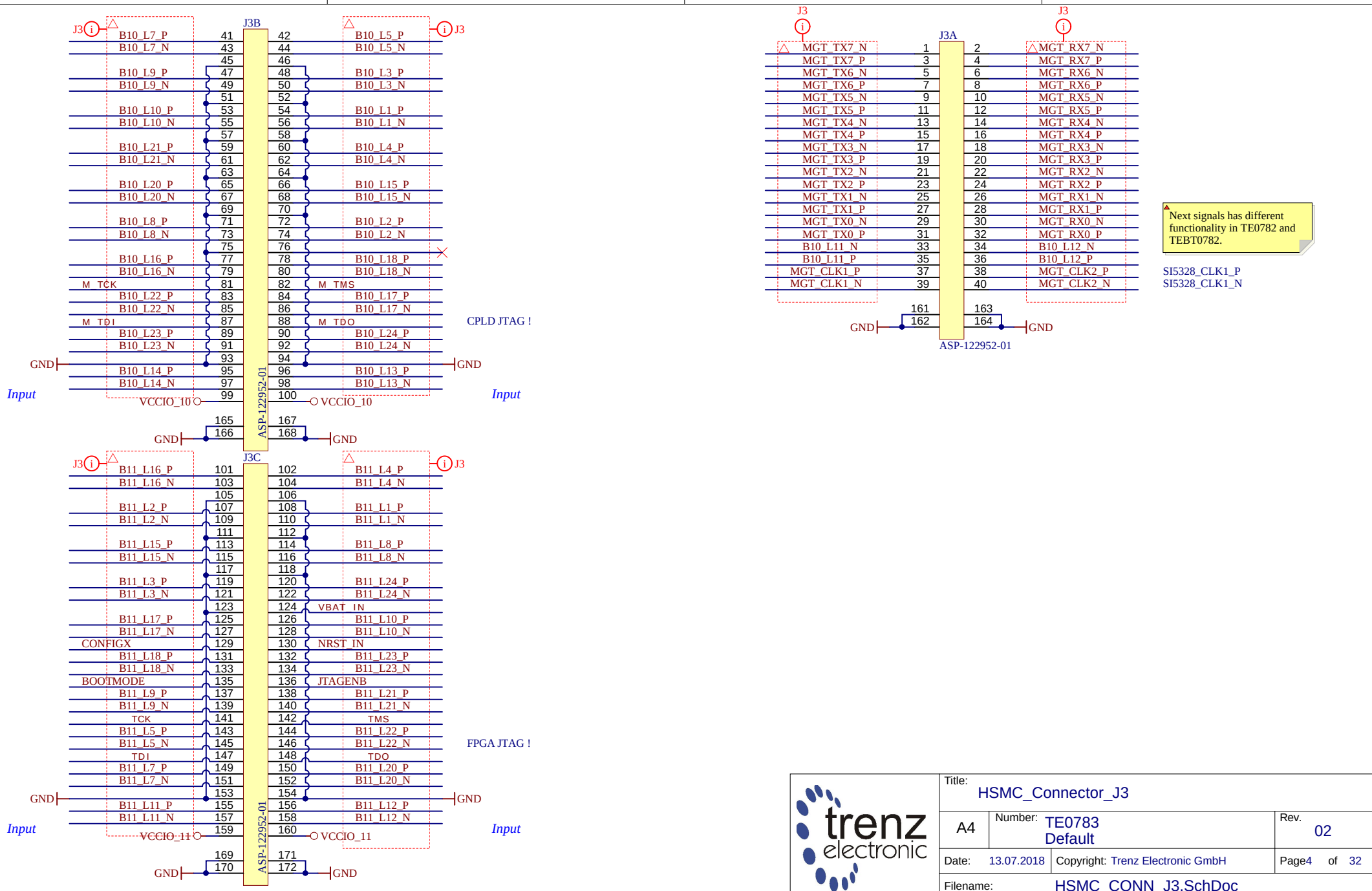
U_HSMC_CONN_J3
HSMC_CONN_J3.SchDoc



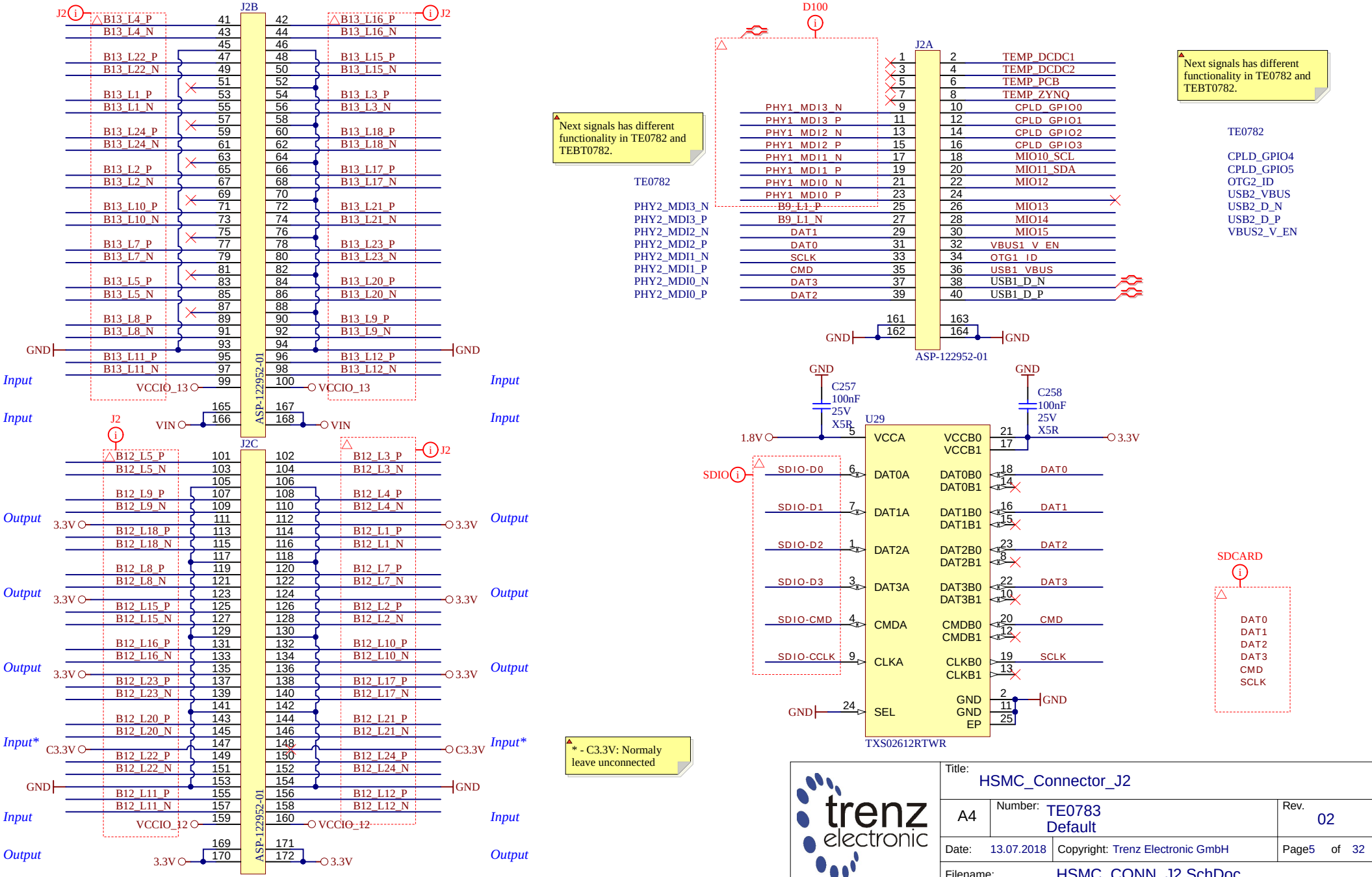
trenz electronic	Title: Connectors		
	A4	Number: TE0783 Default	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page2 of 32
	Filename: Connectors.SchDoc		



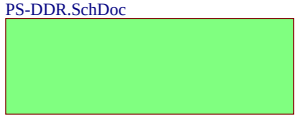
trenz electronic	Title: HSMC_Connector_J1		
A4	Number: TE0783 Default		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page3 of 32
Filename: HSMC_CONN_J1.SchDoc			



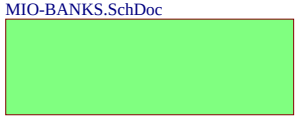
Title: HSMC_Connector_J3			
A4	Number: TE0783 Default		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page4 of 32
Filename: HSMC_CONN_J3.SchDoc			


J2B
J2C
ASP-122952-01
J2A
D100
U29
TXS02612RTWR
SDCARD
Next signals has different functionality in TE0782 and TEBT0782.
TE0782
* - C3.3V: Normaly leave unconnected
Title: HSMC_Connector_J2
A4
Number: TE0783 Default
Rev. 02
Date: 13.07.2018
Copyright: Trenz Electronic GmbH
Page5 of 32
Filename: HSMC_CONN_J2.SchDoc

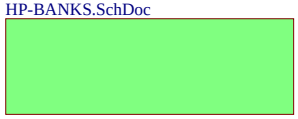
U_PS-DDR
PS-DDR.SchDoc



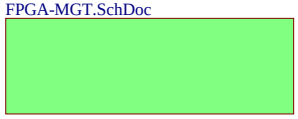
U_MIO-BANKS
MIO-BANKS.SchDoc



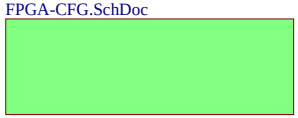
U_HP-BANKS
HP-BANKS.SchDoc



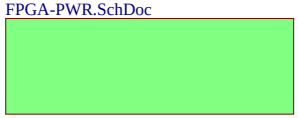
U_FPGA-MGT
FPGA-MGT.SchDoc



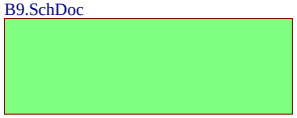
U_FPGA-CFG
FPGA-CFG.SchDoc



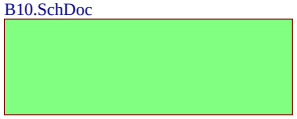
U_FPGA-PWR
FPGA-PWR.SchDoc



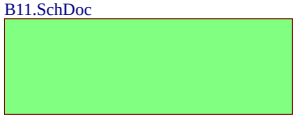
U_B9
B9.SchDoc



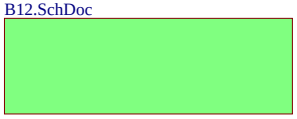
U_B10
B10.SchDoc



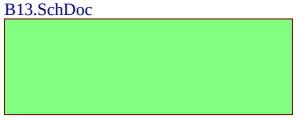
U_B11
B11.SchDoc



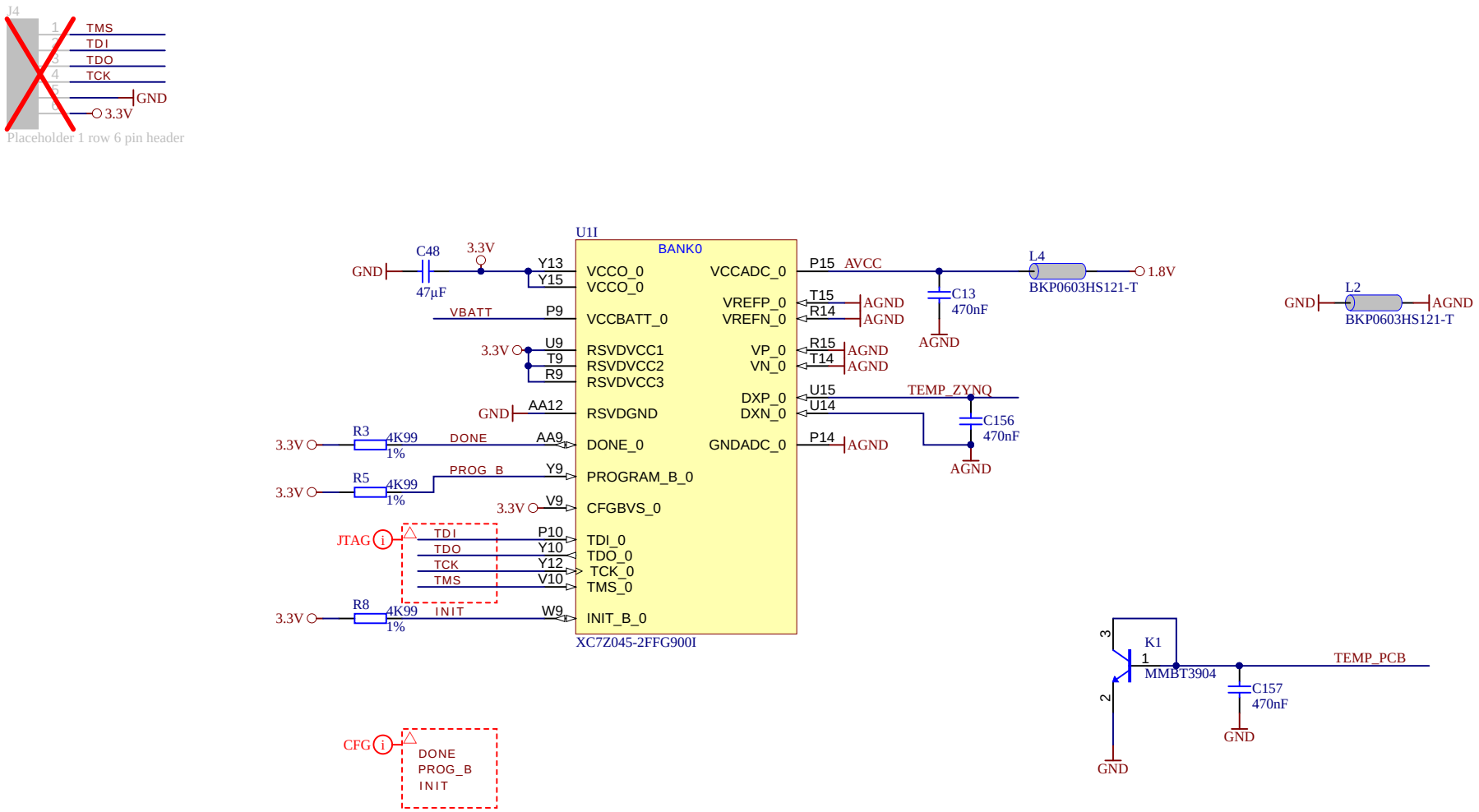
U_B12
B12.SchDoc

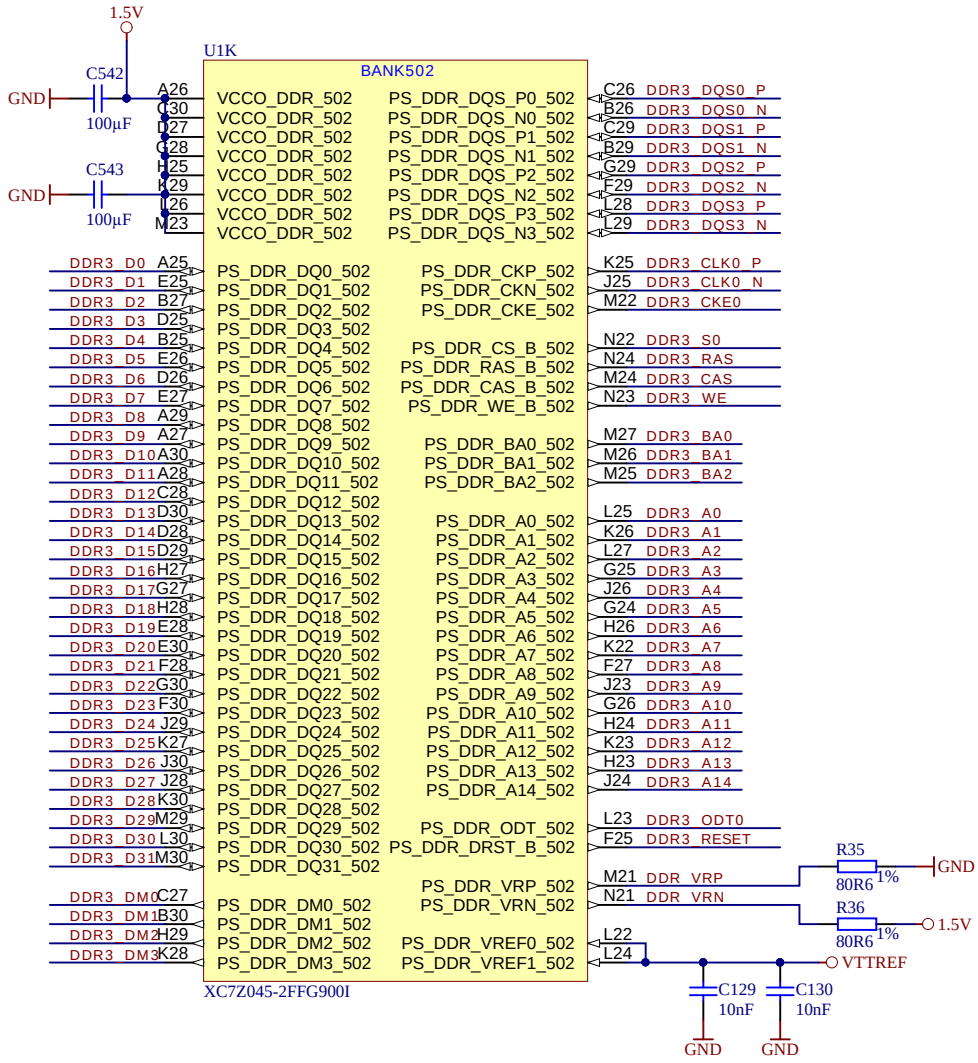


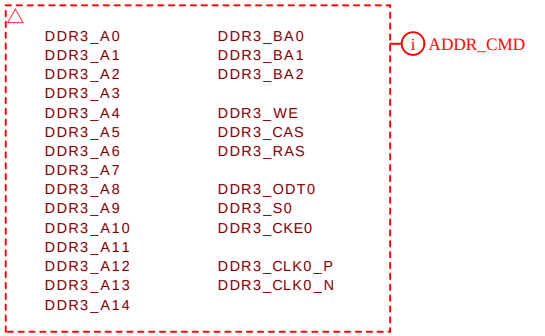
U_B13
B13.SchDoc

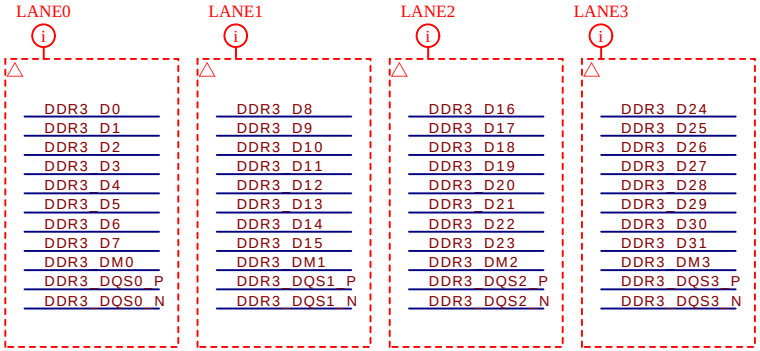


Title: SOC			
A4	Number: TE0783 Default		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page6 of 32
Filename: SOC.SchDoc			


J4
1
2
3
4
5
6
TMS
TDI
TDO
TCK
GND
3.3V
Placeholder 1 row 6 pin header
U1I
BANK0
VCCO_0
VCCO_0
VCCBATT_0
RSVDVCC1
RSVDVCC2
RSVDVCC3
RSVDGND
DONE_0
PROGRAM_B_0
CFGBVS_0
TDI_0
TDO_0
TCK_0
TMS_0
INIT_B_0
VCCADC_0
VREFP_0
VREFN_0
VP_0
VN_0
DXP_0
DXN_0
GNDADC_0
XC7Z045-2FFG900I
C48
47µF
Y13
Y15
VBATT
P9
U9
T9
R9
AA12
R3
4K99
1%
DONE
AA9
R5
PROG_B
Y9
V9
JTAG
P10
Y10
Y12
V10
R8
INIT
W9
CFG
P15
AVCC
T15
R14
R15
T14
U15
U14
P14
C13
470nF
AGND
L4
BKP0603HS121-T
1.8V
TEMP_ZYNQ
C156
K1
MMBT3904
TEMP_PCB
C157
L2
trenz electronic
Title:
FPGA Configuration
A4
Nummer:
TE0783
Default
Rev.
02
Datum:
13.07.2018
Zeichner:
Trenz Electronic GmbH
Blatt 7
von 32
Filename:
FPGA-CFG.SchDoc

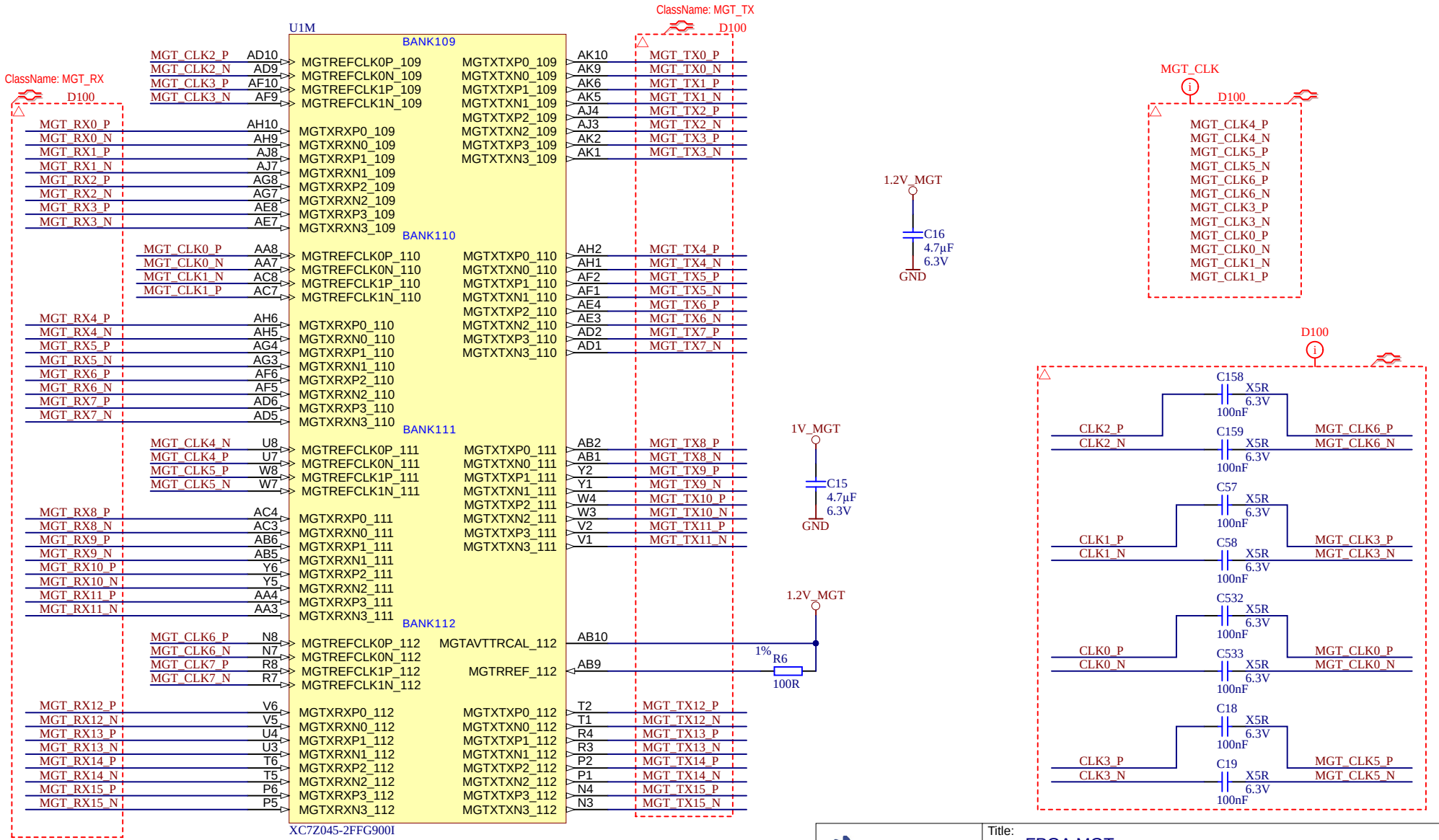




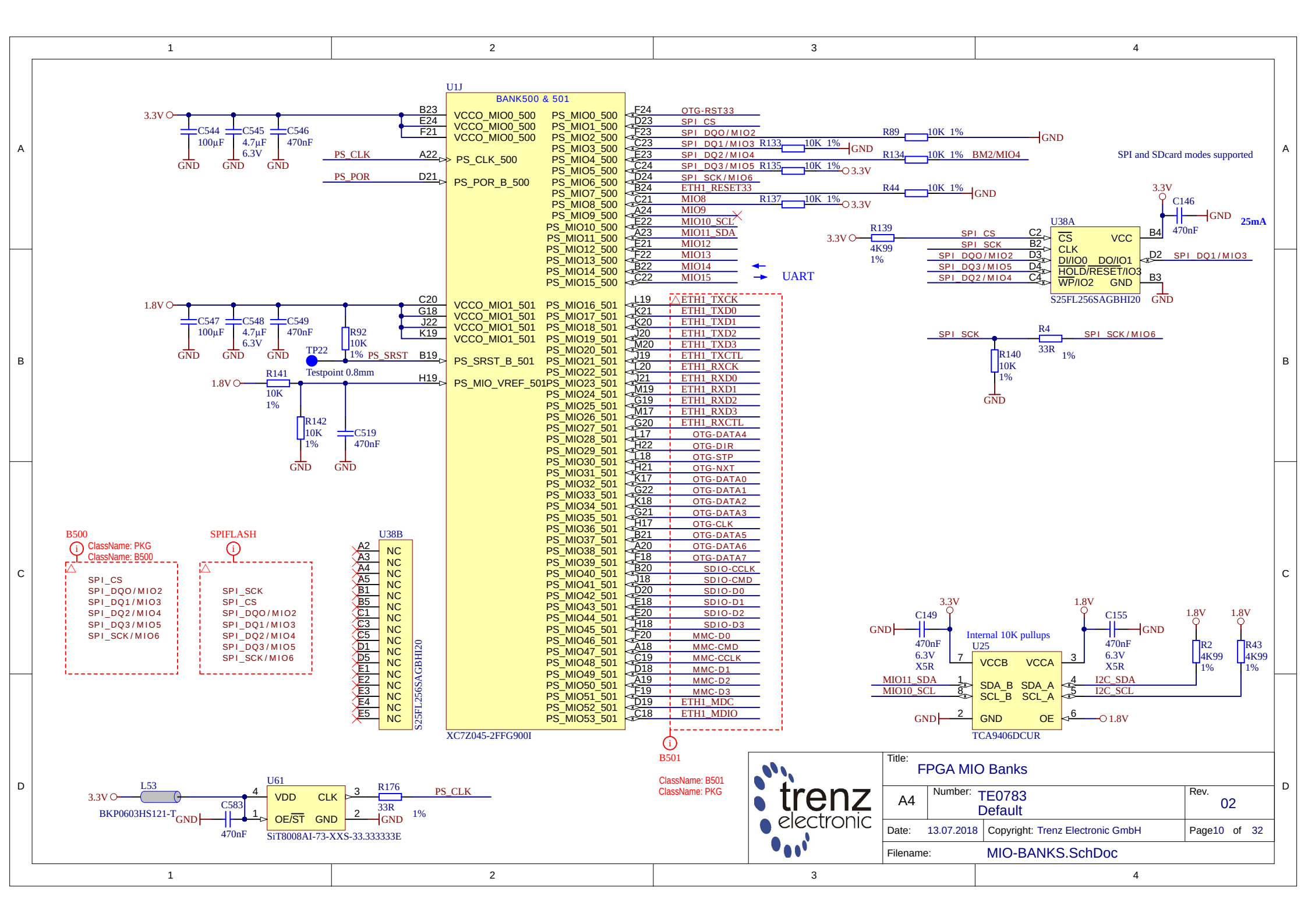


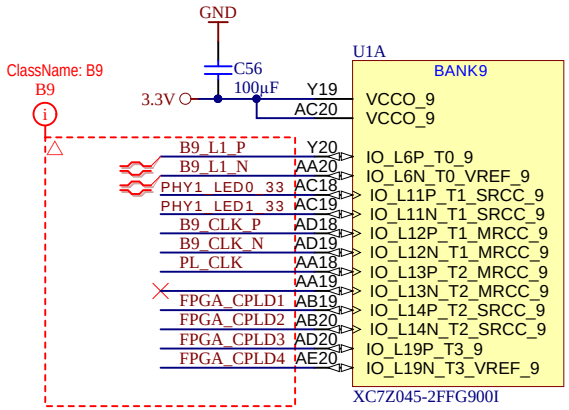
trenz electronic

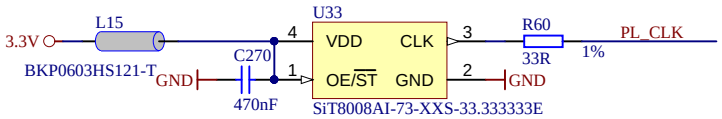
Title: FPGA DDR Banks			
A4	Number: TE0783 Default		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page8 of 32
Filename: PS-DDR.SchDoc			



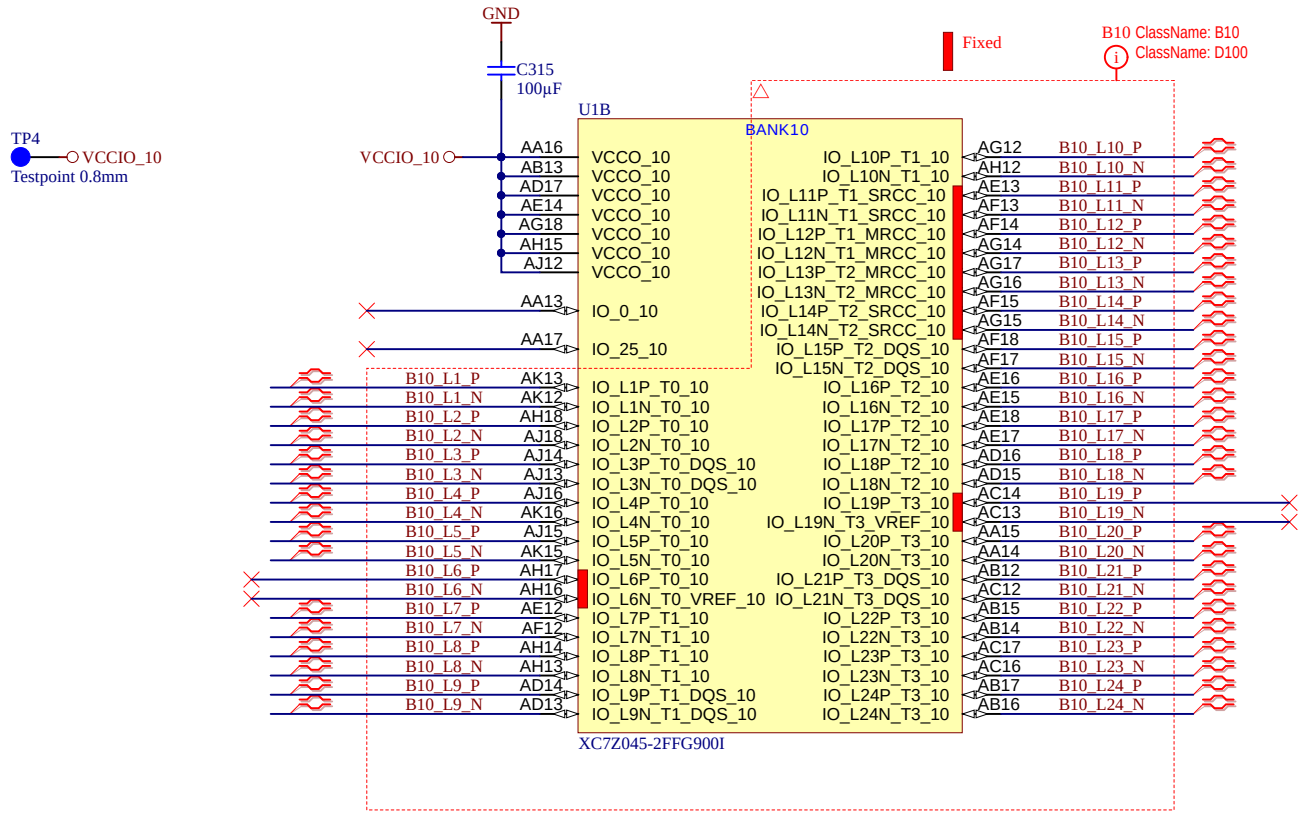
trenz electronic	Title: FPGA MGT		
A4	Number: TE0783 Default		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page9 of 32
Filename: FPGA-MGT.SchDoc			


U1J
BANK500 & 501
XC7Z045-2FFG900I
PS_CLK
PS_POR
PS_SRST
PS_MIO_VREF_501
UART
SPI and SDcard modes supported
U38A
S25FL256SAGBHI20
U38B
S25FL256SAGBHI20
B500
ClassName: PKG
ClassName: B500
SPIFLASH
B501
ClassName: B501
ClassName: PKG
U61
SiT8008AI-73-XXS-33.333333E
BKP0603HS121-T
U25
TCA9406DCUR
Internal 10K pullups
Title: FPGA MIO Banks
A4
Number: TE0783 Default
Rev. 02
Date: 13.07.2018
Copyright: Trenz Electronic GmbH
Page10 of 32
Filename: MIO-BANKS.SchDoc

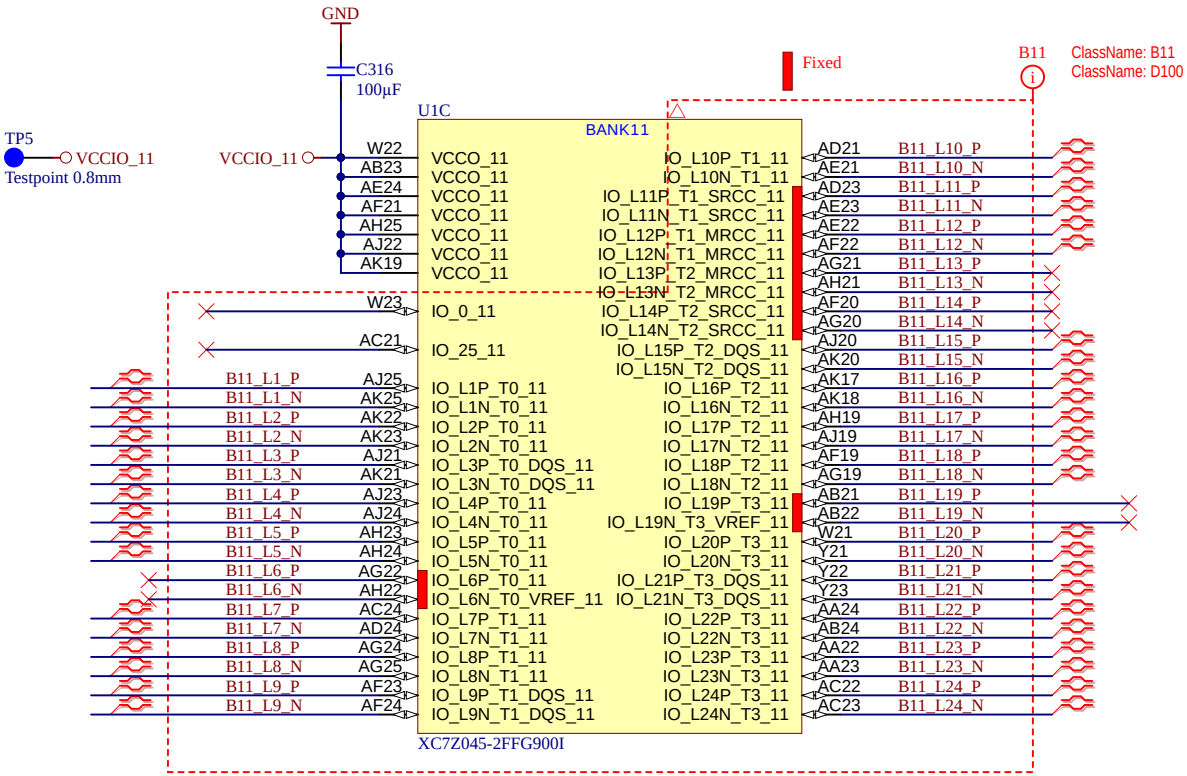




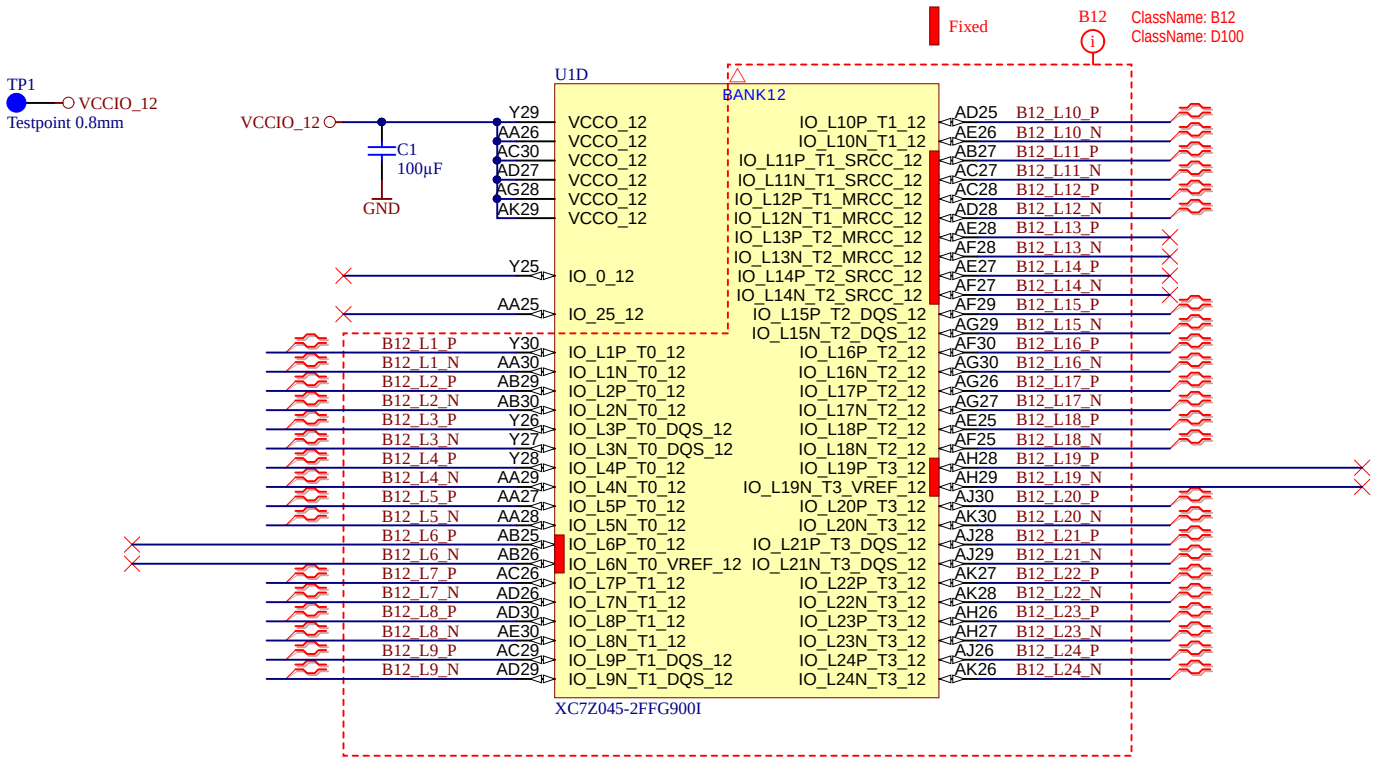
trenz electronic	Title: FPGA B9		
	A4	Number: TE0783 Default	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page11 of 32
	Filename: B9.SchDoc		



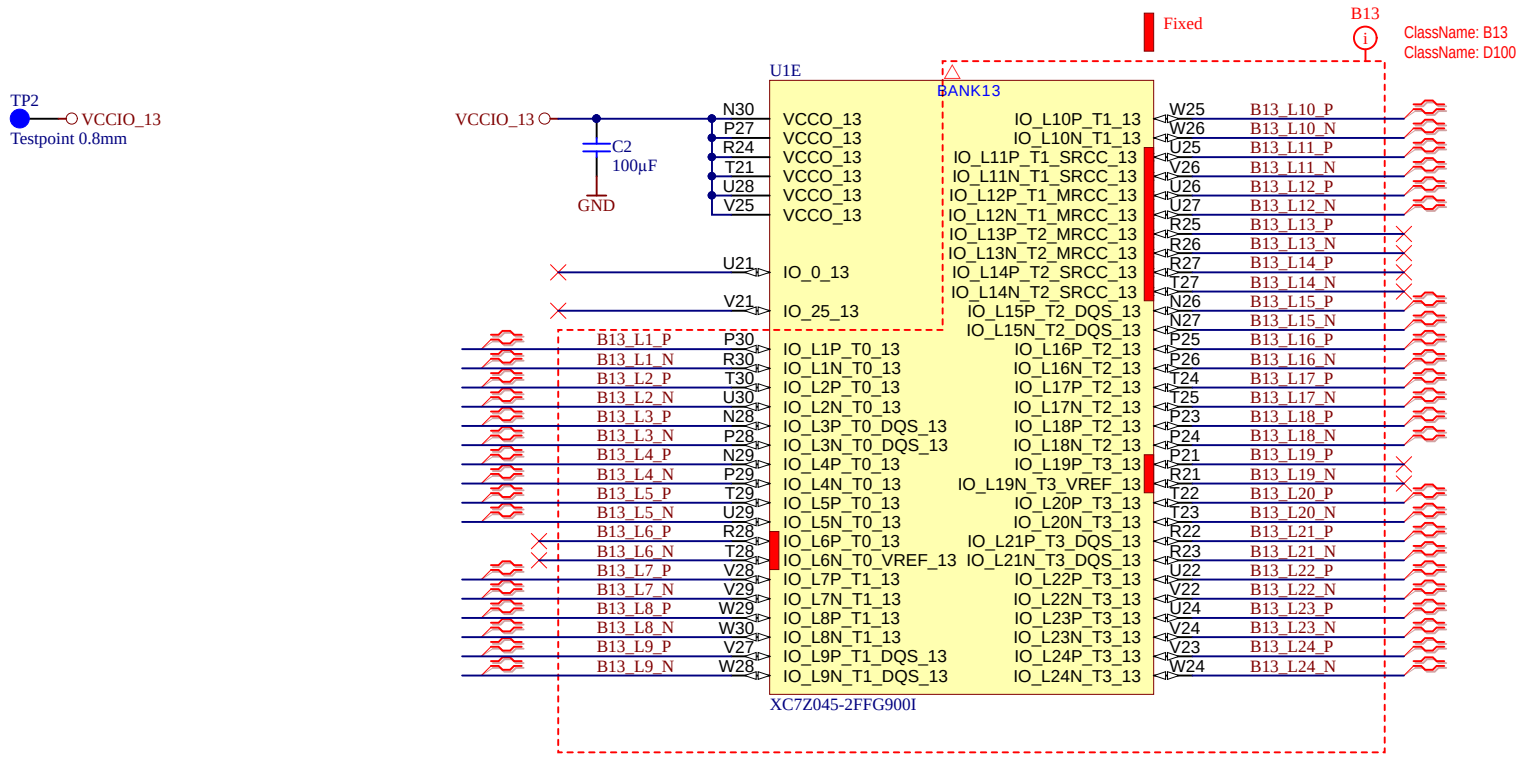
trenz electronic	Title: FPGA B10		
	A4	Number: TE0783 Default	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page12 of 32
	Filename: B10.SchDoc		



trenz electronic	Title: FPGA B11		
	A4	Number: TE0783 Default	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page13 of 32
	Filename: B11.SchDoc		



	Title: FPGA B12		
A4	Number: TE0783 Default		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page14 of 32
Filename: B12.SchDoc			



trenz electronic	Title: FPGA B13		
	A4	Number: TE0783 Default	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page15 of 32
	Filename: B13.SchDoc		

U_B33
B33.SchDoc

U_B34
B34.SchDoc

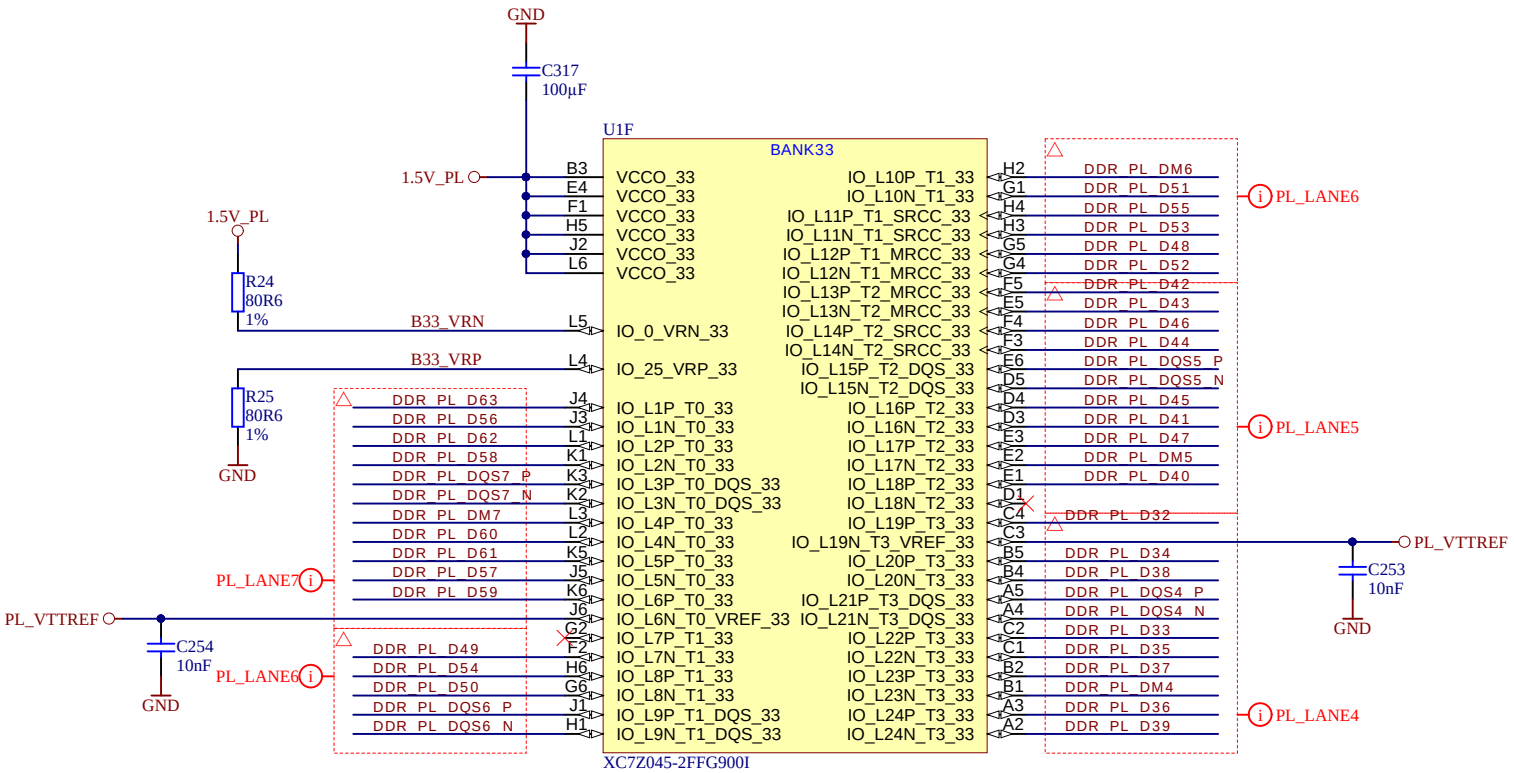
U_B35
B35.SchDoc

U_DDR3-RAM-PL1
DDR3-RAM-PL1.SchDoc

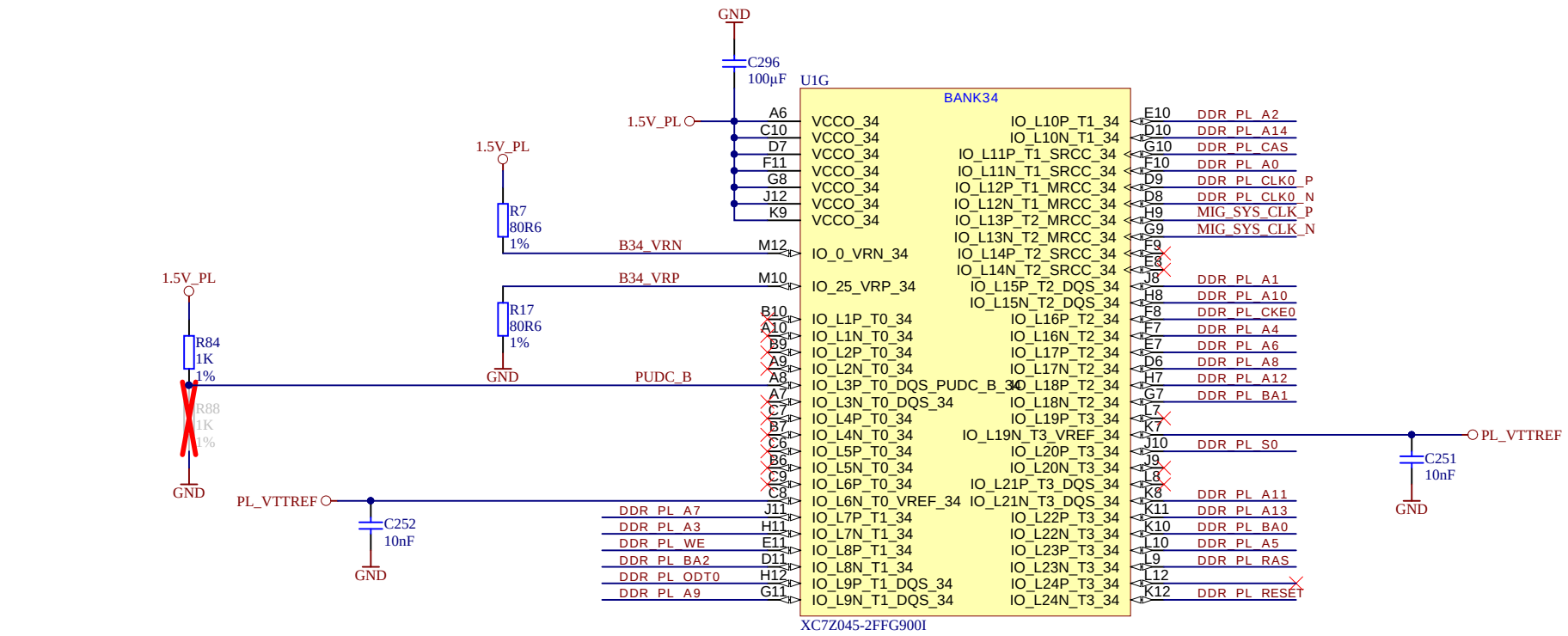
U_DDR3-RAM-PL2
DDR3-RAM-PL2.SchDoc

trenz electronic

Title: FPGA HP Banks		
A4	Number: TE0783 Default	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page16 of 32
Filename: HP-BANKS.SchDoc		

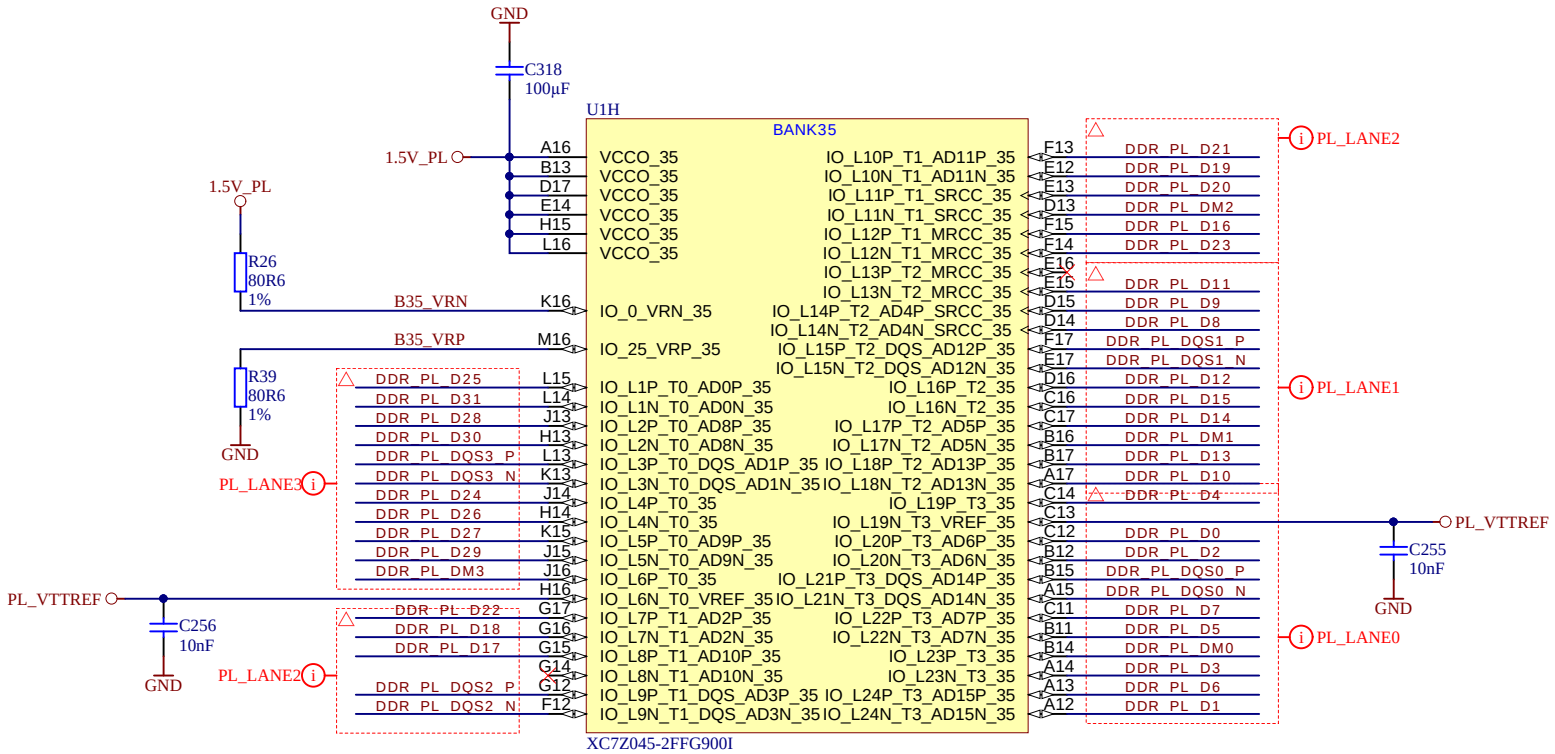


trenz electronic	Title: FPGA B33		
	A4	Number: TE0783 Default	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page17 of 32
	Filename: B33.SchDoc		

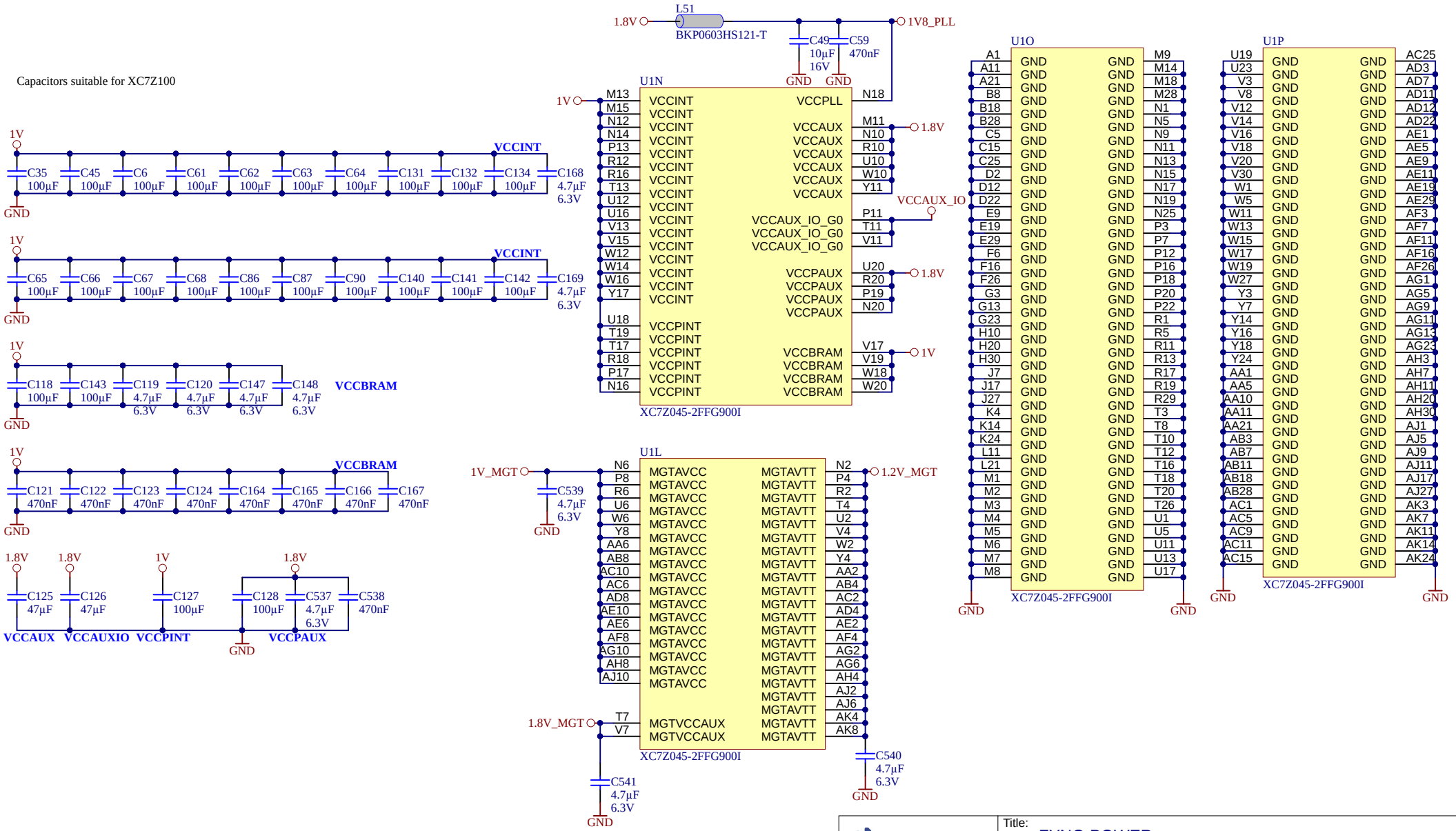


Check clock source. R74 100R changed to 100K

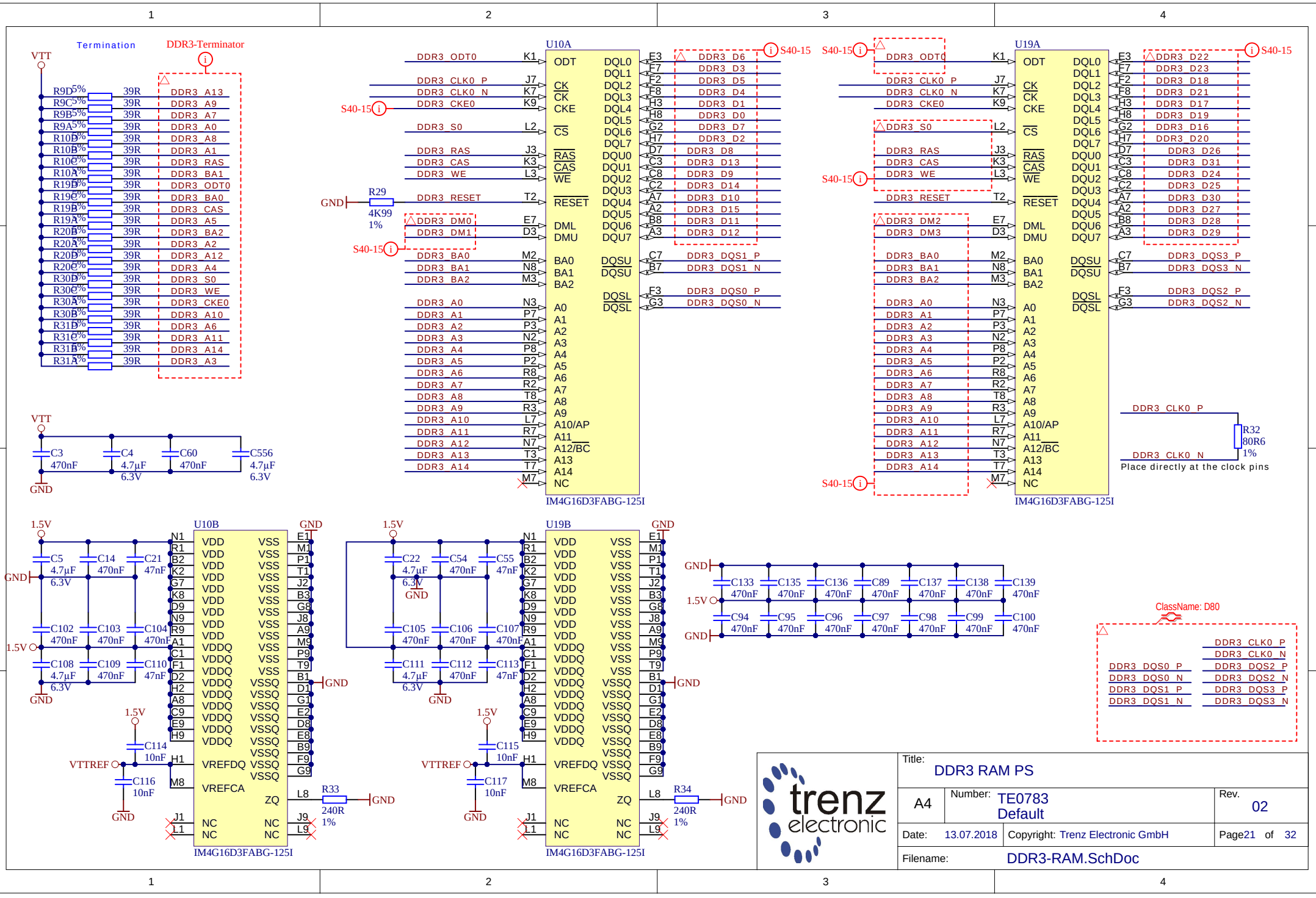
Title: FPGA B34			
A4	Number: TE0783 Default		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page18 of 32
Filename: B34.SchDoc			

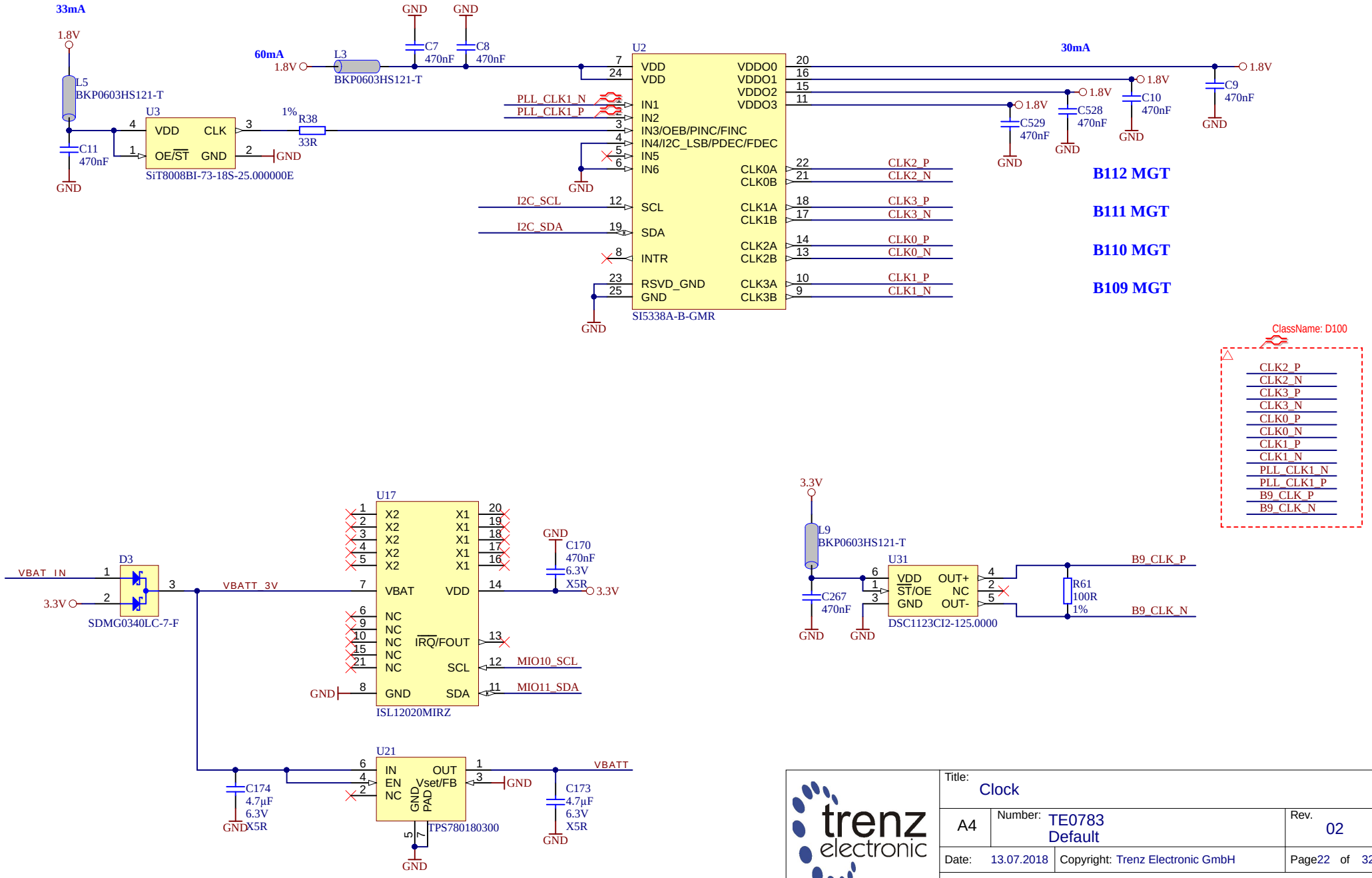


trenz electronic	Title: FPGA B35		
	A4	Number: TE0783 Default	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page19 of 32
	Filename: B35.SchDoc		

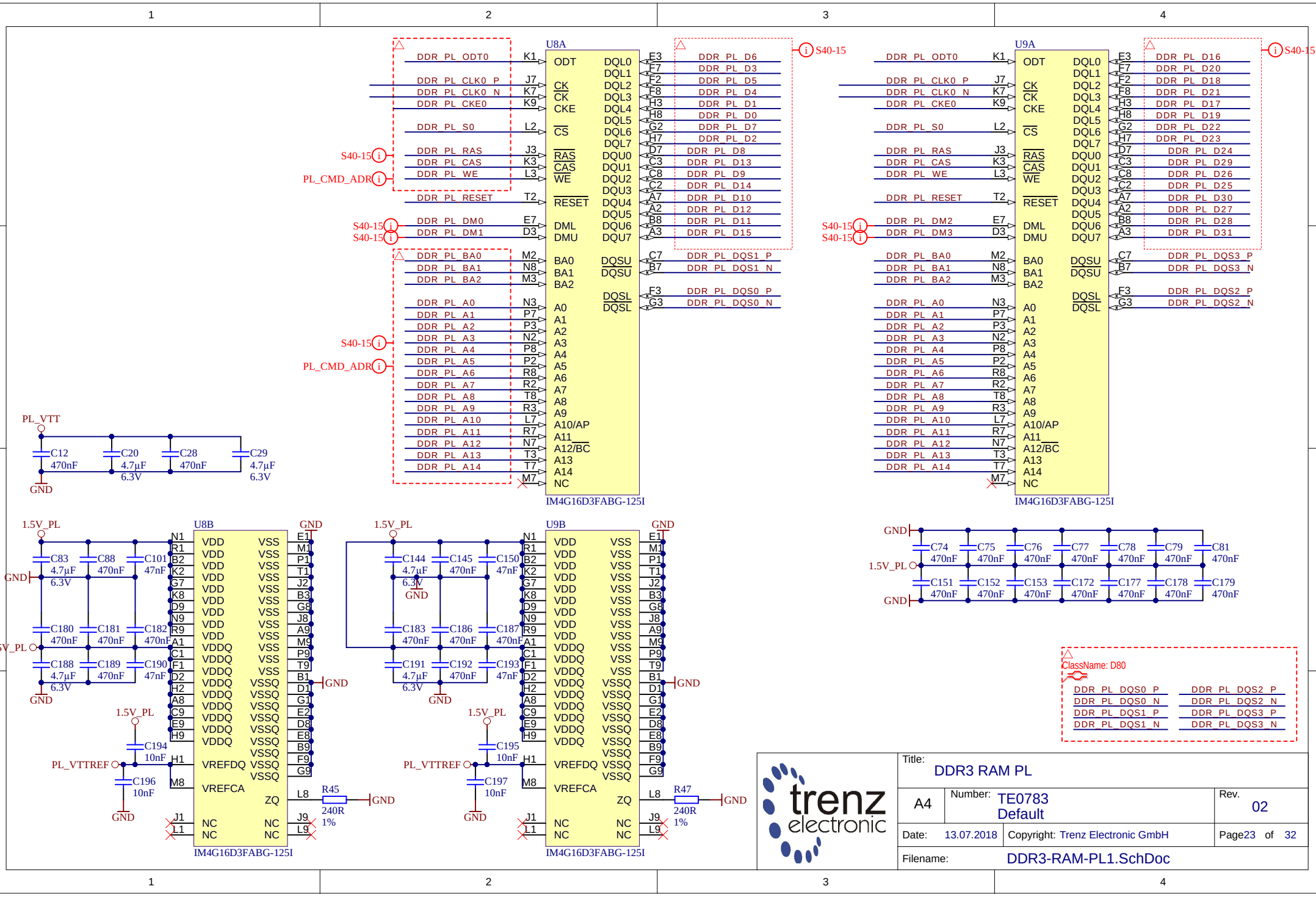


Title: ZYNQ POWER			
A4	Number: TE0783 Default		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page20 of 32
Filename: FPGA-PWR.SchDoc			


Termination
DDR3-Terminator
VTT
R9D 5% 39R DDR3_A13
R9C 5% 39R DDR3_A9
R9B 5% 39R DDR3_A7
R9A 5% 39R DDR3_A0
R10D 5% 39R DDR3_A8
R10B 5% 39R DDR3_A1
R10C 5% 39R DDR3_RAS
R10A 5% 39R DDR3_BA1
R19D 5% 39R DDR3_ODT0
R19C 5% 39R DDR3_BA0
R19B 5% 39R DDR3_CAS
R19A 5% 39R DDR3_A5
R20D 5% 39R DDR3_BA2
R20A 5% 39R DDR3_A2
R20B 5% 39R DDR3_A12
R20C 5% 39R DDR3_A4
R30D 5% 39R DDR3_S0
R30C 5% 39R DDR3_WE
R30A 5% 39R DDR3_CKE0
R30B 5% 39R DDR3_A10
R31D 5% 39R DDR3_A6
R31C 5% 39R DDR3_A11
R31B 5% 39R DDR3_A14
R31A 5% 39R DDR3_A3
VTT
C3 470nF
C4 4.7µF 6.3V
C60 470nF
C556 4.7µF 6.3V
GND
U10A
DDR3_ODT0 K1 ODT
DDR3_CLK0_P J7 CK
DDR3_CLK0_N K7 CK
DDR3_CKE0 K9 CKE
S40-15
DDR3_S0 L2 CS
DDR3_RAS J3 RAS
DDR3_CAS K3 CAS
DDR3_WE L3 WE
R29 4K99 1%
GND
DDR3_RESET T2 RESET
DDR3_DM0 E7 DML
DDR3_DM1 D3 DMU
S40-15
DDR3_BA0 M2 BA0
DDR3_BA1 N8 BA1
DDR3_BA2 M3 BA2
DDR3_A0 N3 A0
DDR3_A1 P7 A1
DDR3_A2 P3 A2
DDR3_A3 N2 A3
DDR3_A4 P8 A4
DDR3_A5 P2 A5
DDR3_A6 R8 A6
DDR3_A7 R2 A7
DDR3_A8 T8 A8
DDR3_A9 R3 A9
DDR3_A10 L7 A10/AP
DDR3_A11 R7 A11
DDR3_A12 N7 A12/BC
DDR3_A13 T3 A13
DDR3_A14 T7 A14
M7 NC
DQL0 DQL1 DQL2 DQL3 DQL4 DQL5 DQL6 DQL7 DQU0 DQU1 DQU2 DQU3 DQU4 DQU5 DQU6 DQU7
DQSU DQSU
DQSL DQSL
E3 DDR3_D6
F7 DDR3_D3
F2 DDR3_D5
F8 DDR3_D4
H3 DDR3_D1
H8 DDR3_D0
G2 DDR3_D7
H7 DDR3_D2
D7 DDR3_D8
C3 DDR3_D13
C8 DDR3_D9
C2 DDR3_D14
A7 DDR3_D10
A2 DDR3_D15
B8 DDR3_D11
A3 DDR3_D12
C7 DDR3_DQS1_P
B7 DDR3_DQS1_N
E3 DDR3_DQS0_P
G3 DDR3_DQS0_N
IM4G16D3FABG-125I
S40-15
U19A
DDR3_ODT0 K1 ODT
DDR3_CLK0_P J7 CK
DDR3_CLK0_N K7 CK
DDR3_CKE0 K9 CKE
S40-15
DDR3_S0 L2 CS
DDR3_RAS J3 RAS
DDR3_CAS K3 CAS
DDR3_WE L3 WE
S40-15
DDR3_RESET T2 RESET
DDR3_DM2 E7 DML
DDR3_DM3 D3 DMU
DDR3_BA0 M2 BA0
DDR3_BA1 N8 BA1
DDR3_BA2 M3 BA2
DDR3_A0 N3 A0
DDR3_A1 P7 A1
DDR3_A2 P3 A2
DDR3_A3 N2 A3
DDR3_A4 P8 A4
DDR3_A5 P2 A5
DDR3_A6 R8 A6
DDR3_A7 R2 A7
DDR3_A8 T8 A8
DDR3_A9 R3 A9
DDR3_A10 L7 A10/AP
DDR3_A11 R7 A11
DDR3_A12 N7 A12/BC
DDR3_A13 T3 A13
DDR3_A14 T7 A14
M7 NC
S40-15
DQL0 DQL1 DQL2 DQL3 DQL4 DQL5 DQL6 DQL7 DQU0 DQU1 DQU2 DQU3 DQU4 DQU5 DQU6 DQU7
DQSU DQSU
DQSL DQSL
E3 DDR3_D22
F7 DDR3_D23
F2 DDR3_D18
F8 DDR3_D21
H3 DDR3_D17
H8 DDR3_D19
G2 DDR3_D16
H7 DDR3_D20
D7 DDR3_D26
C3 DDR3_D31
C8 DDR3_D24
C2 DDR3_D25
A7 DDR3_D30
A2 DDR3_D27
B8 DDR3_D28
A3 DDR3_D29
C7 DDR3_DQS3_P
B7 DDR3_DQS3_N
E3 DDR3_DQS2_P
G3 DDR3_DQS2_N
IM4G16D3FABG-125I
S40-15
DDR3_CLK0_P
R32 80R6 1%
DDR3_CLK0_N
Place directly at the clock pins
1.5V
C5 4.7µF 6.3V
C14 470nF
C21 47nF
GND
C102 470nF
C103 470nF
C104 470nF
1.5V
C108 4.7µF 6.3V
C109 470nF
C110 47nF
GND
U10B
N1 VDD
R1 VDD
B2 VDD
K2 VDD
G7 VDD
K8 VDD
D9 VDD
N9 VDD
R9 VDD
A1 VDD
C1 VDDQ
F1 VDDQ
D2 VDDQ
H2 VDDQ
A8 VDDQ
C9 VDDQ
E9 VDDQ
H9 VDDQ
H1 VREFDQ
M8 VREFCA
L8 ZQ
J1 NC
L1 NC
VSS E1
VSS M1
VSS P1
VSS T1
VSS J2
VSS B3
VSS G8
VSS J8
VSS A9
VSS M9
VSS P9
VSS T9
VSSQ B1
VSSQ D1
VSSQ G1
VSSQ E2
VSSQ D8
VSSQ E8
VSSQ B9
VSSQ F9
VSSQ G9
NC J9
NC L9
GND
1.5V
C114 10nF
VTTREF
C116 10nF
GND
R33 240R 1%
GND
IM4G16D3FABG-125I
1.5V
C22 4.7µF 6.3V
C54 470nF
C55 47nF
GND
C105 470nF
C106 470nF
C107 470nF
C111 4.7µF 6.3V
C112 470nF
C113 47nF
GND
U19B
N1 VDD
R1 VDD
B2 VDD
K2 VDD
G7 VDD
K8 VDD
D9 VDD
N9 VDD
R9 VDD
A1 VDD
C1 VDDQ
F1 VDDQ
D2 VDDQ
H2 VDDQ
A8 VDDQ
C9 VDDQ
E9 VDDQ
H9 VDDQ
H1 VREFDQ
M8 VREFCA
L8 ZQ
J1 NC
L1 NC
VSS E1
VSS M1
VSS P1
VSS T1
VSS J2
VSS B3
VSS G8
VSS J8
VSS A9
VSS M9
VSS P9
VSS T9
VSSQ B1
VSSQ D1
VSSQ G1
VSSQ E2
VSSQ D8
VSSQ E8
VSSQ B9
VSSQ F9
VSSQ G9
NC J9
NC L9
GND
1.5V
C115 10nF
VTTREF
C117 10nF
GND
R34 240R 1%
GND
IM4G16D3FABG-125I
GND
1.5V
C133 470nF
C135 470nF
C136 470nF
C89 470nF
C137 470nF
C138 470nF
C139 470nF
C94 470nF
C95 470nF
C96 470nF
C97 470nF
C98 470nF
C99 470nF
C100 470nF
ClassName: D80
DDR3_DQS0_P
DDR3_DQS0_N
DDR3_DQS1_P
DDR3_DQS1_N
DDR3_CLK0_P
DDR3_CLK0_N
DDR3_DQS2_P
DDR3_DQS2_N
DDR3_DQS3_P
DDR3_DQS3_N
trenz electronic
Title: DDR3 RAM PS
A4
Number: TE0783 Default
Rev. 02
Date: 13.07.2018
Copyright: Trenz Electronic GmbH
Page21 of 32
Filename: DDR3-RAM.SchDoc



Title: Clock			
A4	Number: TE0783 Default		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page22 of 32
Filename: Clock.SchDoc			


U8A
U9A
U8B
U9B
IM4G16D3FABG-125I
PL_VTT
GND
1.5V_PL
PL_VTTREF
PL_CMD_ADR
S40-15
R45
240R
1%
R47
ClassName: D80
DDR_PL_DQS0_P
DDR_PL_DQS0_N
DDR_PL_DQS1_P
DDR_PL_DQS1_N
DDR_PL_DQS2_P
DDR_PL_DQS2_N
DDR_PL_DQS3_P
DDR_PL_DQS3_N
trenz electronic
Title: DDR3 RAM PL
A4
Number: TE0783 Default
Rev. 02
Date: 13.07.2018
Copyright: Trenz Electronic GmbH
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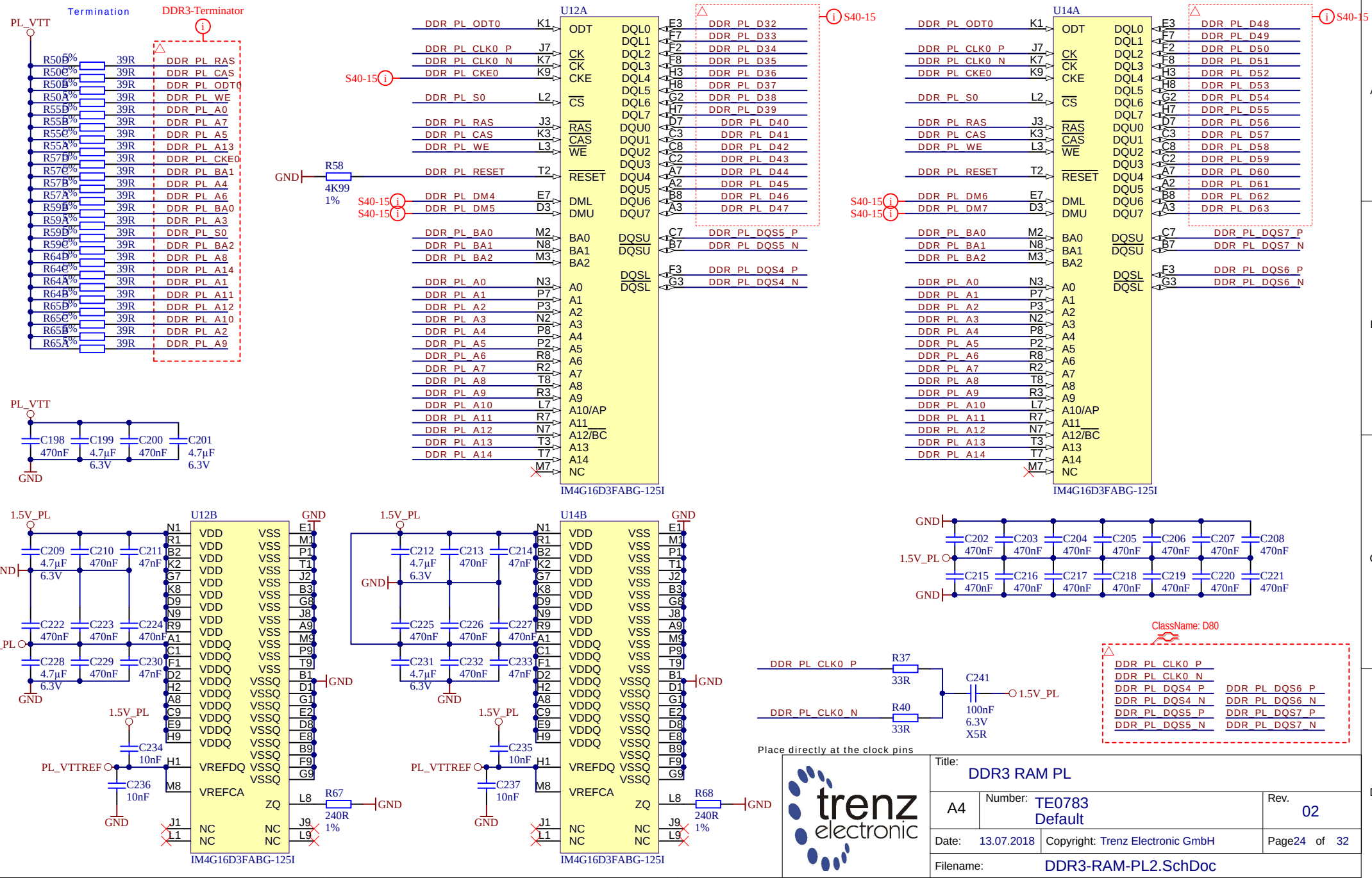
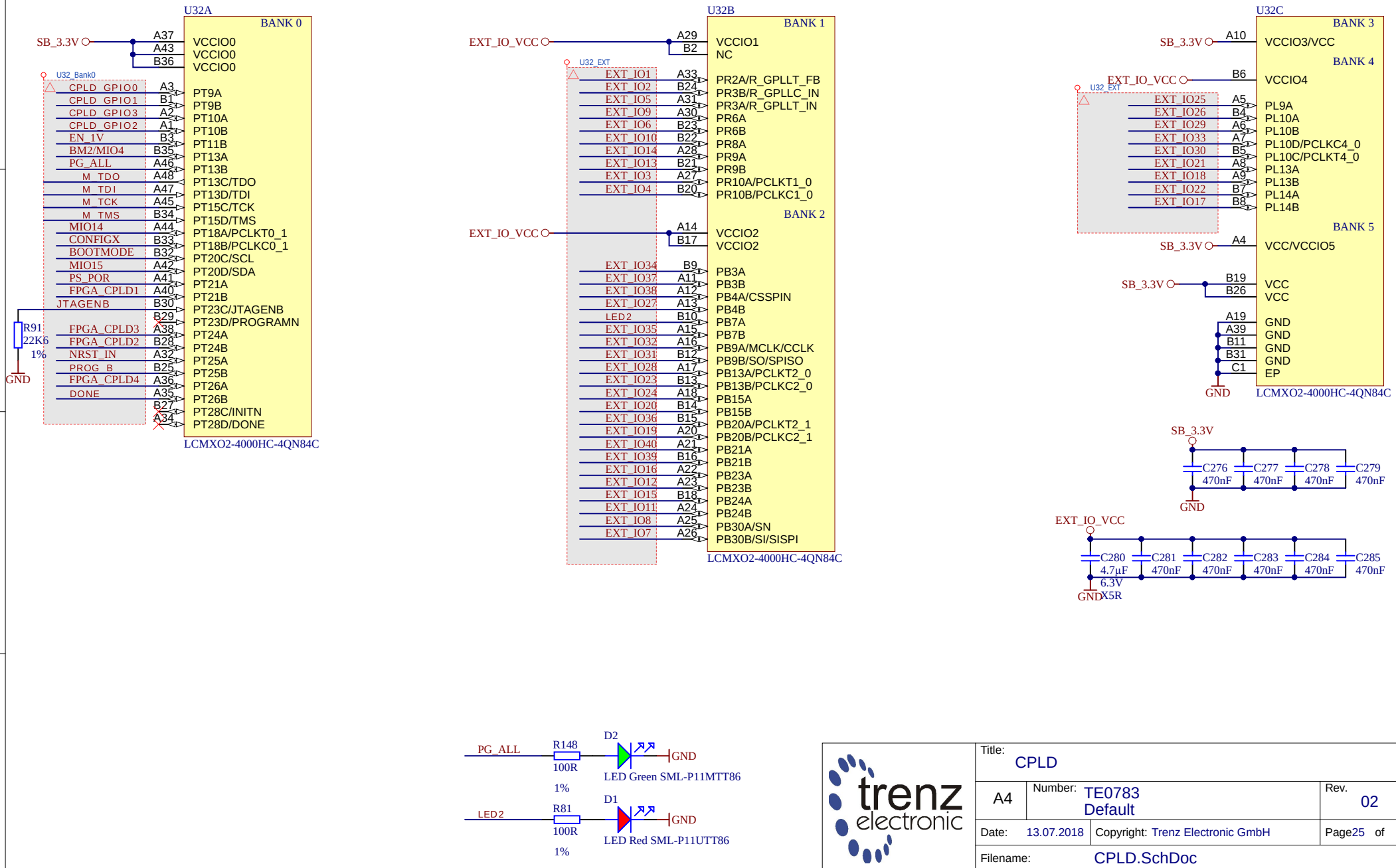
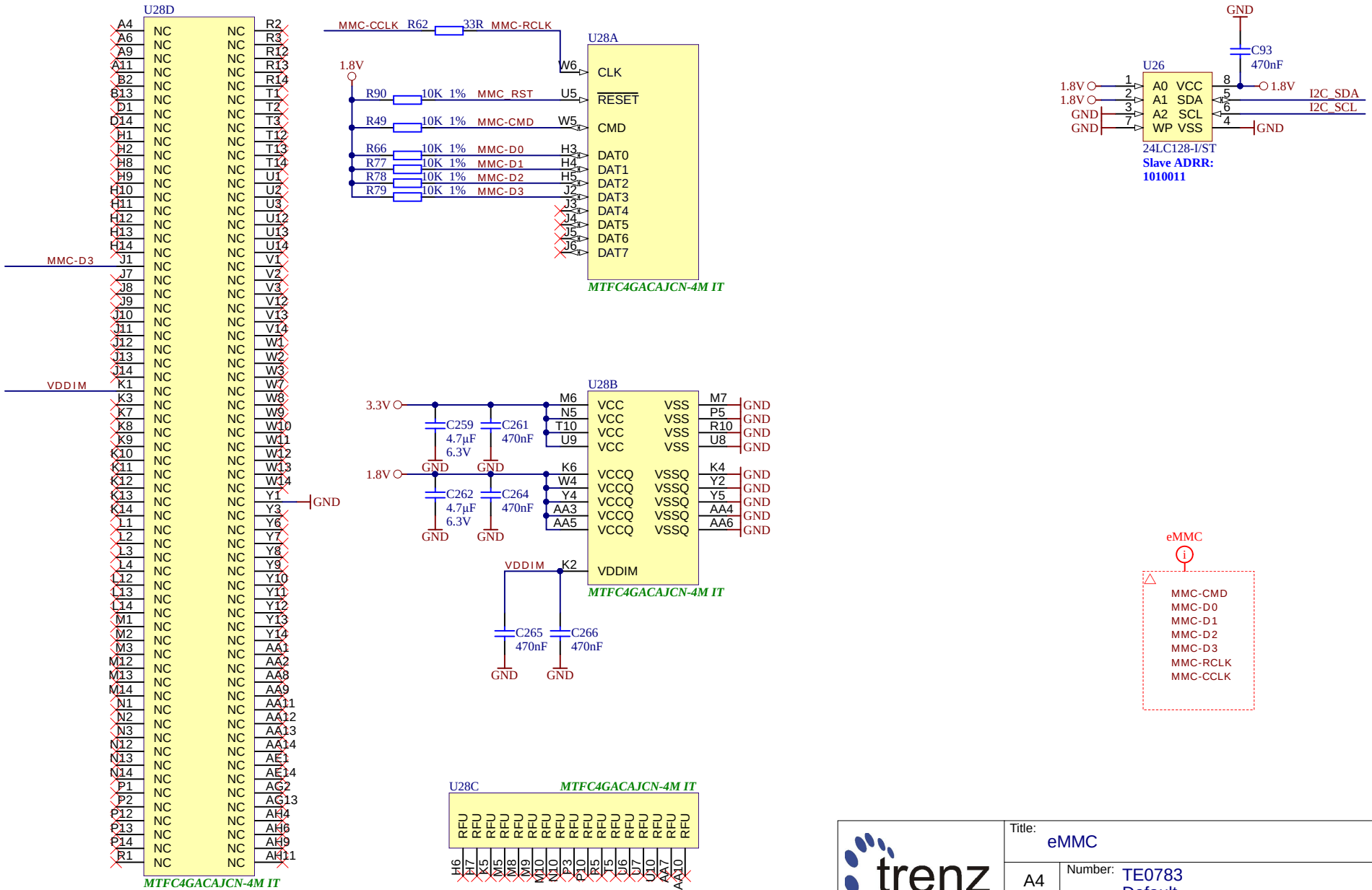
Filename: DDR3-RAM-PL1.SchDoc


Termination
DDR3-Terminator
PL_VTT
R50B 5% 39R DDR_PL_RAS
R50A 5% 39R DDR_PL_CAS
R55B 5% 39R DDR_PL_ODT0
R55A 5% 39R DDR_PL_WE
R57B 5% 39R DDR_PL_A0
R57A 5% 39R DDR_PL_A7
R59B 5% 39R DDR_PL_A5
R59A 5% 39R DDR_PL_A13
R64B 5% 39R DDR_PL_CKE0
R64A 5% 39R DDR_PL_BA1
R65B 5% 39R DDR_PL_A4
R65A 5% 39R DDR_PL_A6
R50B 5% 39R DDR_PL_BA0
R50A 5% 39R DDR_PL_A3
R55B 5% 39R DDR_PL_S0
R55A 5% 39R DDR_PL_BA2
R57B 5% 39R DDR_PL_A8
R57A 5% 39R DDR_PL_A14
R59B 5% 39R DDR_PL_A1
R59A 5% 39R DDR_PL_A11
R64B 5% 39R DDR_PL_A12
R64A 5% 39R DDR_PL_A10
R65B 5% 39R DDR_PL_A2
R65A 5% 39R DDR_PL_A9
PL_VTT
C198 470nF
C199 4.7µF 6.3V
C200 470nF
C201 4.7µF 6.3V
GND
U12A
DDR_PL_ODT0 K1 ODT
DDR_PL_CLK0_P J7 CK
DDR_PL_CLK0_N K7 CK
DDR_PL_CKE0 K9 CKE
S40-15
DDR_PL_S0 L2 CS
DDR_PL_RAS J3 RAS
DDR_PL_CAS K3 CAS
DDR_PL_WE L3 WE
R58 4K99 1%
GND
DDR_PL_RESET T2 RESET
S40-15 DDR_PL_DM4 E7 DML
S40-15 DDR_PL_DM5 D3 DMU
DDR_PL_BA0 M2 BA0
DDR_PL_BA1 N8 BA1
DDR_PL_BA2 M3 BA2
DDR_PL_A0 N3 A0
DDR_PL_A1 P7 A1
DDR_PL_A2 P3 A2
DDR_PL_A3 N2 A3
DDR_PL_A4 P8 A4
DDR_PL_A5 P2 A5
DDR_PL_A6 R8 A6
DDR_PL_A7 R2 A7
DDR_PL_A8 T8 A8
DDR_PL_A9 R3 A9
DDR_PL_A10 L7 A10/AP
DDR_PL_A11 R7 A11
DDR_PL_A12 N7 A12/BC
DDR_PL_A13 T3 A13
DDR_PL_A14 T7 A14
M7 NC
DQL0 E3 DDR_PL_D32
DQL1 F7 DDR_PL_D33
DQL2 F2 DDR_PL_D34
DQL3 F8 DDR_PL_D35
DQL4 H3 DDR_PL_D36
DQL5 H8 DDR_PL_D37
DQL6 G2 DDR_PL_D38
DQL7 H7 DDR_PL_D39
DQU0 D7 DDR_PL_D40
DQU1 C3 DDR_PL_D41
DQU2 C8 DDR_PL_D42
DQU3 C2 DDR_PL_D43
DQU4 A7 DDR_PL_D44
DQU5 A2 DDR_PL_D45
DQU6 B8 DDR_PL_D46
DQU7 A3 DDR_PL_D47
DQSU C7 DDR_PL_DQS5_P
DQSU B7 DDR_PL_DQS5_N
DQSL E3 DDR_PL_DQS4_P
DQSL G3 DDR_PL_DQS4_N
S40-15
IM4G16D3FABG-125I
U14A
DDR_PL_ODT0 K1 ODT
DDR_PL_CLK0_P J7 CK
DDR_PL_CLK0_N K7 CK
DDR_PL_CKE0 K9 CKE
DDR_PL_S0 L2 CS
DDR_PL_RAS J3 RAS
DDR_PL_CAS K3 CAS
DDR_PL_WE L3 WE
DDR_PL_RESET T2 RESET
S40-15 DDR_PL_DM6 E7 DML
S40-15 DDR_PL_DM7 D3 DMU
DDR_PL_BA0 M2 BA0
DDR_PL_BA1 N8 BA1
DDR_PL_BA2 M3 BA2
DDR_PL_A0 N3 A0
DDR_PL_A1 P7 A1
DDR_PL_A2 P3 A2
DDR_PL_A3 N2 A3
DDR_PL_A4 P8 A4
DDR_PL_A5 P2 A5
DDR_PL_A6 R8 A6
DDR_PL_A7 R2 A7
DDR_PL_A8 T8 A8
DDR_PL_A9 R3 A9
DDR_PL_A10 L7 A10/AP
DDR_PL_A11 R7 A11
DDR_PL_A12 N7 A12/BC
DDR_PL_A13 T3 A13
DDR_PL_A14 T7 A14
M7 NC
DQL0 E3 DDR_PL_D48
DQL1 F7 DDR_PL_D49
DQL2 F2 DDR_PL_D50
DQL3 F8 DDR_PL_D51
DQL4 H3 DDR_PL_D52
DQL5 H8 DDR_PL_D53
DQL6 G2 DDR_PL_D54
DQL7 H7 DDR_PL_D55
DQU0 D7 DDR_PL_D56
DQU1 C3 DDR_PL_D57
DQU2 C8 DDR_PL_D58
DQU3 C2 DDR_PL_D59
DQU4 A7 DDR_PL_D60
DQU5 A2 DDR_PL_D61
DQU6 B8 DDR_PL_D62
DQU7 A3 DDR_PL_D63
DQSU C7 DDR_PL_DQS7_P
DQSU B7 DDR_PL_DQS7_N
DQSL E3 DDR_PL_DQS6_P
DQSL G3 DDR_PL_DQS6_N
S40-15
IM4G16D3FABG-125I
1.5V_PL
GND
C209 4.7µF 6.3V
C210 470nF
C211 47nF
C222 470nF
C223 470nF
C224 470nF
C228 4.7µF 6.3V
C229 470nF
C230 47nF
U12B
VDD N1 R1 B2 K2 G7 K8 D9 N9 R9 A1 C1 F1 D2 H2 A8 C9 E9 H9
VDDQ C1 F1 D2 H2 A8 C9 E9 H9
VSS E1 M1 P1 T1 J2 B3 G8 J8 A9 M9 P9 T9 B1 D1 G1 E2 D8 E8 B9 F9 G9
VSSQ D1 G1 E2 D8 E8 B9 F9 G9
VREFDQ H1
VREFCA M8
ZQ L8
NC J1 L1
NC J9 L9
GND
C234 10nF
PL_VTTREF
C236 10nF
R67 240R 1%
IM4G16D3FABG-125I
C212 4.7µF 6.3V
C213 470nF
C214 47nF
C225 470nF
C226 470nF
C227 470nF
C231 4.7µF 6.3V
C232 470nF
C233 47nF
C235 10nF
C237 10nF
R68 240R 1%
C202 470nF
C203 470nF
C204 470nF
C205 470nF
C206 470nF
C207 470nF
C208 470nF
C215 470nF
C216 470nF
C217 470nF
C218 470nF
C219 470nF
C220 470nF
C221 470nF
DDR_PL_CLK0_P
DDR_PL_CLK0_N
R37 33R
R40 33R
C241 100nF 6.3V X5R
Place directly at the clock pins
ClassName: D80
DDR_PL_CLK0_P
DDR_PL_CLK0_N
DDR_PL_DQS4_P
DDR_PL_DQS4_N
DDR_PL_DQS5_P
DDR_PL_DQS5_N
DDR_PL_DQS6_P
DDR_PL_DQS6_N
DDR_PL_DQS7_P
DDR_PL_DQS7_N
trenz electronic
Title: DDR3 RAM PL
A4
Number: TE0783 Default
Rev. 02
Date: 13.07.2018
Copyright: Trenz Electronic GmbH
Page24 of 32
Filename: DDR3-RAM-PL2.SchDoc



trenz electronic	Title: CPLD		
A4	Number: TE0783 Default		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page25 of 32
Filename: CPLD.SchDoc			



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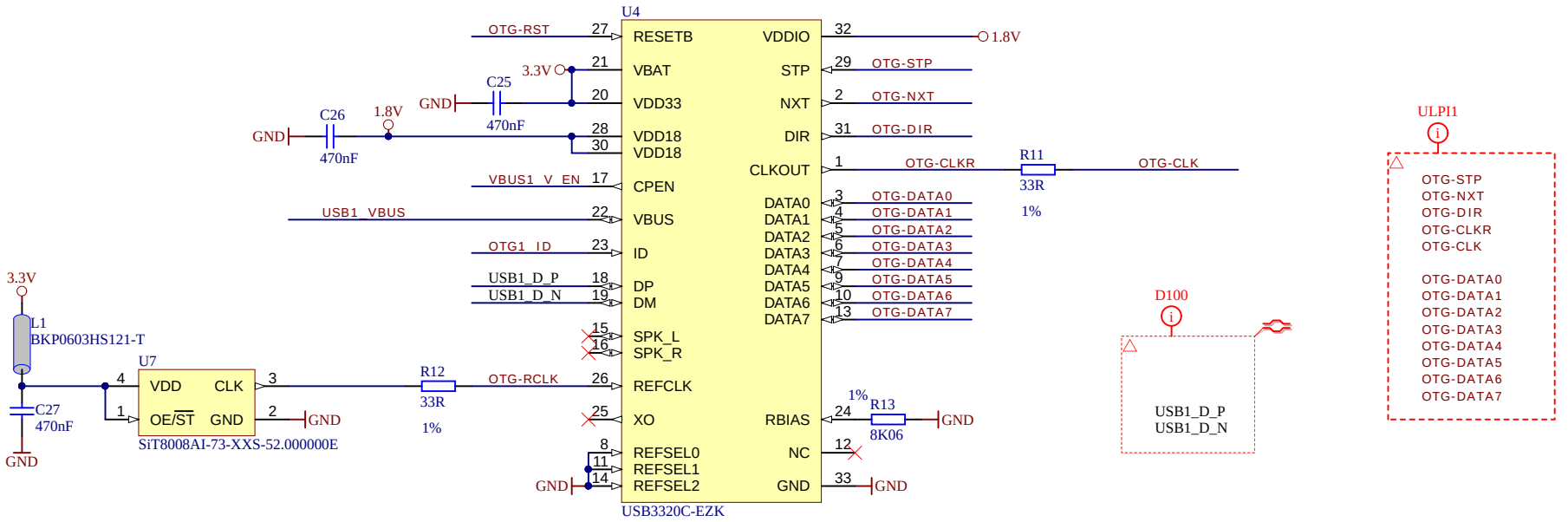
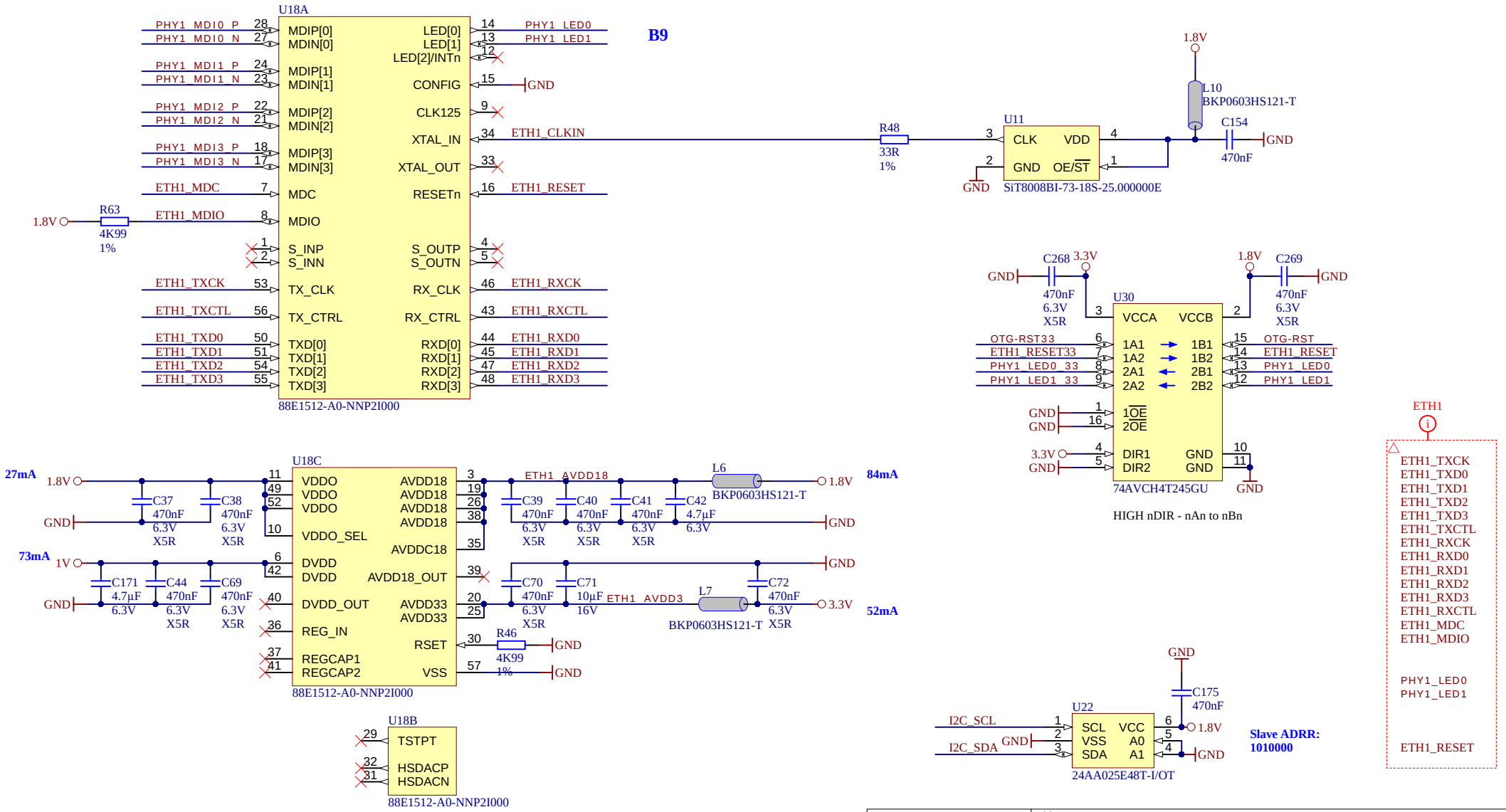
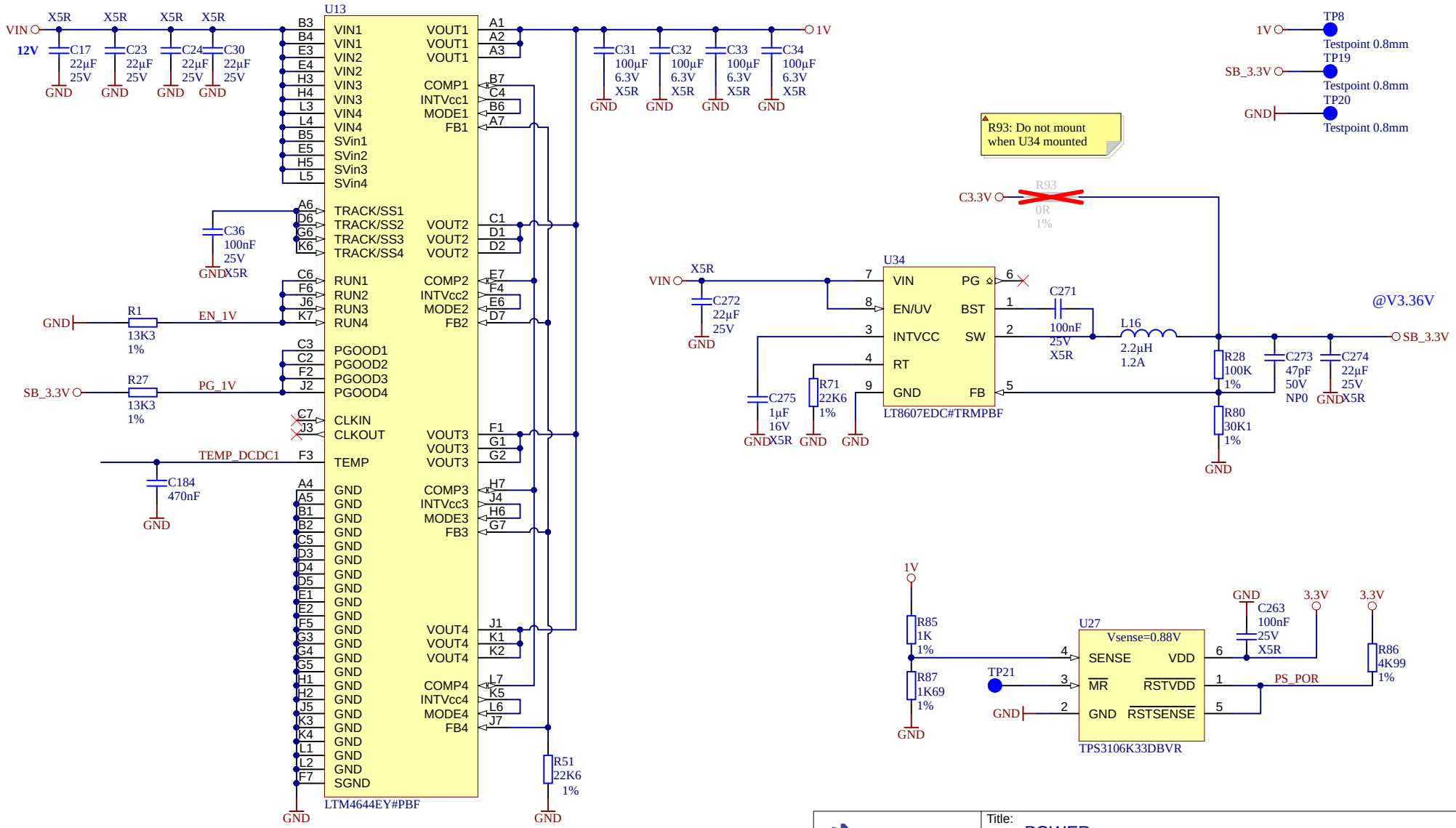
Title: eMMC		
A4	Number: TE0783 Default	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page26 of 32
Filename: eMMC.SchDoc		



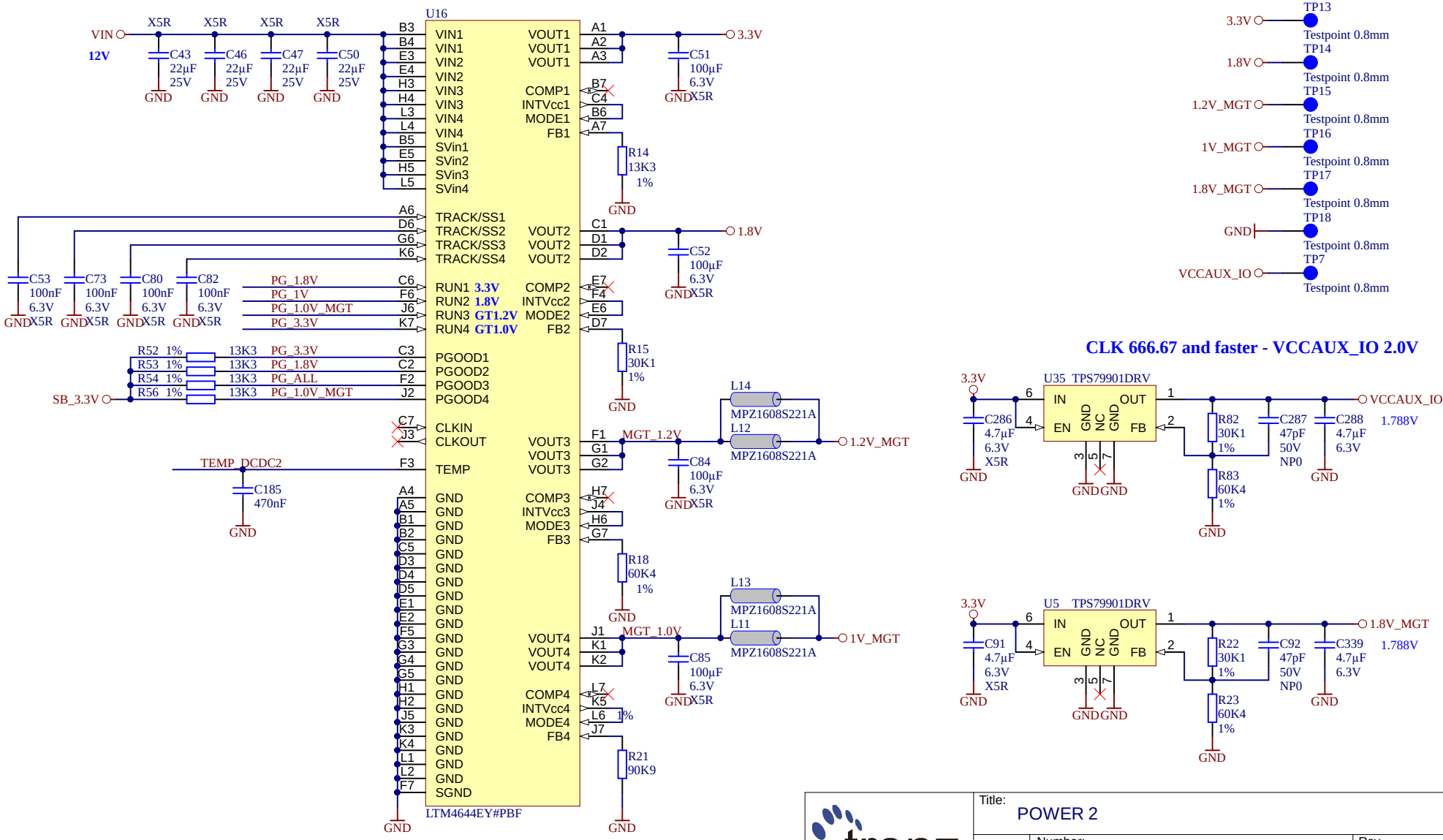
trenz electronic	Title: USB-PHY		
	A4	Number: TE0783 Default	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page27 of 32
	Filename: USB-PHY.SchDoc		



Title: ETH_PHY1			
A4	Number: TE0783 Default		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page28 of 32
Filename: ETH1.SchDoc			

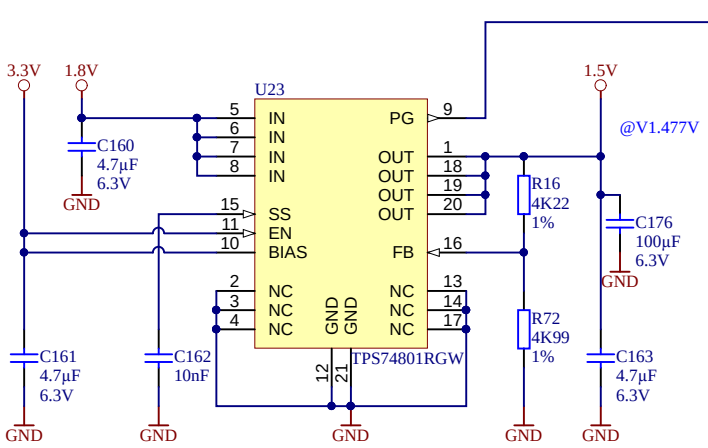


trenz electronic	Title: POWER		
	A4	Number: TE0783 Default	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page29 of 32
	Filename: POWER.SchDoc		

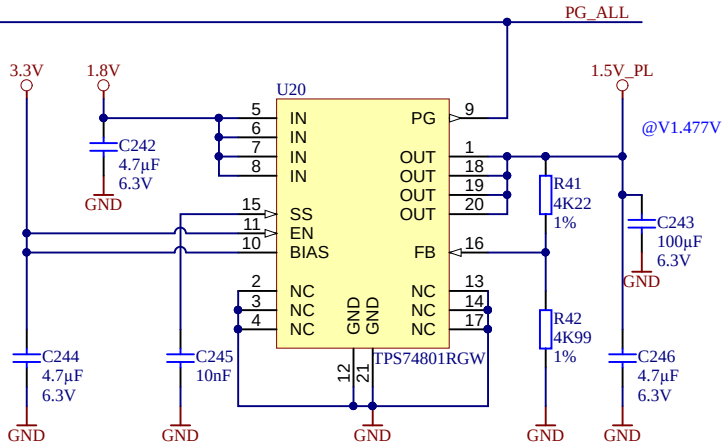


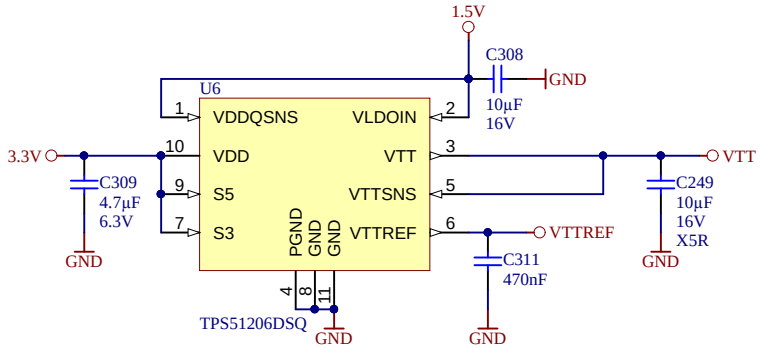
Title: POWER 2			
A4	Number: TE0783 Default		Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH		Page30 of 32
Filename: POWER2.SchDoc			

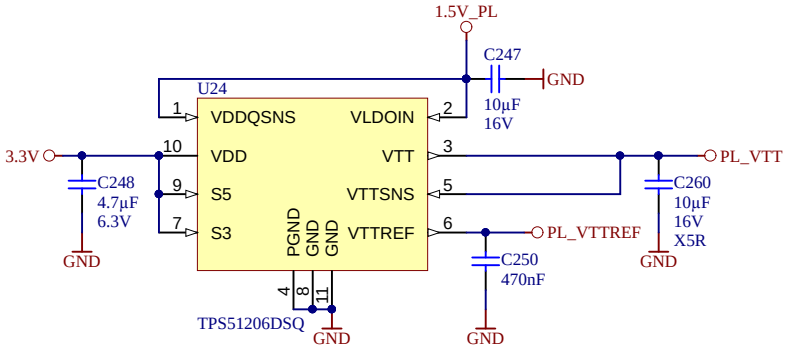
DDR3 PS

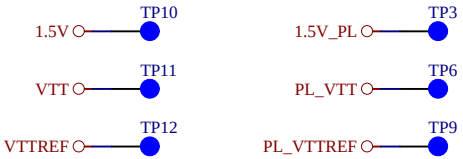


DDR3 PL









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Title: POWER 2		
A4	Number: TE0783 Default	Rev. 02
Date: 13.07.2018	Copyright: Trenz Electronic GmbH	Page31 of 32
Filename: POWER3.SchDoc		

REV. 02:

1) Changed power-up sequence: 3.3V next to 1.8V. MGT power domain next to 3.3V

trenz electronic	Title: Revision Changes		
	A4	Number: TE0783 Default	Rev. 02
	Date: 13.07.2018	Copyright: Trenz Electronic GmbH / TT	Page32 of 32
	Filename: Revision Changes.SchDoc		