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U_DDR3-RAM
DDR3-RAM.SchDoc

U_Ethernet
Ethernet.SchDoc

U_SOC
SOC.SchDoc

U_CPLD
CPLD.SchDoc

U_POWER2
POWER2.SchDoc

U_HyperFlash_RAM
HyperFlash_RAM.SchDoc

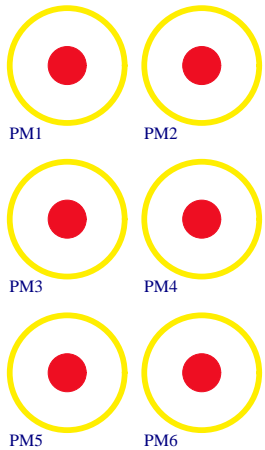
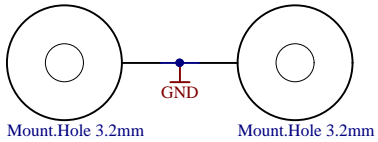
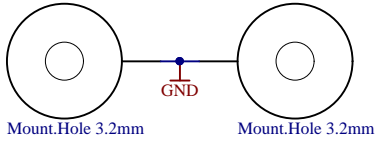
U_Clock
Clock.SchDoc

U_eMMC
eMMC.SchDoc

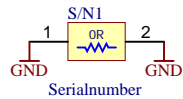
U_Connectors
Connectors.SchDoc

U_POWER
POWER.SchDoc

LOGO1
TE Logo PRINT Layer
LOGO PRINT



Serial
Serialnumber 6,3 x 6.3mm



Title: TE0784 - Overview		
A4	Number: TE0784 045-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page1 of 30
Filename: TE0784.SchDoc		

1

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A

A

B

B

C

C

D

D

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A

A

U_HSMC_CONN_J1
HSMC_CONN_J1.SchDoc



U_HSMC_CONN_J2
HSMC_CONN_J2.SchDoc



U_HSMC_CONN_J3
HSMC_CONN_J3.SchDoc



B

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Title: TE0784 - Connectors		
A4	Number: TE0784 045-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 2 of 30
Filename: Connectors.SchDoc		

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A

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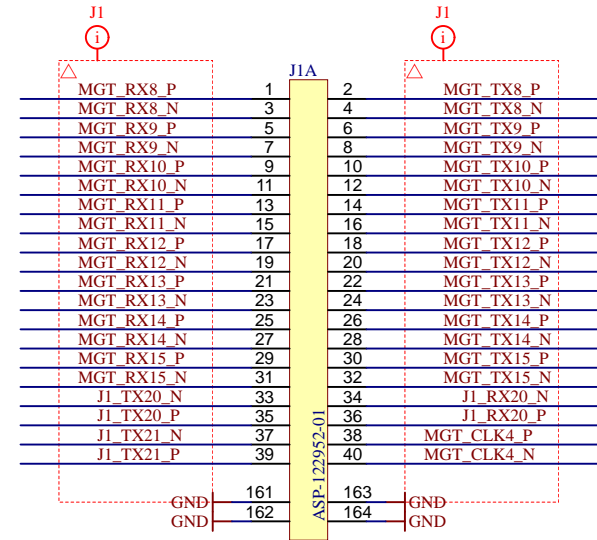
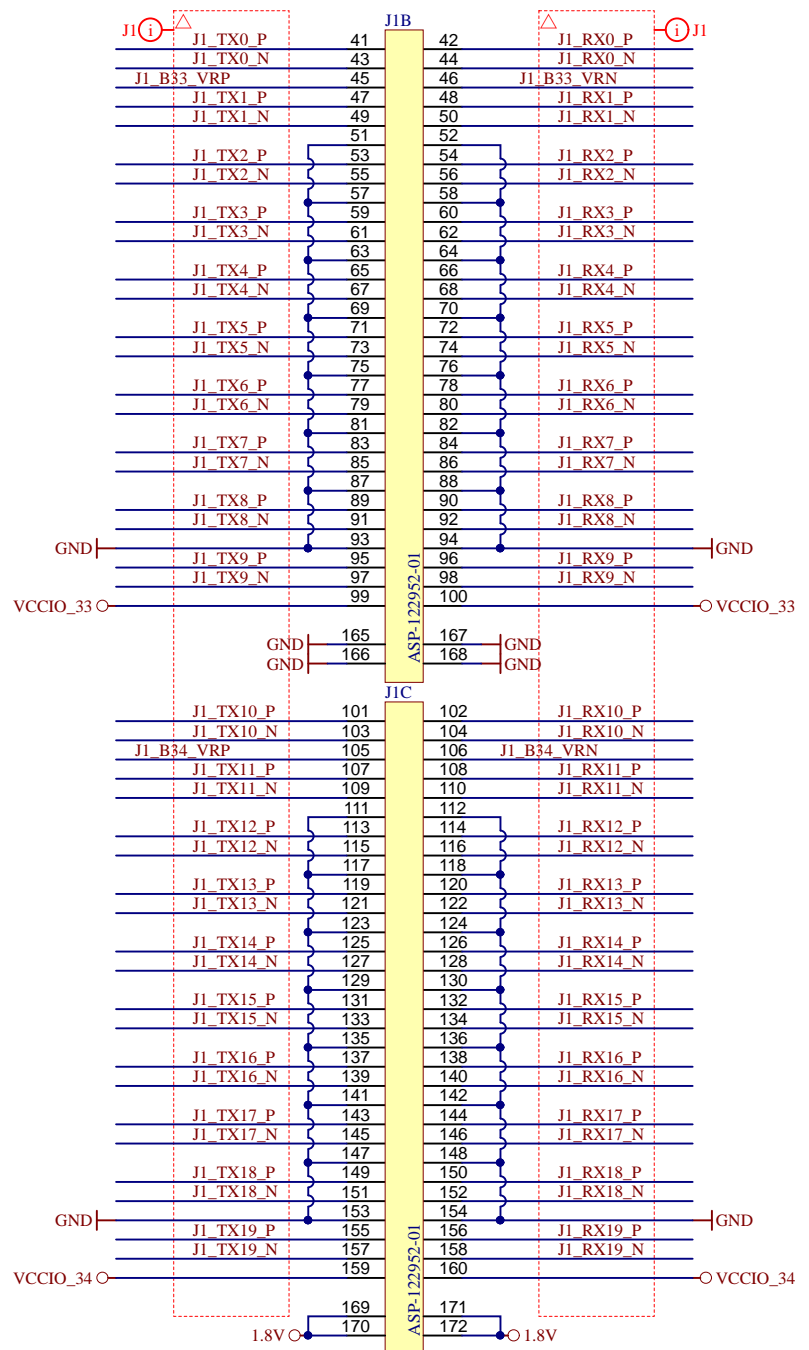

B

C

C

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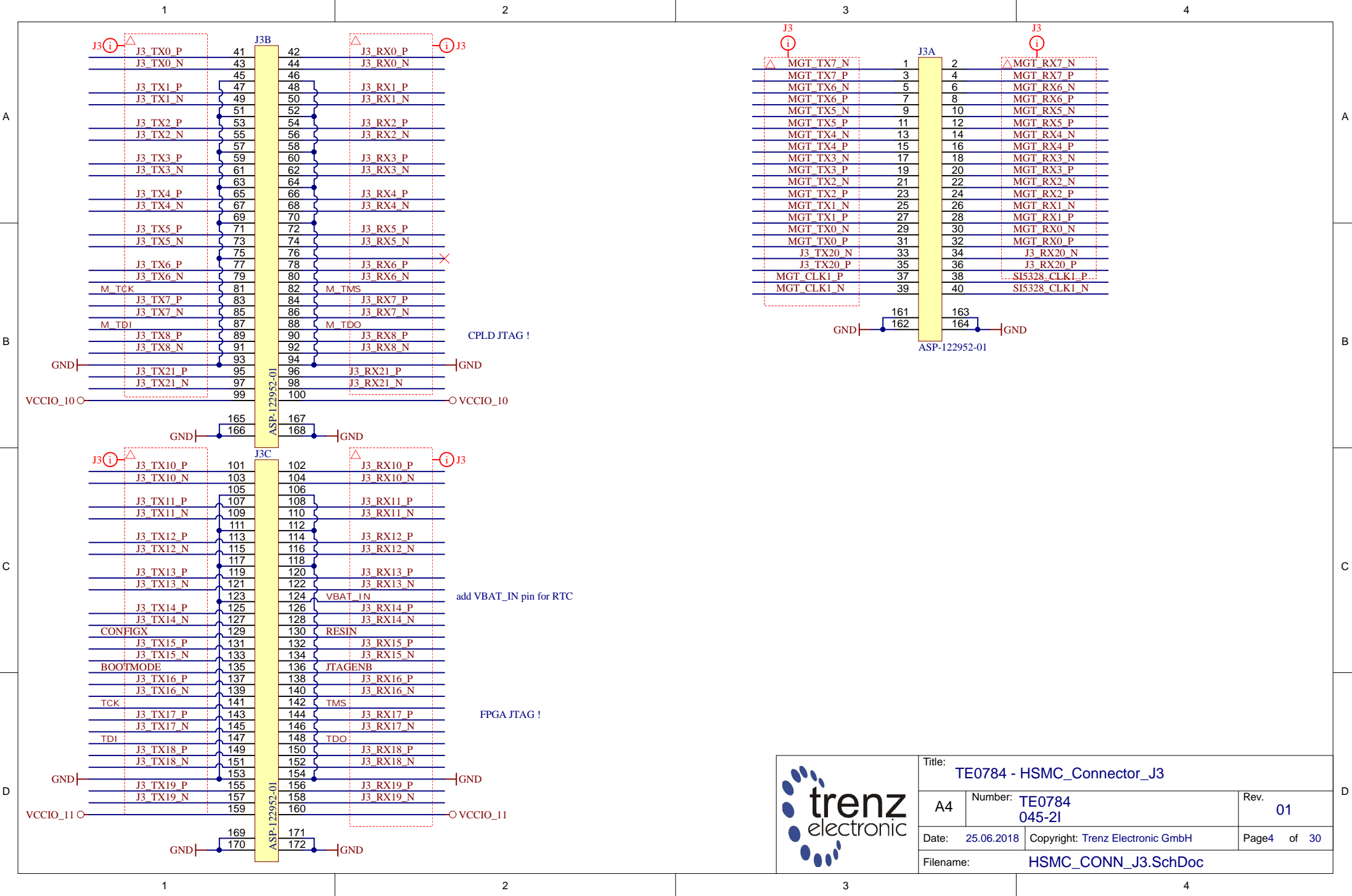
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A4	Number: TE0784 045-21	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page3 of 30
Filename: HSMC_CONN_J1.SchDoc		

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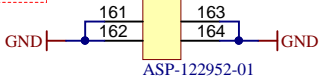
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J3		J3A		J3	
△	MGT TX7 N	1	2	△	MGT RX7 N
	MGT TX7 P	3	4		MGT RX7 P
	MGT TX6 N	5	6		MGT RX6 N
	MGT TX6 P	7	8		MGT RX6 P
	MGT TX5 N	9	10		MGT RX5 N
	MGT TX5 P	11	12		MGT RX5 P
	MGT TX4 N	13	14		MGT RX4 N
	MGT TX4 P	15	16		MGT RX4 P
	MGT TX3 N	17	18		MGT RX3 N
	MGT TX3 P	19	20		MGT RX3 P
	MGT TX2 N	21	22		MGT RX2 N
	MGT TX2 P	23	24		MGT RX2 P
	MGT TX1 N	25	26		MGT RX1 N
	MGT TX1 P	27	28		MGT RX1 P
	MGT TX0 N	29	30		MGT RX0 N
	MGT TX0 P	31	32		MGT RX0 P
	J3 TX20 N	33	34		J3 RX20 N
	J3 TX20 P	35	36		J3 RX20 P
	MGT CLK1 P	37	38		SI5328_CLK1_P
	MGT CLK1 N	39	40		SI5328_CLK1_N



CPLD JTAG !

add VBAT_IN pin for RTC

FPGA JTAG !



Title: TE0784 - HSMC_Connector_J3		
A4	Number: TE0784 045-21	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page4 of 30
Filename: HSMC_CONN_J3.SchDoc		

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A

A

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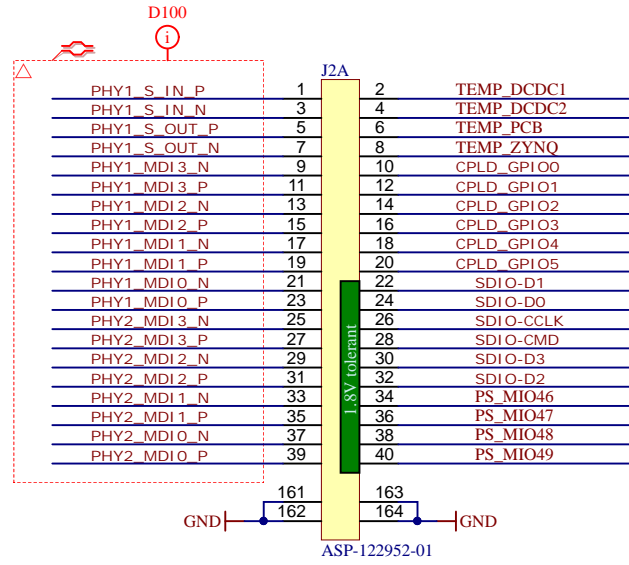
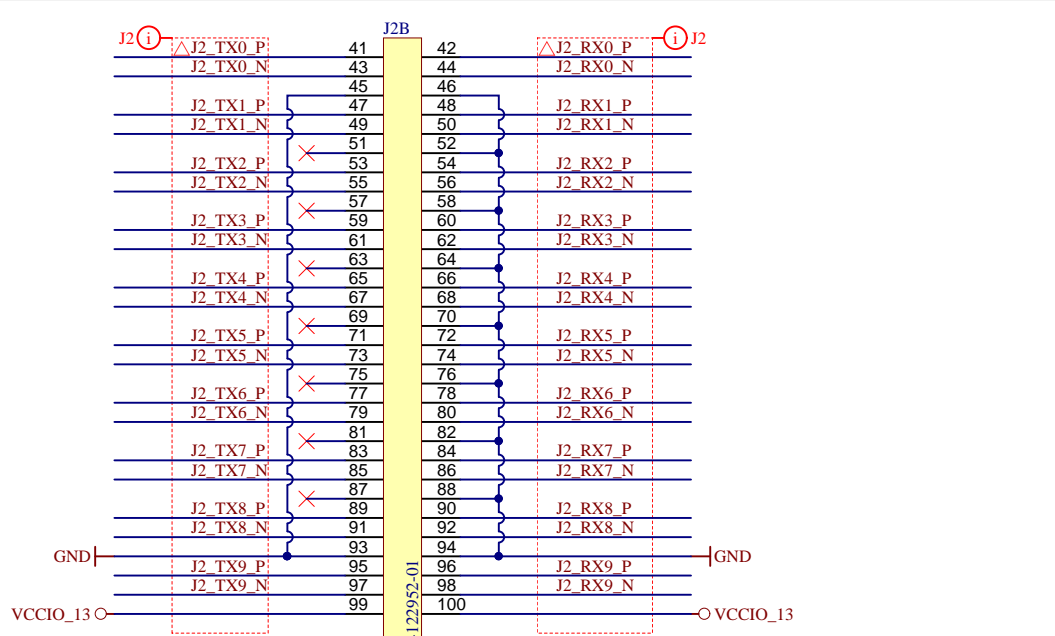
B

C

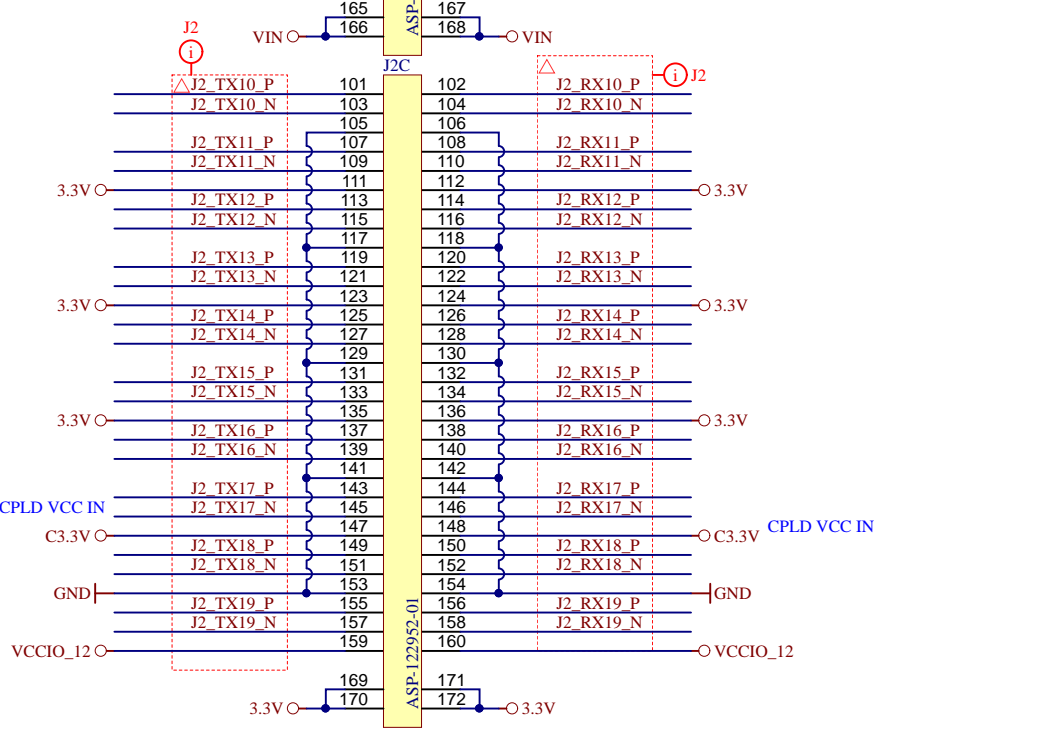
C

D

D



CPLD C3.3V



Title: TE0784 - HSMC_Connector_J2		
A4	Number: TE0784 045-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page5 of 30
Filename: HSMC_CONN_J2.SchDoc		

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A

A

U_PS-DDR
PS-DDR.SchDoc



U_B9
B9.SchDoc



U_MIO-BANKS
MIO-BANKS.SchDoc



U_B10
B10.SchDoc



U_HP-BANKS
HP-BANKS.SchDoc



U_B11
B11.SchDoc



B

B

U_FPGA-MGT
FPGA-MGT.SchDoc



U_B12
B12.SchDoc



U_FPGA-CFG
FPGA-CFG.SchDoc



U_B13
B13.SchDoc



C

C

U_FPGA-PWR
FPGA-PWR.SchDoc



D

D



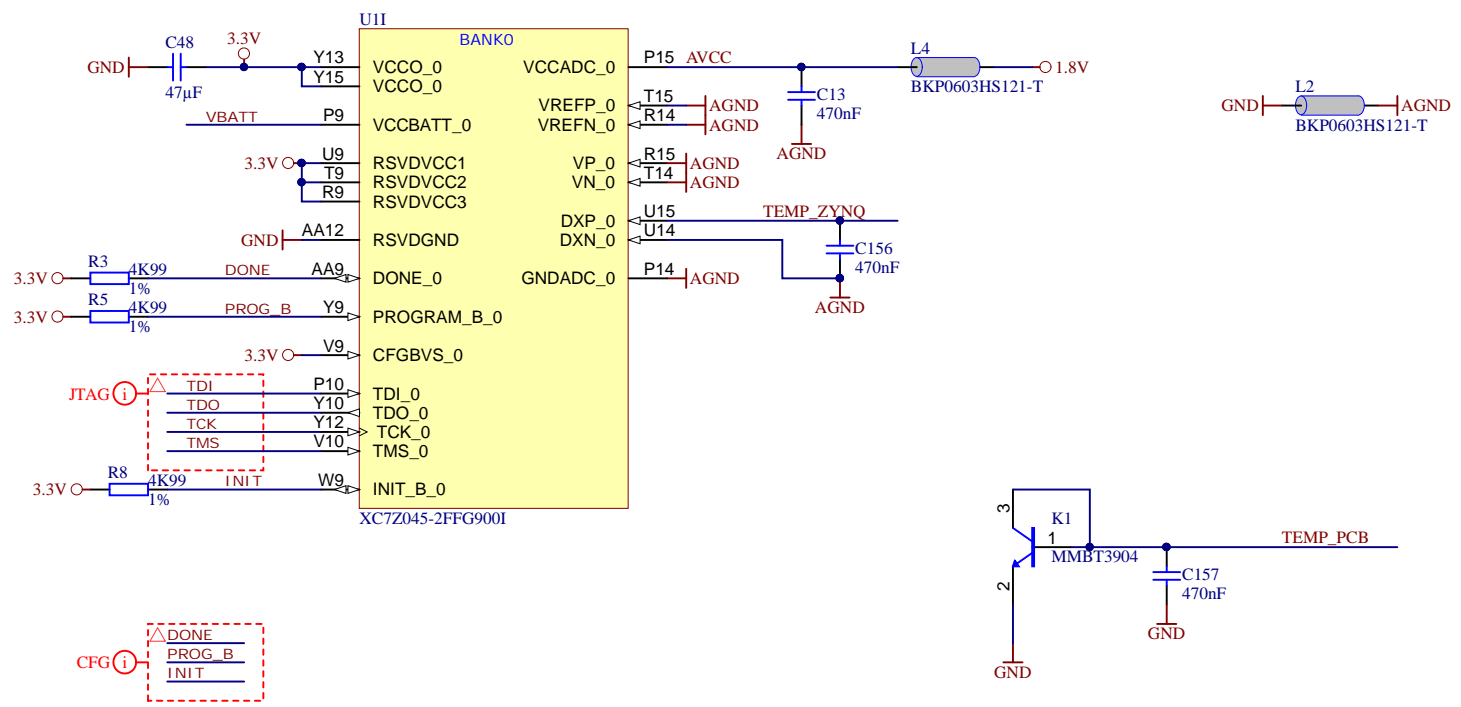
Title: TE0784 - SOC		
A4	Number: TE0784 045-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 6 of 30
Filename: SOC.SchDoc		


1

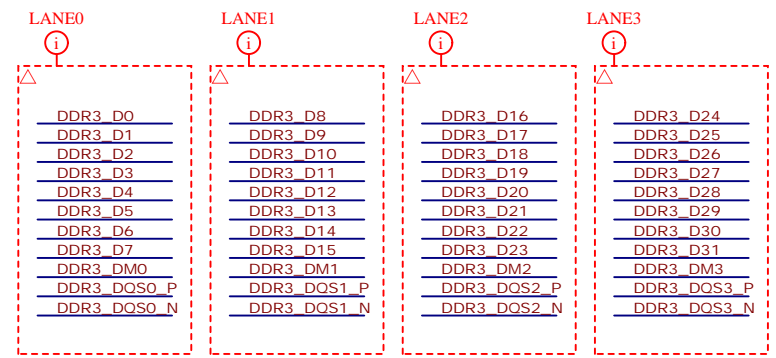
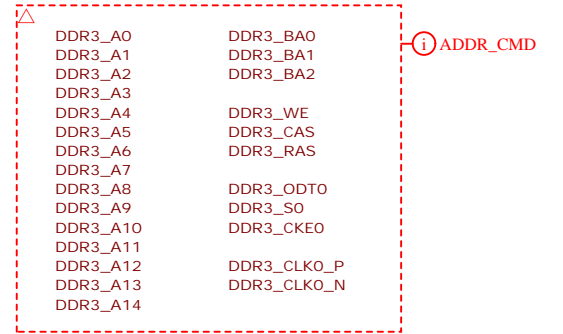
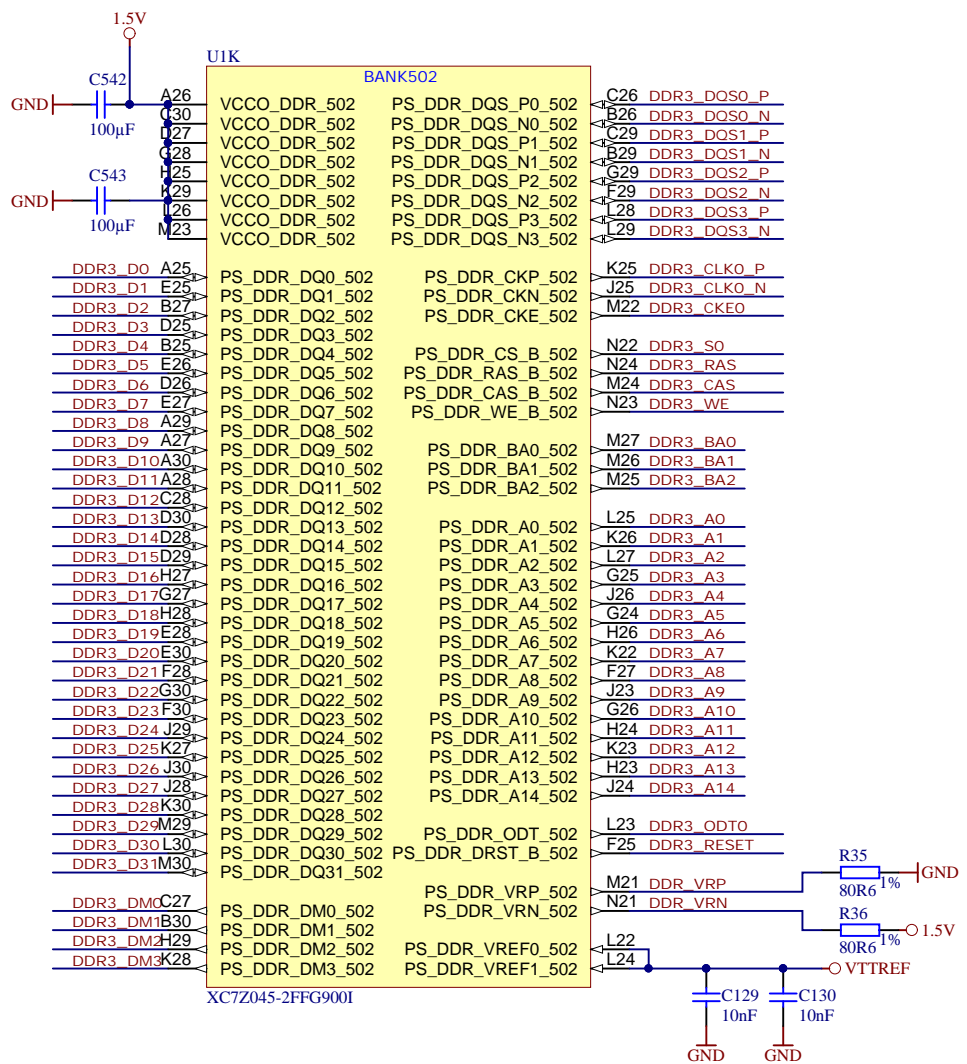
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		A4	Nummer: TE0784 045-2I
Datum: 25.06.2018		Zeichner: Trenz Electronic GmbH	
Filename: FPGA-CFG.SchDoc		Blatt 7 von 30	



Title: TE0784 - FPGA DDR Banks		
A4	Number: TE0784 045-21	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 8 of 30
Filename: PS-DDR.SchDoc		

A

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D

U1M

ClassName: MGT_TX

D100

BANK109

BANK110

BANK111

BANK112

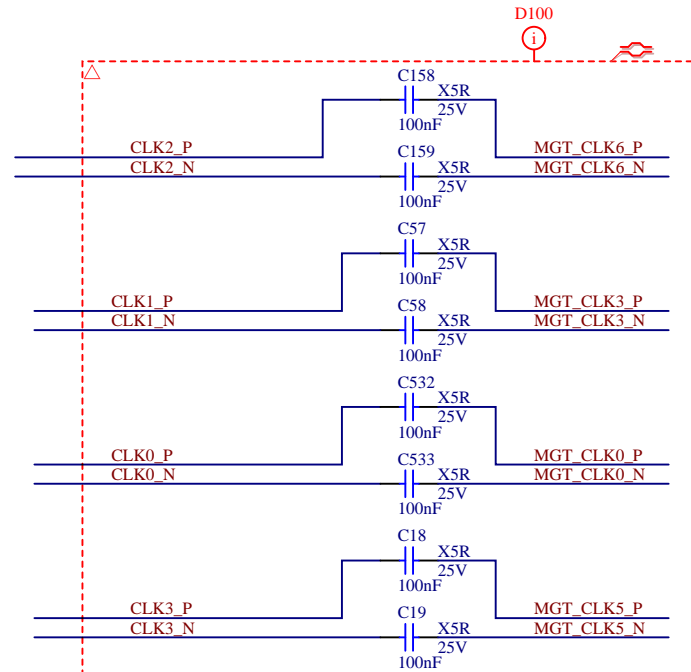
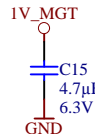
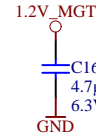
XC7Z045-2FFG900I

ClassName: MGT_RX

D100

MGT_CLK

D100



Title: TE0784 - FPGA MGT		
A4	Number: TE0784 045-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page9 of 30
Filename: FPGA-MGT.SchDoc		

A

B

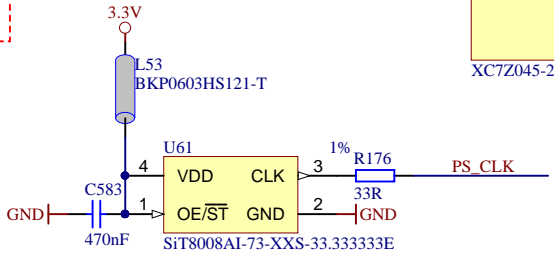
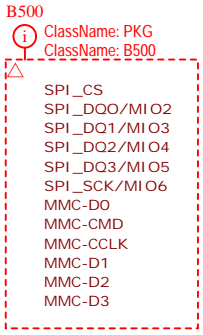
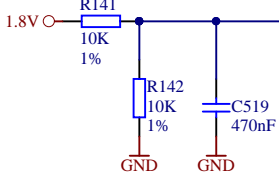
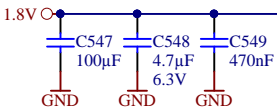
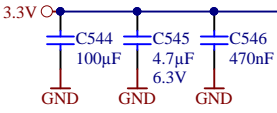
C

D

SPI and JTAG modes supported
Cascade and independent modes supported

U1J

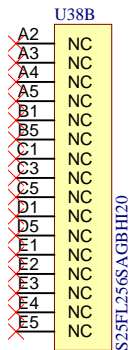
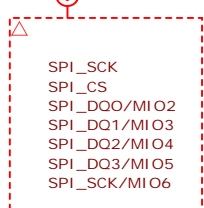
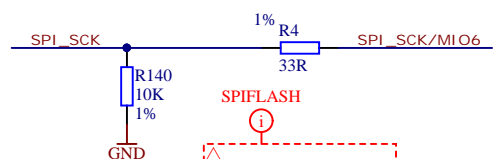
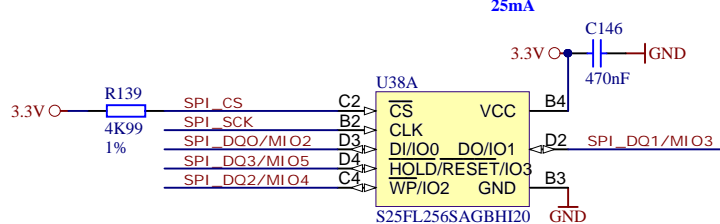
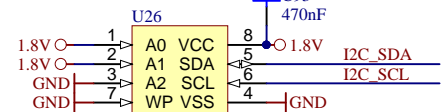
BANK500 & 501



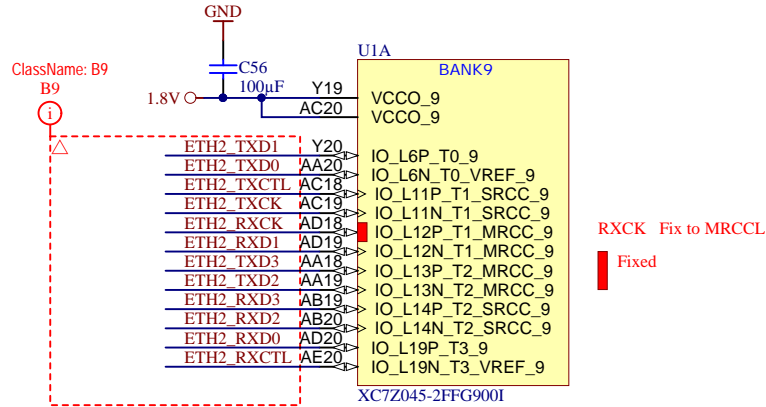
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VCCO_MIO0_500	PS_MIO1_500	D23	SPI_CS
VCCO_MIO0_500	PS_MIO2_500	F23	SPI_DQ0/MIO2
	PS_MIO3_500	C23	SPI_DQ1/MIO3
	PS_MIO4_500	E23	SPI_DQ2/MIO4
	PS_MIO5_500	C24	SPI_DQ3/MIO5
	PS_MIO6_500	D24	SPI_SCK/MIO6
	PS_MIO7_500	B24	ETH1_RESET33
	PS_MIO8_500	C21	MIO8
	PS_MIO9_500	A24	MIO9
	PS_MIO10_500	E22	MMC-D0
	PS_MIO11_500	A23	MMC-CMD
	PS_MIO12_500	E21	MMC-CCLK
	PS_MIO13_500	F22	MMC-D1
	PS_MIO14_500	B22	MMC-D2
	PS_MIO15_500	C22	MMC-D3
	PS_MIO16_501	L19	ETH1_TXCK
	PS_MIO17_501	K21	ETH1_TXD0
	PS_MIO18_501	K20	ETH1_TXD1
	PS_MIO19_501	J20	ETH1_TXD2
	PS_MIO20_501	M20	ETH1_TXD3
	PS_MIO21_501	J19	ETH1_TXCTL
	PS_MIO22_501	L20	ETH1_RXCK
	PS_MIO23_501	J21	ETH1_RXD0
	PS_MIO24_501	M19	ETH1_RXD1
	PS_MIO25_501	G19	ETH1_RXD2
	PS_MIO26_501	M17	ETH1_RXD3
	PS_MIO27_501	G20	ETH1_RXCTL
	PS_MIO28_501	L17	
	PS_MIO29_501	H22	
	PS_MIO30_501	L18	
	PS_MIO31_501	H21	
	PS_MIO32_501	K17	
	PS_MIO33_501	G22	
	PS_MIO34_501	K18	
	PS_MIO35_501	G21	
	PS_MIO36_501	H17	
	PS_MIO37_501	B21	
	PS_MIO38_501	A20	
	PS_MIO39_501	F18	
	PS_MIO40_501	B20	SDIO-CCLK
	PS_MIO41_501	J18	SDIO-CMD
	PS_MIO42_501	D20	SDIO-D0
	PS_MIO43_501	E18	SDIO-D1
	PS_MIO44_501	E20	SDIO-D2
	PS_MIO45_501	H18	SDIO-D3
	PS_MIO46_501	F20	PS_MIO46
	PS_MIO47_501	A18	PS_MIO47
	PS_MIO48_501	C19	PS_MIO48
	PS_MIO49_501	D18	PS_MIO49
	PS_MIO50_501	A19	PS_MIO50
	PS_MIO51_501	F19	PS_MIO51
	PS_MIO52_501	D19	ETH1_MDC
	PS_MIO53_501	C18	ETH1_MDIO


XC7Z045-2FFG9001

B501
ClassName: B501
ClassName: PKG

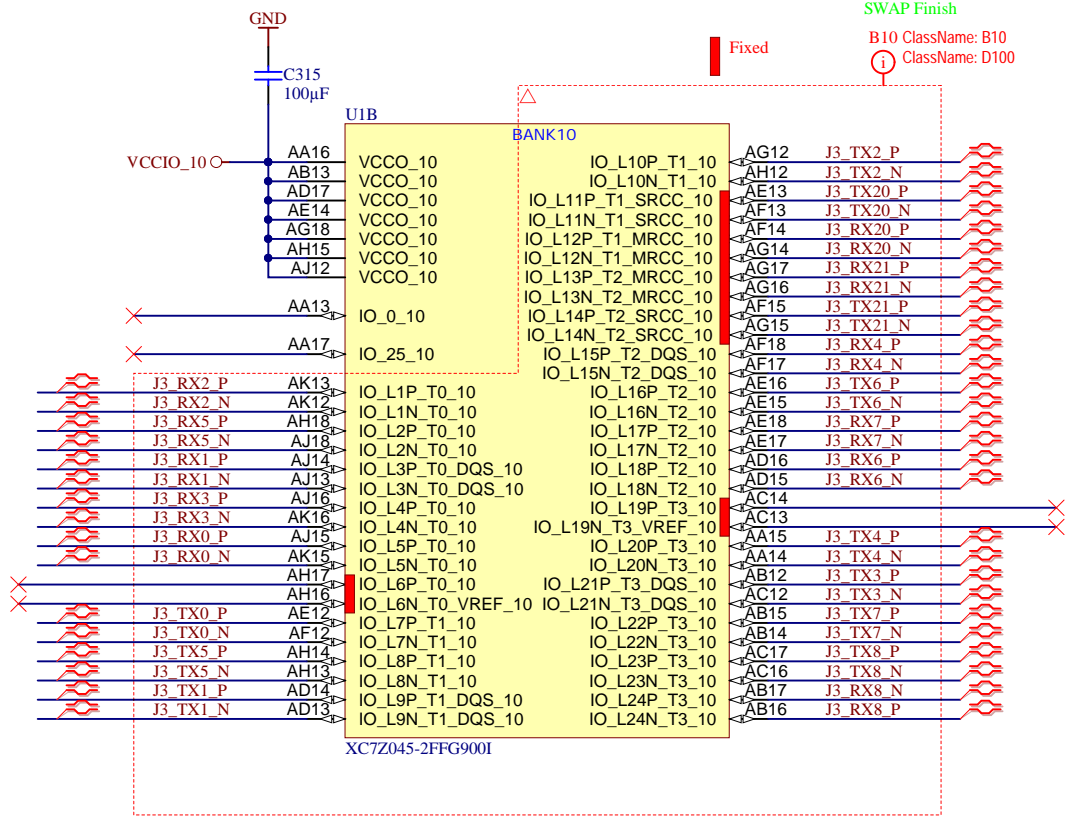


Title: TE0784 - FPGA MIO Banks		
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Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 10 of 30
Filename: MIO-BANKS.SchDoc		

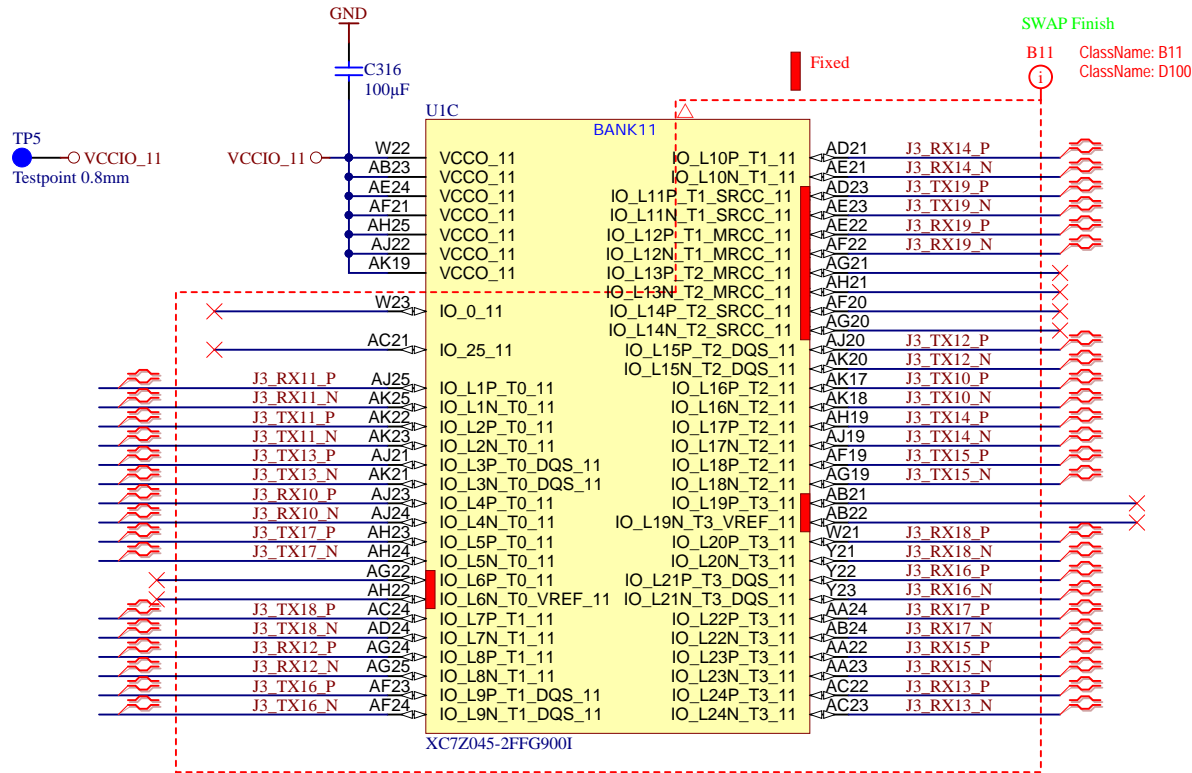



			Title: TE0784 - FPGA B9	
			A4	Number: TE0784 045-2I
Date: 25.06.2018		Copyright: Trenz Electronic GmbH		Page 11 of 30
Filename: B9.SchDoc				


TP4
 ●—○ VCCIO_10
 Testpoint 0.8mm

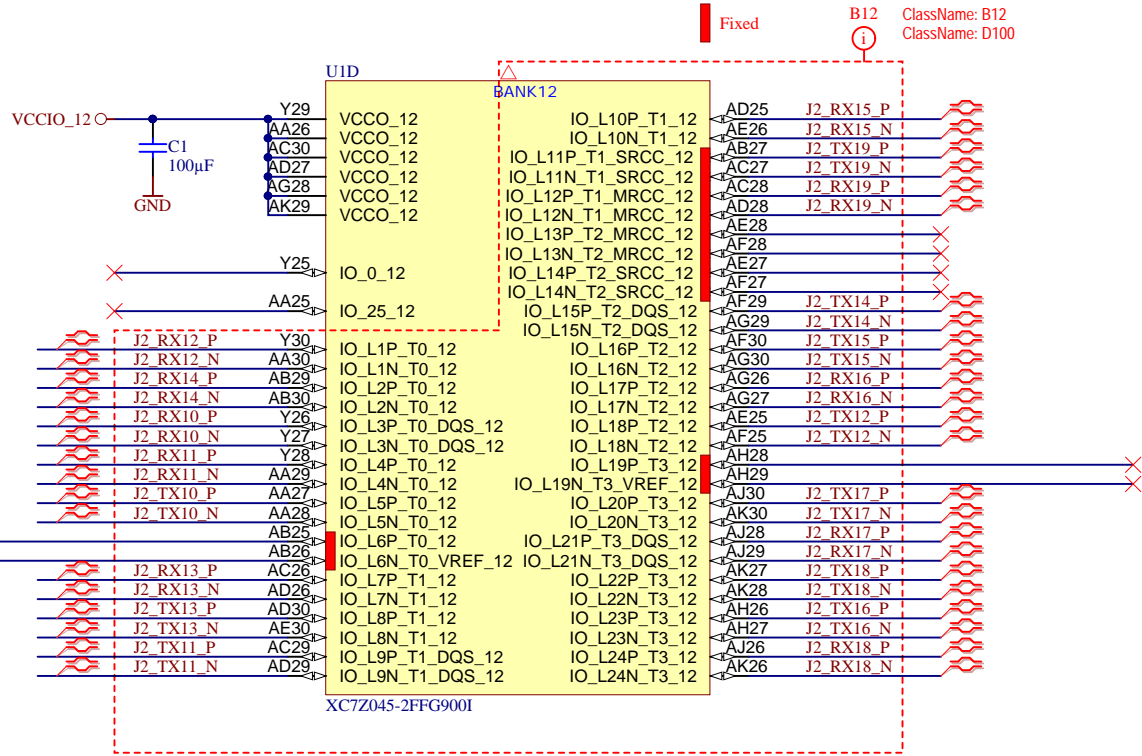


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Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 12 of 30
Filename: B10.SchDoc		




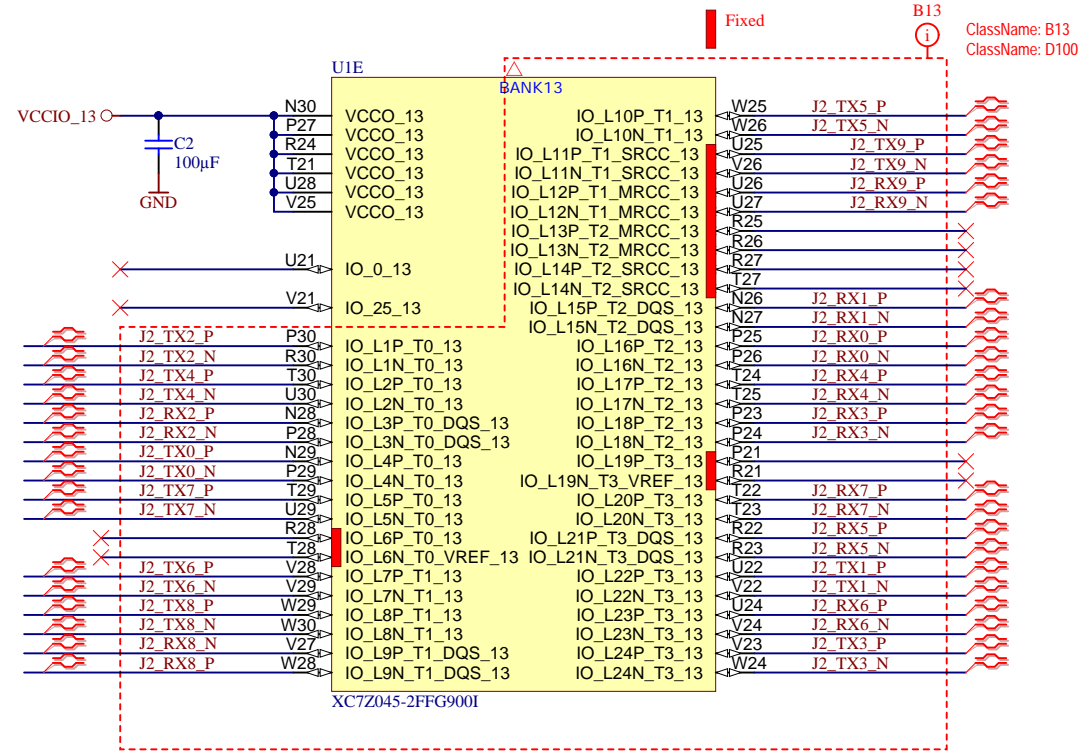
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		A4	Number: TE0784 045-2I
Date: 25.06.2018		Copyright: Trenz Electronic GmbH	
Page 13 of 30		Filename: B11.SchDoc	


TP1
 VCCIO_12
 Testpoint 0.8mm



Title: TE0784 - FPGA B12		
A4	Number: TE0784 045-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 14 of 30
Filename: B12.SchDoc		

TP2

 Testpoint 0.8mm



	Title: TE0784 - FPGA B13		
	A4	Number: TE0784 045-2I	Rev. 01
	Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 15 of 30
	Filename: B13.SchDoc		

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U_B33
B33.SchDoc



U_B34
B34.SchDoc



U_B35
B35.SchDoc



A

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D

D

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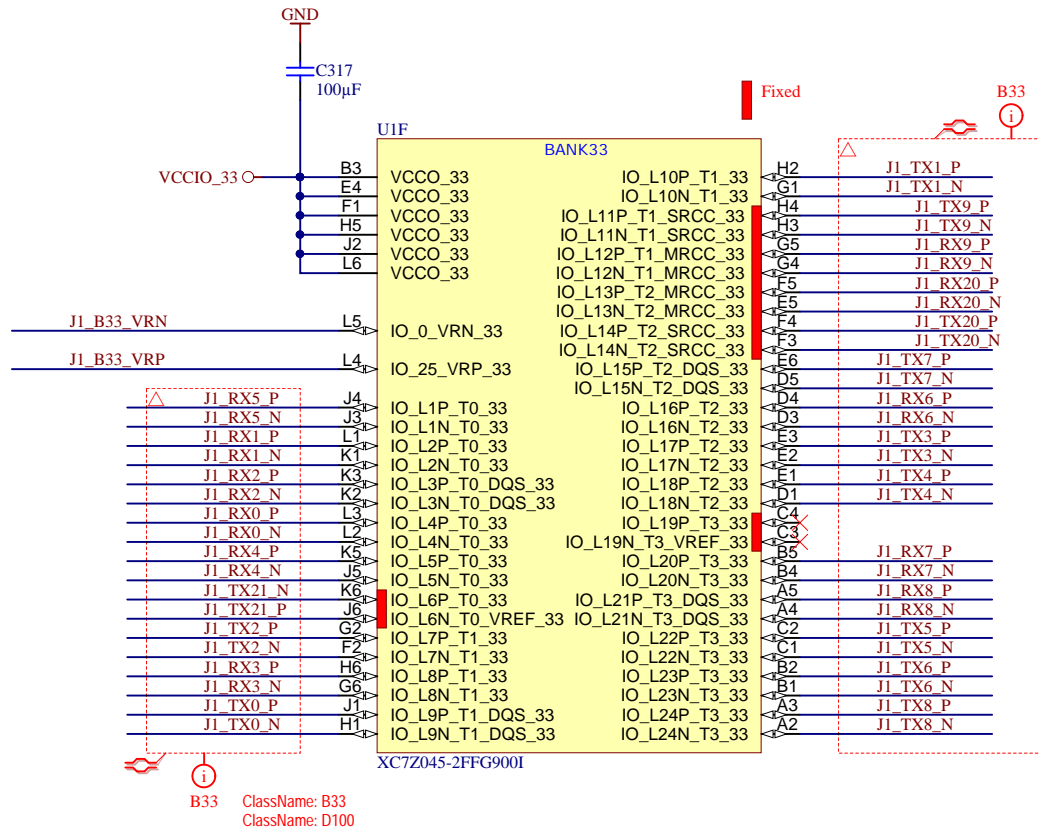
3

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Title: TE0784 - FPGA HP Banks		
A4	Number: TE0784 045-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 16 of 30
Filename: HP-BANKS.SchDoc		


TP6
 VCCIO_33
 Testpoint 0.8mm

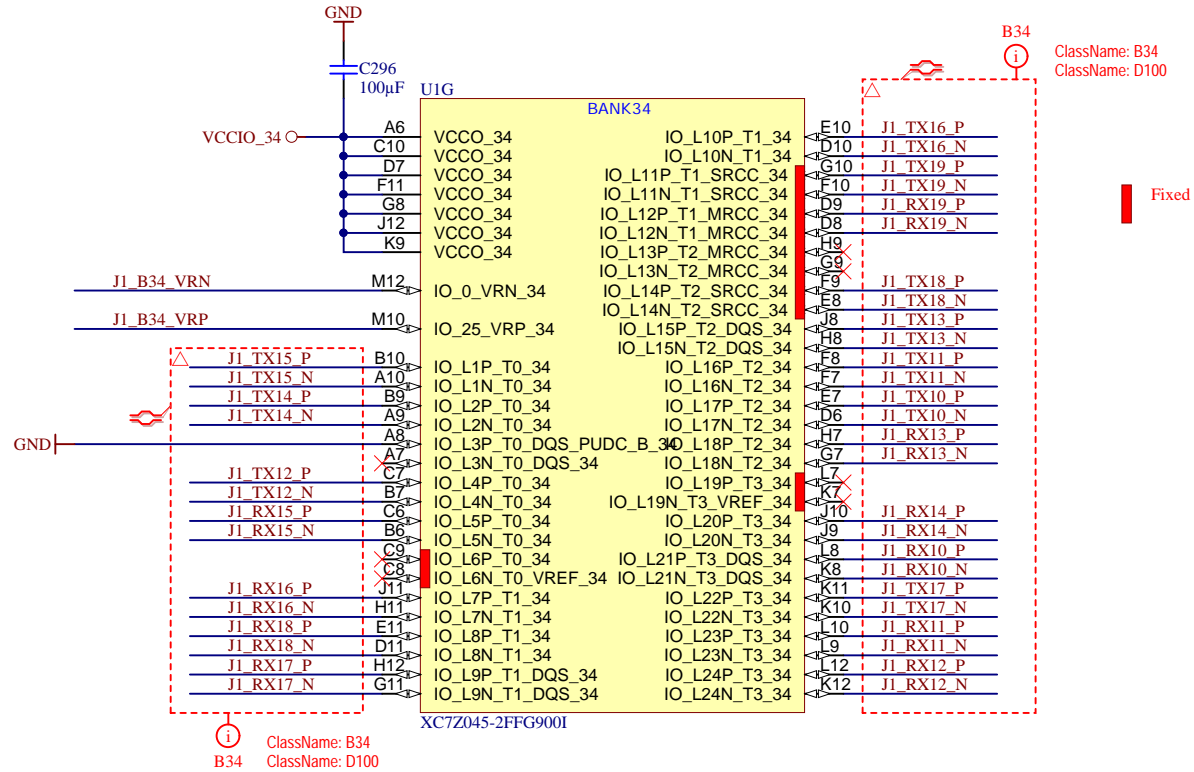


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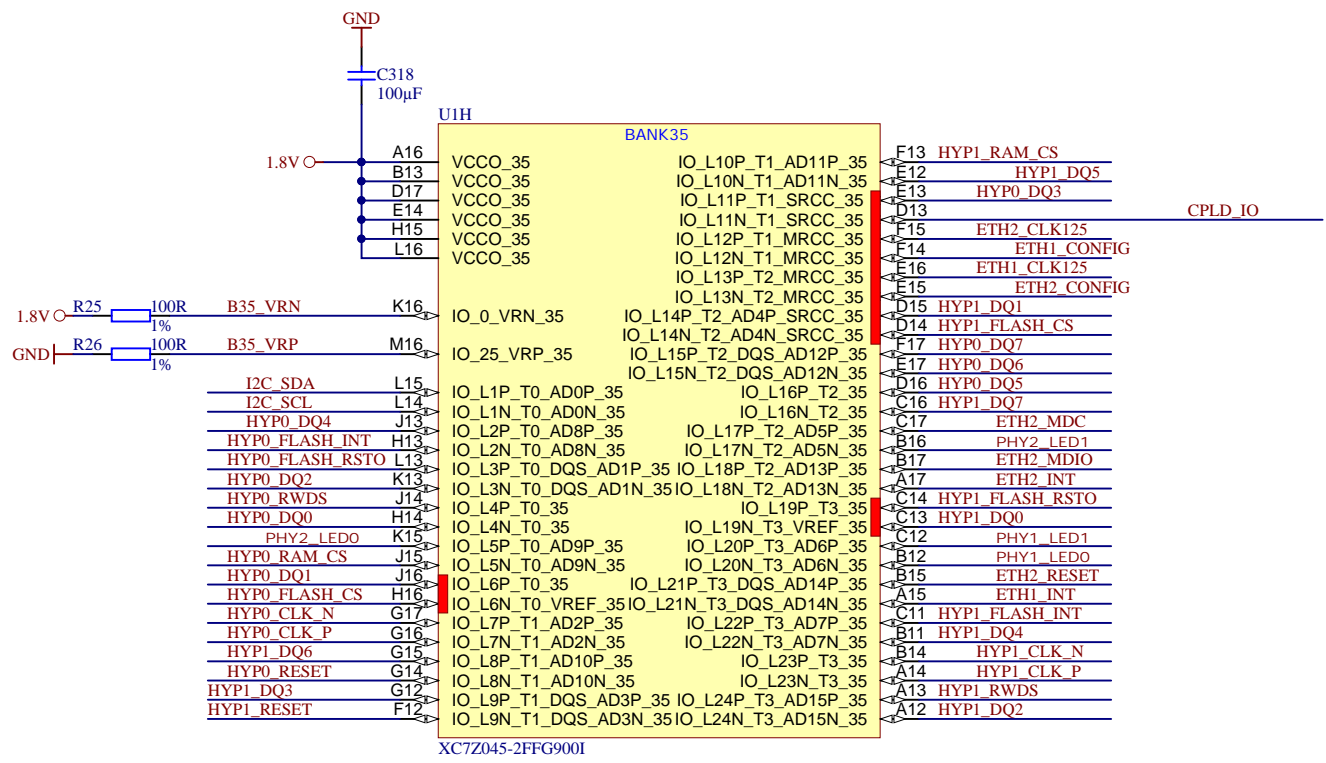


Title: TE0784 - FPGA B33		
A4	Number: TE0784 045-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 17 of 30
Filename: B33.SchDoc		

TP3
 VCCIO_34
 Testpoint 0.8mm

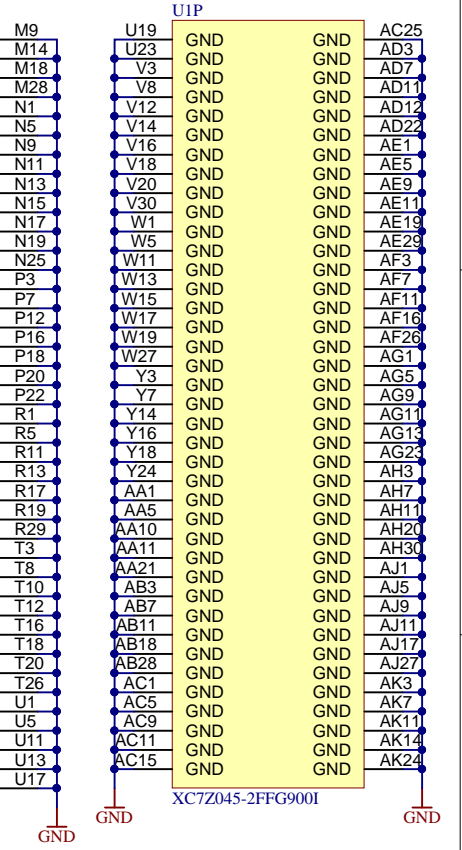
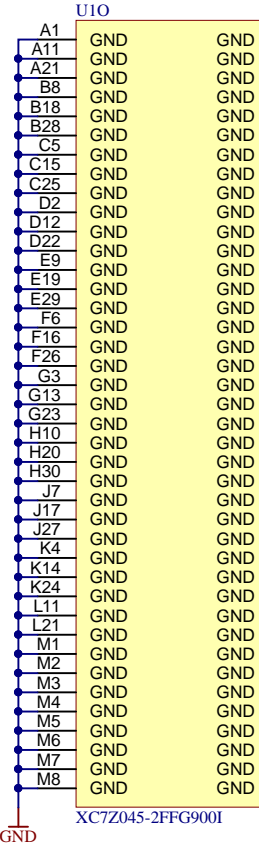
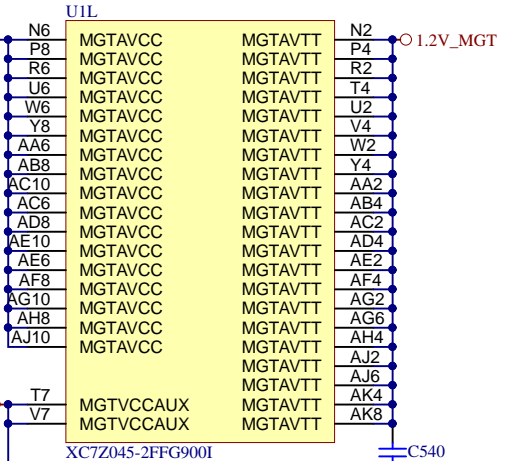
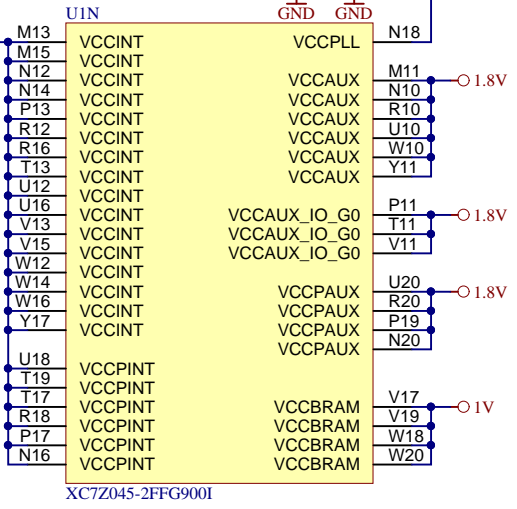
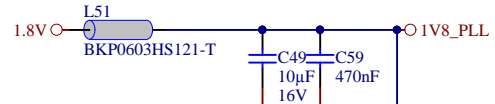
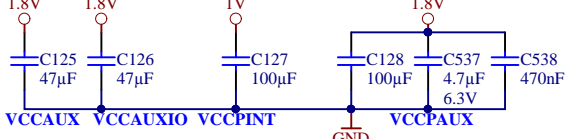
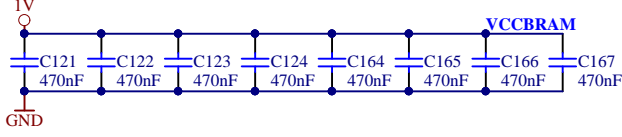
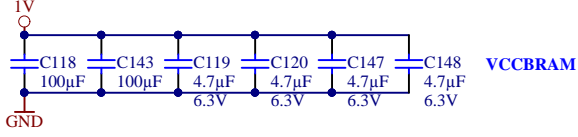
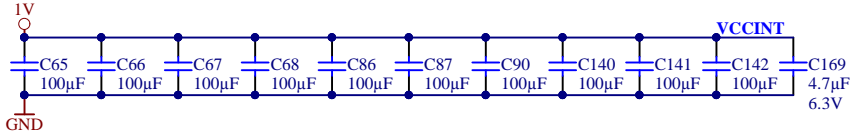
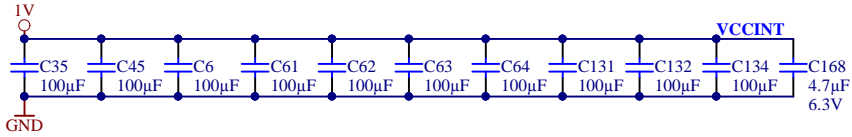


Title: TE0784 - FPGA B34		
A4	Number: TE0784 045-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page18 of 30
Filename: B34.SchDoc		



Title: TE0784 - FPGA B35		
A4	Number: TE0784 045-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 19 of 30
Filename: B35.SchDoc		

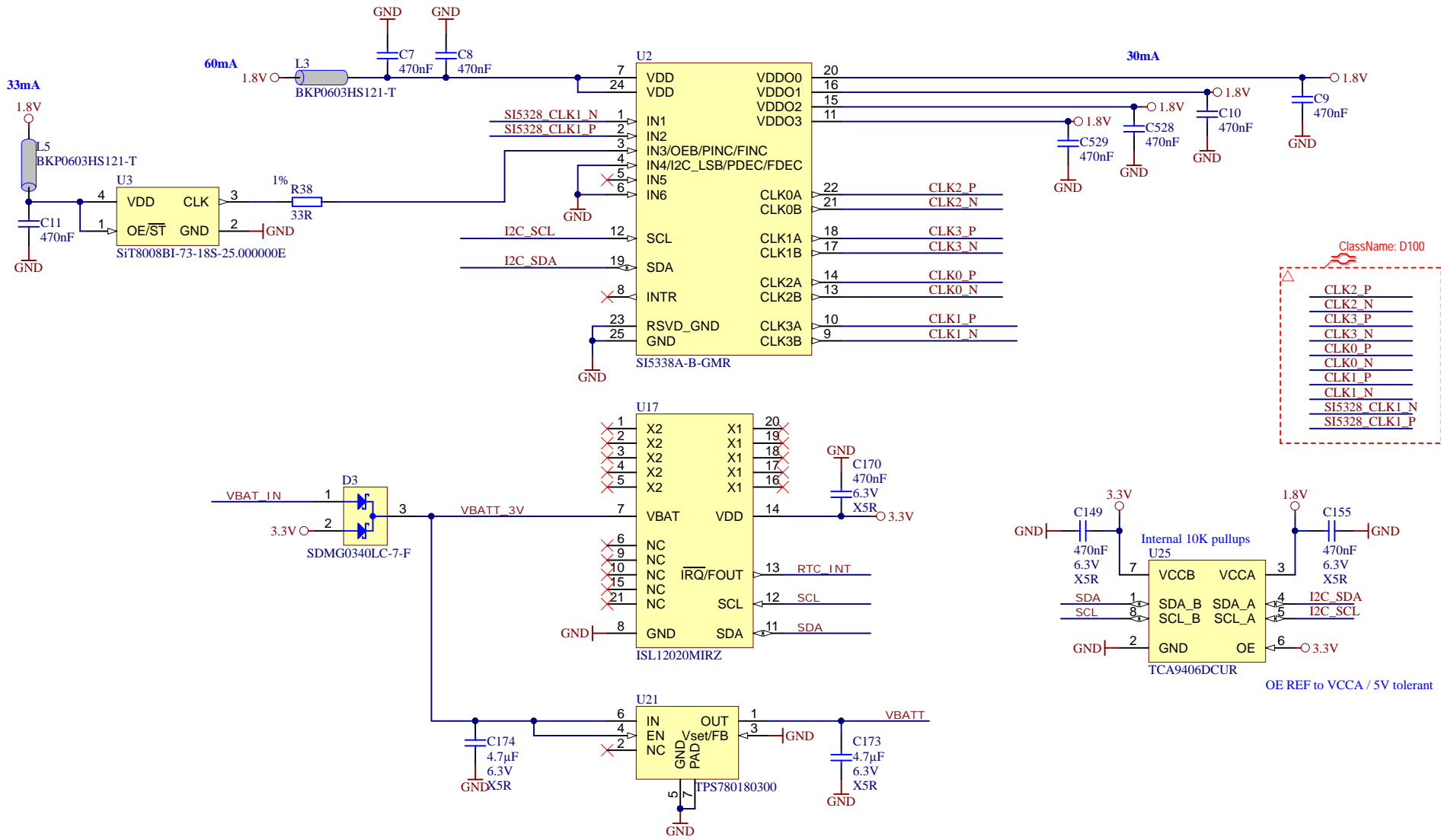
Capacitors suitable for XC7Z100



D



Title: TE0784 - ZYNQ POWER		
A4	Number: TE0784 045-21	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 20 of 30
Filename: FPGA-PWR.SchDoc		



ClassName: D100

- CLK2_P
- CLK2_N
- CLK3_P
- CLK3_N
- CLK0_P
- CLK0_N
- CLK1_P
- CLK1_N
- SI5328_CLK1_N
- SI5328_CLK1_P

OE REF to VCCA / 5V tolerant



Title: TE0784 - Clock		
A4	Number: TE0784 045-21	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page21 of 30
Filename: Clock.SchDoc		

A

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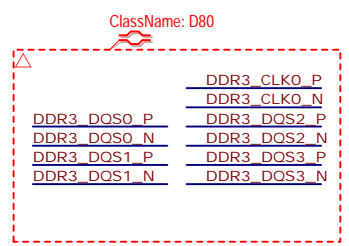
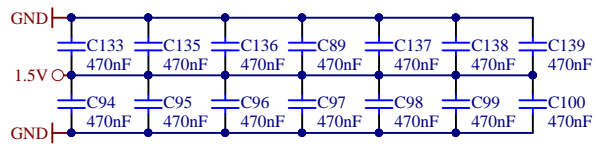
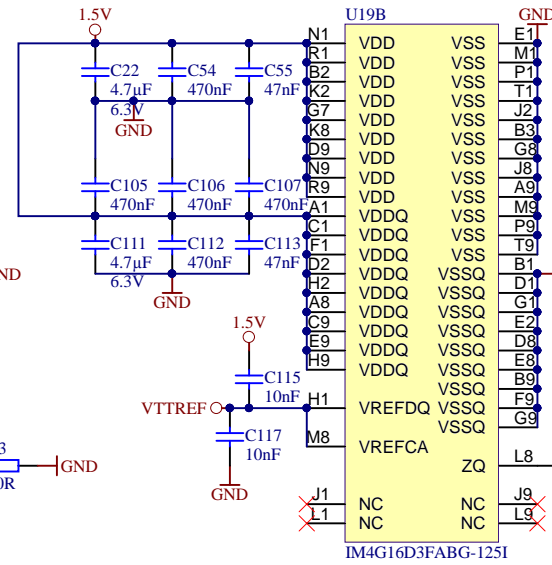
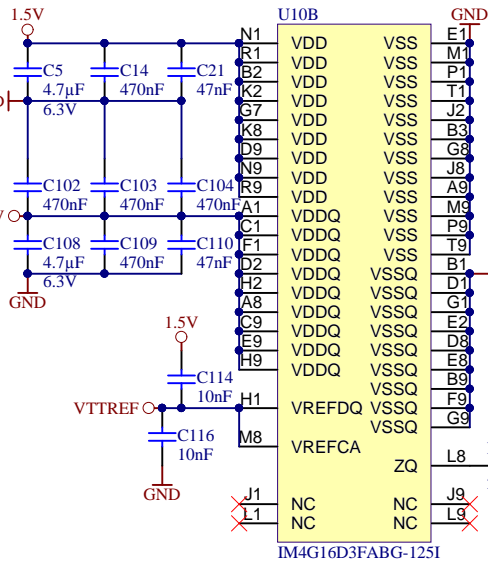
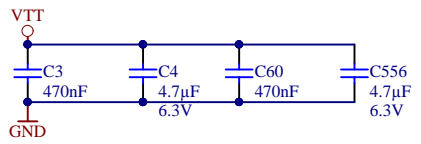
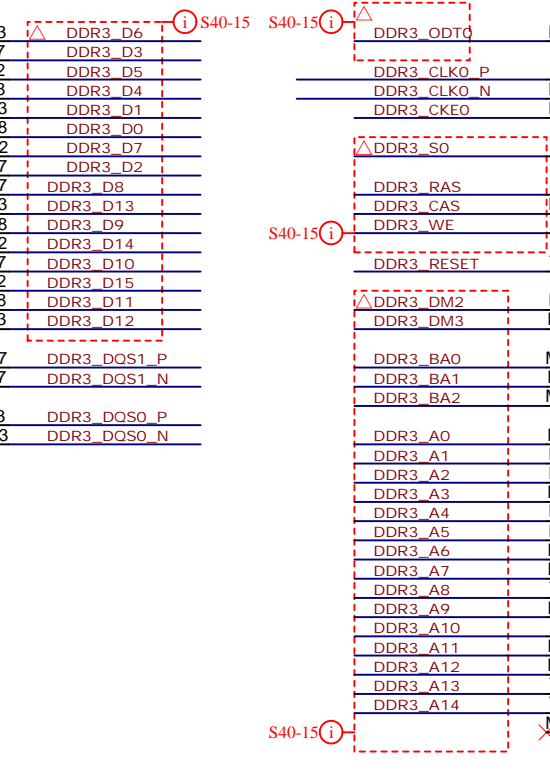
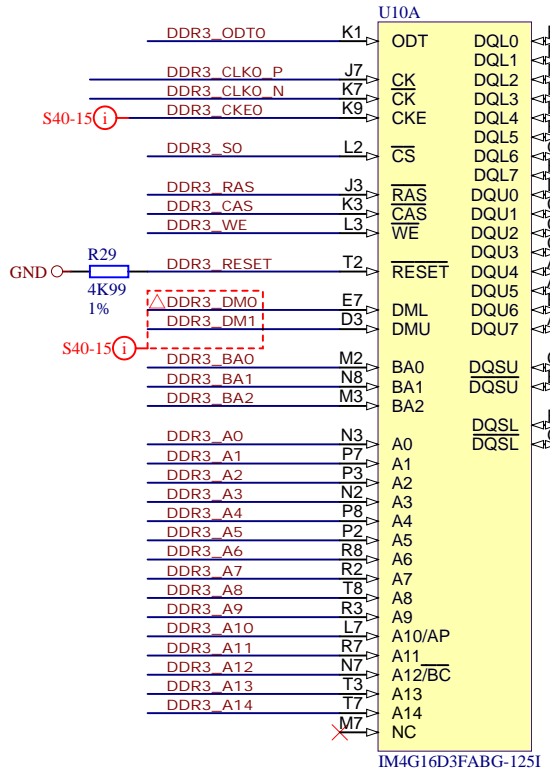
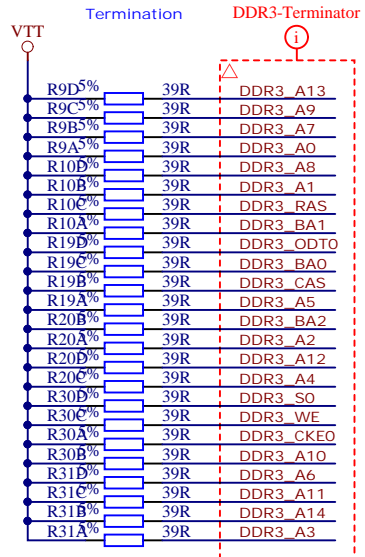
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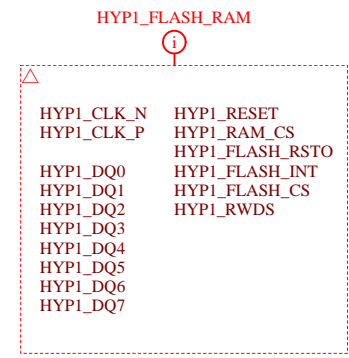
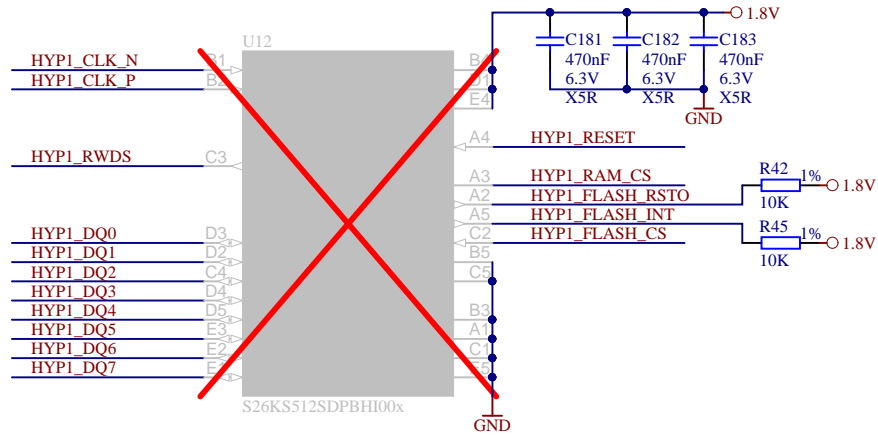
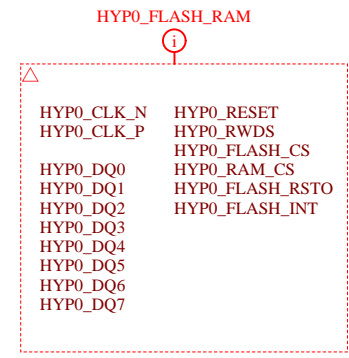
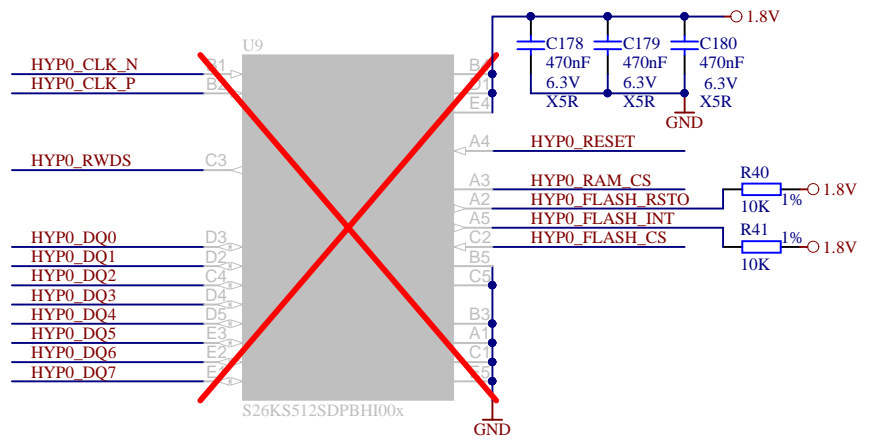
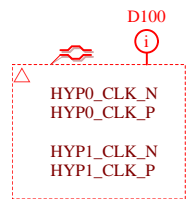
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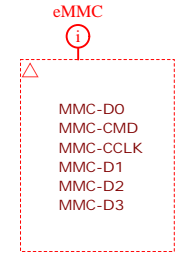
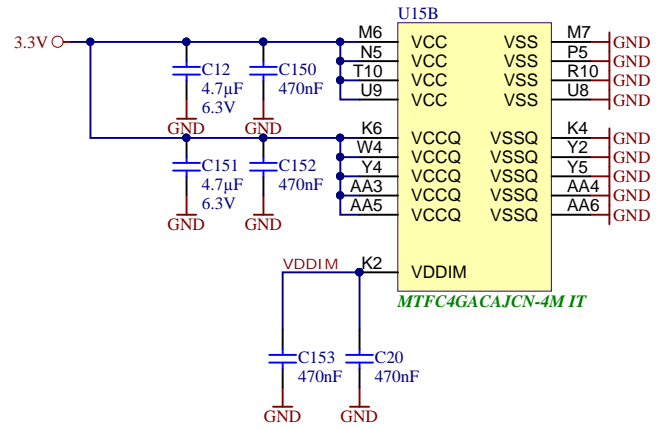
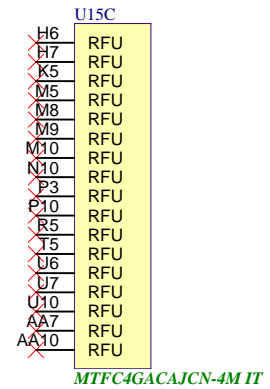
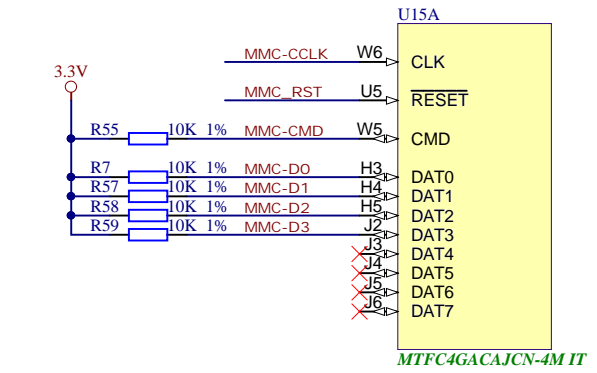
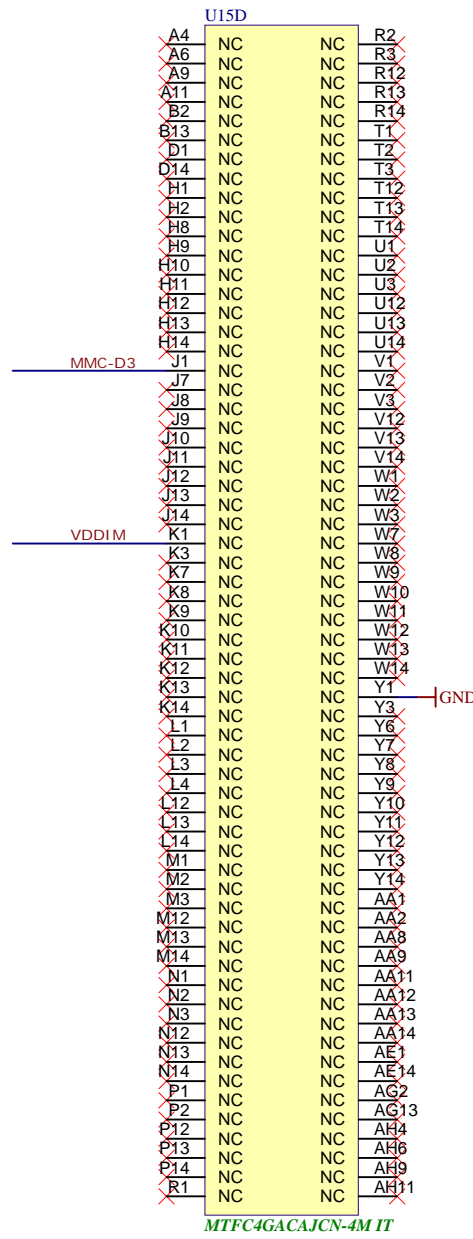
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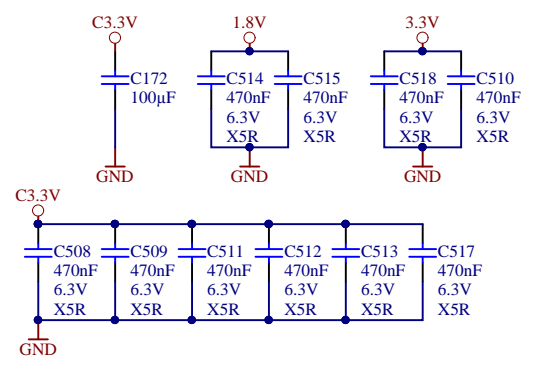
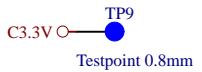
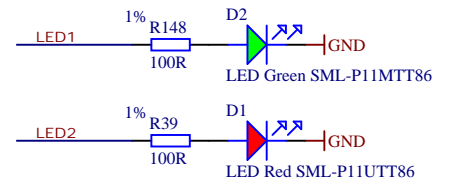
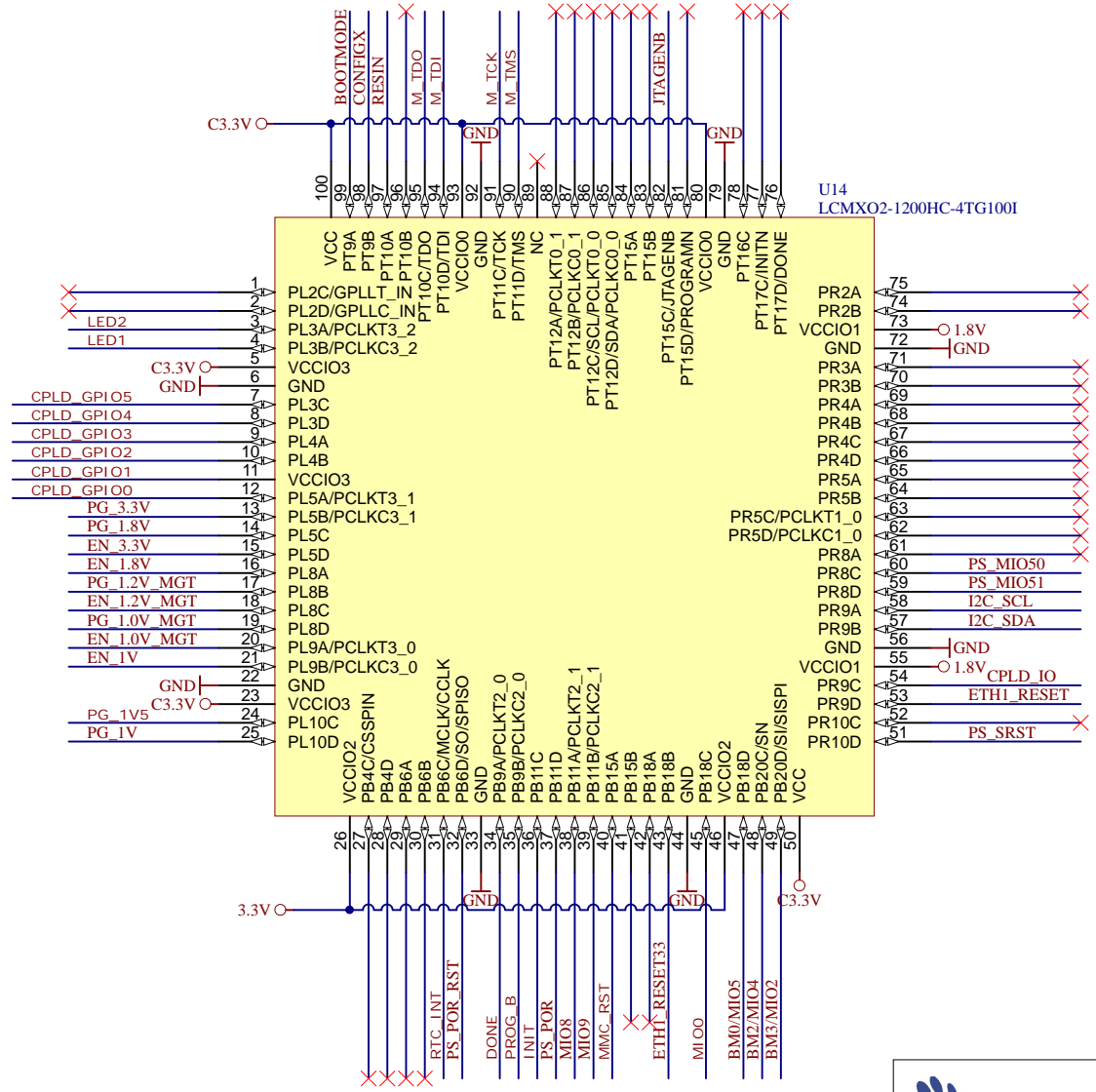


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Title: TE0784 - CPLD		
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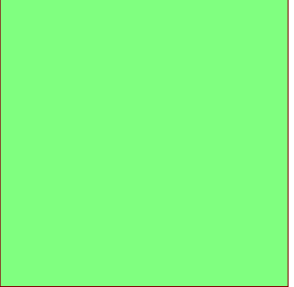
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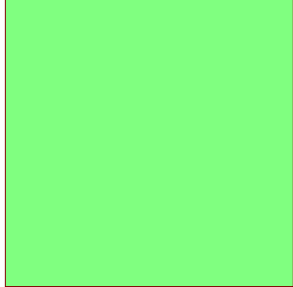
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4

U_ETH1
ETH1.SchDoc



U_ETH2
ETH2.SchDoc



A

A

B

B

C

C

D

D



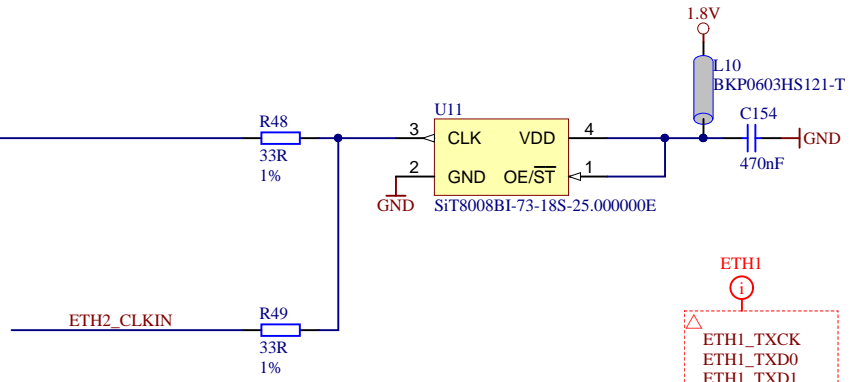
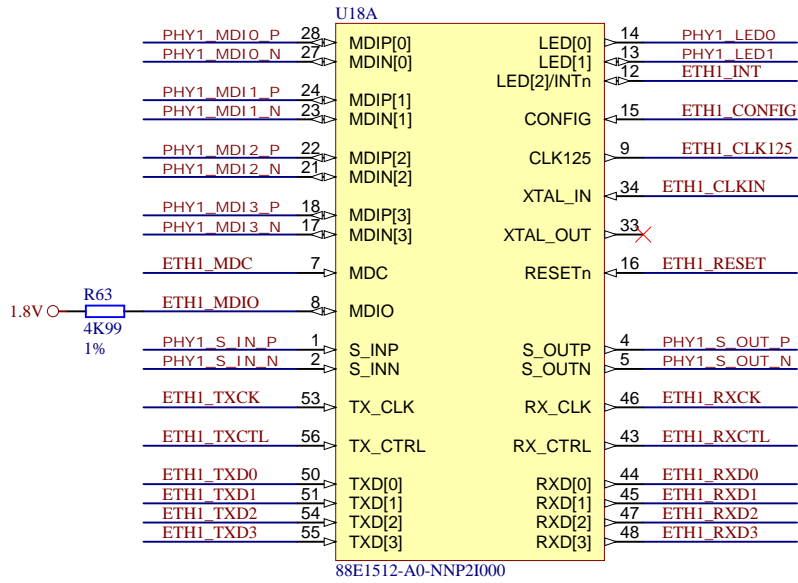
Title: TE0784 - Ethernet		
A4	Number: TE0784 045-2I	Rev. 01
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Filename: Ethernet.SchDoc		

1

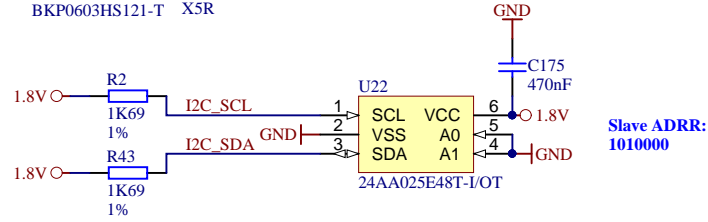
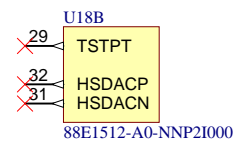
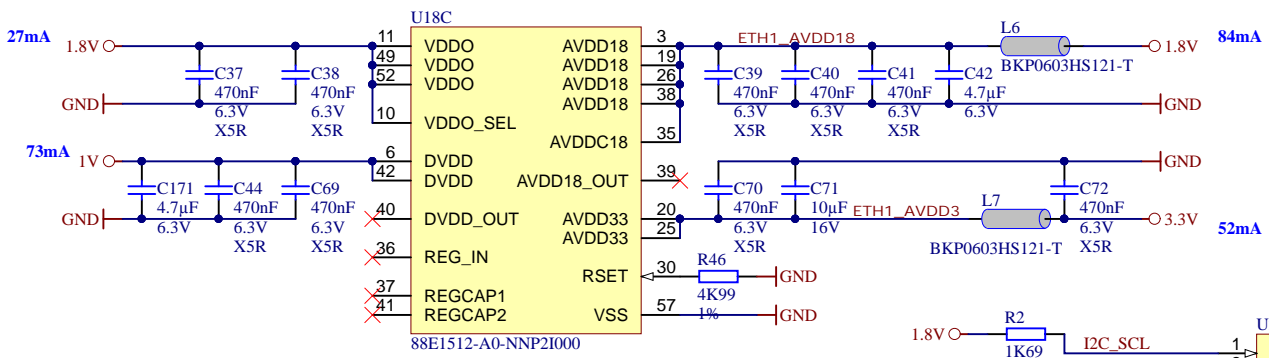
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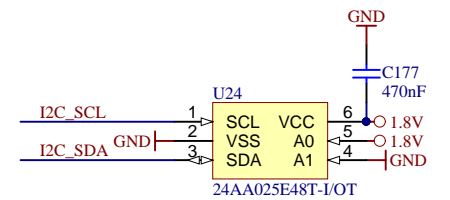
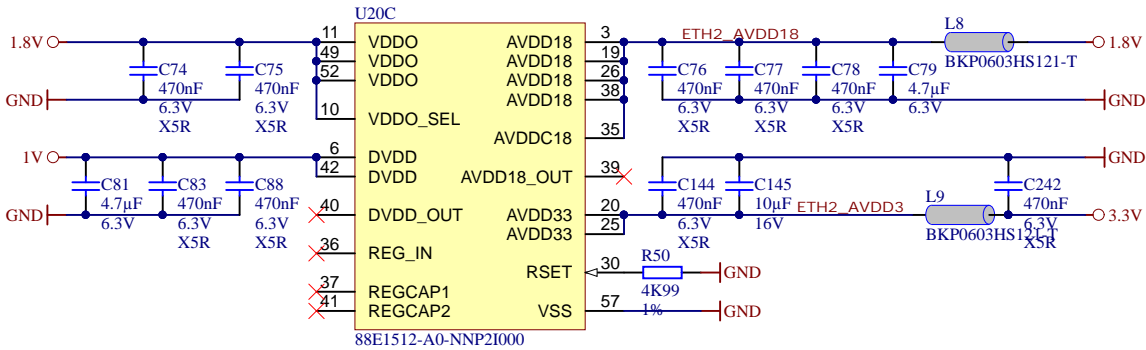
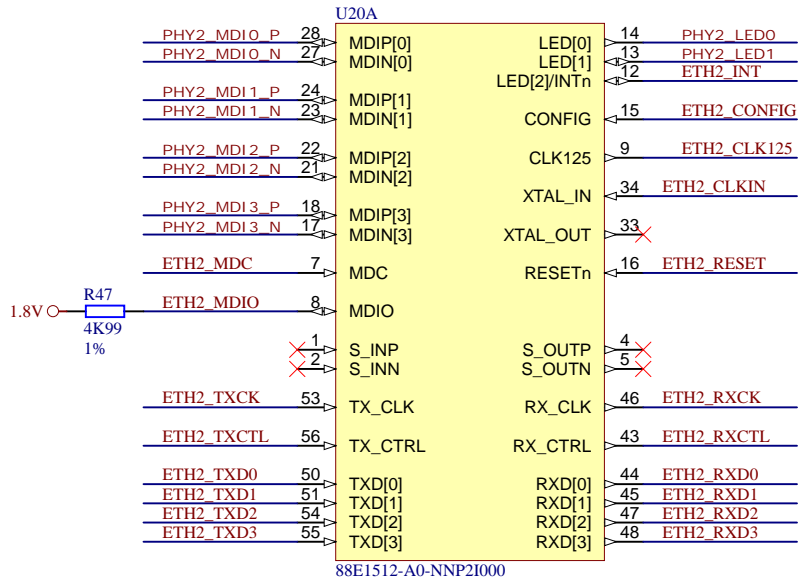
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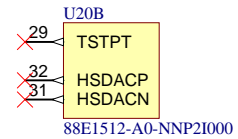
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- ETH1_TXCK
 - ETH1_TXD0
 - ETH1_TXD1
 - ETH1_TXD2
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 - ETH1_TXCTL
 - ETH1_RXCK
 - ETH1_RXD0
 - ETH1_RXD1
 - ETH1_RXD2
 - ETH1_RXD3
 - ETH1_RXCTL
 - ETH1_MDC
 - ETH1_MDIO
- PHY1_LED0
 PHY1_LED1
 ETH1_INT
 ETH1_CONFIG
 ETH1_CLK125
 ETH1_RESET



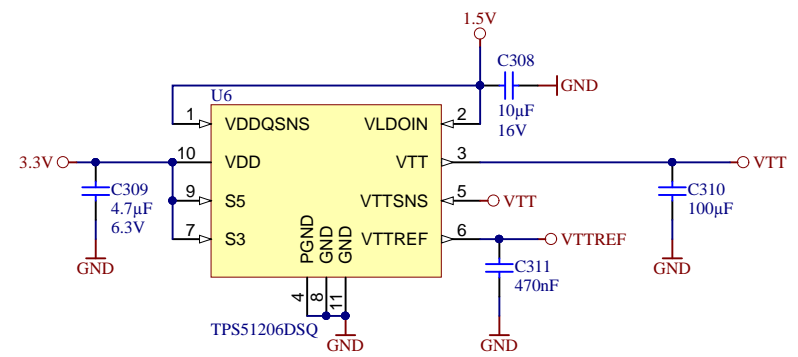
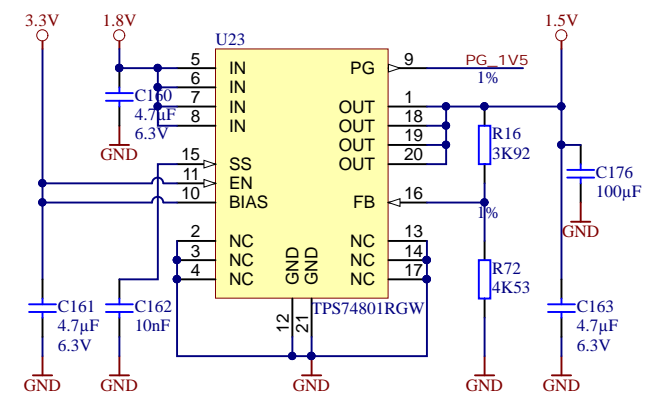
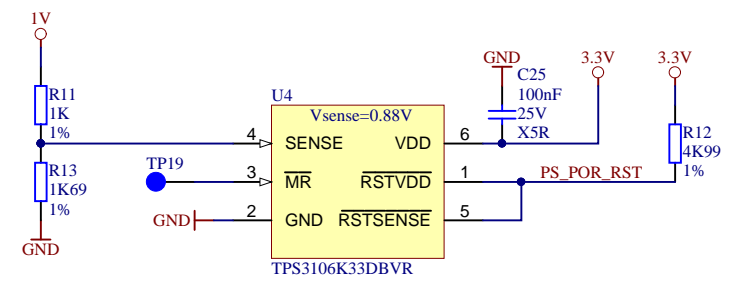
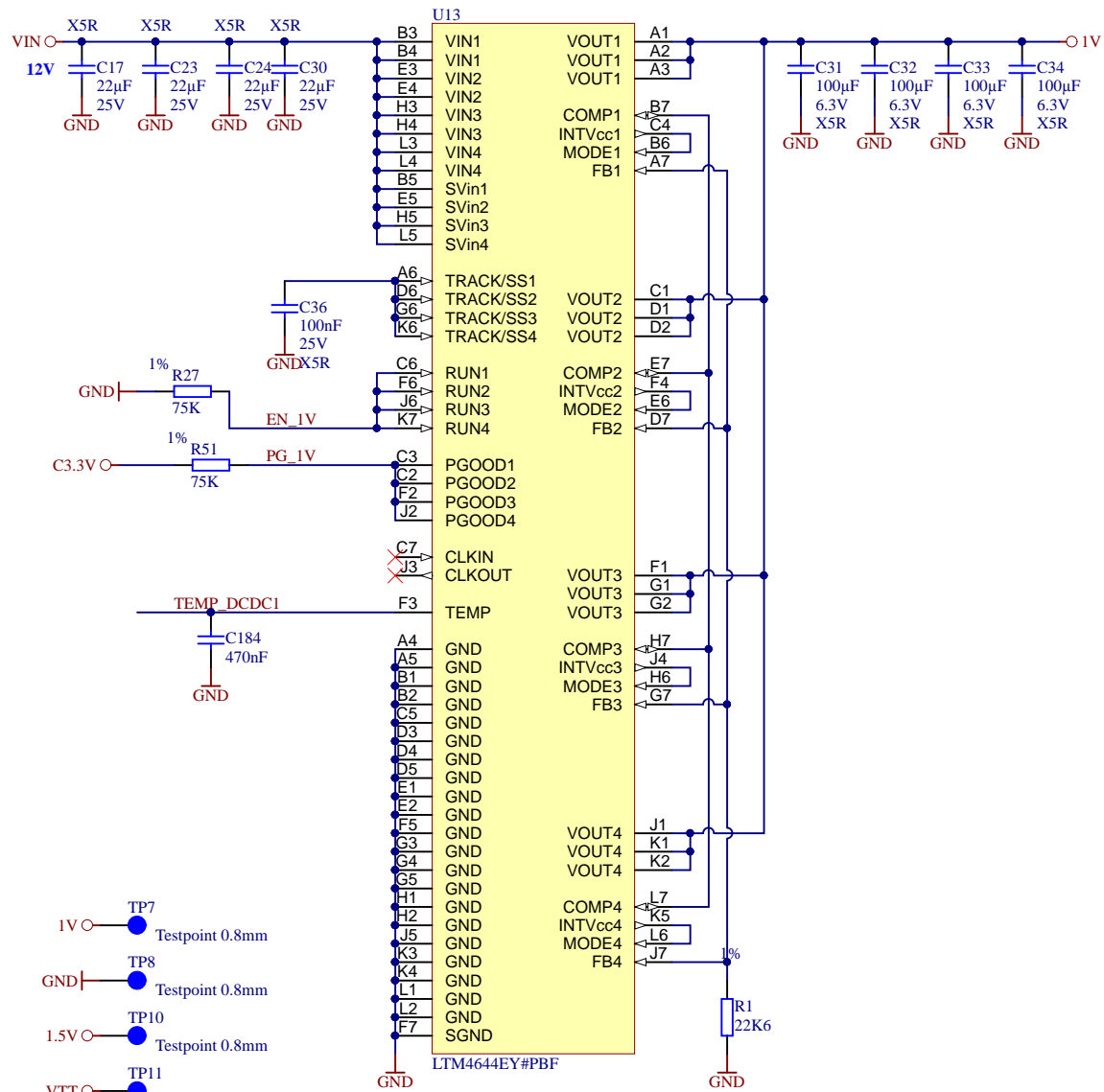
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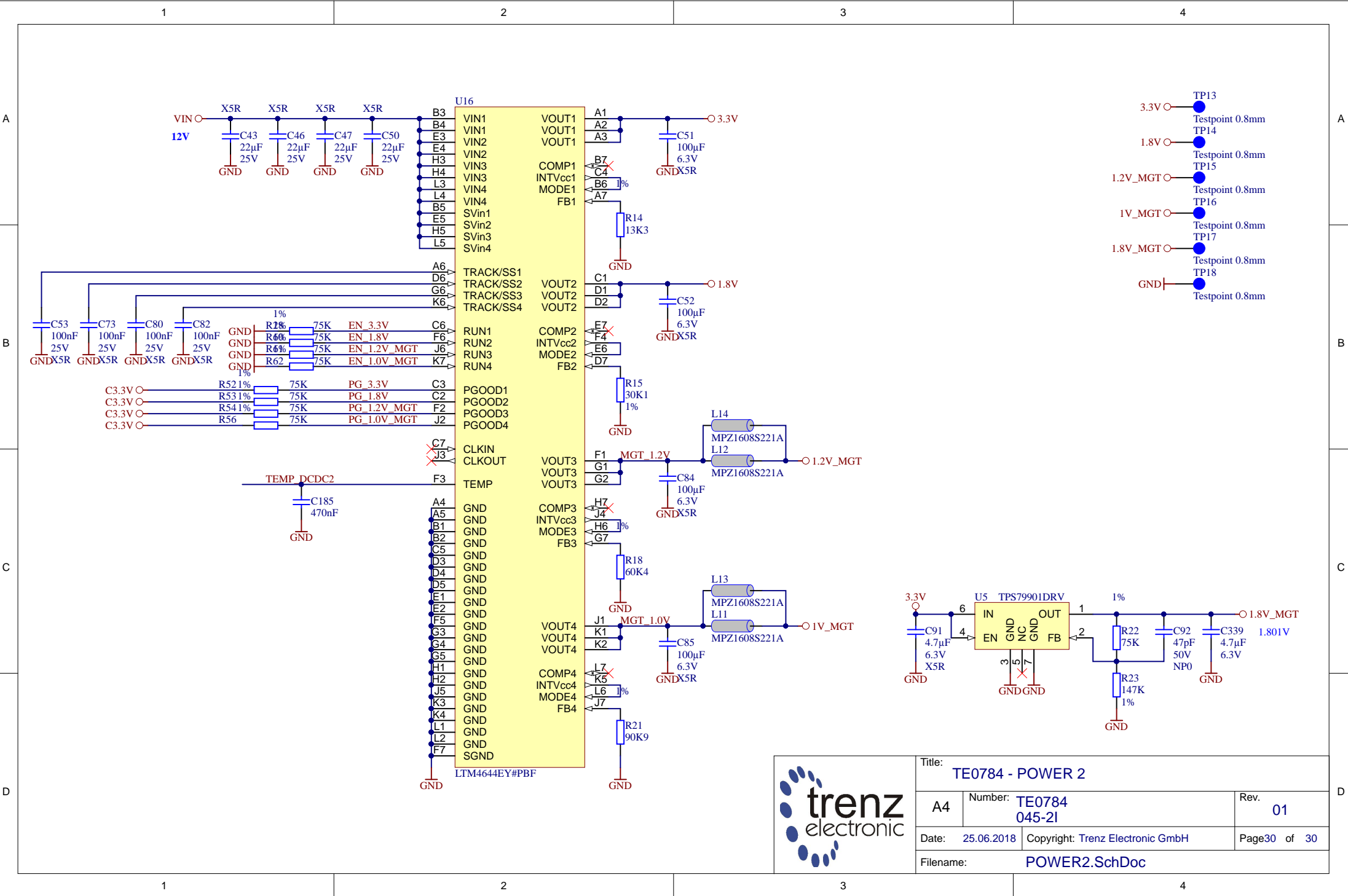
Slave ADDR:
1010001



Title: TE0784 - ETH_PHY2		
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