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U_DDR3-RAM
DDR3-RAM.SchDoc

U_Ethernet
Ethernet.SchDoc

U_SOC
SOC.SchDoc

U_CPLD
CPLD.SchDoc

U_POWER2
POWER2.SchDoc

U_HyperFlash_RAM
HyperFlash_RAM.SchDoc

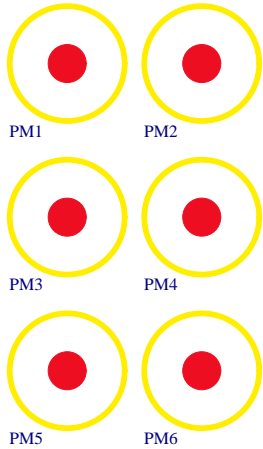
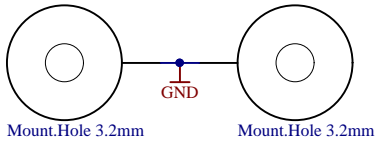
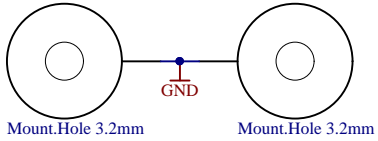
U_Clock
Clock.SchDoc

U_eMMC
eMMC.SchDoc

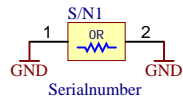
U_Connectors
Connectors.SchDoc

U_POWER
POWER.SchDoc

LOGO1
TE Logo PRINT Layer
LOGO PRINT



Serial
Serialnumber 6,3 x 6.3mm



Title: TE0784 - Overview		
A4	Number: TE0784 100-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page1 of 30
Filename: TE0784.SchDoc		

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A

A

B

B

C

C

D

D

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A

A

U_HSMC_CONN_J1
HSMC_CONN_J1.SchDoc



U_HSMC_CONN_J2
HSMC_CONN_J2.SchDoc



U_HSMC_CONN_J3
HSMC_CONN_J3.SchDoc



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		Title: TE0784 - Connectors	
		A4	Number: TE0784 100-2I
Date: 25.06.2018		Copyright: Trenz Electronic GmbH	
Filename: Connectors.SchDoc		Page 2 of 30	

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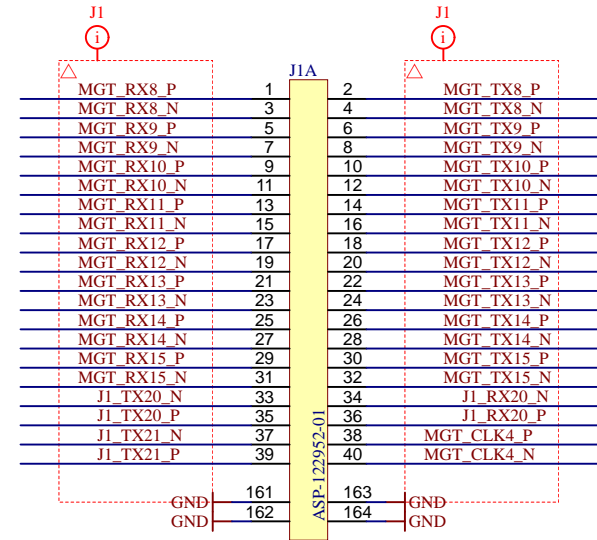
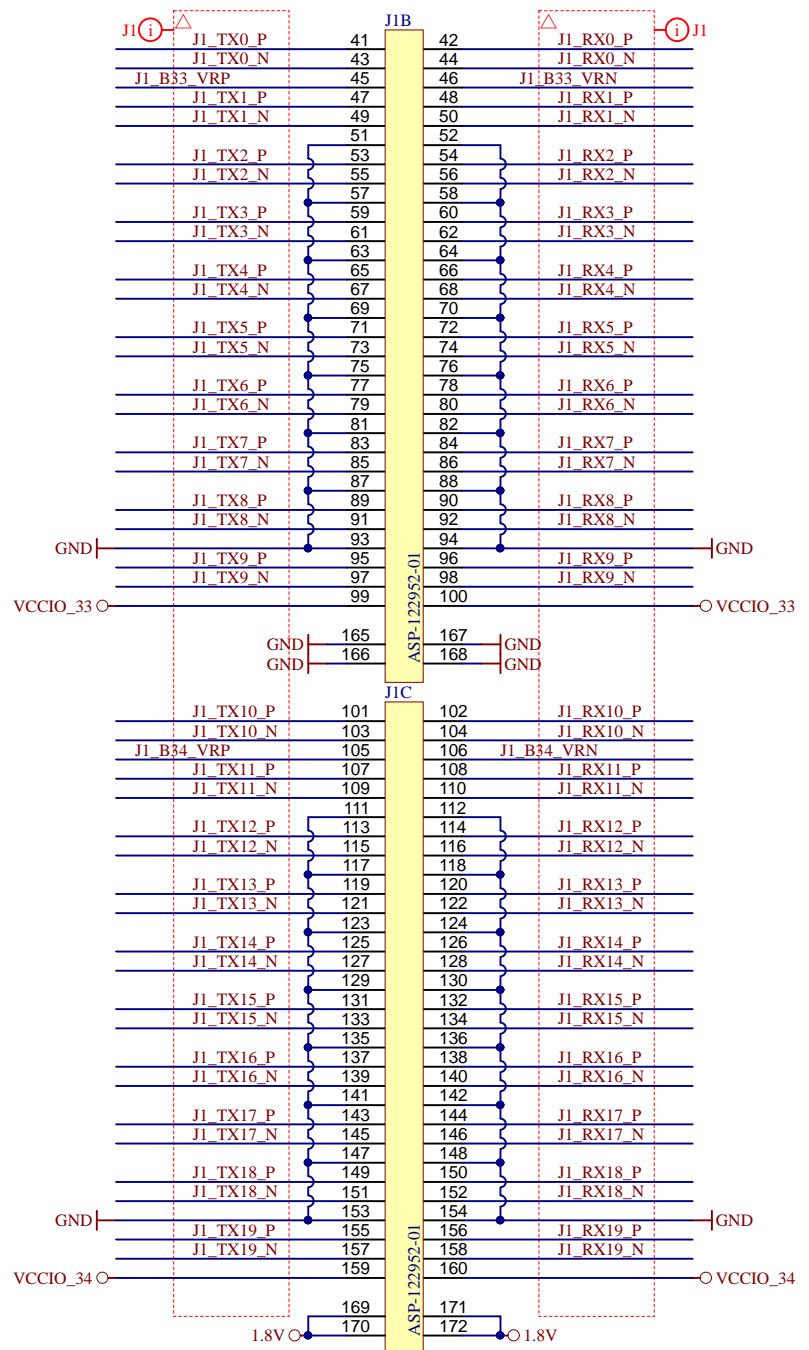
B

C

C

D

D



Title: TE0784 - HSMC_Connector_J1		
A4	Number: TE0784 100-21	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page3 of 30
Filename: HSMC_CONN_J1.SchDoc		

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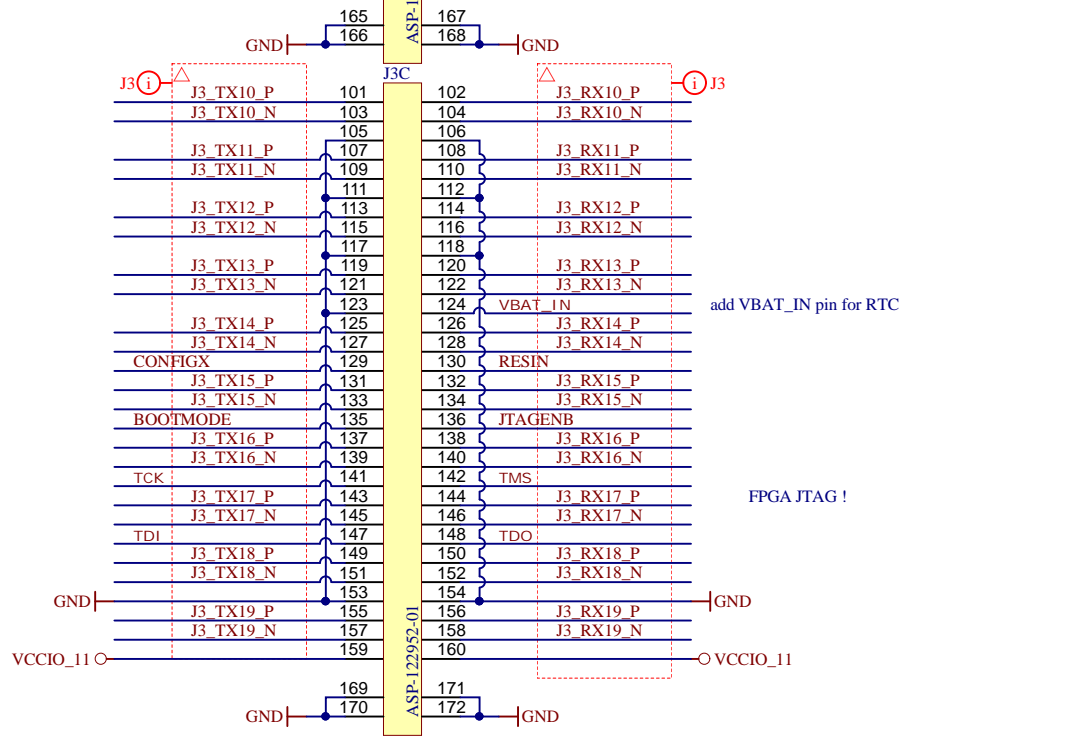
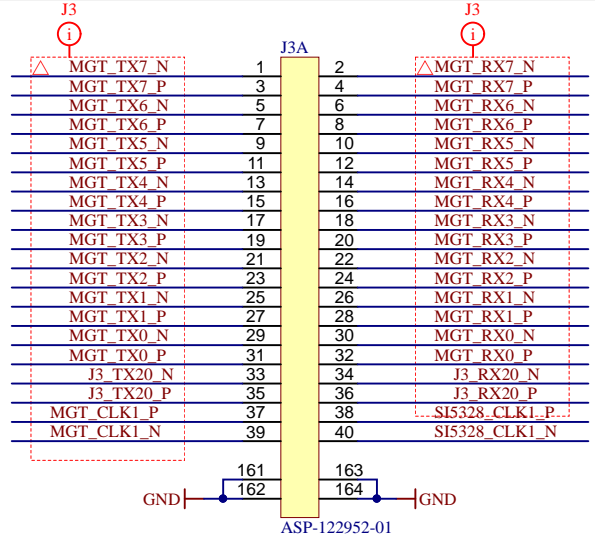
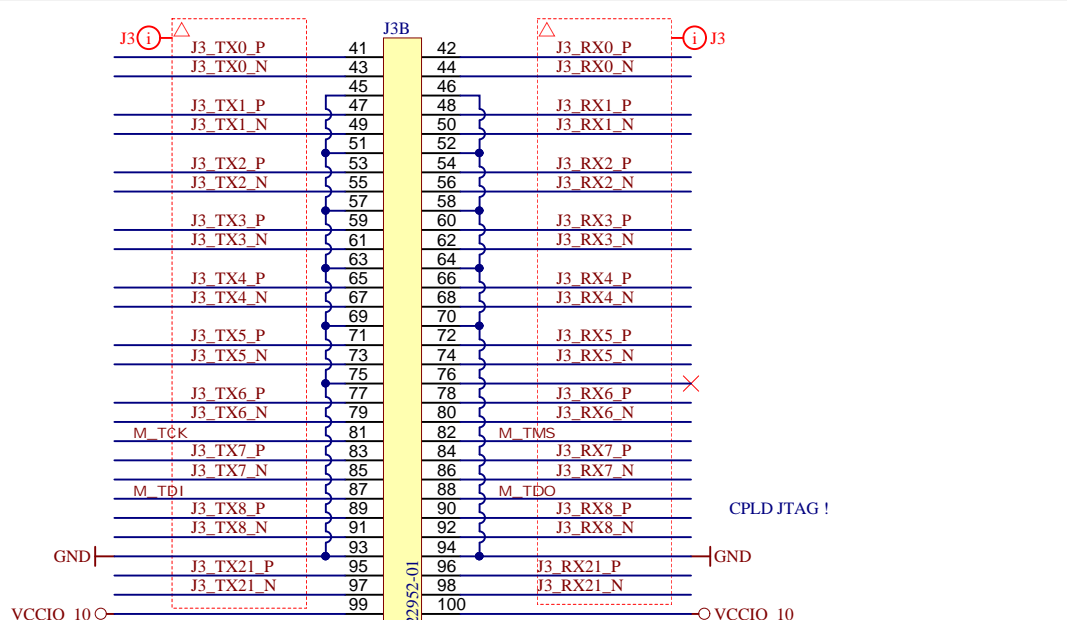
B

C

C

D

D



Title: TE0784 - HSMC_Connector_J3		
A4	Number: TE0784 100-21	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 4 of 30
Filename: HSMC_CONN_J3.SchDoc		

A

A

B

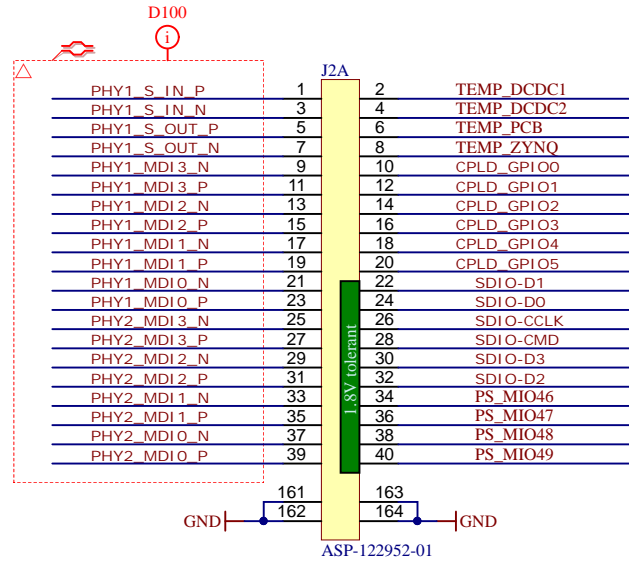
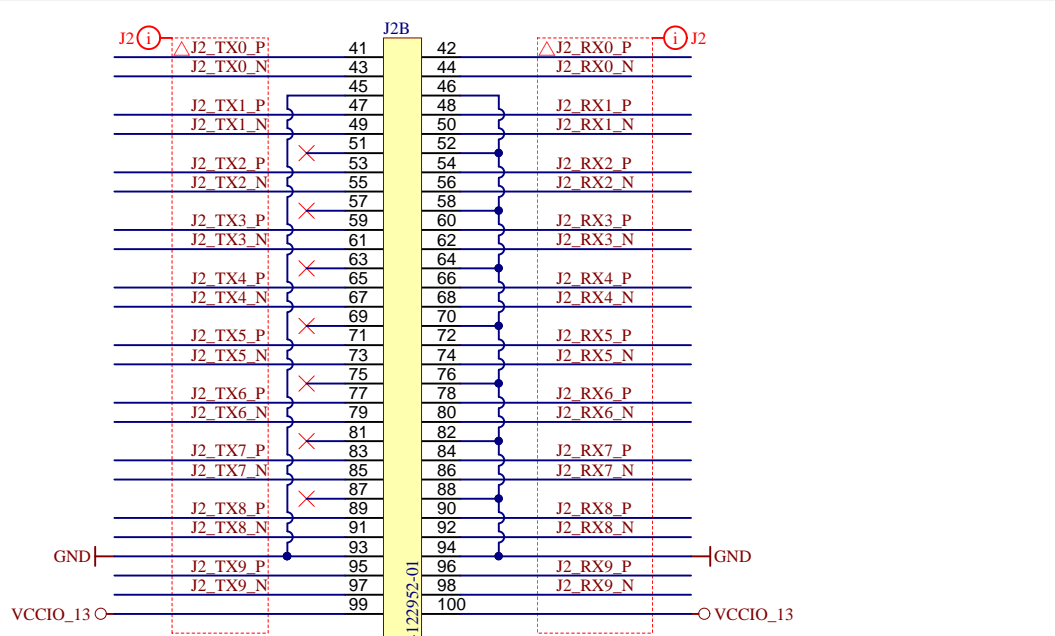
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C

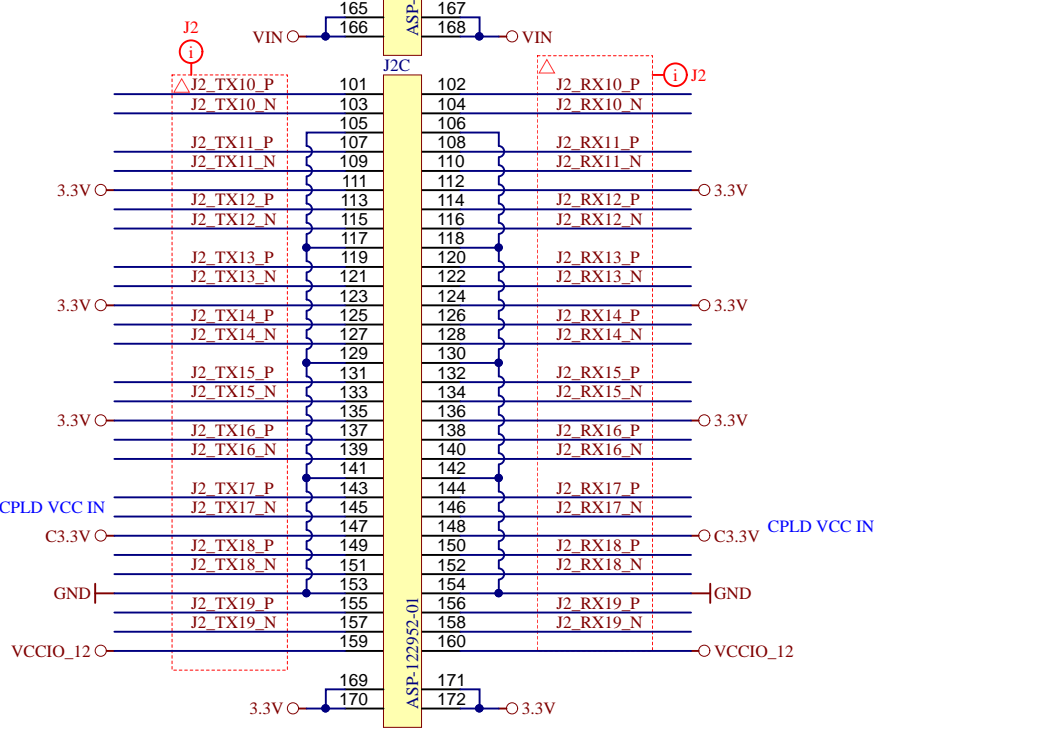
C

D

D



CPLD C3.3V



Title: TE0784 - HSMC_Connector_J2		
A4	Number: TE0784 100-2I	Rev. 01
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Filename: HSMC_CONN_J2.SchDoc		

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A

A

U_PS-DDR
PS-DDR.SchDoc



U_B9
B9.SchDoc



U_MIO-BANKS
MIO-BANKS.SchDoc



U_B10
B10.SchDoc



U_HP-BANKS
HP-BANKS.SchDoc



U_B11
B11.SchDoc



B

B

U_FPGA-MGT
FPGA-MGT.SchDoc



U_B12
B12.SchDoc



U_FPGA-CFG
FPGA-CFG.SchDoc



U_B13
B13.SchDoc



C

C

U_FPGA-PWR
FPGA-PWR.SchDoc



D

D



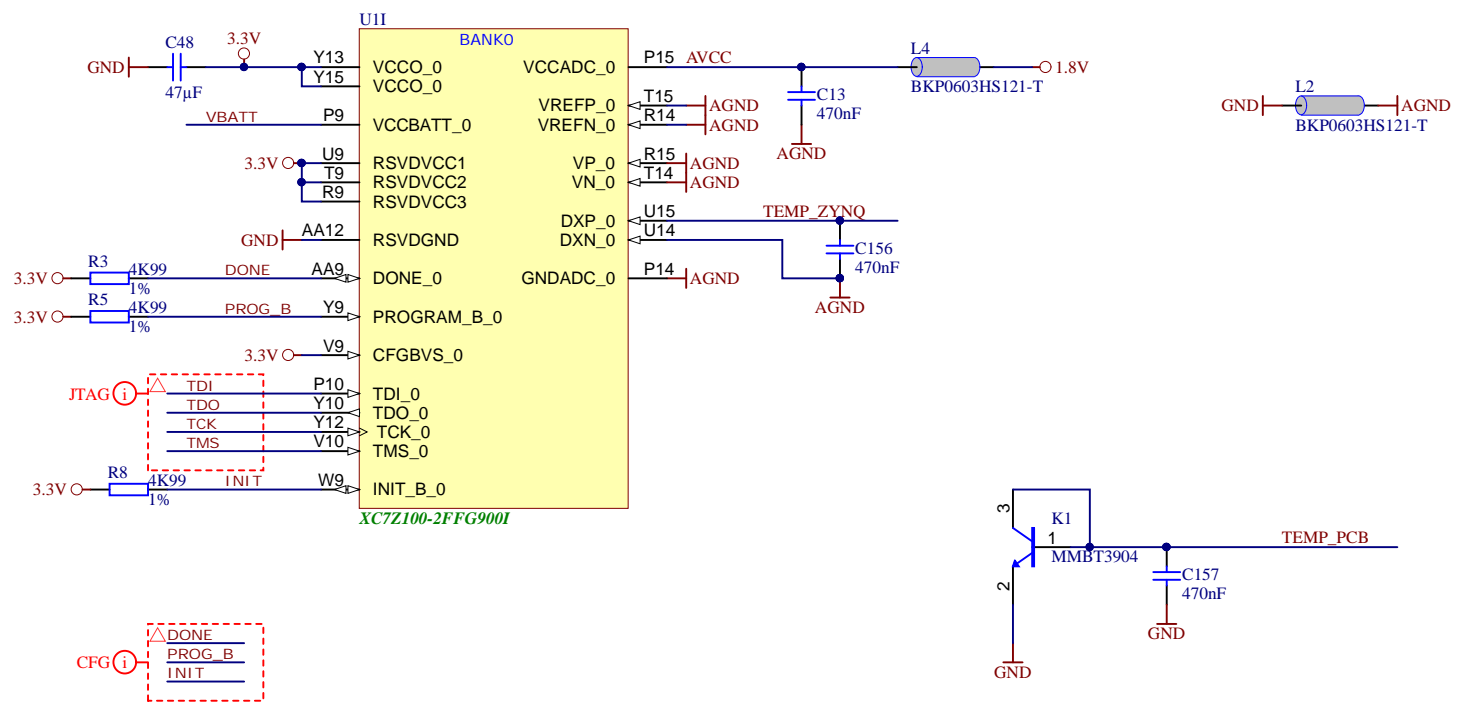
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A4	Number: TE0784 100-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 6 of 30
Filename: SOC.SchDoc		


1

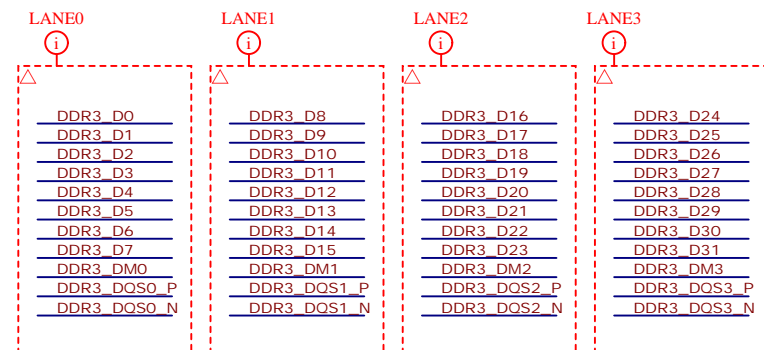
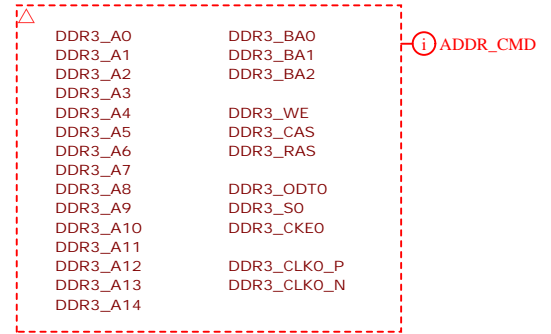
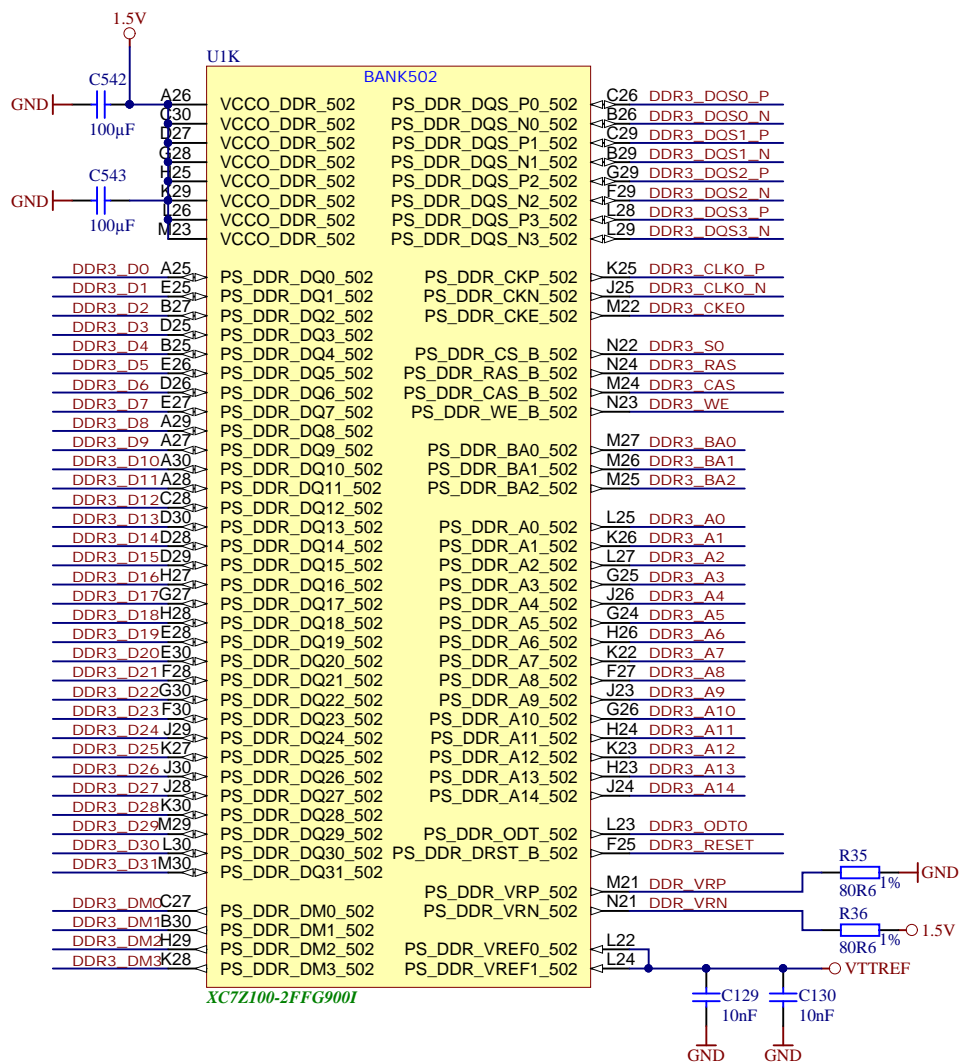
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		A4	Nummer: TE0784 100-2I
Datum: 25.06.2018		Zeichner: Trenz Electronic GmbH	
Filename: FPGA-CFG.SchDoc		Blatt 7 von 30	



Title: TE0784 - FPGA DDR Banks		
A4	Number: TE0784 100-21	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 8 of 30
Filename: PS-DDR.SchDoc		

A

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D

U1M

ClassName: MGT_TX

D100

BANK109

BANK110

BANK111

BANK112

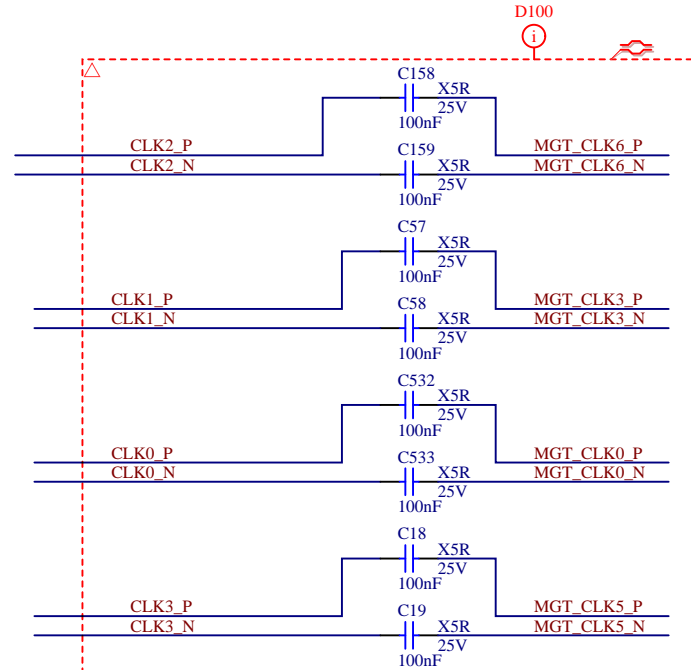
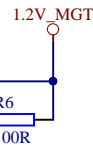
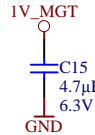
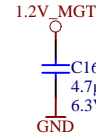
XC7Z100-2FFG900I

ClassName: MGT_RX

MGT_CLK

D100

D100



Title: TE0784 - FPGA MGT		
A4	Number: TE0784 100-2I	Rev. 01
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Filename: FPGA-MGT.SchDoc		

U1J

BANK500 & 501

VCCO_MIO0_500 PS_MIO0_500
 VCCO_MIO0_500 PS_MIO1_500
 VCCO_MIO0_500 PS_MIO2_500
 PS_CLK_500 PS_MIO3_500
 PS_MIO4_500 PS_MIO4_500
 PS_MIO5_500 PS_MIO5_500
 PS_MIO6_500 PS_MIO6_500
 PS_MIO7_500 PS_MIO7_500
 PS_MIO8_500 PS_MIO8_500
 PS_MIO9_500 PS_MIO9_500
 PS_MIO10_500 PS_MIO10_500
 PS_MIO11_500 PS_MIO11_500
 PS_MIO12_500 PS_MIO12_500
 PS_MIO13_500 PS_MIO13_500
 PS_MIO14_500 PS_MIO14_500
 PS_MIO15_500 PS_MIO15_500

VCCO_MIO1_501 PS_MIO16_501
 VCCO_MIO1_501 PS_MIO17_501
 VCCO_MIO1_501 PS_MIO18_501
 VCCO_MIO1_501 PS_MIO19_501
 PS_SRST_B_501 PS_MIO20_501
 PS_MIO21_501 PS_MIO21_501
 PS_MIO22_501 PS_MIO22_501
 PS_MIO_VREF_501 PS_MIO23_501
 PS_MIO24_501 PS_MIO24_501
 PS_MIO25_501 PS_MIO25_501
 PS_MIO26_501 PS_MIO26_501
 PS_MIO27_501 PS_MIO27_501
 PS_MIO28_501 PS_MIO28_501
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XC7Z100-2FFG9001

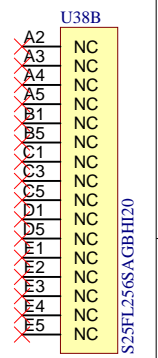
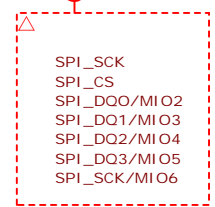
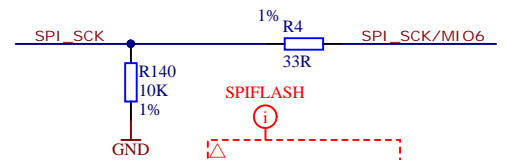
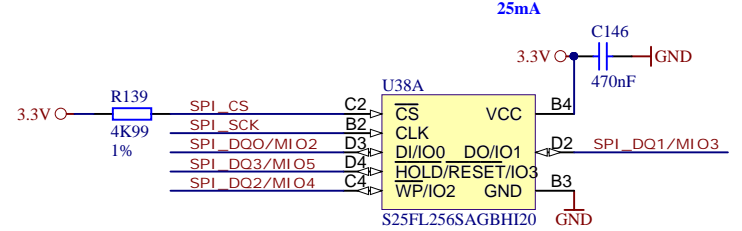
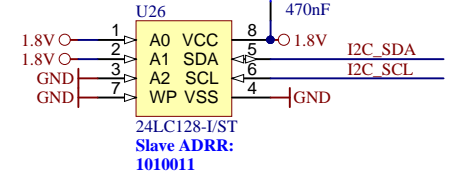
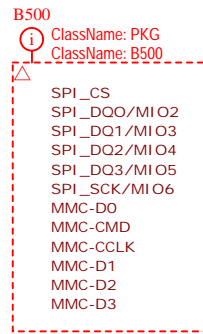
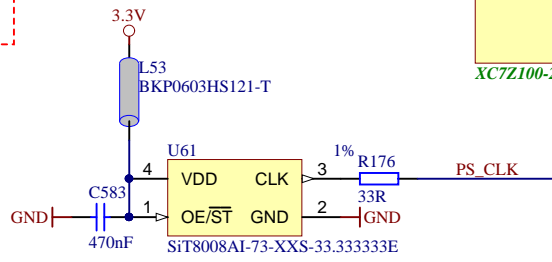
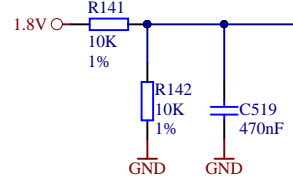
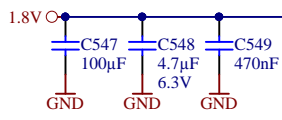
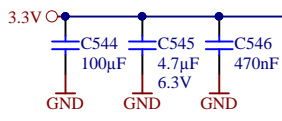
F24 MIO0
 D23 SPI_CS
 F23 SPI_DQ0/MIO2
 C23 SPI_DQ1/MIO3 R133 10K 1% GND
 E23 SPI_DQ2/MIO4 R134 10K 1% GND
 C24 SPI_DQ3/MIO5 R135 10K 1% GND
 D24 SPI_SCK/MIO6 R44 10K 1% GND
 B24 ETH1_RESET33
 C21 MIO8 R137 10K 1% 0.3.3V
 A24 MIO9
 E22 MMC-D0
 A23 MMC-CMD
 E21 MMC-CCLK
 F22 MMC-D1
 B22 MMC-D2
 C22 MMC-D3

L19 ETH1_TXCK
 K21 ETH1_TXD0
 K20 ETH1_TXD1
 J20 ETH1_TXD2
 M20 ETH1_TXD3
 J19 ETH1_TXCTL
 L20 ETH1_RXCK
 J21 ETH1_RXD0
 M19 ETH1_RXD1
 G19 ETH1_RXD2
 M17 ETH1_RXD3
 G20 ETH1_RXCTL

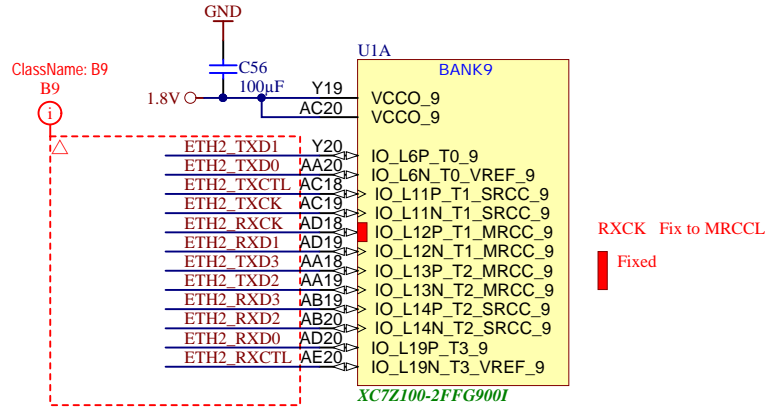
F18 SDIO-CCLK R17 1%
 B20 SDIO-CMD R33R
 D20 SDIO-D0
 E18 SDIO-D1
 E20 SDIO-D2
 H18 SDIO-D3
 F20 PS_MIO46
 A18 PS_MIO47
 C19 PS_MIO48
 D18 PS_MIO49
 A19 PS_MIO50
 F19 PS_MIO51
 D19 ETH1_MDC
 C18 ETH1_MDIO


B501
 ClassName: B501
 ClassName: PKG

SPI and JTAG modes supported
 Cascade and independent modes supported

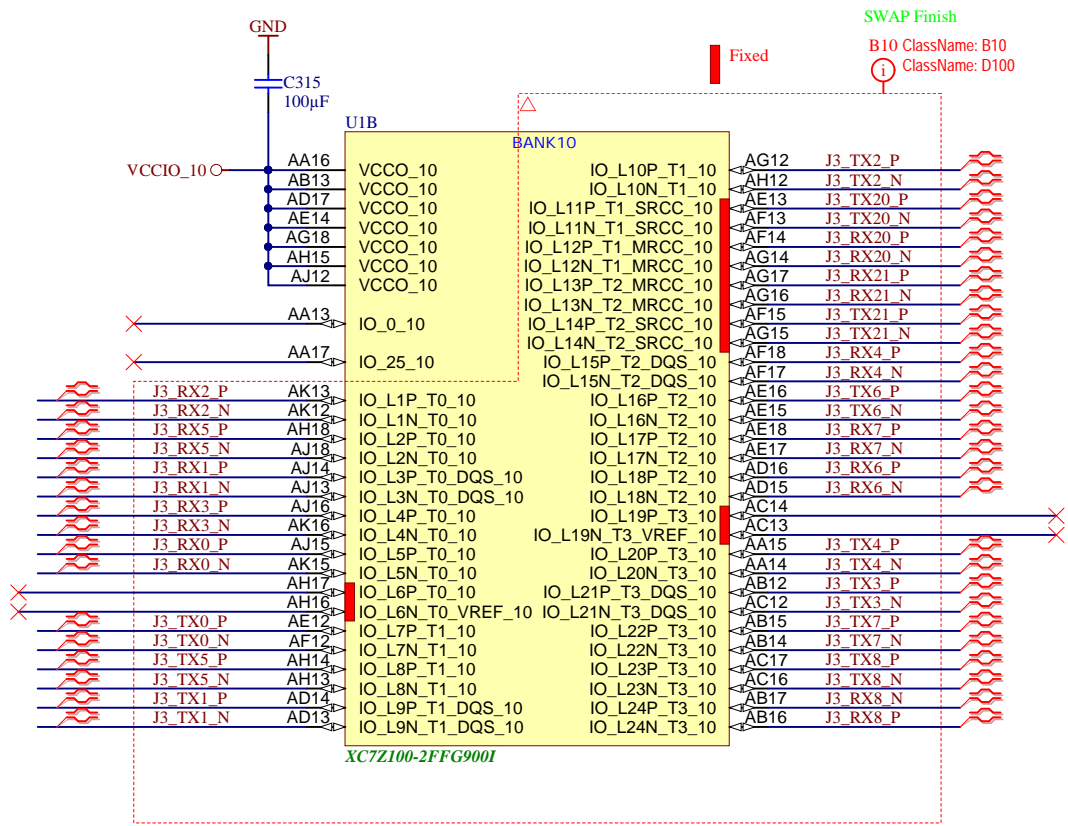


Title: TE0784 - FPGA MIO Banks		
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Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page10 of 30
Filename: MIO-BANKS.SchDoc		

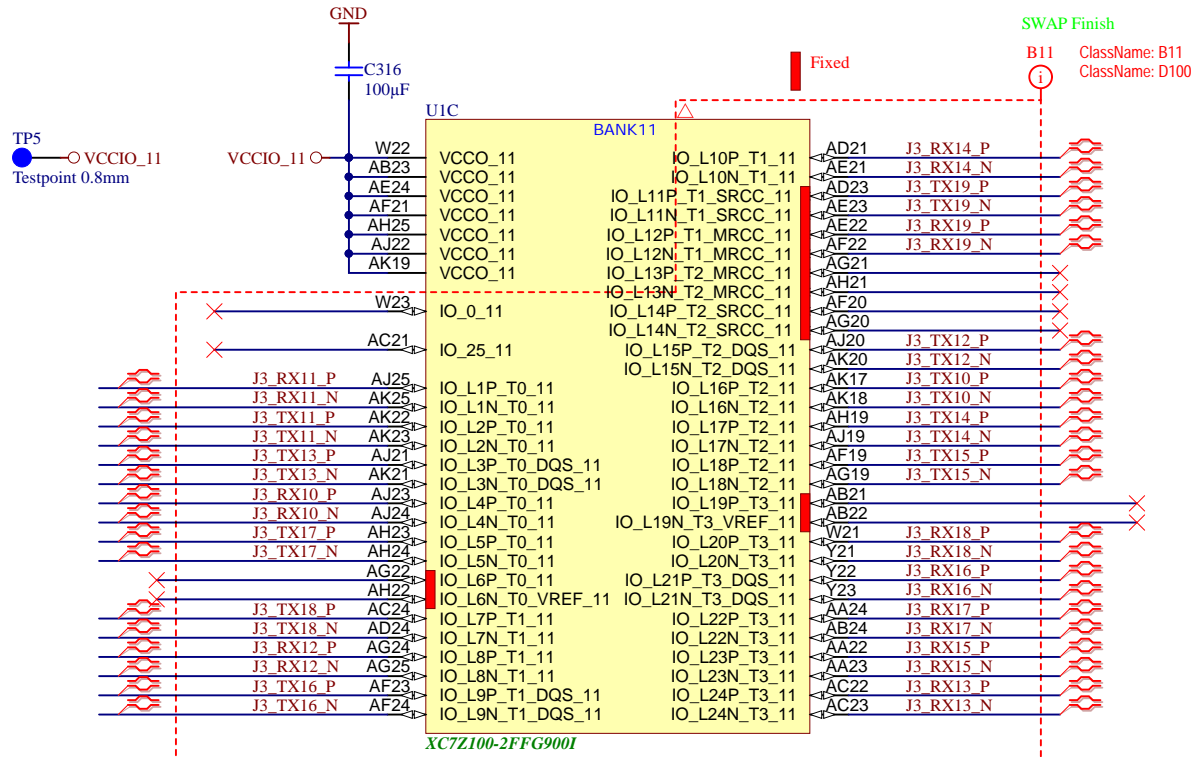


		Title: TE0784 - FPGA B9	
		A4	Number: TE0784 100-2I
Date: 25.06.2018		Copyright: Trenz Electronic GmbH	
Page 11 of 30		Filename: B9.SchDoc	


TP4
 ● VCCIO_10
 ○ Testpoint 0.8mm

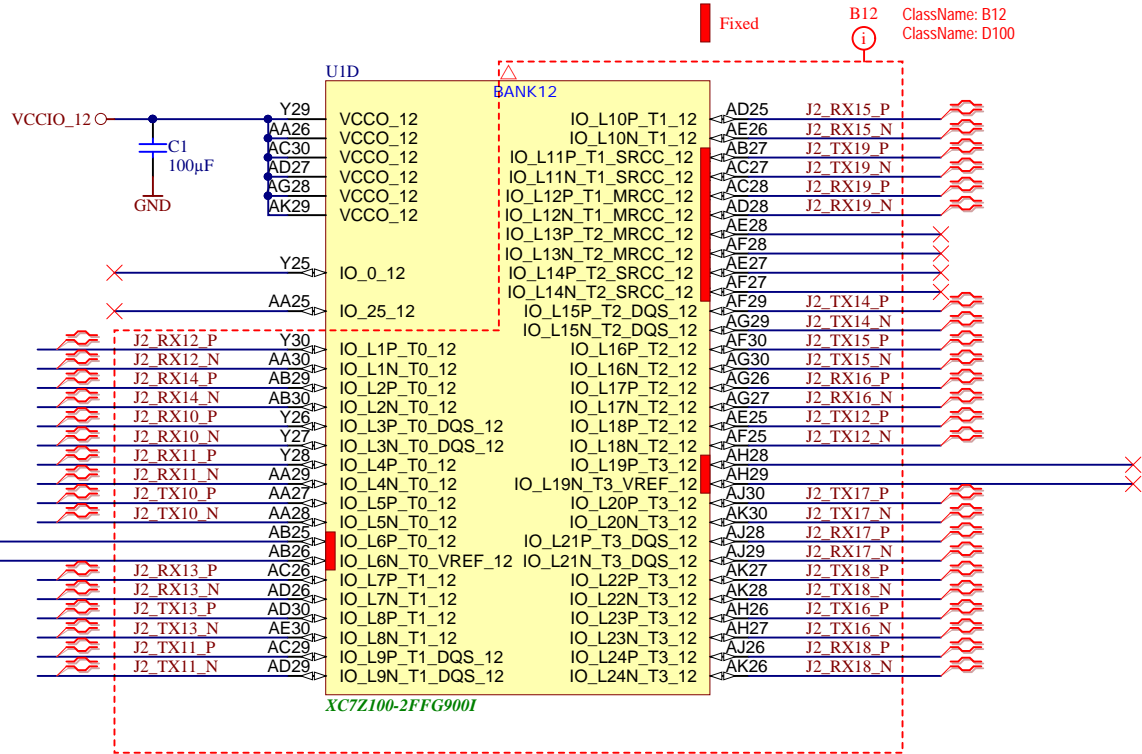


Title: TE0784 - FPGA B10		
A4	Number: TE0784 100-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 12 of 30
Filename: B10.SchDoc		




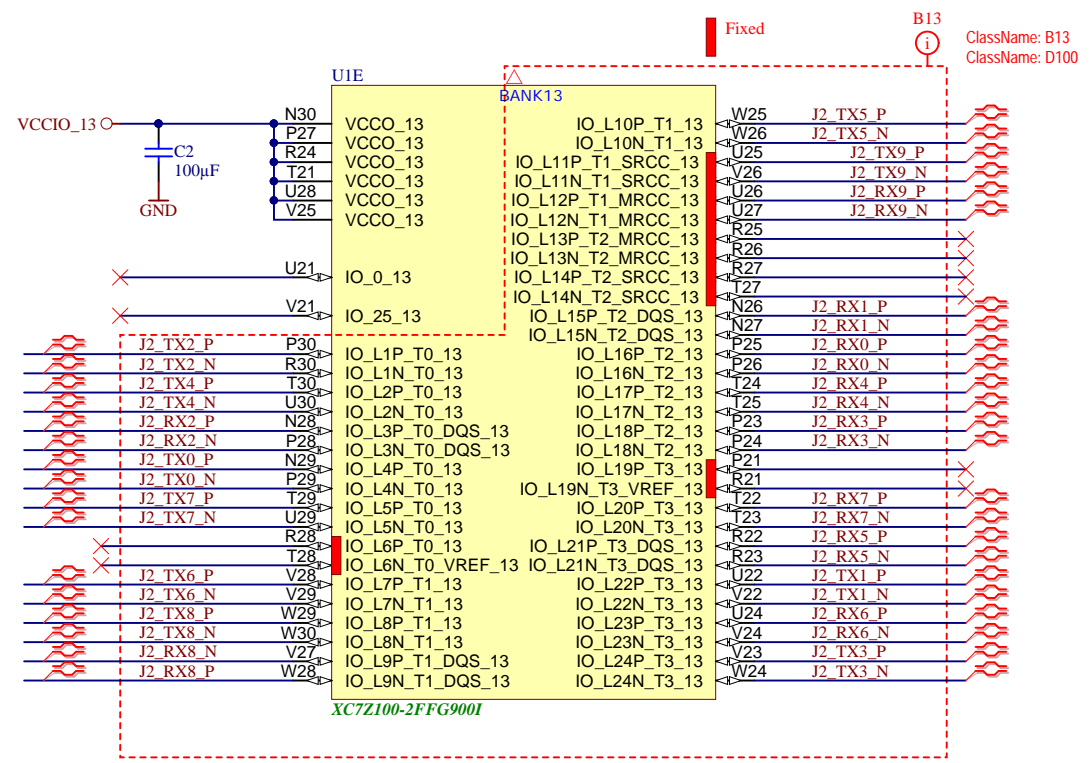
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	A4	Number: TE0784 100-2I	Rev. 01
	Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page13 of 30
	Filename: B11.SchDoc		

TP1
 VCCIO_12
 Testpoint 0.8mm



Title: TE0784 - FPGA B12		
A4	Number: TE0784 100-2I	Rev. 01
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Filename: B12.SchDoc		

TP2
 VCCIO_13
 Testpoint 0.8mm



Title: TE0784 - FPGA B13		
A4	Number: TE0784 100-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 15 of 30
Filename: B13.SchDoc		

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U_B33
B33.SchDoc



U_B34
B34.SchDoc



U_B35
B35.SchDoc



A

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C

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Title: TE0784 - FPGA HP Banks		
A4	Number: TE0784 100-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 16 of 30
Filename: HP-BANKS.SchDoc		

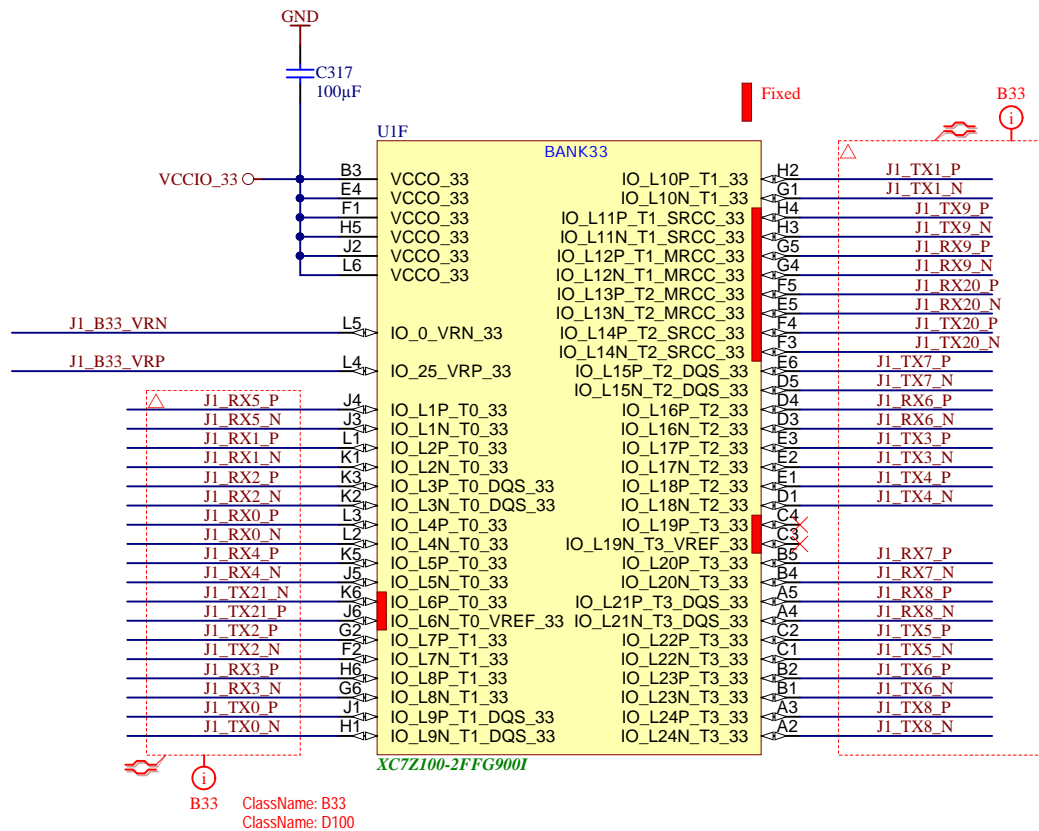
1

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TP6
 VCCIO_33
 Testpoint 0.8mm

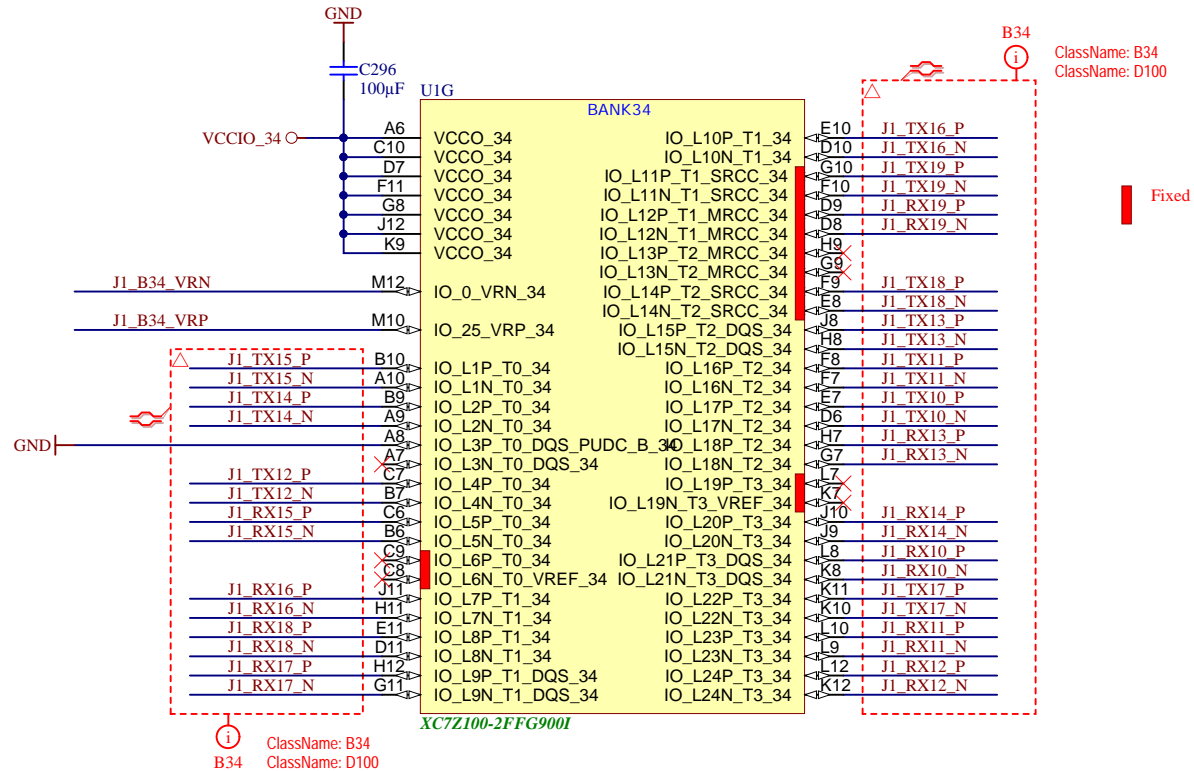


B33
 ClassName: B33
 ClassName: D100

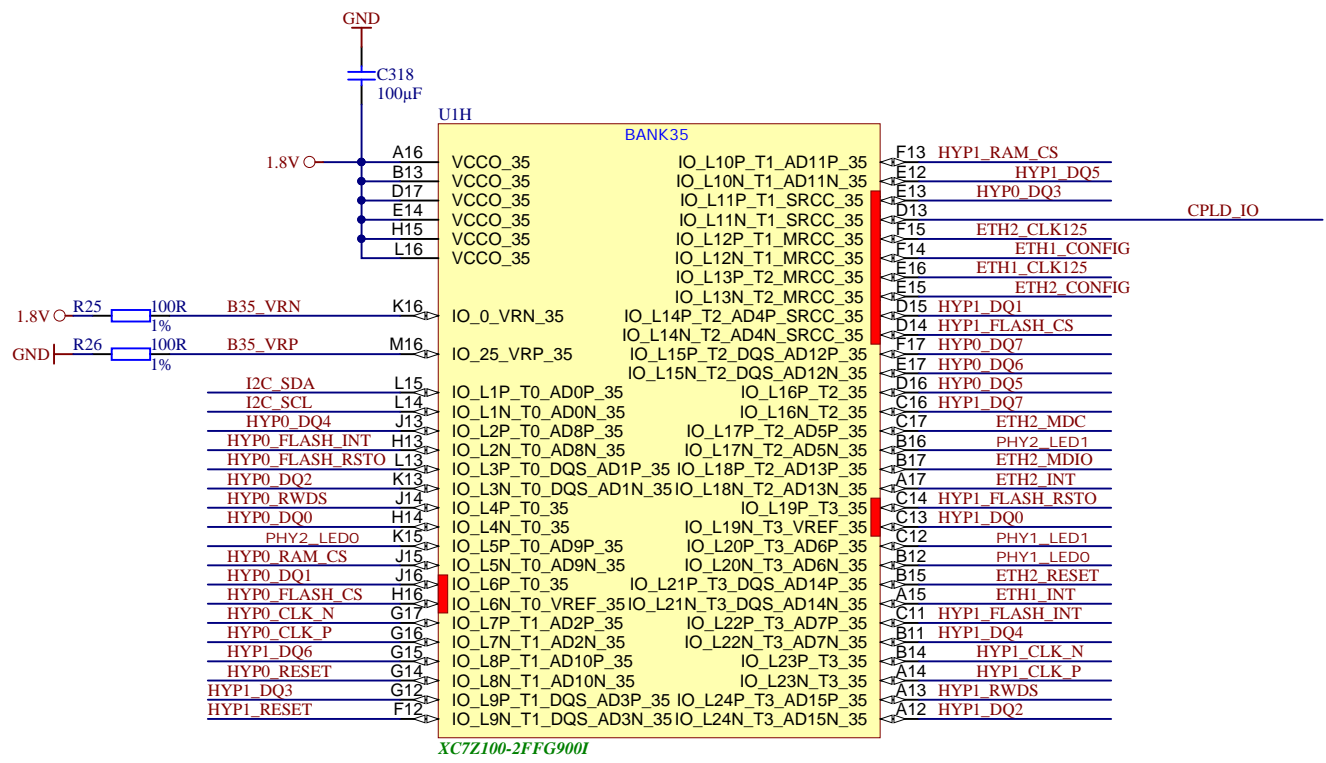


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A4	Number: TE0784 100-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 17 of 30
Filename: B33.SchDoc		

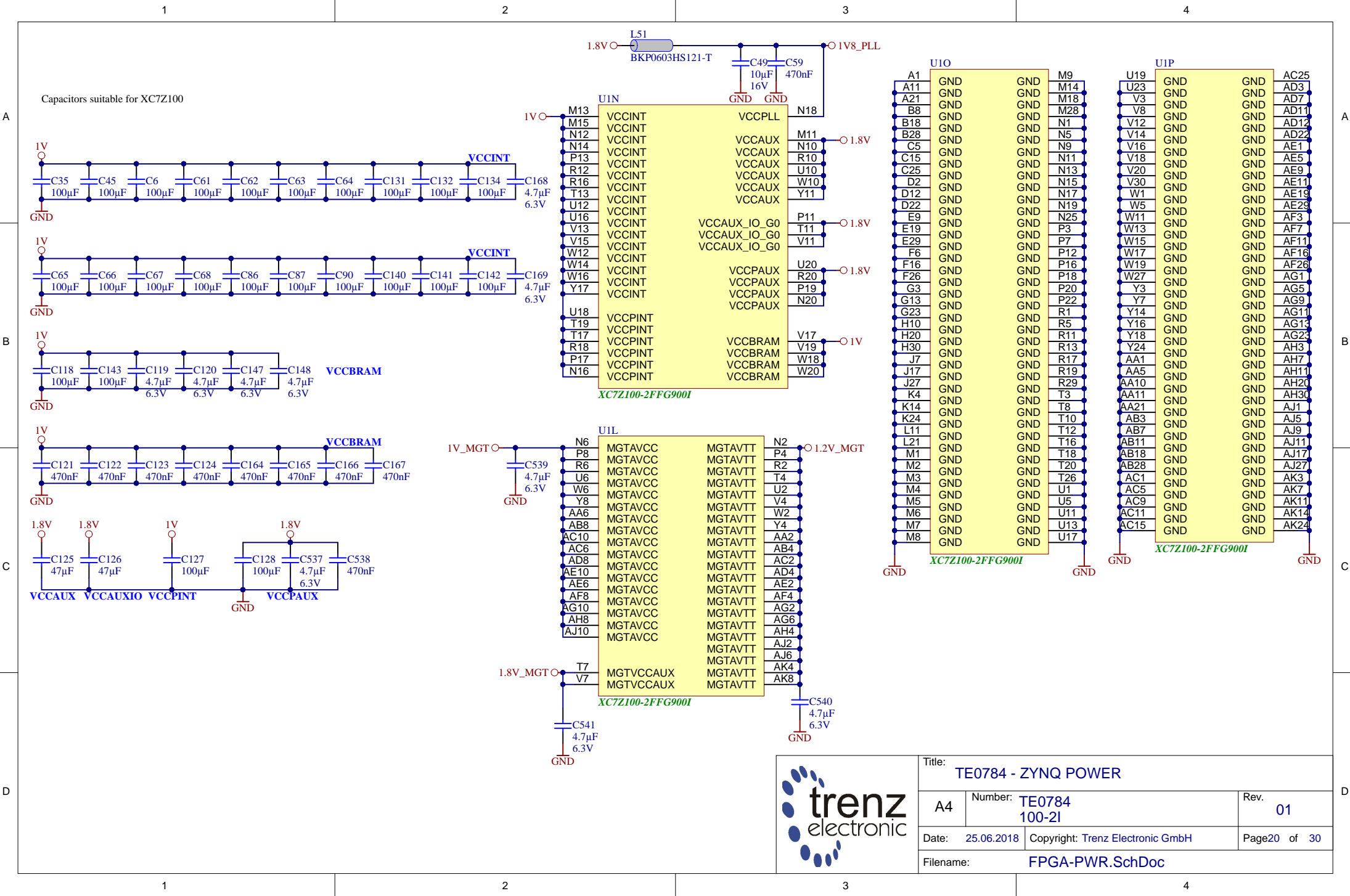
TP3
 VCCIO_34
 Testpoint 0.8mm



Title: TE0784 - FPGA B34		
A4	Number: TE0784 100-2I	Rev. 01
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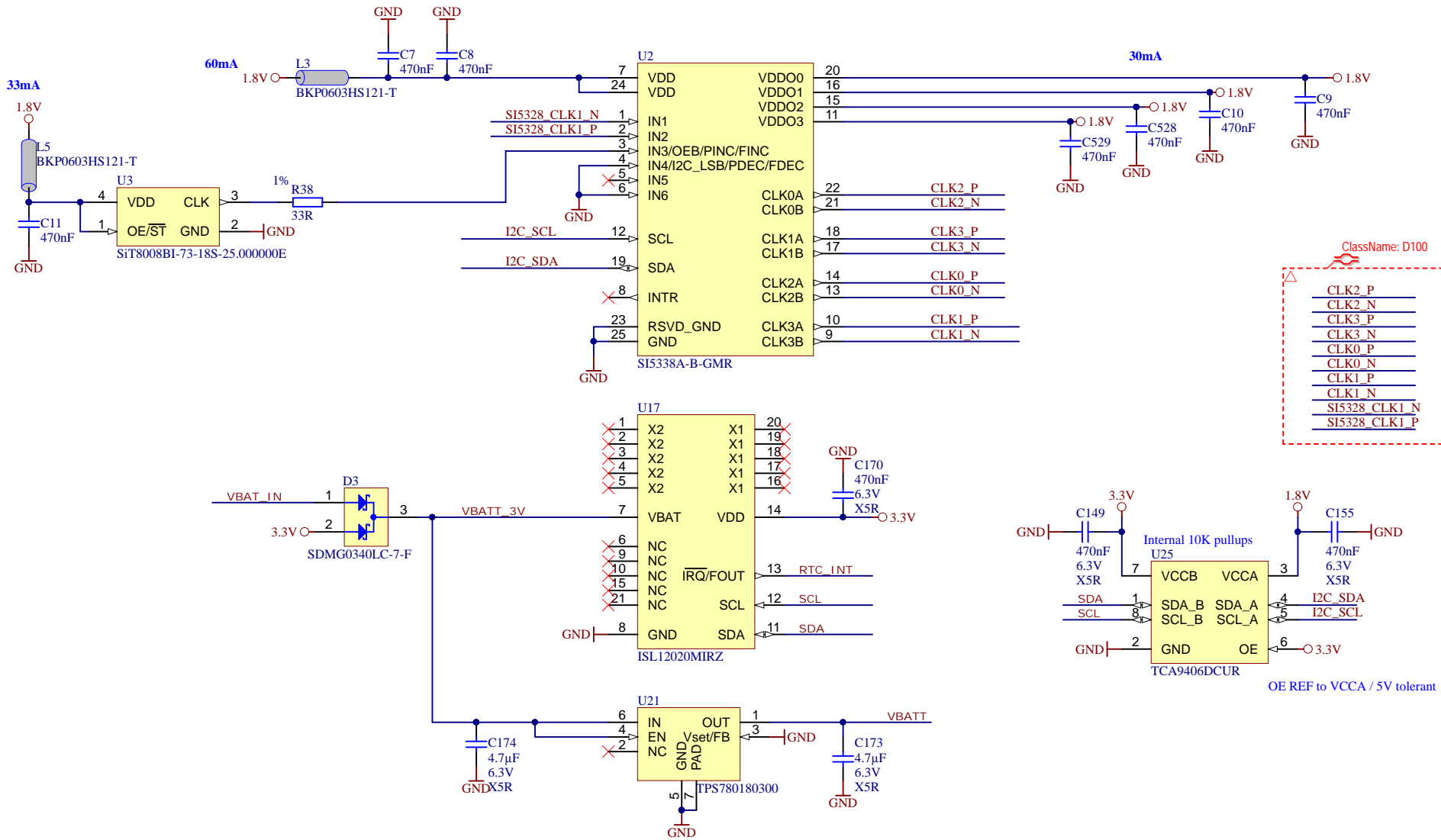
Title: TE0784 - FPGA B35		
A4	Number: TE0784 100-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 19 of 30
Filename: B35.SchDoc		



trenz electronic

Title: **TE0784 - ZYNQ POWER**

A4	Number: TE0784 100-21	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 20 of 30
Filename: FPGA-PWR.SchDoc		



- ClassName: D100
- CLK2_P
 - CLK2_N
 - CLK3_P
 - CLK3_N
 - CLK0_P
 - CLK0_N
 - CLK1_P
 - CLK1_N
 - SI5328_CLK1_N
 - SI5328_CLK1_P



Title: TE0784 - Clock		
A4	Number: TE0784 100-21	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page21 of 30
Filename: Clock.SchDoc		

A

B

C

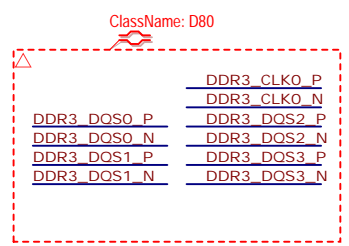
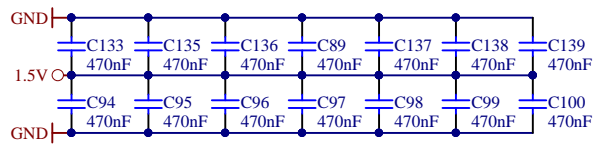
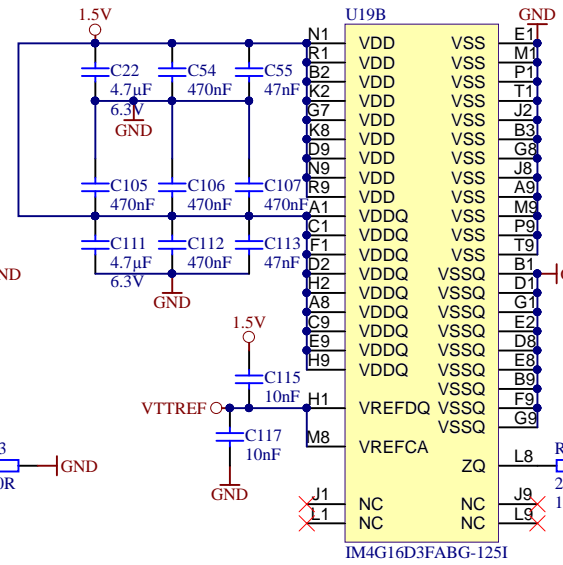
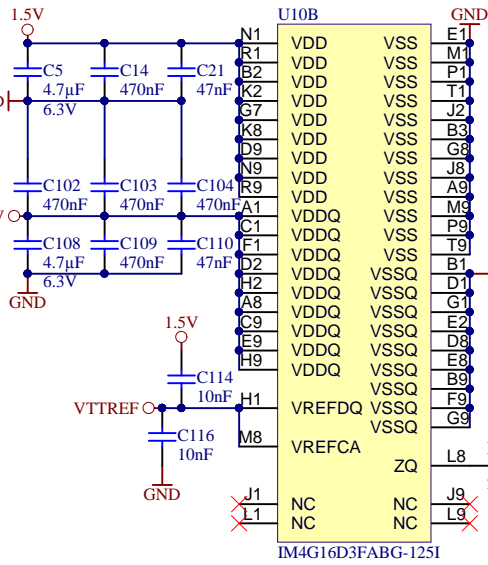
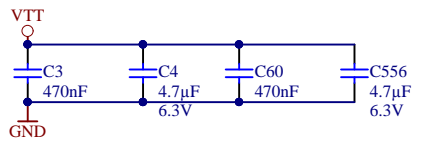
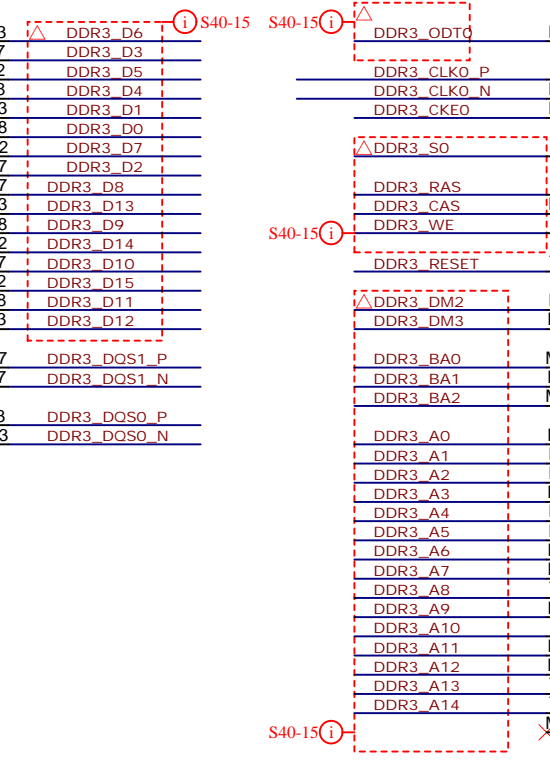
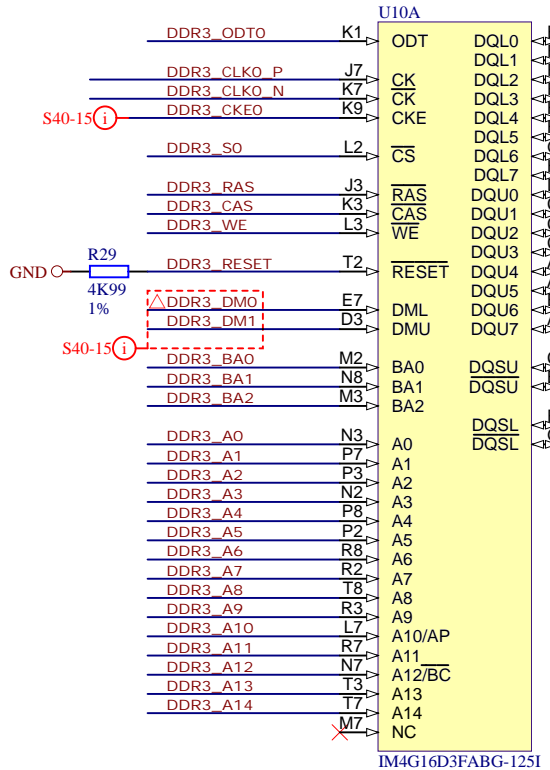
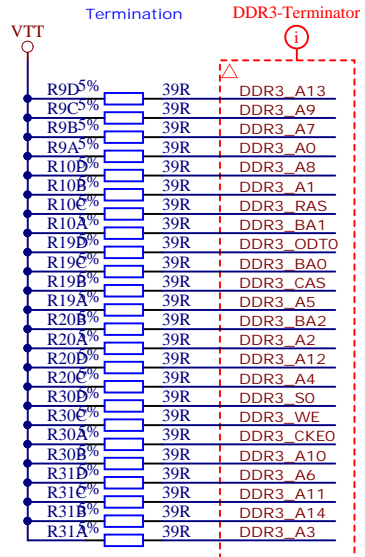
D

A

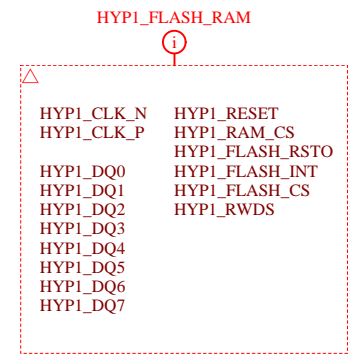
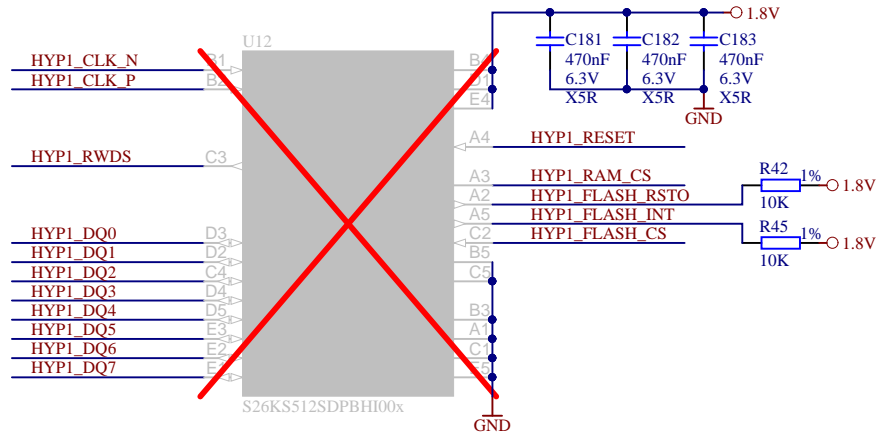
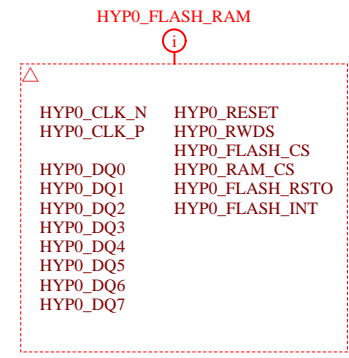
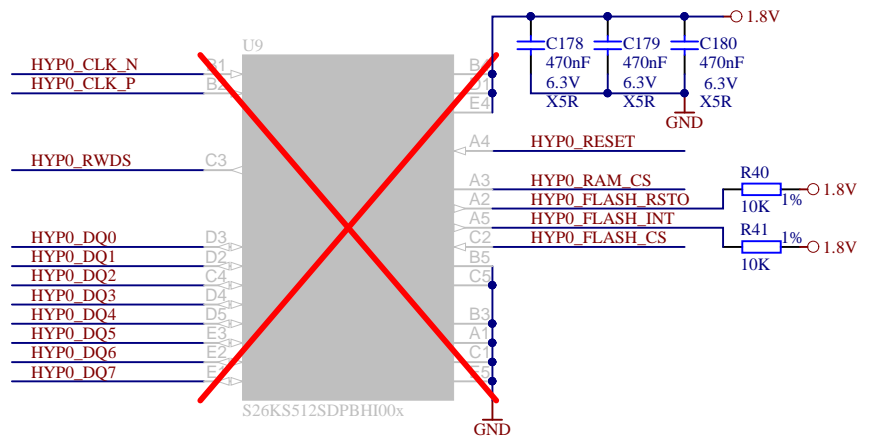
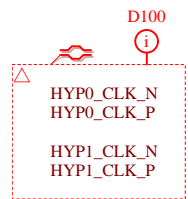
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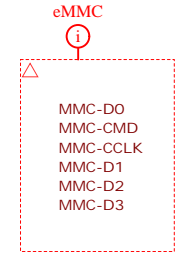
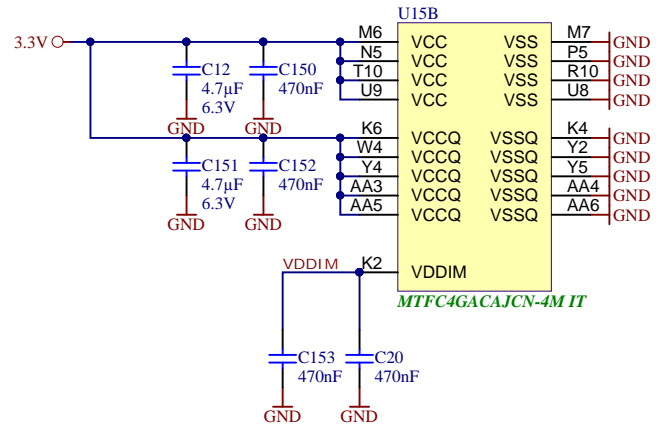
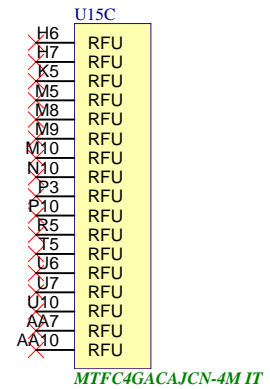
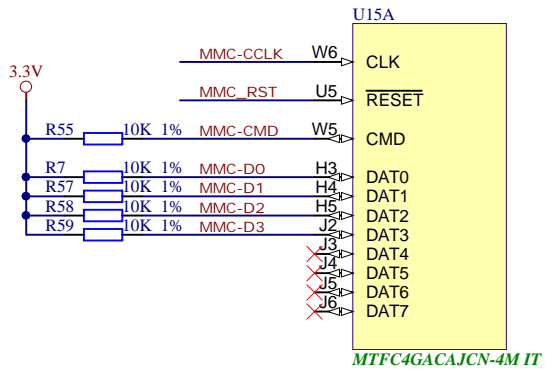
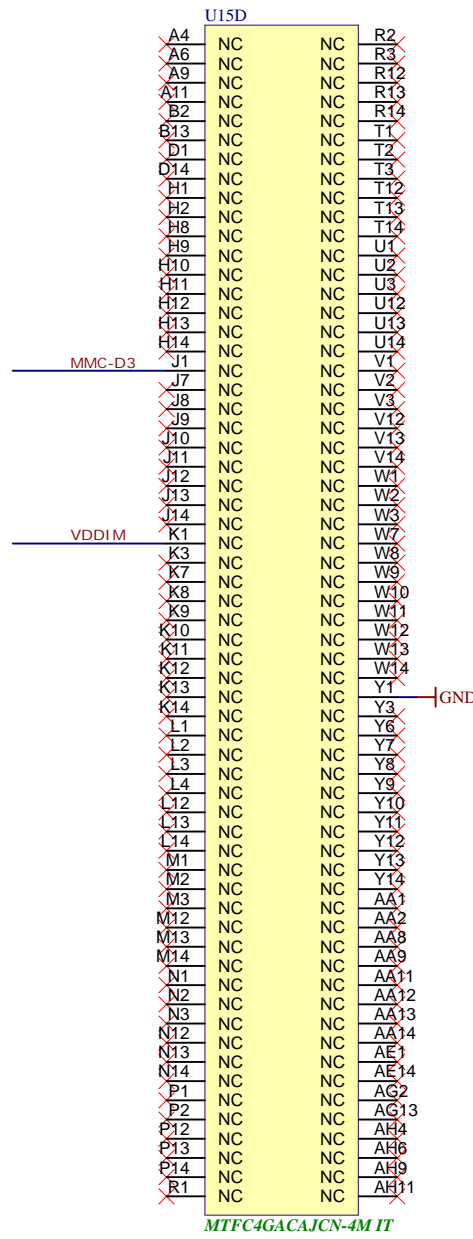
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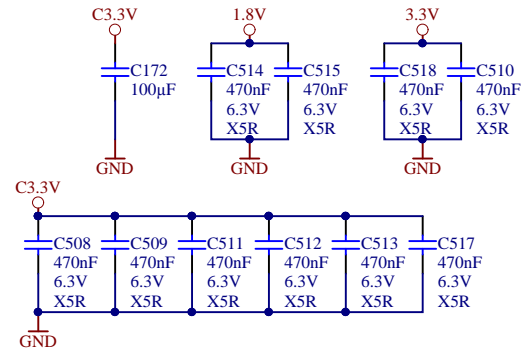
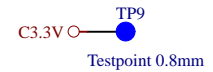
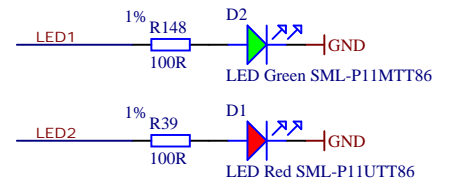
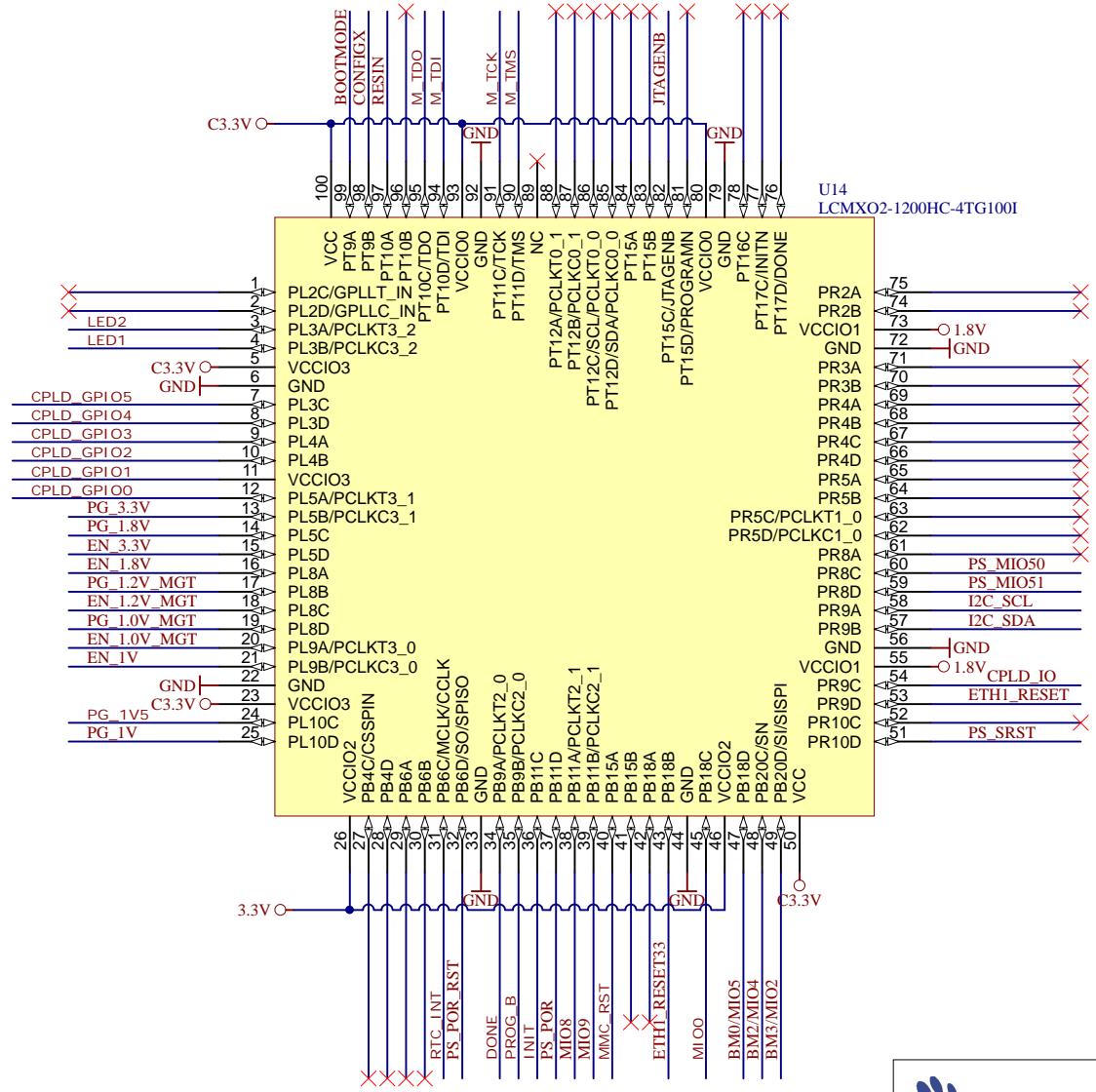
Title: TE0784 - DDR3 RAM		
A4	Number: TE0784 100-21	Rev. 01
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Filename: DDR3-RAM.SchDoc		



Title: TE0784 - HyperFlash_RAM		
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Title: TE0784 - CPLD		
A4	Number: TE0784 100-21	Rev. 01
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Filename: CPLD.SchDoc		

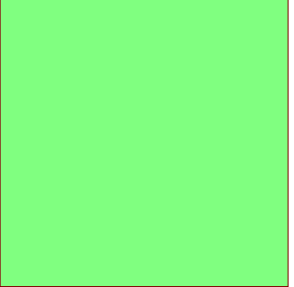
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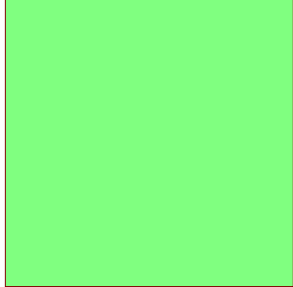
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4

U_ETH1
ETH1.SchDoc



U_ETH2
ETH2.SchDoc



A

A

B

B

C

C

D

D



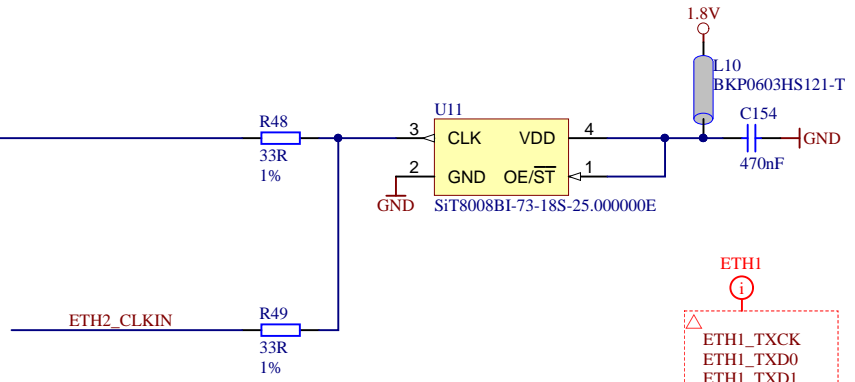
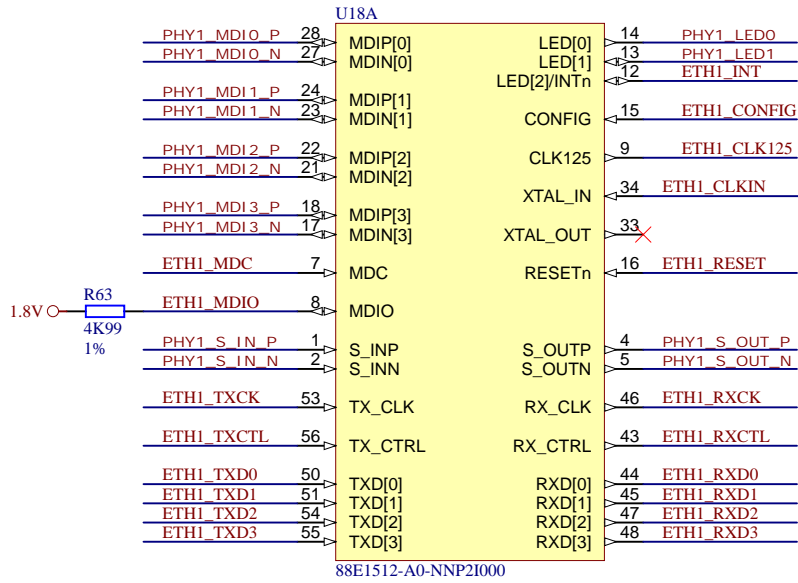
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A4	Number: TE0784 100-2I	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 26 of 30
Filename: Ethernet.SchDoc		

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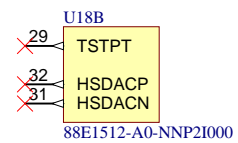
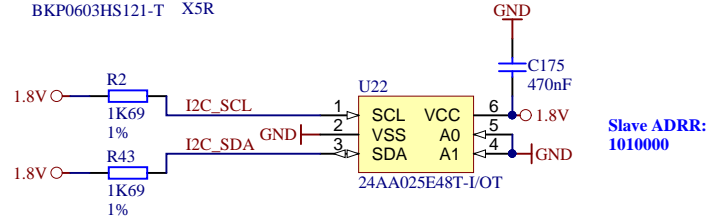
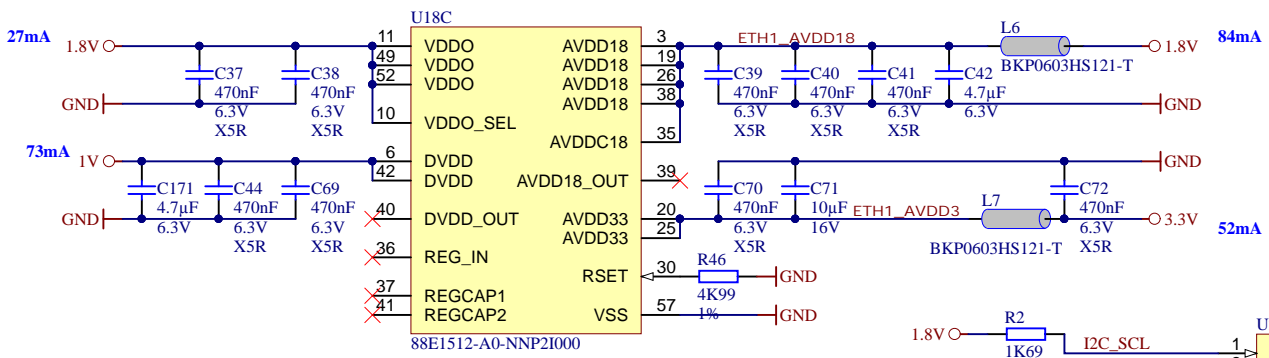
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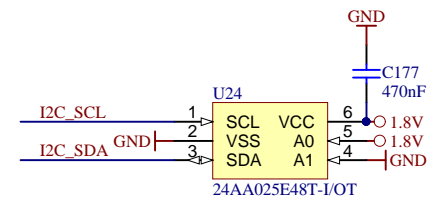
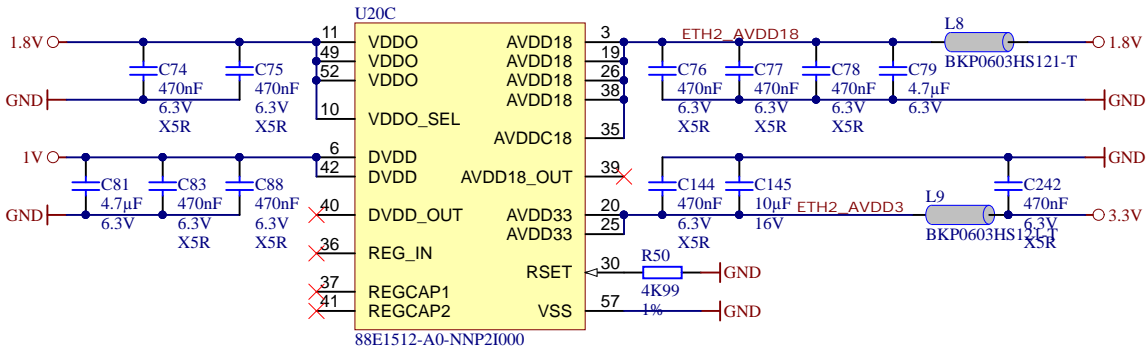
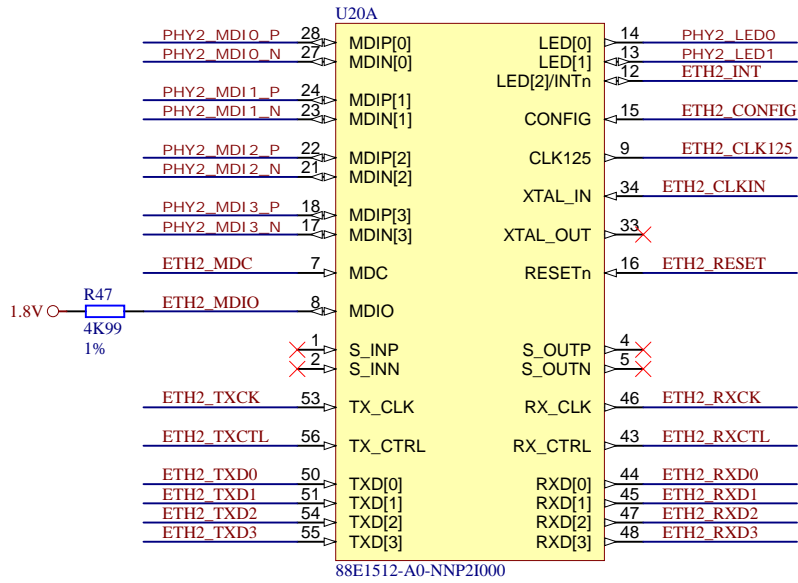
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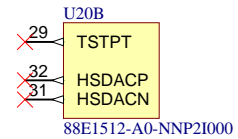
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- ETH1_TXCK
 - ETH1_TXD0
 - ETH1_TXD1
 - ETH1_TXD2
 - ETH1_TXD3
 - ETH1_TXCTL
 - ETH1_RXCK
 - ETH1_RXD0
 - ETH1_RXD1
 - ETH1_RXD2
 - ETH1_RXD3
 - ETH1_RXCTL
 - ETH1_MDC
 - ETH1_MDIO
- PHY1_LED0
PHY1_LED1
ETH1_INT
ETH1_CONFIG
ETH1_CLK125
ETH1_RESET



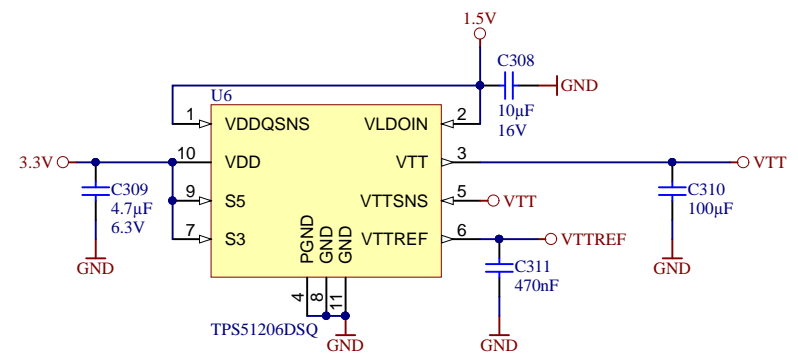
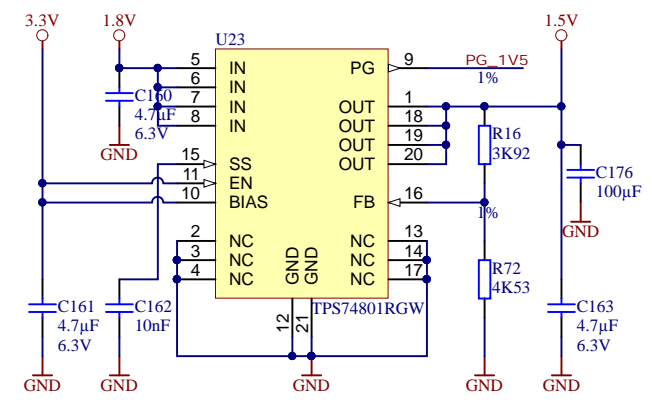
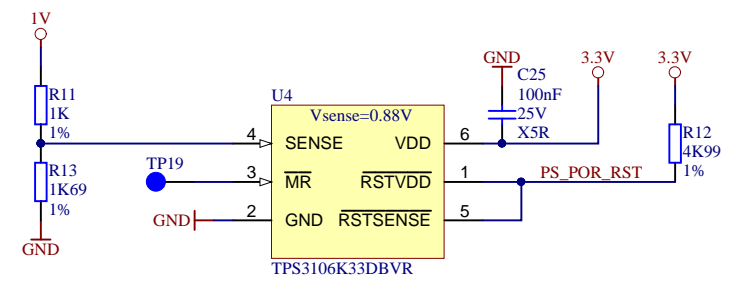
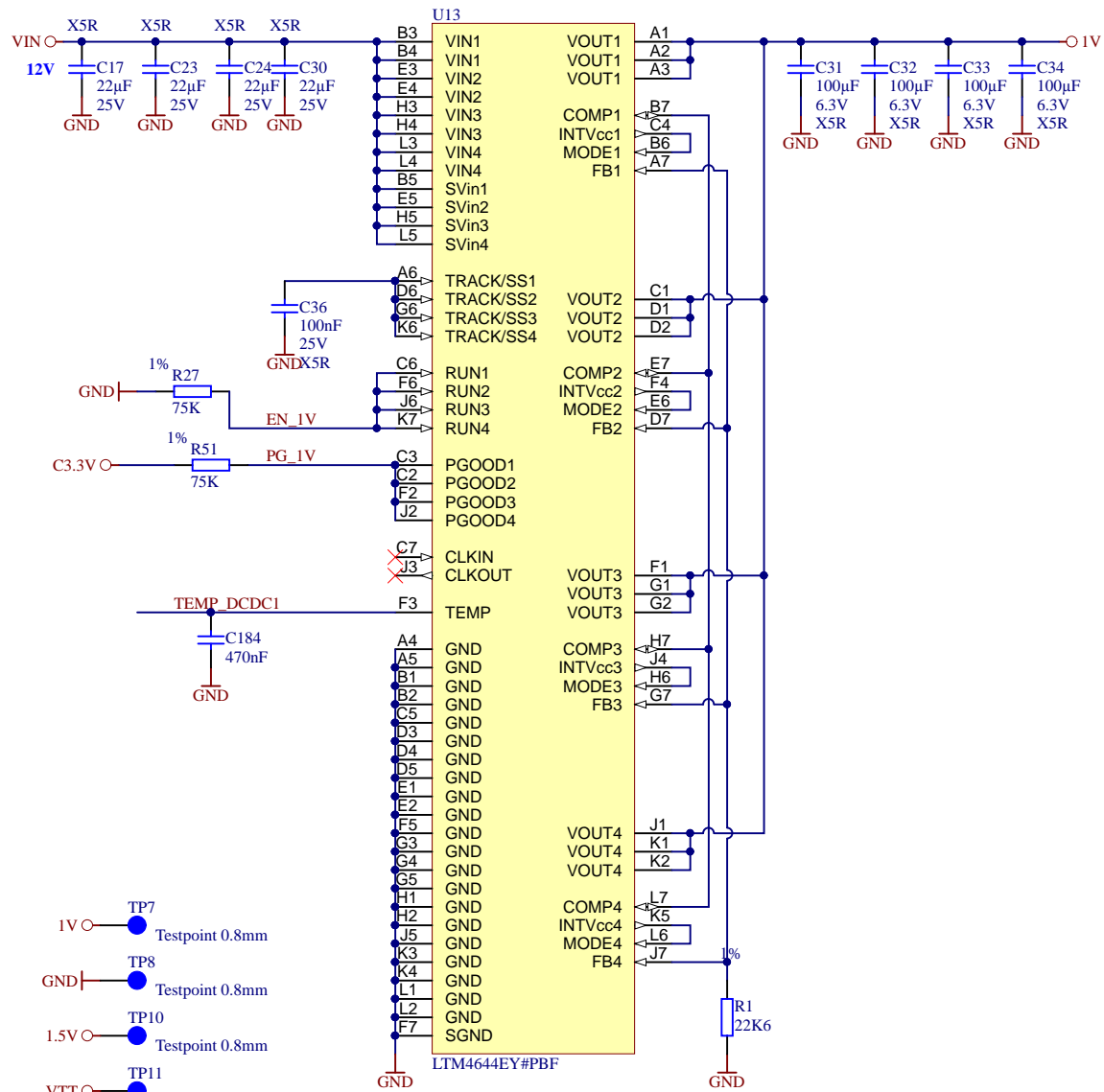
Title: TE0784 - ETH_PHY1		
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Filename: ETH1.SchDoc		




Slave ADDR:
1010001

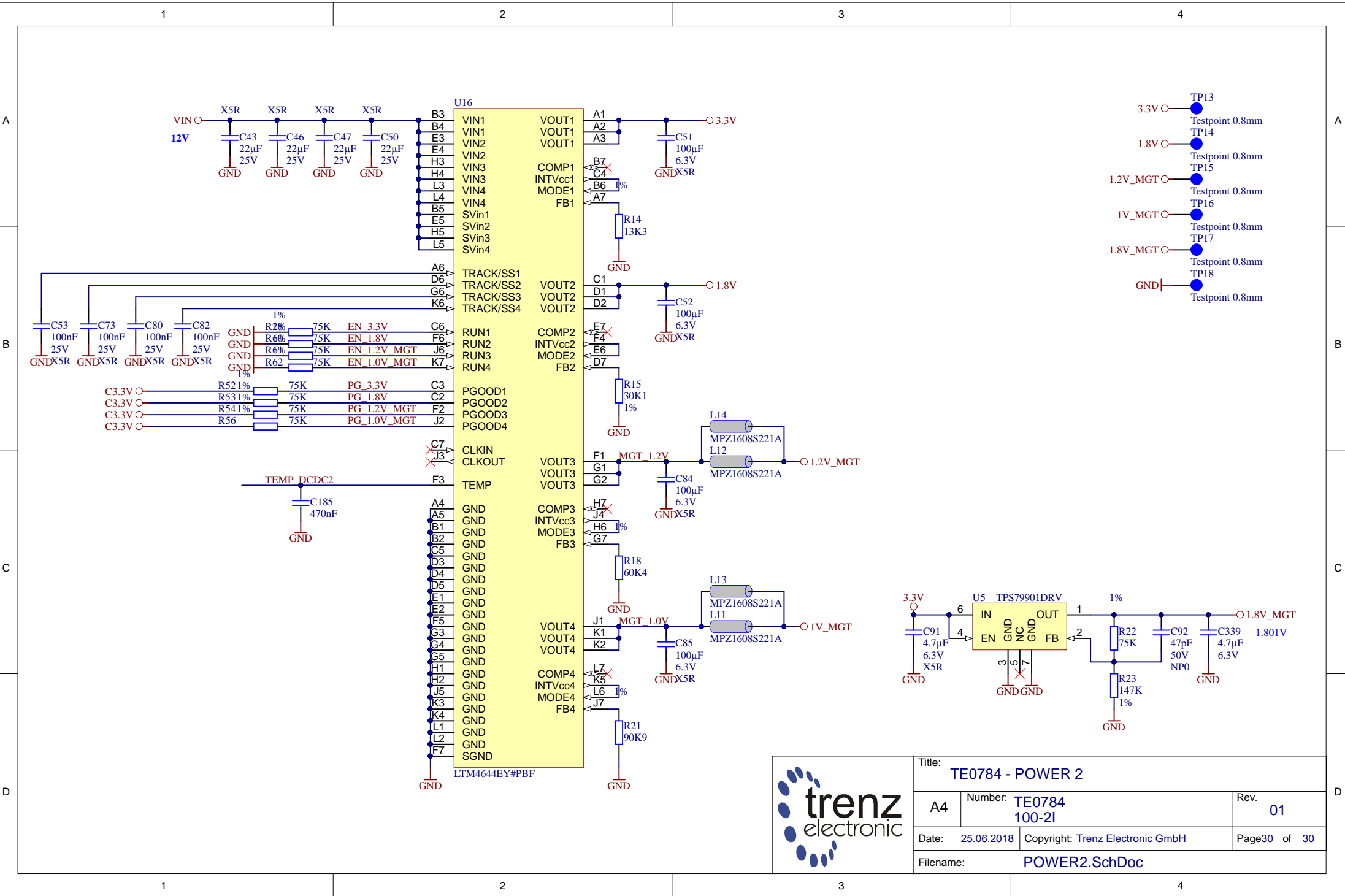


	Title: TE0784 - ETH_PHY2		
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	Filename: ETH2.SchDoc		



- 1V ○ TP7 Testpoint 0.8mm
- GND TP8 Testpoint 0.8mm
- 1.5V ○ TP10 Testpoint 0.8mm
- VTT ○ TP11 Testpoint 0.8mm
- VTTREF ○ TP12 Testpoint 0.8mm

			Title: TE0784 - POWER	
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Title: TE0784 - POWER 2		
A4	Number: TE0784 100-21	Rev. 01
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Filename: POWER2.SchDoc		