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U_DDR3-RAM
DDR3-RAM.SchDoc

U_Ethernet
Ethernet.SchDoc

U_SOC
SOC.SchDoc

U_CPLD
CPLD.SchDoc

U_POWER2
POWER2.SchDoc

U_HyperFlash_RAM
HyperFlash_RAM.SchDoc

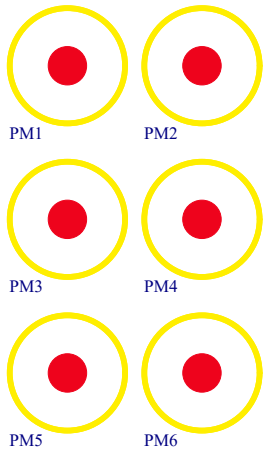
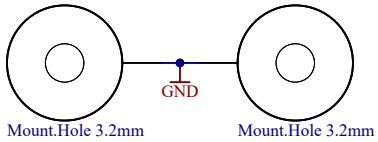
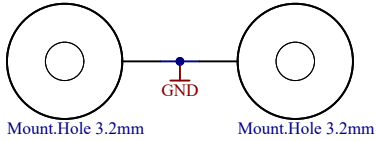
U_Clock
Clock.SchDoc

U_eMMC
eMMC.SchDoc

U_Connectors
Connectors.SchDoc

U_POWER
POWER.SchDoc

LOGO1
TE Logo PRINT Layer
LOGO PRINT



Serial
Serialnumber 6,3 x 6.3mm



Design drawn by:	*
Checked by:	*
Assembly variant:	92I33MA
Created by:	MR
Modified by:	MR
Modified at:	2021-10-25



Title: TE0784 - Overview		
A4	Number: TE0784 92I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page1 of 30
Filename: TE0784.SchDoc		

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A

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U_HSMC_CONN_J1
HSMC_CONN_J1.SchDoc



U_HSMC_CONN_J2
HSMC_CONN_J2.SchDoc



U_HSMC_CONN_J3
HSMC_CONN_J3.SchDoc



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		Title: TE0784 - Connectors	
		A4	Number: TE0784 92133MA
Date: 25.06.2018		Copyright: Trenz Electronic GmbH	
Filename: Connectors.SchDoc		Page2 of 30	

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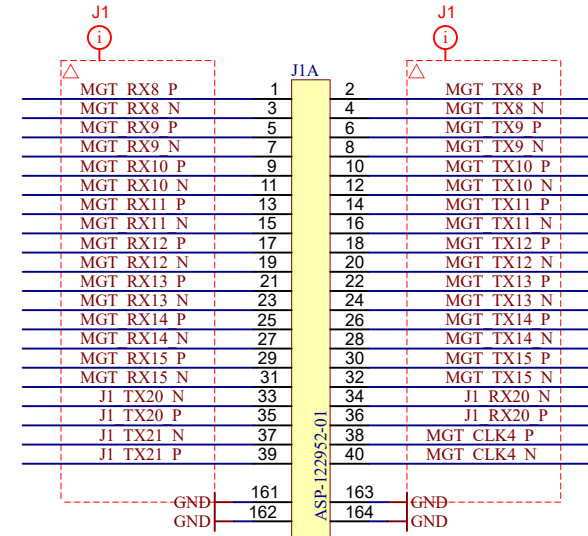
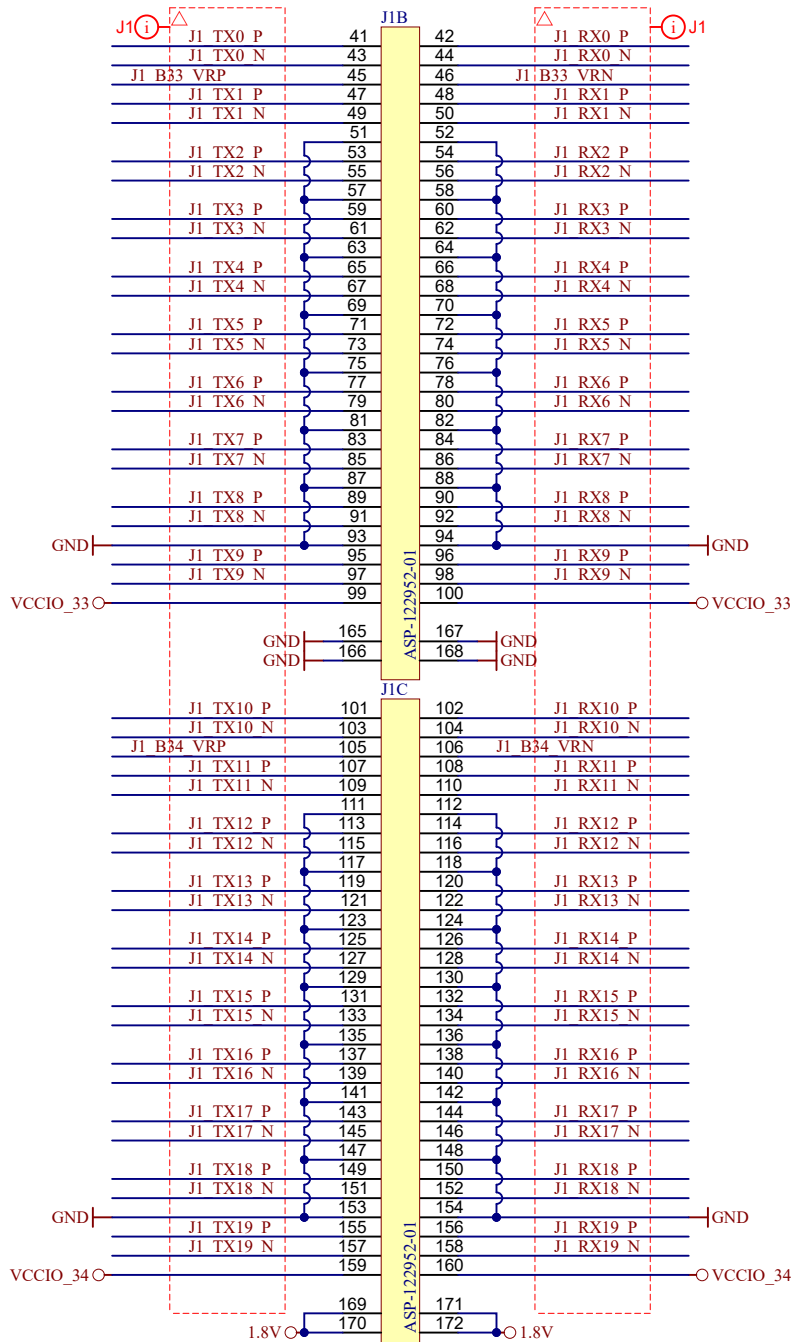
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Title: TE0784 - HSMC_Connector_J1		
A4	Number: TE0784 92I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page3 of 30
Filename: HSMC_CONN_J1.SchDoc		

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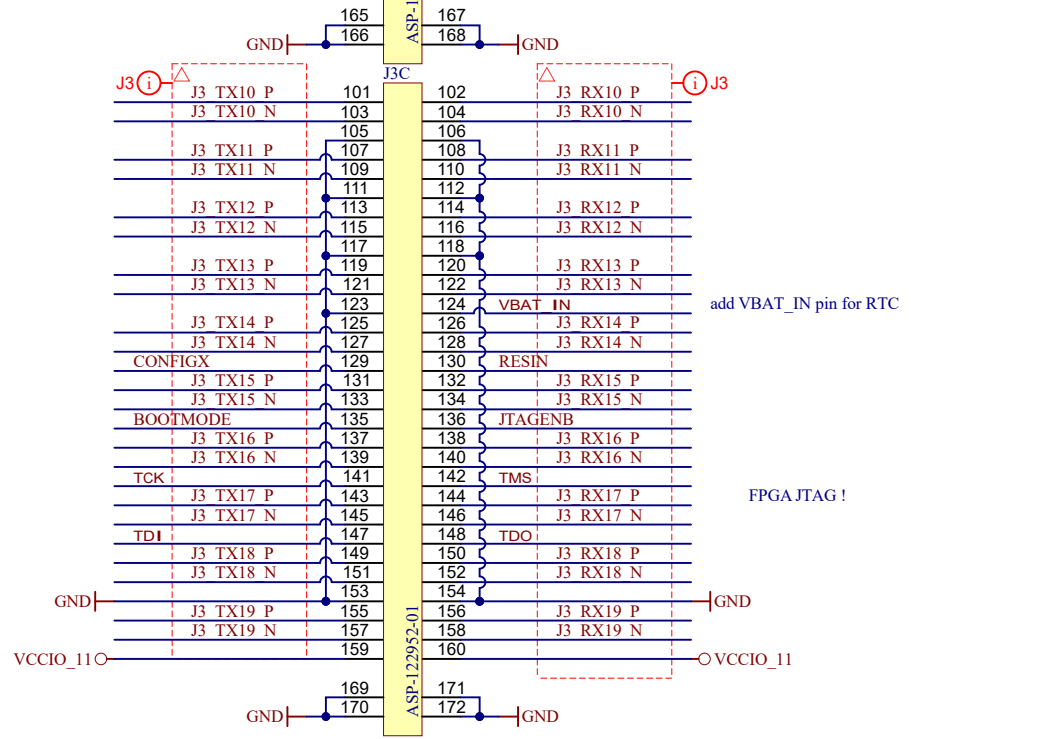
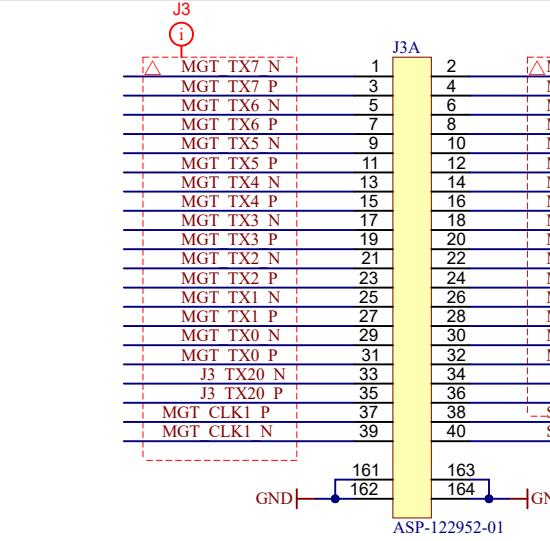
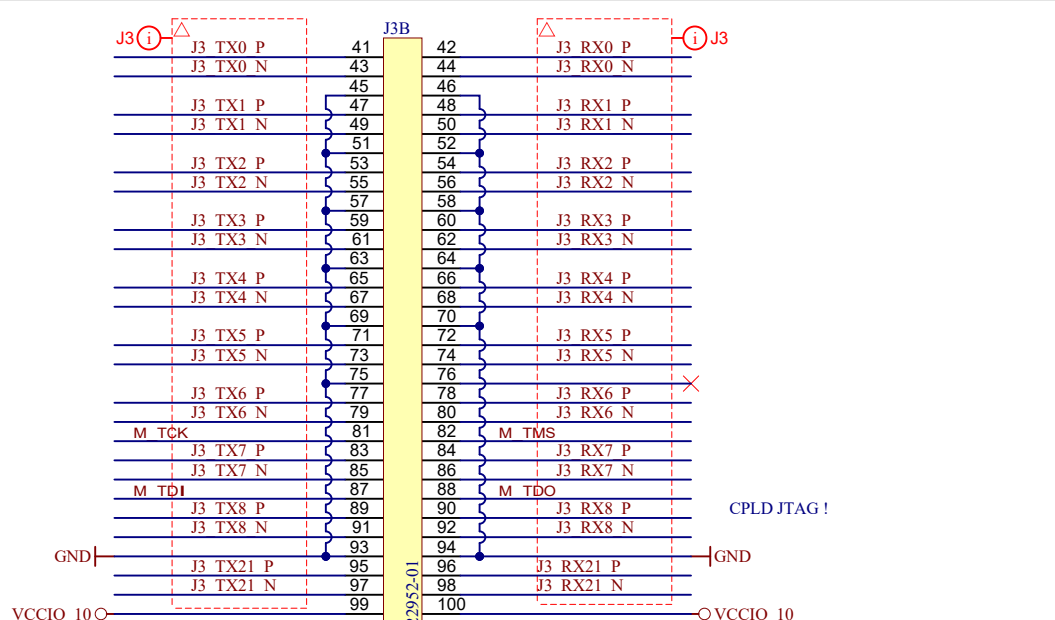
B

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D



Title: TE0784 - HSMC_Connector_J3		
A4	Number: TE0784 92I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 4 of 30
Filename: HSMC_CONN_J3.SchDoc		

A

A

B

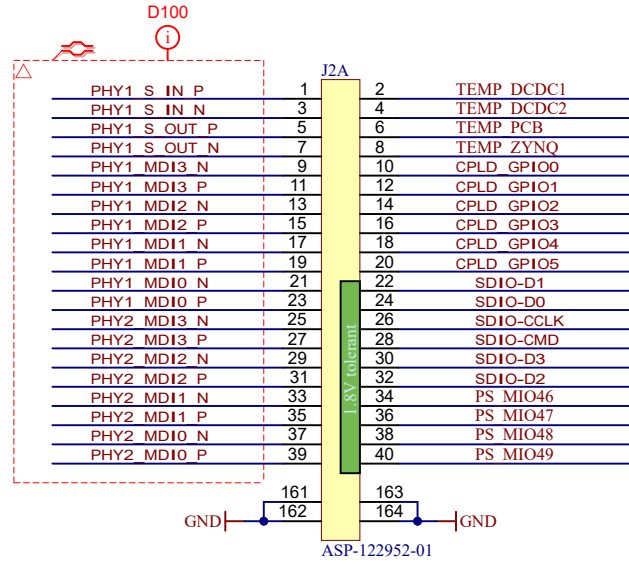
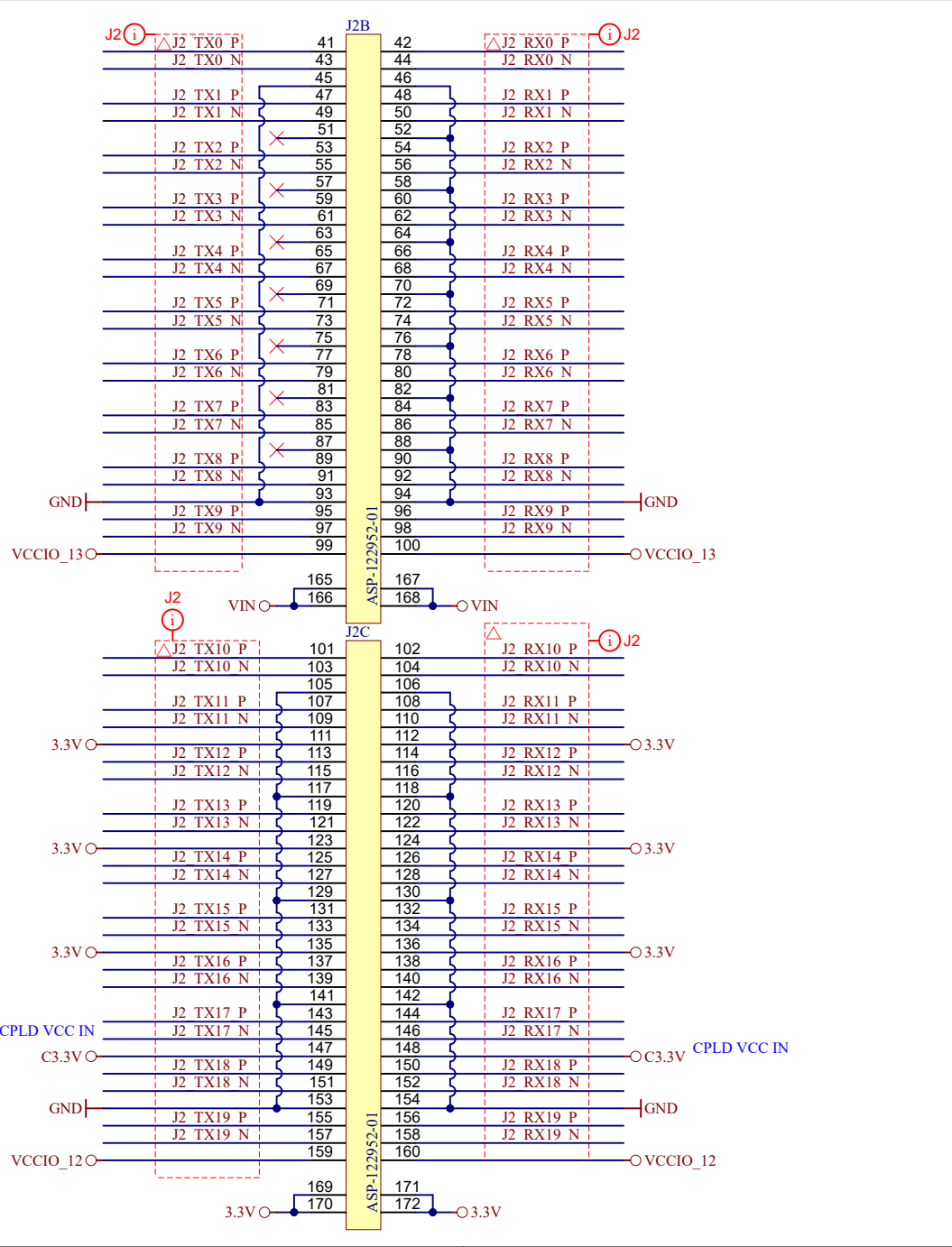
B

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CPLD C3.3V



Title: TE0784 - HSMC_Connector_J2		
A4	Number: TE0784 92I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page5 of 30
Filename: HSMC_CONN_J2.SchDoc		

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A

U_PS-DDR
PS-DDR.SchDoc



U_B9
B9.SchDoc



U_MIO-BANKS
MIO-BANKS.SchDoc



U_B10
B10.SchDoc



U_HP-BANKS
HP-BANKS.SchDoc



U_B11
B11.SchDoc



U_FPGA-MGT
FPGA-MGT.SchDoc



U_B12
B12.SchDoc



U_FPGA-CFG
FPGA-CFG.SchDoc



U_B13
B13.SchDoc



U_FPGA-PWR
FPGA-PWR.SchDoc



B

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D

A

B

C

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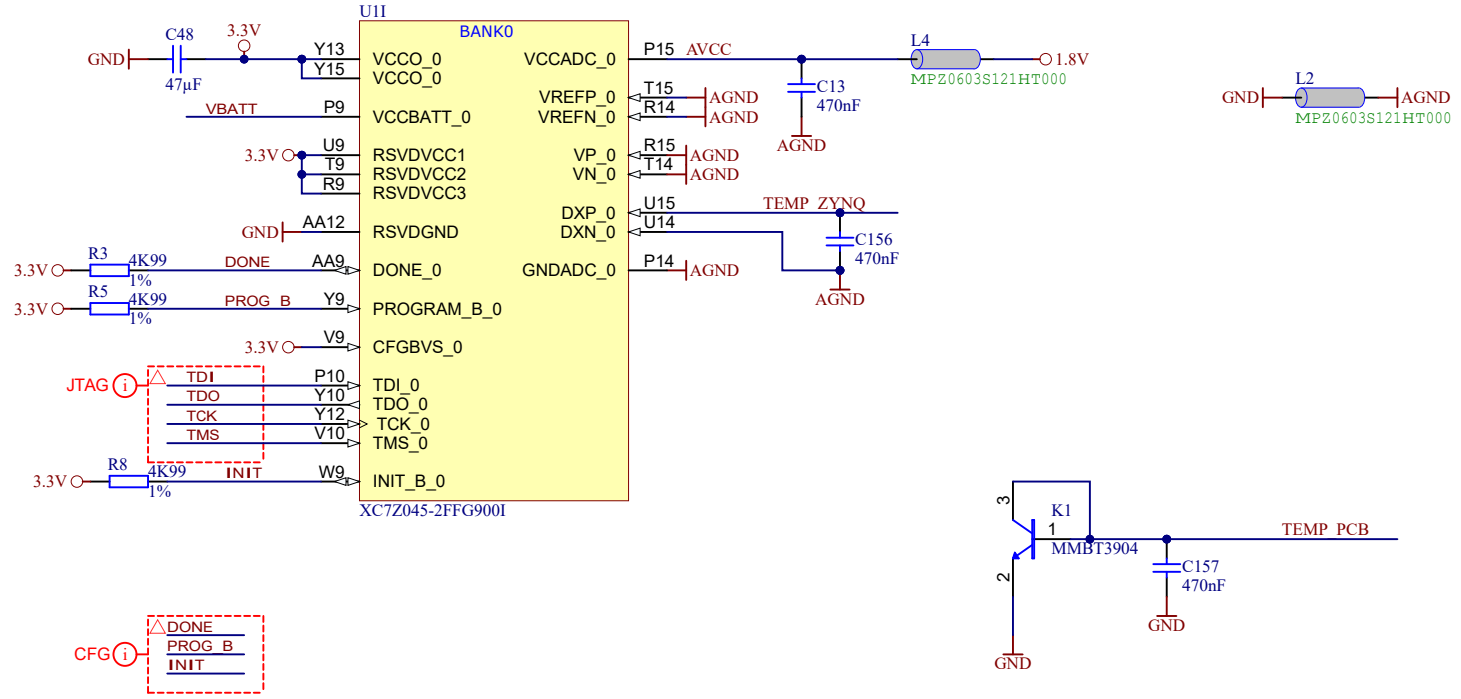
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			A4	Number: TE0784 92I33MA	Rev. 01
Date: 25.06.2018		Copyright: Trenz Electronic GmbH		Page6 of 30	
Filename: SOC.SchDoc					


1

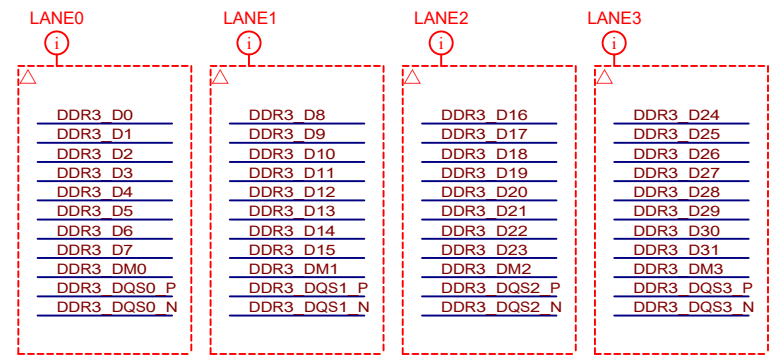
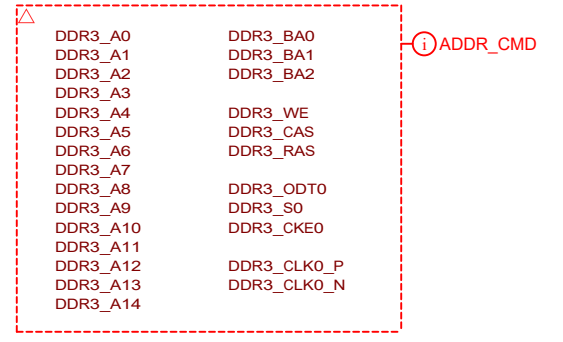
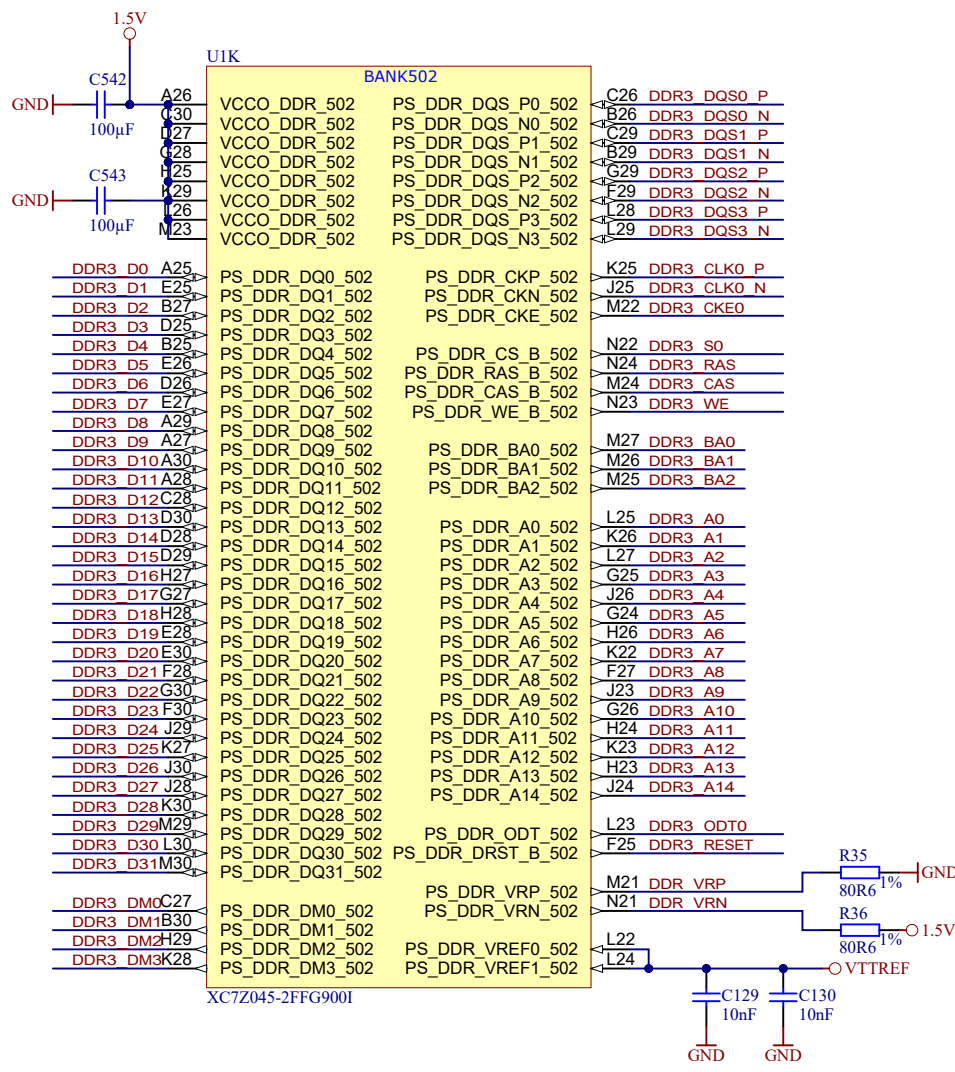
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3

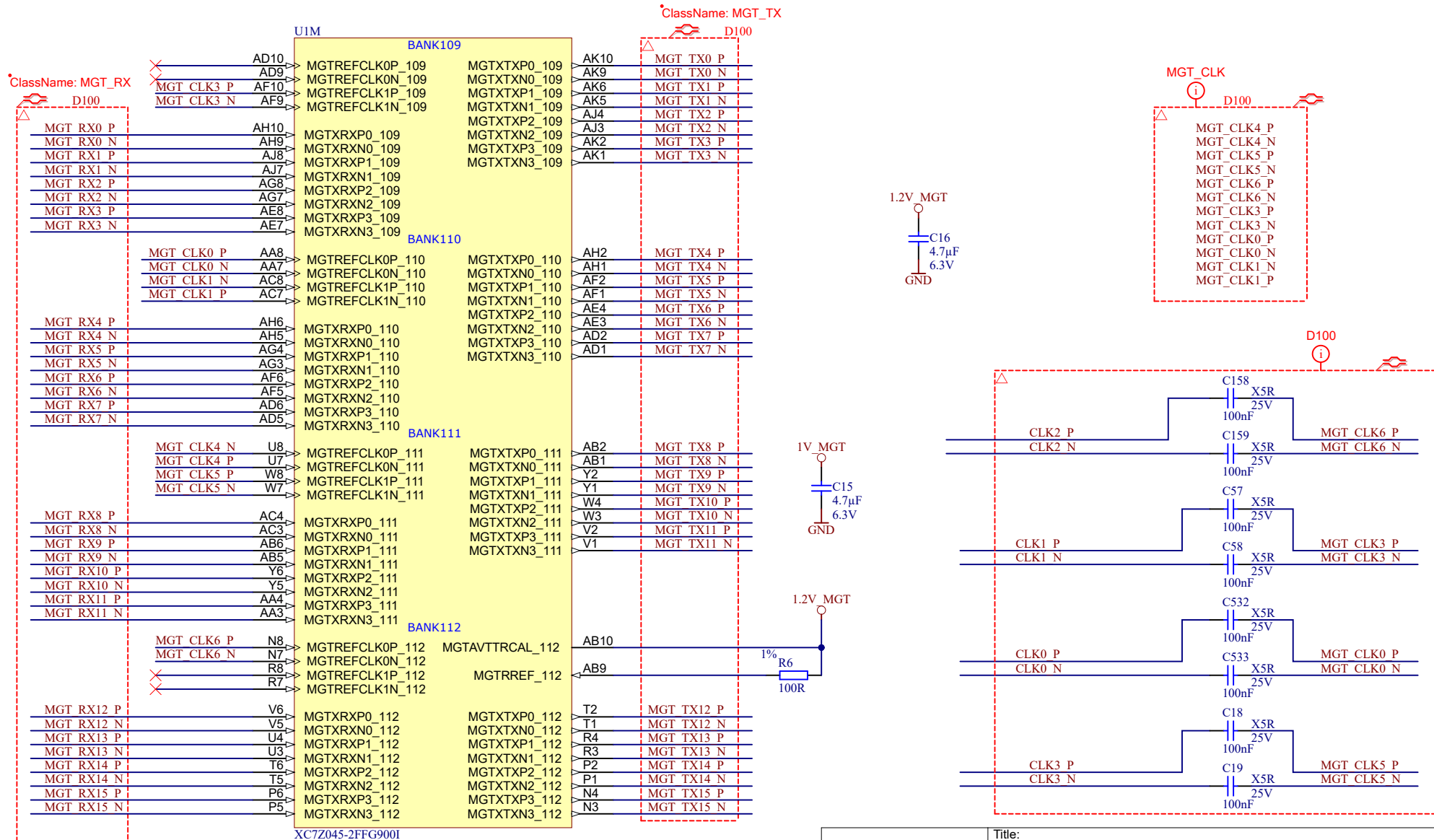
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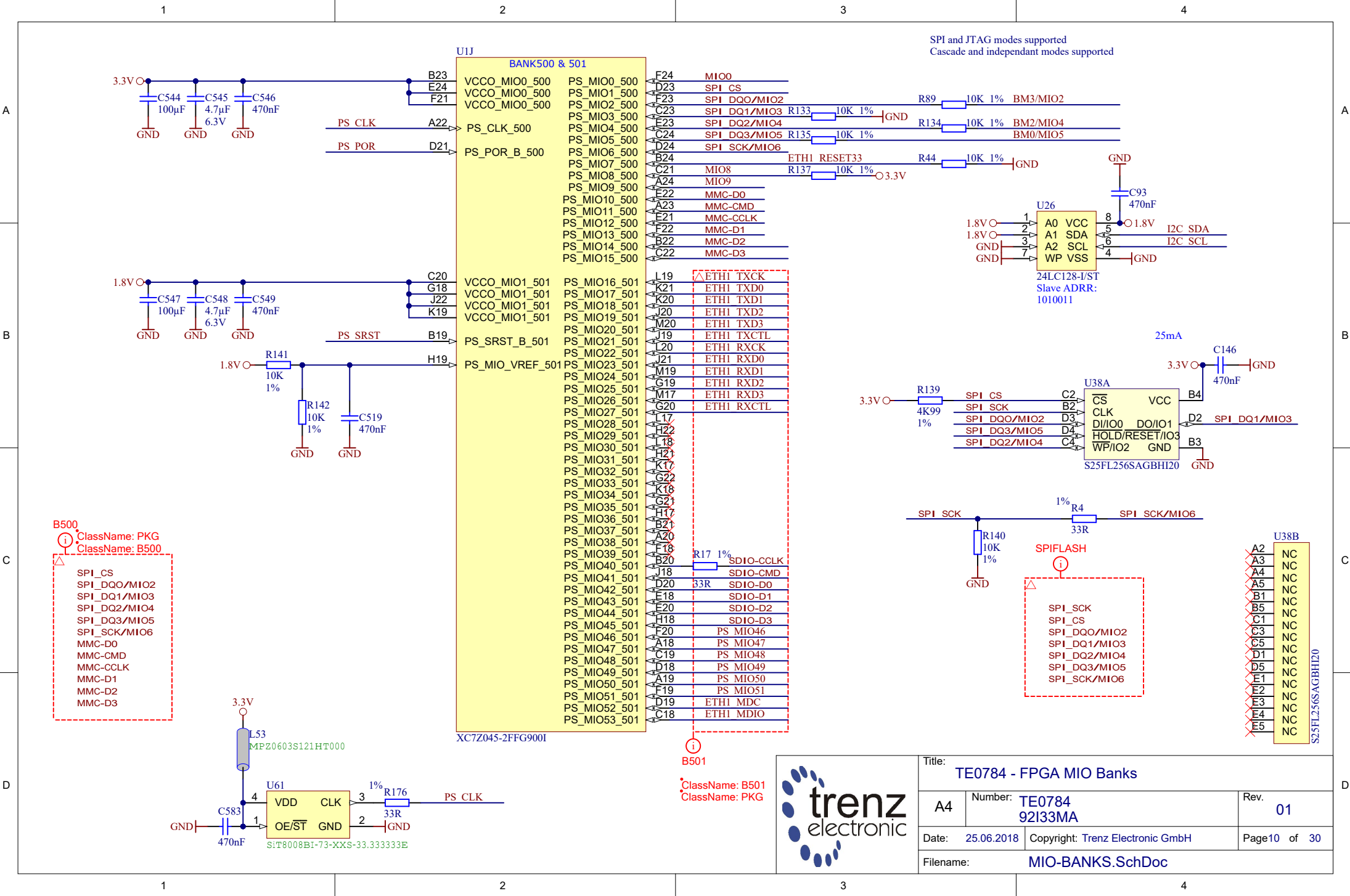
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		A4	Nummer: TE0784 92I33MA
Datum: 25.06.2018		Zeichner: Trenz Electronic GmbH	
Filename: FPGA-CFG.SchDoc		Blatt 7 von 30	



Title: TE0784 - FPGA DDR Banks		
A4	Number: TE0784 92133MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 8 of 30
Filename: PS-DDR.SchDoc		



Title: TE0784 - FPGA MGT		
A4	Number: TE0784 92133MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 9 of 30
Filename: FPGA-MGT.SchDoc		



SPI and JTAG modes supported
Cascade and independent modes supported

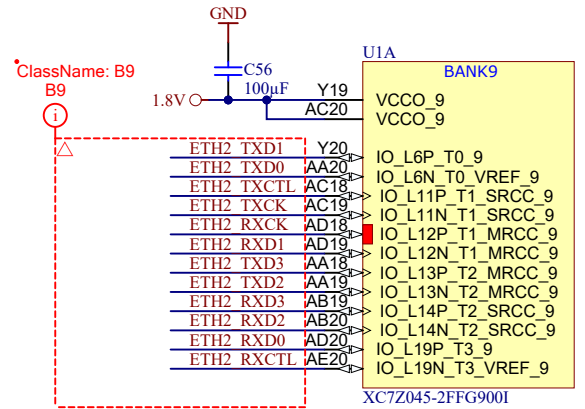
- B500**
- ClassName: PKG
 - ClassName: B500
 - SPI_CS
 - SPI_DQ0/MIO2
 - SPI_DQ1/MIO3
 - SPI_DQ2/MIO4
 - SPI_DQ3/MIO5
 - SPI_SCK/MIO6
 - MMC-D0
 - MMC-CMD
 - MMC-CCLK
 - MMC-D1
 - MMC-D2
 - MMC-D3

- SPIFLASH**
- SPI_SCK
 - SPI_CS
 - SPI_DQ0/MIO2
 - SPI_DQ1/MIO3
 - SPI_DQ2/MIO4
 - SPI_DQ3/MIO5
 - SPI_SCK/MIO6

- U38B**
- A2 NC
 - A3 NC
 - A4 NC
 - A5 NC
 - B1 NC
 - B5 NC
 - C1 NC
 - C3 NC
 - C5 NC
 - D1 NC
 - D5 NC
 - E1 NC
 - E3 NC
 - E4 NC
 - E5 NC




Title: TE0784 - FPGA MIO Banks		
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Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 10 of 30
Filename: MIO-BANKS.SchDoc		

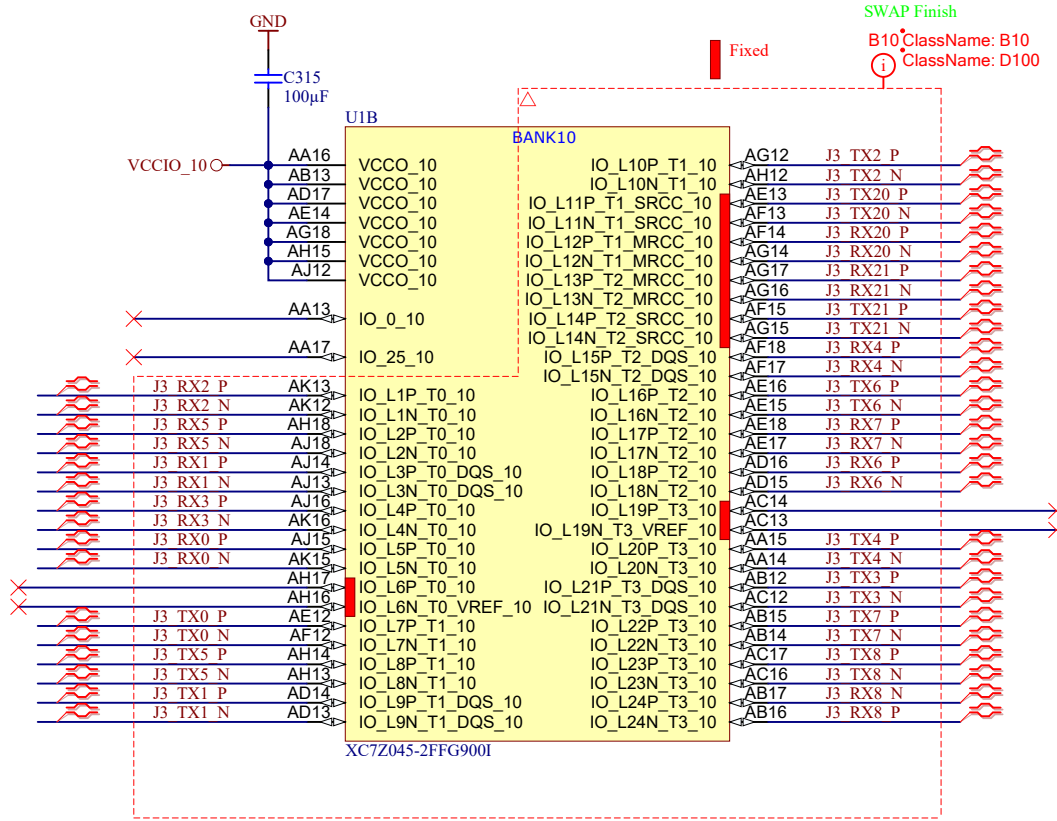


RXCK Fix to MRCCL

Fixed

			Title: TE0784 - FPGA B9	
			A4	Number: TE0784 92I33MA
Date: 25.06.2018		Copyright: Trenz Electronic GmbH		Page 11 of 30
Filename: B9.SchDoc				

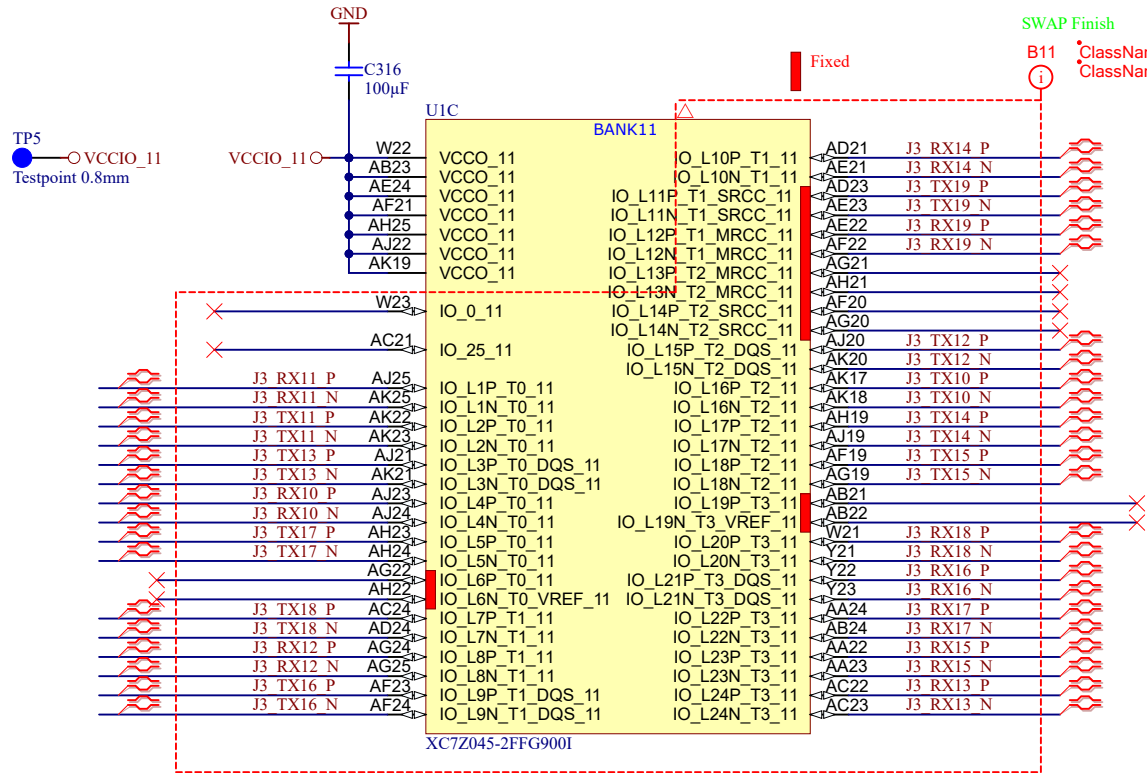
TP4
 ●—○ VCCIO_10
 Testpoint 0.8mm





SWAP Finish
 Fixed
 B10 ClassName: B10
 D100 ClassName: D100

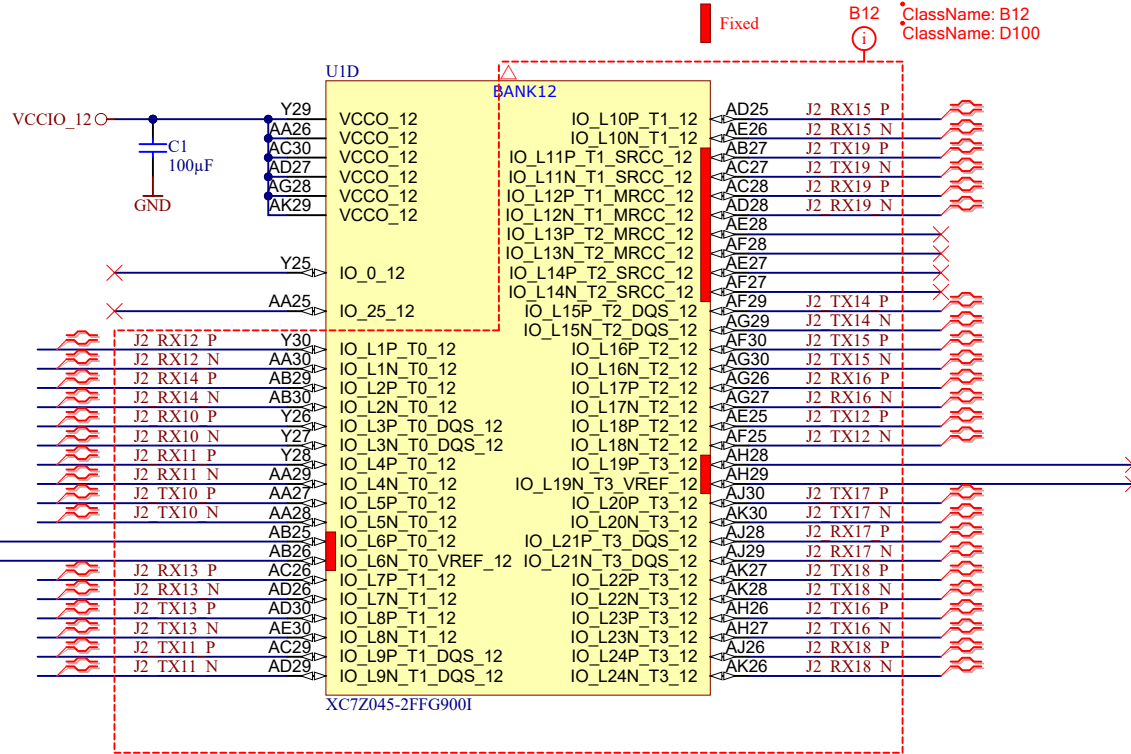



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Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 12 of 30
Filename: B10.SchDoc		




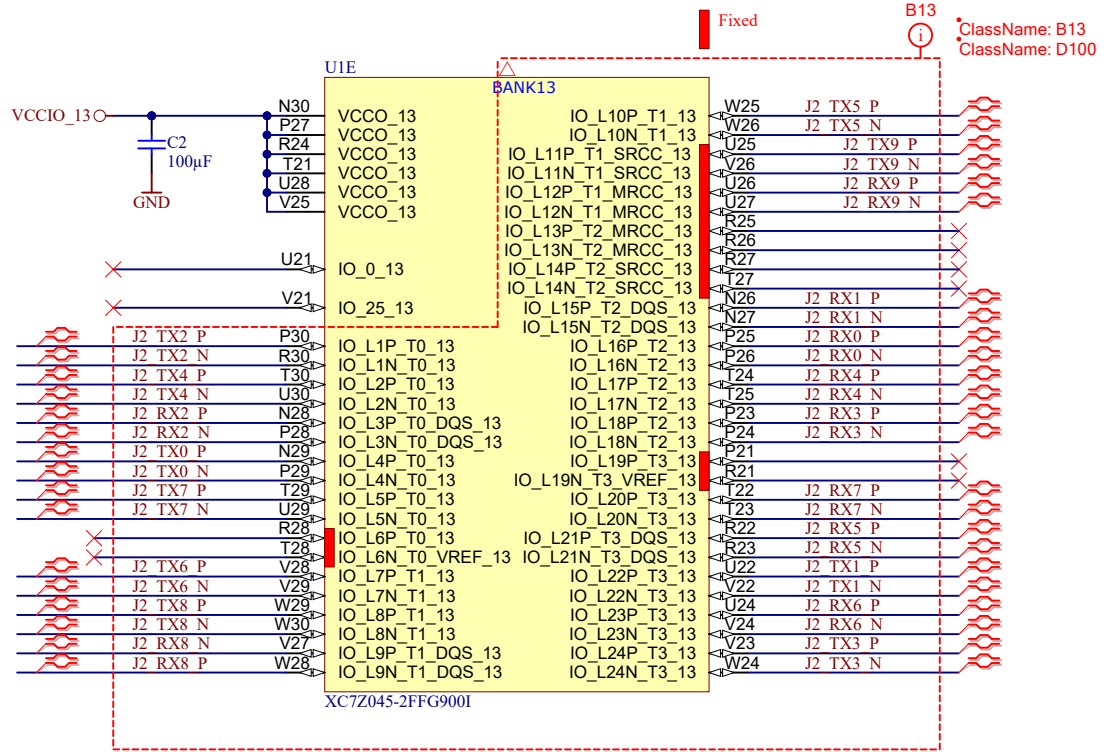
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		A4	Number: TE0784 92I33MA
Date: 25.06.2018		Copyright: Trenz Electronic GmbH	
Filename: B11.SchDoc		Page 13 of 30	


TP1
 VCCIO_12
 Testpoint 0.8mm



	Title: TE0784 - FPGA B12		
	A4	Number: TE0784 92I33MA	Rev. 01
	Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 14 of 30
	Filename: B12.SchDoc		

TP2
 VCCIO_13
 Testpoint 0.8mm



	Title: TE0784 - FPGA B13		
	A4	Number: TE0784 92I33MA	Rev. 01
	Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 15 of 30
	Filename: B13.SchDoc		

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U_B33
B33.SchDoc



U_B34
B34.SchDoc



U_B35
B35.SchDoc



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Title: TE0784 - FPGA HP Banks		
A4	Number: TE0784 92I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 16 of 30
Filename: HP-BANKS.SchDoc		

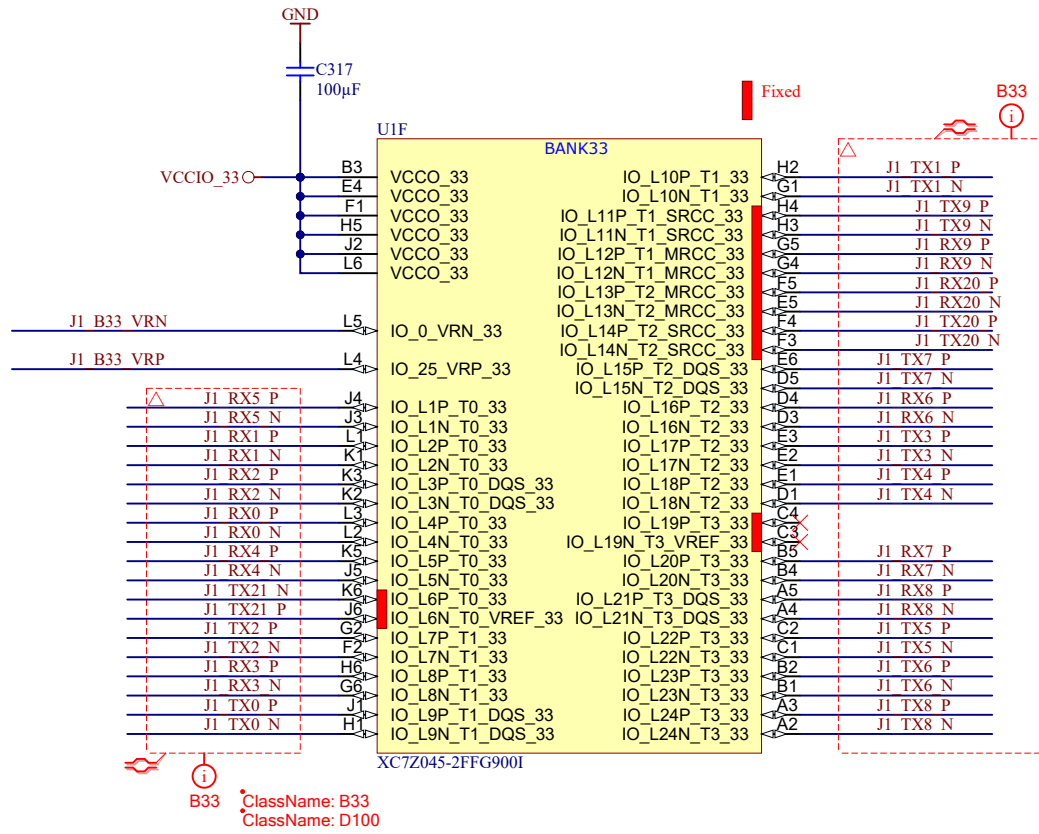
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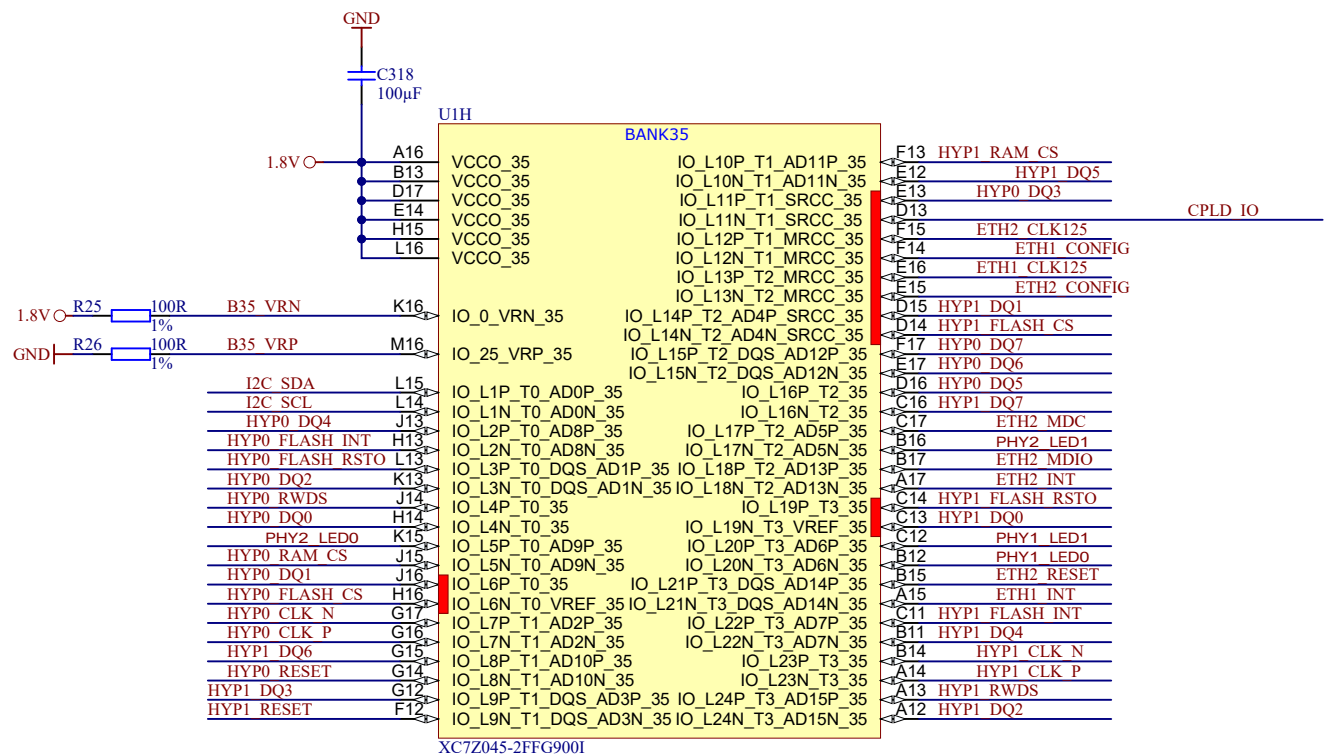
TP6
 VCCIO_33
 Testpoint 0.8mm



B33
 ClassName: B33
 ClassName: D100

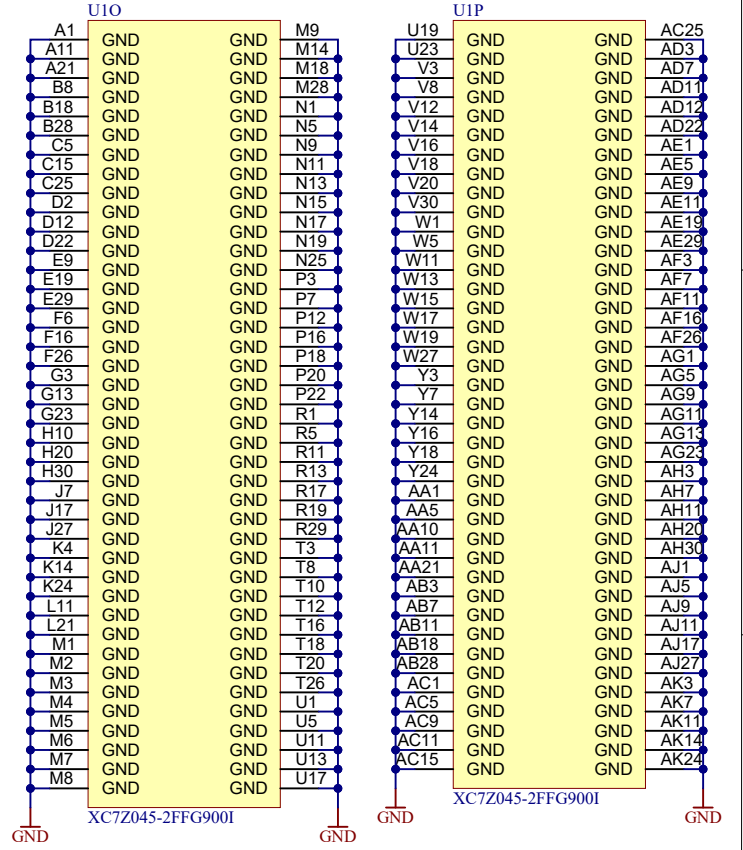
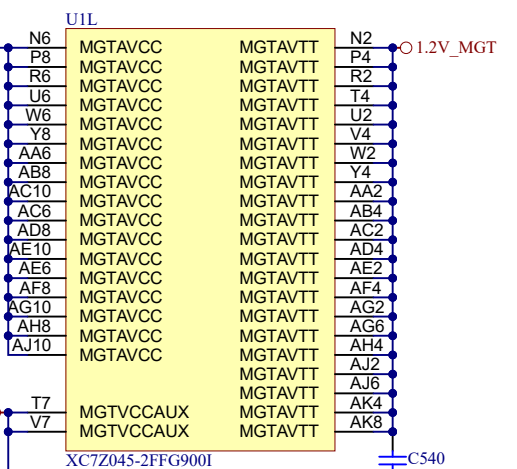
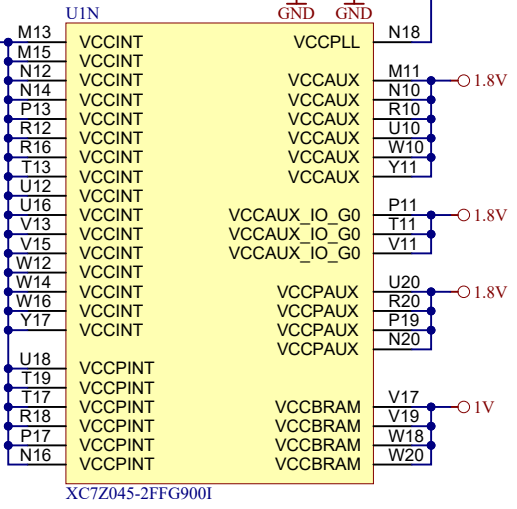
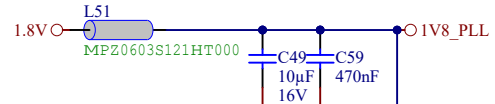
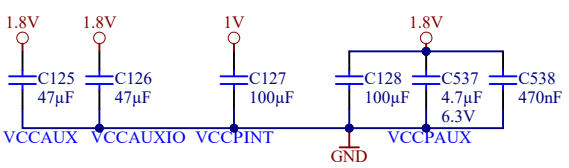
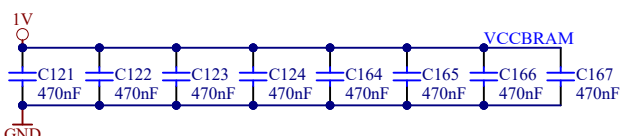
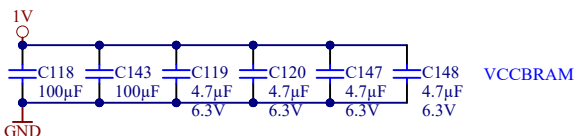
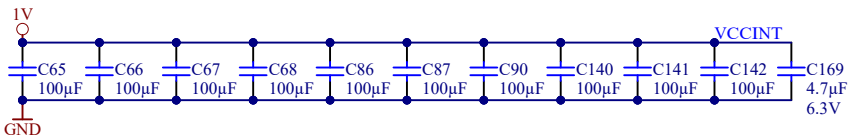
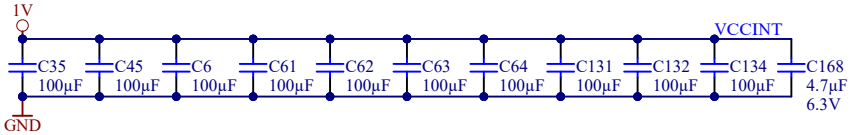
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 ClassName: B33
 ClassName: D100

	Title: TE0784 - FPGA B33		
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	Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 17 of 30
	Filename: B33.SchDoc		

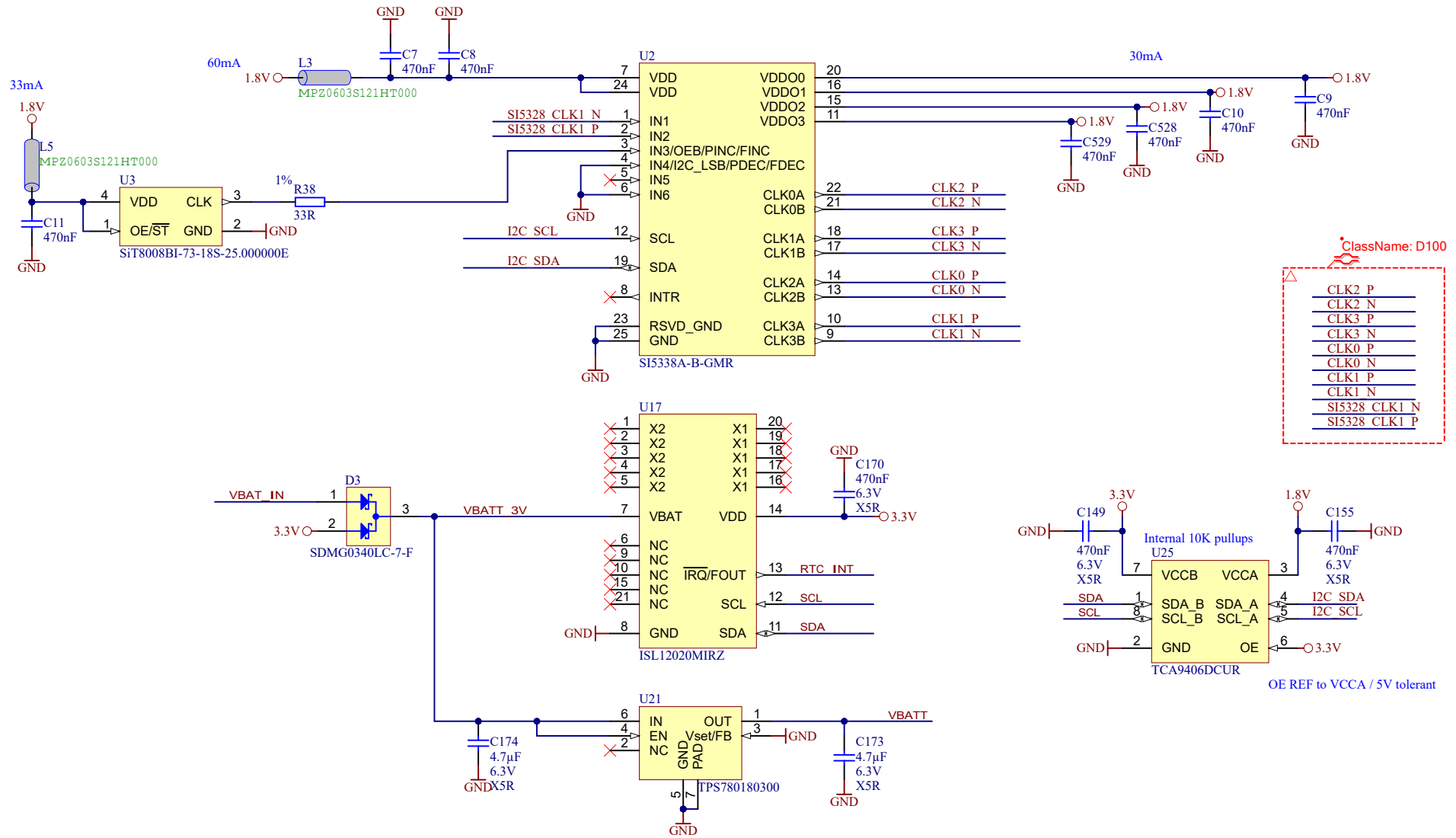


Title: TE0784 - FPGA B35		
A4	Number: TE0784 92I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 19 of 30
Filename: B35.SchDoc		

Capacitors suitable for XC7Z100



Title: TE0784 - ZYNQ POWER		
A4	Number: TE0784 92I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page20 of 30
Filename: FPGA-PWR.SchDoc		



	Title: TE0784 - Clock	
	A4	Number: TE0784 92133MA
	Date: 25.06.2018	Copyright: Trenz Electronic GmbH
	Filename: Clock.SchDoc	Page 21 of 30

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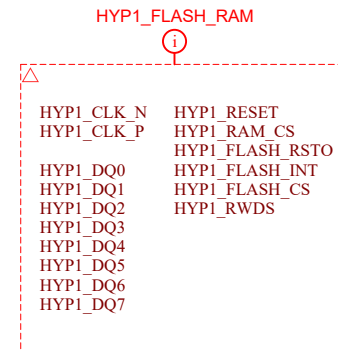
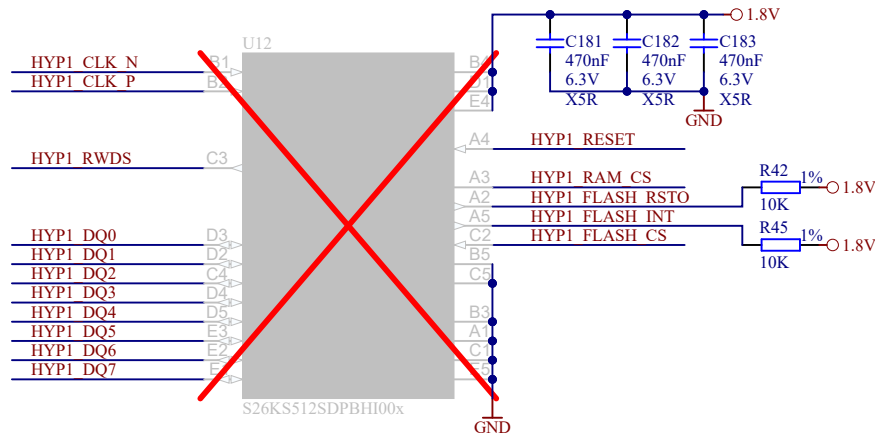
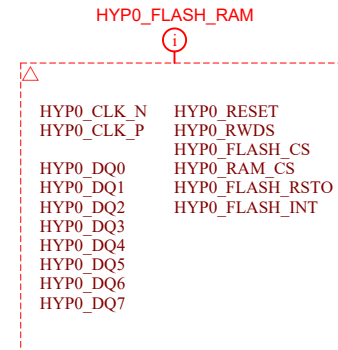
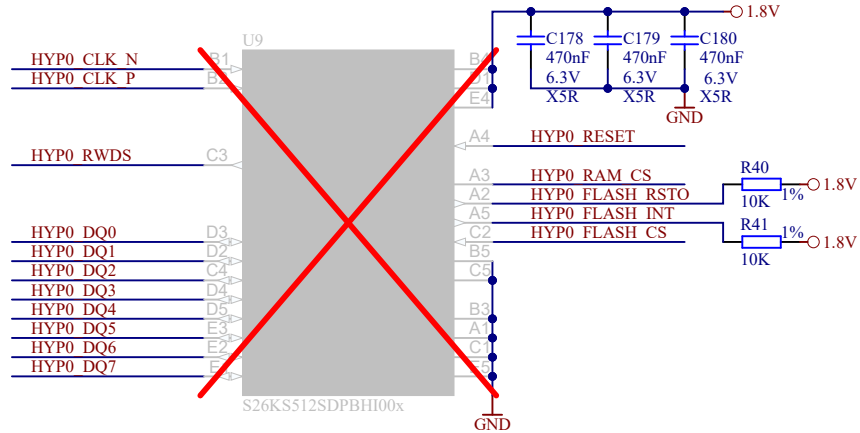
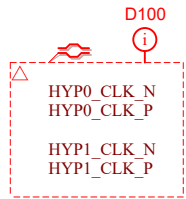

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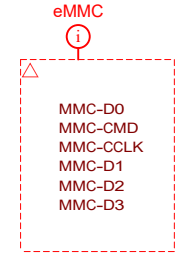
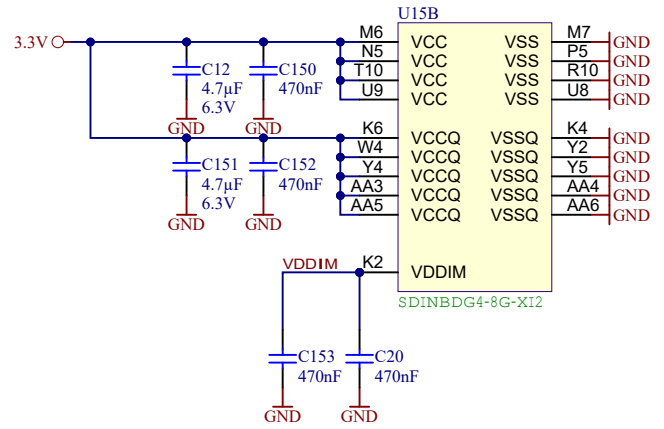
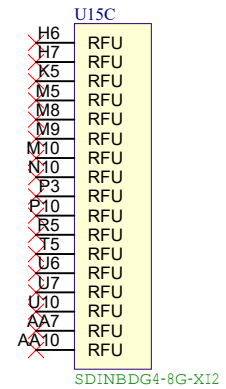
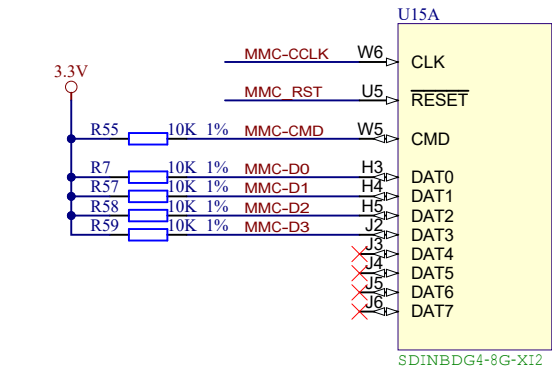
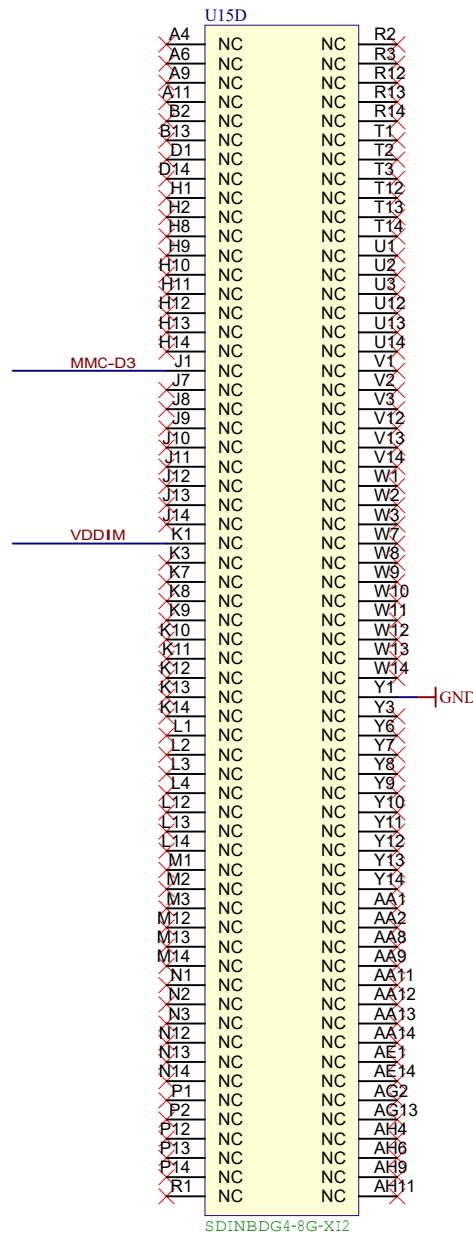
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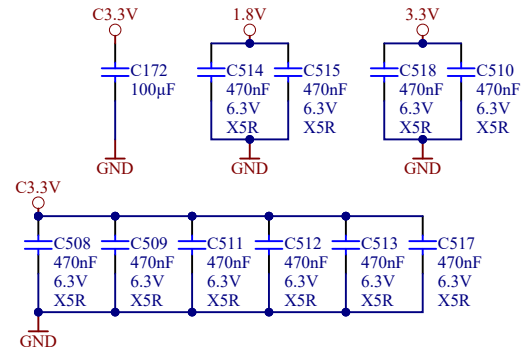
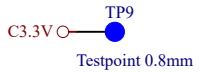
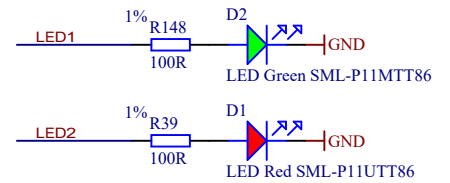
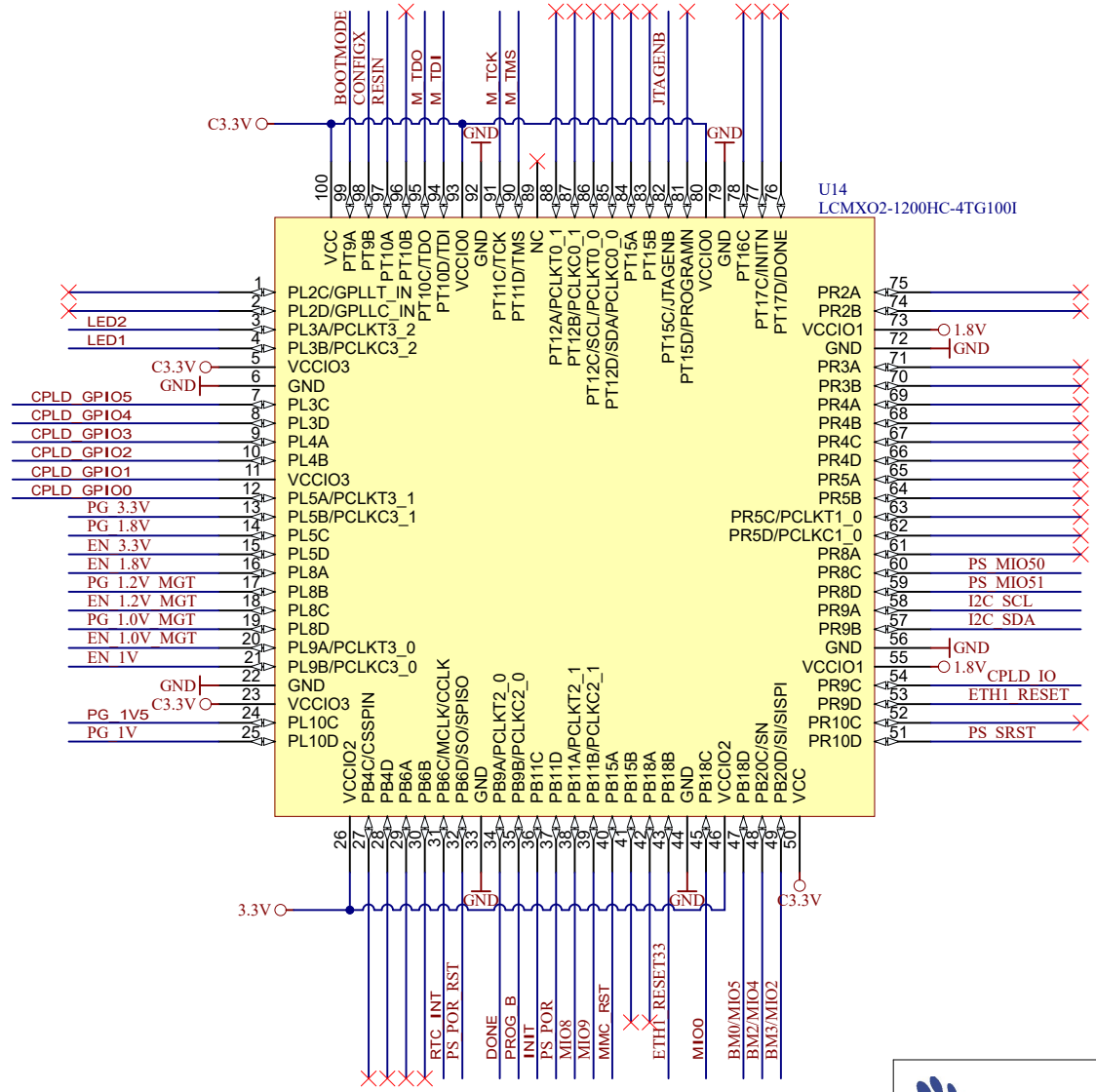
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Title: TE0784 - HyperFlash_RAM		
A4	Number: TE0784 92I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 23 of 30
Filename: HyperFlash_RAM.SchDoc		



Title: TE0784 - eMMC		
A4	Number: TE0784 92I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page24 of 30
Filename: eMMC.SchDoc		



Title: TE0784 - CPLD		
A4	Number: TE0784 92I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 25 of 30
Filename: CPLD.SchDoc		

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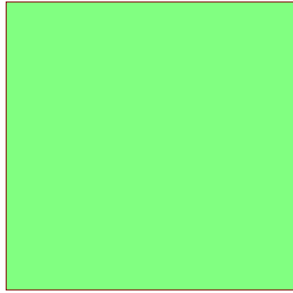
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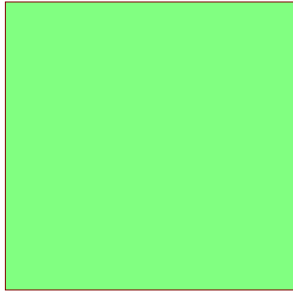
A

A

U_ETH1
ETH1.SchDoc



U_ETH2
ETH2.SchDoc



B


B

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	Title: TE0784 - Ethernet		
	A4	Number: TE0784 92I33MA	Rev. 01
	Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 26 of 30
	Filename: Ethernet.SchDoc		

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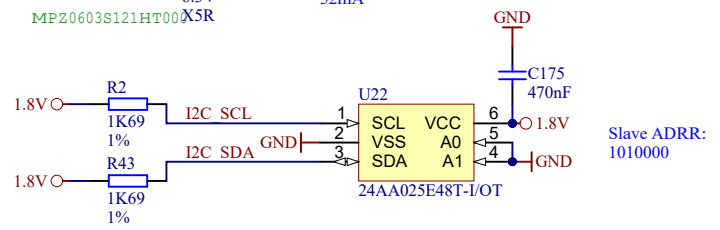
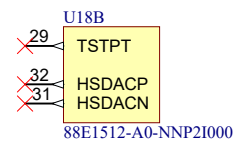
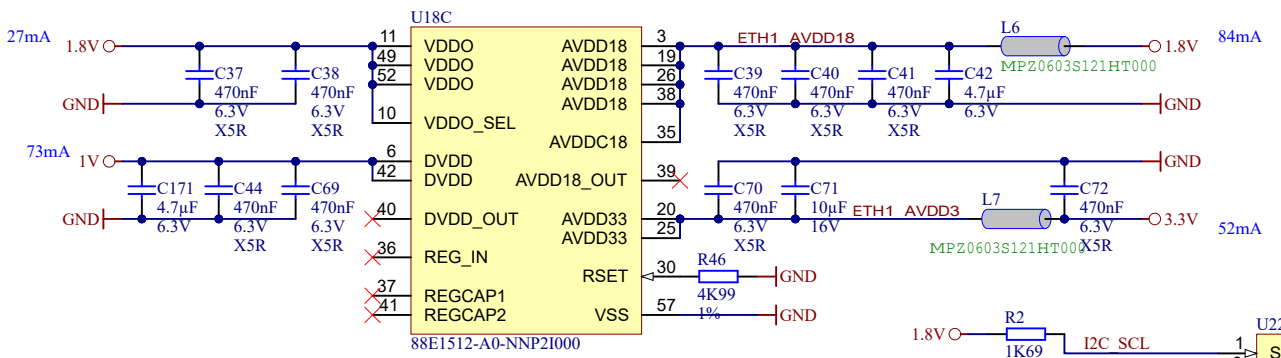
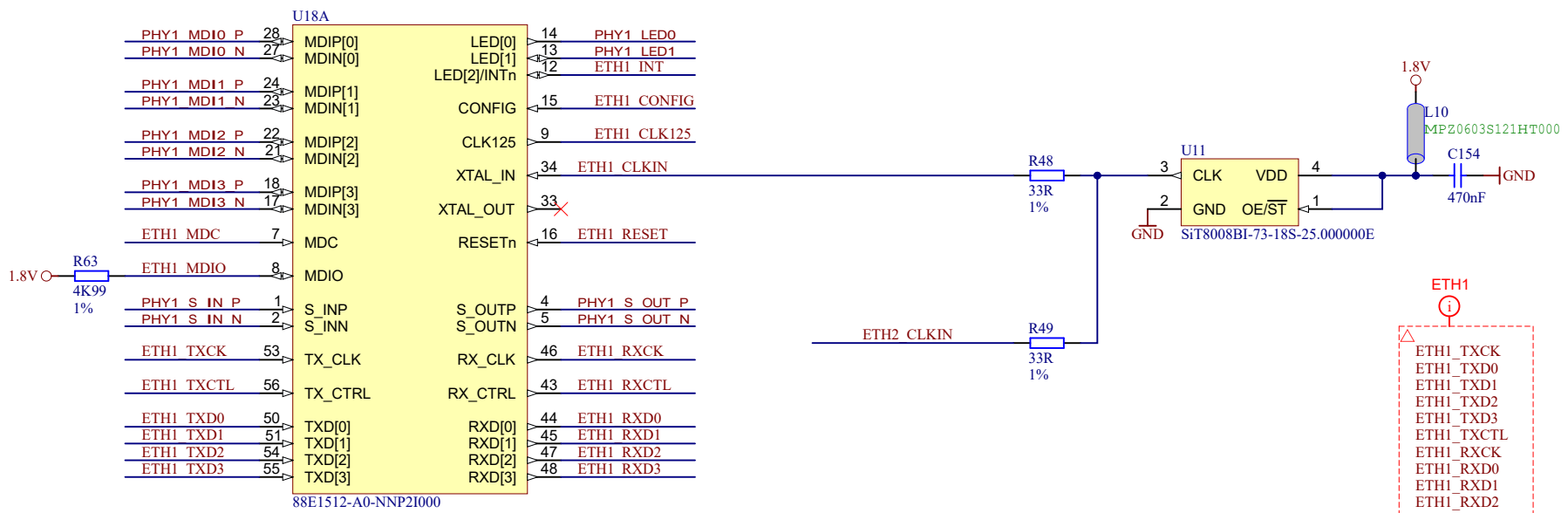
B

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Title: TE0784 - ETH_PHY1		
A4	Number: TE0784 92I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 27 of 30
Filename: ETH1.SchDoc		

A

A

B

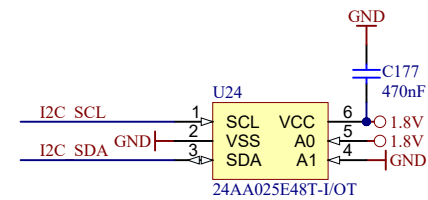
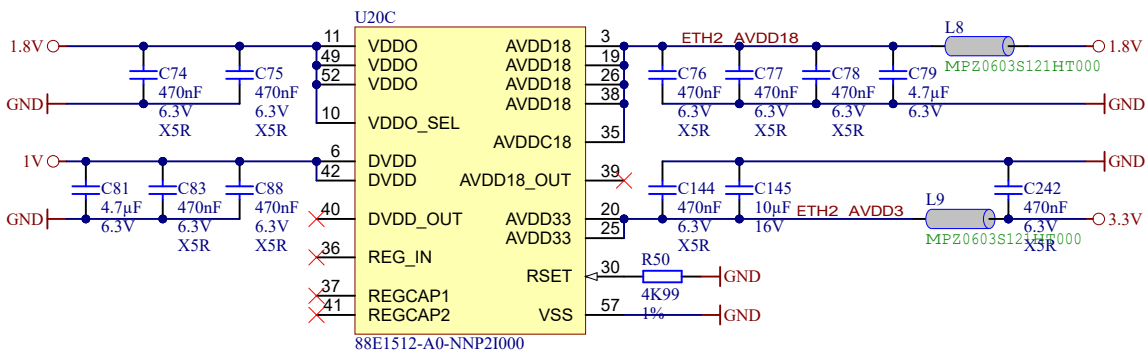
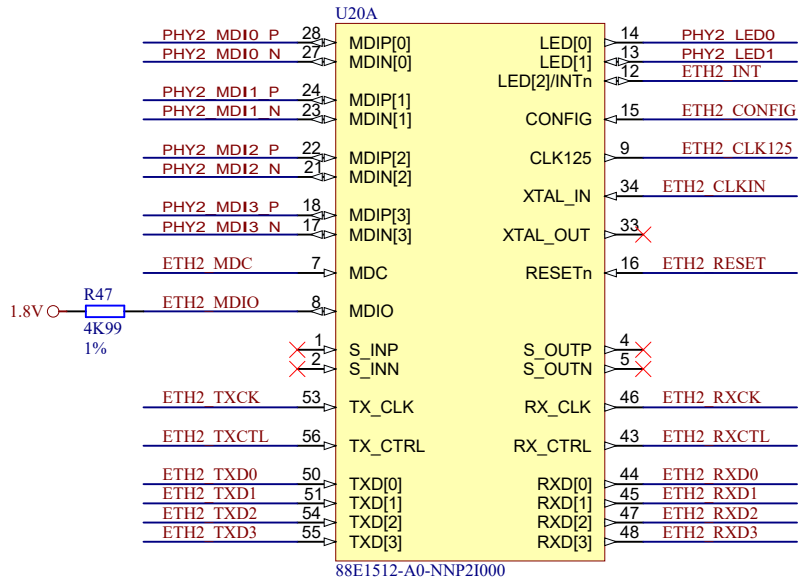
B

C

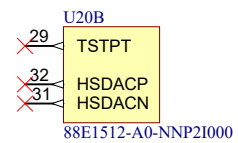
C

D

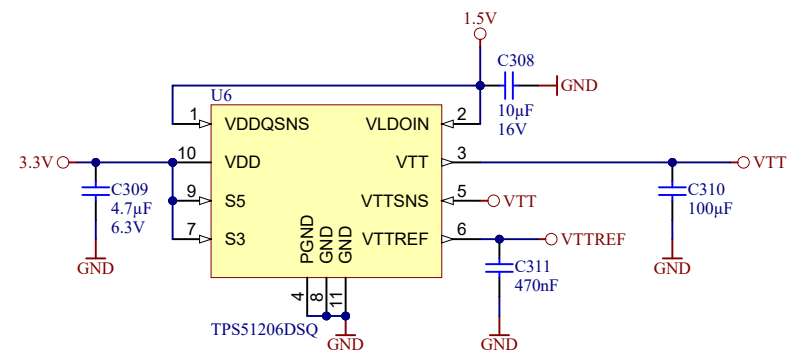
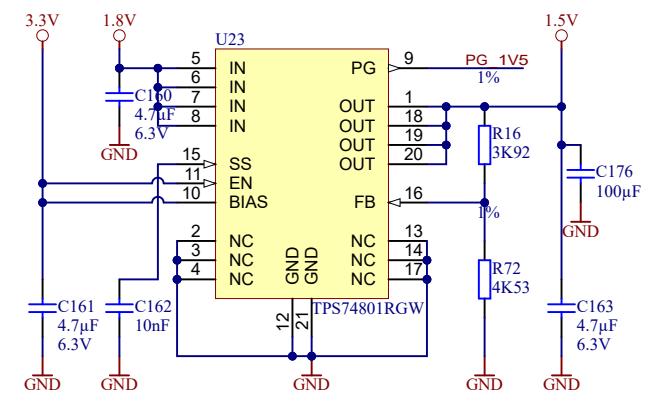
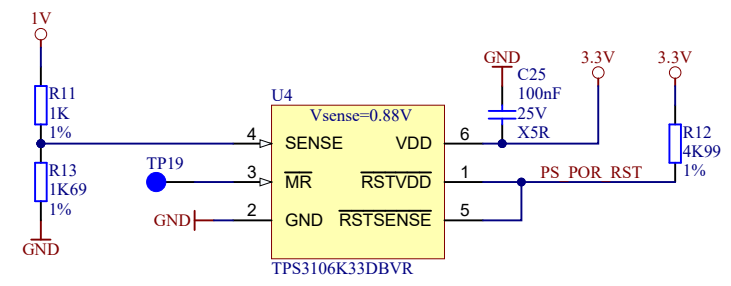
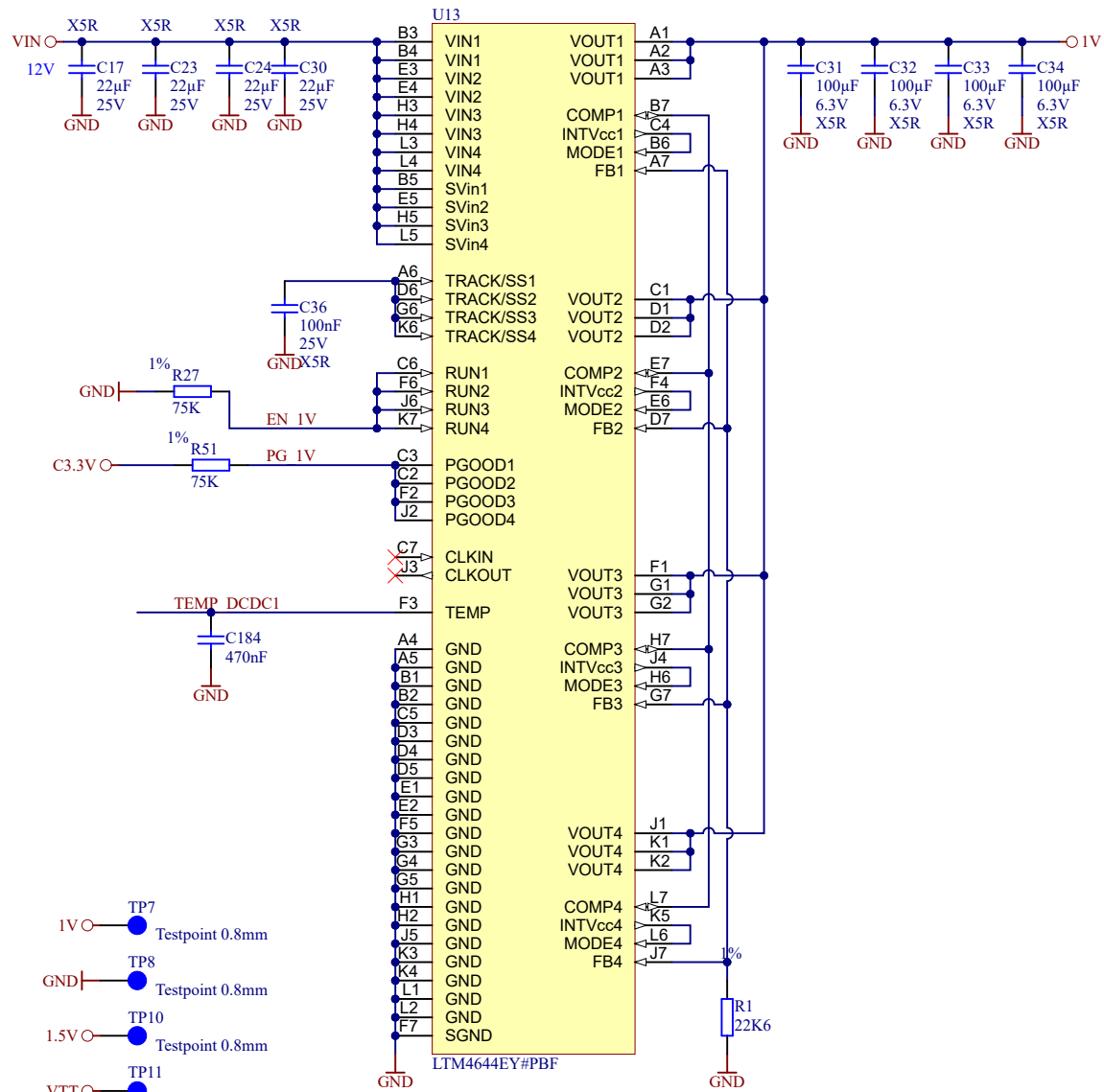
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Slave ADDR: 1010001

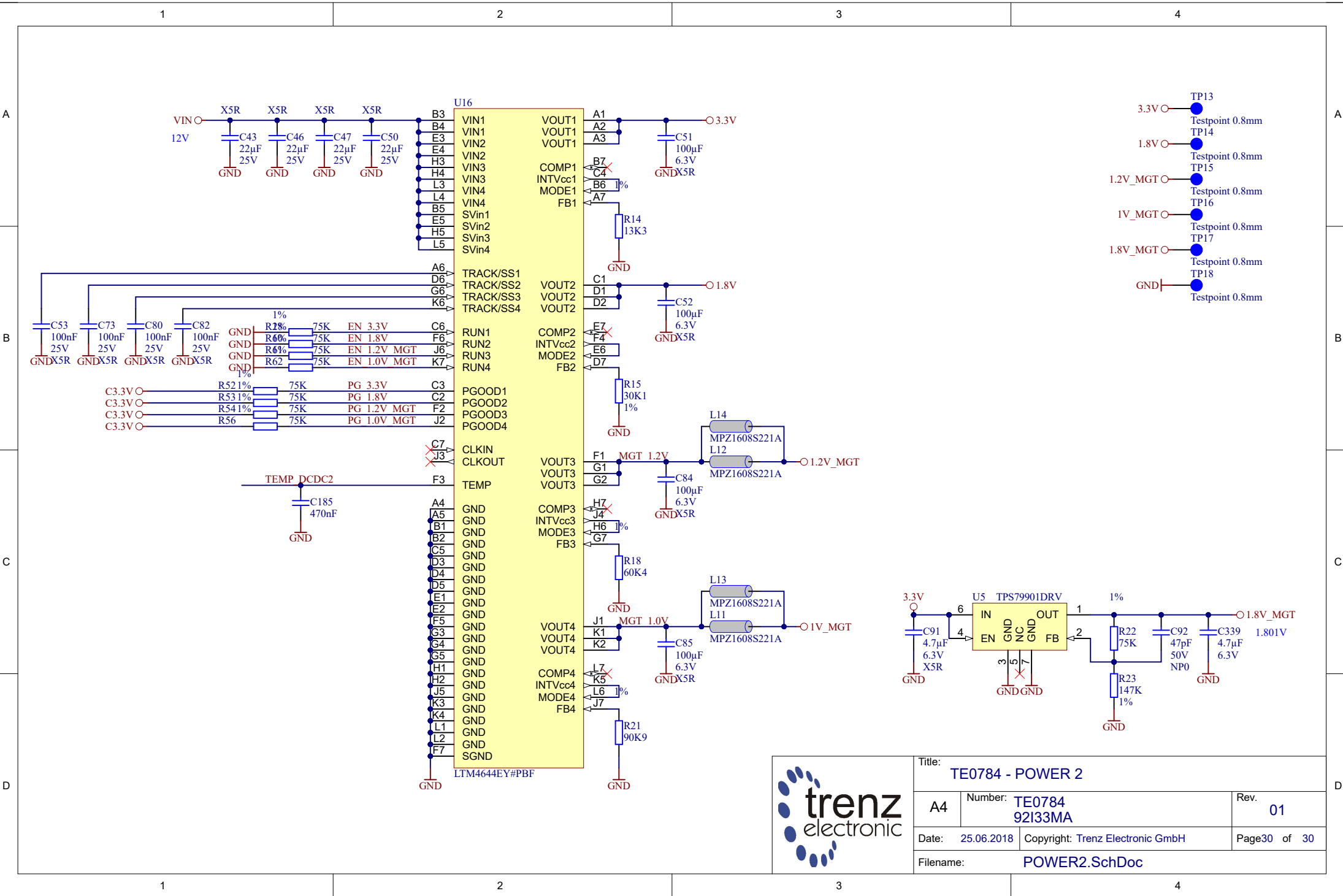


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- IV ○ ● TP7 Testpoint 0.8mm
- GND ○ ● TP8 Testpoint 0.8mm
- 1.5V ○ ● TP10 Testpoint 0.8mm
- VTT ○ ● TP11 Testpoint 0.8mm
- VTTREF ○ ● TP12 Testpoint 0.8mm

			Title: TE0784 - POWER	
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- 3.3V ○ TP13 Testpoint 0.8mm
- 1.8V ○ TP14 Testpoint 0.8mm
- 1.2V_MGT ○ TP15 Testpoint 0.8mm
- 1V_MGT ○ TP16 Testpoint 0.8mm
- 1.8V_MGT ○ TP17 Testpoint 0.8mm
- GND ○ TP18 Testpoint 0.8mm



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