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U\_DDR3-RAM  
DDR3-RAM.SchDoc

U\_Ethernet  
Ethernet.SchDoc

U\_SOC  
SOC.SchDoc

U\_CPLD  
CPLD.SchDoc

U\_POWER2  
POWER2.SchDoc

U\_HyperFlash\_RAM  
HyperFlash\_RAM.SchDoc

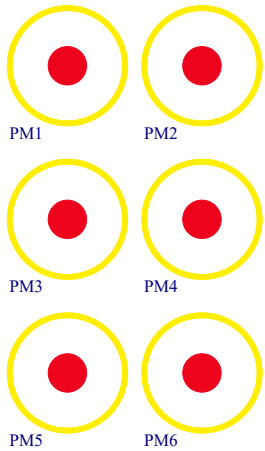
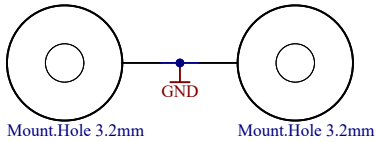
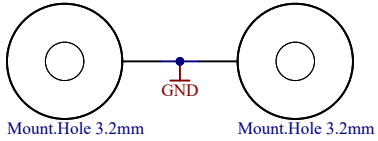
U\_Clock  
Clock.SchDoc

U\_eMMC  
eMMC.SchDoc

U\_Connectors  
Connectors.SchDoc

U\_POWER  
POWER.SchDoc

LOGO1  
TE Logo PRINT Layer  
LOGO PRINT



Serial  
Serialnummer 6,3 x 6.3mm



Design drawn by:	*
Checked by:	*
Assembly variant:	A2I33MA
Created by:	MR
Modified by:	MR
Modified at:	2021-10-25



Title: TE0784 - Overview		
A4	Number: TE0784 A2I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page1 of 30
Filename: TE0784.SchDoc		

1

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A

A

B

B

C

C

D

D

1

2

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U\_HSMC\_CONN\_J1  
HSMC\_CONN\_J1.SchDoc



U\_HSMC\_CONN\_J2  
HSMC\_CONN\_J2.SchDoc



U\_HSMC\_CONN\_J3  
HSMC\_CONN\_J3.SchDoc



A

A

B

B

C

C

D


D

1

2

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			Title: <b>TE0784 - Connectors</b>		
			A4	Number: <b>TE0784 A2133MA</b>	Rev. <b>01</b>
Date: <b>25.06.2018</b>		Copyright: <b>Trenz Electronic GmbH</b>		Page <b>2</b> of <b>30</b>	
Filename: <b>Connectors.SchDoc</b>					

A

A

B

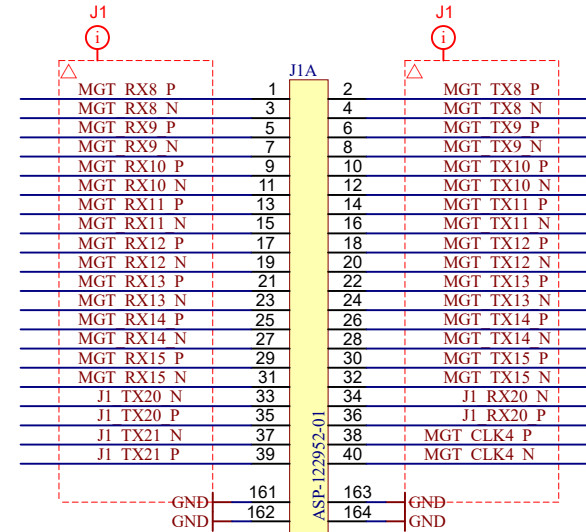
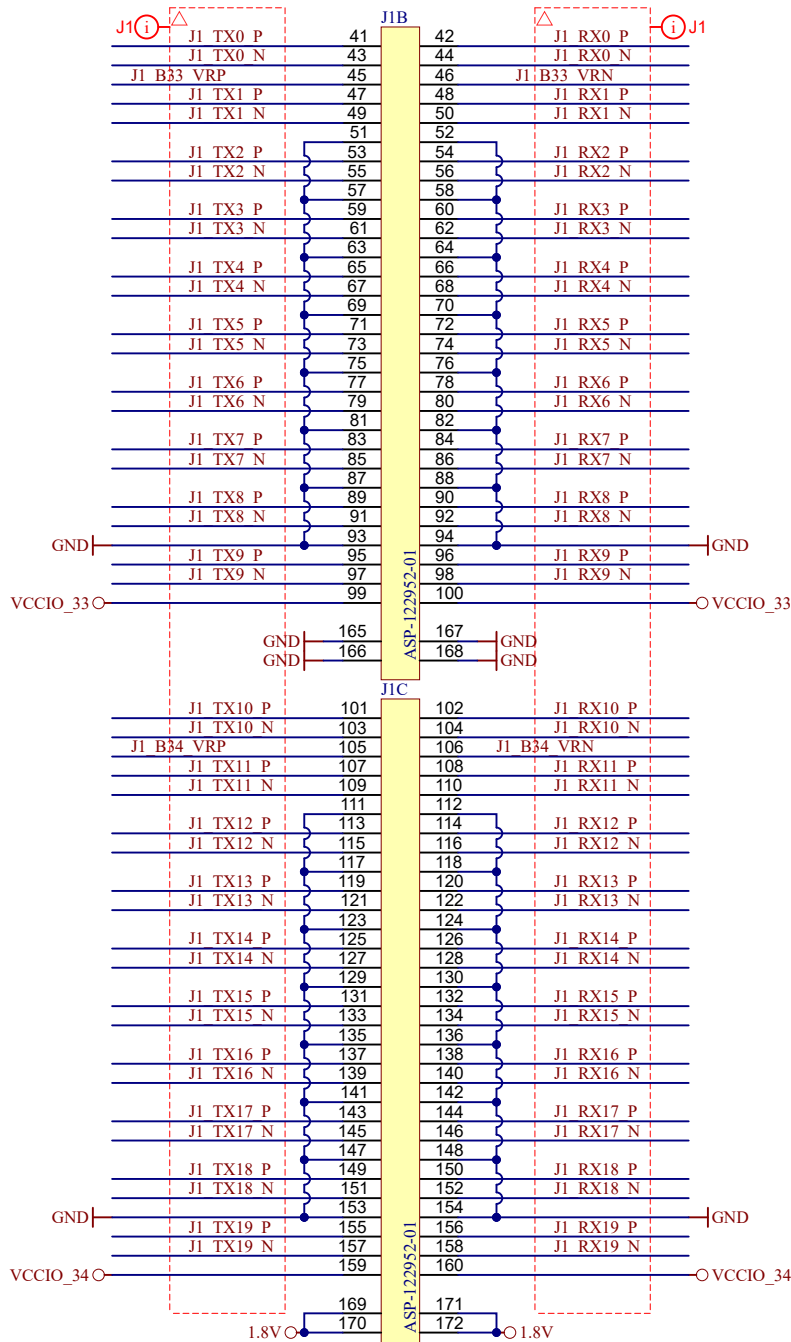
B

C

C

D

D



Title: TE0784 - HSMC_Connector_J1		
A4	Number: TE0784 A2133MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page3 of 30
Filename: HSMC_CONN_J1.SchDoc		

A

A

B

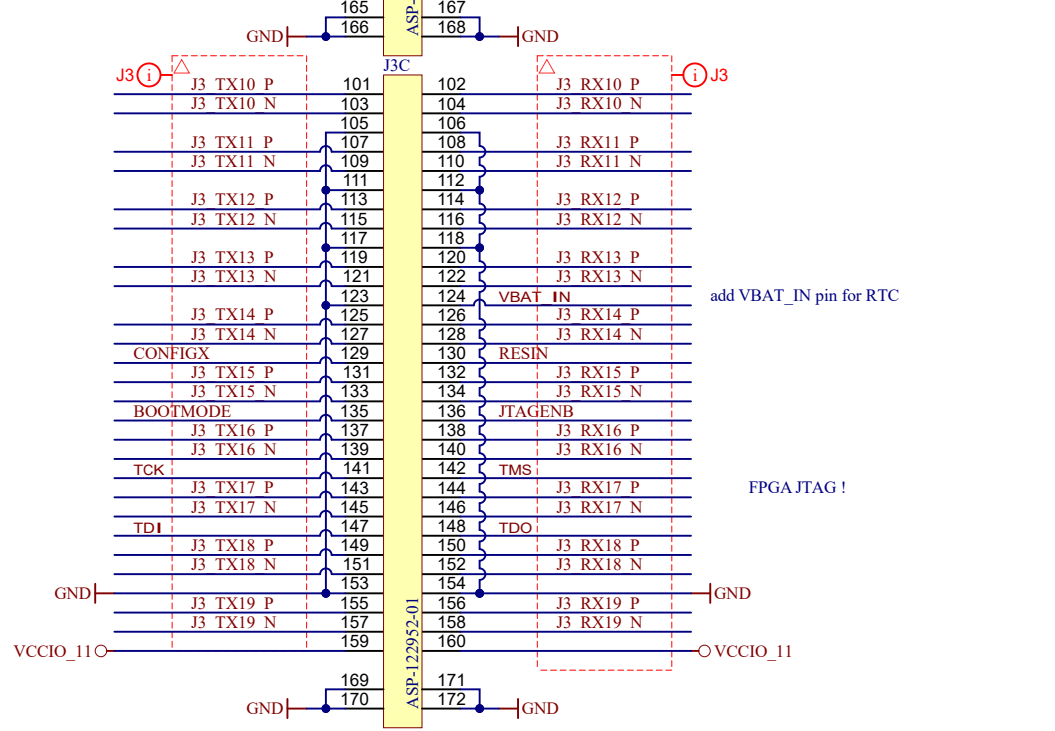
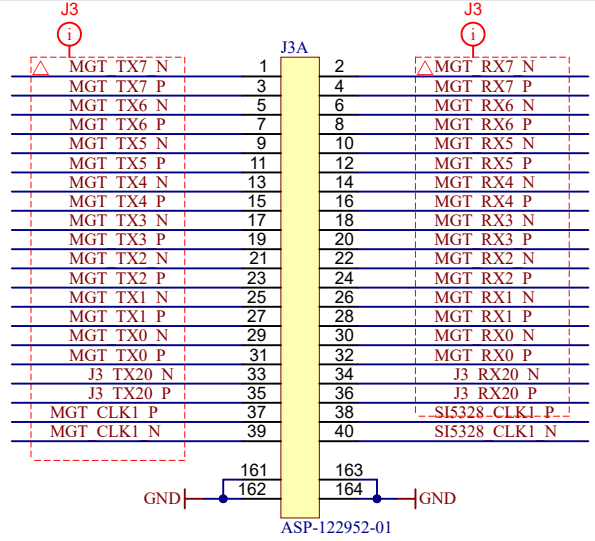
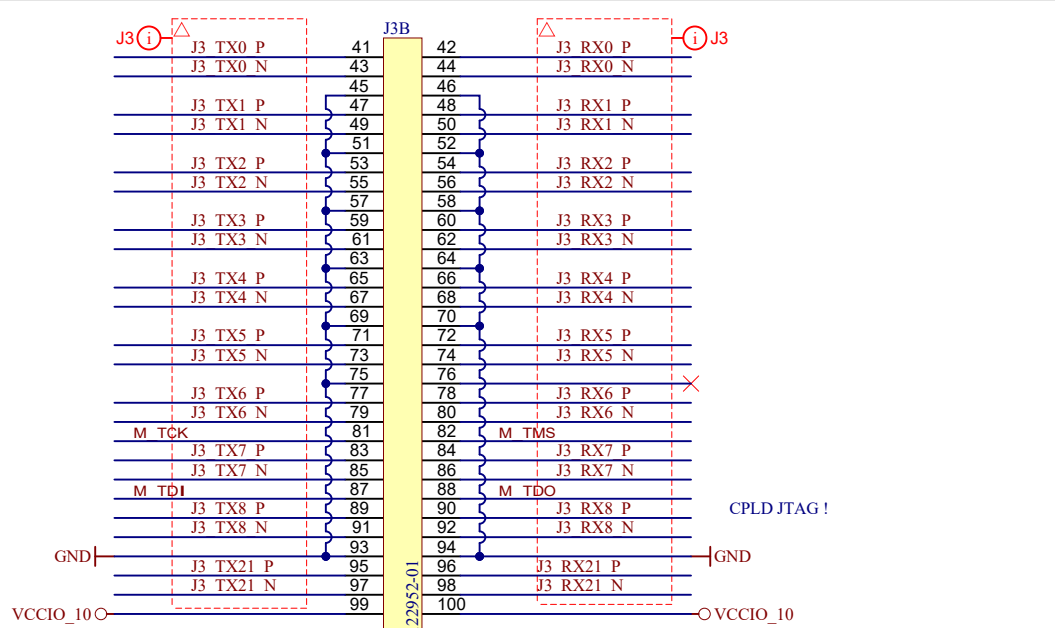
B

C

C

D

D



Title: TE0784 - HSMC_Connector_J3		
A4	Number: TE0784 A2133MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 4 of 30
Filename: HSMC_CONN_J3.SchDoc		

A

A

B

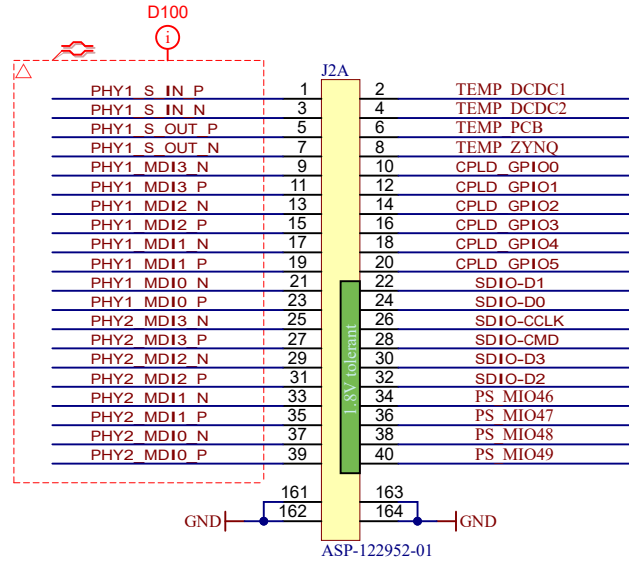
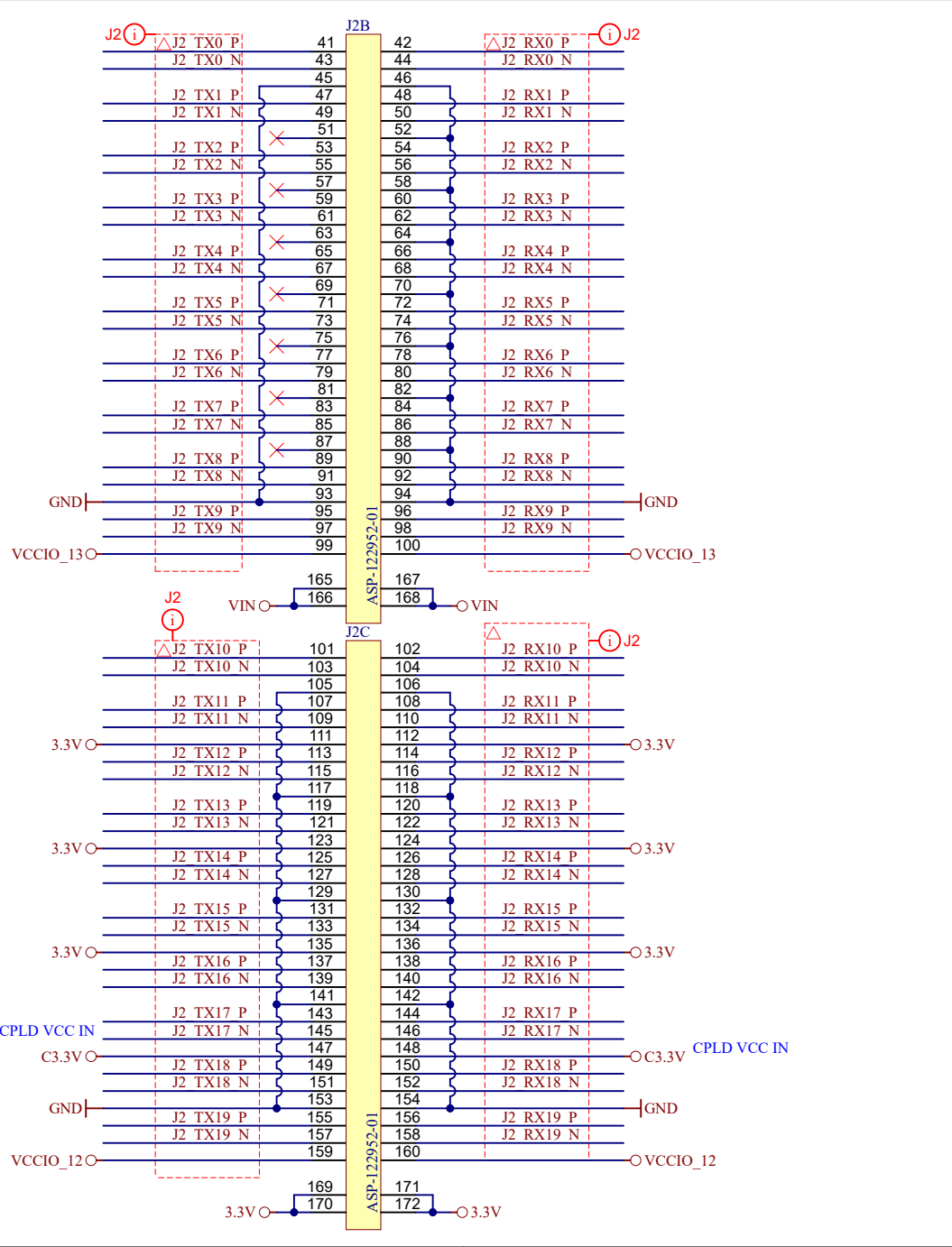
B

C

C

D

D



CPLD C3.3V



Title: TE0784 - HSMC_Connector_J2		
A4	Number: TE0784 A2I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page5 of 30
Filename: HSMC_CONN_J2.SchDoc		

1

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U\_PS-DDR  
PS-DDR.SchDoc



U\_B9  
B9.SchDoc



U\_MIO-BANKS  
MIO-BANKS.SchDoc



U\_B10  
B10.SchDoc



U\_HP-BANKS  
HP-BANKS.SchDoc



U\_B11  
B11.SchDoc



U\_FPGA-MGT  
FPGA-MGT.SchDoc



U\_B12  
B12.SchDoc



U\_FPGA-CFG  
FPGA-CFG.SchDoc



U\_B13  
B13.SchDoc



U\_FPGA-PWR  
FPGA-PWR.SchDoc



A

A

B

B

C

C

D


D

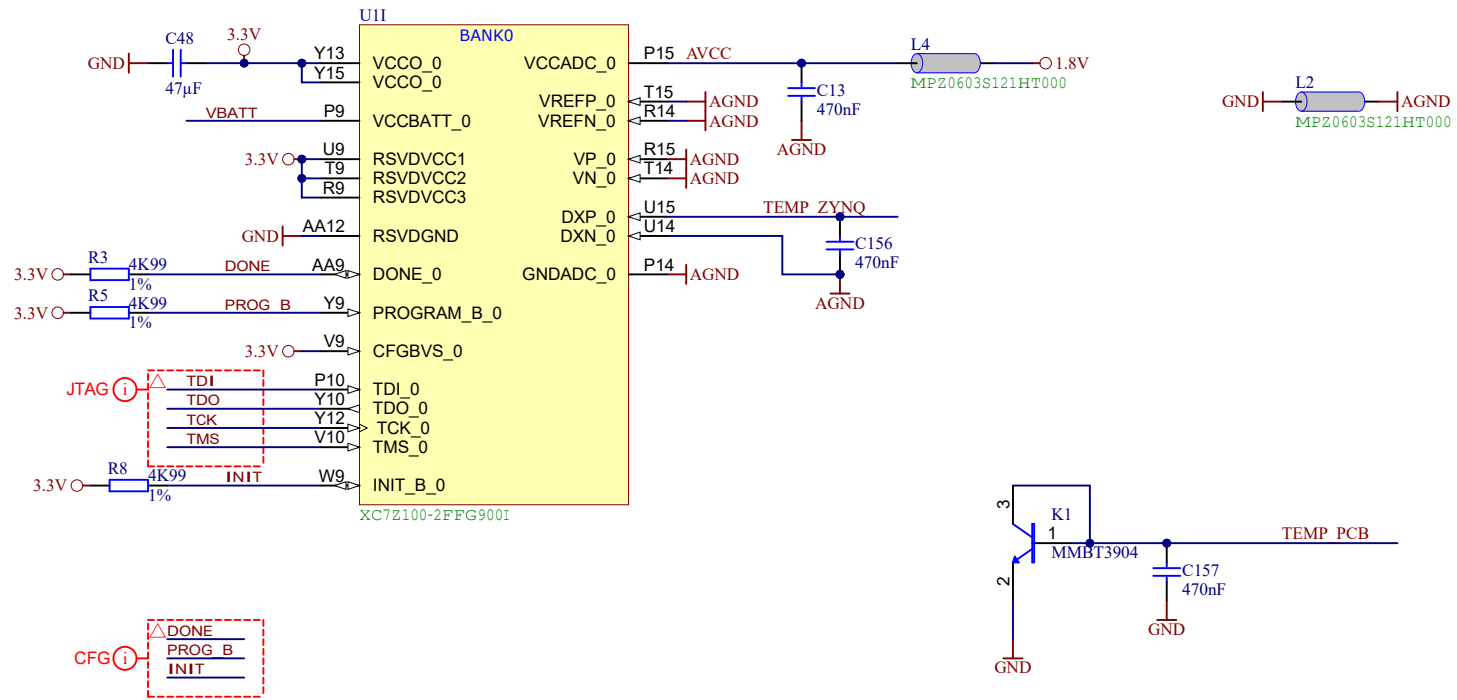
1


2

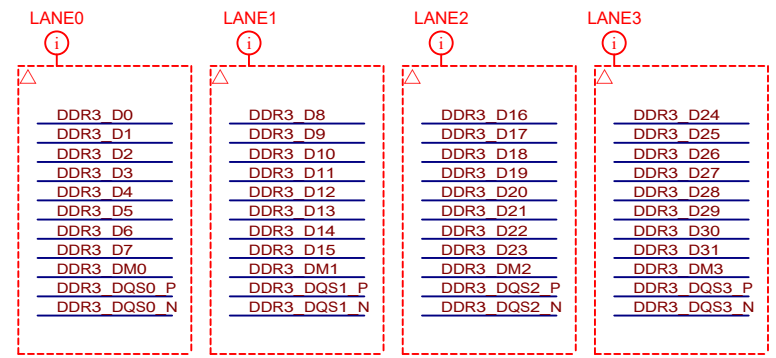
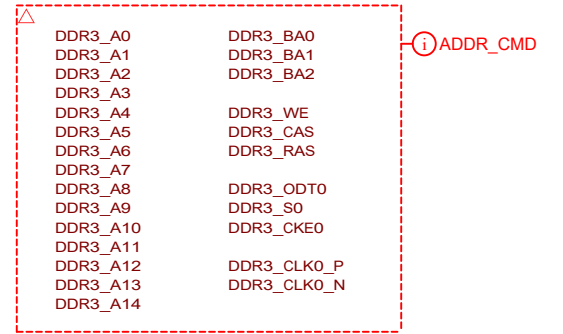
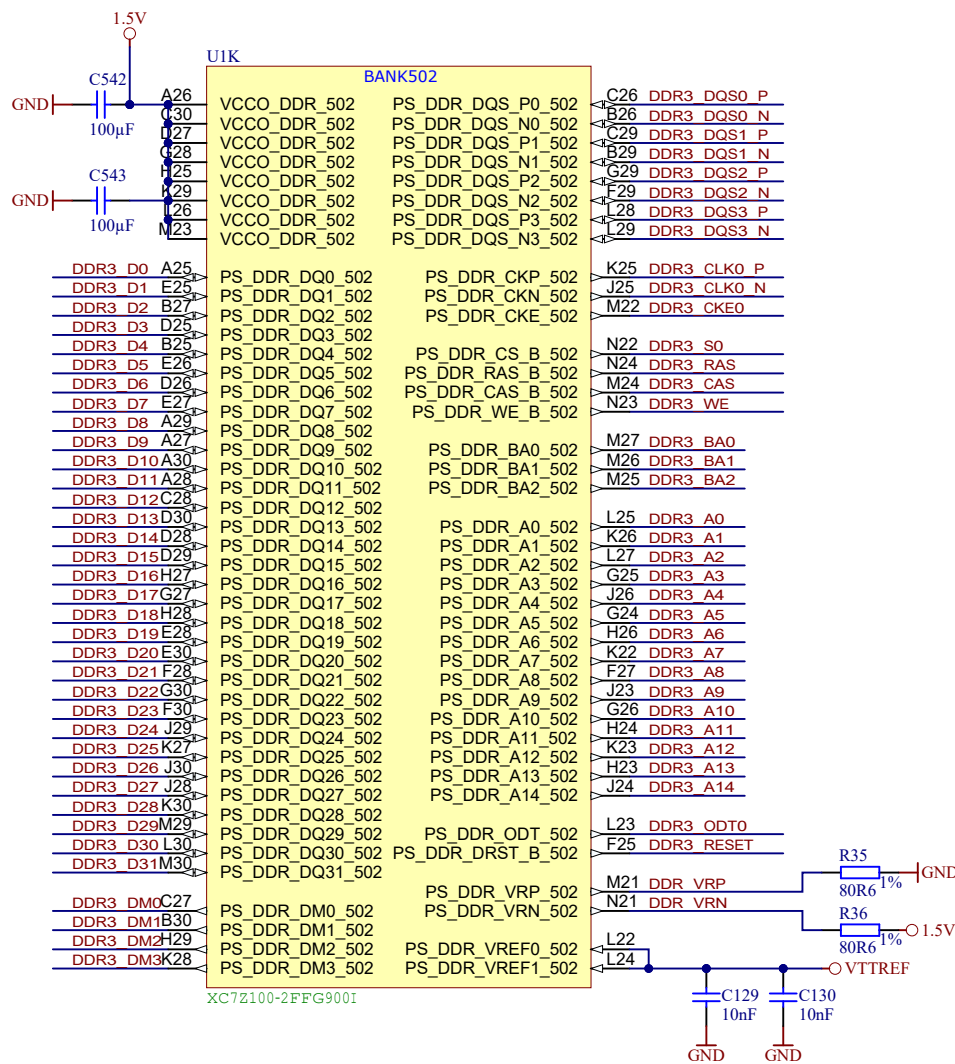
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4

		Title: TE0784 - SOC	
		A4	Number: TE0784 A2I33MA
Date: 25.06.2018		Copyright: Trenz Electronic GmbH	
Filename: SOC.SchDoc		Page6 of 30	



		Title: TE0784 - FPGA Configuration	
		A4	Nummer: TE0784 A2I33MA
Datum: 25.06.2018		Zeichner: Trenz Electronic GmbH	
Filename: FPGA-CFG.SchDoc		Blatt 7 von 30	



**trenz electronic**

Title: TE0784 - FPGA DDR Banks		
A4	Number: TE0784 A2133MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 8 of 30
Filename: PS-DDR.SchDoc		



A

B

C

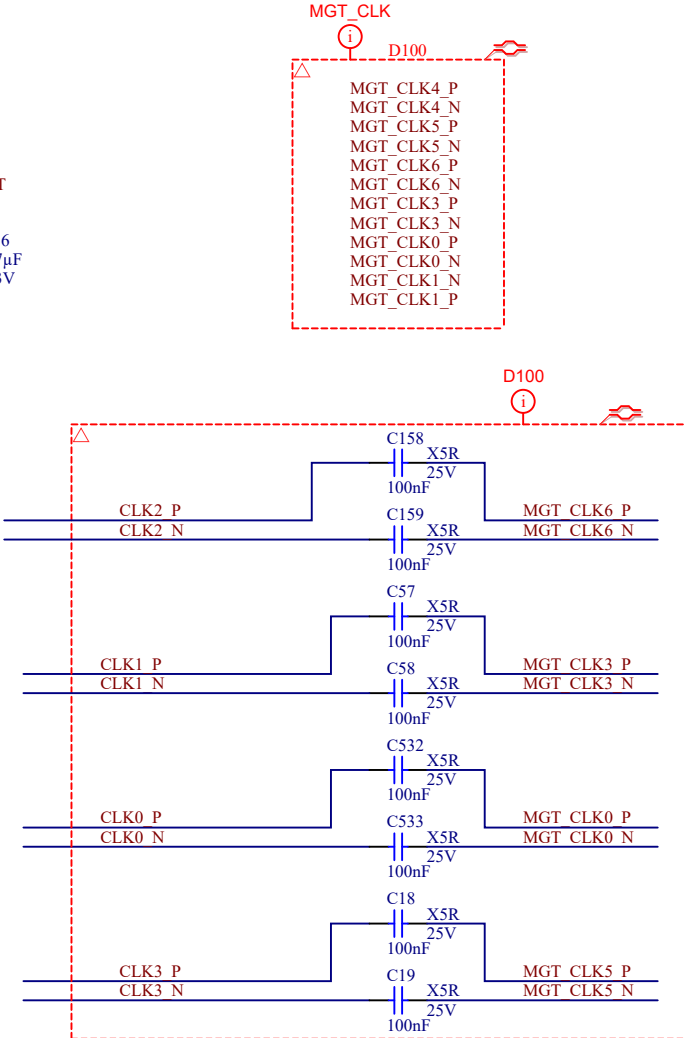
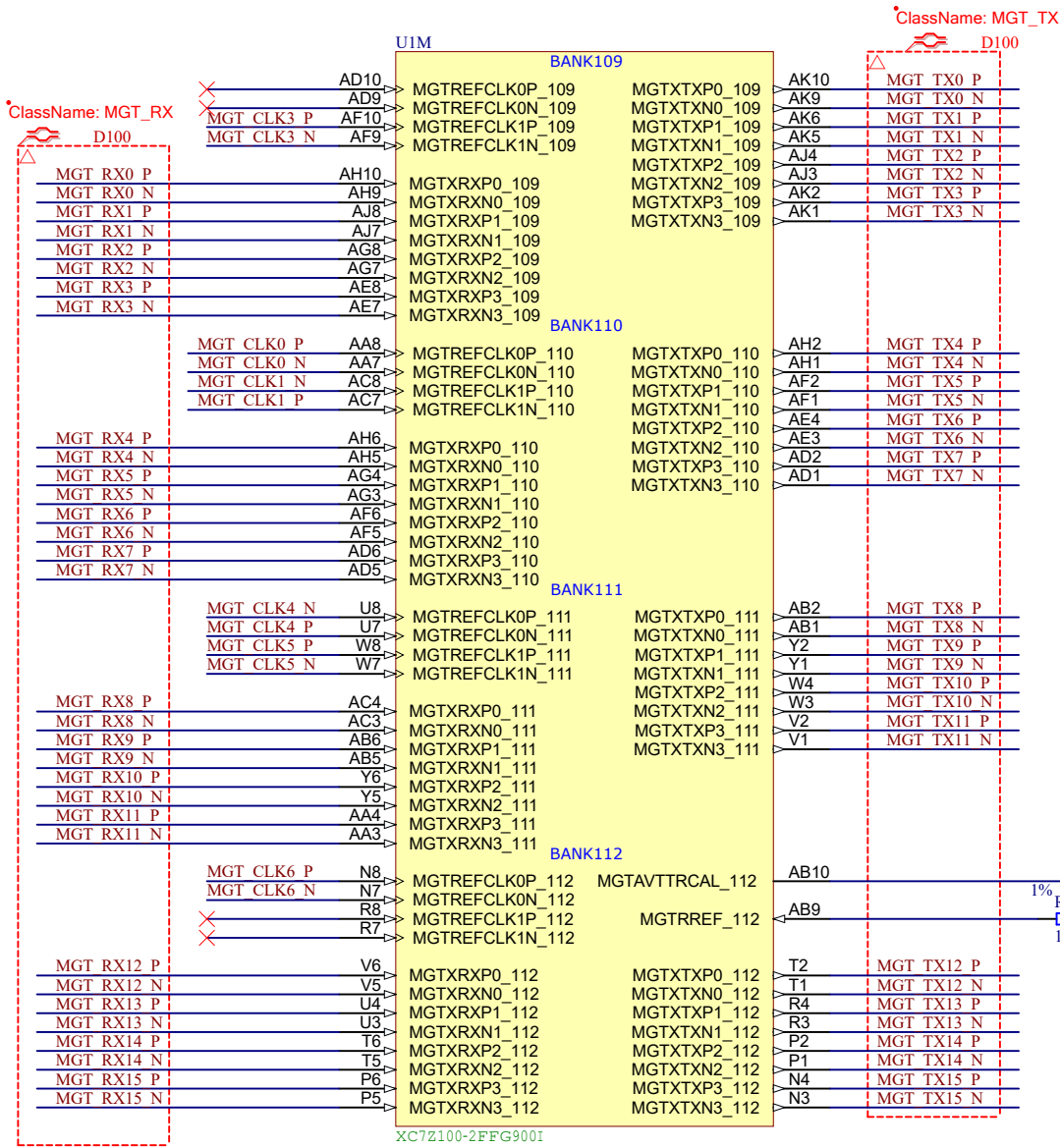
D

A

B

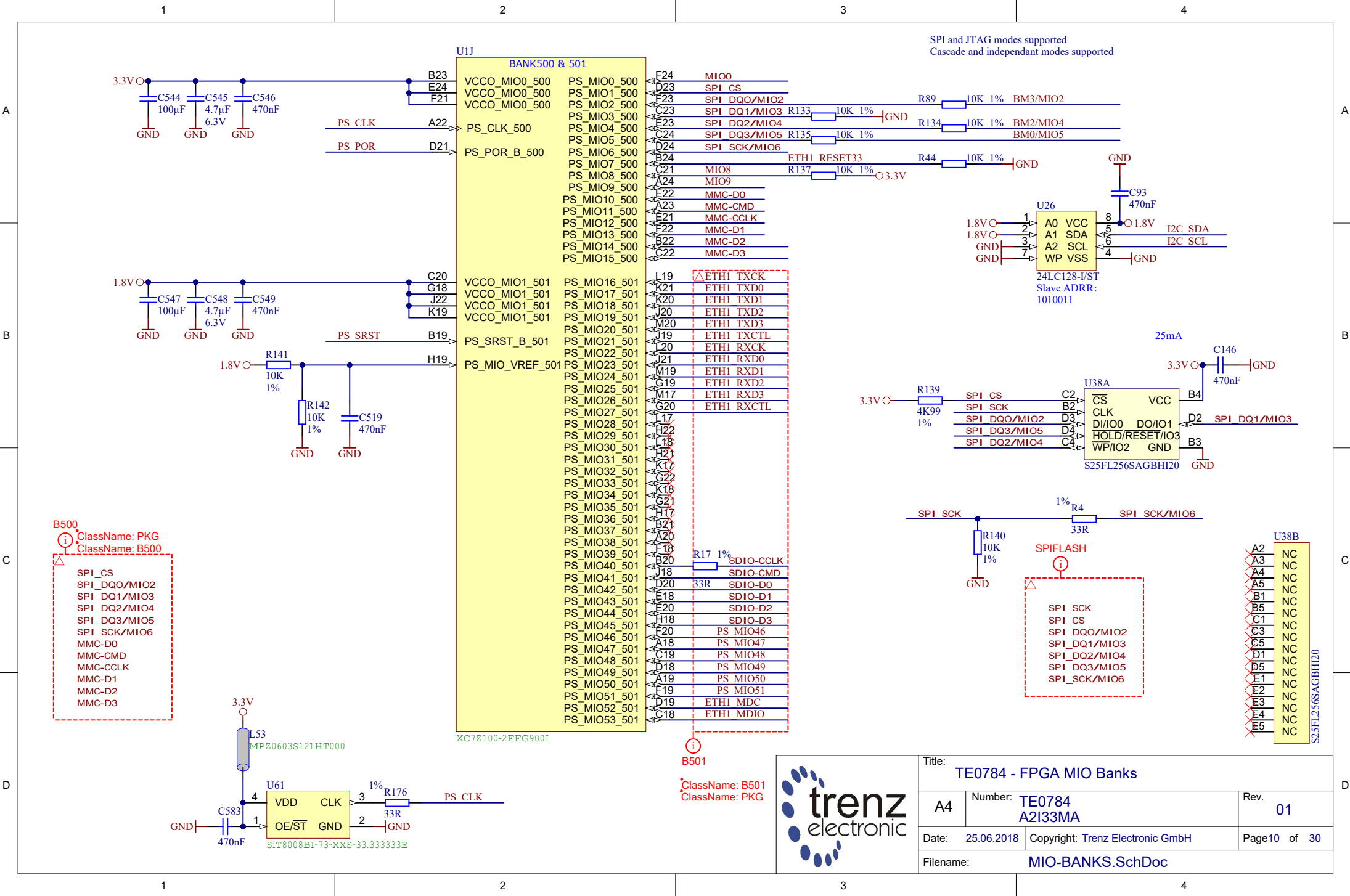
C

D

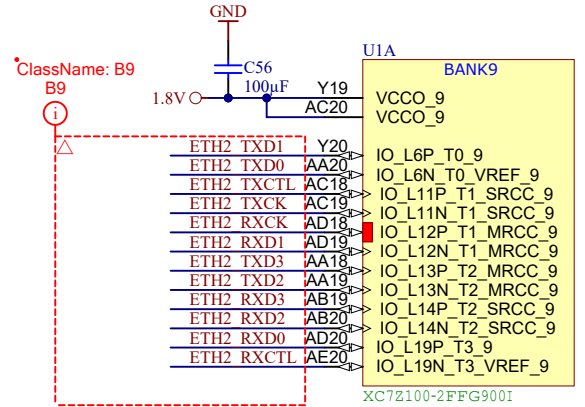


**trenz electronic**

Title: TE0784 - FPGA MGT		
A4	Number: TE0784 A2133MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page9 of 30
Filename: FPGA-MGT.SchDoc		




Title: TE0784 - FPGA MIO Banks		
A4	Number: TE0784 A2I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 10 of 30
Filename: MIO-BANKS.SchDoc		

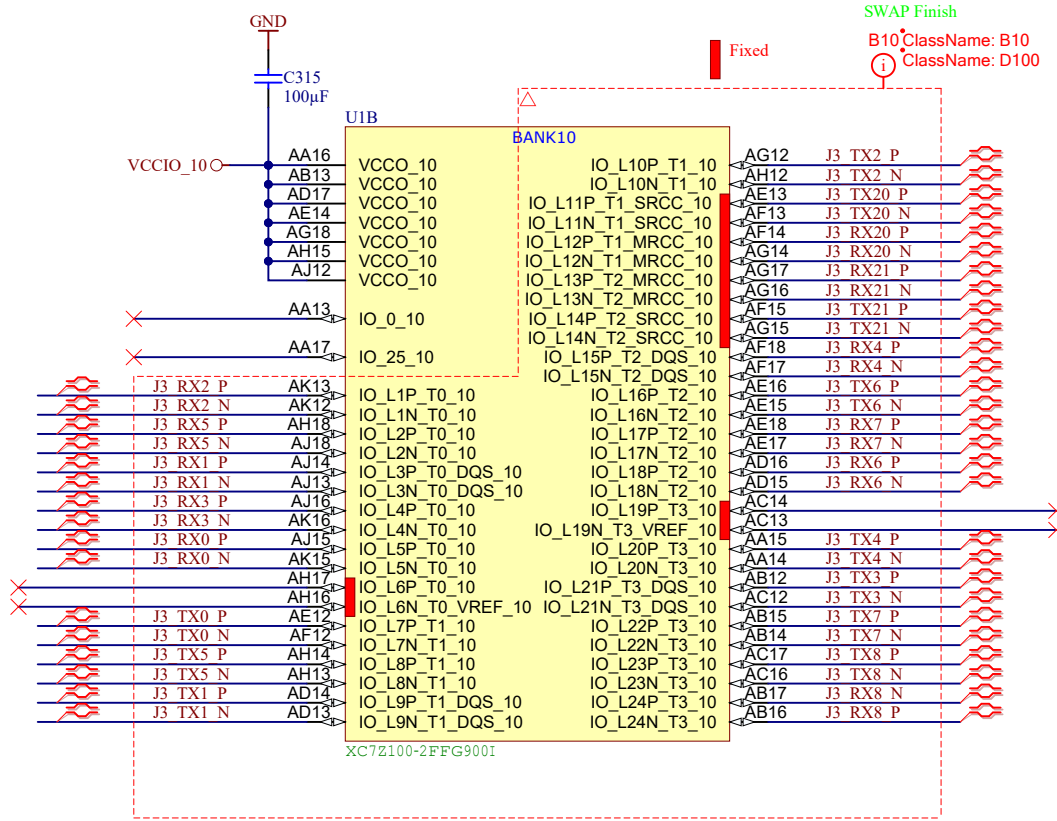


RXCK Fix to MRCCL

Fixed

	Title: TE0784 - FPGA B9		
	A4	Number: TE0784 A2I33MA	Rev. 01
	Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 11 of 30
	Filename: B9.SchDoc		

TP4  
 ●—○ VCCIO\_10  
 Testpoint 0.8mm



SWAP Finish  
 Fixed  
 B10 ClassName: B10  
 D100 ClassName: D100

XC7Z100-2FFG9001



Title: TE0784 - FPGA B10		
A4	Number: TE0784 A2I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 12 of 30
Filename: B10.SchDoc		

A

A

B

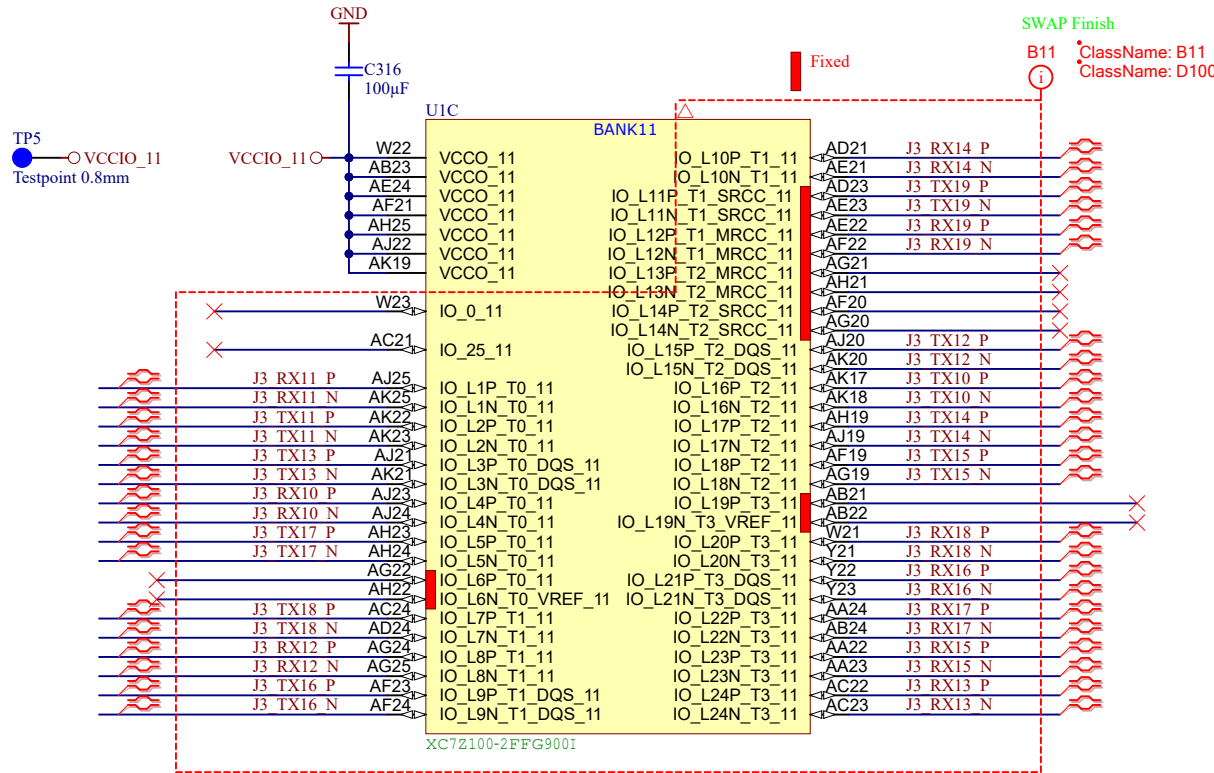
B


C


C

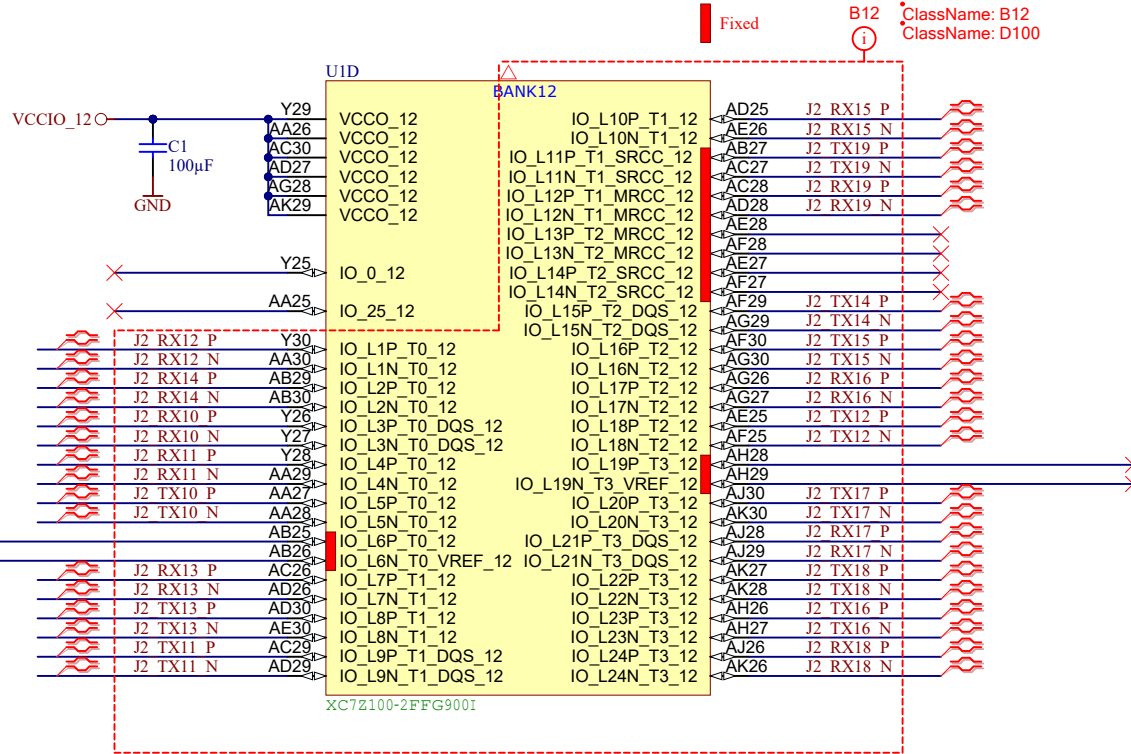
D


D



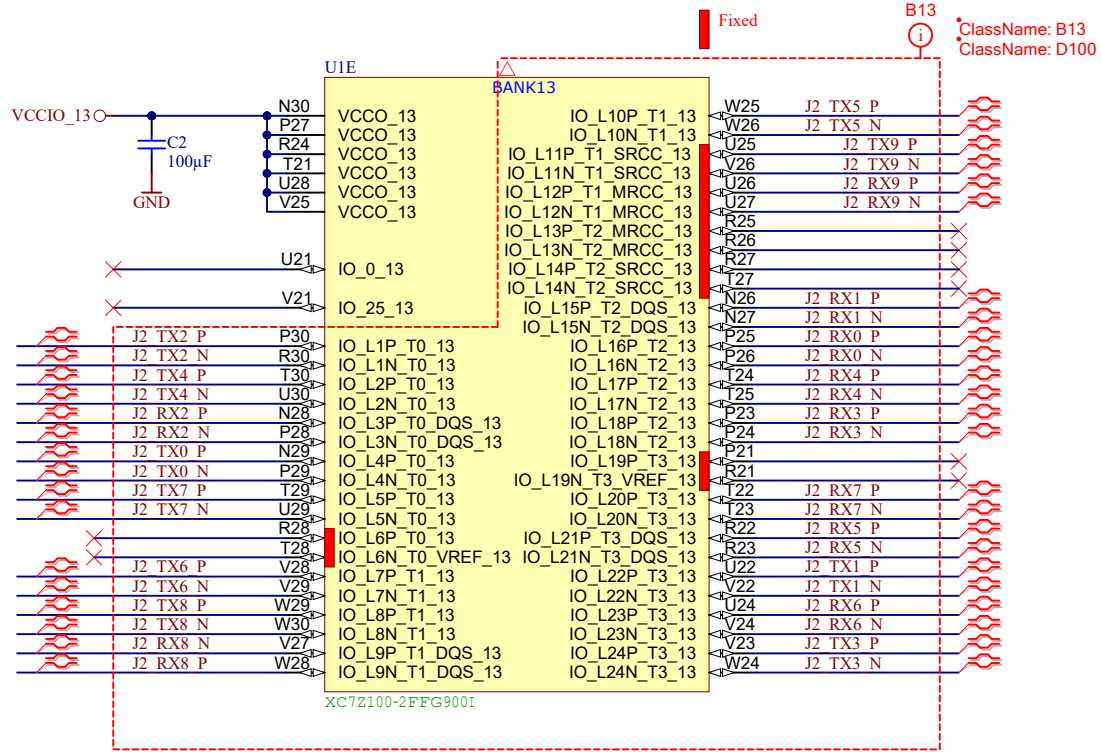
			Title: TE0784 - FPGA B11	
			A4	Number: TE0784 A2I33MA
Date: 25.06.2018		Copyright: Trenz Electronic GmbH		Page 13 of 30
Filename: B11.SchDoc				

TP1  
 VCCIO\_12  
 Testpoint 0.8mm



	Title: <b>TE0784 - FPGA B12</b>		
	A4	Number: <b>TE0784 A2I33MA</b>	Rev. <b>01</b>
	Date: <b>25.06.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>14</b> of <b>30</b>
	Filename: <b>B12.SchDoc</b>		

TP2  
 ● ○ VCCIO\_13  
 Testpoint 0.8mm



Title: TE0784 - FPGA B13		
A4	Number: TE0784 A2I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 15 of 30
Filename: B13.SchDoc		

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U\_B33  
B33.SchDoc



U\_B34  
B34.SchDoc



U\_B35  
B35.SchDoc



A

A

B

B

C

C

D

D



Title: TE0784 - FPGA HP Banks		
A4	Number: TE0784 A2I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 16 of 30
Filename: HP-BANKS.SchDoc		


1

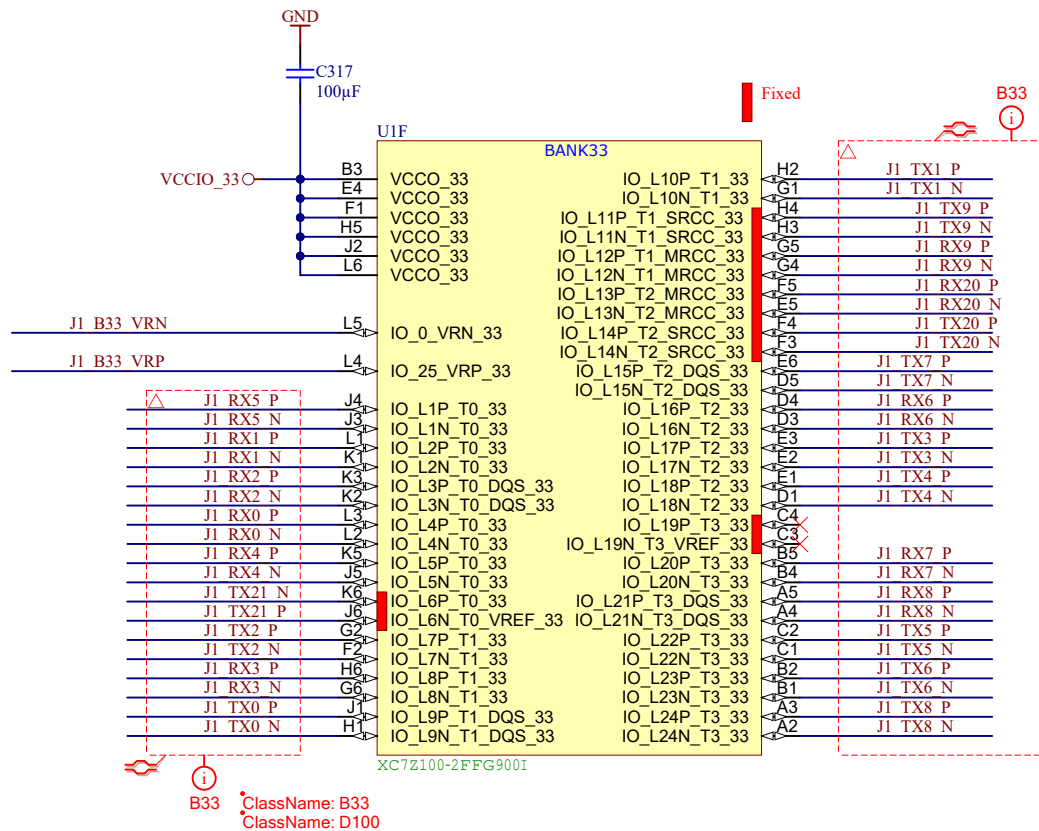
2

3

4




TP6  
 VCCIO\_33  
 Testpoint 0.8mm

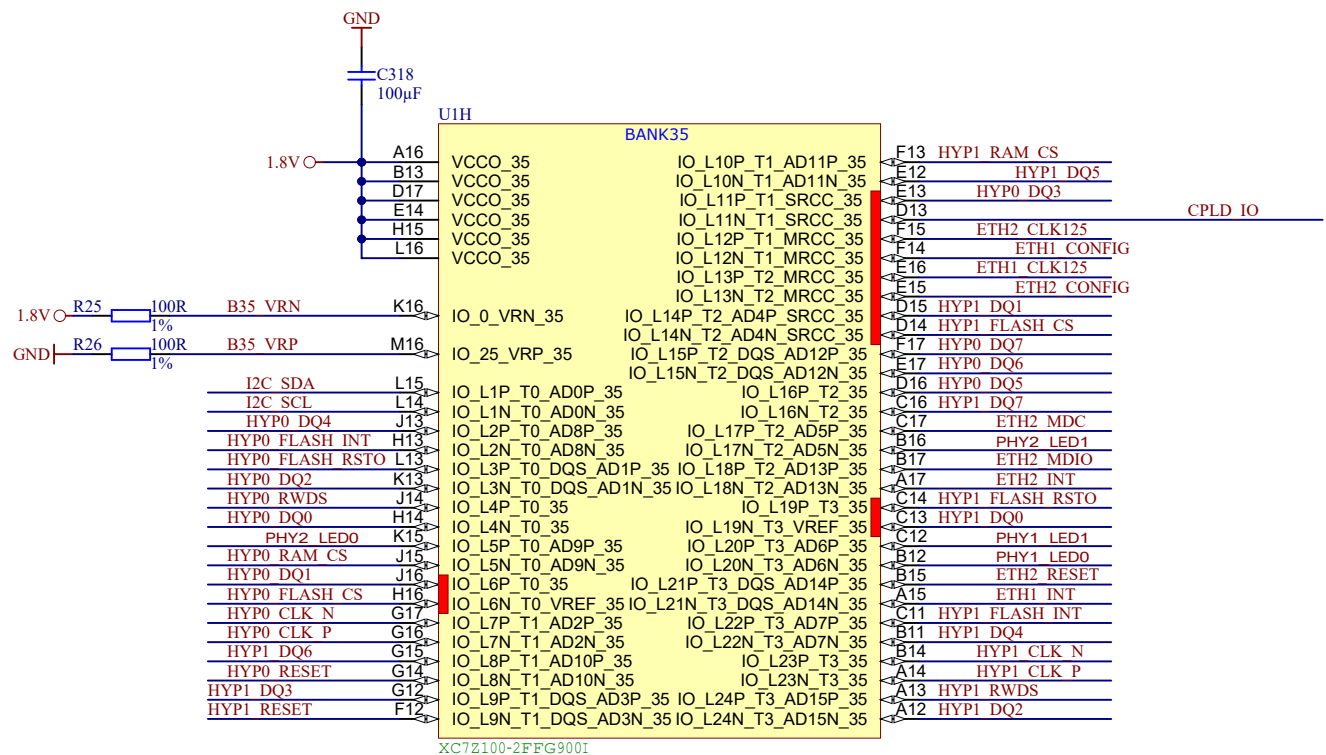


B33  
 ClassName: B33  
 ClassName: D100

B33  
 ClassName: B33  
 ClassName: D100

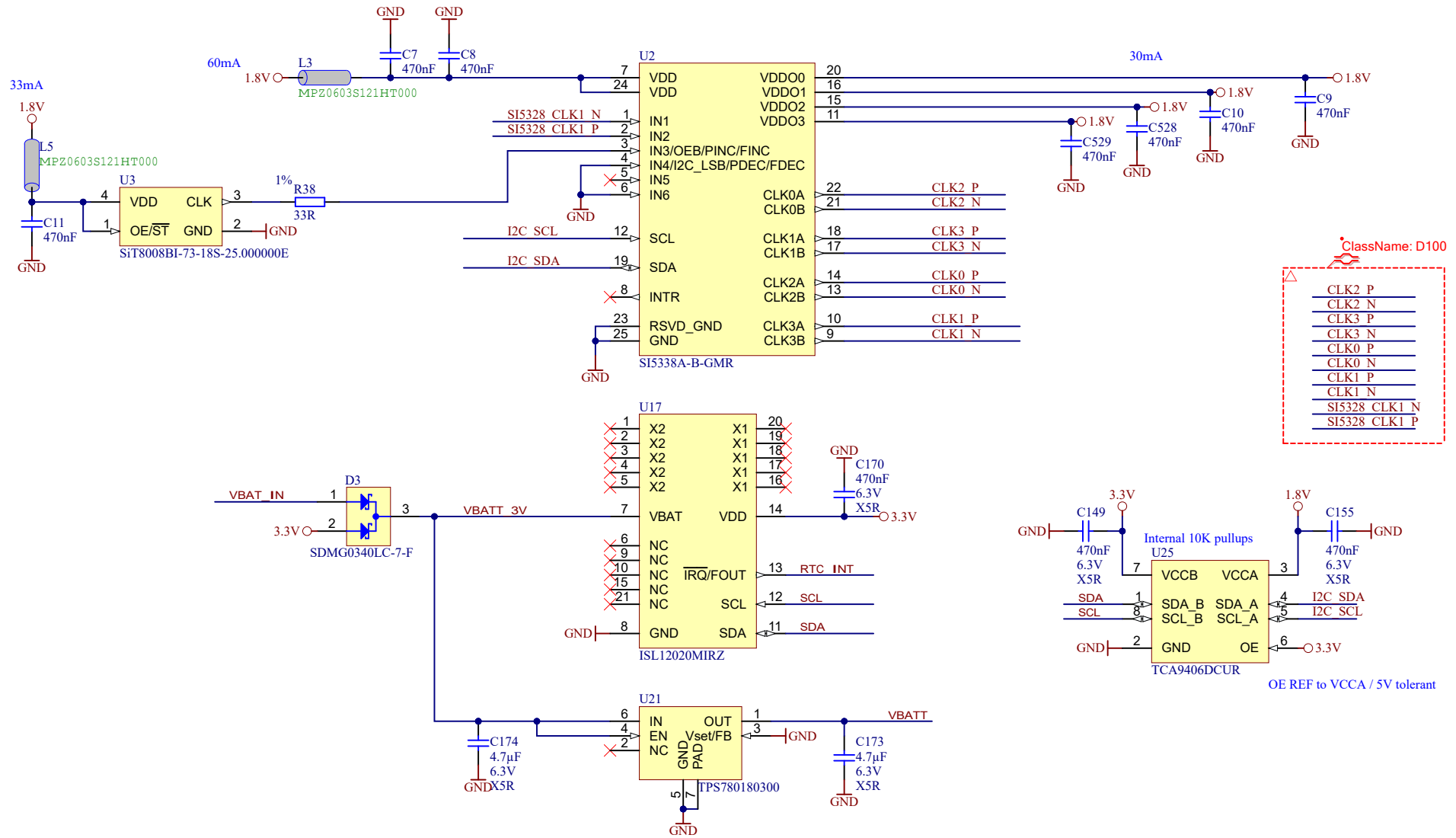
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	A4	Number: TE0784 A2I33MA	Rev. 01
	Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 17 of 30
	Filename: B33.SchDoc		





Title: TE0784 - FPGA B35		
A4	Number: TE0784 A2I33MA	Rev. 01
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Filename: B35.SchDoc		



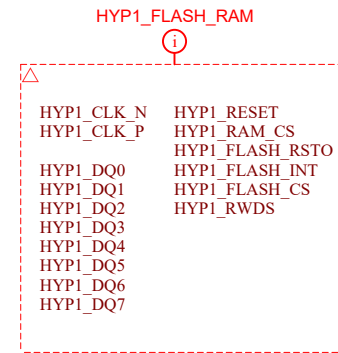
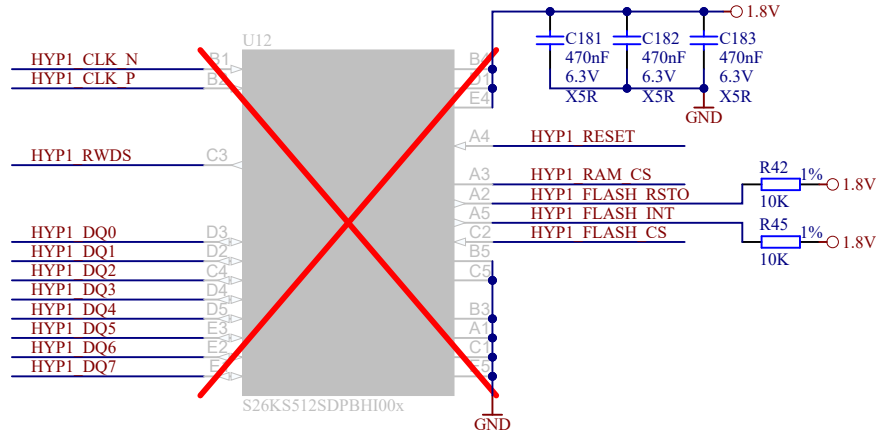
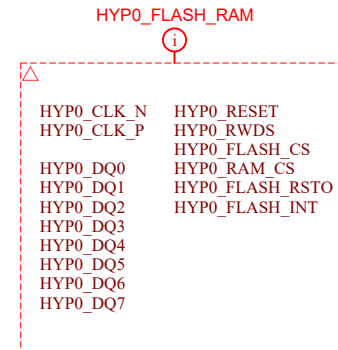
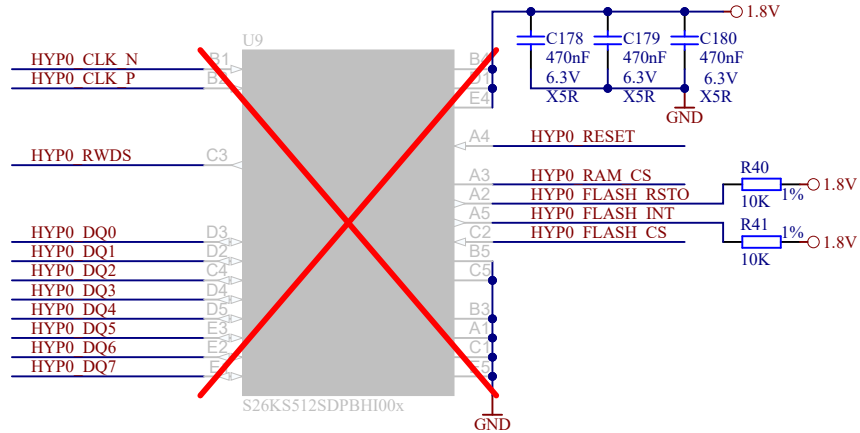
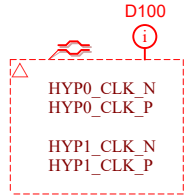



- ClassName: D100
- CLK2 P
  - CLK2 N
  - CLK3 P
  - CLK3 N
  - CLK0 P
  - CLK0 N
  - CLK1 P
  - CLK1 N
  - SI5328 CLK1 N
  - SI5328 CLK1 P

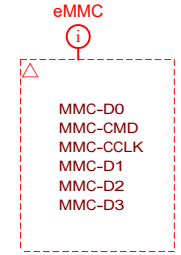
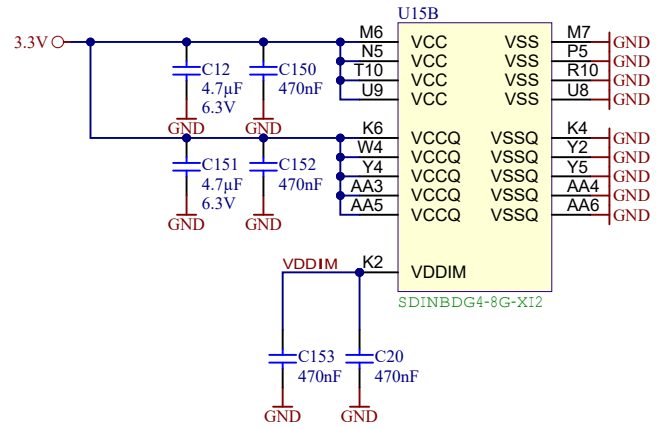
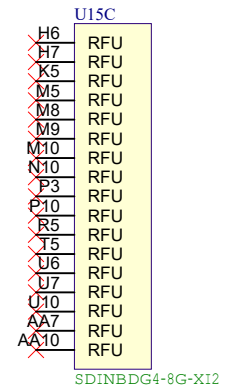
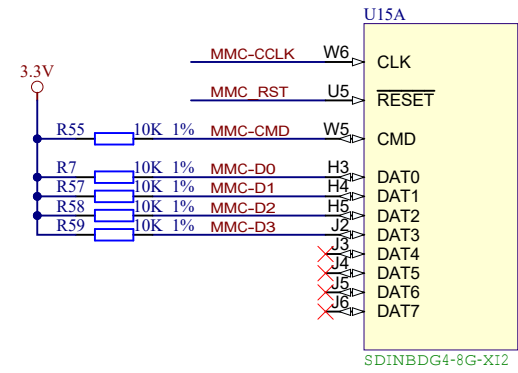
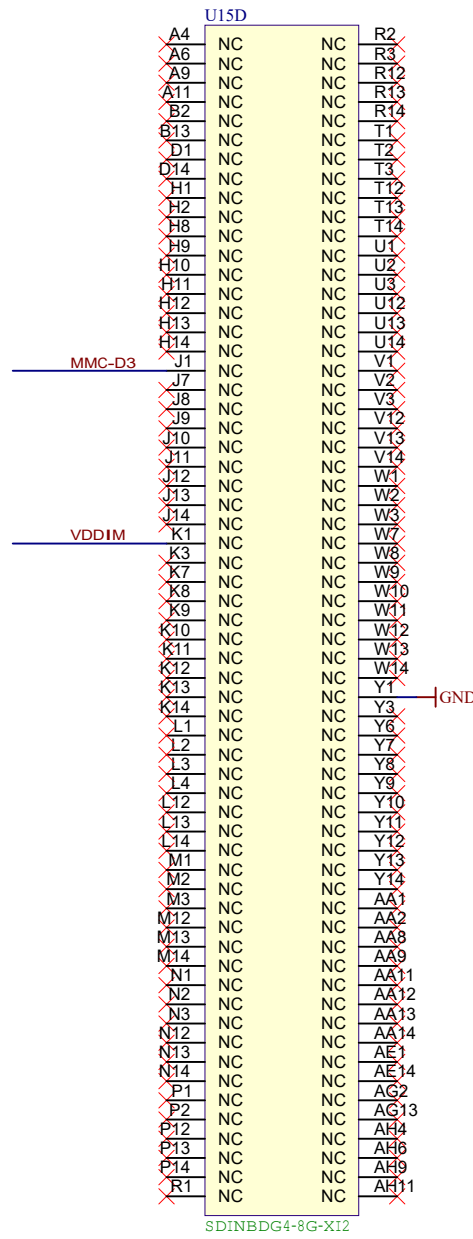


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A4	Number: TE0784 A2133MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 21 of 30
Filename: Clock.SchDoc		



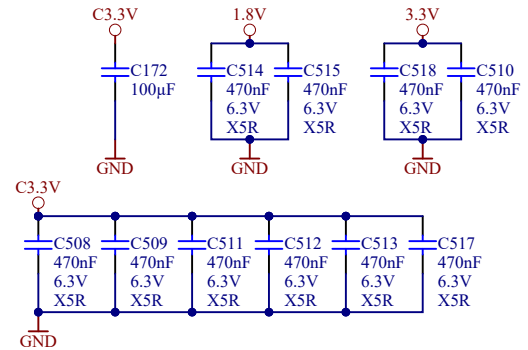
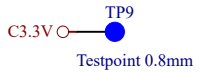
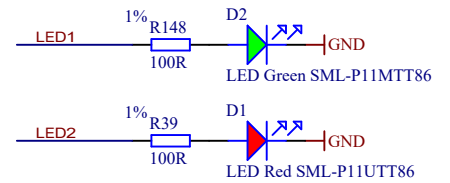
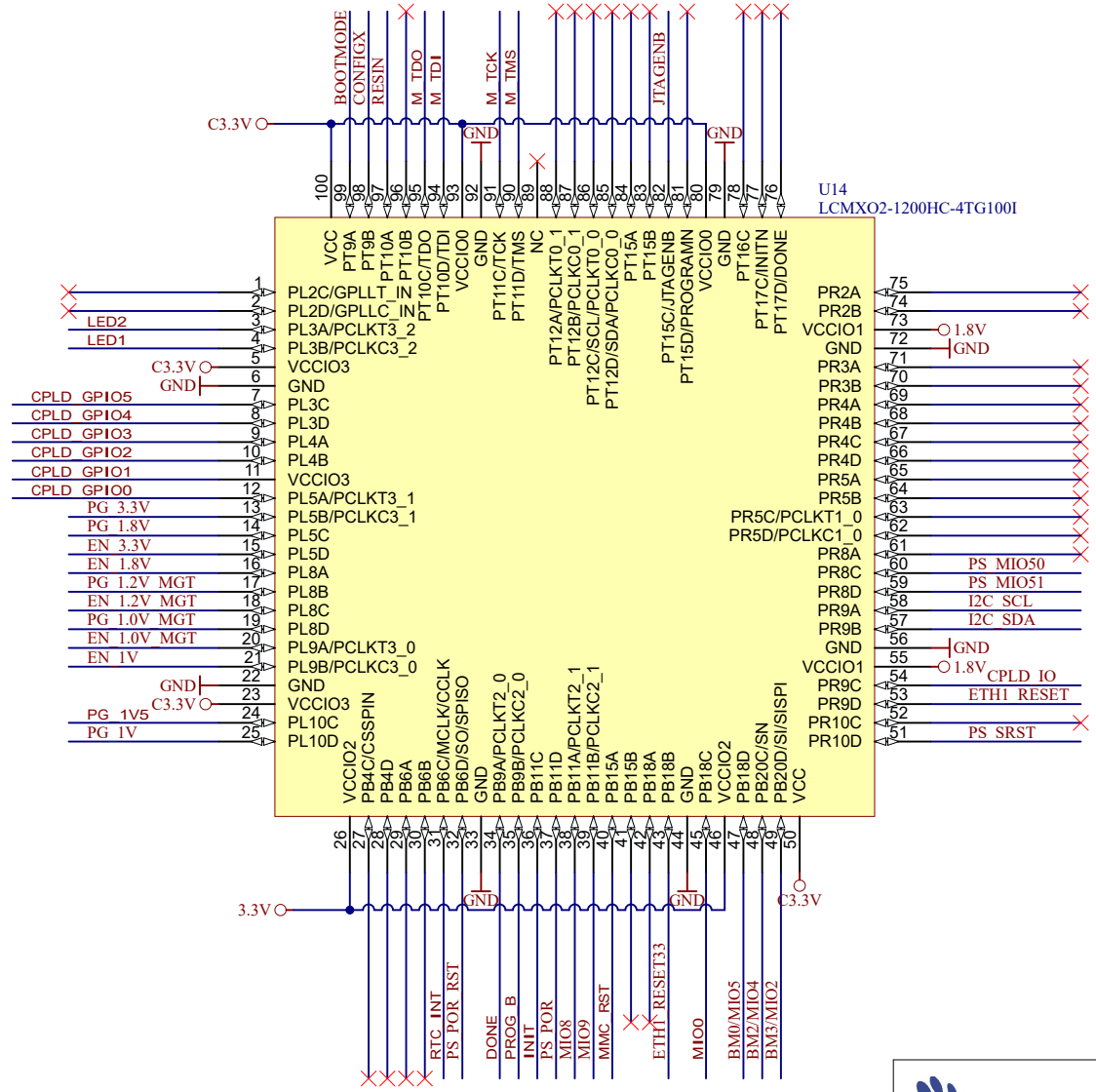



Title: TE0784 - HyperFlash_RAM		
A4	Number: TE0784 A2I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 23 of 30
Filename: HyperFlash_RAM.SchDoc		



Title: TE0784 - eMMC		
A4	Number: TE0784 A2I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page24 of 30
Filename: eMMC.SchDoc		





Title: <b>TE0784 - CPLD</b>		
A4	Number: <b>TE0784 A2133MA</b>	Rev. <b>01</b>
Date: <b>25.06.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>25</b> of <b>30</b>
Filename: <b>CPLD.SchDoc</b>		

1

2

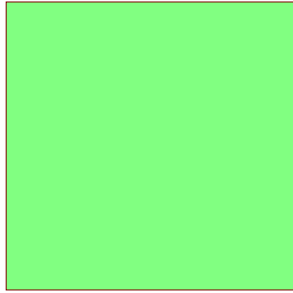
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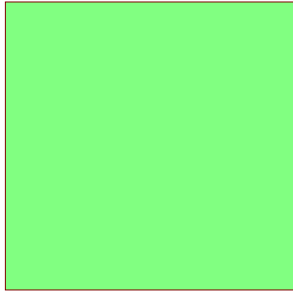
A

A

U\_ETH1  
ETH1.SchDoc



U\_ETH2  
ETH2.SchDoc



B

B

C

C

D

D



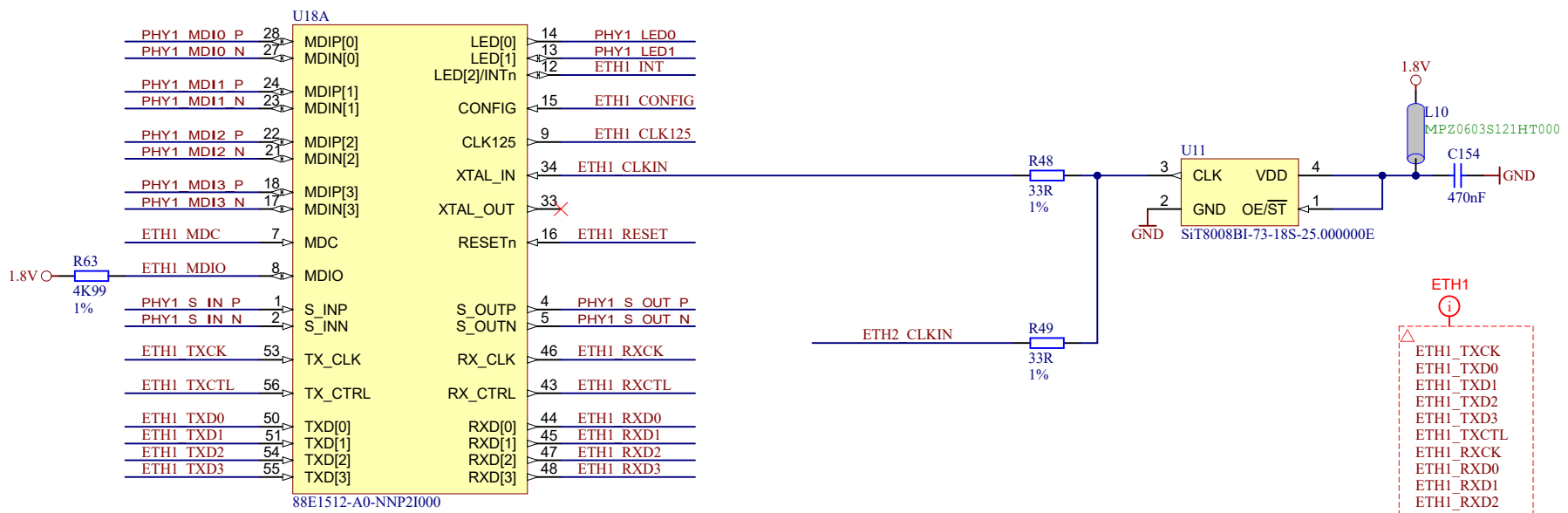
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A4	Number: <b>TE0784 A2I33MA</b>	Rev. <b>01</b>
Date: <b>25.06.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>26</b> of <b>30</b>
Filename: <b>Ethernet.SchDoc</b>		

1

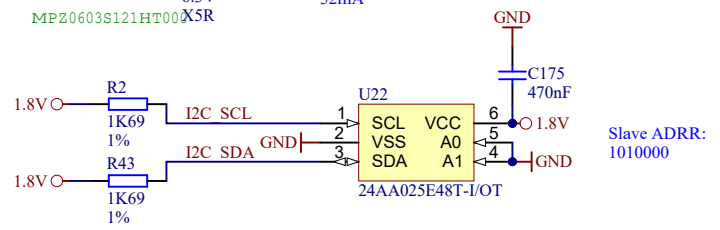
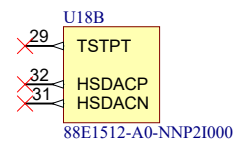
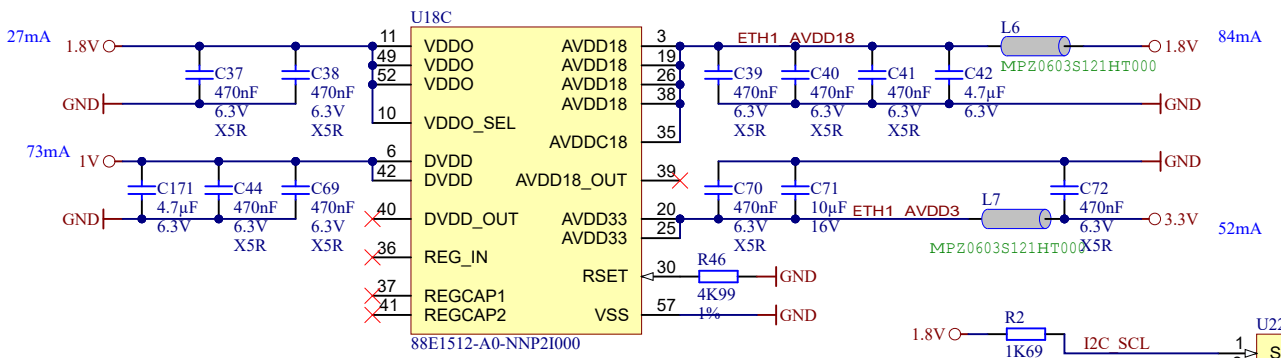
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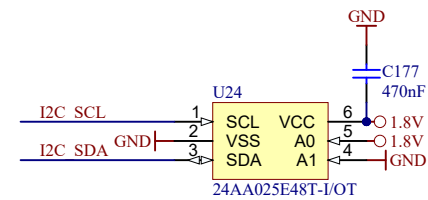
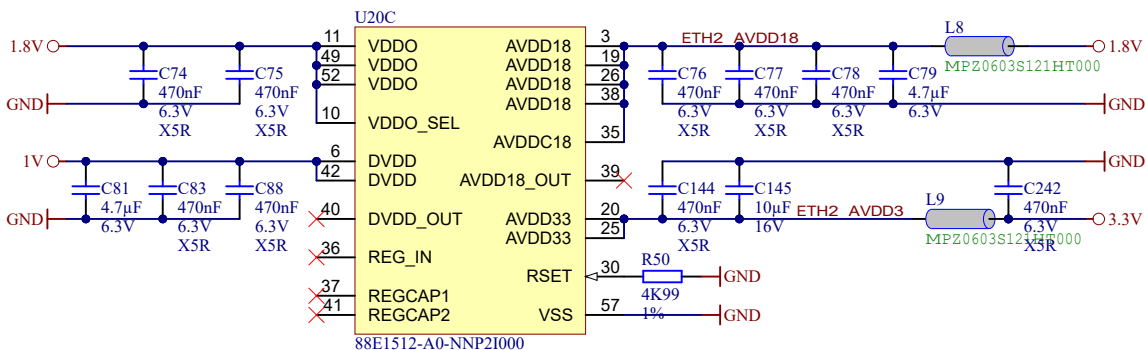
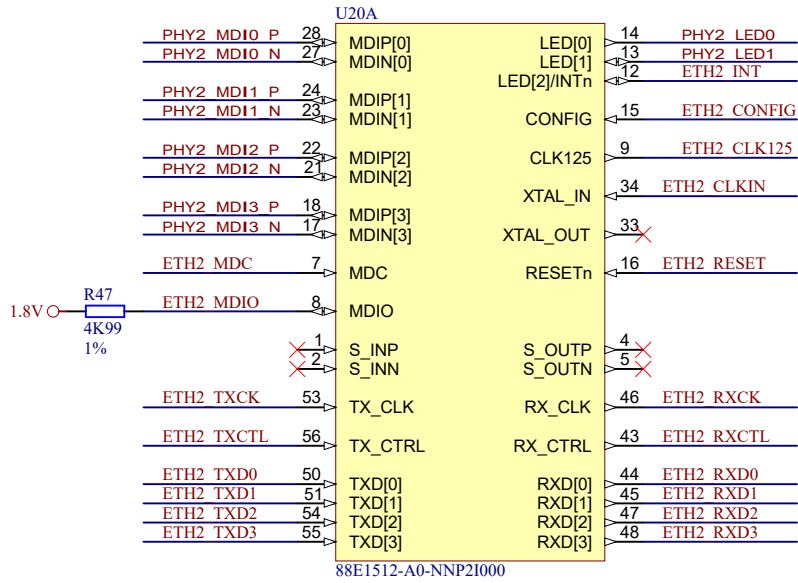
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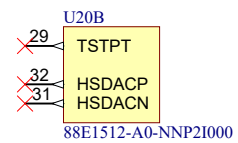
- ETH1**
- ETH1\_TXCK
  - ETH1\_TXD0
  - ETH1\_TXD1
  - ETH1\_TXD2
  - ETH1\_TXD3
  - ETH1\_TXCTL
  - ETH1\_RXCK
  - ETH1\_RXD0
  - ETH1\_RXD1
  - ETH1\_RXD2
  - ETH1\_RXD3
  - ETH1\_RXCTL
  - ETH1\_MDC
  - ETH1\_MDIO
- PHY1\_LED0  
PHY1\_LED1  
ETH1\_INT  
ETH1\_CONFIG  
ETH1\_CLK125  
ETH1\_RESET



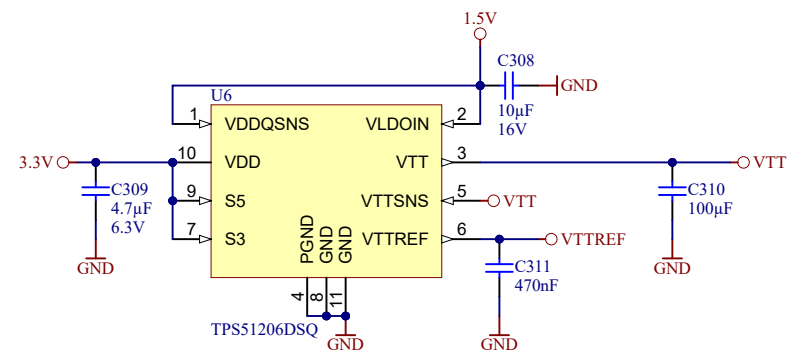
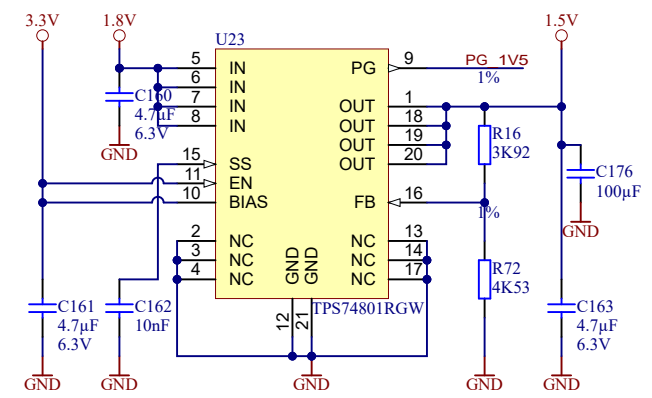
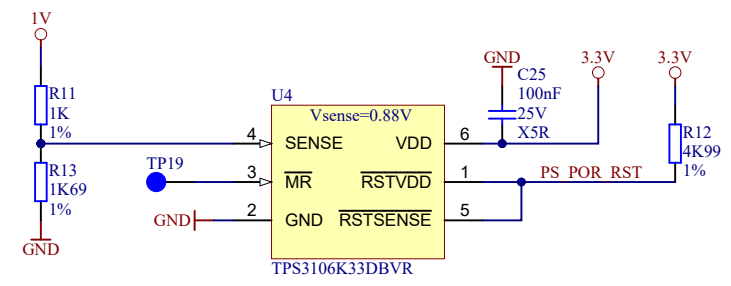
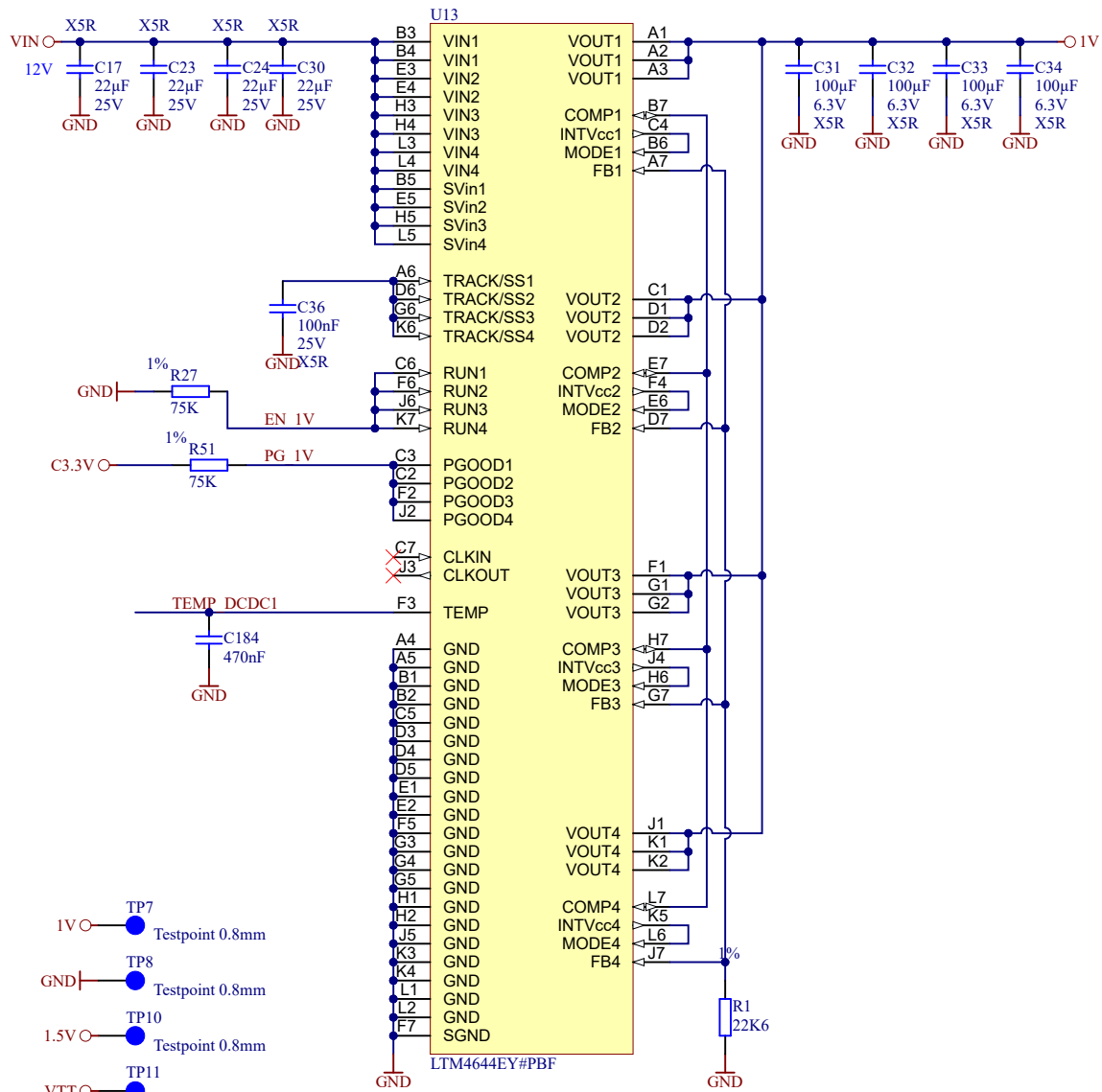
Title: TE0784 - ETH_PHY1		
A4	Number: TE0784 A2I33MA	Rev. 01
Date: 25.06.2018	Copyright: Trenz Electronic GmbH	Page 27 of 30
Filename: ETH1.SchDoc		




Slave ADDR:  
1010001

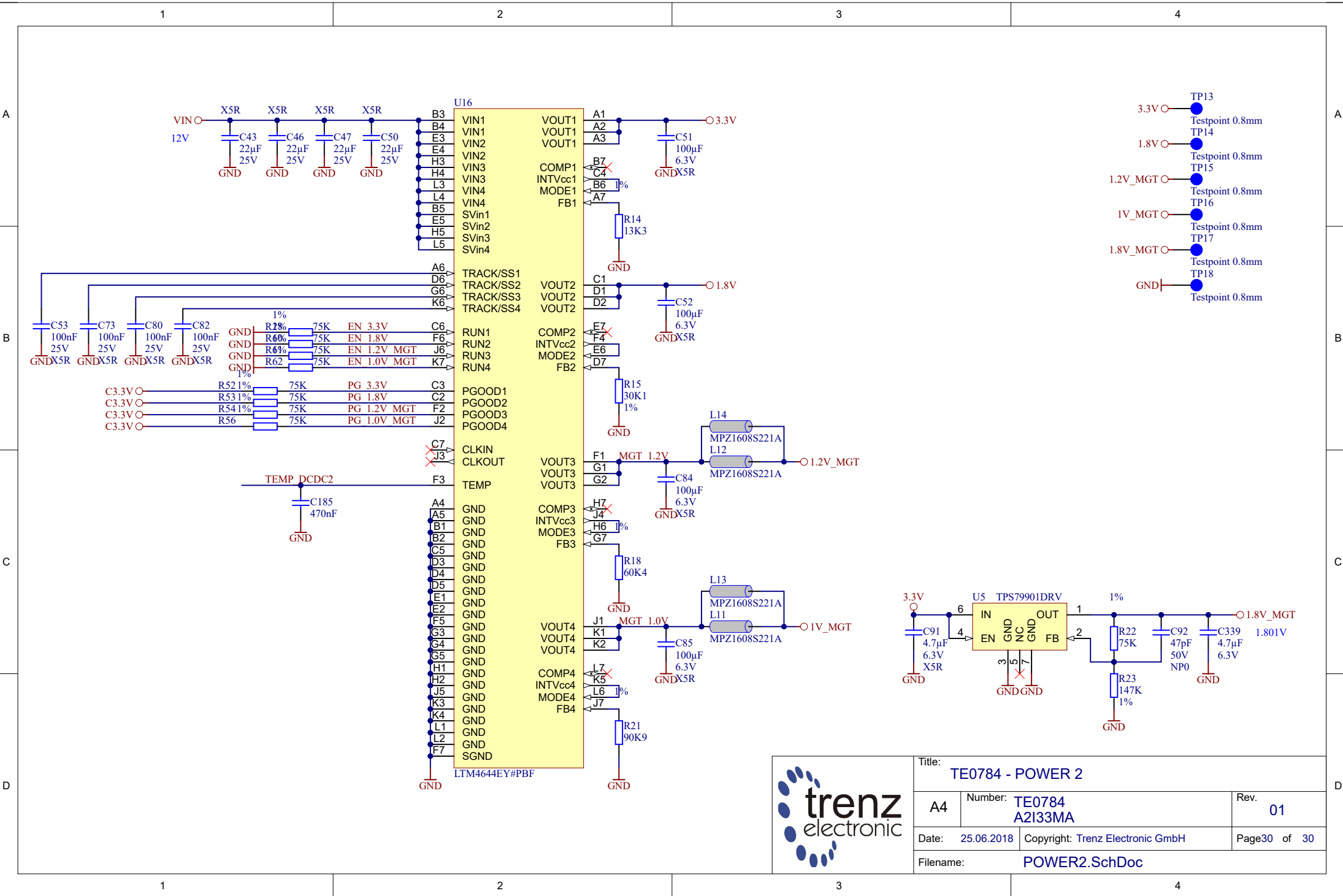


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	A4	Number: <b>TE0784 A2I33MA</b>	Rev. <b>01</b>
	Date: <b>25.06.2018</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>28</b> of <b>30</b>
	Filename: <b>ETH2.SchDoc</b>		



- IV ○ ● TP7 Testpoint 0.8mm
- GND ○ ● TP8 Testpoint 0.8mm
- 1.5V ○ ● TP10 Testpoint 0.8mm
- VTT ○ ● TP11 Testpoint 0.8mm
- VTTREF ○ ● TP12 Testpoint 0.8mm

			Title: TE0784 - POWER	
			A4	Number: TE0784 A2I33MA
Date: 25.06.2018		Copyright: Trenz Electronic GmbH		Page 29 of 30
Filename: POWER.SchDoc				



- 3.3V ○ TP13 Testpoint 0.8mm
- 1.8V ○ TP14 Testpoint 0.8mm
- 1.2V\_MGT ○ TP15 Testpoint 0.8mm
- 1V\_MGT ○ TP16 Testpoint 0.8mm
- 1.8V\_MGT ○ TP17 Testpoint 0.8mm
- GND ○ TP18 Testpoint 0.8mm



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