U_Power
Power.SchDoc

U_FPGA_PWR
FPGA_PWR.SchDoc

U_DDR3_RAM
DDR3_RAM.SchDoc

U_FPGA_CFG_CLK
FPGA_CFG_CLK.SchDoc

U_FPGA_B3
FPGA_B3.SchDoc

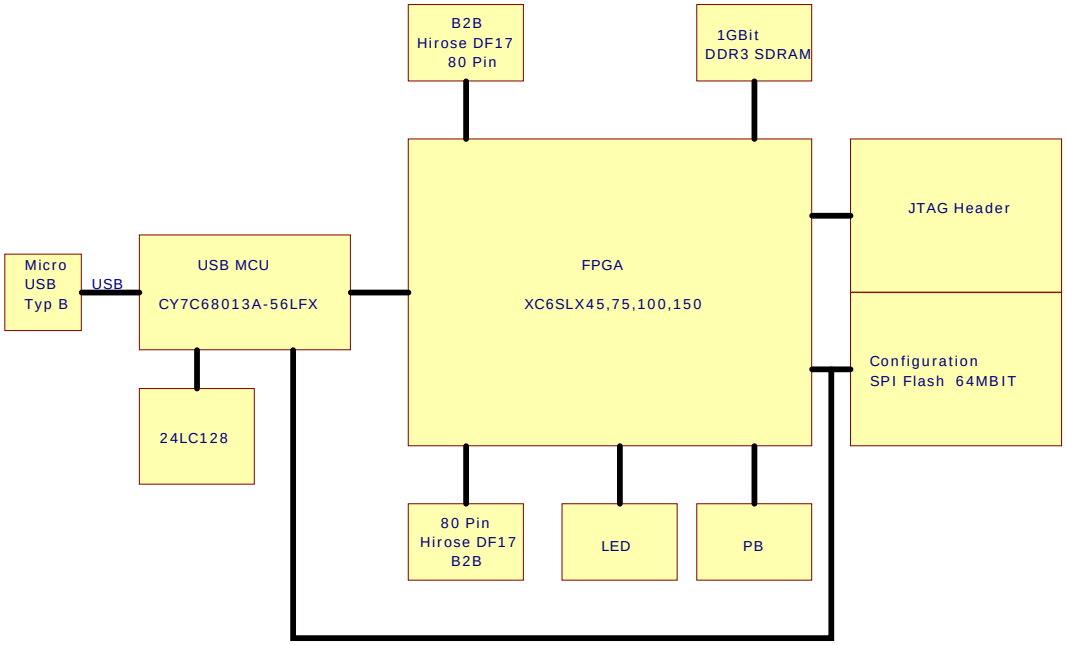
U_FPGA_DDR3
FPGA_DDR3.SchDoc

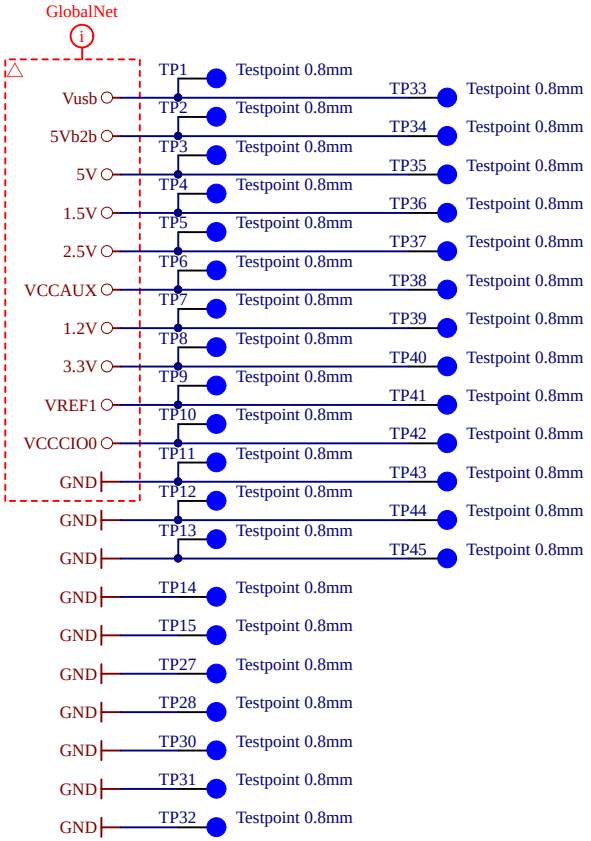
U_FPGA_B2
FPGA_B2.SchDoc

U_FPGA_B0
FPGA_B0.SchDoc

U_USB
USB.SchDoc

U_B2B_Connectors
B2B_Connectors.SchDoc

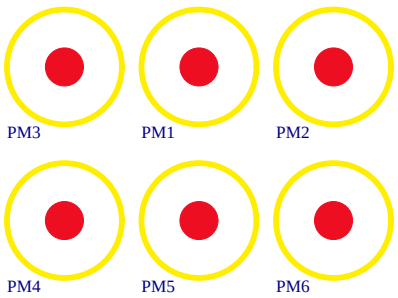


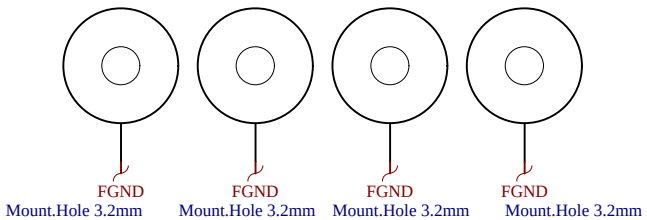


Serial
Serial
Serialnumber 6,3 x 6.3mm

S/N1
1
0R
2
Serialnumber

LOGO1
TE Logo PRINT Layer
LOGO PRINT





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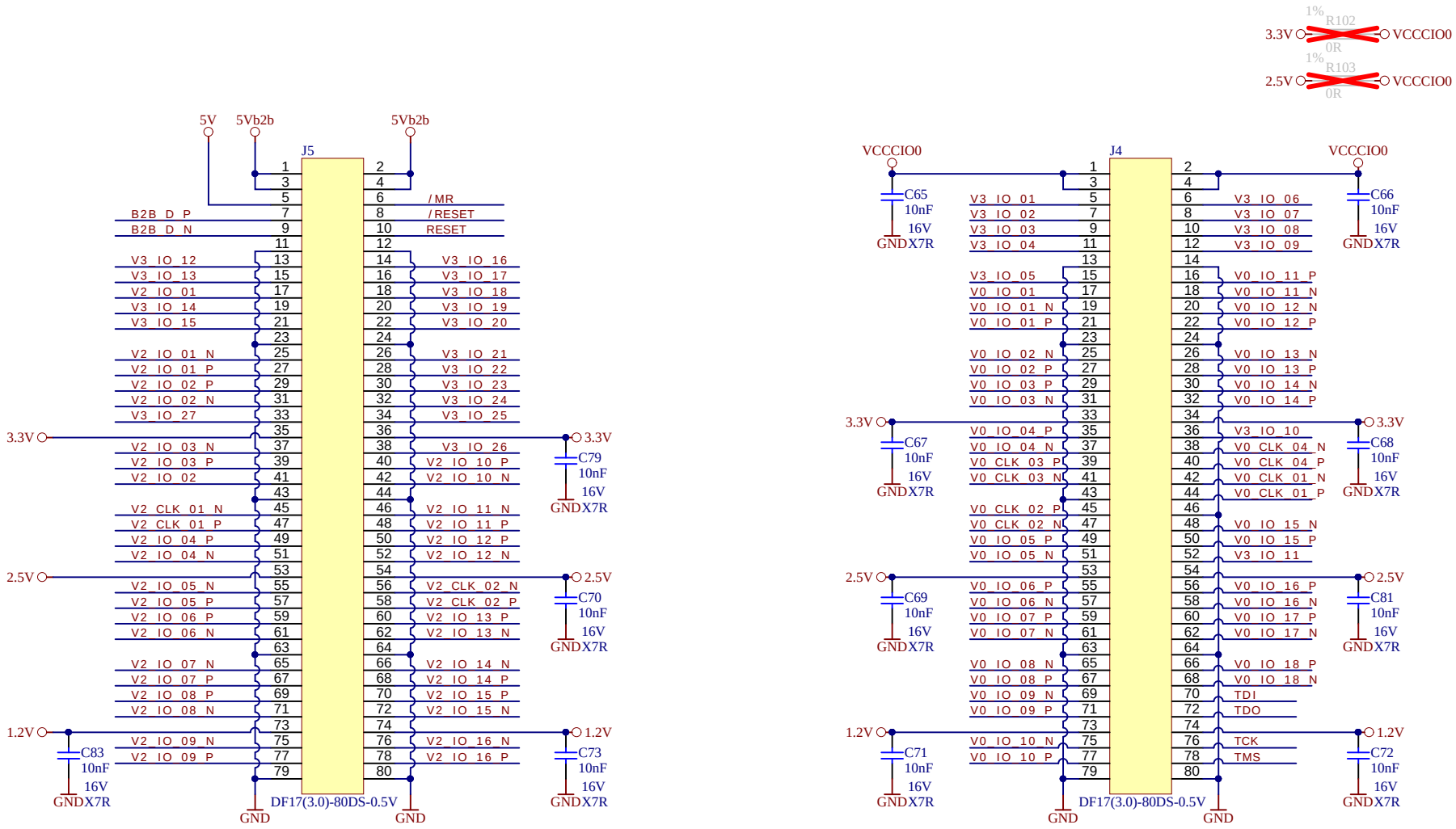
Title: TE0630		
A4	Number: TE0630 TE0630-02	Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page1 of 12
Filename: TE0630.SchDoc		



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Title: TE0630 - B2B_Connectors			
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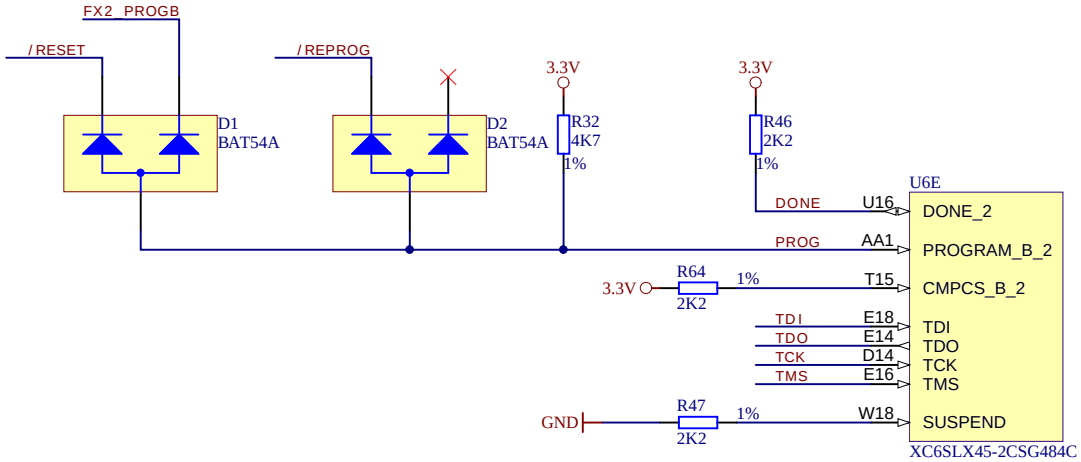
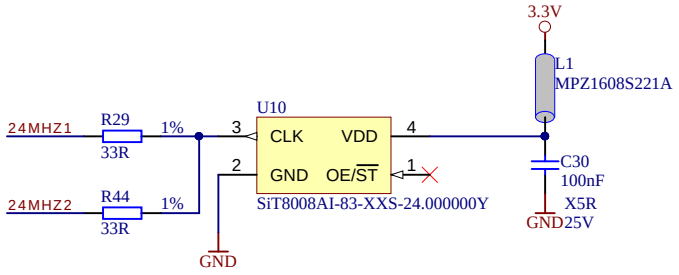
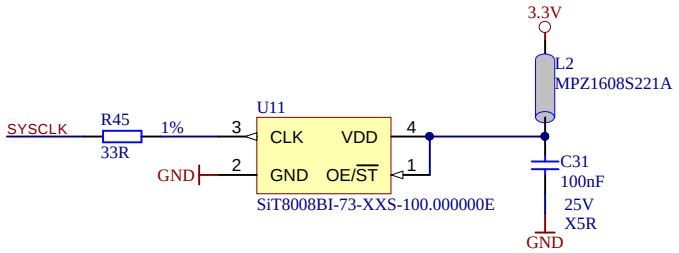
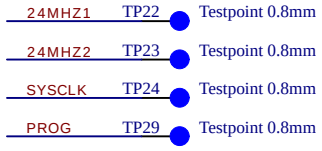
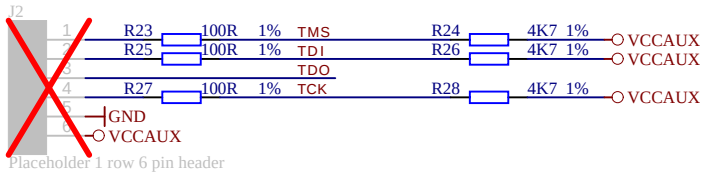
Date: 2018-11-28	Copyright: Trenz Electronic GmbH		Page2 of 12
Filename: B2B_Connectors.SchDoc			











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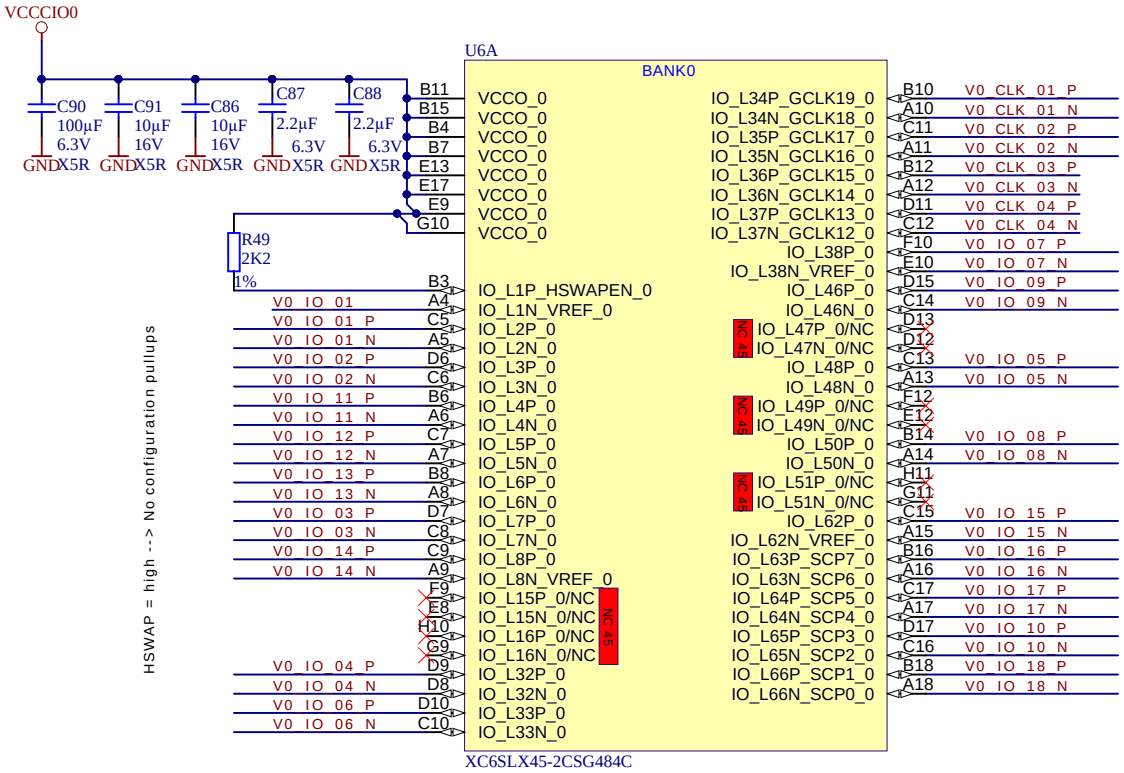
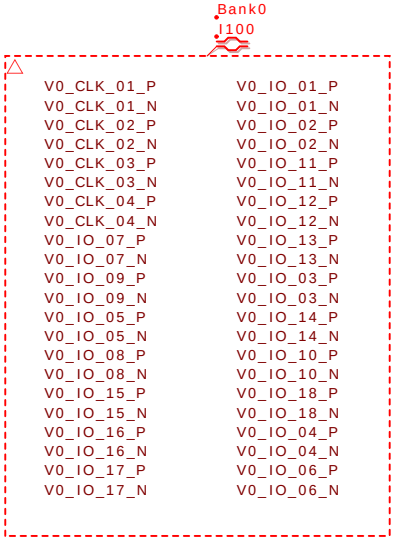
Title: TE0630 - FPGA_CFG_CLK		
A4	Number: TE0630 TE0630-02	Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page3 of 12
Filename: FPGA_CFG_CLK.SchDoc		





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Title: TE0630 - FPGA_B0			
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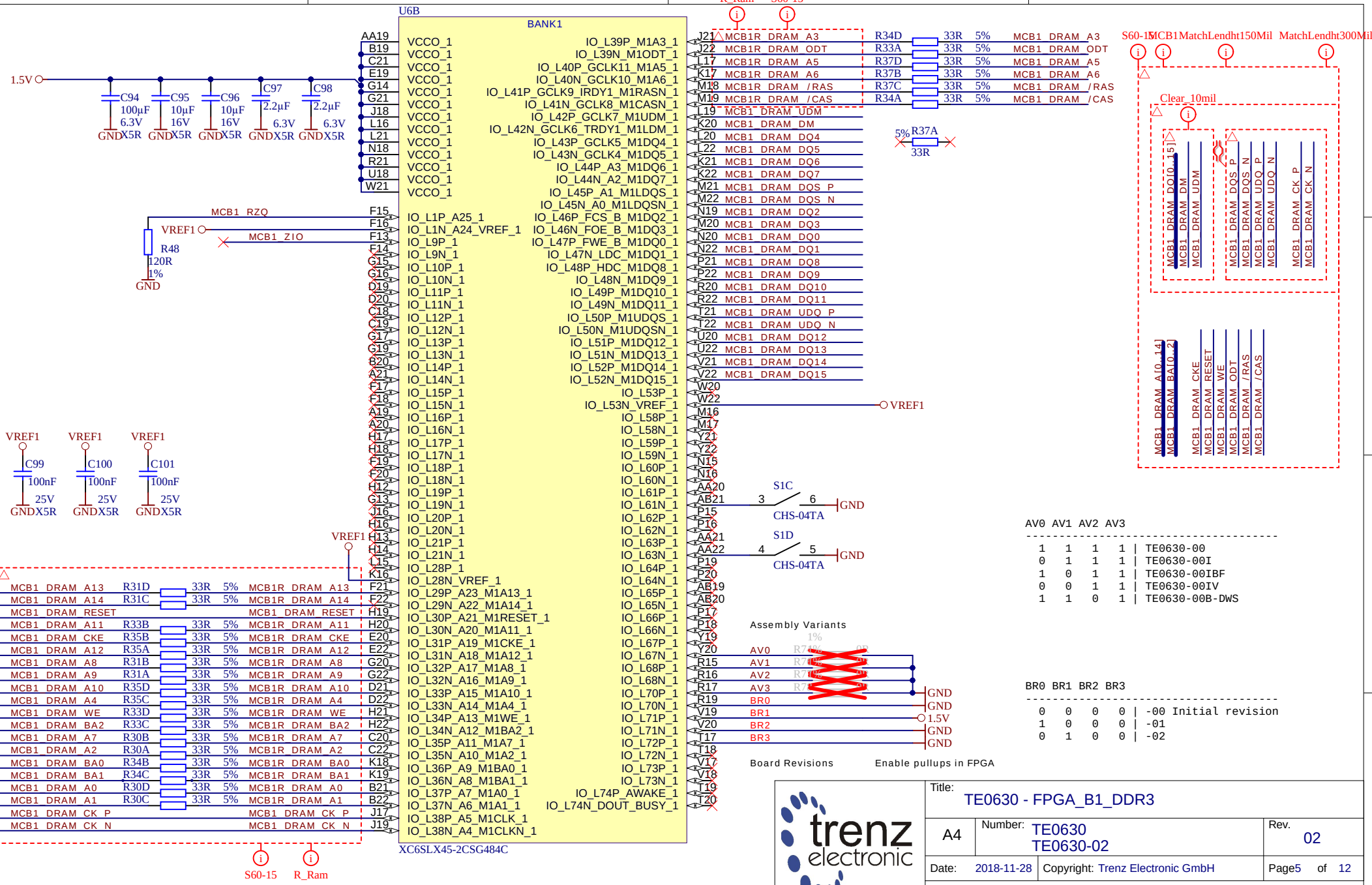
Date: 2018-11-28	Copyright: Trenz Electronic GmbH		Page4 of 12
Filename: FPGA_B0.SchDoc			



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Title: TE0630 - FPGA_B1_DDR3			
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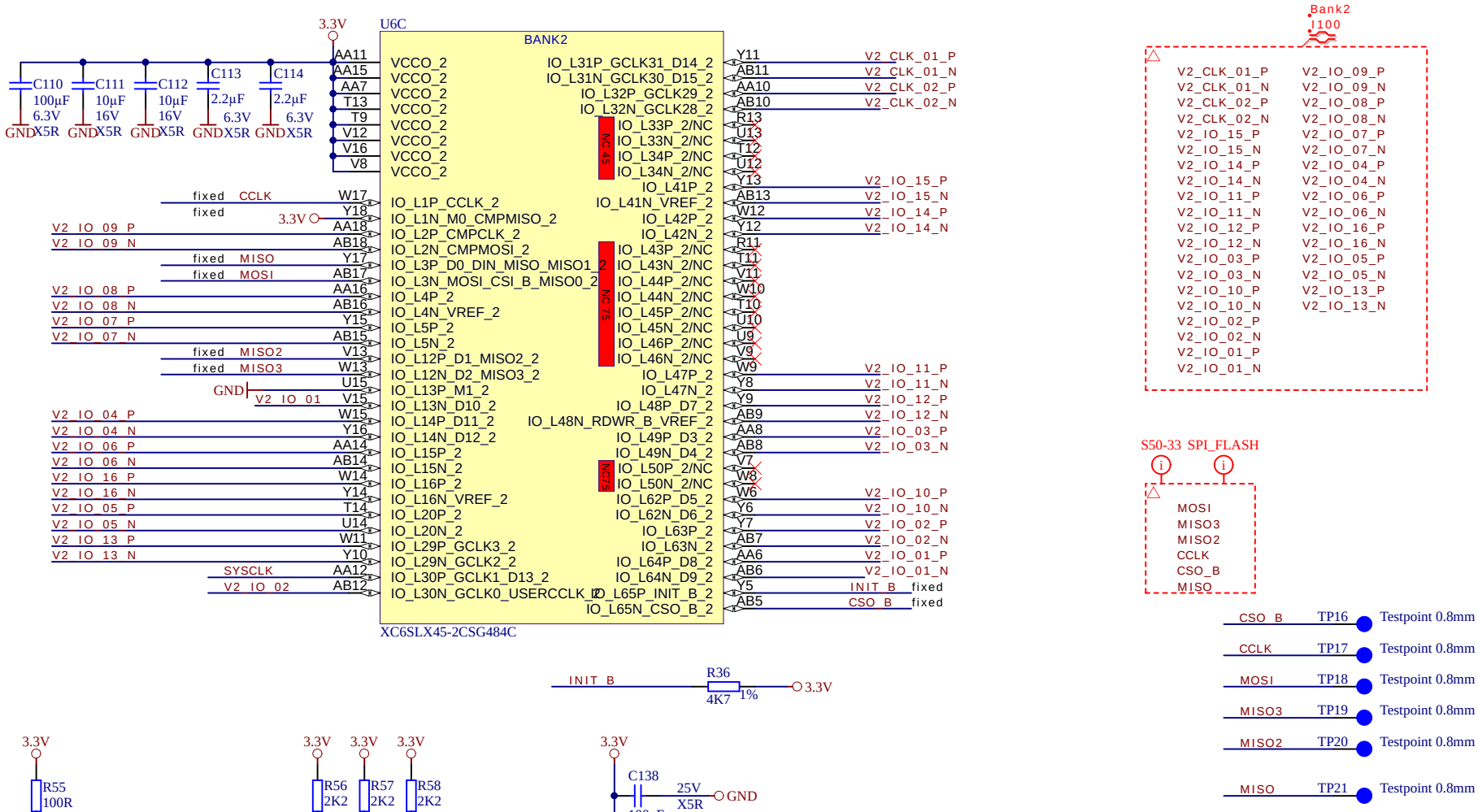
Date: 2018-11-28	Copyright: Trenz Electronic GmbH		Page5 of 12
Filename: FPGA_DDR3.SchDoc			



Title: TE0630 - FPGA_B2			
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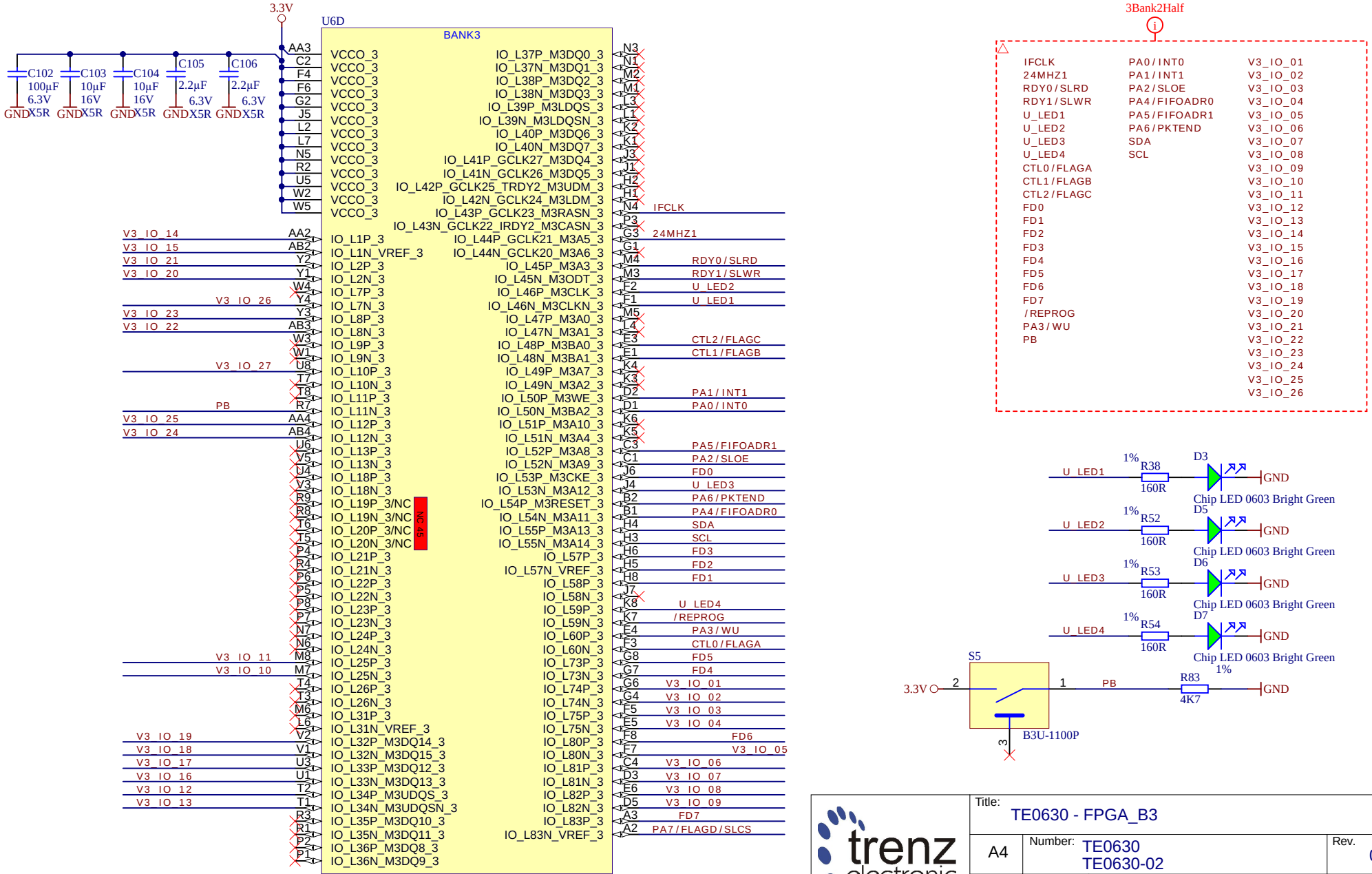
Date: 2018-11-28	Copyright: Trenz Electronic GmbH		Page6 of 12
Filename: FPGA_B2.SchDoc			



Title: TE0630 - FPGA_B3			
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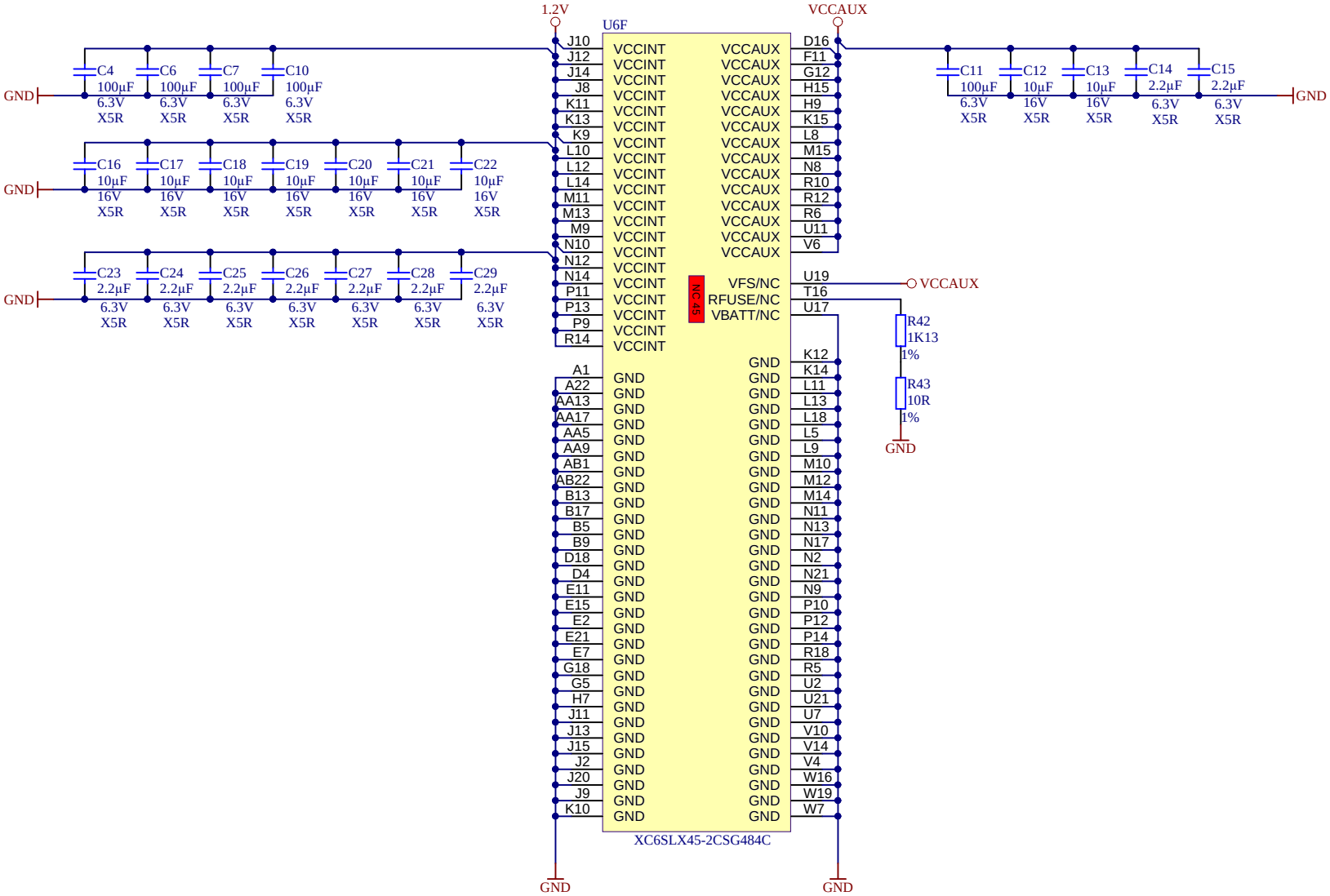
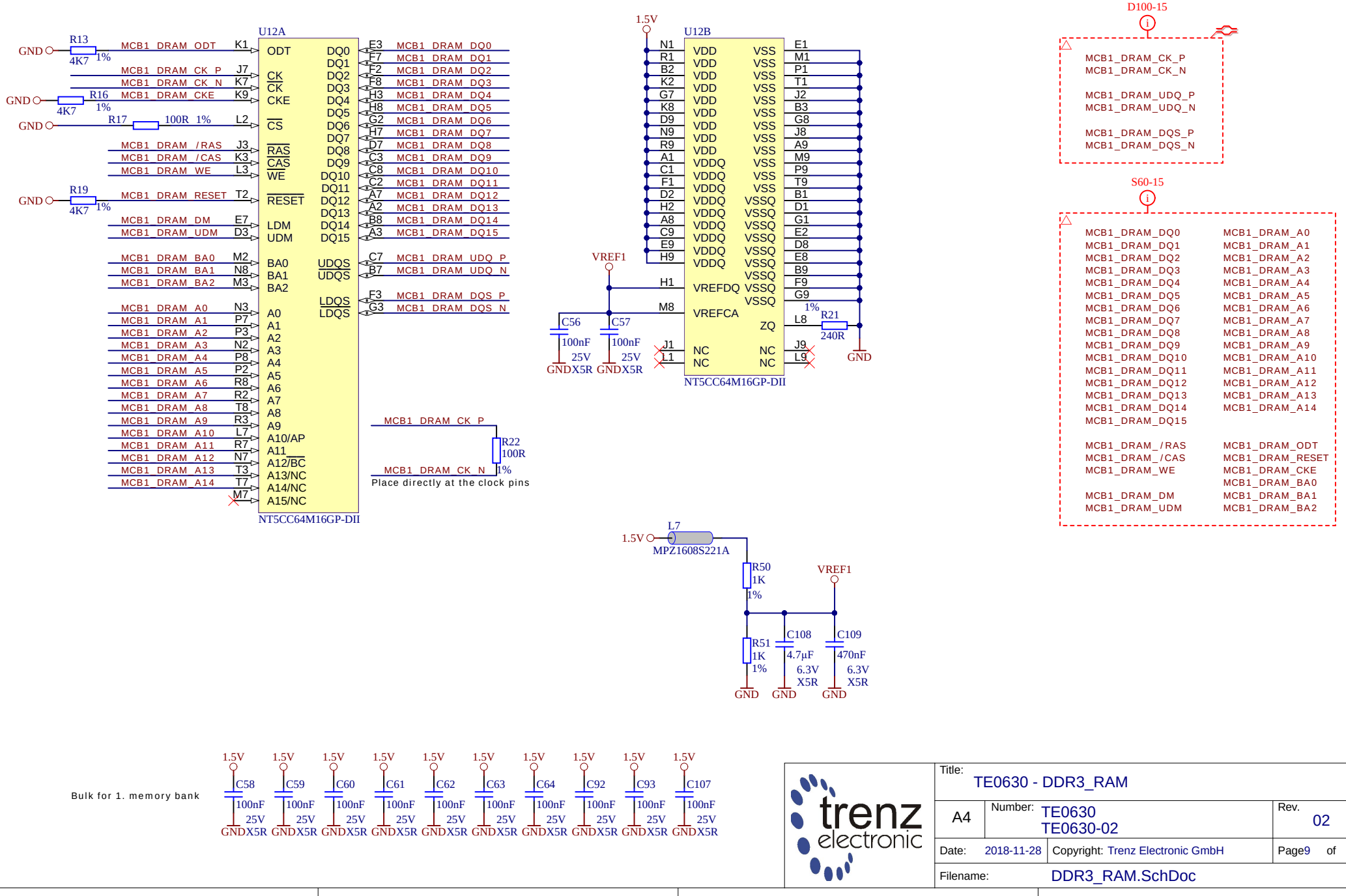
Date: 2018-11-28	Copyright: Trenz Electronic GmbH		Page7 of 12
Filename: FPGA_B3.SchDoc			



Title: TE0630 - FPGA_PWR			
A4	Number: TE0630 TE0630-02		Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH		Page 8 of 12
Filename: FPGA_PWR.SchDoc			


U12A
NT5CC64M16GP-DII
U12B
NT5CC64M16GP-DII
R13
R16
R17
100R 1% L2
R19
4K7 1%
MCB1_DRAM_ODT K1
MCB1_DRAM_CK_P J7
MCB1_DRAM_CK_N K7
MCB1_DRAM_CKE K9
MCB1_DRAM_/RAS J3
MCB1_DRAM_/CAS K3
MCB1_DRAM_WE L3
MCB1_DRAM_RESET T2
MCB1_DRAM_DM E7
MCB1_DRAM_UDM D3
MCB1_DRAM_BA0 M2
MCB1_DRAM_BA1 N8
MCB1_DRAM_BA2 M3
MCB1_DRAM_A0 N3
MCB1_DRAM_A1 P7
MCB1_DRAM_A2 P3
MCB1_DRAM_A3 N2
MCB1_DRAM_A4 P8
MCB1_DRAM_A5 P2
MCB1_DRAM_A6 R8
MCB1_DRAM_A7 R2
MCB1_DRAM_A8 T8
MCB1_DRAM_A9 R3
MCB1_DRAM_A10 L7
MCB1_DRAM_A11 R7
MCB1_DRAM_A12 N7
MCB1_DRAM_A13 T3
MCB1_DRAM_A14 T7
M7
ODT
CK
CK
CKE
CS
RAS
CAS
WE
RESET
LDM
UDM
BA0
BA1
BA2
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12/BC
A13/NC
A14/NC
A15/NC
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
UDQS
UDQS
LDQS
LDQS
MCB1_DRAM_DQ0 E3
MCB1_DRAM_DQ1 F7
MCB1_DRAM_DQ2 F2
MCB1_DRAM_DQ3 F8
MCB1_DRAM_DQ4 H3
MCB1_DRAM_DQ5 H8
MCB1_DRAM_DQ6 G2
MCB1_DRAM_DQ7 H7
MCB1_DRAM_DQ8 D7
MCB1_DRAM_DQ9 C3
MCB1_DRAM_DQ10 C8
MCB1_DRAM_DQ11 C2
MCB1_DRAM_DQ12 A7
MCB1_DRAM_DQ13 A2
MCB1_DRAM_DQ14 B8
MCB1_DRAM_DQ15 A3
MCB1_DRAM_UDQ_P C7
MCB1_DRAM_UDQ_N B7
MCB1_DRAM_DQS_P F3
MCB1_DRAM_DQS_N G3
MCB1_DRAM_CK_P
MCB1_DRAM_CK_N
R22 100R 1%
Place directly at the clock pins
1.5V
VREF1
C56 100nF 25V X5R
C57 100nF 25V X5R
R21 240R 1%
L8
J1
L1
J9
L9
N1 R1 B2 K2 G7 K8 D9 N9 R9 A1 C1 F1 D2 H2 A8 C9 E9 H9
VDD
H1
VREFDQ
M8
VREFCA
NC
ZQ
VSS
VSSQ
VDDQ
E1 M1 P1 T1 J2 B3 G8 J8 A9 M9 P9 T9 B1 D1 G1 E2 D8 E8 B9 F9 G9
GND
D100-15
MCB1_DRAM_CK_P
MCB1_DRAM_CK_N
MCB1_DRAM_UDQ_P
MCB1_DRAM_UDQ_N
MCB1_DRAM_DQS_P
MCB1_DRAM_DQS_N
S60-15
MCB1_DRAM_DQ0
MCB1_DRAM_DQ1
MCB1_DRAM_DQ2
MCB1_DRAM_DQ3
MCB1_DRAM_DQ4
MCB1_DRAM_DQ5
MCB1_DRAM_DQ6
MCB1_DRAM_DQ7
MCB1_DRAM_DQ8
MCB1_DRAM_DQ9
MCB1_DRAM_DQ10
MCB1_DRAM_DQ11
MCB1_DRAM_DQ12
MCB1_DRAM_DQ13
MCB1_DRAM_DQ14
MCB1_DRAM_DQ15
MCB1_DRAM_/RAS
MCB1_DRAM_/CAS
MCB1_DRAM_WE
MCB1_DRAM_DM
MCB1_DRAM_UDM
MCB1_DRAM_A0
MCB1_DRAM_A1
MCB1_DRAM_A2
MCB1_DRAM_A3
MCB1_DRAM_A4
MCB1_DRAM_A5
MCB1_DRAM_A6
MCB1_DRAM_A7
MCB1_DRAM_A8
MCB1_DRAM_A9
MCB1_DRAM_A10
MCB1_DRAM_A11
MCB1_DRAM_A12
MCB1_DRAM_A13
MCB1_DRAM_A14
MCB1_DRAM_ODT
MCB1_DRAM_RESET
MCB1_DRAM_CKE
MCB1_DRAM_BA0
MCB1_DRAM_BA1
MCB1_DRAM_BA2
L7
MPZ1608S221A
R50 1K 1%
R51 1K 1%
C108 4.7µF 6.3V X5R
C109 470nF 6.3V X5R
Bulk for 1. memory bank
C58 C59 C60 C61 C62 C63 C64 C92 C93 C107
100nF 25V X5R
trenz electronic
Title: TE0630 - DDR3_RAM
A4
Number: TE0630 TE0630-02
Rev. 02
Date: 2018-11-28
Copyright: Trenz Electronic GmbH
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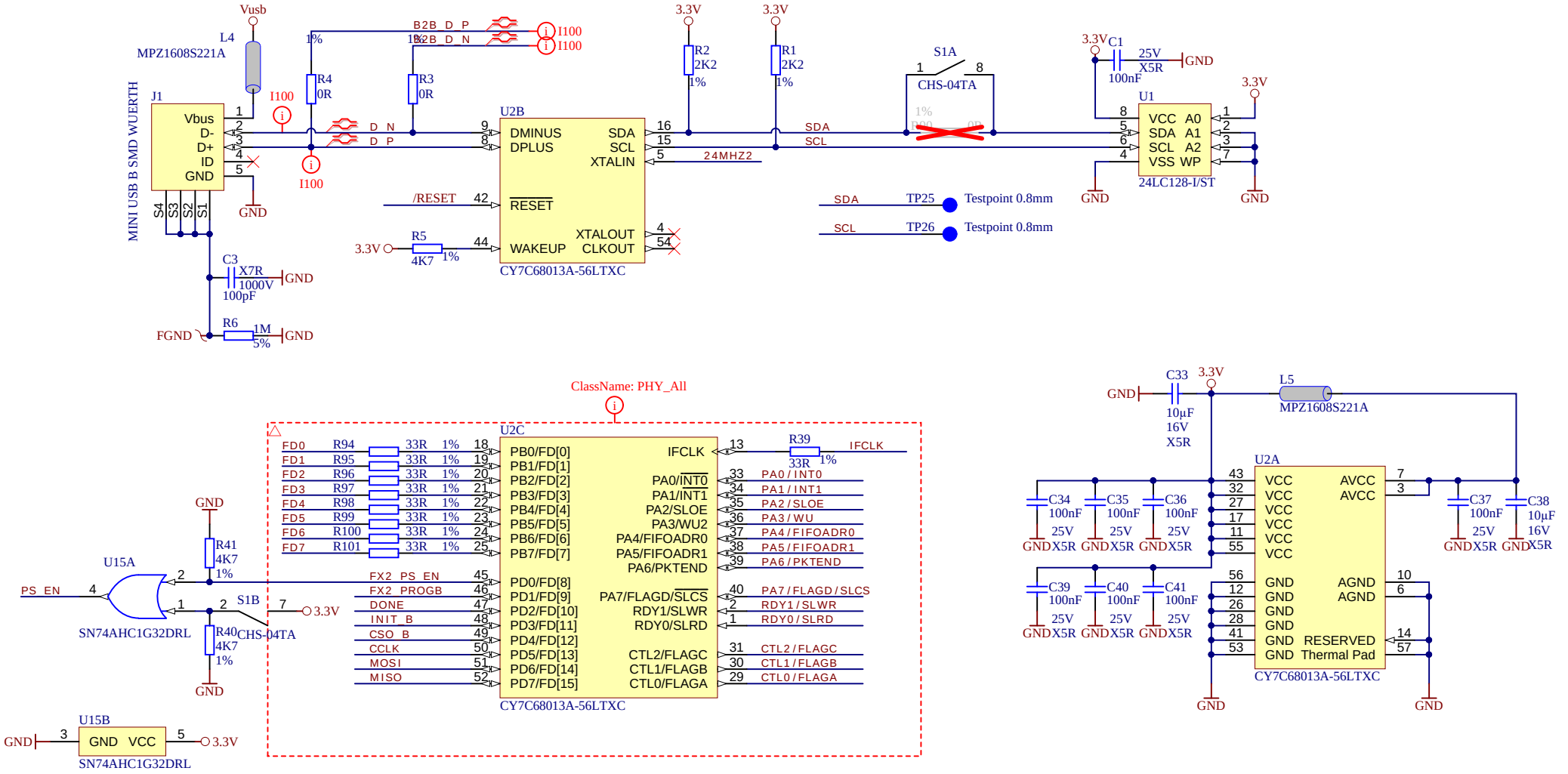
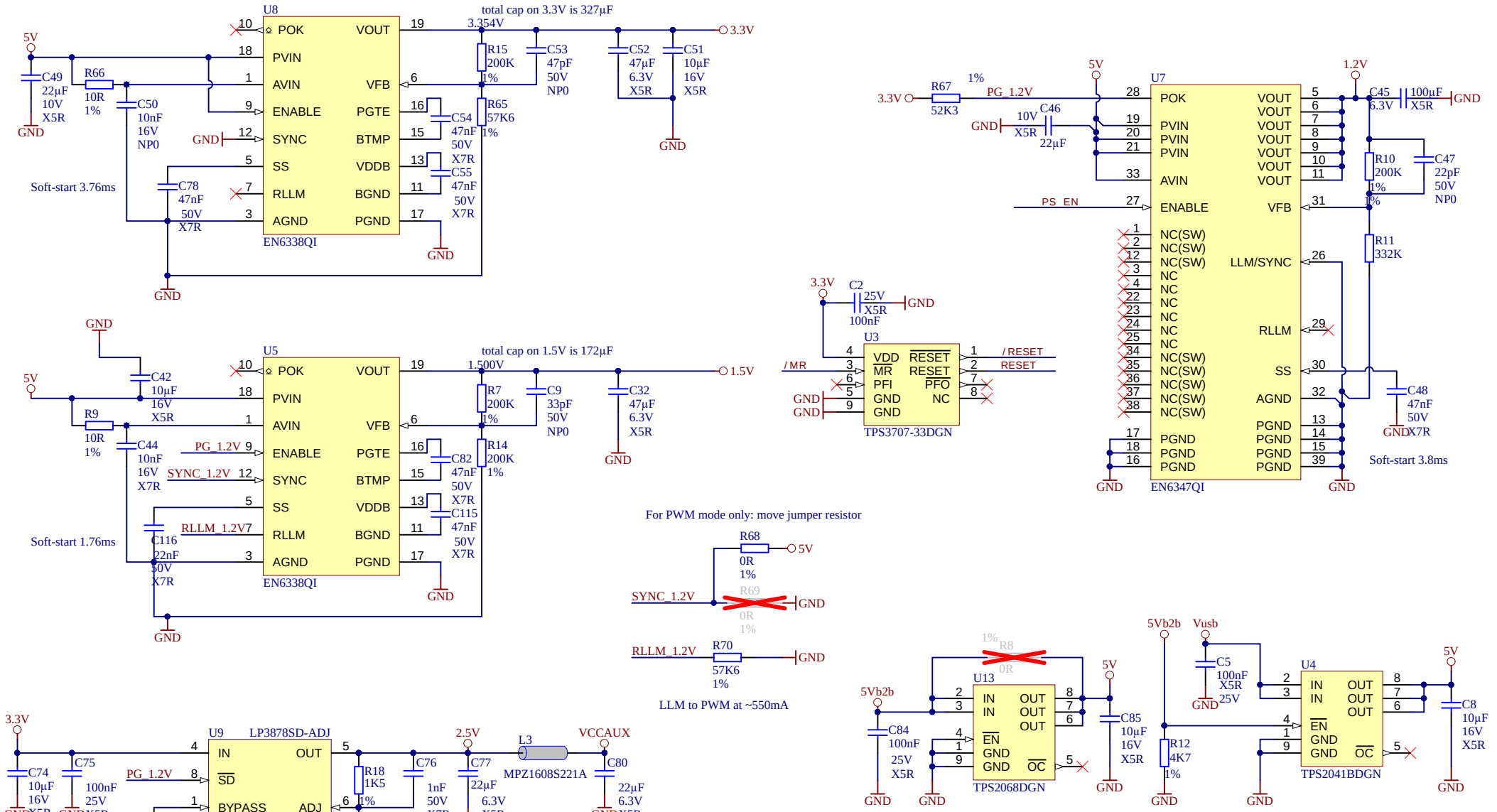
Filename: DDR3_RAM.SchDoc



trenz electronic	Title: TE0630 - USB		
A4	Number: TE0630 TE0630-02		Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH		Page10 of 12
Filename: USB.SchDoc			



trenz electronic	Title: TE0630 - POWER		
	A4	Number: TE0630 TE0630-02	Rev. 02
	Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page11 of 12
	Filename: Power.SchDoc		

CHANGES REV01 to REV02

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1) Replaced U8 by EN6338QI
2) Rerouted nets around U8, results in new track length for:
   Signal V3_IO_06 15.2475 mm (was 15.0047mm)
   Signal V3_IO_07 16.0151 mm (was 15.0452 mm)
3) Replaced U5 by EN 6338QI
4) PS_EN now via OR gate
5) Replaced obsolete Diodes D1, D2 D4, by BAT54A
6) Fixed Footprint of U10 according to datasheet
7) Update from LIB
8) Rearranged Testpoints
9) Added Traceability Pad
10) Replaced S5 by smaller PB AN26337
11) Hardware revision coding updated to Rev02

trenz electronic	Title: TE0630 - Changes list		
A4	Number: TE0630 TE0630-02		Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH		Page12 of 12
Filename: Revision_Changes.SchDoc			