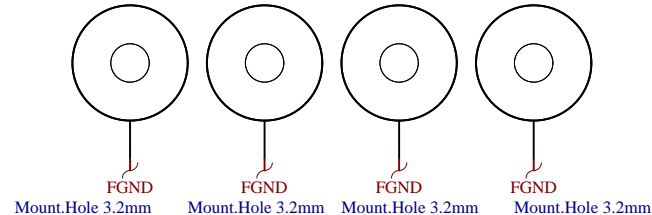
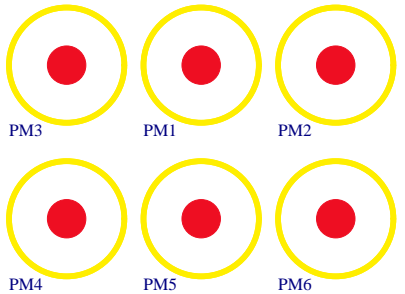
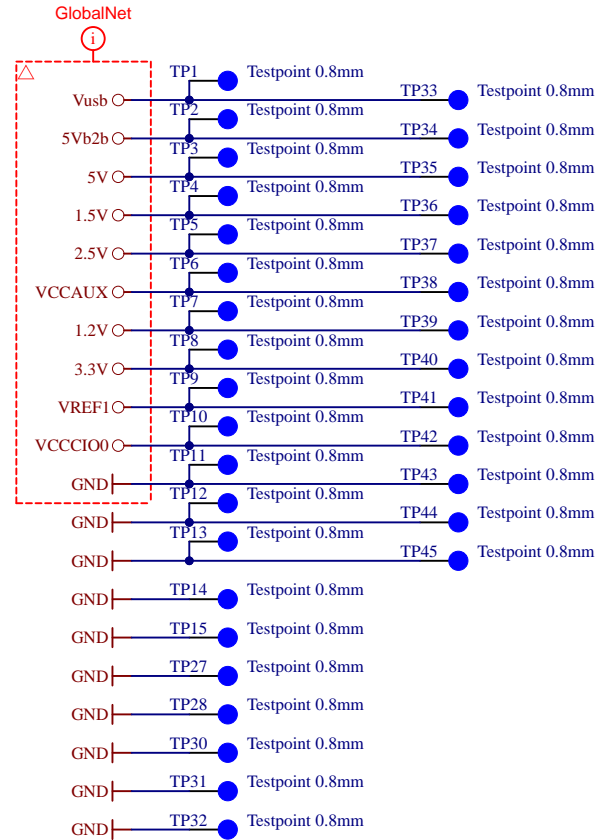
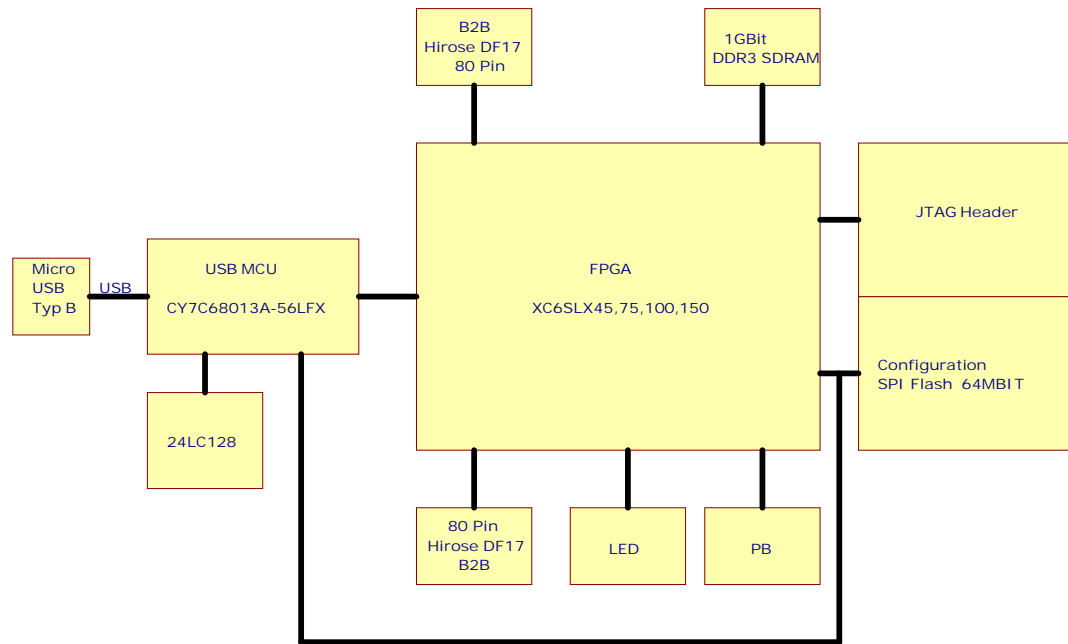


- U\_Power  
Power.SchDoc
- U\_FPGA\_PWR  
FPGA\_PWR.SchDoc
- U\_DDR3\_RAM  
DDR3\_RAM.SchDoc
- U\_FPGA\_CFG\_CLK  
FPGA\_CFG\_CLK.SchDoc
- U\_FPGA\_B3  
FPGA\_B3.SchDoc
- U\_FPGA\_DDR3  
FPGA\_DDR3.SchDoc
- U\_FPGA\_B2  
FPGA\_B2.SchDoc
- U\_FPGA\_B0  
FPGA\_B0.SchDoc
- U\_USB  
USB.SchDoc
- U\_B2B\_Connectors  
B2B\_Connectors.SchDoc



Assembly variant	B-DWS
Created by	na
Modified by	MR
Modified at	2020-03-30
SVN Revision	9220

Title: TE0630		
A4	Number: TE0630 B-DWS	Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page1 of 12
Filename: TE0630.SchDoc		

1

2

3

4

A

A

B

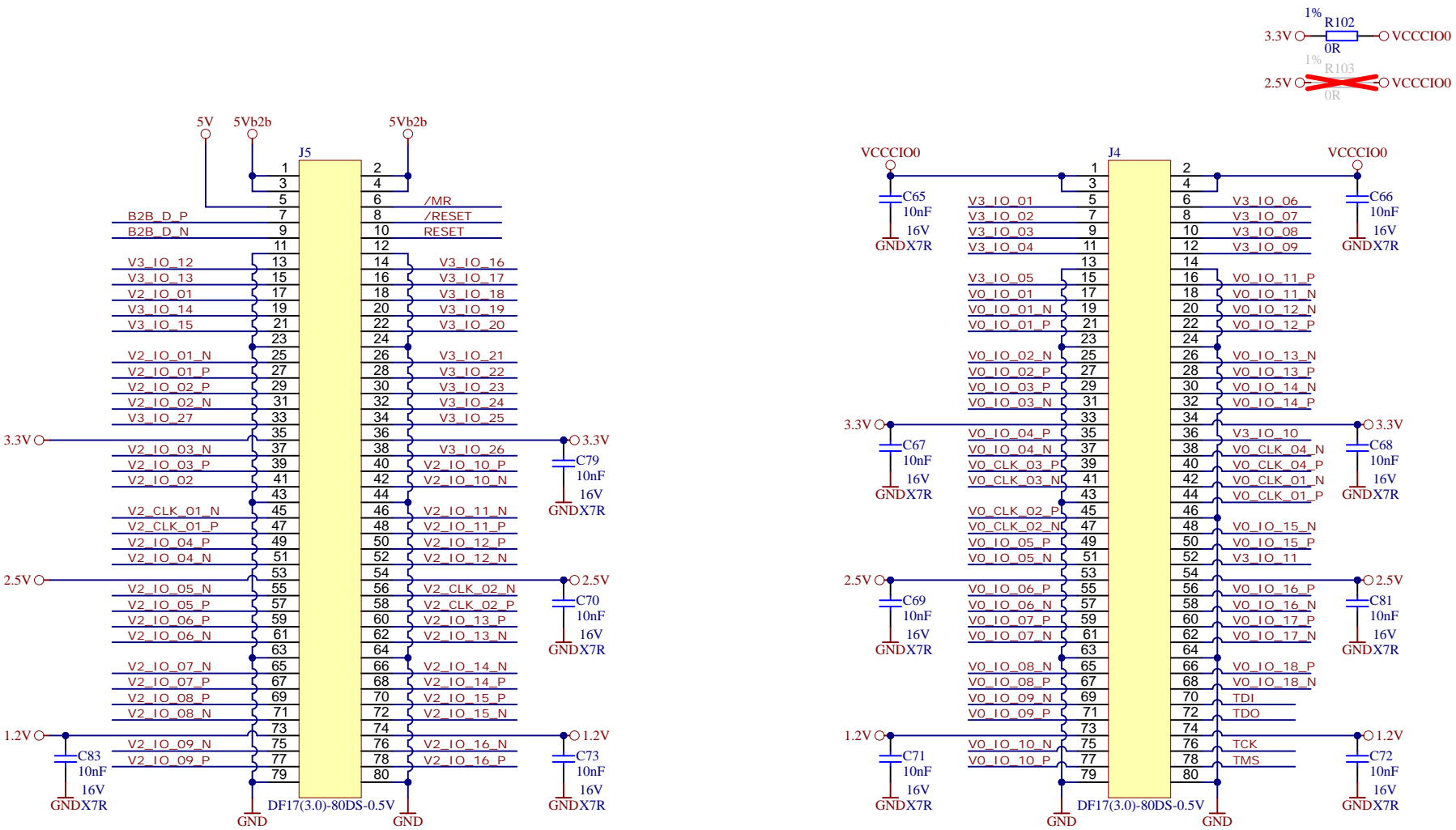
B

C

C

D

D



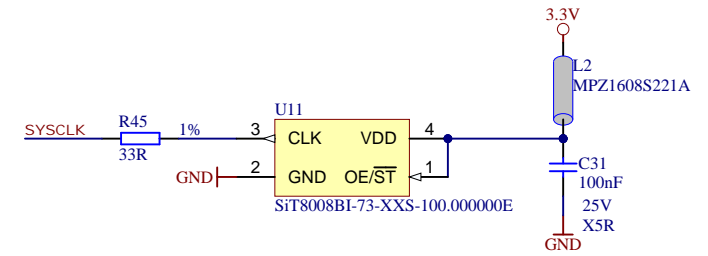
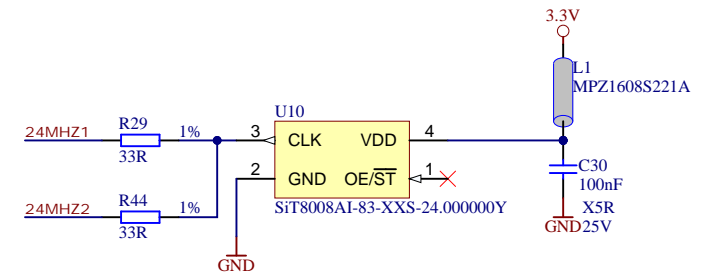
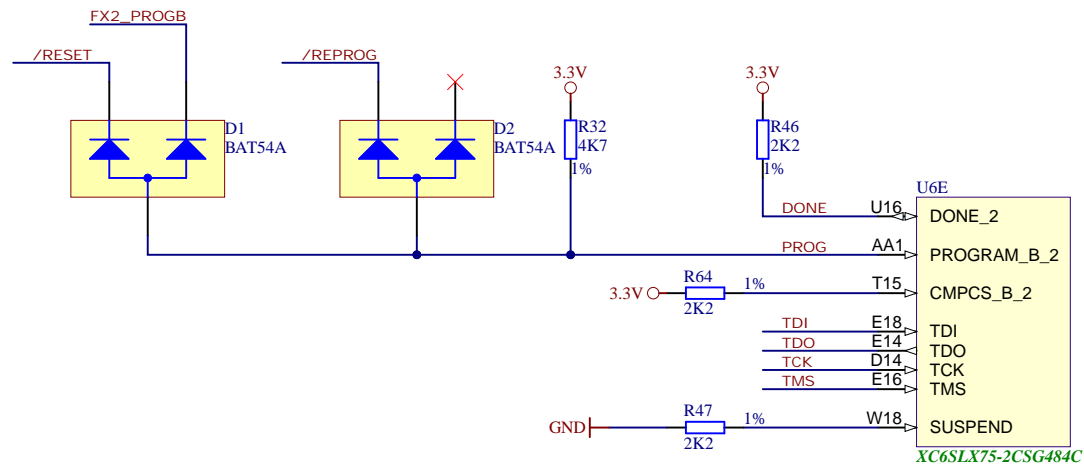
Title: TE0630 - B2B_Connectors		
A4	Number: TE0630 B-DWS	Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page2 of 12
Filename: B2B_Connectors.SchDoc		

1

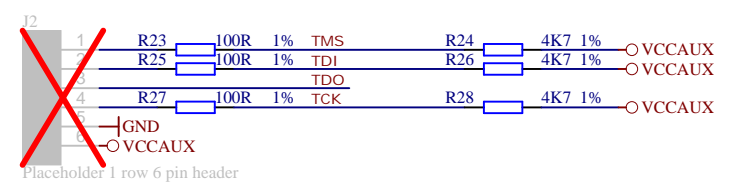
2


3

4

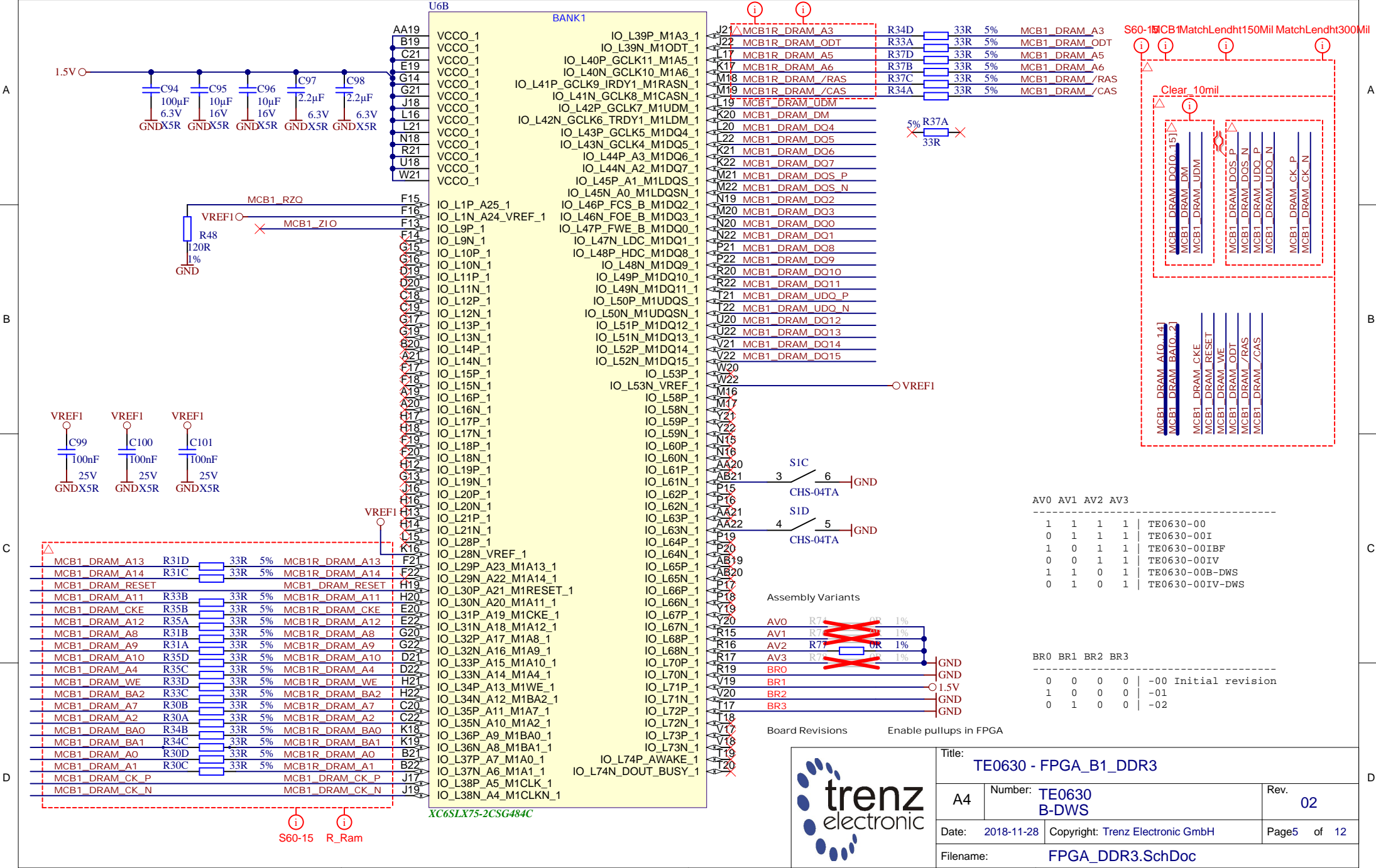


- 24MHZ1 TP22 Testpoint 0.8mm
- 24MHZ2 TP23 Testpoint 0.8mm
- SYSCLK TP24 Testpoint 0.8mm
- PROG TP29 Testpoint 0.8mm

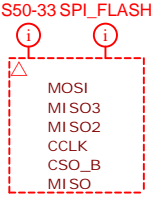
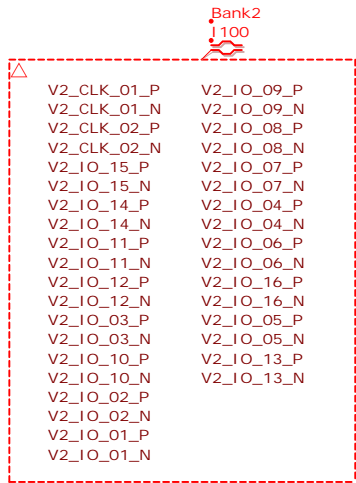
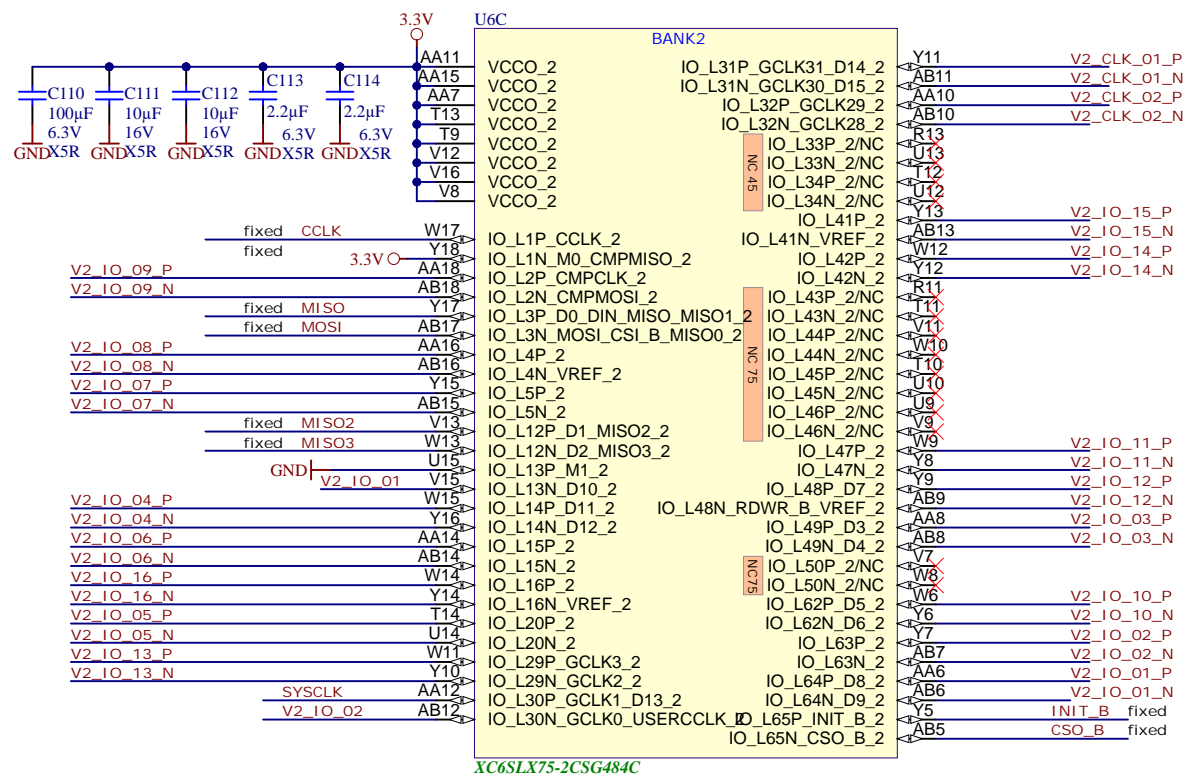


		Title: TE0630 - FPGA_CFG_CLK	
		A4	Number: TE0630 B-DWS
Date: 2018-11-28		Copyright: Trenz Electronic GmbH	
Page 3		of 12	
Filename: FPGA_CFG_CLK.SchDoc			

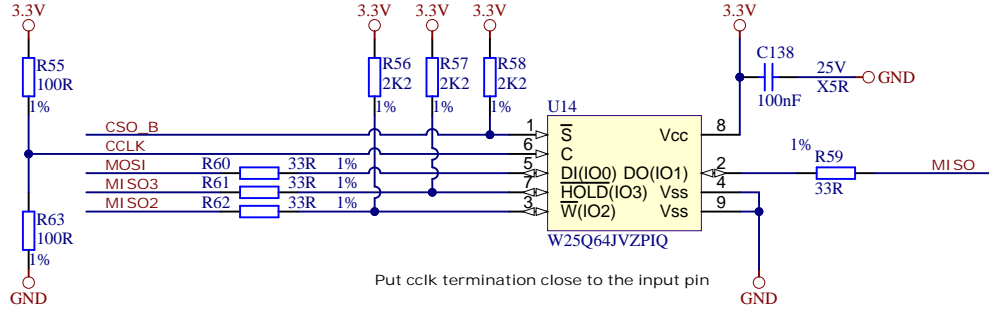
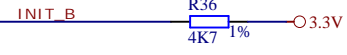




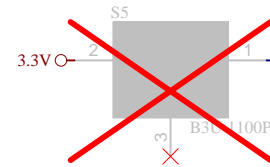
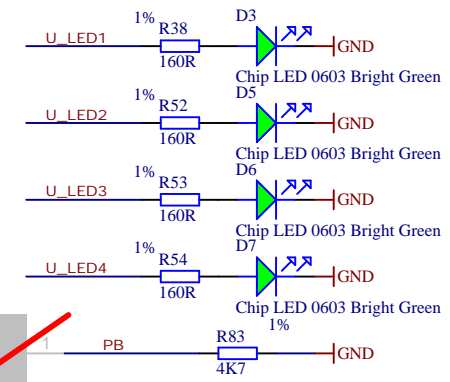
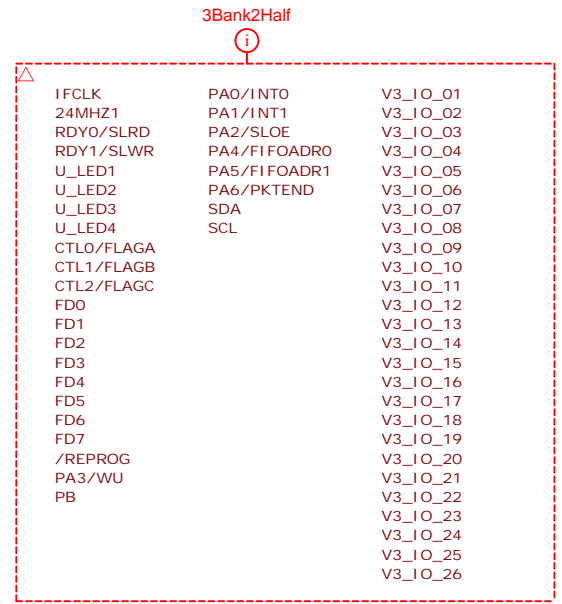
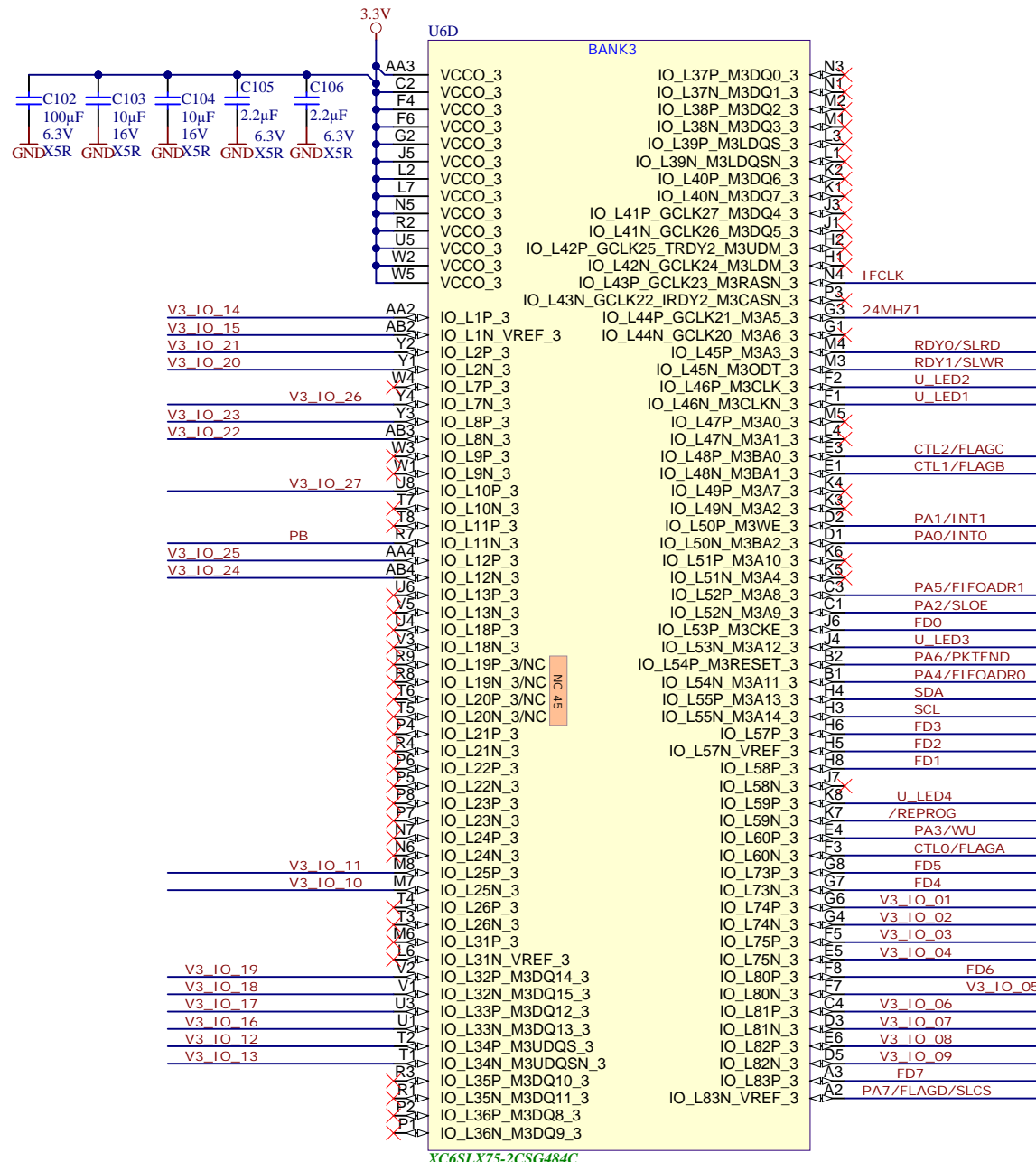
Title: <b>TE0630 - FPGA_B1_DDR3</b>			
A4	Number: <b>TE0630 B-DWS</b>	Rev. <b>02</b>	
Date: <b>2018-11-28</b>	Copyright: <b>Trenz Electronic GmbH</b>		Page <b>5</b> of <b>12</b>
Filename: <b>FPGA_DDR3.SchDoc</b>			



- CSO\_B TP16 ● Testpoint 0.8mm
- CCLK TP17 ● Testpoint 0.8mm
- MOSI TP18 ● Testpoint 0.8mm
- MISO3 TP19 ● Testpoint 0.8mm
- MISO2 TP20 ● Testpoint 0.8mm
- MISO TP21 ● Testpoint 0.8mm



Title: TE0630 - FPGA_B2		
A4	Number: TE0630 B-DWS	Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page 6 of 12
Filename: FPGA_B2.SchDoc		

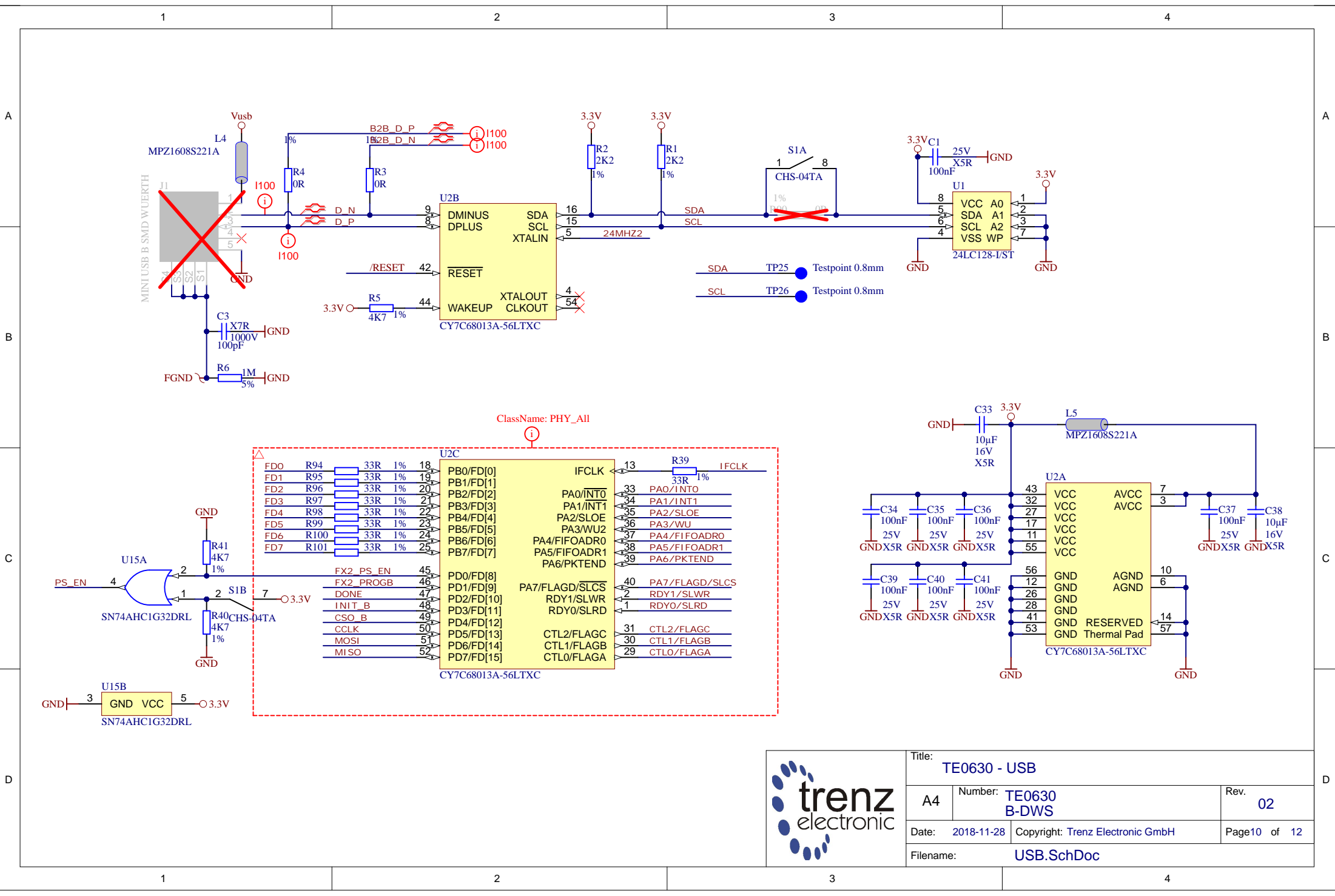


Title: <b>TE0630 - FPGA_B3</b>		
A4	Number: <b>TE0630 B-DWS</b>	Rev. <b>02</b>
Date: <b>2018-11-28</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>7</b> of <b>12</b>
Filename: <b>FPGA_B3.SchDoc</b>		

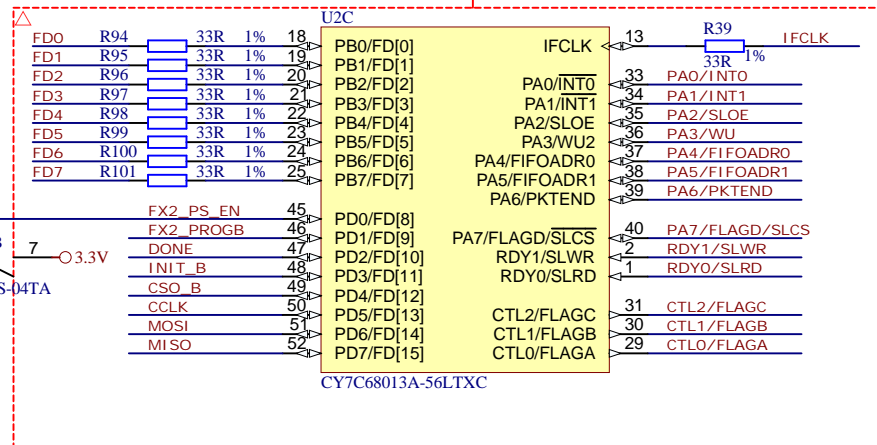








ClassName: PHY\_All



Title: TE0630 - USB		
A4	Number: TE0630 B-DWS	Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page 10 of 12
Filename: USB.SchDoc		



1

2

3

4

A

A

CHANGES REV01 to REV02

- 1) Replaced U8 by EN6338QI
- 2) Rerouted nets around U8, results in new track length for:  
     Signal V3\_IO\_06 15.2475 mm (was 15.0047mm)  
     Signal V3\_IO\_07 16.0151 mm (was 15.0452 mm)
- 3) Replaced U5 by EN 6338QI
- 4) PS\_EN now via OR gate
- 5) Replaced obsolete Diodes D1, D2 D4, by BAT54A
- 6) Fixed Footprint of U10 according to datasheet
- 7) Update from LIB
- 8) Rearranged Testpoints
- 9) Added Traceability Pad
- 10) Replaced S5 by smaller PB AN26337
- 11) Hardware revision coding updated to Rev02

CHANGES REV02

- 2020-03-30
- 1) Flash change (U14)

B


B

C

C

D

D

		Title: TE0630 - Changes list	
		A4	Number: TE0630 B-DWS
Date: 2018-11-28		Copyright: Trenz Electronic GmbH	
Filename: Revision_Changes.SchDoc		Page 12 of 12	

1

2

3

4