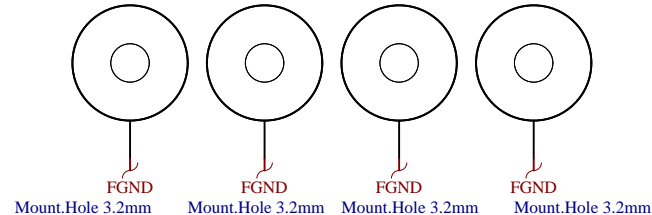
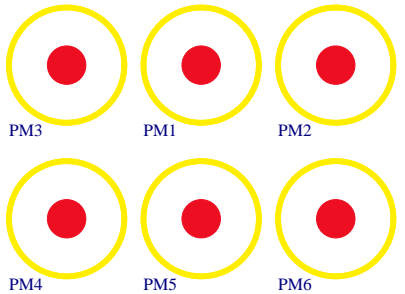
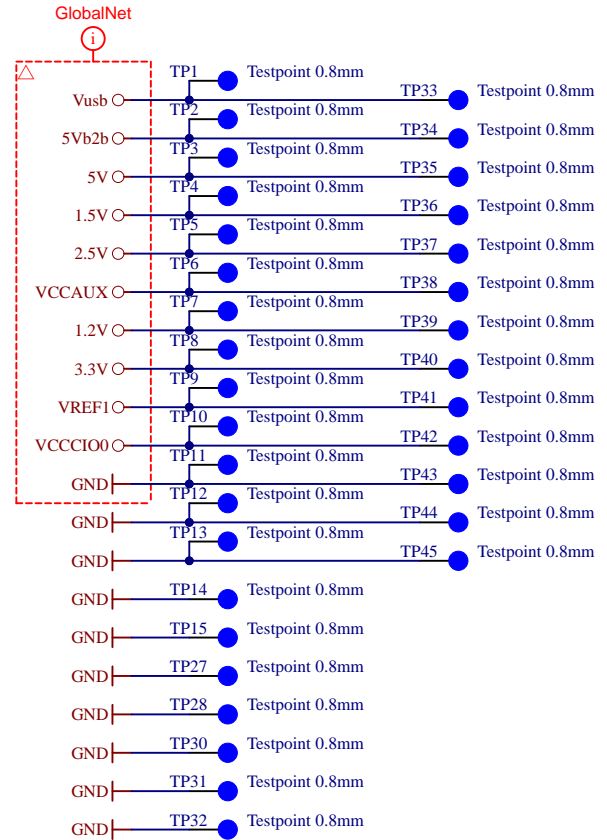
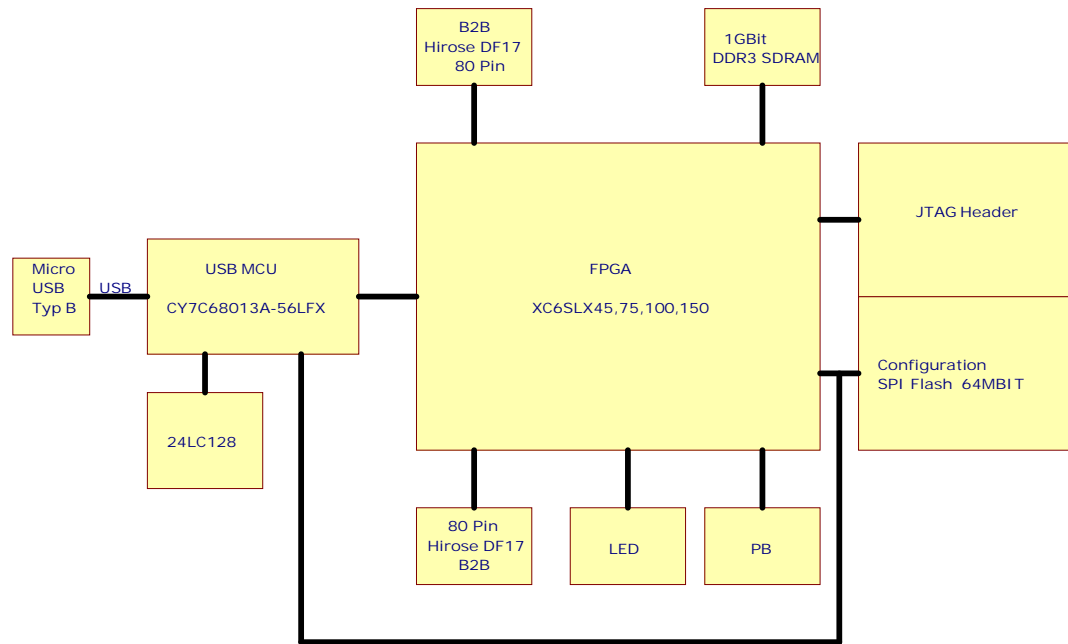
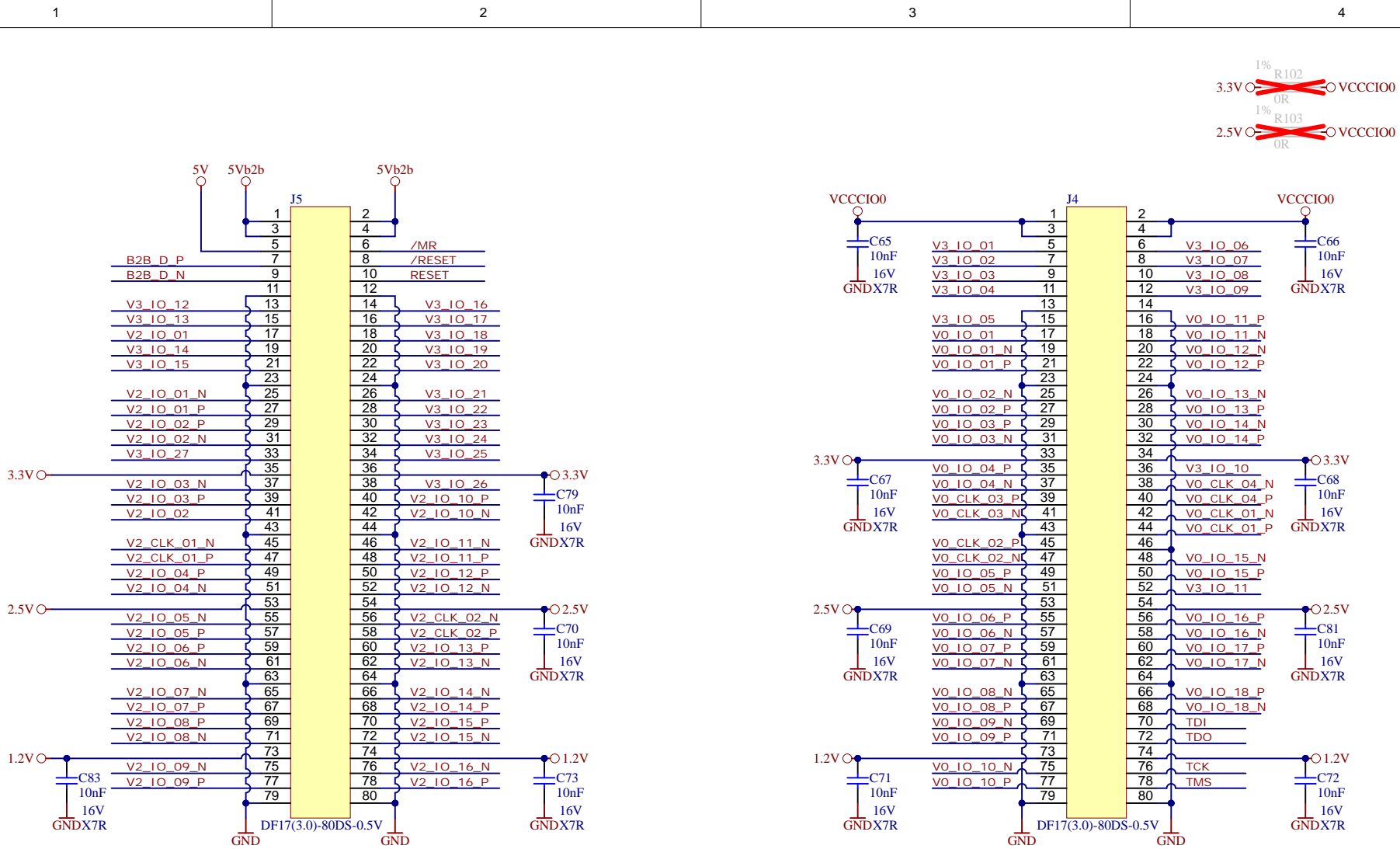



- U_Power
Power.SchDoc
- U_FPGA_PWR
FPGA_PWR.SchDoc
- U_DDR3_RAM
DDR3_RAM.SchDoc
- U_FPGA_CFG_CLK
FPGA_CFG_CLK.SchDoc
- U_FPGA_B3
FPGA_B3.SchDoc
- U_FPGA_DDR3
FPGA_DDR3.SchDoc
- U_FPGA_B2
FPGA_B2.SchDoc
- U_FPGA_B0
FPGA_B0.SchDoc
- U_USB
USB.SchDoc
- U_B2B_Connectors
B2B_Connectors.SchDoc

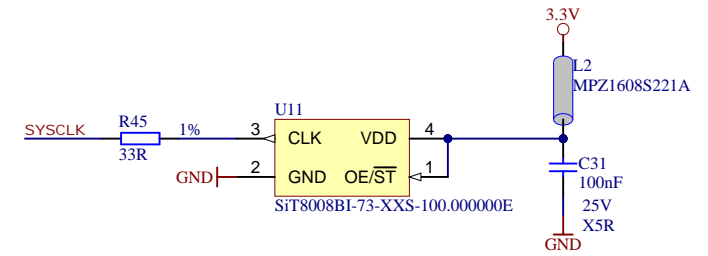
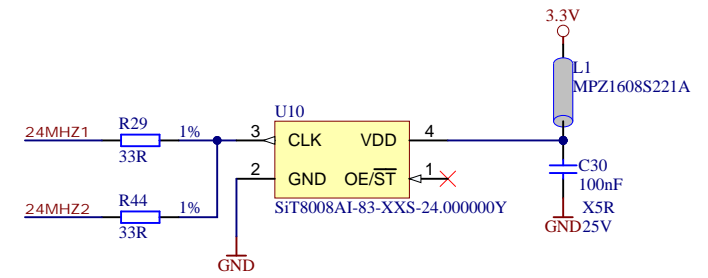
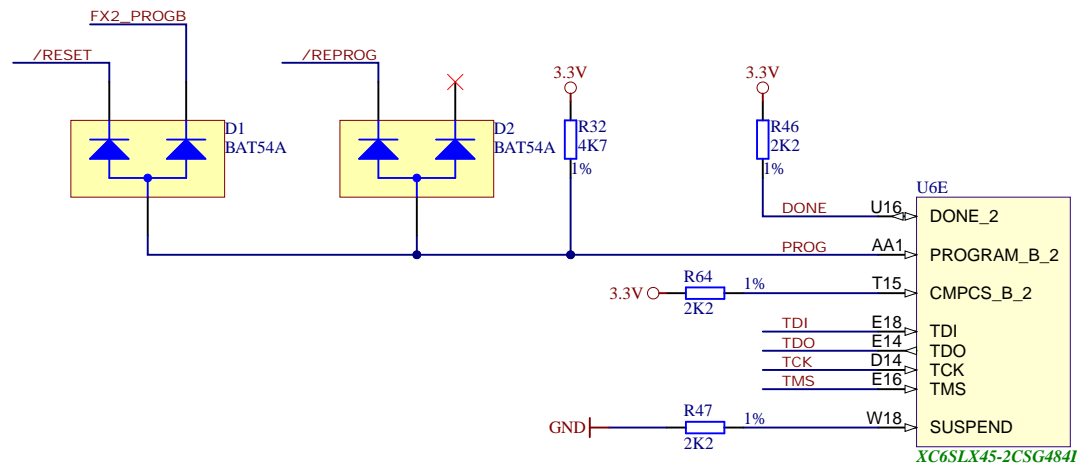


Assembly variant	I
Created by	na
Modified by	MR
Modified at	2020-03-30
SVN Revision	9220

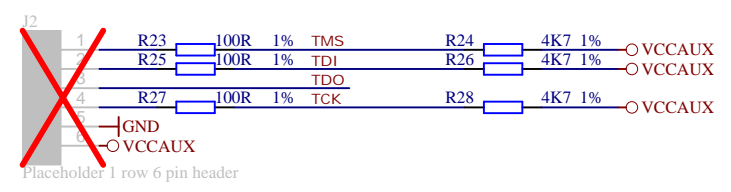
Title: TE0630		
A4	Number: TE0630	Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page1 of 12
Filename: TE0630.SchDoc		



	Title: TE0630 - B2B_Connectors		
	A4	Number: TE0630	Rev. 02
	Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page2 of 12
	Filename: B2B_Connectors.SchDoc		



- 24MHZ1 TP22 Testpoint 0.8mm
- 24MHZ2 TP23 Testpoint 0.8mm
- SYSCLK TP24 Testpoint 0.8mm
- PROG TP29 Testpoint 0.8mm



	Title: TE0630 - FPGA_CFG_CLK		
	A4	Number: TE0630	Rev. 02
	Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page3 of 12
	Filename: FPGA_CFG_CLK.SchDoc		

A

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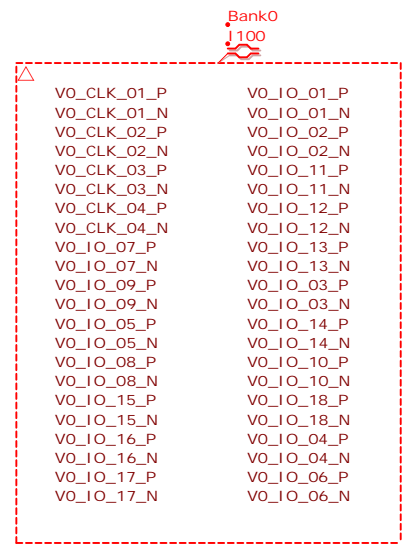
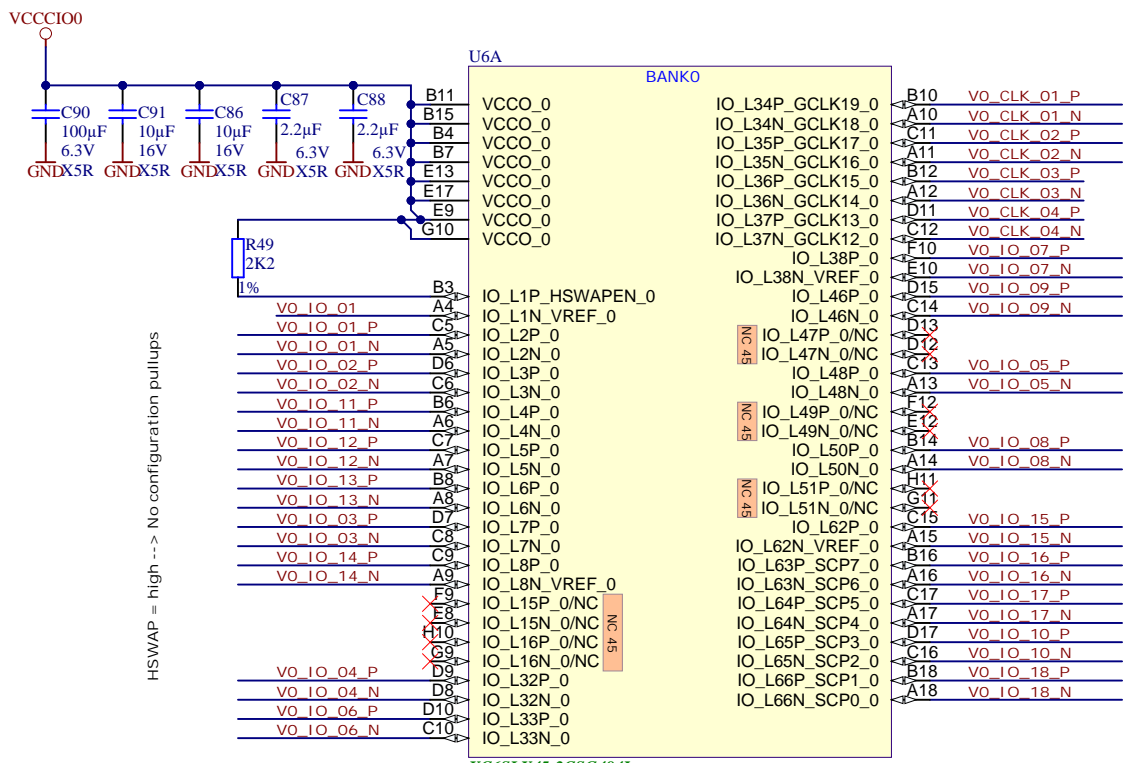
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D

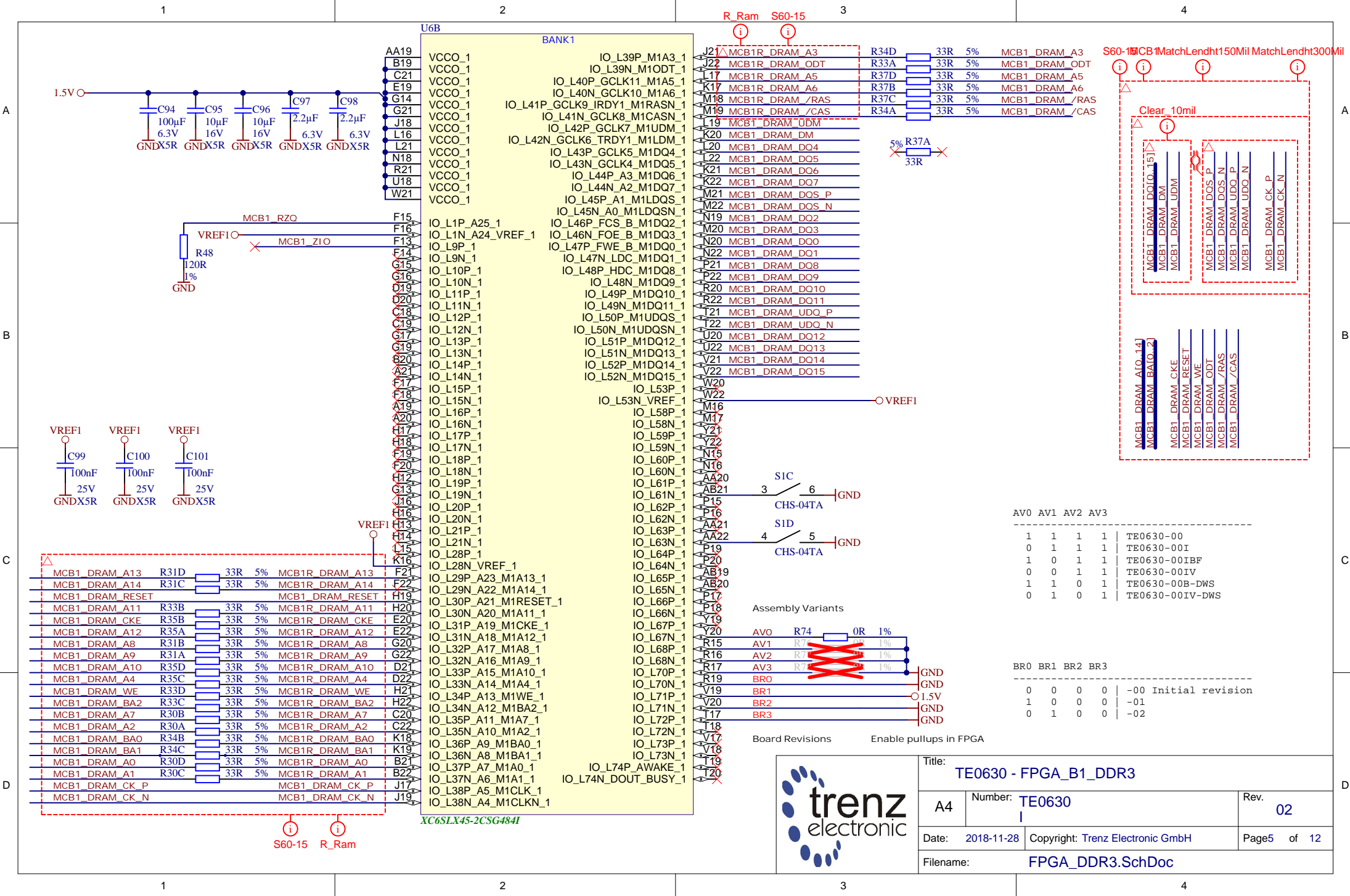


HSWAP = high --> No configuration pullups

XC6SLX45-2CSG484I

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Title: TE0630 - FPGA_B0		
A4	Number: TE0630	Rev. 02
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Filename: FPGA_B0.SchDoc		



BANK1

AA19	VCCO_1	IO_L39P_M1A3_1
B19	VCCO_1	IO_L39N_M1ODT_1
C21	VCCO_1	IO_L40P_GCLK11_M1A5_1
E19	VCCO_1	IO_L40N_GCLK10_M1A6_1
G14	VCCO_1	IO_L41P_GCLK9_IRDY1_M1RASN_1
G21	VCCO_1	IO_L41N_GCLK8_M1CASN_1
J18	VCCO_1	IO_L42P_GCLK7_M1UDM_1
L16	VCCO_1	IO_L42N_GCLK6_TRDY1_M1LDM_1
L21	VCCO_1	IO_L43P_GCLK5_M1DQ4_1
N18	VCCO_1	IO_L43N_GCLK4_M1DQ5_1
R21	VCCO_1	IO_L44P_A3_M1DQ6_1
U18	VCCO_1	IO_L44N_A2_M1DQ7_1
W21	VCCO_1	IO_L45P_A1_M1LDQS_1
F15	IO_L1P_A25_1	IO_L46P_FCS_B_M1DQ2_1
F16	IO_L1N_A24_VREF_1	IO_L46N_FOE_B_M1DQ3_1
F13	IO_L9P_1	IO_L47P_FWE_B_M1DQ0_1
F14	IO_L9N_1	IO_L47N_LDC_M1DQ1_1
G15	IO_L10P_1	IO_L48P_HDC_M1DQ8_1
G16	IO_L10N_1	IO_L48N_M1DQ9_1
D19	IO_L11P_1	IO_L49P_M1DQ10_1
D20	IO_L11N_1	IO_L49N_M1DQ11_1
C18	IO_L12P_1	IO_L50P_M1UDQS_1
C19	IO_L12N_1	IO_L50N_M1UDQSN_1
G17	IO_L13P_1	IO_L51P_M1DQ12_1
G19	IO_L13N_1	IO_L51N_M1DQ13_1
B20	IO_L14P_1	IO_L52P_M1DQ14_1
B21	IO_L14N_1	IO_L52N_M1DQ15_1
A21	IO_L15P_1	IO_L53P_1
F17	IO_L15N_1	IO_L53N_VREF_1
A19	IO_L16P_1	IO_L58P_1
A20	IO_L16N_1	IO_L58N_1
H17	IO_L17P_1	IO_L59P_1
H18	IO_L17N_1	IO_L59N_1
F19	IO_L18P_1	IO_L60P_1
F20	IO_L18N_1	IO_L60N_1
H12	IO_L19P_1	IO_L61P_1
H13	IO_L19N_1	IO_L61N_1
G13	IO_L20P_1	IO_L62P_1
J16	IO_L20N_1	IO_L62N_1
H16	IO_L21P_1	IO_L63P_1
L15	IO_L21N_1	IO_L63N_1
K16	IO_L28P_1	IO_L64P_1
F21	IO_L28N_VREF_1	IO_L64N_1
F22	IO_L29P_A23_M1A13_1	IO_L65P_1
F23	IO_L29N_A22_M1A14_1	IO_L65N_1
H19	IO_L30P_A21_M1RESET_1	IO_L66P_1
H20	IO_L30N_A20_M1A11_1	IO_L66N_1
E20	IO_L31P_A19_M1CKE_1	IO_L67P_1
E22	IO_L31N_A18_M1A12_1	IO_L67N_1
G20	IO_L32P_A17_M1A8_1	IO_L68P_1
G22	IO_L32N_A16_M1A9_1	IO_L68N_1
D21	IO_L33P_A15_M1A10_1	IO_L70P_1
D22	IO_L33N_A14_M1A4_1	IO_L70N_1
H21	IO_L34P_A13_M1WE_1	IO_L71P_1
H22	IO_L34N_A12_M1BA2_1	IO_L71N_1
C20	IO_L35P_A11_M1A7_1	IO_L72P_1
C22	IO_L35N_A10_M1A2_1	IO_L72N_1
K18	IO_L36P_A9_M1BA0_1	IO_L73P_1
K19	IO_L36N_A8_M1BA1_1	IO_L73N_1
B21	IO_L37P_A7_M1A0_1	IO_L73N_1
B22	IO_L37N_A6_M1A1_1	IO_L74N_DOUT_BUSY_1
J17	IO_L38P_A5_M1CLK_1	
J19	IO_L38N_A4_M1CLKN_1	

XC6SLX45-2CSG4841

R_Ram S60-15

S60-15 CB MatchLendht150Mil MatchLendht300Mil

AV0	AV1	AV2	AV3	
1	1	1	1	TE0630-00
0	1	1	1	TE0630-00I
1	0	1	1	TE0630-00IBF
0	0	1	1	TE0630-00IV
1	1	0	1	TE0630-00B-DWS
0	1	0	1	TE0630-00IV-DWS

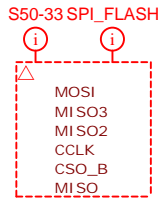
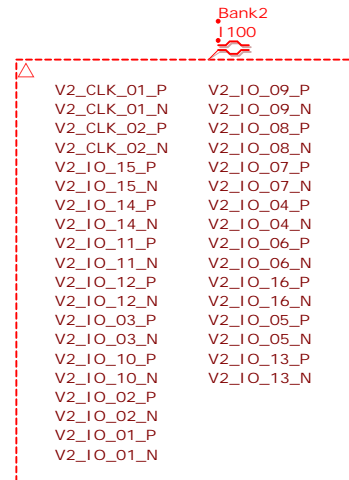
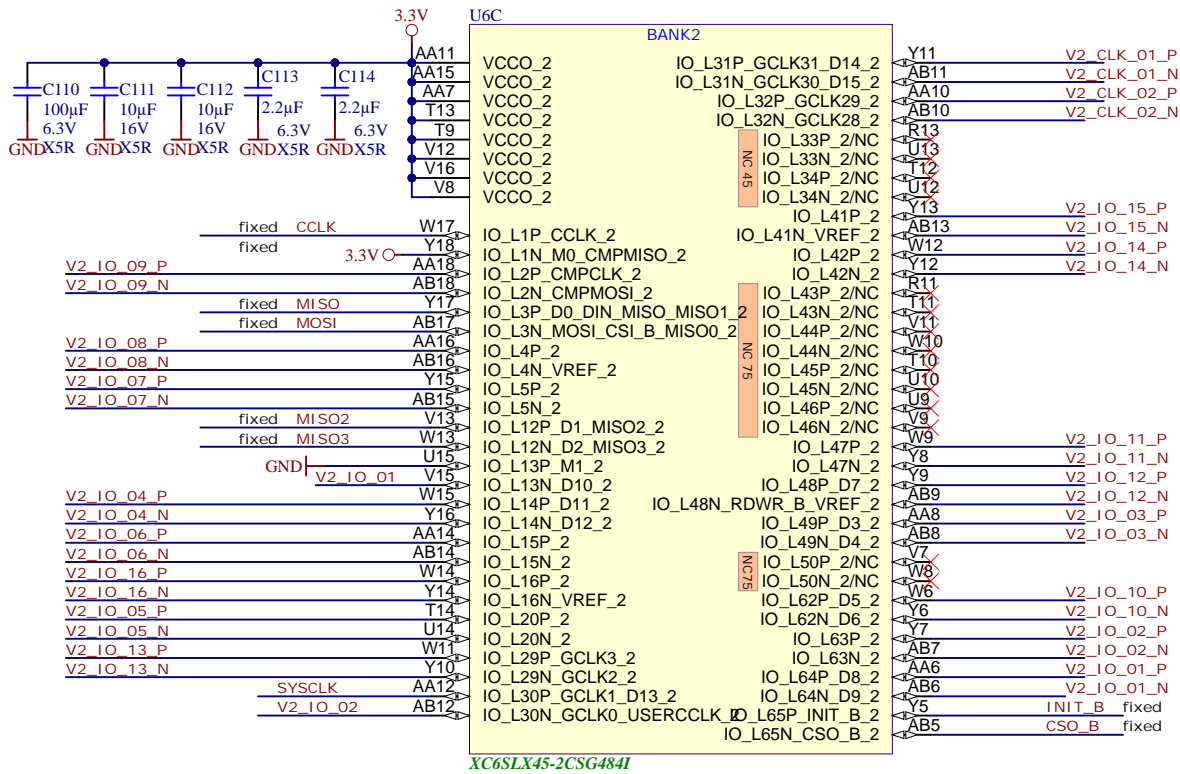
BR0	BR1	BR2	BR3	
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1	0	0	0	-01
0	1	0	0	-02

Assembly Variants

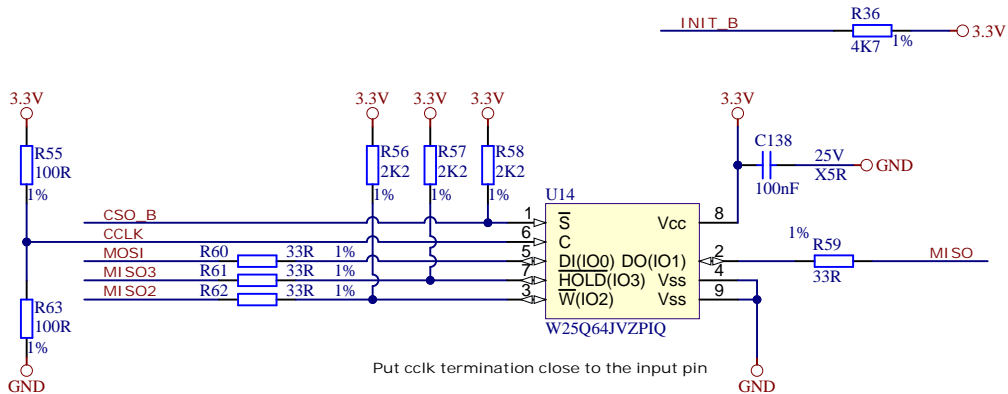
Board Revisions Enable pullups in FPGA



Title: TE0630 - FPGA_B1_DDR3		
A4	Number: TE0630	Rev: 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page 5 of 12
Filename: FPGA_DDR3.SchDoc		



- CSO_B TP16 ● Testpoint 0.8mm
- CCLK TP17 ● Testpoint 0.8mm
- MOSI TP18 ● Testpoint 0.8mm
- MISO3 TP19 ● Testpoint 0.8mm
- MISO2 TP20 ● Testpoint 0.8mm
- MISO TP21 ● Testpoint 0.8mm



Title: TE0630 - FPGA_B2		
A4	Number: TE0630	Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page6 of 12
Filename: FPGA_B2.SchDoc		

A

A

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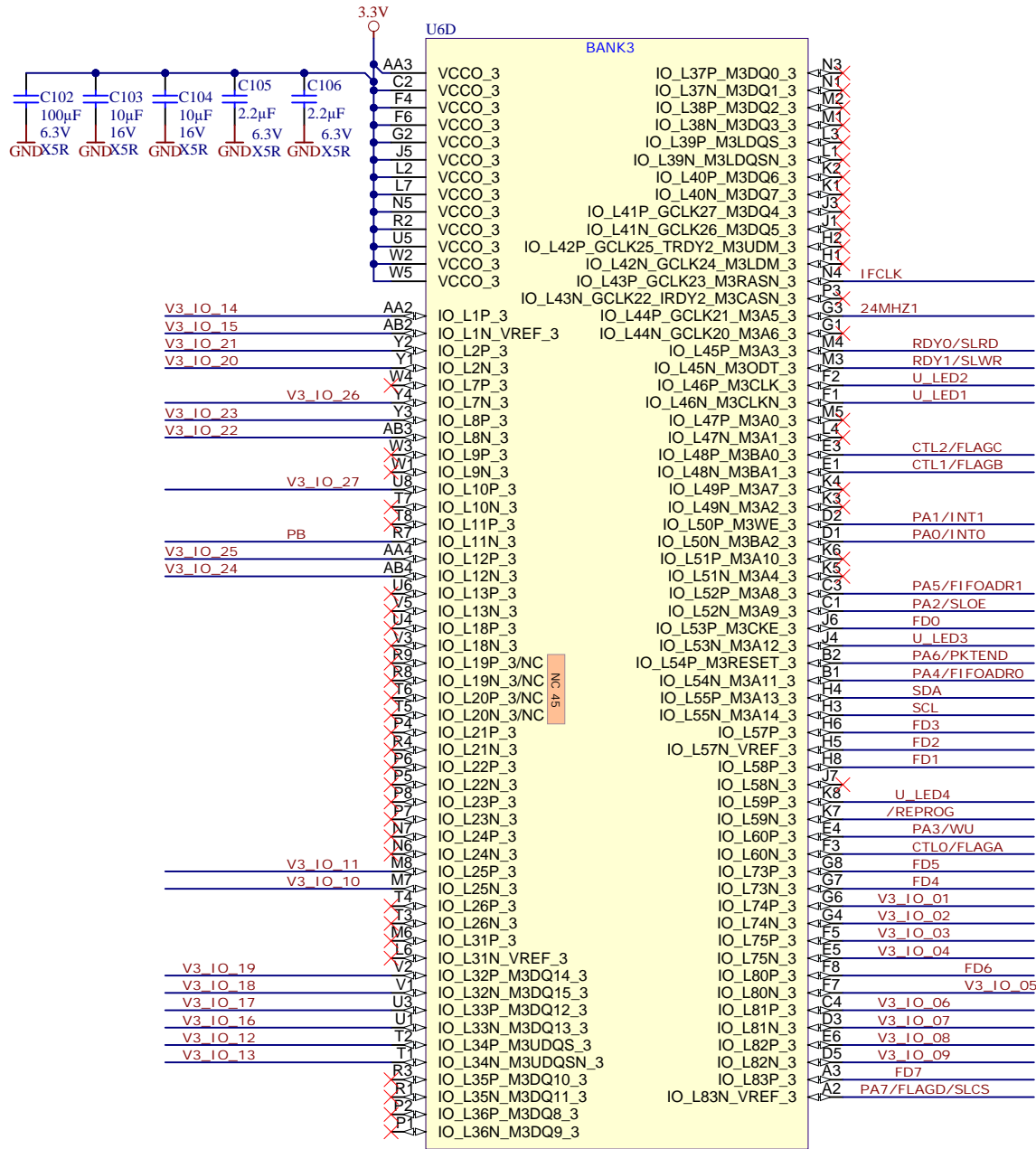
B

C

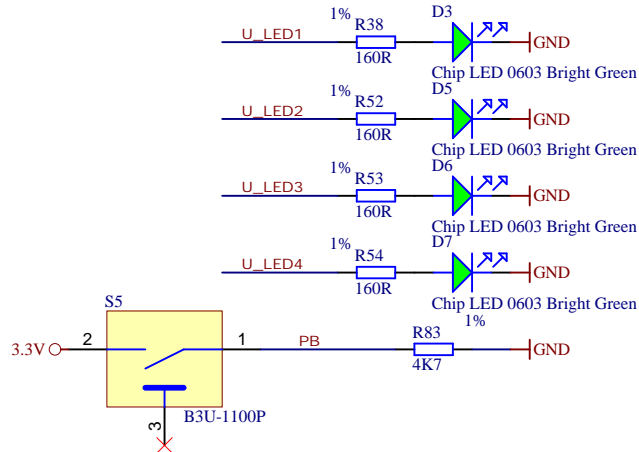
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D

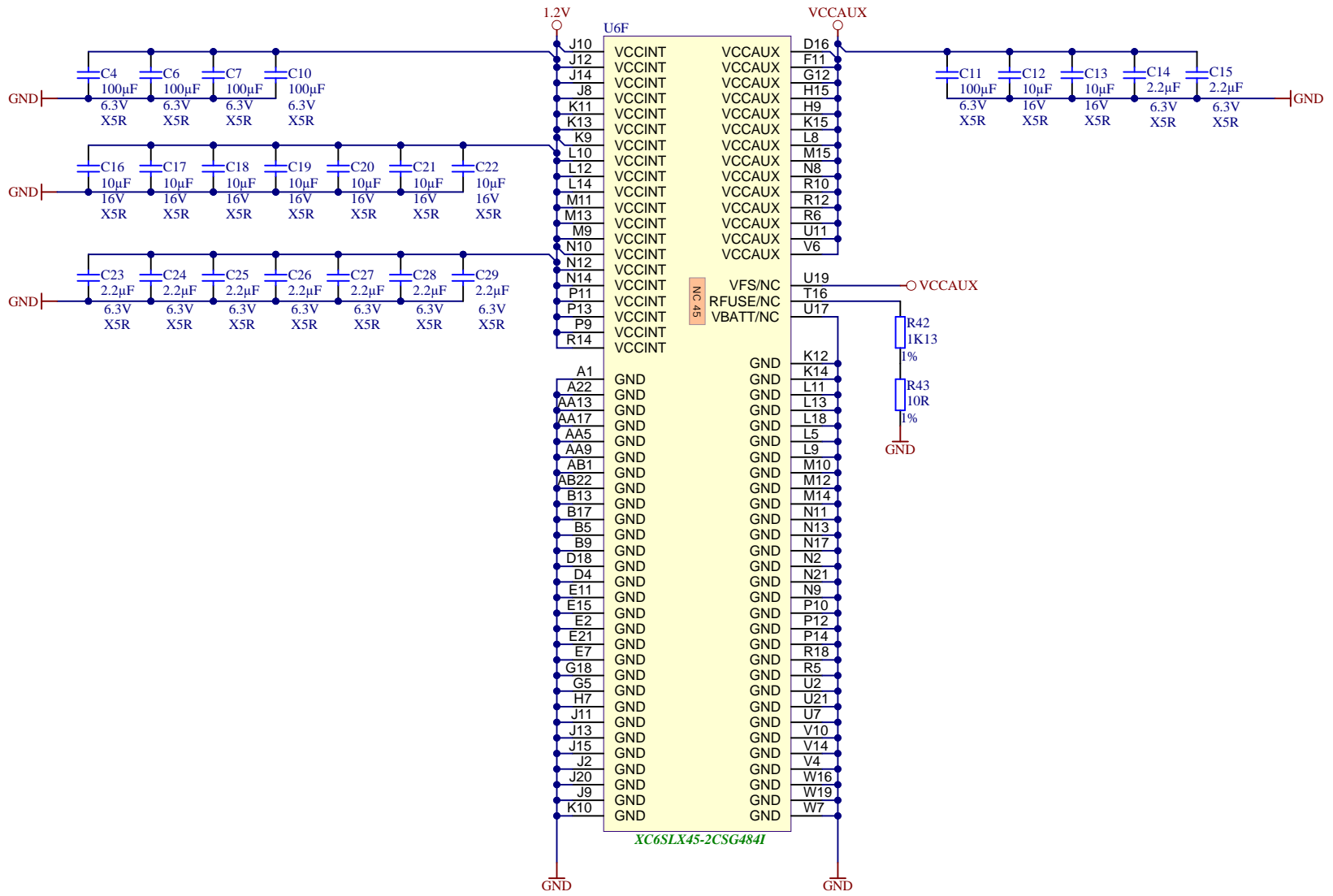
D



XC6SLX45-2CSG484I



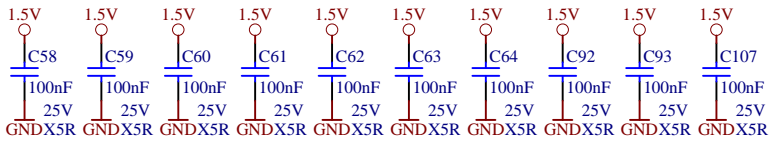
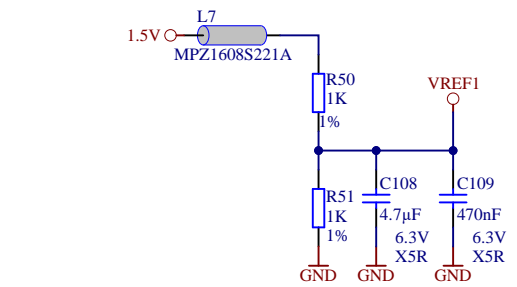
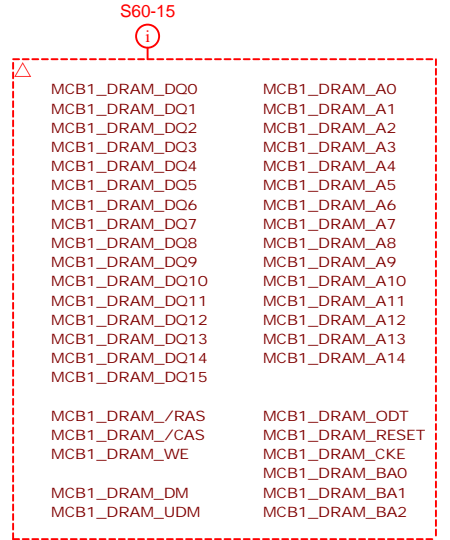
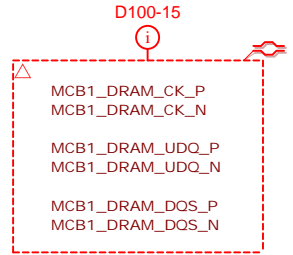
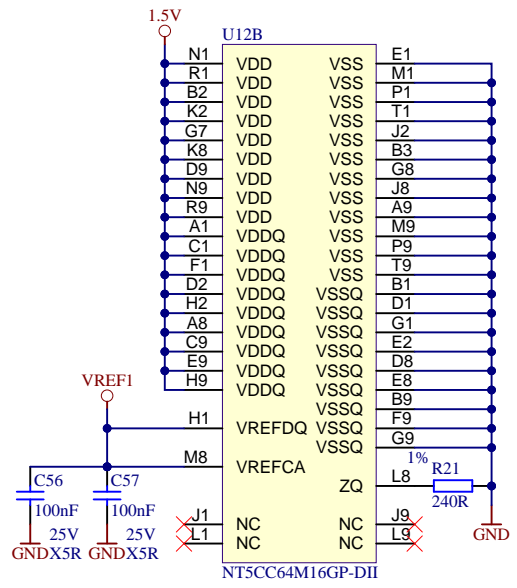
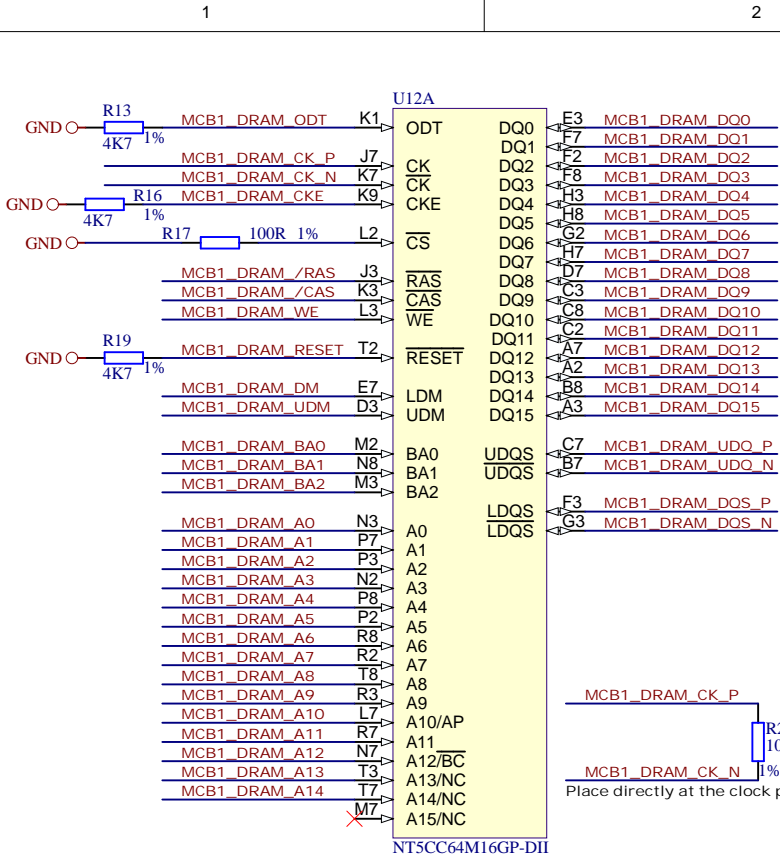
Title: TE0630 - FPGA_B3		
A4	Number: TE0630	Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page 7 of 12
Filename: FPGA_B3.SchDoc		



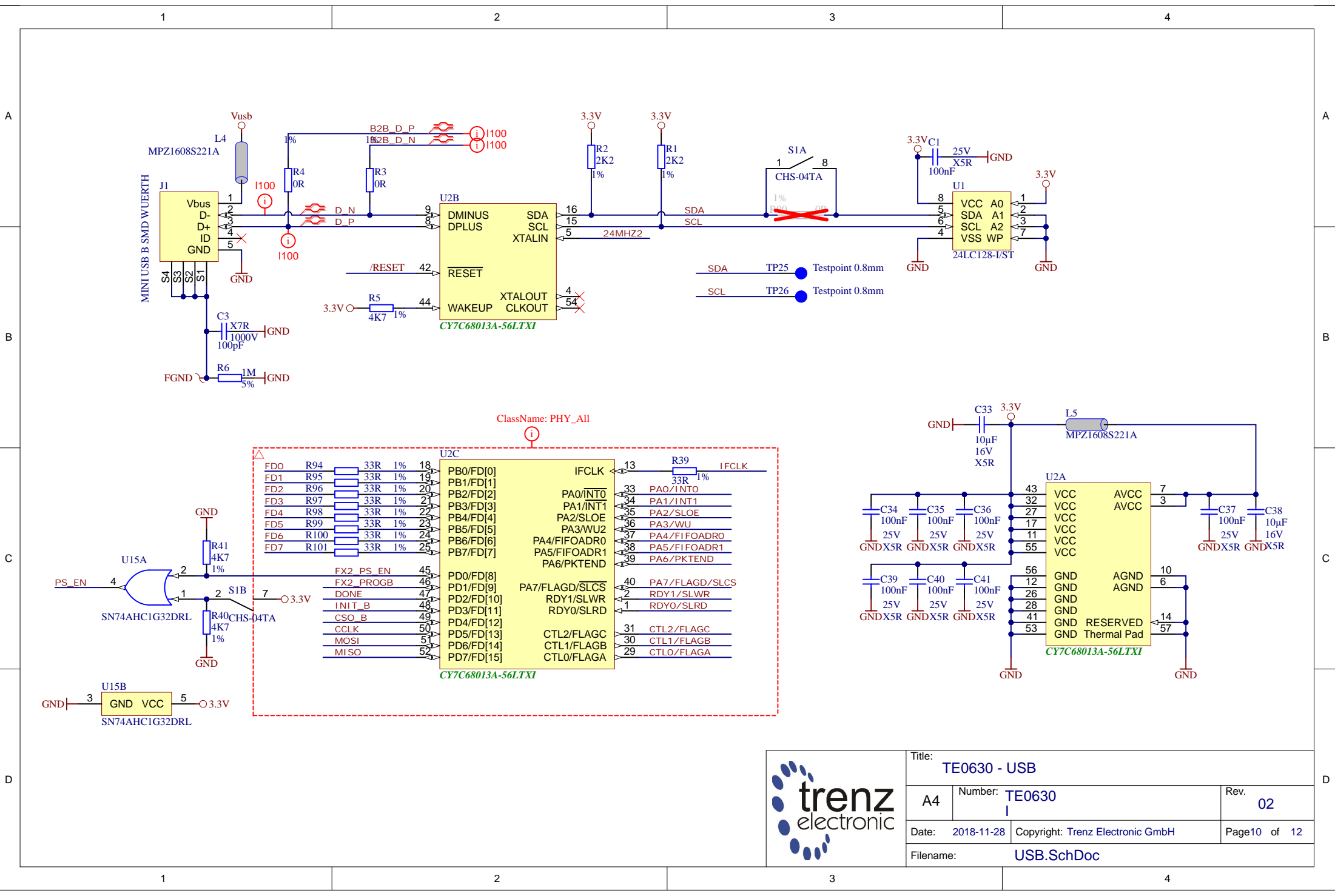
XC6SLX45-2CSG484I




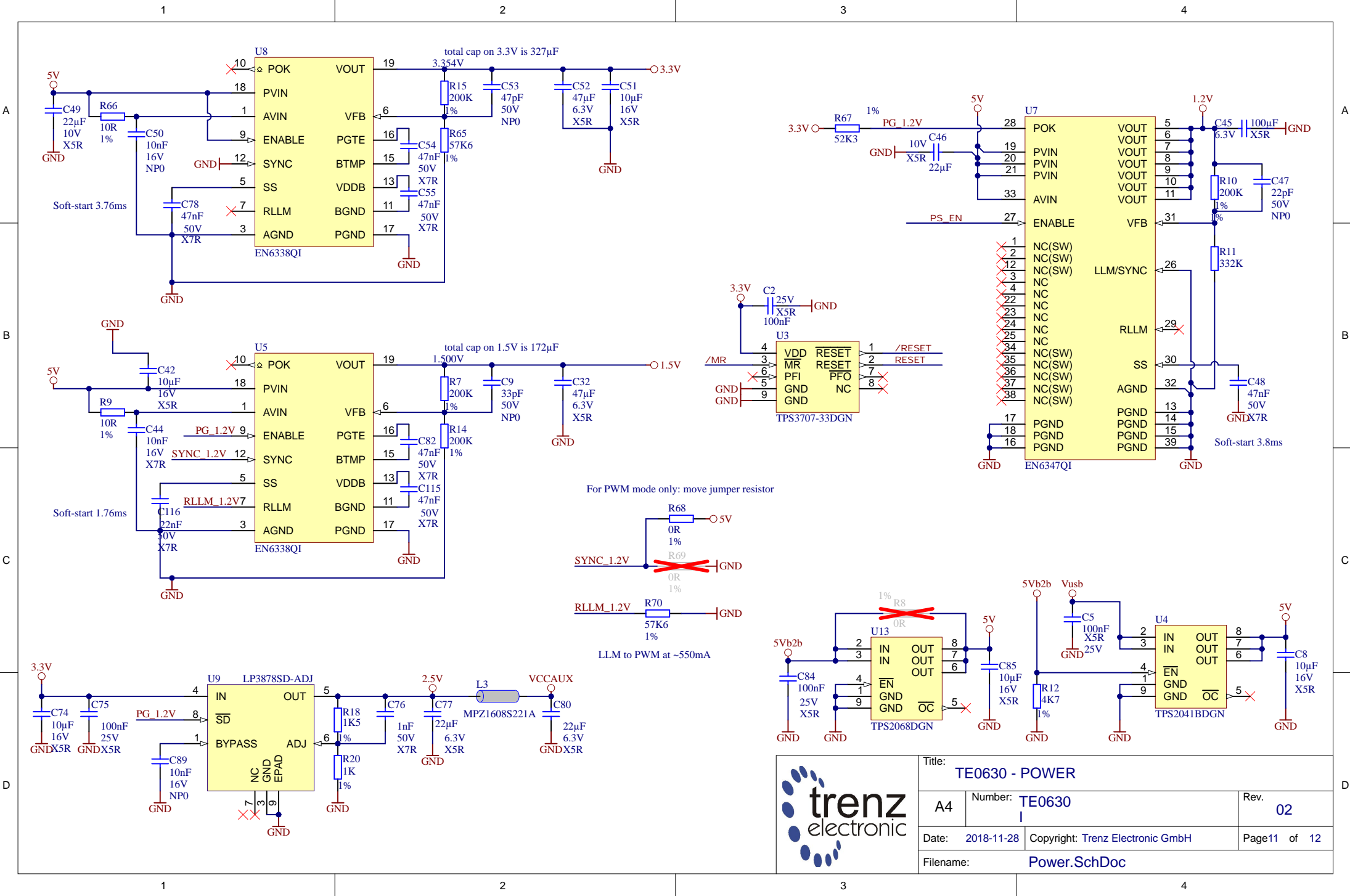
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A4	Number: TE0630	Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page8 of 12
Filename: FPGA_PWR.SchDoc		



Title: TE0630 - DDR3_RAM		
A4	Number: TE0630	Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page 9 of 12
Filename: DDR3_RAM.SchDoc		



			Title: TE0630 - USB	
			A4	Number: TE0630
Date: 2018-11-28		Copyright: Trenz Electronic GmbH		Page 10 of 12
Filename: USB.SchDoc				



Title: TE0630 - POWER		
A4	Number: TE0630	Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page 11 of 12
Filename: Power.SchDoc		

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CHANGES REV01 to REV02

- 1) Replaced U8 by EN6338QI
- 2) Rerouted nets around U8, results in new track length for:
 Signal V3_IO_06 15.2475 mm (was 15.0047mm)
 Signal V3_IO_07 16.0151 mm (was 15.0452 mm)
- 3) Replaced U5 by EN 6338QI
- 4) PS_EN now via OR gate
- 5) Replaced obsolete Diodes D1, D2 D4, by BAT54A
- 6) Fixed Footprint of U10 according to datasheet
- 7) Update from LIB
- 8) Rearranged Testpoints
- 9) Added Traceability Pad
- 10) Replaced S5 by smaller PB AN26337
- 11) Hardware revision coding updated to Rev02

CHANGES REV02

- 2020-03-30
- 1) Flash change (U14)

B


B

C

C

D

D

		Title: TE0630 - Changes list	
		A4	Number: TE0630
Date: 2018-11-28		Copyright: Trenz Electronic GmbH	
Filename: Revision_Changes.SchDoc		Page 12 of 12	

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