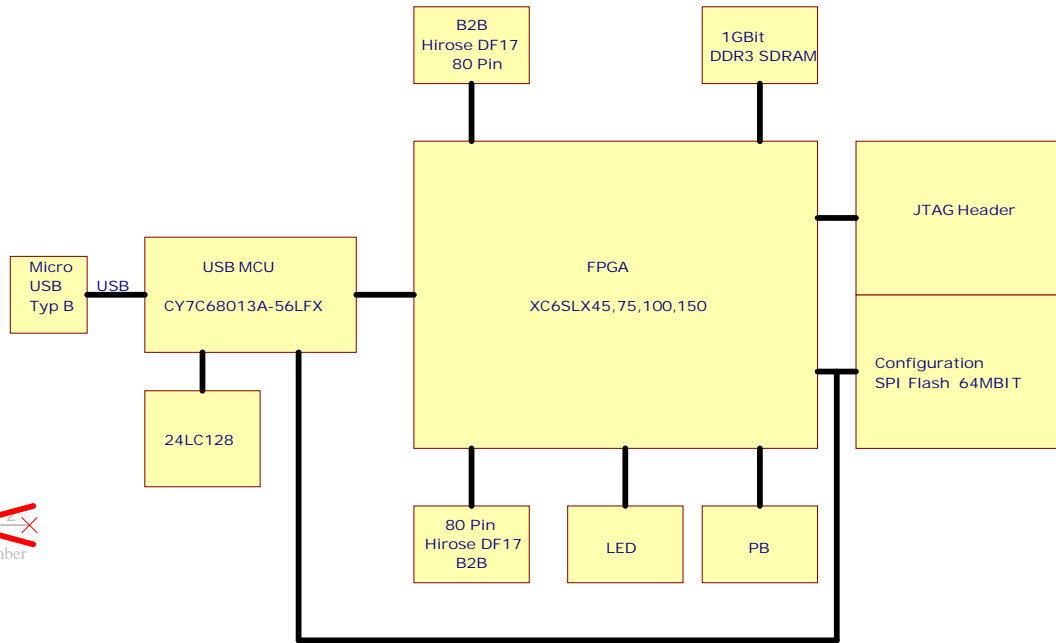


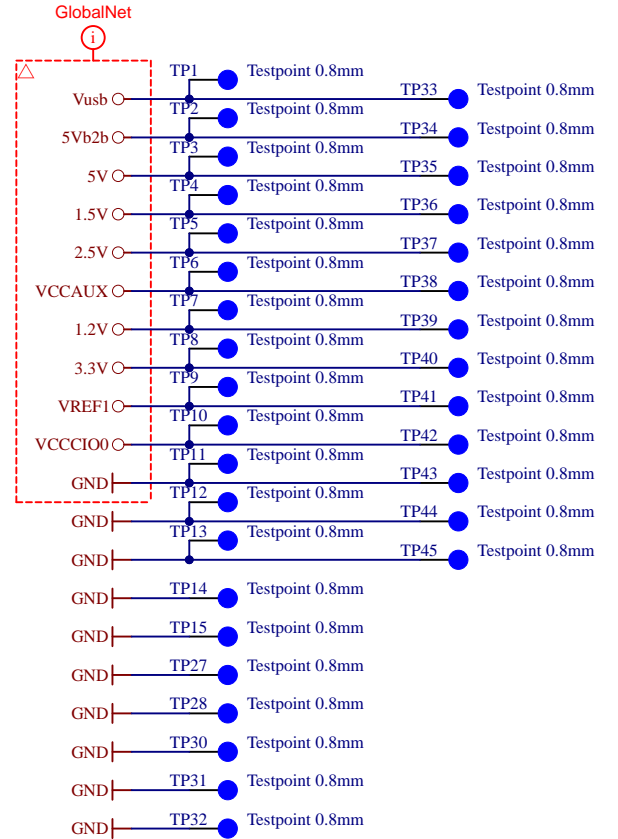
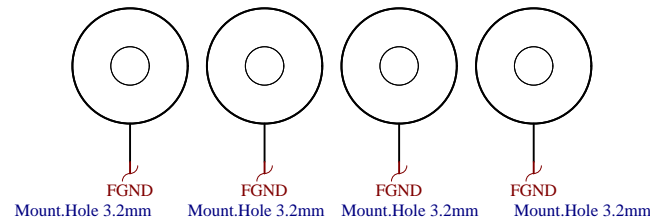
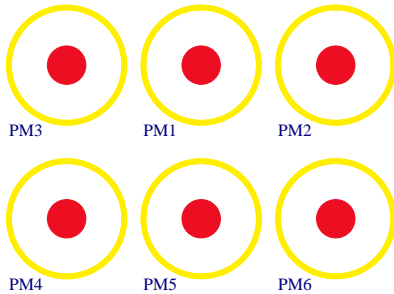
Special notes:

- U_Power
Power.SchDoc
- U_FPGA_PWR
FPGA_PWR.SchDoc
- U_DDR3_RAM
DDR3_RAM.SchDoc
- U_FPGA_CFG_CLK
FPGA_CFG_CLK.SchDoc
- U_FPGA_B3
FPGA_B3.SchDoc
- U_FPGA_DDR3
FPGA_DDR3.SchDoc
- U_FPGA_B2
FPGA_B2.SchDoc
- U_FPGA_B0
FPGA_B0.SchDoc
- U_USB
USB.SchDoc
- U_B2B_Connectors
B2B_Connectors.SchDoc



Serial
Serial
Serialnumber 6,3 x 6,3mm

~~S/N1
Serialnumber~~

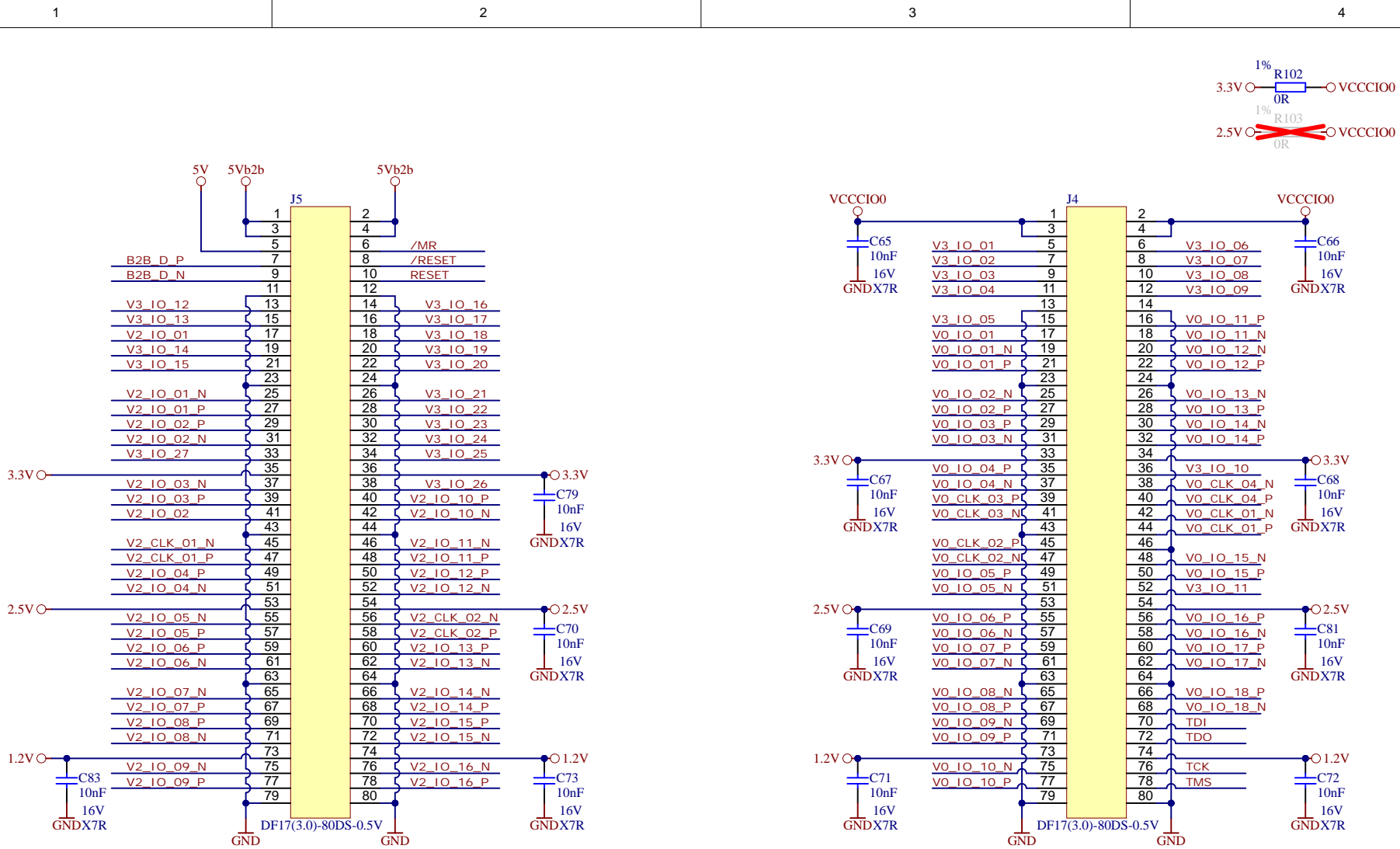


LOGO1
TE Logo PRINT Layer
LOGO PRINT

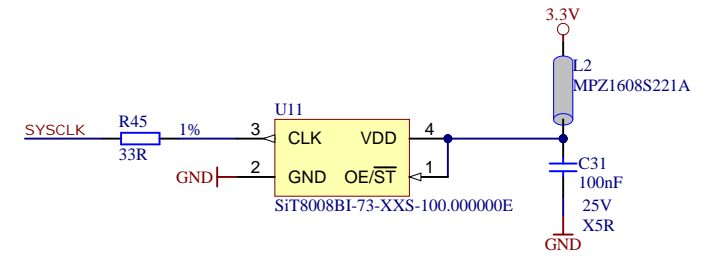
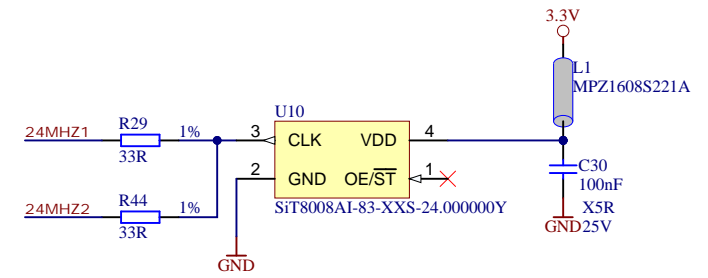
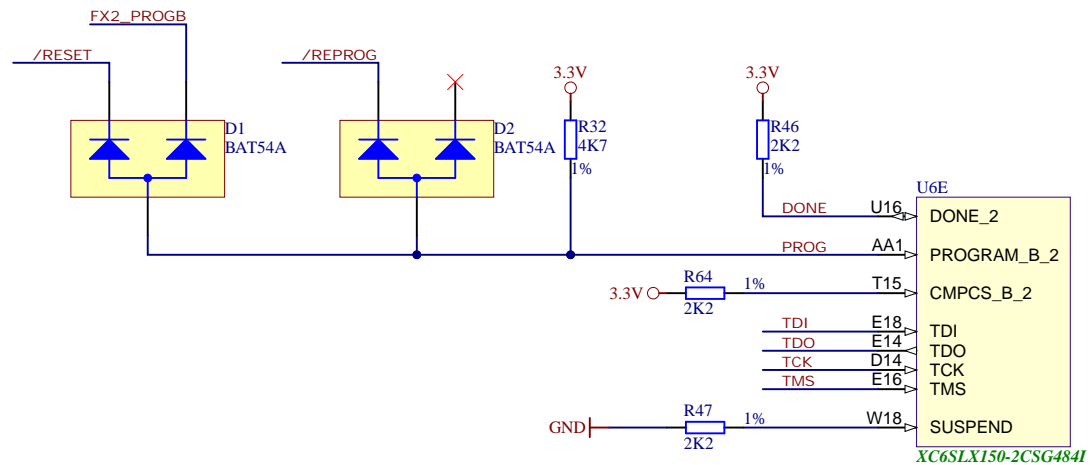
Assembly variant	IV-DWS
Created by	VY
Modified by	VY
Modified at	2020-10-19
SVN Revision	

Title: TE0630		
A4	Number: TE0630 IV-DWS	Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page1 of 12
Filename: TE0630.SchDoc		

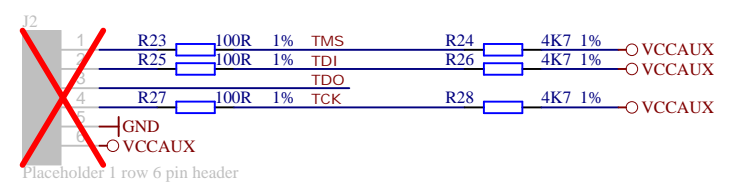




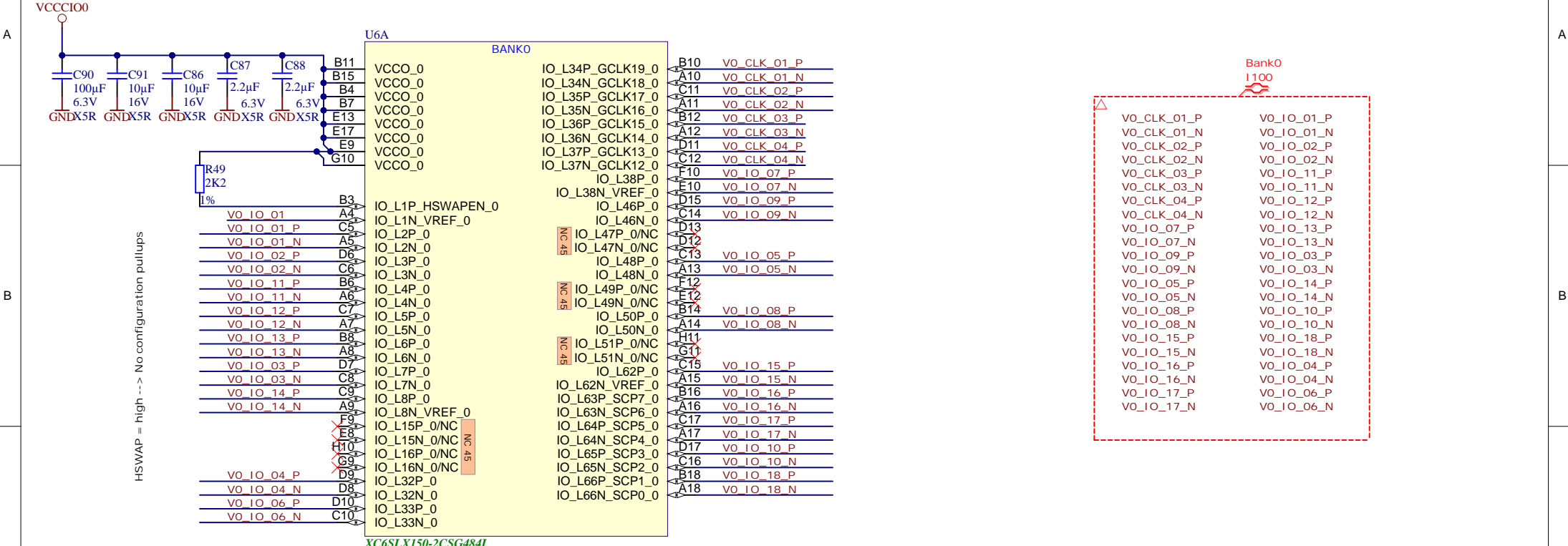

Title: TE0630 - B2B_Connectors		
A4	Number: TE0630 IV-DWS	Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH	Page2 of 12
Filename: B2B_Connectors.SchDoc		



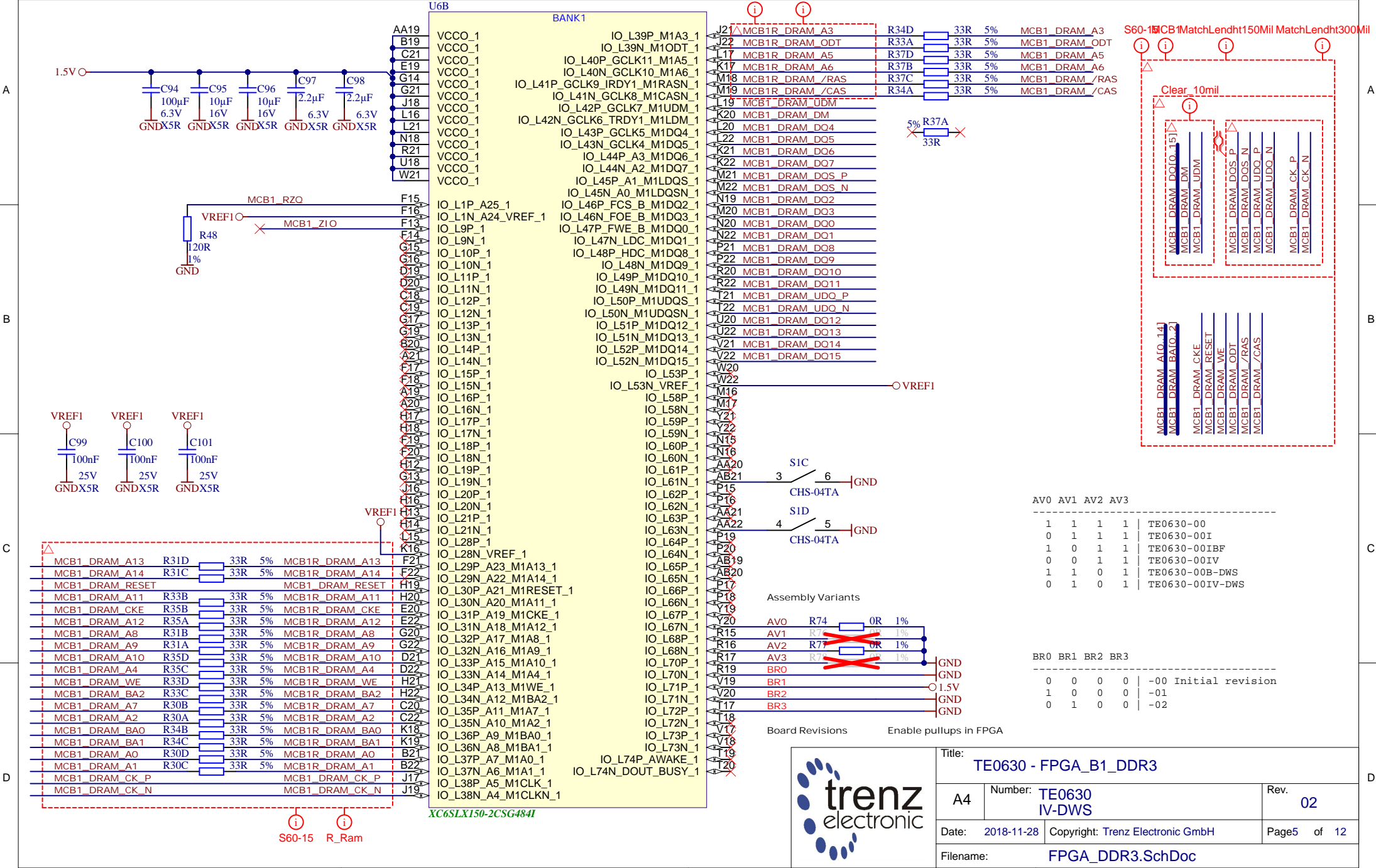
- 24MHZ1 TP22 ● Testpoint 0.8mm
- 24MHZ2 TP23 ● Testpoint 0.8mm
- SYSCLK TP24 ● Testpoint 0.8mm
- PROG TP29 ● Testpoint 0.8mm

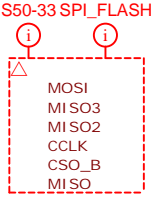
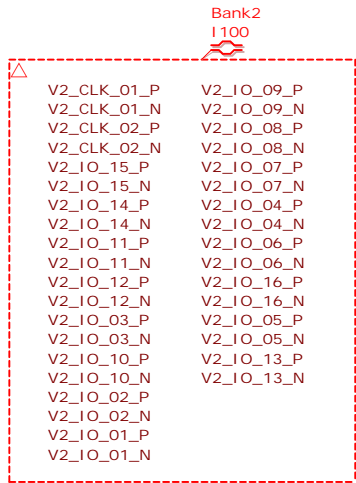
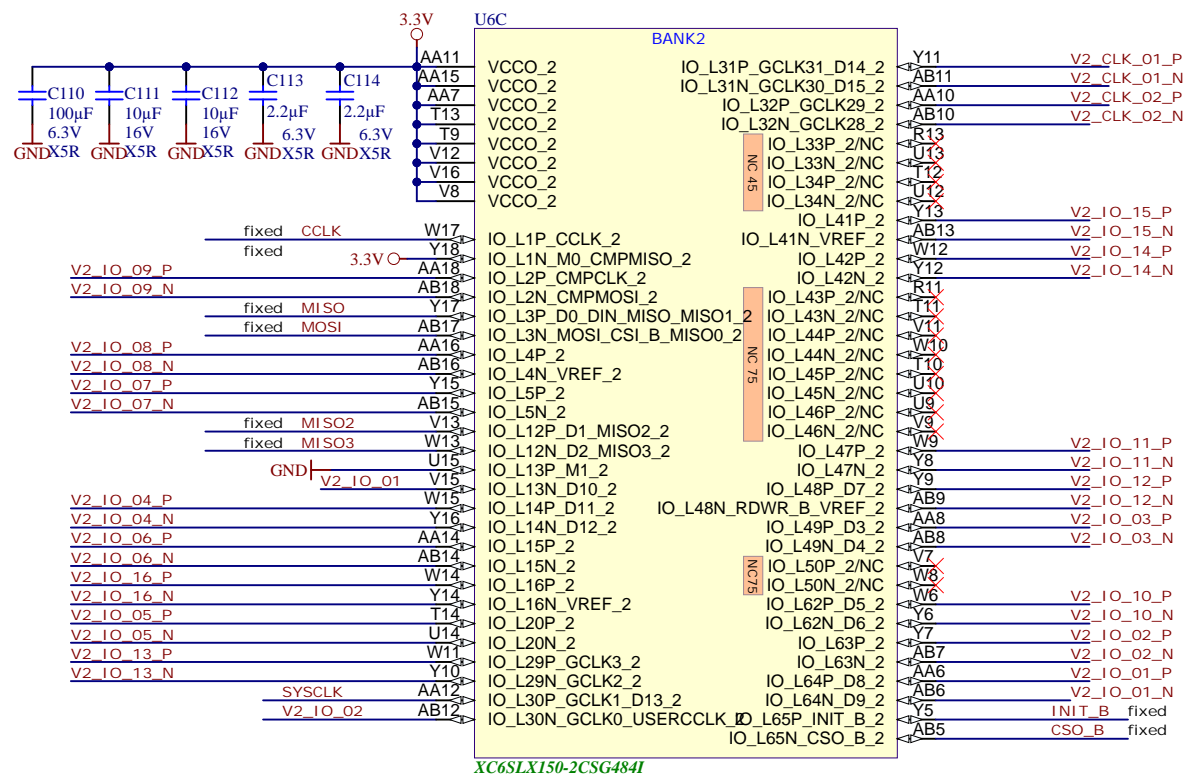


	Title: TE0630 - FPGA_CFG_CLK	
	A4	Number: TE0630 IV-DWS
	Date: 2018-11-28	Copyright: Trenz Electronic GmbH
	Filename: FPGA_CFG_CLK.SchDoc	
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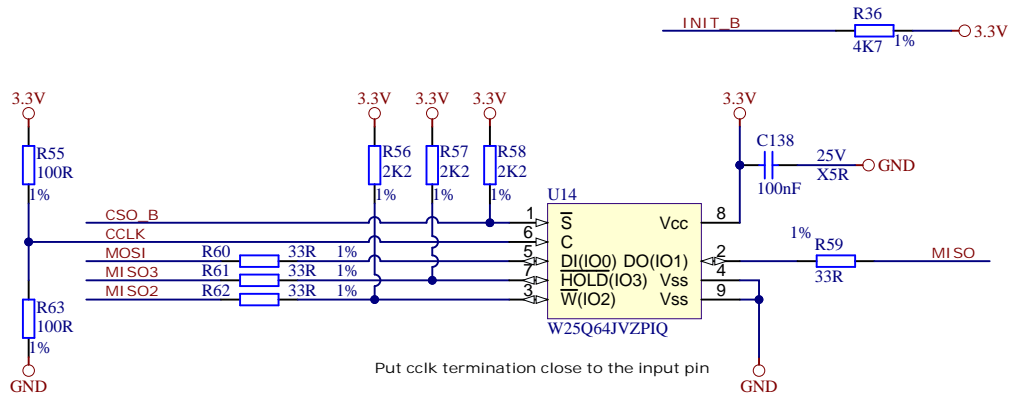



Title: TE0630 - FPGA_B0		
A4	Number: TE0630 IV-DWS	Rev. 02
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Filename: FPGA_B0.SchDoc		

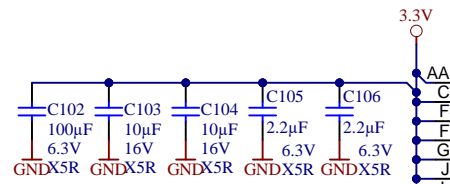




- CSO_B TP16 ● Testpoint 0.8mm
- CCLK TP17 ● Testpoint 0.8mm
- MOSI TP18 ● Testpoint 0.8mm
- MISO3 TP19 ● Testpoint 0.8mm
- MISO2 TP20 ● Testpoint 0.8mm
- MISO TP21 ● Testpoint 0.8mm

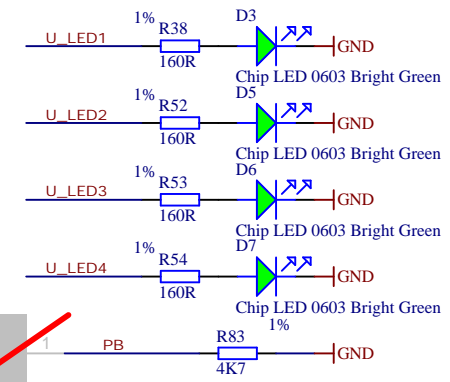
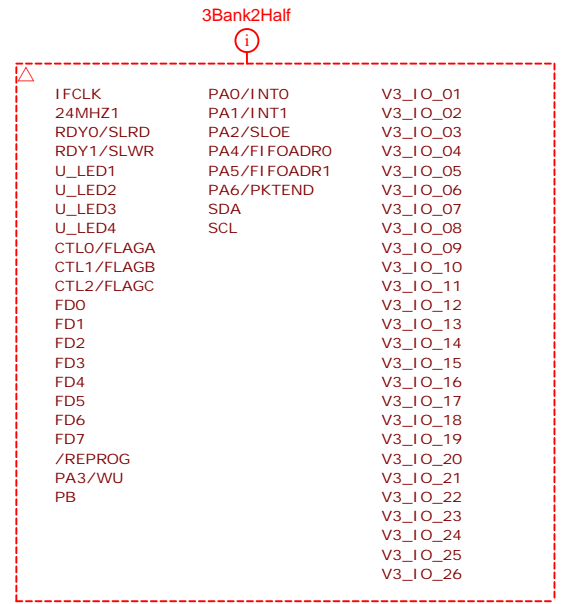


Title: TE0630 - FPGA_B2		
A4	Number: TE0630 IV-DWS	Rev. 02
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Filename: FPGA_B2.SchDoc		

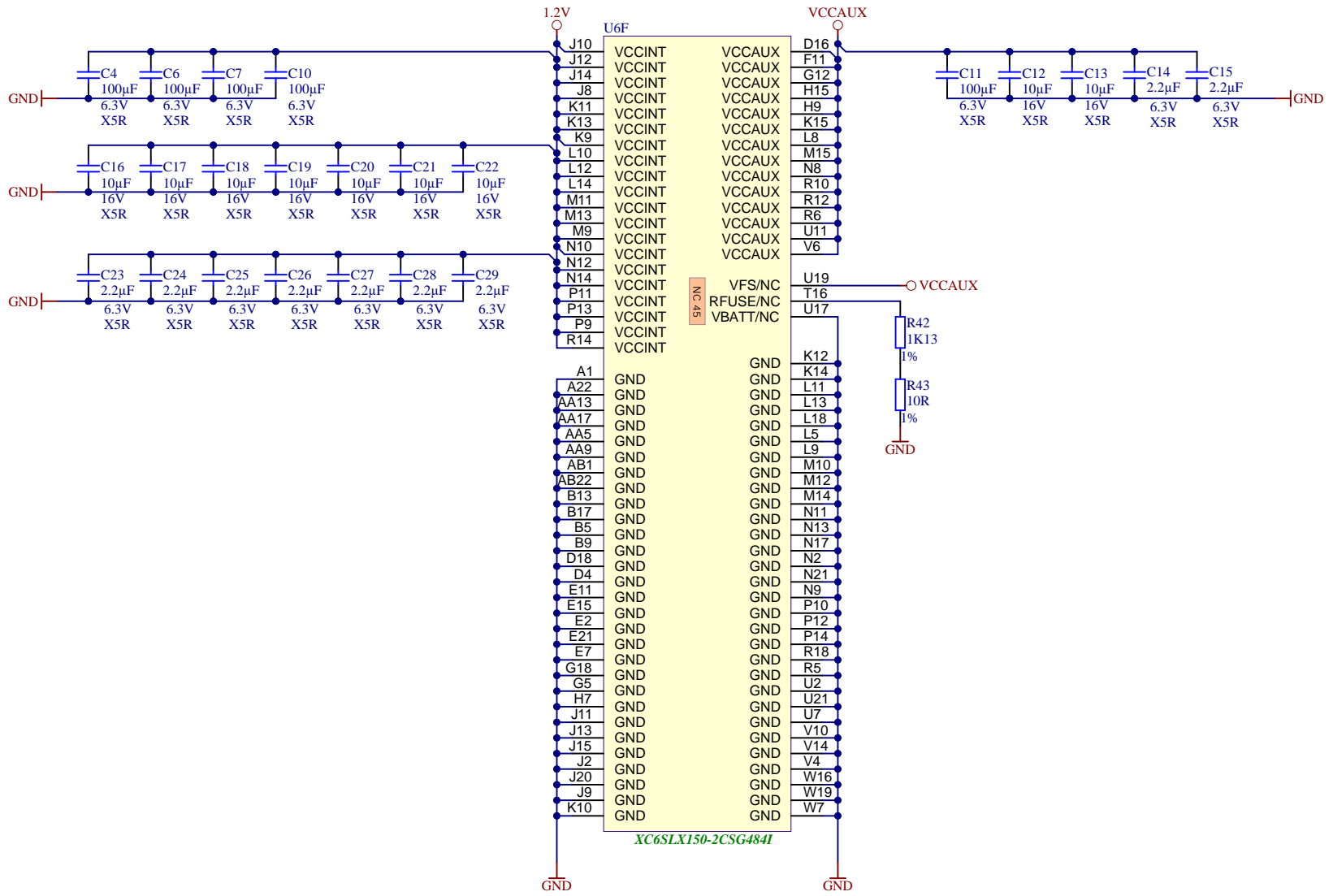


Pin	Signal	Pin	Signal
AA3	VCCO_3	N3	IFCLK
C2	VCCO_3	M1	24MHZ1
F4	VCCO_3	M2	
F6	VCCO_3	M3	RDY0/SLRD
G2	VCCO_3	M4	RDY1/SLWR
J5	VCCO_3	F2	U_LED2
L2	VCCO_3	F1	U_LED1
L7	VCCO_3	M5	
N5	VCCO_3	L4	CTL2/FLAGC
R2	VCCO_3	L1	CTL1/FLAGB
U5	VCCO_3	E3	PA1/INT1
W2	VCCO_3	D1	PA0/INT0
W5	VCCO_3	K6	
AA2	IO_L1P_3	C3	PA5/FIFOADR1
AB2	IO_L1N_VREF_3	C1	PA2/SLOE
Y2	IO_L2P_3	J6	FD0
Y1	IO_L2N_3	J4	U_LED3
Y4	IO_L7P_3	B2	PA6/PKTEND
Y3	IO_L7N_3	B1	PA4/FIFOADRO
Y2	IO_L8P_3	H4	SDA
AB3	IO_L8N_3	H3	SCL
W3	IO_L9P_3	H6	FD3
W1	IO_L9N_3	H5	FD2
U8	IO_L10P_3	H8	FD1
U7	IO_L10N_3	J7	
U8	IO_L11P_3	K8	U_LED4
R7	IO_L11N_3	K7	/REPROG
AA4	IO_L12P_3	E4	PA3/WU
AB4	IO_L12N_3	F3	CTL0/FLAGA
U6	IO_L13P_3	G8	FD5
U5	IO_L13N_3	G7	FD4
U4	IO_L18P_3	G6	V3_IO_01
U3	IO_L18N_3	G4	V3_IO_02
R9	IO_L19P_3/NC	F5	V3_IO_03
R8	IO_L19N_3/NC	F5	V3_IO_04
T6	IO_L20P_3/NC	F8	FD6
T5	IO_L20N_3/NC	F7	V3_IO_05
P4	IO_L21P_3	C4	V3_IO_06
R4	IO_L21N_3	D3	V3_IO_07
P6	IO_L22P_3	E6	V3_IO_08
P5	IO_L22N_3	D5	V3_IO_09
P8	IO_L23P_3	A3	FD7
P7	IO_L23N_3	A2	PA7/FLAGD/SLCS
N7	IO_L24P_3		
N6	IO_L24N_3		
M8	IO_L24P_3		
M7	IO_L25P_3		
T4	IO_L25N_3		
T3	IO_L26P_3		
M6	IO_L26N_3		
L6	IO_L31P_3		
V2	IO_L31N_VREF_3		
V1	IO_L32P_M3DQ14_3		
V1	IO_L32N_M3DQ15_3		
U3	IO_L33P_M3DQ12_3		
U1	IO_L33N_M3DQ13_3		
T2	IO_L34P_M3UDQS_3		
T1	IO_L34N_M3UDQSN_3		
R3	IO_L35P_M3DQ10_3		
R1	IO_L35N_M3DQ11_3		
P2	IO_L36P_M3DQ8_3		
P1	IO_L36N_M3DQ9_3		
	IO_L37P_M3DQ0_3		
	IO_L37N_M3DQ1_3		
	IO_L38P_M3DQ2_3		
	IO_L38N_M3DQ3_3		
	IO_L39P_M3LDQS_3		
	IO_L39N_M3LDQSN_3		
	IO_L40P_M3DQ6_3		
	IO_L40N_M3DQ7_3		
	IO_L41P_GCLK27_M3DQ4_3		
	IO_L41N_GCLK26_M3DQ5_3		
	IO_L42P_GCLK25_TRDY2_M3UDM_3		
	IO_L42N_GCLK24_M3LDM_3		
	IO_L43P_GCLK23_M3RASN_3		
	IO_L43N_GCLK22_IRDY2_M3CASN_3		
	IO_L44P_GCLK21_M3A5_3		
	IO_L44N_GCLK20_M3A6_3		
	IO_L45P_M3A3_3		
	IO_L45N_M3ODT_3		
	IO_L46P_M3CLK_3		
	IO_L46N_M3CLKN_3		
	IO_L47P_M3A0_3		
	IO_L47N_M3A1_3		
	IO_L48P_M3BA0_3		
	IO_L48N_M3BA1_3		
	IO_L49P_M3A7_3		
	IO_L49N_M3A2_3		
	IO_L50P_M3WE_3		
	IO_L50N_M3BA2_3		
	IO_L51P_M3A10_3		
	IO_L51N_M3A4_3		
	IO_L52P_M3A8_3		
	IO_L52N_M3A9_3		
	IO_L53P_M3CKE_3		
	IO_L53N_M3A12_3		
	IO_L54P_M3RESET_3		
	IO_L54N_M3A11_3		
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	IO_L55N_M3A14_3		
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	IO_L80P_3		
	IO_L80N_3		
	IO_L81P_3		
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	IO_L82P_3		
	IO_L82N_3		
	IO_L83P_3		
	IO_L83N_VREF_3		

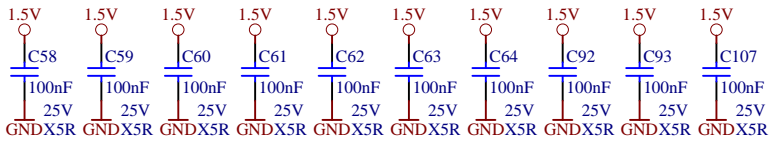
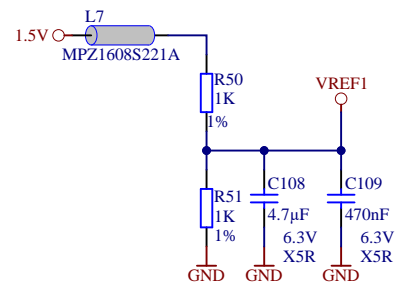
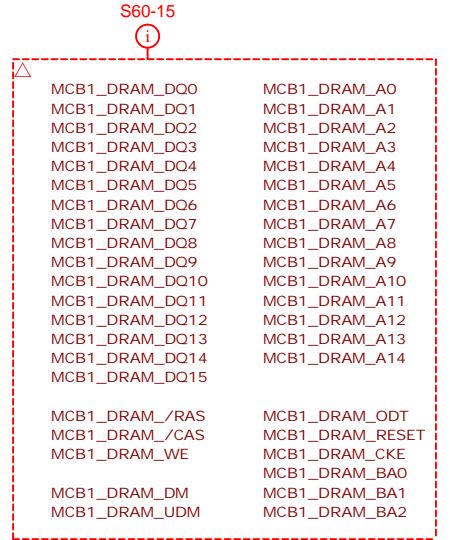
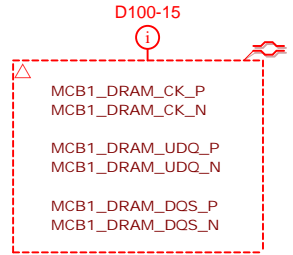
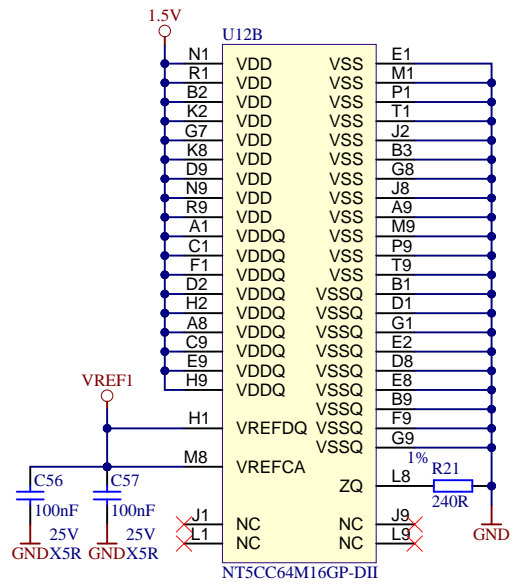
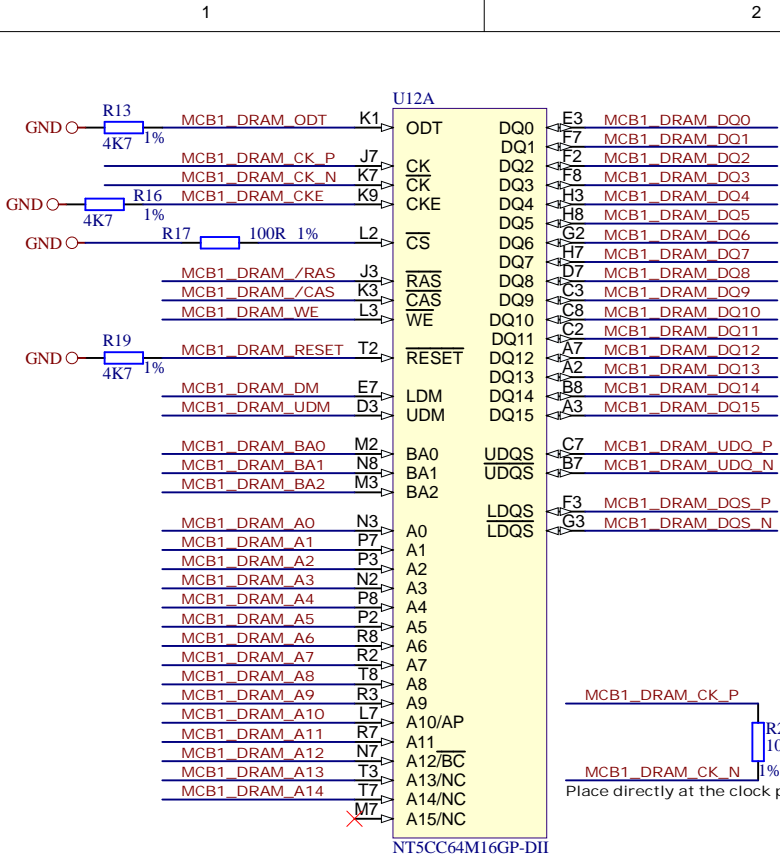
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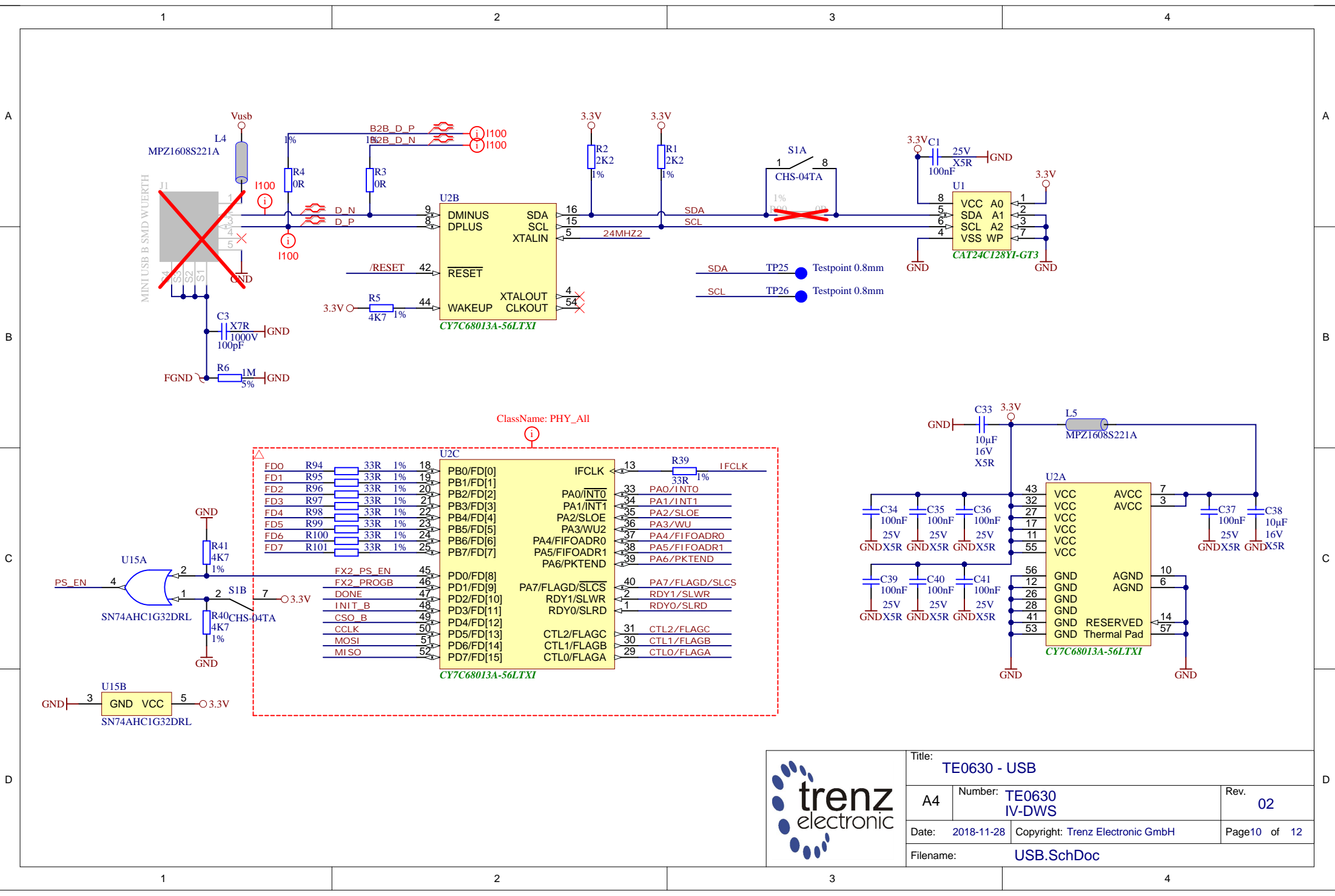
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A4	Number: TE0630 IV-DWS	Rev. 02
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Filename: FPGA_B3.SchDoc		



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A4	Number: TE0630 IV-DWS	Rev. 02
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Filename: FPGA_PWR.SchDoc		



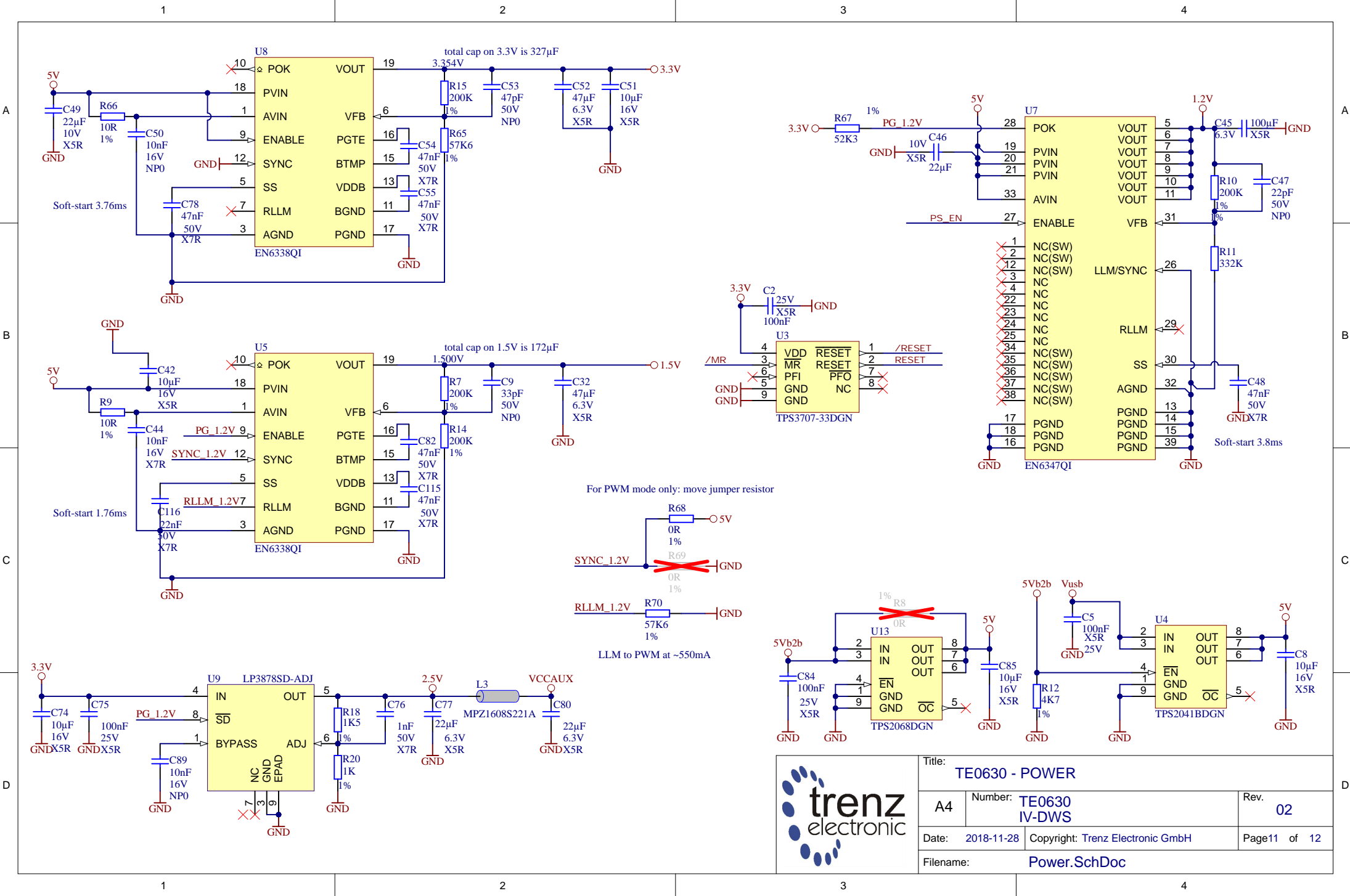
Title: TE0630 - DDR3_RAM		
A4	Number: TE0630 IV-DWS	Rev. 02
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Filename: DDR3_RAM.SchDoc		



ClassName: PHY_All



Title: TE0630 - USB		
A4	Number: TE0630 IV-DWS	Rev. 02
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Filename: USB.SchDoc		



Title: TE0630 - POWER		
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Filename: Power.SchDoc		

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A

A

CHANGES REV01 to REV02

- 1) Replaced U8 by EN6338QI
- 2) Rerouted nets around U8, results in new track length for:
 Signal V3_IO_06 15.2475 mm (was 15.0047mm)
 Signal V3_IO_07 16.0151 mm (was 15.0452 mm)
- 3) Replaced U5 by EN 6338QI
- 4) PS_EN now via OR gate
- 5) Replaced obsolete Diodes D1, D2 D4, by BAT54A
- 6) Fixed Footprint of U10 according to datasheet
- 7) Update from LIB
- 8) Rearranged Testpoints
- 9) Added Traceability Pad
- 10) Replaced S5 by smaller PB AN26337
- 11) Hardware revision coding updated to Rev02

CHANGES REV02

- 2020-03-30
- 1) Flash change (U14)

B


B

C

C

D

D

	Title: TE0630 - Changes list		
	A4	Number: TE0630 IV-DWS	Rev. 02
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	Filename: Revision_Changes.SchDoc		

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