U_Power
Power.SchDoc

U_FPGA_PWR
FPGA_PWR.SchDoc

U_DDR3_RAM
DDR3_RAM.SchDoc

U_FPGA_CFG_CLK
FPGA_CFG_CLK.SchDoc

U_FPGA_B3
FPGA_B3.SchDoc

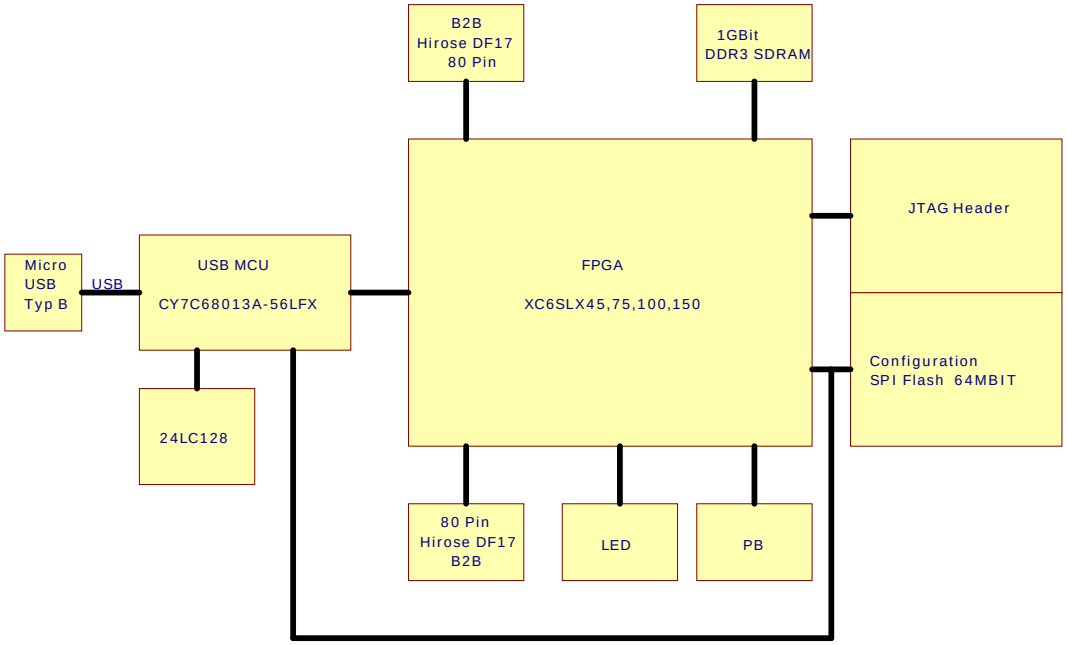
U_FPGA_DDR3
FPGA_DDR3.SchDoc

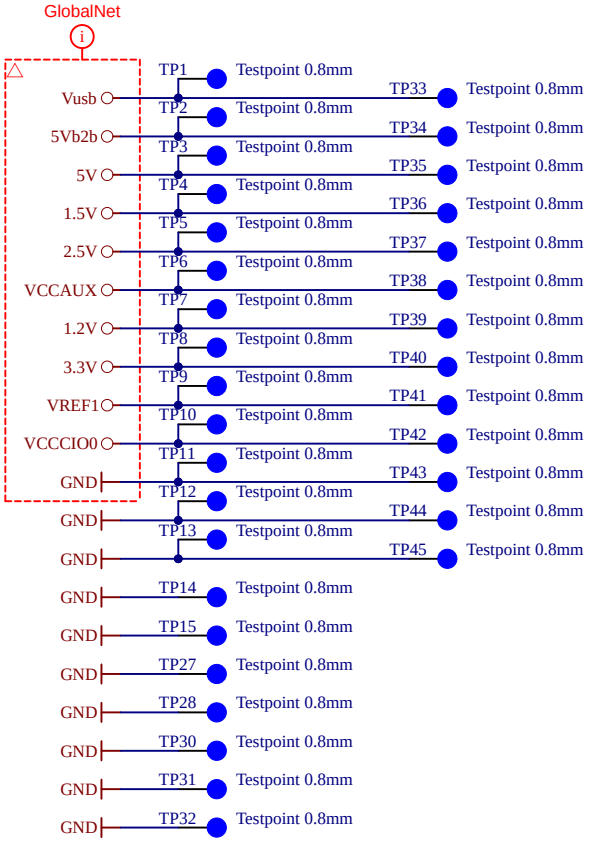
U_FPGA_B2
FPGA_B2.SchDoc

U_FPGA_B0
FPGA_B0.SchDoc

U_USB
USB.SchDoc

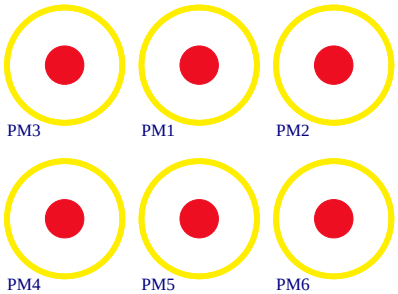
U_B2B_Connectors
B2B_Connectors.SchDoc

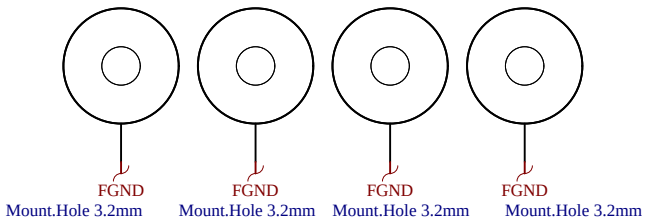




Serial
Serial
Serialnumber 6,3 x 6.3mm

LOGO1
TE Logo PRINT Layer
LOGO PRINT





Assembly variant	IV
Created by	na
Modified by	MR
Modified at	2020-03-30
SVN Revision	9220

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Title: TE0630		
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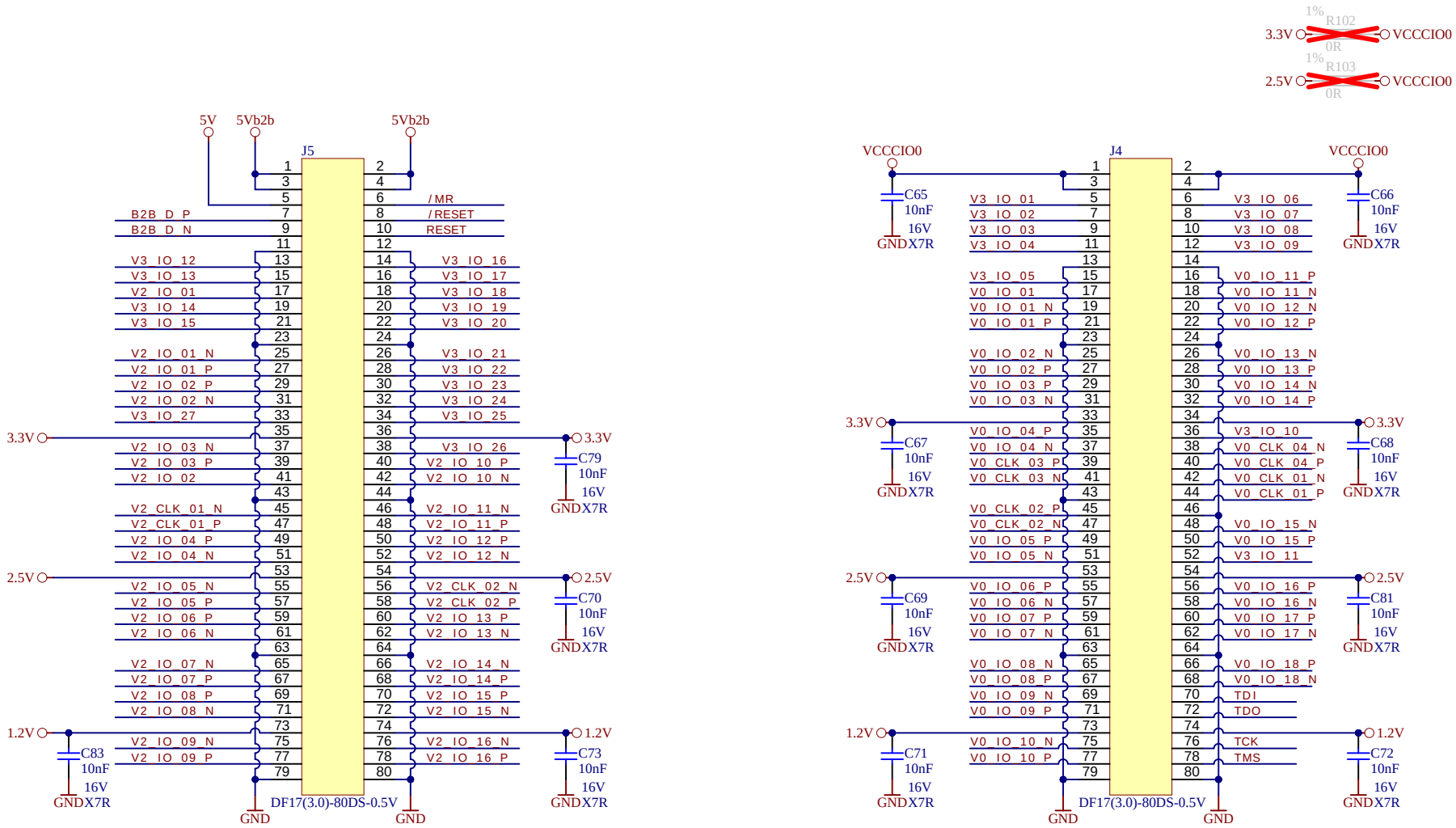
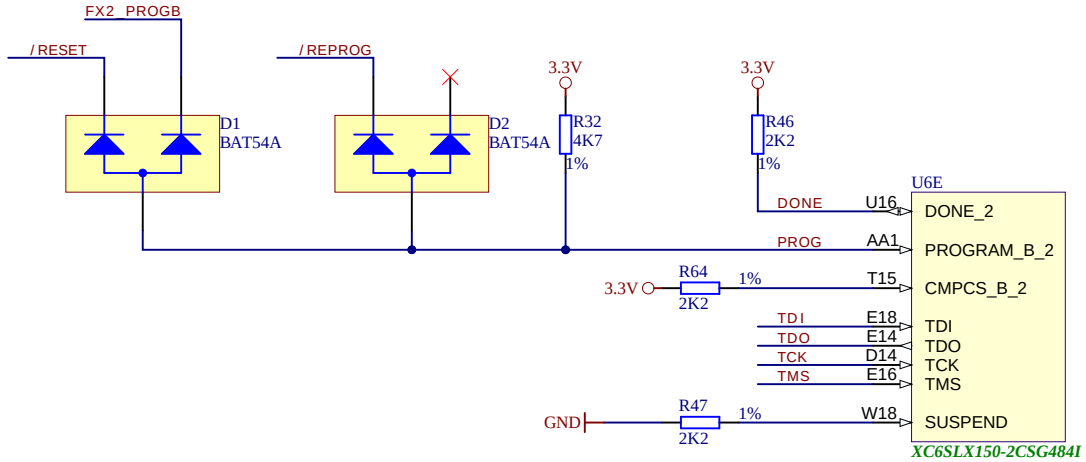
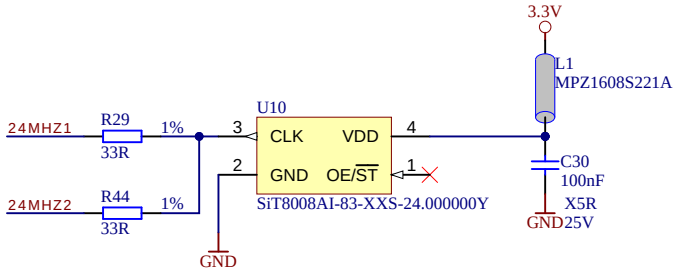
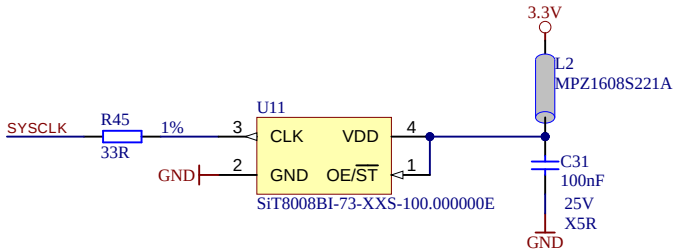
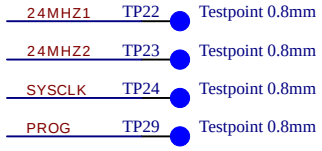


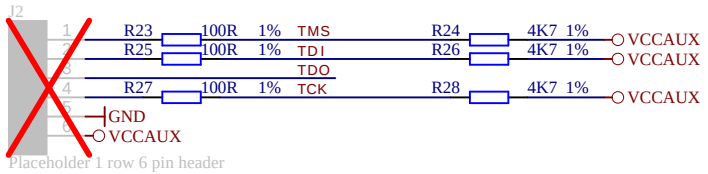
Title: TE0630 - B2B_Connectors			
A4	Number: TE0630 IV		Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH		Page2 of 12
Filename: B2B_Connectors.SchDoc			











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Title: TE0630 - FPGA_CFG_CLK		
A4	Number: TE0630 IV	Rev. 02
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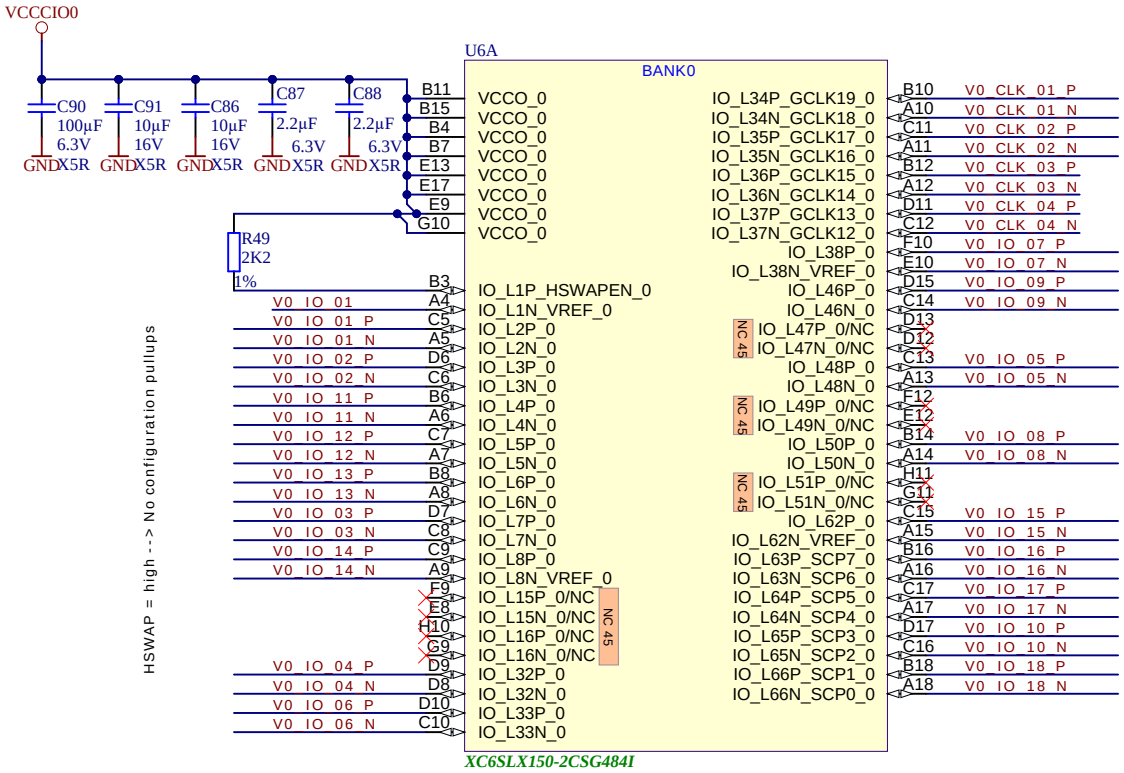

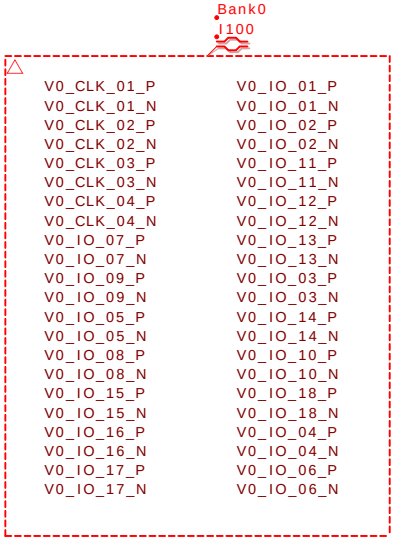

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Title: TE0630 - FPGA_B0			
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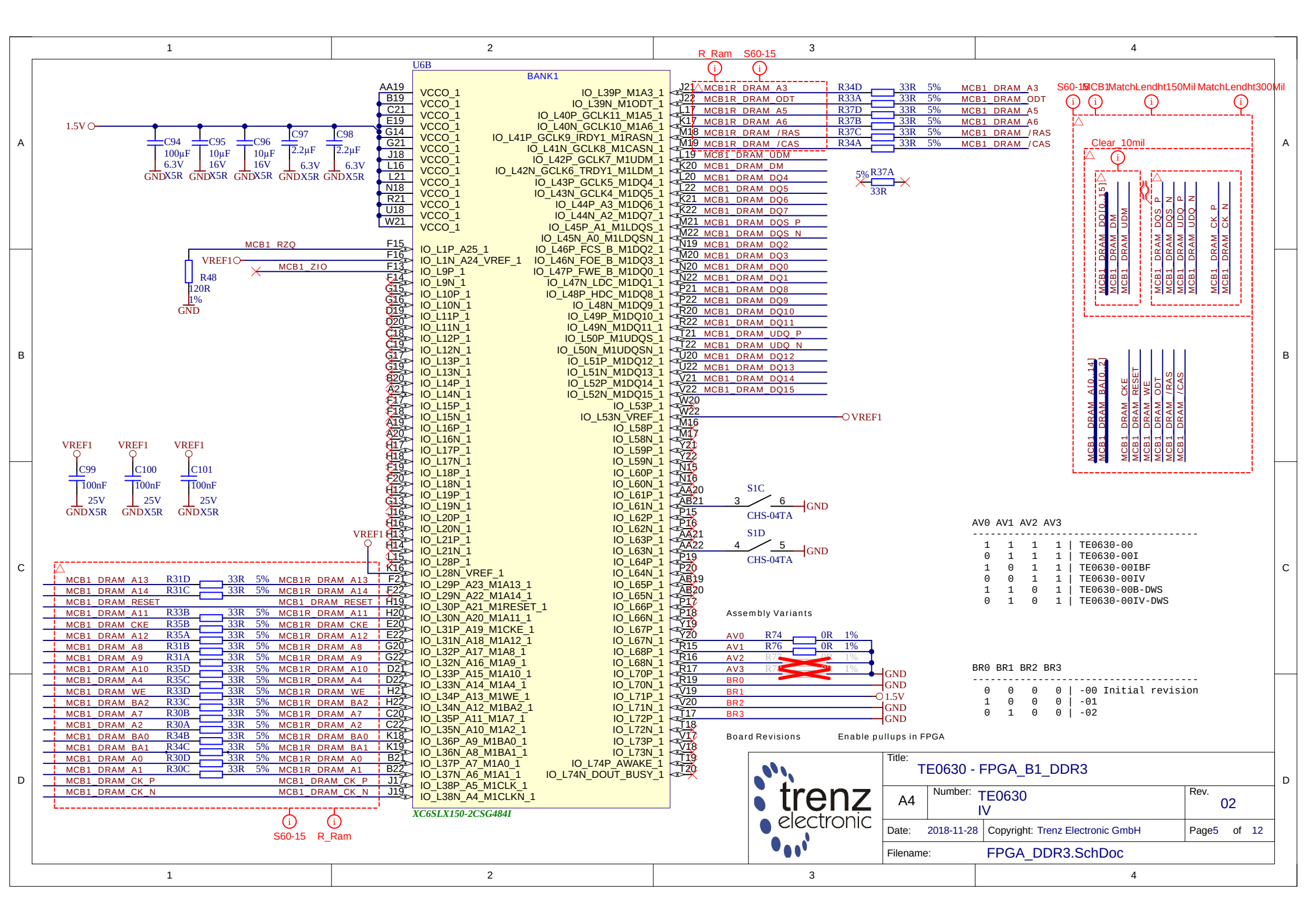
Filename: FPGA_B0.SchDoc			


U6B
BANK1
XC6SLX150-2CSG484I
1.5V
VREF1
MCB1_RZQ
MCB1_ZIO
R48
120R
1%
GND
C94 100µF 6.3V X5R
C95 10µF 16V X5R
C96 10µF 16V X5R
C97 2.2µF 6.3V X5R
C98 2.2µF 6.3V X5R
C99 100nF 25V X5R
C100 100nF 25V X5R
C101 100nF 25V X5R
R_Ram
S60-15
MCB1_DRAM_A3
MCB1_DRAM_ODT
MCB1_DRAM_A5
MCB1_DRAM_A6
MCB1_DRAM_/RAS
MCB1_DRAM_/CAS
R34D
R33A
R37D
R37B
R37C
R34A
33R 5%
R37A
MCB1_DRAM_UDM
MCB1_DRAM_DM
MCB1_DRAM_DQ4
MCB1_DRAM_DQ5
MCB1_DRAM_DQ6
MCB1_DRAM_DQ7
MCB1_DRAM_DQS_P
MCB1_DRAM_DQS_N
MCB1_DRAM_DQ2
MCB1_DRAM_DQ3
MCB1_DRAM_DQ0
MCB1_DRAM_DQ1
MCB1_DRAM_DQ8
MCB1_DRAM_DQ9
MCB1_DRAM_DQ10
MCB1_DRAM_DQ11
MCB1_DRAM_UDQ_P
MCB1_DRAM_UDQ_N
MCB1_DRAM_DQ12
MCB1_DRAM_DQ13
MCB1_DRAM_DQ14
MCB1_DRAM_DQ15
VREF1
S1C
S1D
CHS-04TA
GND
MCB1_DRAM_A13
MCB1_DRAM_A14
MCB1_DRAM_RESET
MCB1_DRAM_A11
MCB1_DRAM_CKE
MCB1_DRAM_A12
MCB1_DRAM_A8
MCB1_DRAM_A9
MCB1_DRAM_A10
MCB1_DRAM_A4
MCB1_DRAM_WE
MCB1_DRAM_BA2
MCB1_DRAM_A7
MCB1_DRAM_A2
MCB1_DRAM_BA0
MCB1_DRAM_BA1
MCB1_DRAM_A0
MCB1_DRAM_A1
MCB1_DRAM_CK_P
MCB1_DRAM_CK_N
MCB1Match
Lendht150Mil
MatchLendht300Mil
Clear_10mil
MCB1_DRAM_DQ[0..15]
MCB1_DRAM_A[0..14]
MCB1_DRAM_BA[0..2]
MCB1_DRAM_CKE
MCB1_DRAM_RESET
MCB1_DRAM_WE
MCB1_DRAM_ODT
MCB1_DRAM_/RAS
MCB1_DRAM_/CAS
Assembly Variants
AV0 R74 0R 1%
AV1 R76 0R 1%
AV2 R78 0R 1%
AV3 R79 0R 1%
BR0
BR1
BR2
BR3
1.5V
Board Revisions
Enable pullups in FPGA
AV0 AV1 AV2 AV3
1 1 1 1 | TE0630-00
0 1 1 1 | TE0630-00I
1 0 1 1 | TE0630-00IBF
0 0 1 1 | TE0630-00IV
1 1 0 1 | TE0630-00B-DWS
0 1 0 1 | TE0630-00IV-DWS
BR0 BR1 BR2 BR3
0 0 0 0 | -00 Initial revision
1 0 0 0 | -01
0 1 0 0 | -02
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Title: TE0630 - FPGA_B1_DDR3
A4
Number: TE0630 IV
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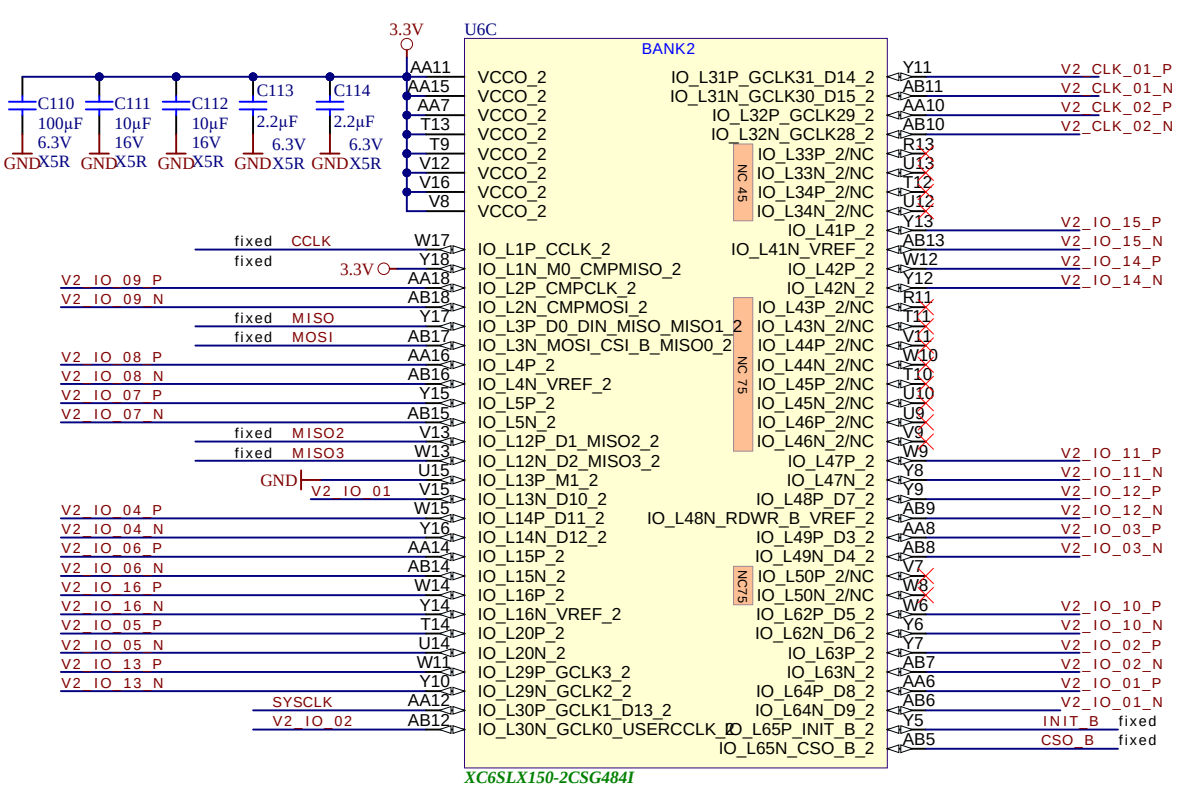
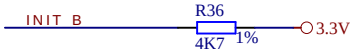
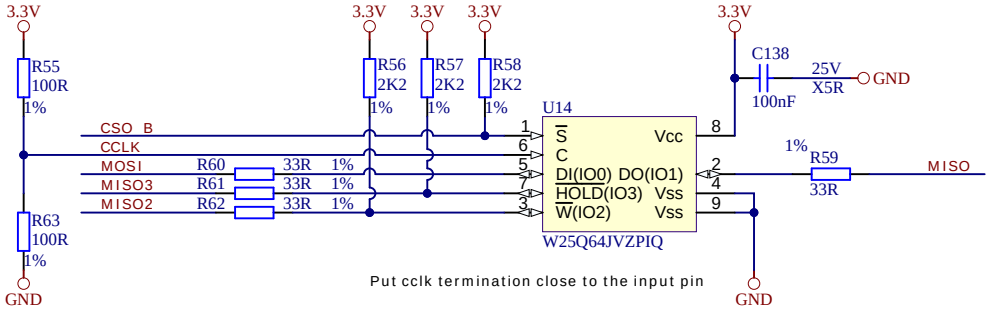
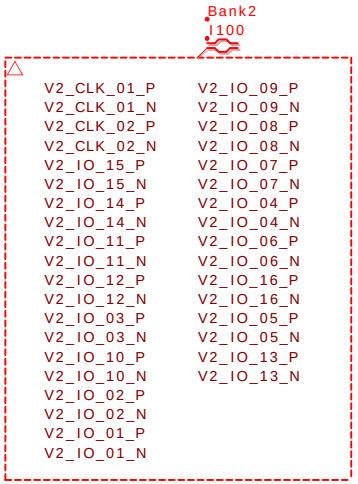
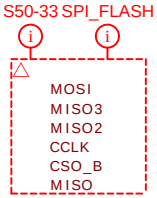
Filename: FPGA_DDR3.SchDoc

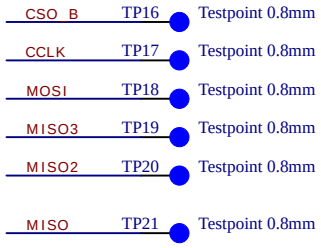












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Title: TE0630 - FPGA_B2			
A4	Number: TE0630 IV		Rev. 02
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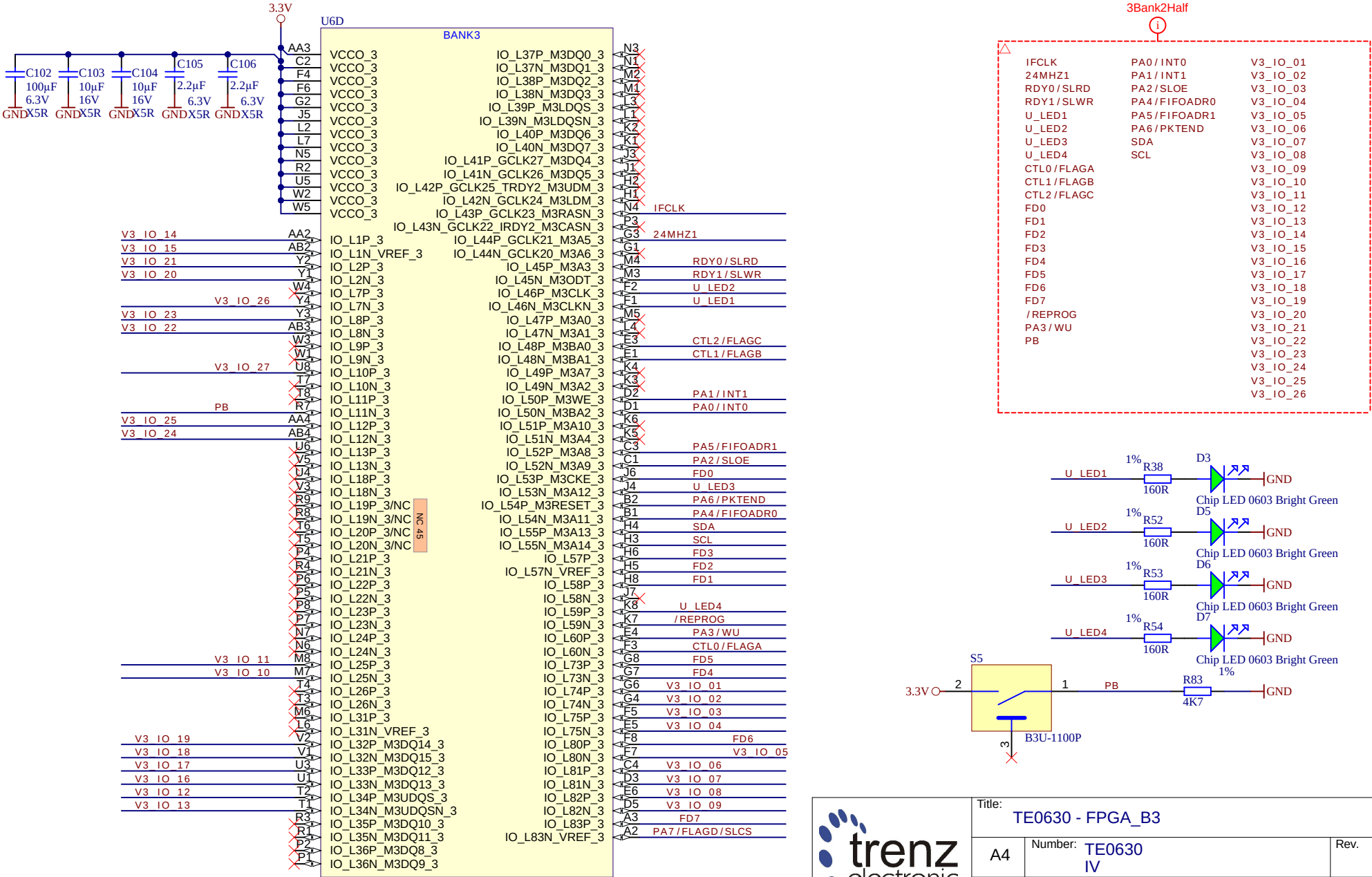
Filename: FPGA_B2.SchDoc			



Title:	TE0630 - FPGA_B3		
A4	Number: TE0630 IV		Rev. 02
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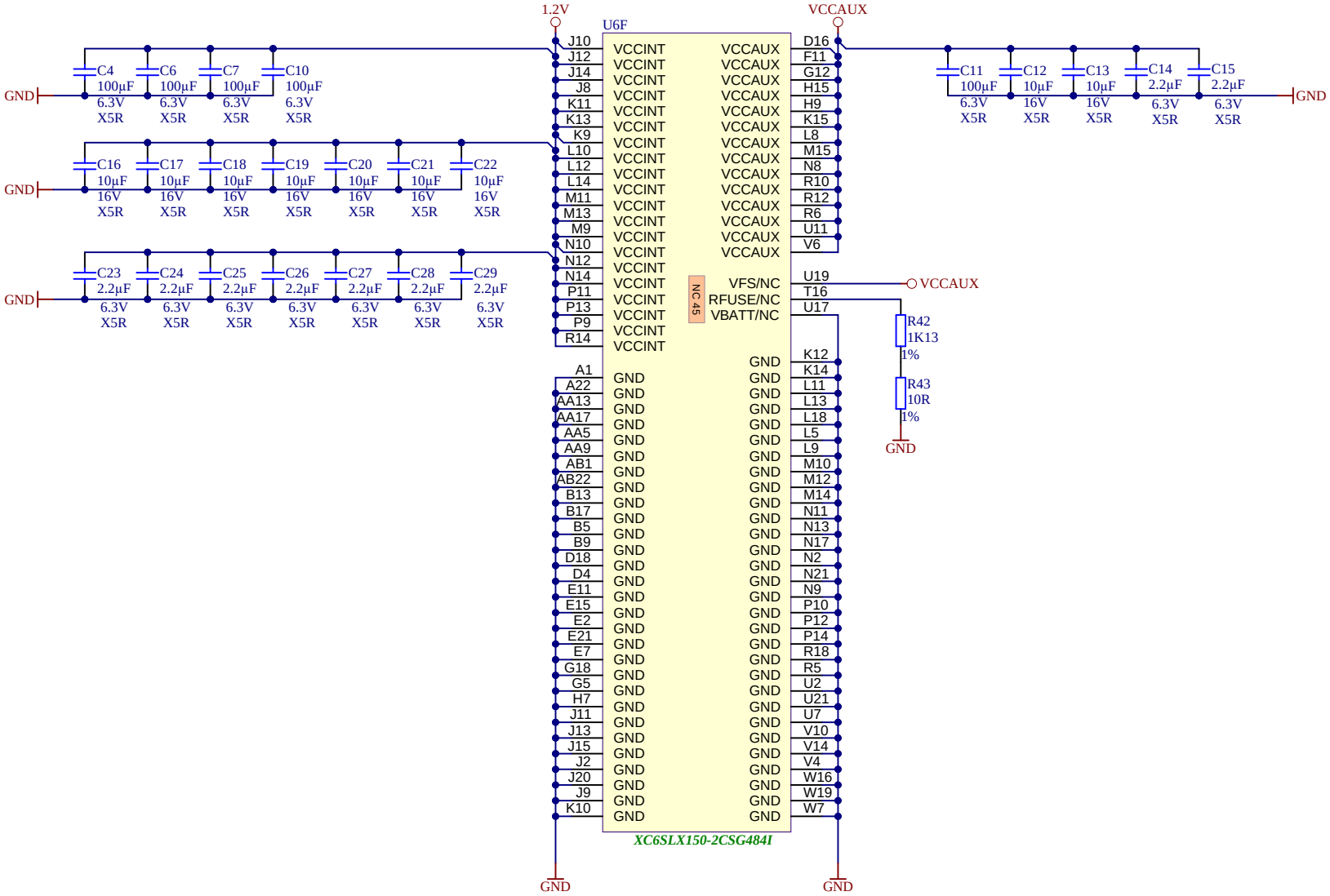
Filename:	FPGA_B3.SchDoc		



Title: TE0630 - FPGA_PWR			
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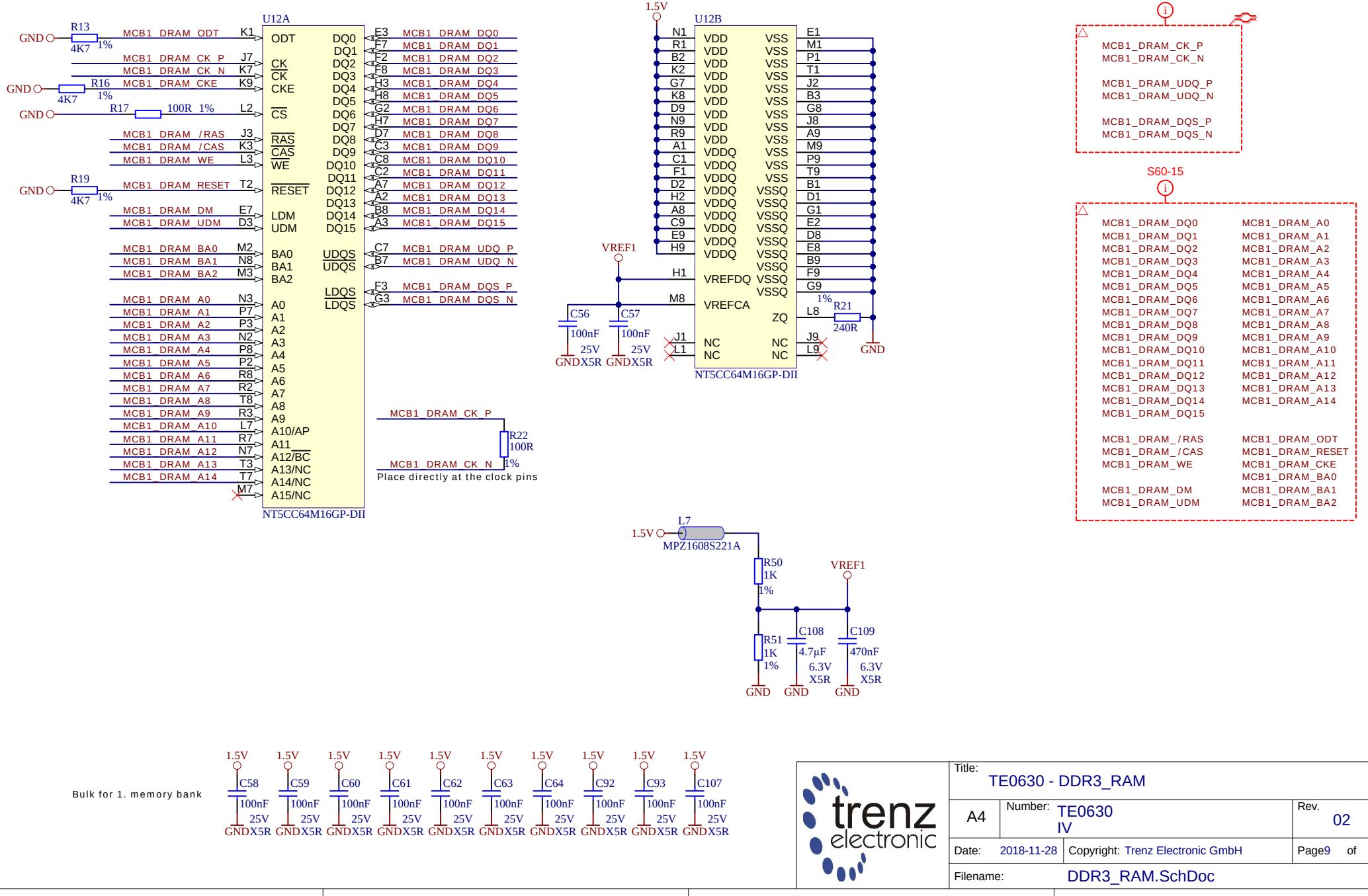
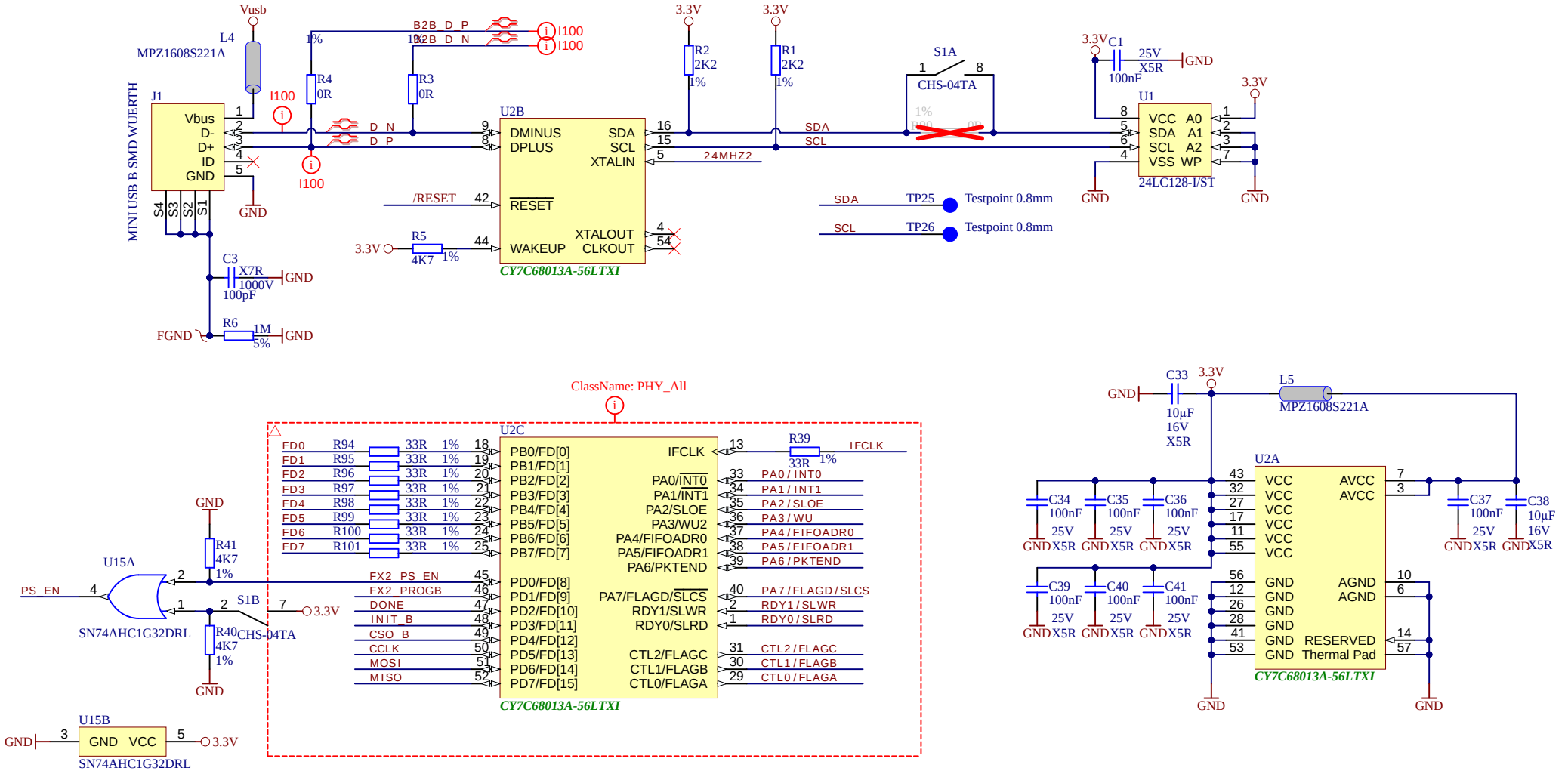
Filename: FPGA_PWR.SchDoc			



Title: TE0630 - DDR3_RAM			
A4	Number: TE0630 IV		Rev. 02
Date: 2018-11-28	Copyright: Trenz Electronic GmbH		Page9 of 12
Filename: DDR3_RAM.SchDoc			



trenz electronic	Title: TE0630 - USB		
	A4	Number: TE0630 IV	Rev. 02
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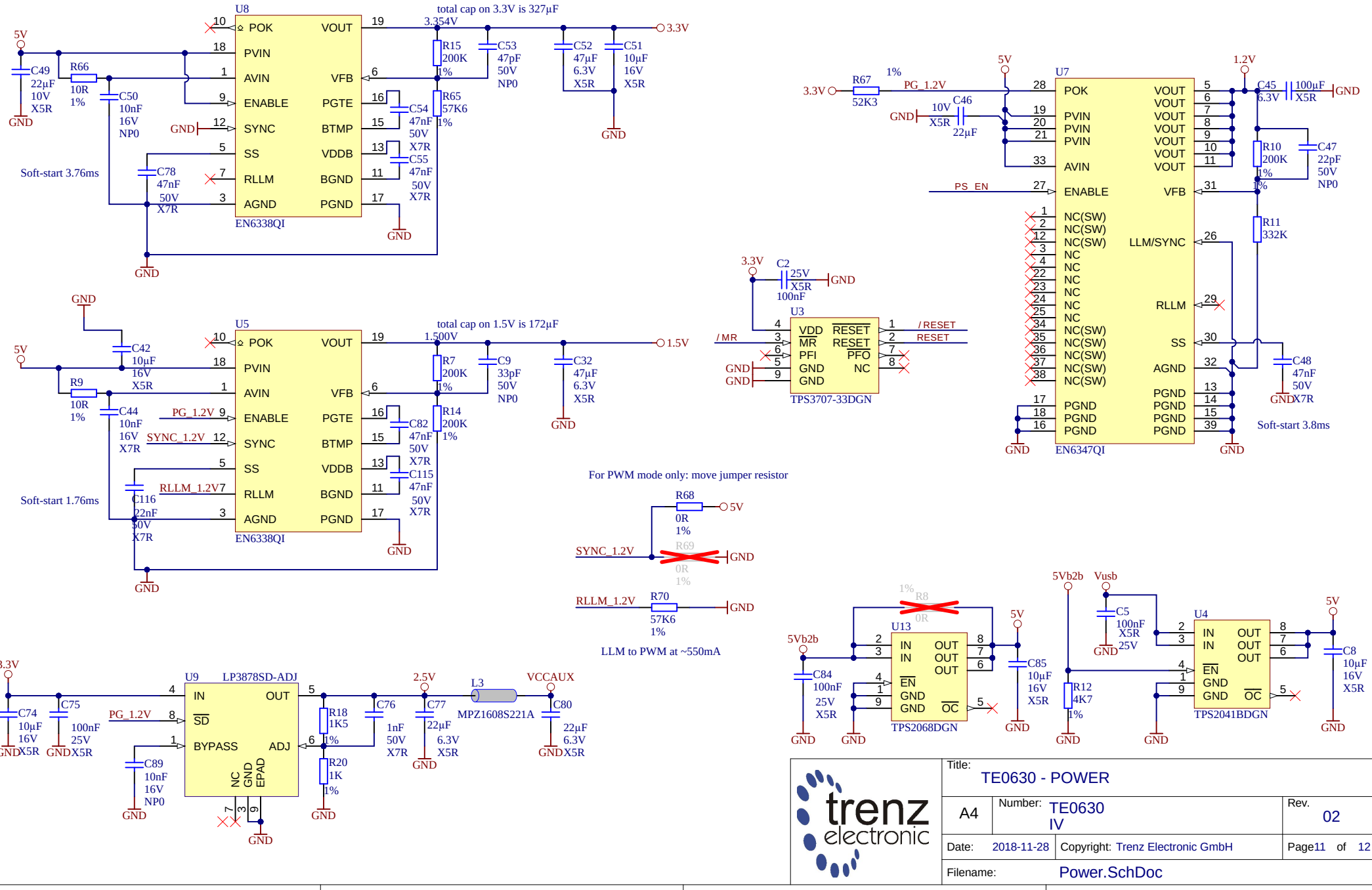
	Filename: USB.SchDoc		


U8
EN6338QI
POK
PVIN
AVIN
ENABLE
SYNC
SS
RLLM
AGND
VOUT
VFB
PGTE
BTMP
VDDB
BGND
PGND
5V
3.3V
GND
C49 22µF 10V X5R
R66 10R 1%
C50 10nF 16V NP0
C78 47nF 50V X7R
Soft-start 3.76ms
R15 200K 1%
R65 57K6 1%
C53 47pF 50V NP0
C52 47µF 6.3V X5R
C51 10µF 16V X5R
C54 47nF 50V X7R
C55 47nF 50V X7R
3.354V
total cap on 3.3V is 327µF
U5
EN6338QI
C42 10µF 16V X5R
R9 10R 1%
C44 10nF 16V X7R
C116 22nF 50V X7R
Soft-start 1.76ms
PG_1.2V
SYNC_1.2V
RLLM_1.2V
R7 200K 1%
R14 200K 1%
C9 33pF 50V NP0
C32 47µF 6.3V X5R
C82 47nF 50V X7R
C115 47nF 50V X7R
1.500V
1.5V
total cap on 1.5V is 172µF
U3
TPS3707-33DGN
C2 25V X5R 100nF
/MR
/RESET
RESET
VDD
MR
PFI
GND
RESET
PFO
NC
U7
EN6347QI
R67 52K3 1%
C46 10V X5R 22µF
PS_EN
ENABLE
NC(SW)
NC
PVIN
AVIN
VOUT
LLM/SYNC
RLLM
SS
AGND
PGND
C45 6.3V 100µF X5R
R10 200K 1%
C47 22pF 50V NP0
R11 332K
C48 47nF 50V X7R
Soft-start 3.8ms
1.2V
For PWM mode only: move jumper resistor
R68 0R 1%
R69 0R 1%
R70 57K6 1%
LLM to PWM at ~550mA
U9
LP3878SD-ADJ
IN
OUT
SD
BYPASS
ADJ
NC
GND
EPAD
C74 10µF 16V X5R
C75 100nF 25V X5R
C89 10nF 16V NP0
R18 1K5 1%
R20 1K 1%
C76 1nF 50V X7R
C77 22µF 6.3V X5R
2.5V
L3
MPZ1608S221A
VCCAUX
C80 22µF 6.3V X5R
U13
TPS2068DGN
R8 0R 1%
C84 100nF 25V X5R
C85 10µF 16V X5R
5Vb2b
Vusb
C5 100nF X5R 25V
U4
TPS2041BDGN
R12 4K7 1%
C8 10µF 16V X5R
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Title: TE0630 - POWER
A4
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CHANGES REV01 to REV02
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1) Replaced U8 by EN6338QI
2) Rerouted nets around U8, results in new track length for:
Signal V3_IO_06 15.2475 mm (was 15.0047mm)
Signal V3_IO_07 16.0151 mm (was 15.0452 mm)
3) Replaced U5 by EN 6338QI
4) PS_EN now via OR gate
5) Replaced obsolete Diodes D1, D2 D4, by BAT54A
6) Fixed Footprint of U10 according to datasheet
7) Update from LIB
8) Rearranged Testpoints
9) Added Traceability Pad
10) Replaced S5 by smaller PB AN26337
11) Hardware revision coding updated to Rev02

CHANGES REV02

2020-03-30
1) Flash change (U14)

trenz electronic	Title: TE0630 - Changes list		
	A4	Number: TE0630 IV	Rev. 02
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	Filename: Revision_Changes.SchDoc		