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Schematics and other handouts serve for informational purposes only!

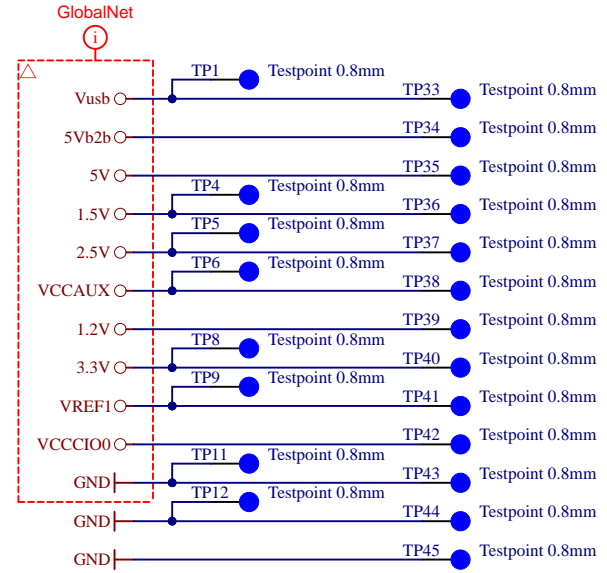
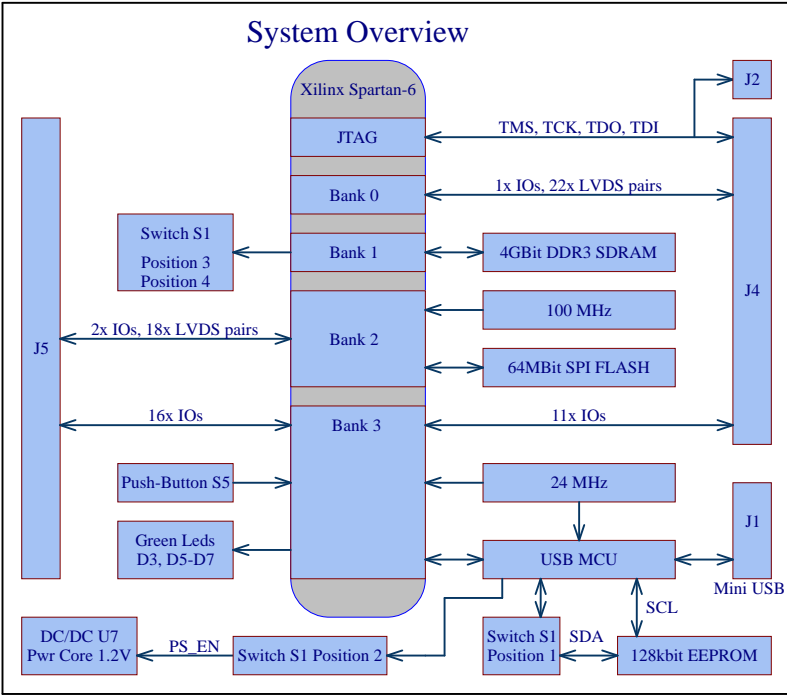
	Title: TE0630 - Legal Notices Modules		
	A4	Number: TE0630 52112-A	Rev. 03
	Date: 19-Sep-23	Copyright: Trenz Electronic GmbH	Page 1 of 13
	Filename: Legal_Notices.SchDoc		

REV	Description	
-01	Initial revision	
-02	<ul style="list-style-type: none"> 1) Replaced U8 by EN6338QI 2) Rerouted nets around U8, results in new track length for: Signal V3_IO_06 15.2475 mm (was 15.0047mm) Signal V3_IO_07 16.0151 mm (was 15.0452 mm) 3) Replaced U5 by EN 6338QI 4) PS_EN now via OR gate 5) Replaced obsolete Diodes D1, D2 D4, by BAT54A 6) Fixed Footprint of U10 according to datasheet 7) Update from LIB 8) Rearranged Testpoints 9) Added Traceability Pad 10) Replaced S5 by smaller PB AN26337 11) Hardware revision coding updated to Rev02 12) Flash change (U14) 2020-03-30 	
-03	<ul style="list-style-type: none"> 1) All sch and pcb components were updated 2) R46 was changed to 330 Ohm 3) "TE0630.SchDoc" page was updated: System Overview was redesigned, Power Up Sequence was added, S/N1 Serialnumber was removed 4) U7 was changed from EN6347QI to MPM3860GQW-Z 5) U8 and U5 were changed from EN6338QI to MPM3834CGPA 6) Added pullups R84 and R85 for ST pin of U10 and U11 on page "FPGA_CFG_CLK.SchDoc" 7) TE logo was changed to UKCA Logo on page "TE0630.SchDoc" 8) "B2B_Connectors.SchDoc" page was updated: service information about IOs pins was added, colored signal groups were added 9) BR0 net was pulled to 1.5V on page "FPGA_DDR3.SchDoc" 10) U12 was changed from NT5CC64M16GP-DII to IS43TR16256BL-125KBLI 11) Assembly option. Pull down resistor R70 was added on page "FPGA_B0.SchDoc" 12) Assembly Variants table was changed on page "FPGA_DDR3.SchDoc": obsolete variants were deleted, new assembly variants were added 13) "Legal_Notices.SchDoc" page was added 14) Parameters of some capacitors were changed: C77 , C80 : 6.3V -> 10V 15) Fiducials PM1-PM6 were updated and moved for same positions on top and bottom layers 16) Removed testpoints TP2,TP3,TP7,TP10,TP13,TP14,TP15,TP17, TP19,TP20,TP21, TP27,TP28,TP30,TP31,TP32 17) Added testpoints TP27 and TP28 on page "USB.SchDoc" 18) Some net classes names were deleted: "MatchLendht150Mil", "MatchLendht300Mil", "Clear_10mil", "S50-33" 19) Net class "3Bank2Half" was renamed to "Bank3" 	MT

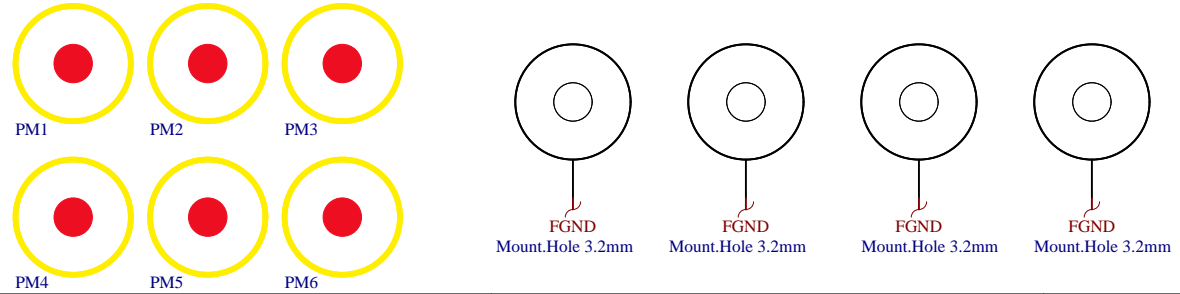
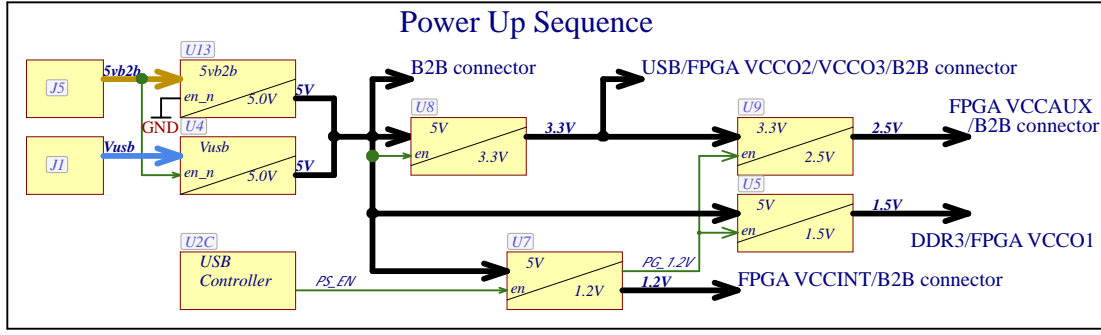


Title: TE0630 - Changes list		
A4	Number: TE0630 52112-A	Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH	Page 2 of 13
Filename: Revision_Changes.SchDoc		

- U_Power
Power.SchDoc
- U_FPGA_PWR
FPGA_PWR.SchDoc
- UKCA
UKCA Logo on Top Overlay
- UKCA-TOOVERLAY
- Serial
Serialnumber 6,3 x 6.3mm



Special notes:



BR0	BR1	BR2	BR3	See BR nets on page "FPGA_DDR3.SchDoc"
0	0	0	0	-00 Initial revision
1	0	0	0	-01
0	1	0	0	-02
1	1	0	0	-03

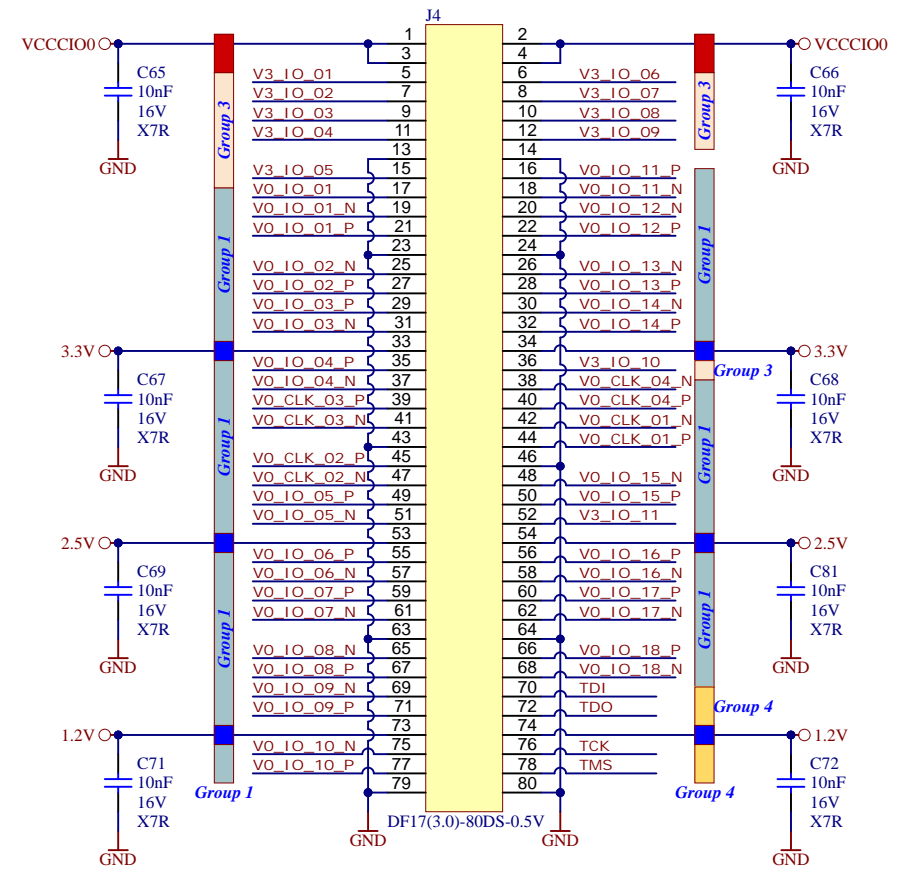
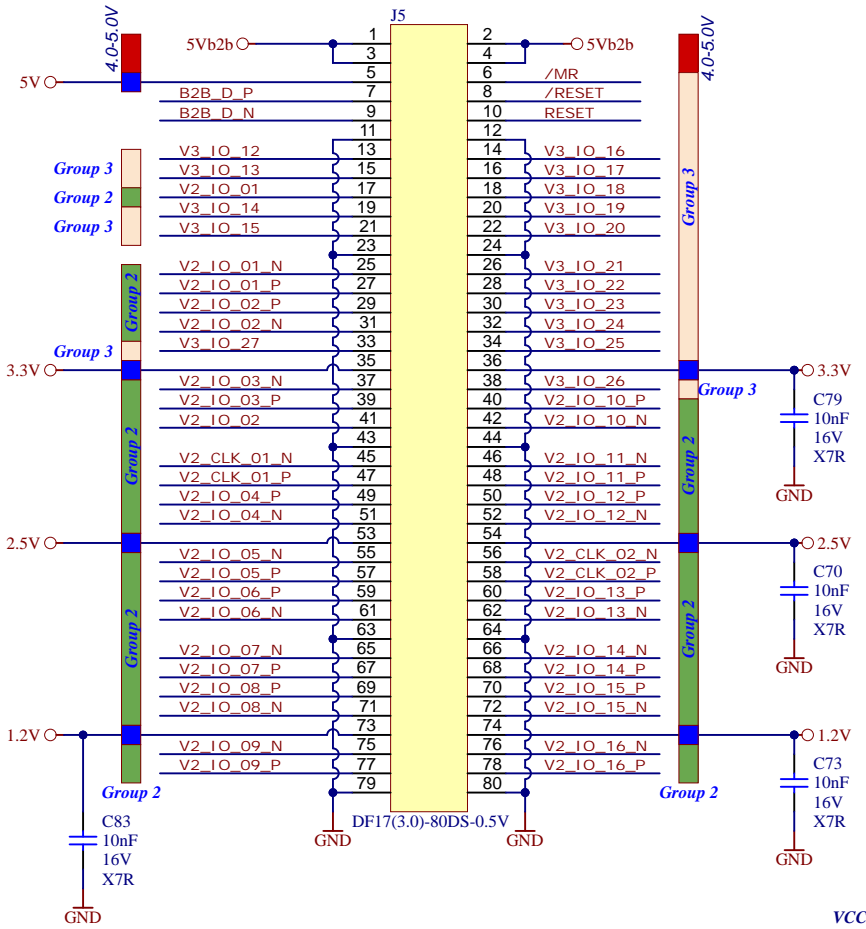
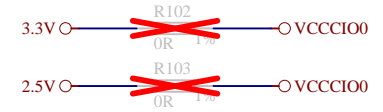
Assembly variant	52112-A
Created by	MT
Modified by	MT
Modified at	2023-09-20



Title: TE0630		
A4	Number: TE0630 52112-A	Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH	Page 3 of 13
Filename: TE0630.SchDoc		

B2 38 IOs 3.3V, 18 LVDS Pairs
 B3 16 IOs 3.3V

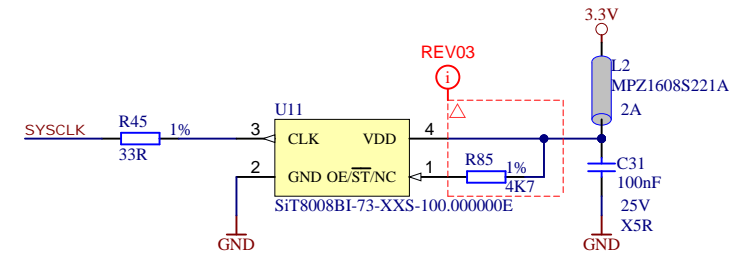
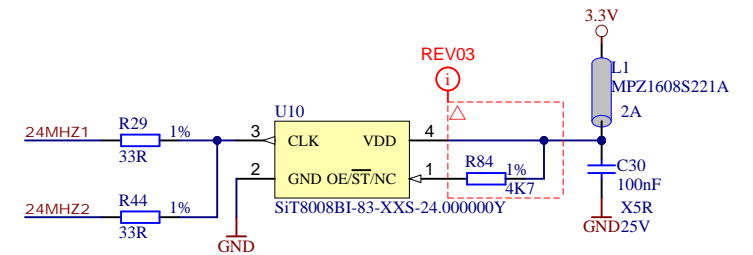
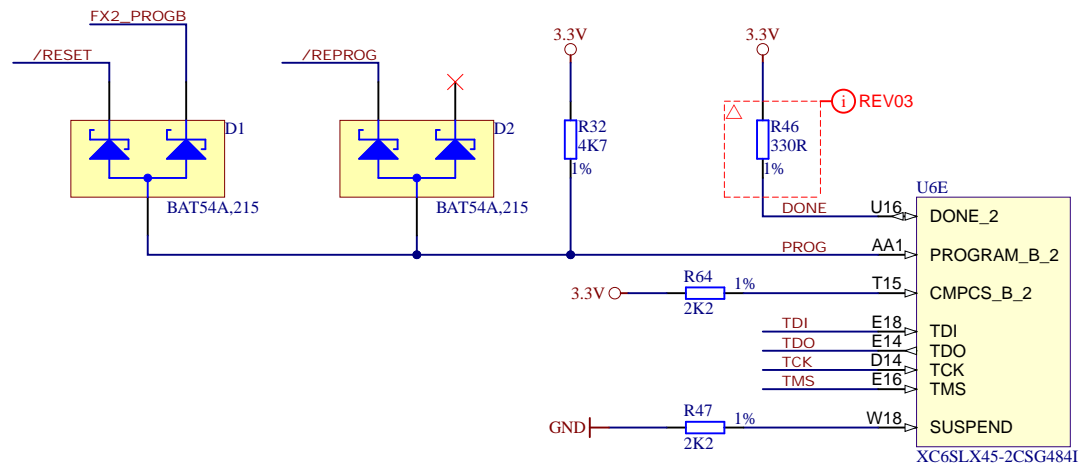
B0 45 IOs VCCIO0, 22 LVDS Pairs
 B3 11 IOs 3.3V



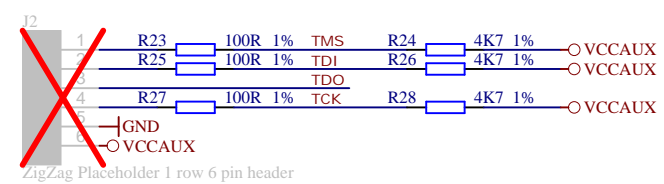
- VCCIO0 1.1..3.45V
- VCCIO2 3.3V
- VCCIO3 3.3V
- VCCAUX 2.5V
- Group 1 0..VCCIO0
- Group 2 0..VCCIO2
- Group 3 0..VCCIO3
- Group 4 0..VCCAUX
- PWR in
- PWR out



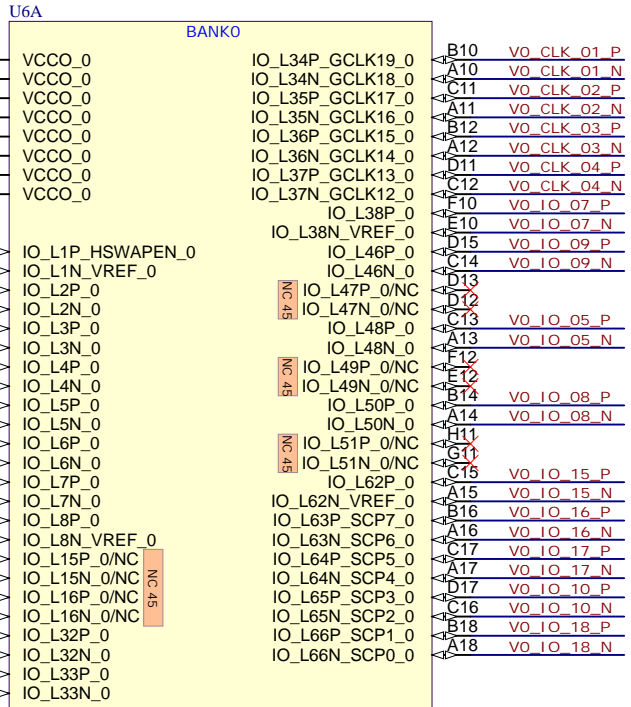
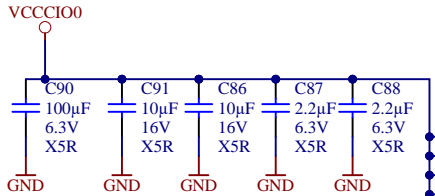
Title: TE0630 - B2B_Connectors		
A4	Number: TE0630 52112-A	Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH	Page 4 of 13
Filename: B2B_Connectors.SchDoc		



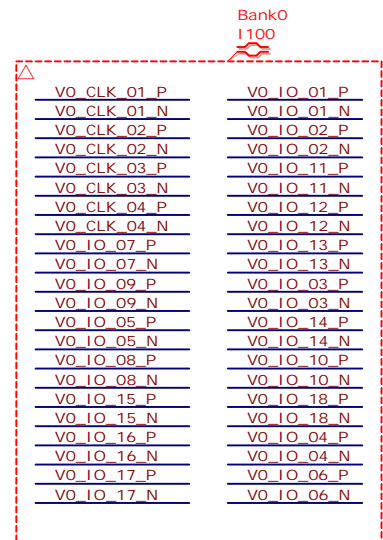
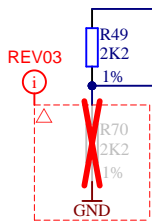
- 24MHZ1 TP22 Testpoint 0.8mm
- 24MHZ2 TP23 Testpoint 0.8mm
- SYSCLK TP24 Testpoint 0.8mm
- PROG TP29 Testpoint 0.8mm



	Title: TE0630 - FPGA_CFG_CLK		
	A4	Number: TE0630 52112-A	Rev. 03
	Date: 19-Sep-23	Copyright: Trenz Electronic GmbH	Page 5 of 13
	Filename: FPGA_CFG_CLK.SchDoc		



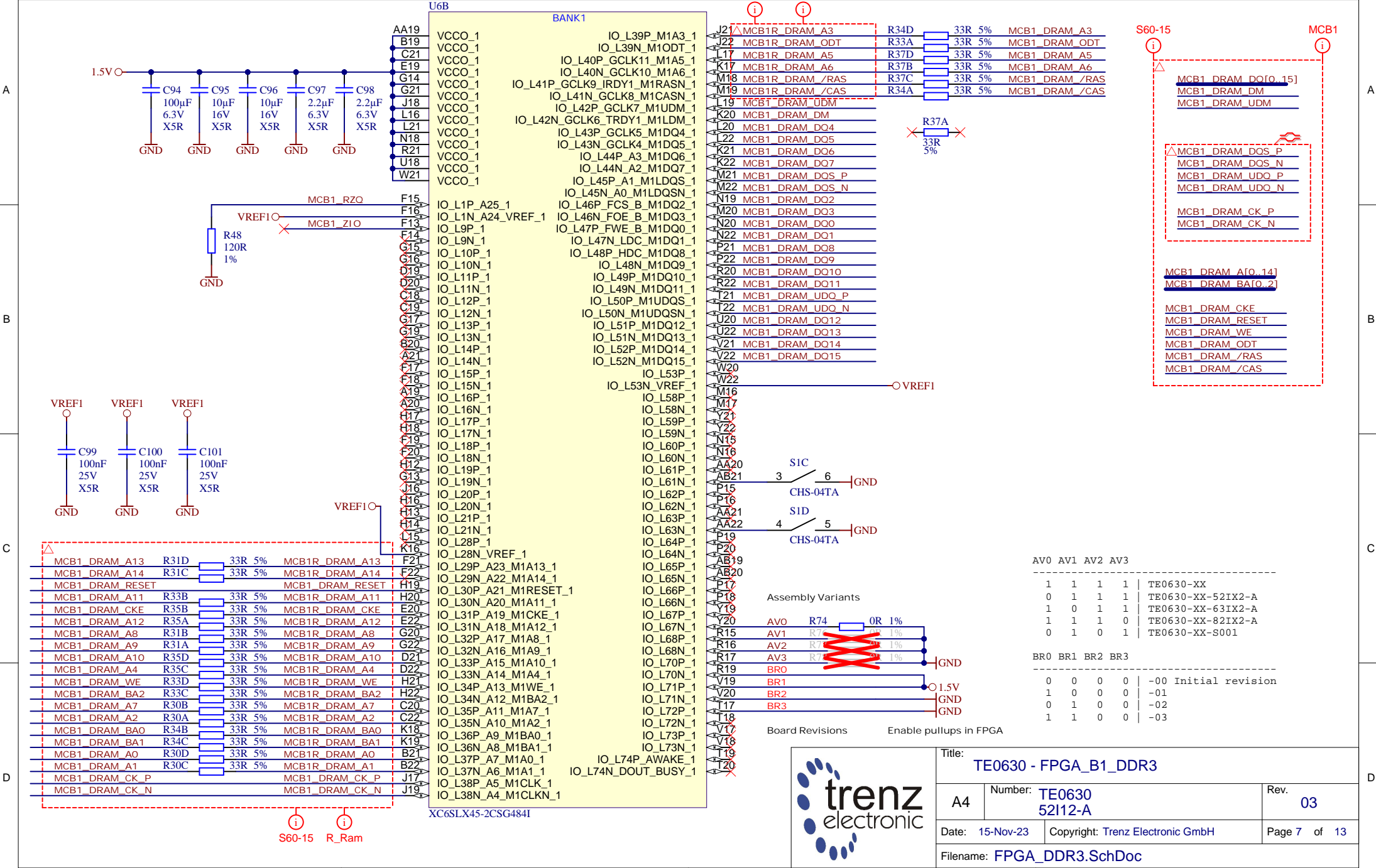
HSWAP = high --> No configuration pullups
 HSWAP = low: R49 DNP, R70 populated



HSWAP = high: R49 populated, R70 DNP
 HSWAP = low: R49 DNP, R70 populated



Title: TE0630 - FPGA_B0		
A4	Number: TE0630 52112-A	Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH	Page 6 of 13
Filename: FPGA_B0.SchDoc		



BANK1

AA19	VCCO_1	IO_L39P_M1A3_1
B19	VCCO_1	IO_L39N_M1ODT_1
C21	VCCO_1	IO_L40P_GCLK11_M1A5_1
E19	VCCO_1	IO_L40N_GCLK10_M1A6_1
G14	VCCO_1	IO_L41P_GCLK9_IRDY1_M1RASN_1
G21	VCCO_1	IO_L41N_GCLK8_M1CASN_1
J18	VCCO_1	IO_L42P_GCLK7_M1UDM_1
L16	VCCO_1	IO_L42N_GCLK6_TRDY1_M1LDM_1
L21	VCCO_1	IO_L43P_GCLK5_M1DQ4_1
N18	VCCO_1	IO_L43N_GCLK4_M1DQ5_1
R21	VCCO_1	IO_L44P_A3_M1DQ6_1
U18	VCCO_1	IO_L44N_A2_M1DQ7_1
W21	VCCO_1	IO_L45P_A1_M1LDQS_1
		IO_L45N_A0_M1LDQSN_1
F15	IO_L1P_A25_1	IO_L46P_FCS_B_M1DQ2_1
F16	IO_L1N_A24_VREF_1	IO_L46N_FOE_B_M1DQ3_1
F13	IO_L9P_1	IO_L47P_FWE_B_M1DQ0_1
F14	IO_L9N_1	IO_L47N_LDC_M1DQ1_1
G15	IO_L10P_1	IO_L48P_HDC_M1DQ8_1
G16	IO_L10N_1	IO_L48N_M1DQ9_1
D19	IO_L11P_1	IO_L49P_M1DQ10_1
D20	IO_L11N_1	IO_L49N_M1DQ11_1
C18	IO_L12P_1	IO_L50P_M1UDQS_1
C19	IO_L12N_1	IO_L50N_M1UDQSN_1
G17	IO_L13P_1	IO_L51P_M1DQ12_1
G19	IO_L13N_1	IO_L51N_M1DQ13_1
B20	IO_L14P_1	IO_L52P_M1DQ14_1
B21	IO_L14N_1	IO_L52N_M1DQ15_1
A21	IO_L15P_1	IO_L53P_1
F17	IO_L15N_1	IO_L53N_VREF_1
A19	IO_L16P_1	IO_L58P_1
A20	IO_L16N_1	IO_L58N_1
H17	IO_L17P_1	IO_L59P_1
H18	IO_L17N_1	IO_L59N_1
F19	IO_L18P_1	IO_L60P_1
F20	IO_L18N_1	IO_L60N_1
H12	IO_L19P_1	IO_L61P_1
G13	IO_L19N_1	IO_L61N_1
J16	IO_L20P_1	IO_L62P_1
H16	IO_L20N_1	IO_L62N_1
H13	IO_L21P_1	IO_L63P_1
H14	IO_L21N_1	IO_L63N_1
L15	IO_L28P_1	IO_L64P_1
K16	IO_L28N_VREF_1	IO_L64N_1
F21	IO_L29P_A23_M1A13_1	IO_L65P_1
F22	IO_L29N_A22_M1A14_1	IO_L65N_1
H19	IO_L30P_A21_M1RESET_1	IO_L66P_1
H20	IO_L30N_A20_M1A11_1	IO_L66N_1
E20	IO_L31P_A19_M1CKE_1	IO_L67P_1
G20	IO_L31N_A18_M1A12_1	IO_L67N_1
G21	IO_L32P_A17_M1A8_1	IO_L68P_1
G22	IO_L32N_A16_M1A9_1	IO_L68N_1
D21	IO_L33P_A15_M1A10_1	IO_L70P_1
D22	IO_L33N_A14_M1A4_1	IO_L70N_1
H21	IO_L34P_A13_M1WE_1	IO_L71P_1
H22	IO_L34N_A12_M1BA2_1	IO_L71N_1
C20	IO_L35P_A11_M1A7_1	IO_L72P_1
C22	IO_L35N_A10_M1A2_1	IO_L72N_1
K18	IO_L36P_A9_M1BA0_1	IO_L73P_1
K19	IO_L36N_A8_M1BA1_1	IO_L73N_1
B21	IO_L37P_A7_M1A0_1	IO_L74N_AWAKE_1
B22	IO_L37N_A6_M1A1_1	IO_L74N_DOUT_BUSY_1
J17	IO_L38P_A5_M1CLK_1	
J19	IO_L38N_A4_M1CLKN_1	

XC6SLX45-2CSG484I

R_Ram S60-15

J21	MCB1R_DRAM_A3	R34D	33R 5%	MCB1_DRAM_A3
J22	MCB1R_DRAM_ODT	R33A	33R 5%	MCB1_DRAM_ODT
L17	MCB1R_DRAM_A5	R37D	33R 5%	MCB1_DRAM_A5
K17	MCB1R_DRAM_A6	R37B	33R 5%	MCB1_DRAM_A6
M18	MCB1R_DRAM /RAS	R37C	33R 5%	MCB1_DRAM /RAS
M19	MCB1R_DRAM /CAS	R34A	33R 5%	MCB1_DRAM /CAS
K19	MCB1R_DRAM_UDM			
K20	MCB1_DRAM_DM			
L20	MCB1_DRAM_DQ4			
L22	MCB1_DRAM_DQ5			
K21	MCB1_DRAM_DQ6			
K22	MCB1_DRAM_DQ7			
M21	MCB1_DRAM_DQS_P			
M22	MCB1_DRAM_DQS_N			
N19	MCB1_DRAM_DQ2			
M20	MCB1_DRAM_DQ3			
N20	MCB1_DRAM_DQ0			
N22	MCB1_DRAM_DQ1			
P21	MCB1_DRAM_DQ8			
P22	MCB1_DRAM_DQ9			
R20	MCB1_DRAM_DQ10			
R22	MCB1_DRAM_DQ11			
T21	MCB1_DRAM_UDQ_P			
T22	MCB1_DRAM_UDQ_N			
U20	MCB1_DRAM_DQ12			
U22	MCB1_DRAM_DQ13			
V21	MCB1_DRAM_DQ14			
V22	MCB1_DRAM_DQ15			
W20				
W22				
M16	VREF1			
M17				
V21				
V22				
N15				
N16				
AA20	SIC	3	6	GND
AB21	CHS-04TA			
P15				
P16	SID	4	5	GND
AA21				
AA22	CHS-04TA			
P19				
P20				
AB19				
AB20				
P17				
P18				
V19				
V20				
R15	AV0	R74	0R 1%	
R16	AV1	R75	0R 1%	
R17	AV2	R76	0R 1%	
R19	AV3	R77	0R 1%	
B19	BR0			
V19	BR1			
V20	BR2			
F17	BR3			
F18				
V17				
V18				
F19				
F20				

S60-15

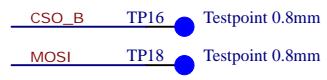
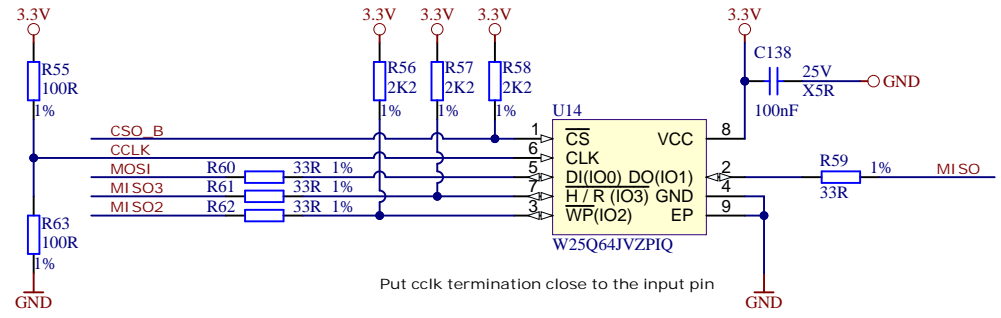
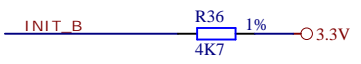
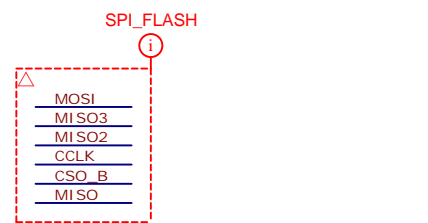
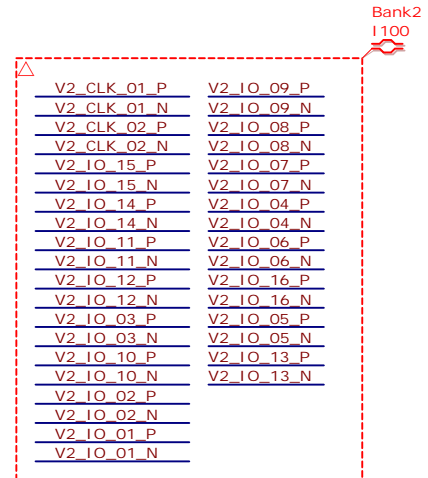
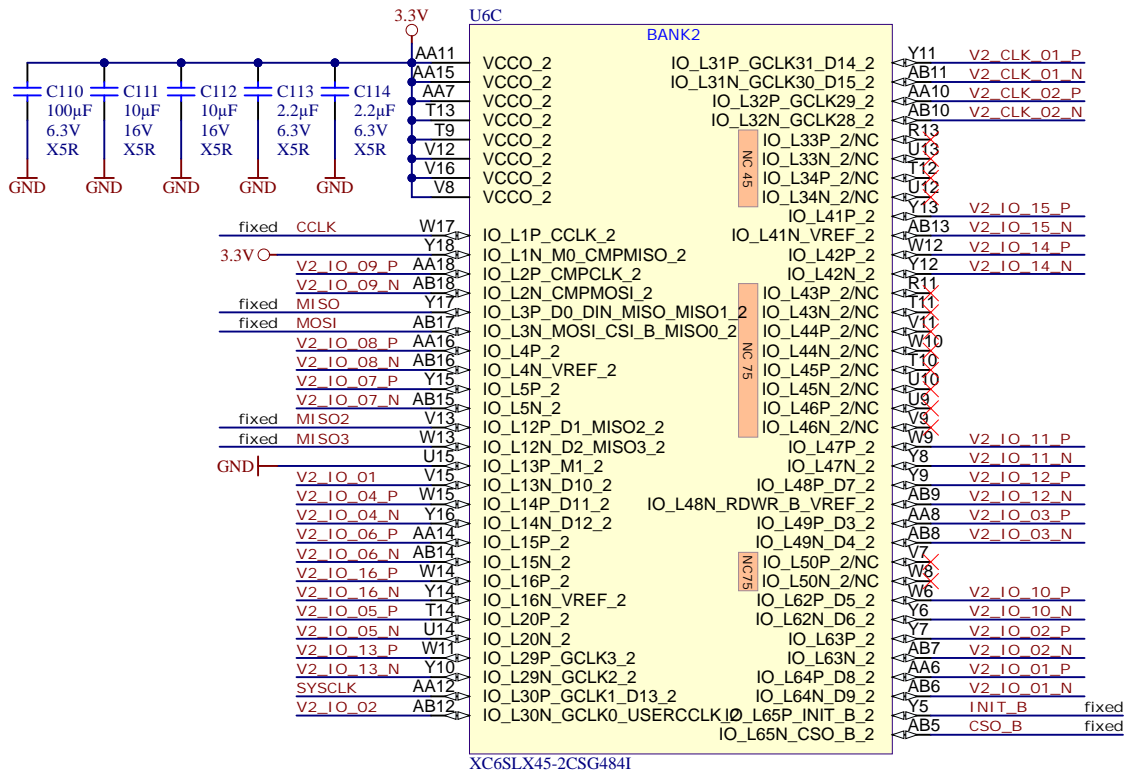
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MCB1_DRAM_DM
MCB1_DRAM_UDM
MCB1_DRAM_DQS_P
MCB1_DRAM_DQS_N
MCB1_DRAM_UDQ_P
MCB1_DRAM_UDQ_N
MCB1_DRAM_CK_P
MCB1_DRAM_CK_N
MCB1_DRAM_A[0..14]
MCB1_DRAM_BA[0..2]
MCB1_DRAM_CKE
MCB1_DRAM_RESET
MCB1_DRAM_WE
MCB1_DRAM_ODT
MCB1_DRAM /RAS
MCB1_DRAM /CAS

AV0	AV1	AV2	AV3	
1	1	1	1	TE0630-XX
0	1	1	1	TE0630-XX-52IX2-A
1	0	1	1	TE0630-XX-63IX2-A
1	1	1	0	TE0630-XX-82IX2-A
0	1	0	1	TE0630-XX-S001

BR0	BR1	BR2	BR3	
0	0	0	0	-00 Initial revision
1	0	0	0	-01
0	1	0	0	-02
1	1	0	0	-03



Title: TE0630 - FPGA_B1_DDR3		
A4	Number: TE0630 52I12-A	Rev. 03
Date: 15-Nov-23	Copyright: Trenz Electronic GmbH	Page 7 of 13
Filename: FPGA_DDR3.SchDoc		



Title: TE0630 - FPGA_B2		
A4	Number: TE0630 52112-A	Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH	Page 8 of 13
Filename: FPGA_B2.SchDoc		

A

A

B

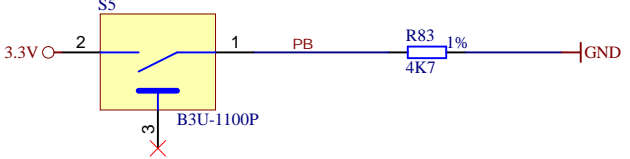
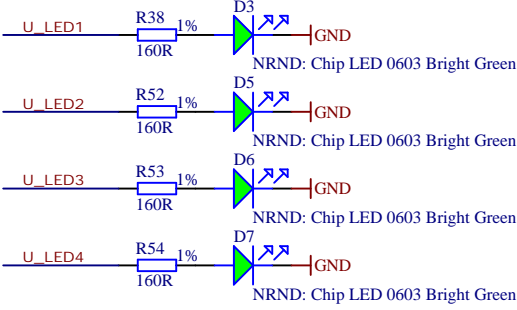
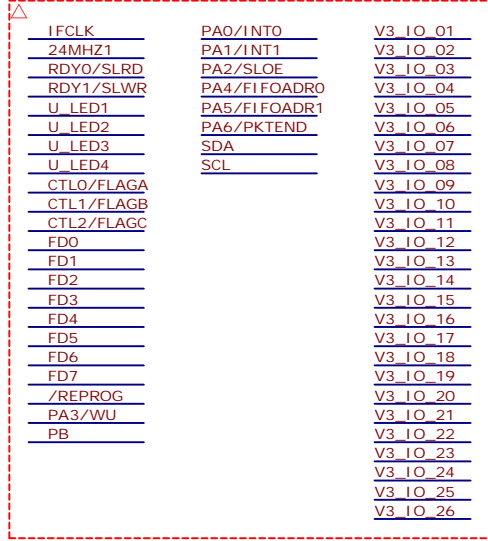
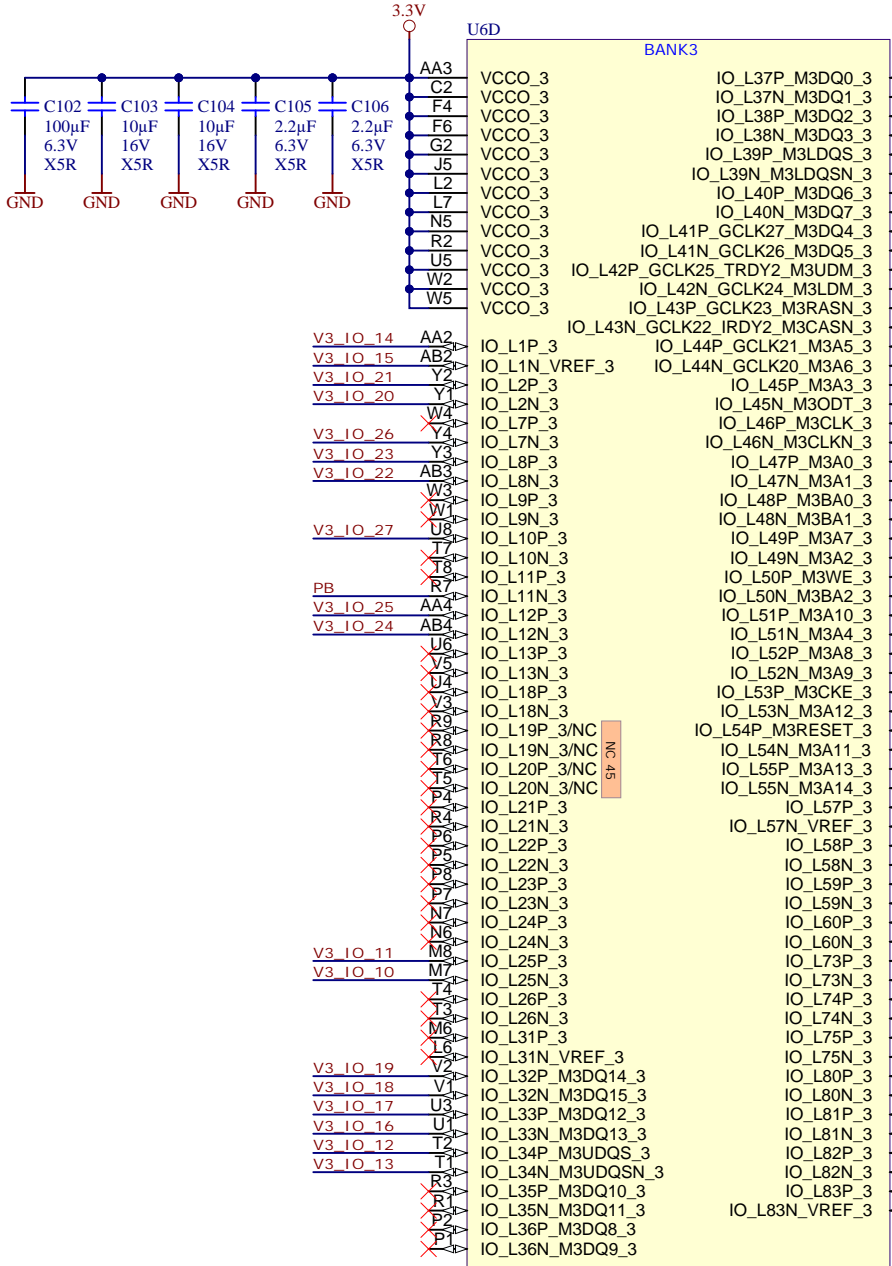
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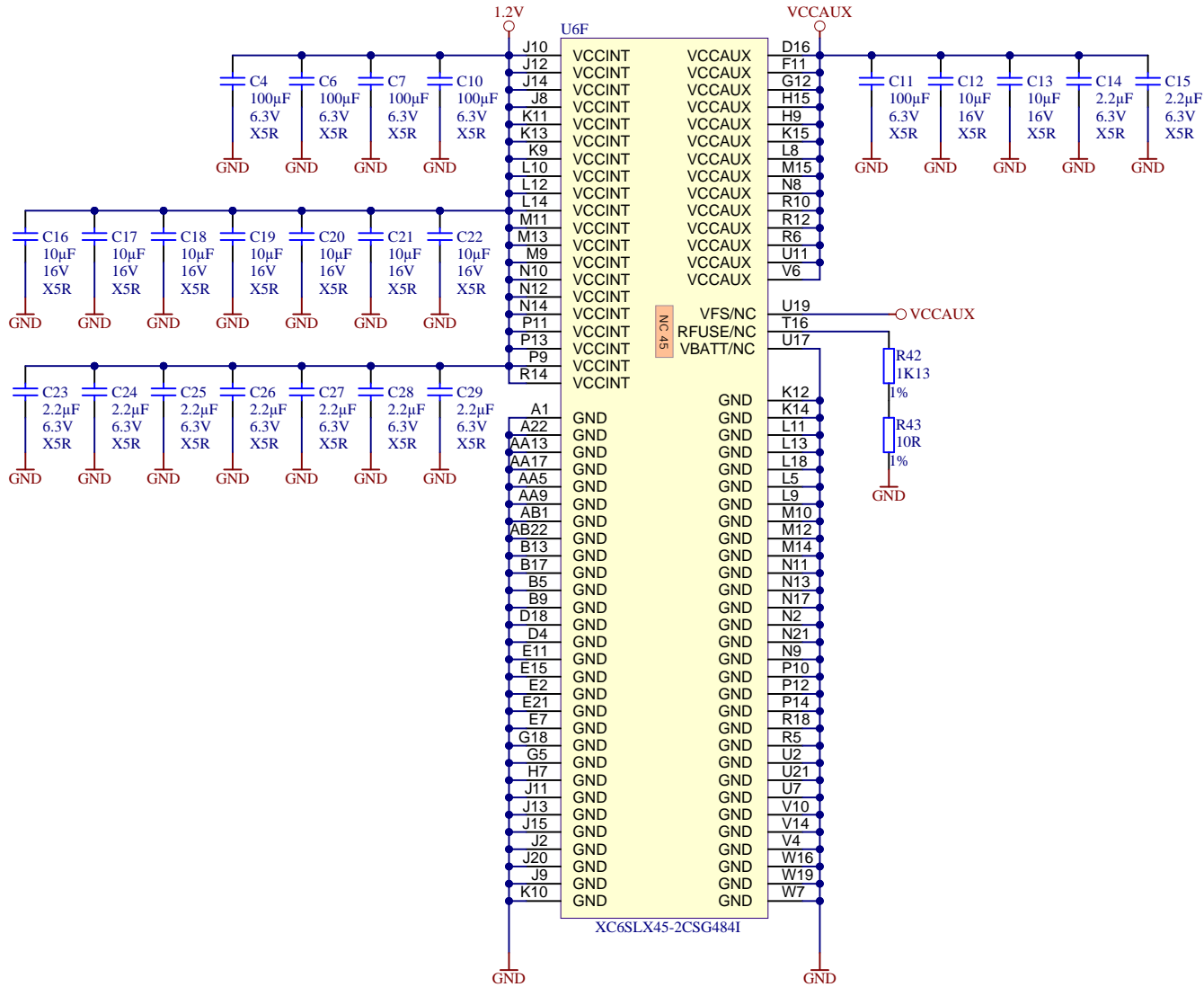
C


D

D



Title: TE0630 - FPGA_B3		
A4	Number: TE0630 52112-A	Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH	
Page 9 of 13		
Filename: FPGA_B3.SchDoc		



		Title: TE0630 - FPGA_PWR	
		A4	Number: TE0630 52112-A
Date: 19-Sep-23		Copyright: Trenz Electronic GmbH	
Filename: FPGA_PWR.SchDoc		Page 10 of 13	

A

B

C

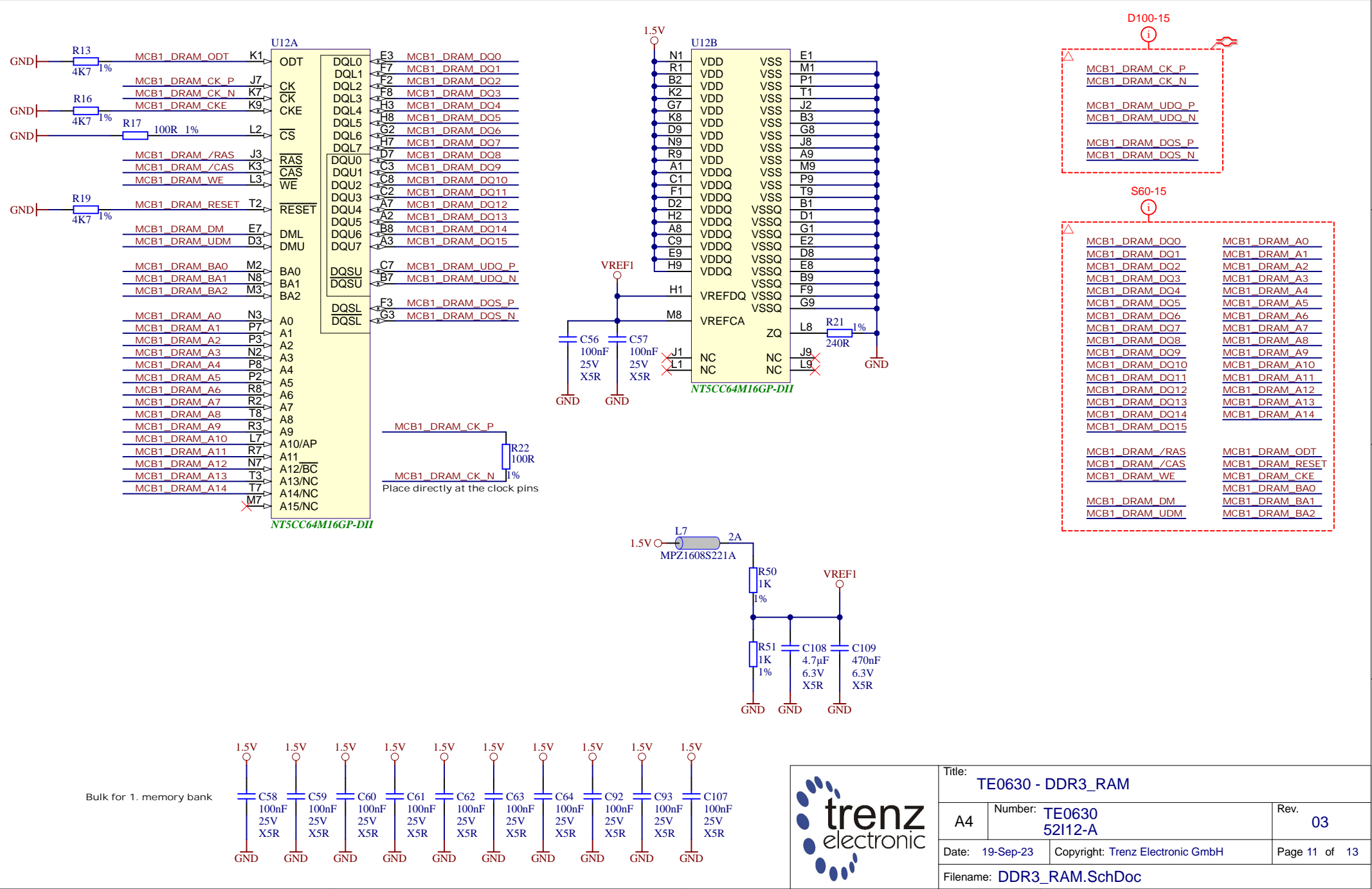
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A

B

C

D

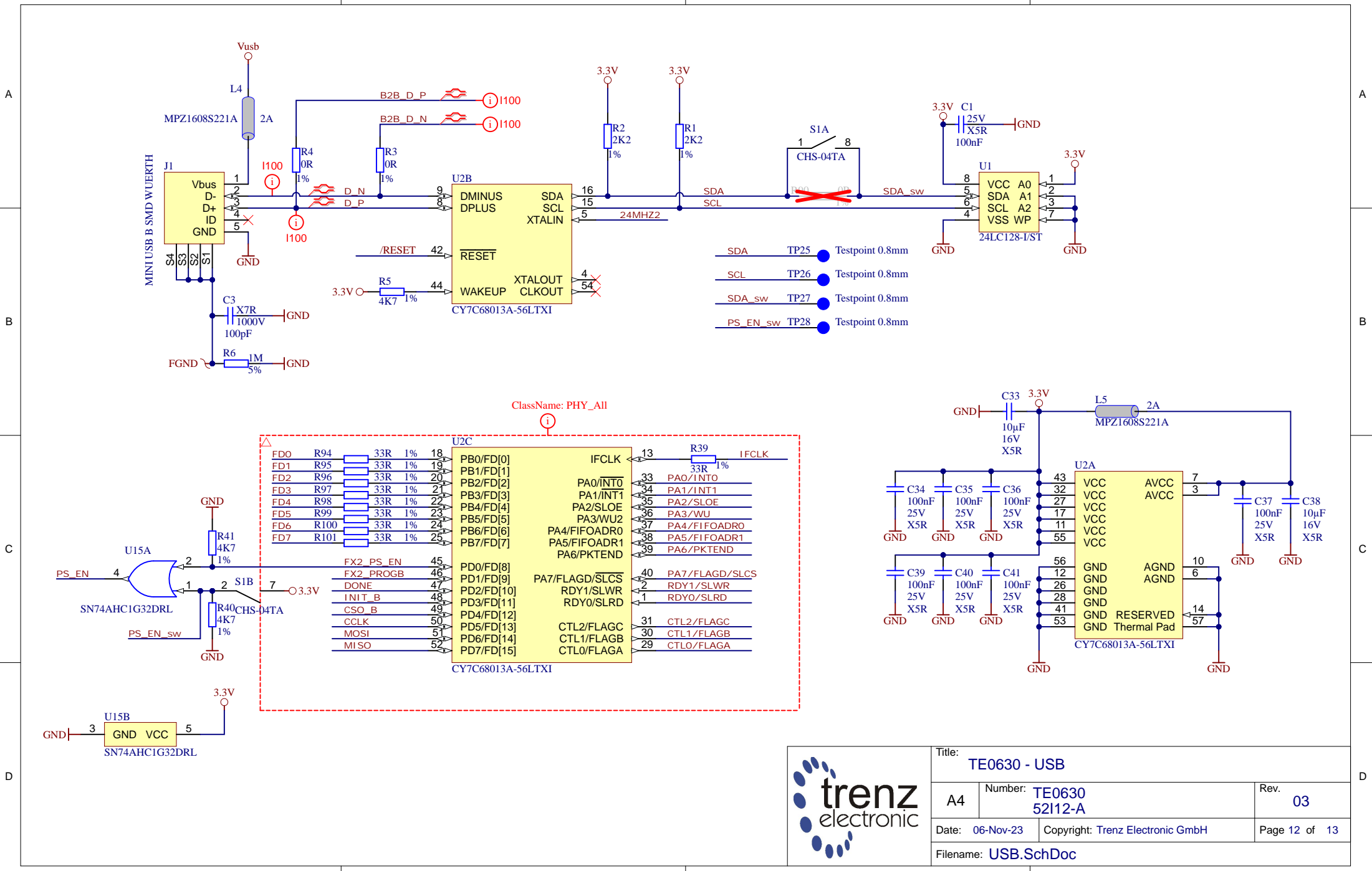


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Title: **TE0630 - DDR3_RAM**

A4	Number: TE0630 52112-A	Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH	
Page 11 of 13		

Filename: **DDR3_RAM.SchDoc**

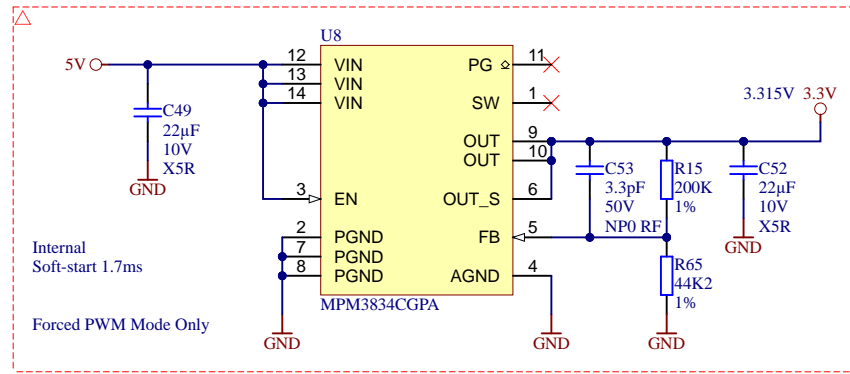


- SDA TP25 Testpoint 0.8mm
- SCL TP26 Testpoint 0.8mm
- SDA_sw TP27 Testpoint 0.8mm
- PS_EN_sw TP28 Testpoint 0.8mm

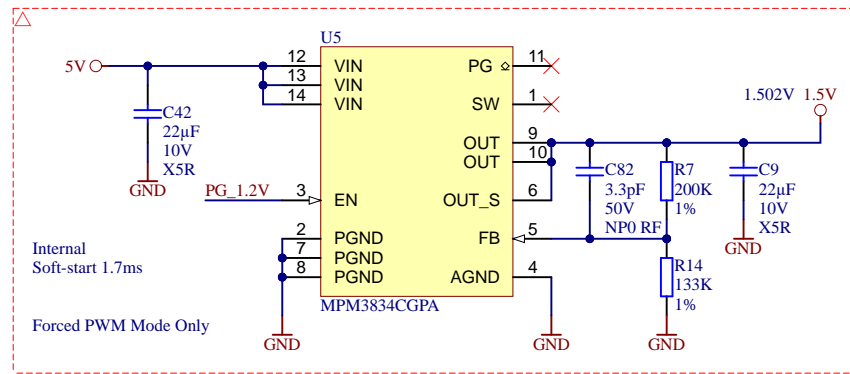
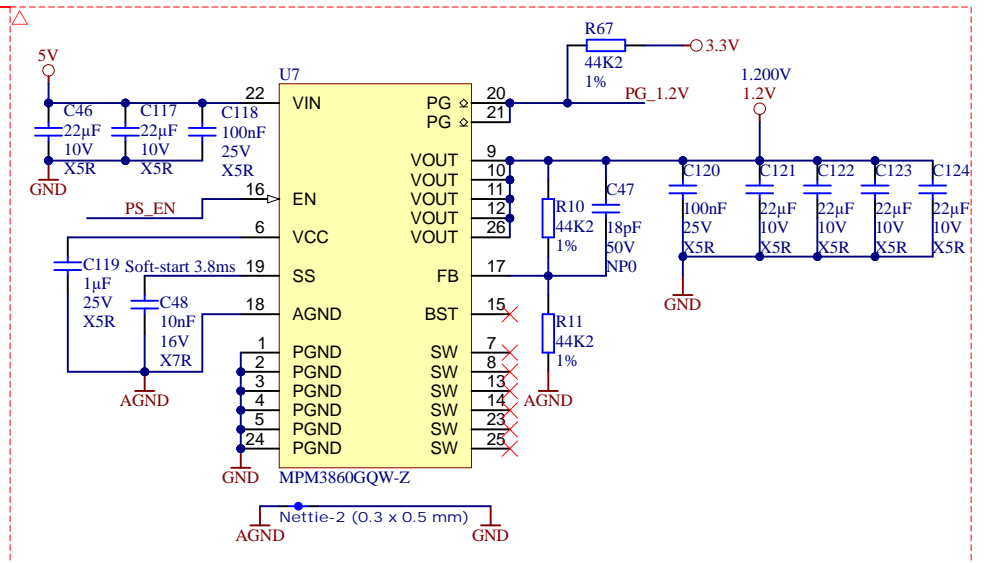
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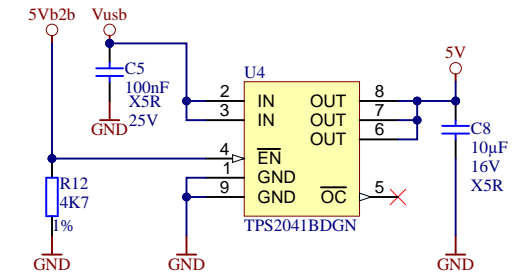
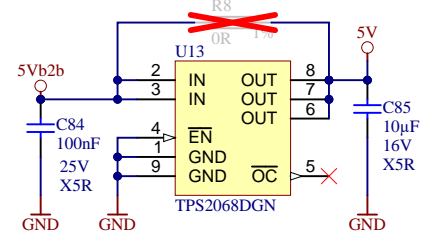
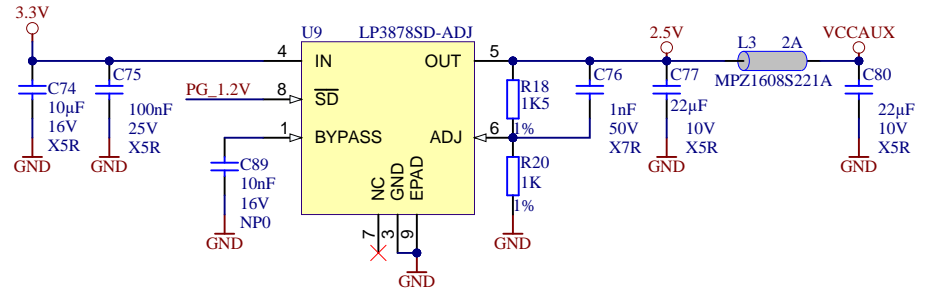
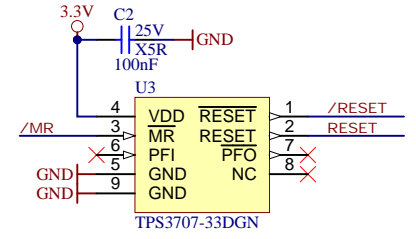
Title: TE0630 - USB		
A4	Number: TE0630 52112-A	Rev. 03
Date: 06-Nov-23	Copyright: Trenz Electronic GmbH	Page 12 of 13
Filename: USB.SchDoc		



REV3



REV3



	Title: TE0630 - POWER	
	A4	Number: TE0630 52112-A
	Date: 19-Sep-23	Copyright: Trenz Electronic GmbH
	Rev: 03	Page 13 of 13
Filename: Power.SchDoc		