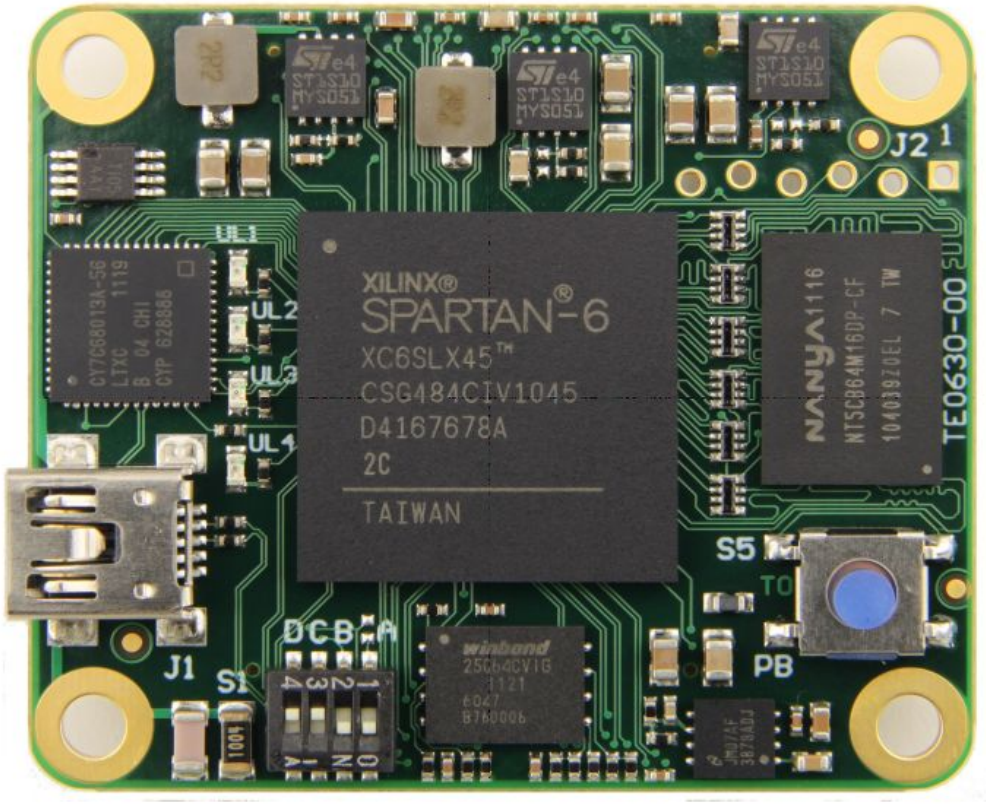

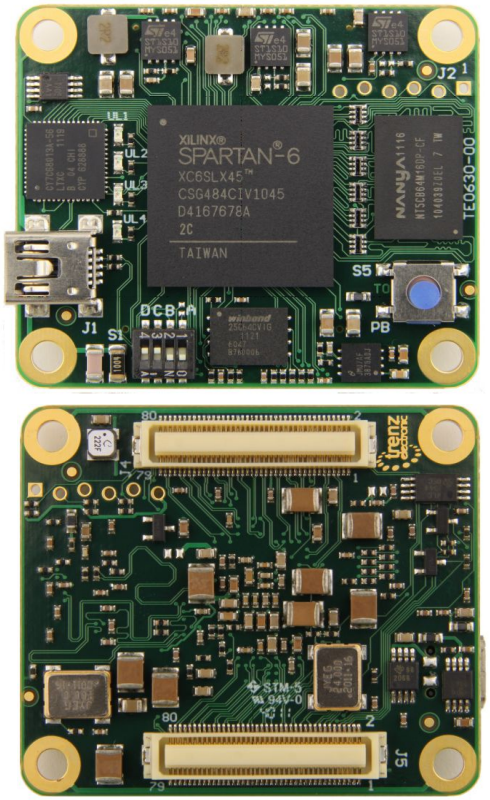

Regarding the usage of our schematics and alike documentation for Trenz module TE0630.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0630 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: TE0630 - Legal Notices Modules		
	A4	Number: TE0630 52I12-A	Rev. 03
	Date: 19-Sep-23	Copyright: Trenz Electronic GmbH	Page 1 of 13
	Filename: Legal_Notices.SchDoc		

REV	Description	
-01	Initial revision	
-02	1) Replaced U8 by EN6338QI 2) Rerouted nets around U8, results in new track length for: Signal V3_IO_06 15.2475 mm (was 15.0047mm) Signal V3_IO_07 16.0151 mm (was 15.0452 mm) 3) Replaced U5 by EN 6338QI 4) PS_EN now via OR gate 5) Replaced obsolete Diodes D1, D2 D4, by BAT54A 6) Fixed Footprint of U10 according to datasheet 7) Update from LIB 8) Rearranged Testpoints 9) Added Traceability Pad 10) Replaced S5 by smaller PB AN26337 11) Hardware revision coding updated to Rev02 12) Flash change (U14) 2020-03-30	
-03	1) All sch and pcb components were updated 2) R46 was changed to 330 Ohm 3) "TE0630.SchDoc" page was updated: System Overview was redesigned, Power Up Sequence was added, S/N1 Serialnumber was removed 4) U7 was changed from EN6347QI to MPM3860GQW-Z 5) U8 and U5 were changed from EN6338QI to MPM3834CGPA 6) Added pullups R84 and R85 for ST pin of U10 and U11 on page "FPGA_CFG_CLK.SchDoc" 7) TE logo was changed to UKCA Logo on page "TE0630.SchDoc" 8) "B2B_Connectors.SchDoc" page was updated: service information about IOs pins was added, colored signal groups were added 9) BR0 net was pulled to 1.5V on page "FPGA_DDR3.SchDoc" 10) U12 was changed from NT5CC64M16GP-DII to IS43TR16256BL-125KBLI 11) Assembly option. Pull down resistor R70 was added on page "FPGA_B0.SchDoc" 12) Assembly Variants table was changed on page "FPGA_DDR3.SchDoc": obsolete variants were deleted, new assembly variants were added 13) "Legal_Notices.SchDoc" page was added 14) Parameters of some capacitors were changed: C77 , C80 : 6.3V -> 10V 15) Fiducials PM1-PM6 were updated and moved for same positions on top and bottom layers 16) Removed testpoints TP2,TP3,TP7,TP10,TP13,TP14,TP15,TP17, TP19,TP20,TP21, TP27,TP28,TP30,TP31,TP32 17) Added testpoints TP27 and TP28 on page "USB.SchDoc" 18) Some net classes names were deleted: "MatchLendht150Mil", "MatchLendht300Mil", "Clear_10mil", "S50-33" 19) Net class "3Bank2Half" was renamed to "Bank3"	MT

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Title: TE0630 - Changes list		
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Filename: Revision_Changes.SchDoc		

U_Power
Power.SchDoc

U_FPGA_PWR
FPGA_PWR.SchDoc

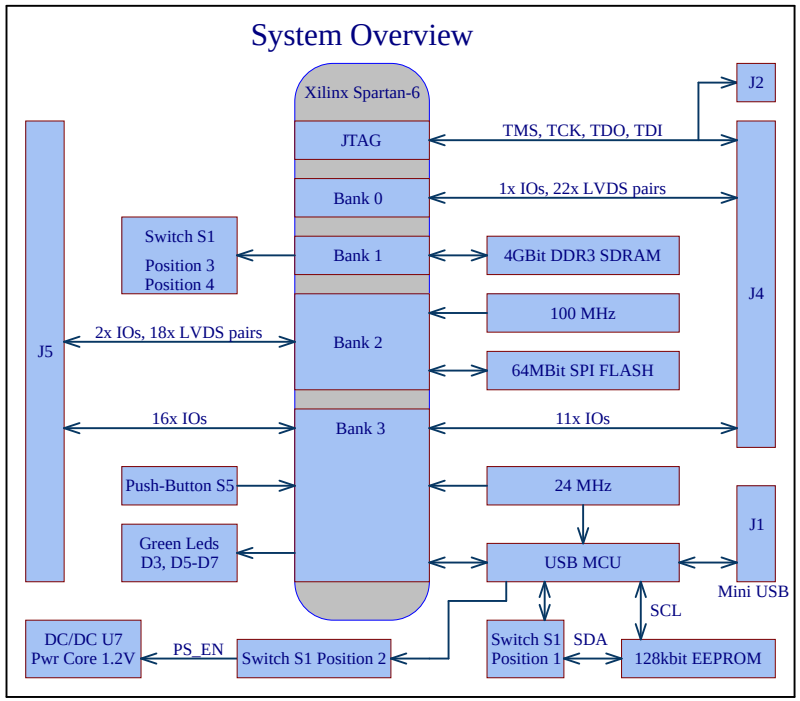
UKCA

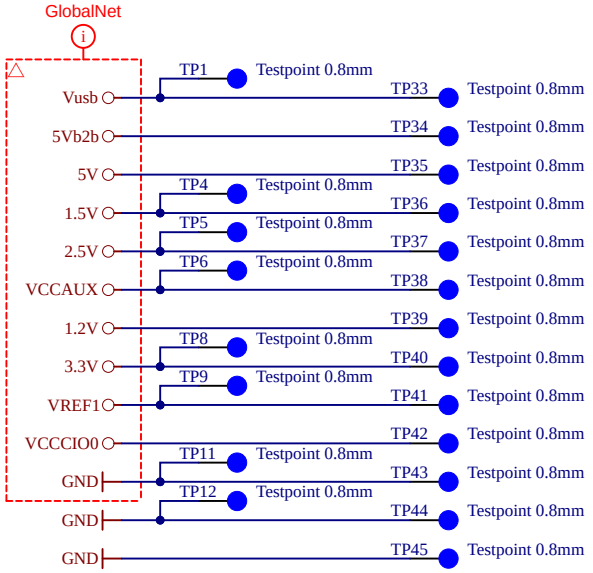
UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

Serial
Serial
Serialnumber 6,3 x 6.3mm

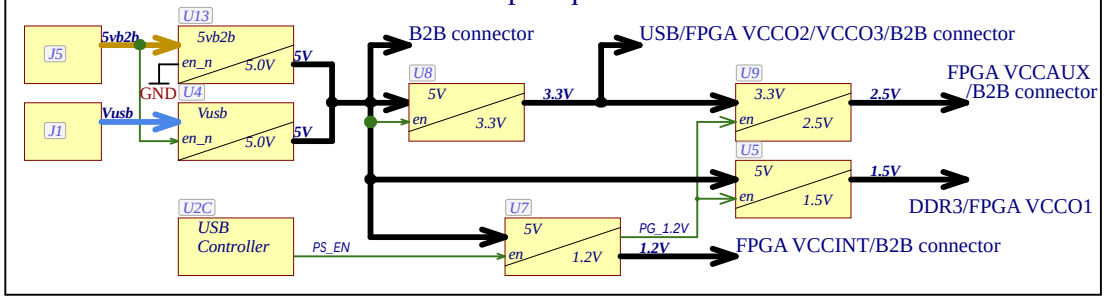
System Overview





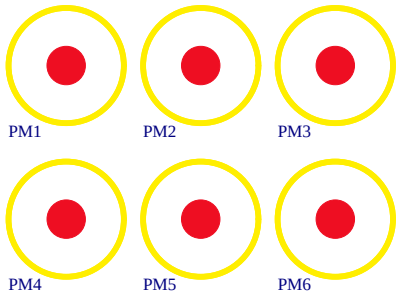
Special notes:

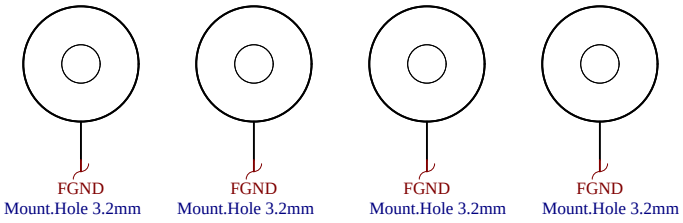
Power Up Sequence




```
BR0 BR1 BR2 BR3  See BR nets on page "FPGA_DDR3.SchDoc"
-----------------------------------------
  0   0   0   0 | -00 Initial revision
  1   0   0   0 | -01
  0   1   0   0 | -02
  1   1   0   0 | -03
```

Assembly variant	52I12-A
Created by	MT
Modified by	MT
Modified at	2023-09-20





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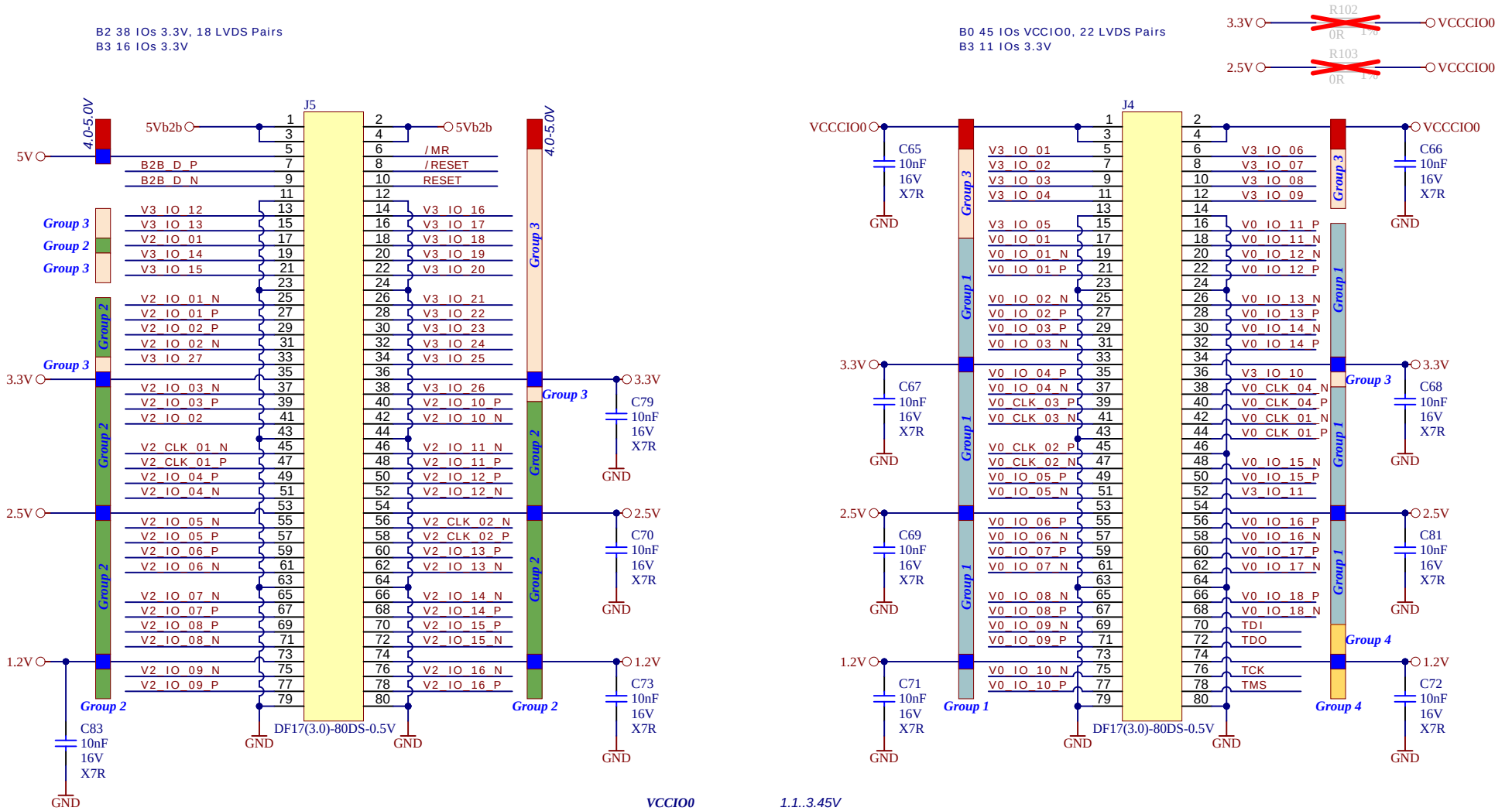
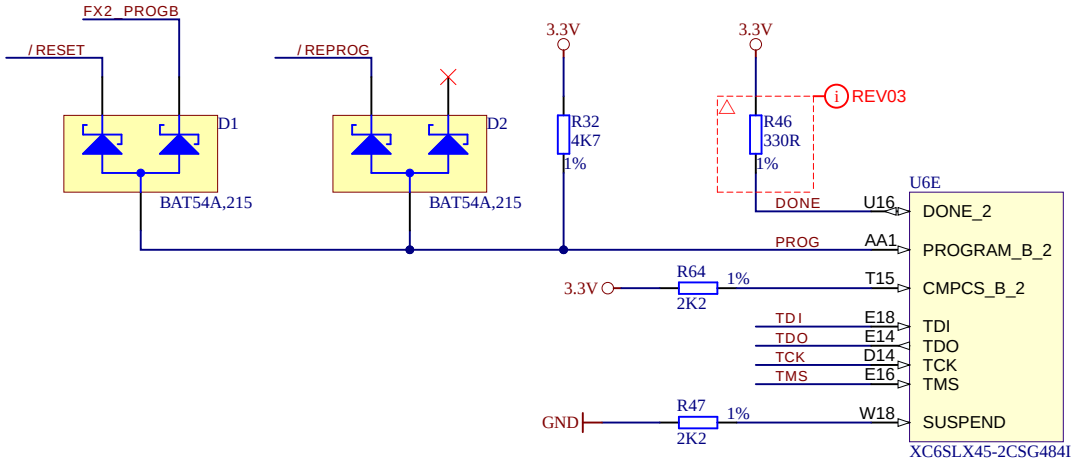
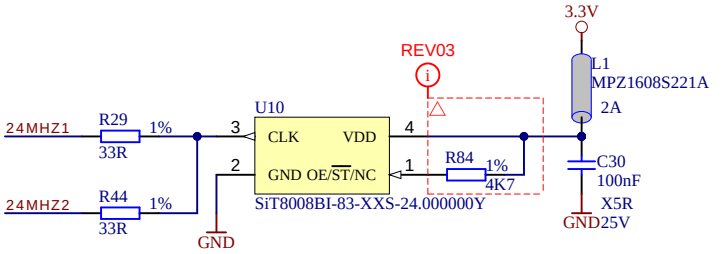
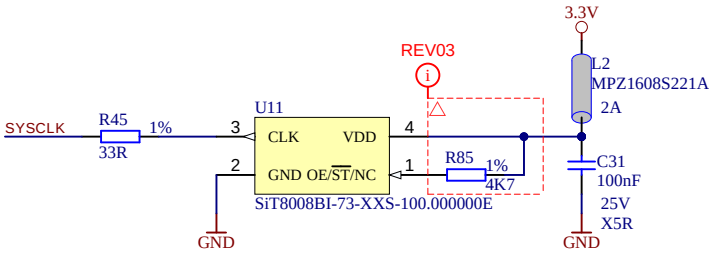
Title: TE0630		
A4	Number: TE0630 52I12-A	Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH	Page 3 of 13
Filename: TE0630.SchDoc		

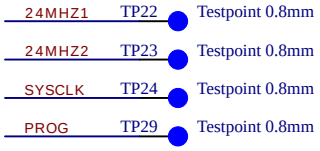


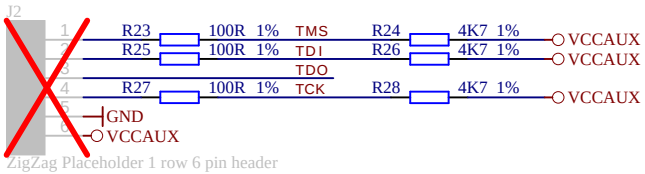
Title: TE0630 - B2B_Connectors			
A4	Number: TE0630 52I12-A		Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH		Page 4 of 13
Filename: B2B_Connectors.SchDoc			











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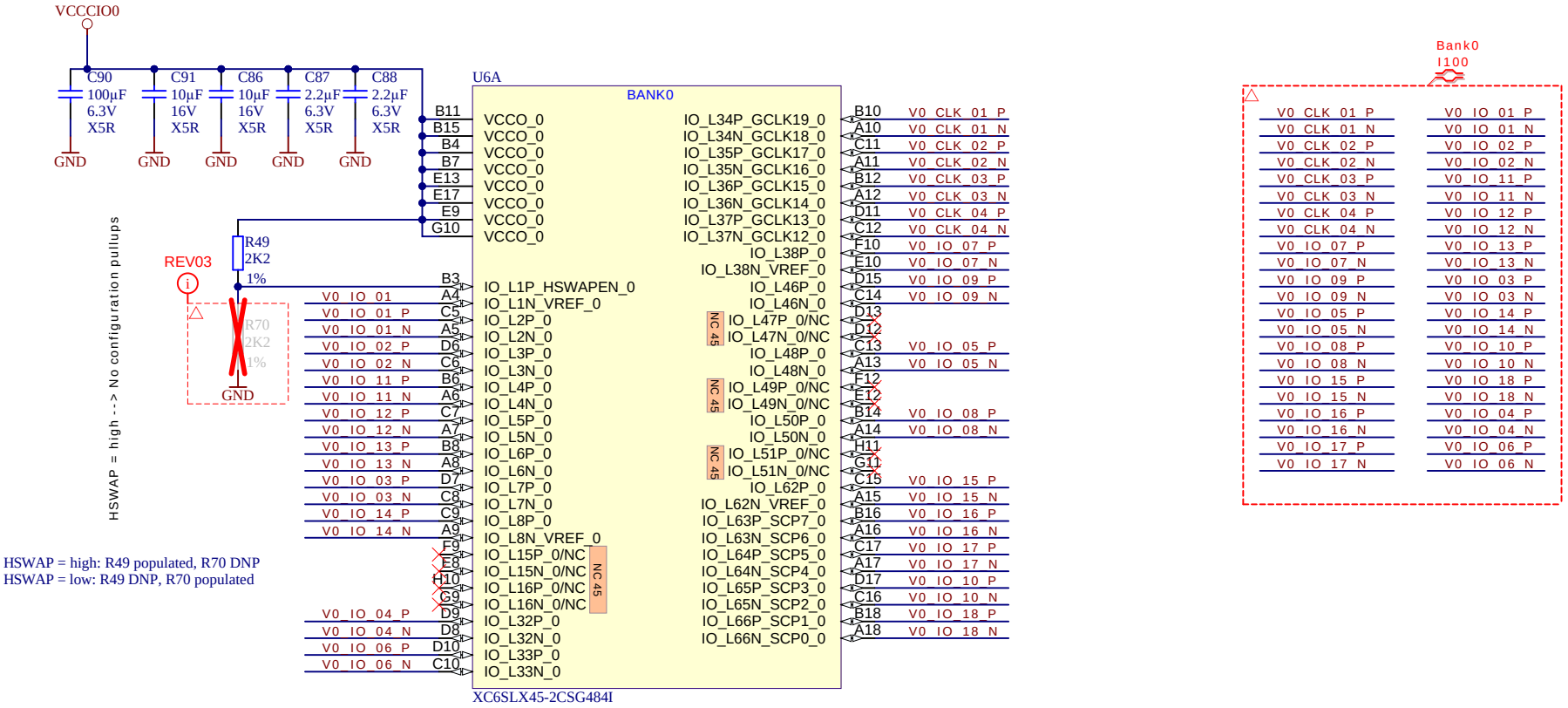
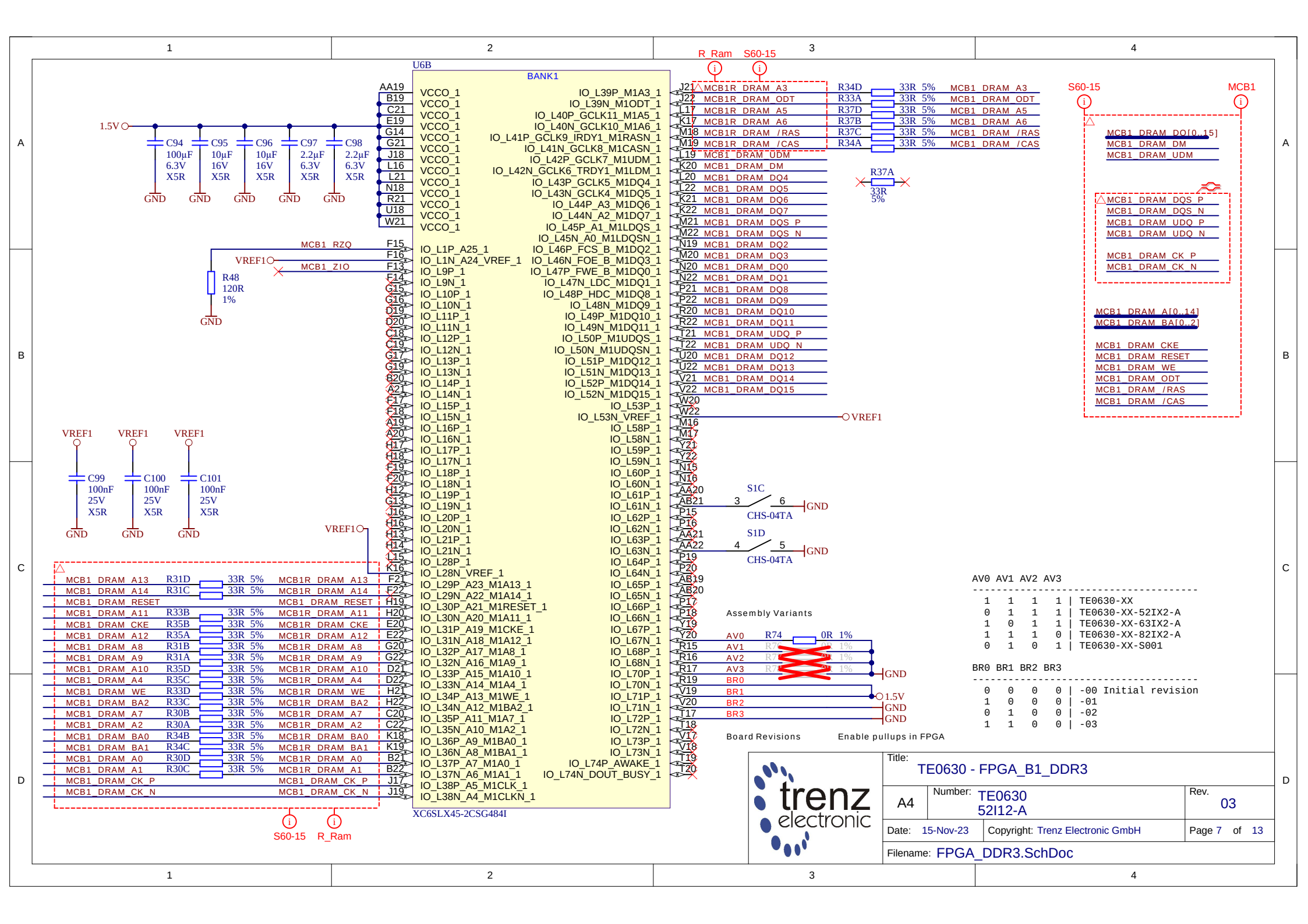
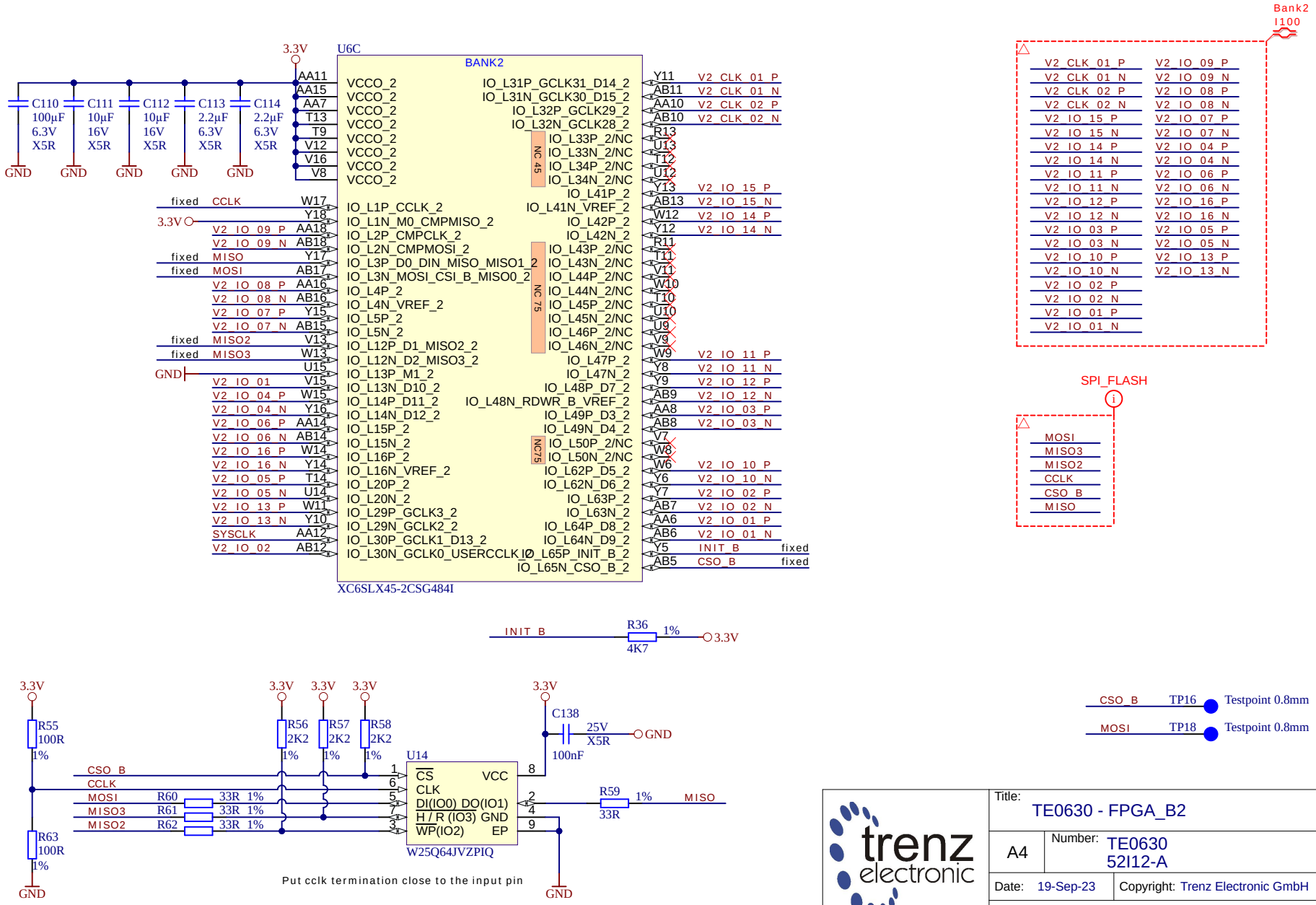
Title: TE0630 - FPGA_CFG_CLK		
A4	Number: TE0630 52I12-A	Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH	Page 5 of 13
Filename: FPGA_CFG_CLK.SchDoc		

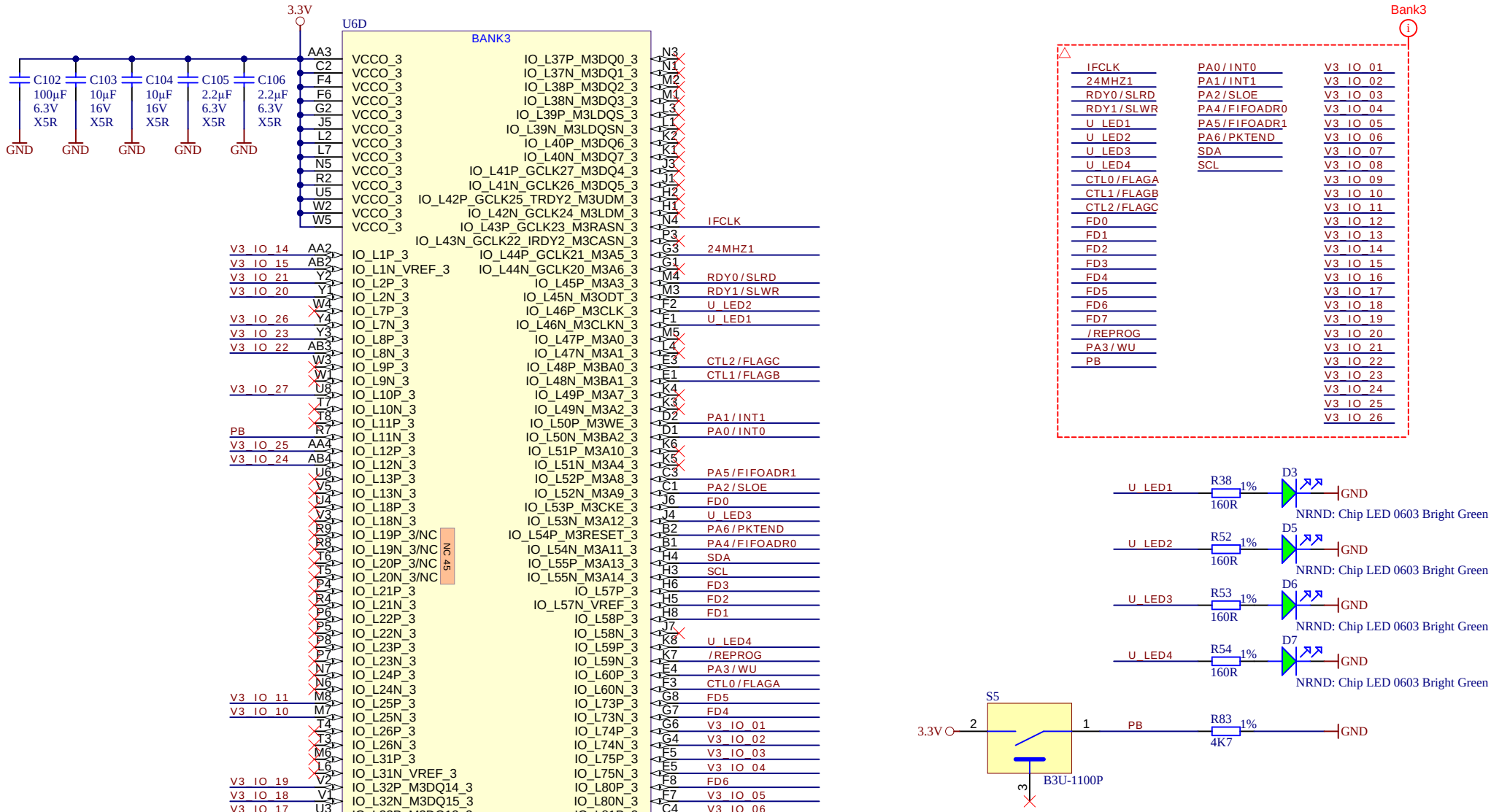


Title: TE0630 - FPGA_B0			
A4	Number: TE0630 52I12-A		Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH		Page 6 of 13
Filename: FPGA_B0.SchDoc			

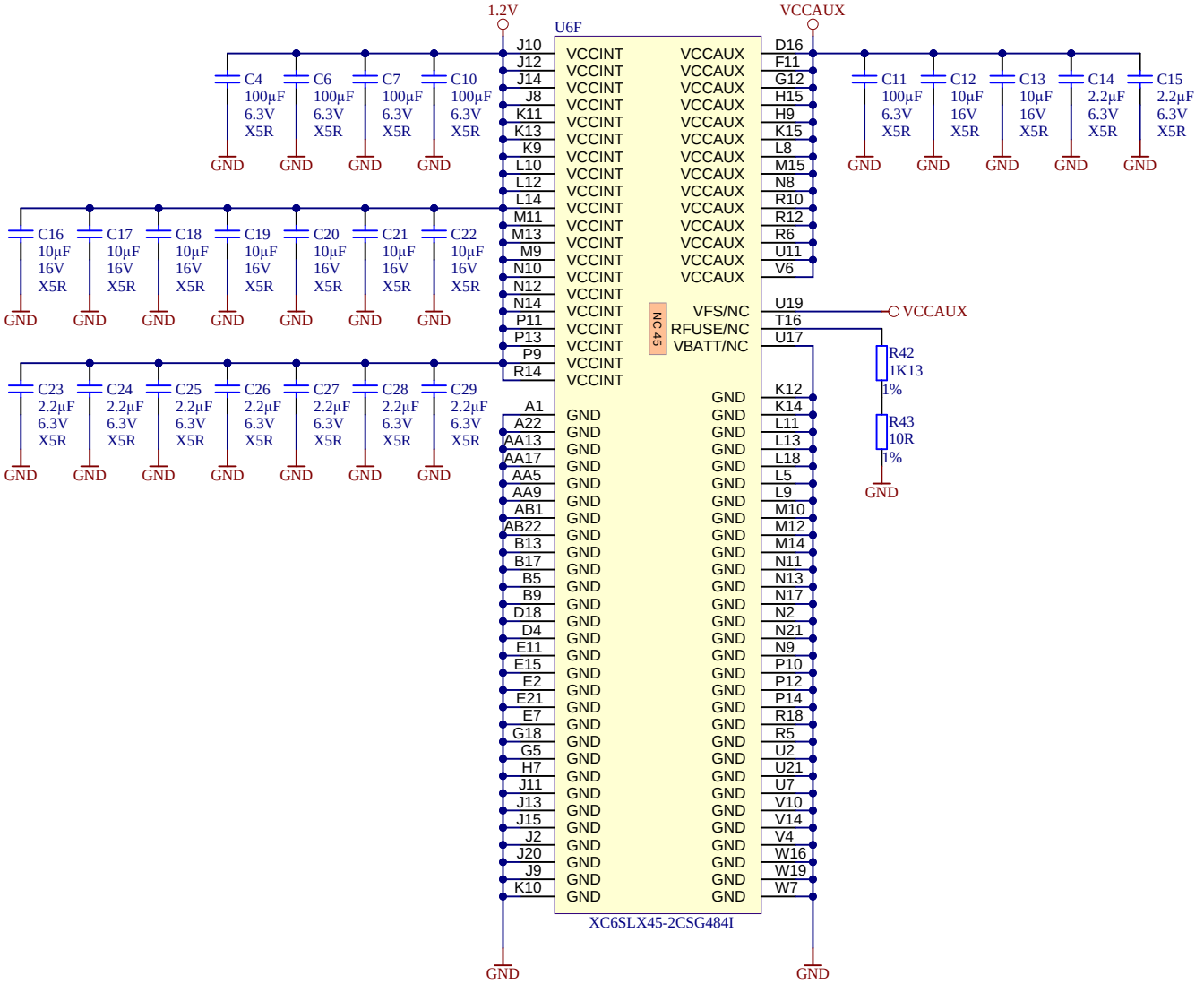

U6B
BANK1
XC6SLX45-2CSG484I
1.5V
C94 100µF 6.3V X5R
C95 10µF 16V X5R
C96 10µF 16V X5R
C97 2.2µF 6.3V X5R
C98 2.2µF 6.3V X5R
GND
MCB1_RZQ
MCB1_ZIO
VREF1
R48 120R 1%
C99 100nF 25V X5R
C100 100nF 25V X5R
C101 100nF 25V X5R
R_Ram
S60-15
MCB1
R34D 33R 5% MCB1_DRAM_A3
R33A 33R 5% MCB1_DRAM_ODT
R37D 33R 5% MCB1_DRAM_A5
R37B 33R 5% MCB1_DRAM_A6
R37C 33R 5% MCB1_DRAM_/RAS
R34A 33R 5% MCB1_DRAM_/CAS
R37A 33R 5%
MCB1_DRAM_DQ[0..15]
MCB1_DRAM_DM
MCB1_DRAM_UDM
MCB1_DRAM_DQS_P
MCB1_DRAM_DQS_N
MCB1_DRAM_UDQ_P
MCB1_DRAM_UDQ_N
MCB1_DRAM_CK_P
MCB1_DRAM_CK_N
MCB1_DRAM_A[0..14]
MCB1_DRAM_BA[0..2]
MCB1_DRAM_CKE
MCB1_DRAM_RESET
MCB1_DRAM_WE
MCB1_DRAM_ODT
MCB1_DRAM_/RAS
MCB1_DRAM_/CAS
S1C CHS-04TA
S1D CHS-04TA
Assembly Variants
AV0 R74 0R 1%
AV1 R75 0R 1%
AV2 R76 0R 1%
AV3 R77 0R 1%
BR0
BR1
BR2
BR3
1.5V
Board Revisions
Enable pullups in FPGA
AV0 AV1 AV2 AV3
1 1 1 1 | TE0630-XX
0 1 1 1 | TE0630-XX-52IX2-A
1 0 1 1 | TE0630-XX-63IX2-A
1 1 1 0 | TE0630-XX-82IX2-A
0 1 0 1 | TE0630-XX-S001
BR0 BR1 BR2 BR3
0 0 0 0 | -00 Initial revision
1 0 0 0 | -01
0 1 0 0 | -02
1 1 0 0 | -03
trenz electronic
Title: TE0630 - FPGA_B1_DDR3
A4
Number: TE0630 52I12-A
Rev. 03
Date: 15-Nov-23
Copyright: Trenz Electronic GmbH
Page 7 of 13
Filename: FPGA_DDR3.SchDoc



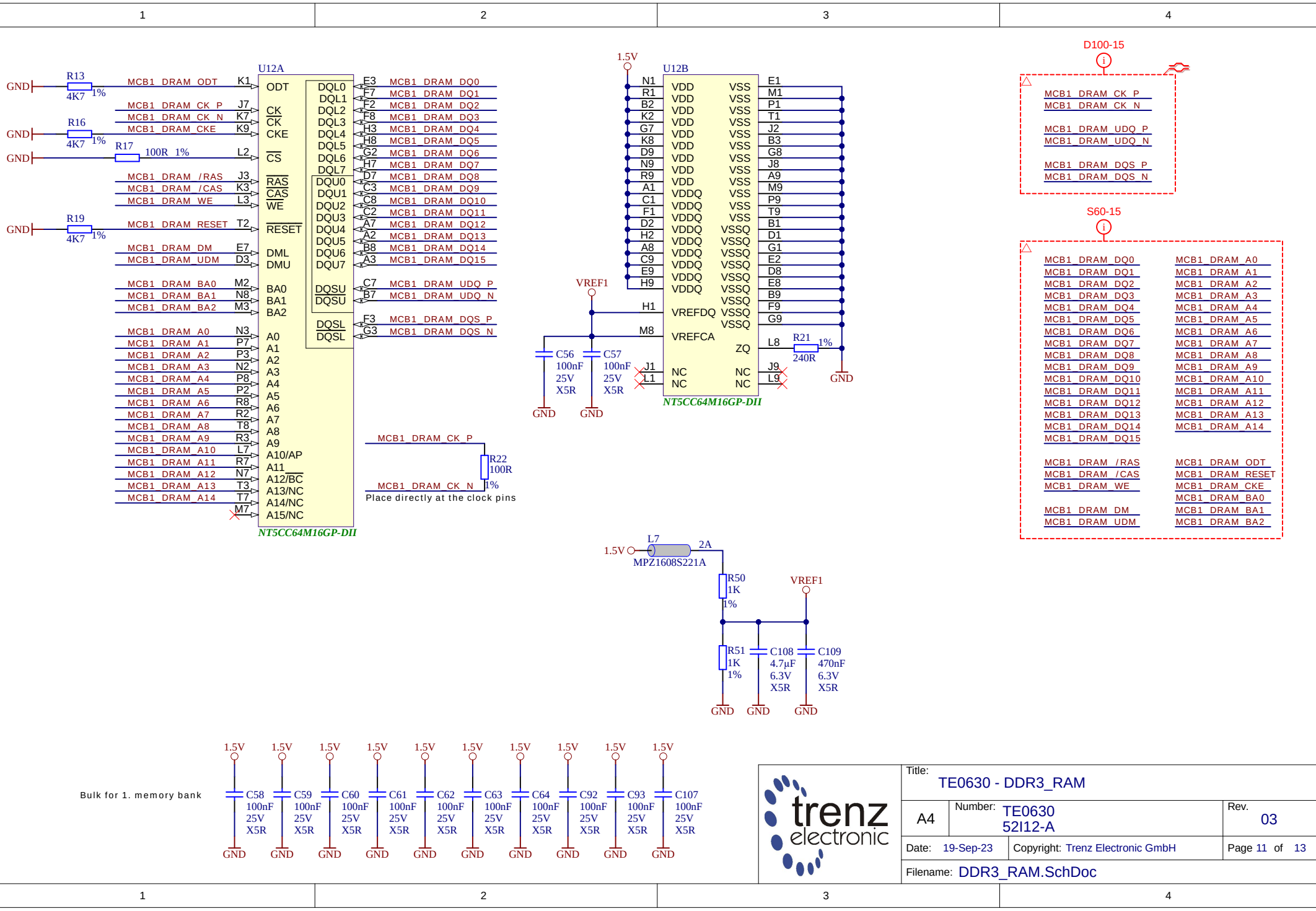
Title: TE0630 - FPGA_B2			
A4	Number: TE0630 52I12-A		Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH		Page 8 of 13
Filename: FPGA_B2.SchDoc			



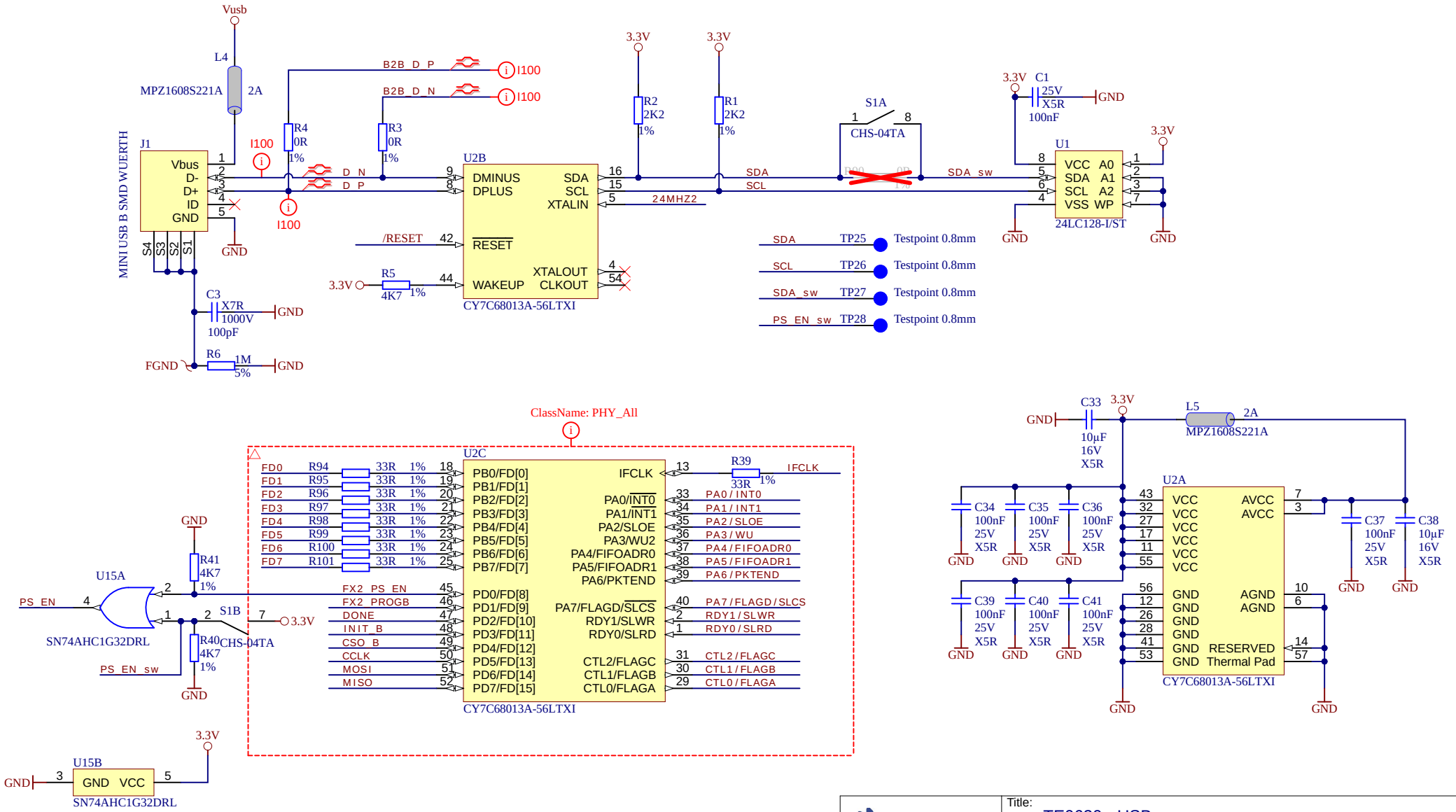
Title: TE0630 - FPGA_B3			
A4	Number: TE0630 52I12-A		Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH		Page 9 of 13
Filename: FPGA_B3.SchDoc			



trenz electronic	Title: TE0630 - FPGA_PWR		
A4	Number: TE0630 52I12-A		Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH		Page 10 of 13
Filename: FPGA_PWR.SchDoc			



Title:	TE630 - DDR3_RAM
A4	Number: TE0630 52I12-A
Rev.	03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH
Page 11 of 13	
Filename:	DDR3_RAM.SchDoc


Vusb
L4
MPZ1608S221A
2A
J1
MINI USB B SMD WUERTH
Vbus
D-
D+
ID
GND
S4
S3
S2
S1
B2B_D_P
B2B_D_N
I100
R4
0R
1%
R3
0R
1%
D_N
D_P
C3
X7R
1000V
100pF
R6
1M
5%
FGND
U2B
DMINUS
DPLUS
SDA
SCL
XTALIN
RESET
XTALOUT
WAKEUP
CLKOUT
CY7C68013A-56LTXI
/RESET
R5
4K7
1%
24MHZ2
3.3V
R2
2K2
1%
R1
2K2
1%
S1A
CHS-04TA
SDA_sw
PS_EN_sw
TP25
TP26
TP27
TP28
Testpoint 0.8mm
C1
25V
X5R
100nF
U1
VCC
SDA
SCL
VSS
A0
A1
A2
WP
24LC128-I/ST
ClassName: PHY_All
U2C
FD0
FD1
FD2
FD3
FD4
FD5
FD6
FD7
R94
R95
R96
R97
R98
R99
R100
R101
33R
PB0/FD[0]
PB1/FD[1]
PB2/FD[2]
PB3/FD[3]
PB4/FD[4]
PB5/FD[5]
PB6/FD[6]
PB7/FD[7]
PD0/FD[8]
PD1/FD[9]
PD2/FD[10]
PD3/FD[11]
PD4/FD[12]
PD5/FD[13]
PD6/FD[14]
PD7/FD[15]
FX2_PS_EN
FX2_PROGB
DONE
INIT_B
CSO_B
CCLK
MOSI
MISO
IFCLK
R39
PA0/INT0
PA1/INT1
PA2/SLOE
PA3/WU2
PA4/FIFOADR0
PA5/FIFOADR1
PA6/PKTEND
PA7/FLAGD/SLCS
RDY1/SLWR
RDY0/SLRD
CTL2/FLAGC
CTL1/FLAGB
CTL0/FLAGA
U15A
SN74AHC1G32DRL
R41
4K7
R40
S1B
U15B
GND VCC
C33
10µF
16V
X5R
L5
MPZ1608S221A
U2A
VCC
AVCC
AGND
RESERVED
Thermal Pad
C34
C35
C36
C37
C38
C39
C40
C41
100nF
10µF
Title: TE0630 - USB
A4
Number: TE0630 52I12-A
Rev. 03
Date: 06-Nov-23
Copyright: Trenz Electronic GmbH
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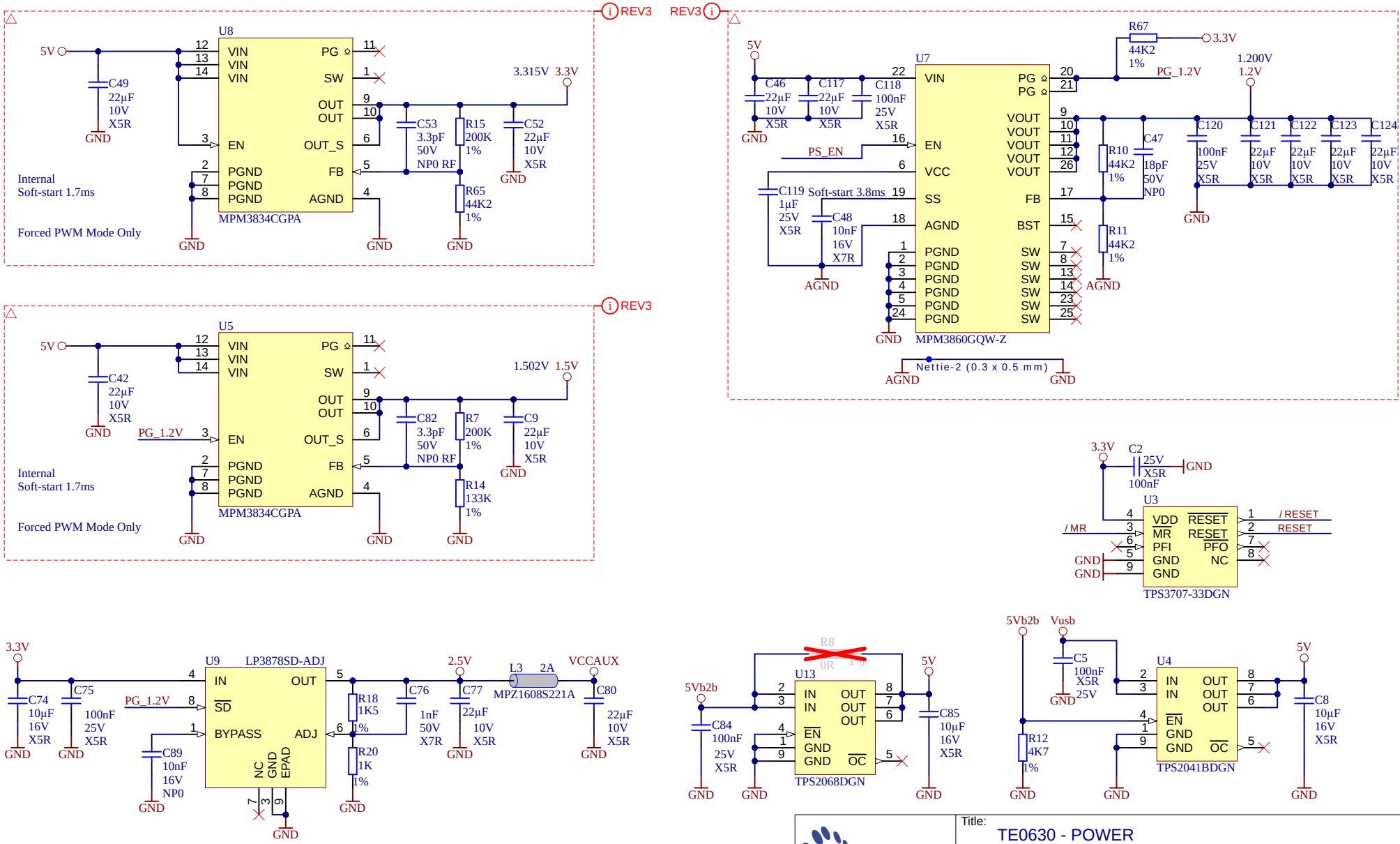
Filename: USB.SchDoc


U8
MPM3834CGPA
5V
3.315V 3.3V
Internal
Soft-start 1.7ms
Forced PWM Mode Only
U5
MPM3834CGPA
1.502V 1.5V
PG_1.2V
U7
MPM3860GQW-Z
PS_EN
Soft-start 3.8ms
Nettie-2 (0.3 x 0.5 mm)
U3
TPS3707-33DGN
/MR
/RESET
U9
LP3878SD-ADJ
2.5V
VCCAUX
MPZ1608S221A
U13
TPS2068DGN
5Vb2b
U4
TPS2041BDGN
Vusb
Title: TE0630 - POWER
A4
Number: TE0630 52I12-A
Rev. 03
Date: 19-Sep-23
Copyright: Trenz Electronic GmbH
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Filename: Power.SchDoc