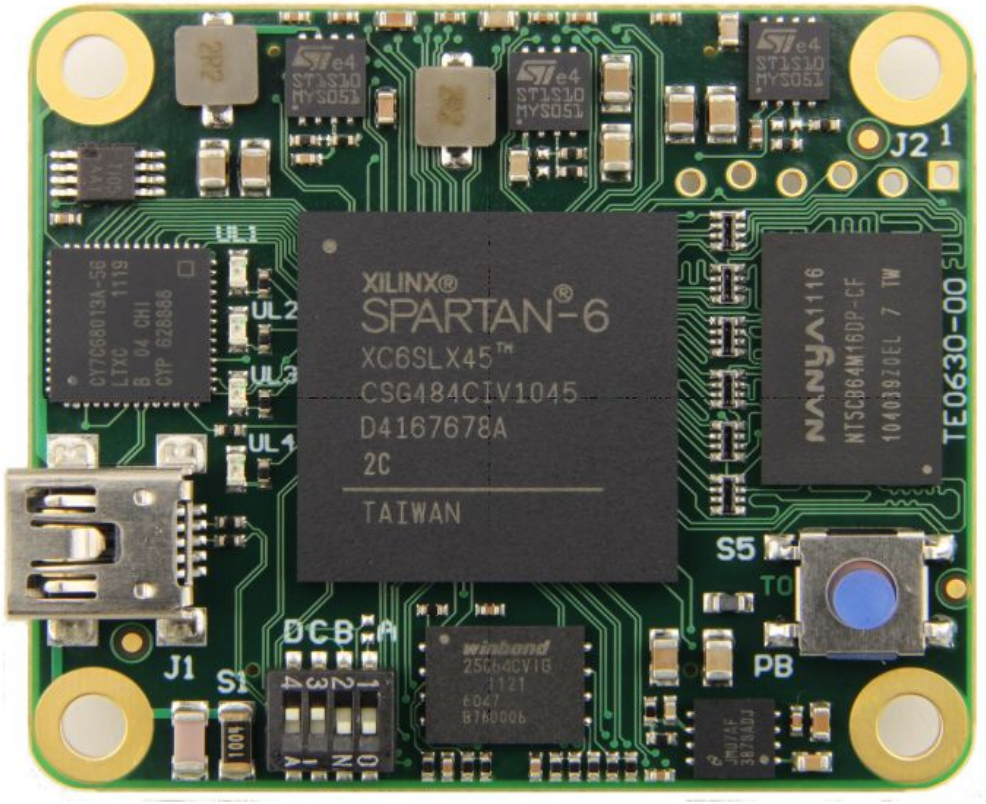

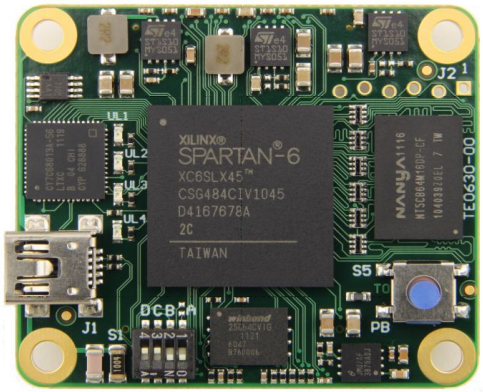

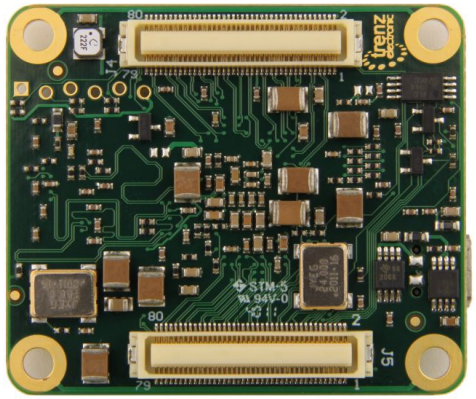

Regarding the usage of our schematics and alike documentation for Trenz module TE0630.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0630 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: TE0630 - Legal Notices Modules		
	A4	Number: TE0630 63I12-A	Rev. 03
	Date: 19-Sep-23	Copyright: Trenz Electronic GmbH	Page 1 of 13
	Filename: Legal_Notices.SchDoc		

REV	Description	
-01	Initial revision	
-02	1) Replaced U8 by EN6338QI 2) Rerouted nets around U8, results in new track length for: Signal V3_IO_06 15.2475 mm (was 15.0047mm) Signal V3_IO_07 16.0151 mm (was 15.0452 mm) 3) Replaced U5 by EN 6338QI 4) PS_EN now via OR gate 5) Replaced obsolete Diodes D1, D2 D4, by BAT54A 6) Fixed Footprint of U10 according to datasheet 7) Update from LIB 8) Rearranged Testpoints 9) Added Traceability Pad 10) Replaced S5 by smaller PB AN26337 11) Hardware revision coding updated to Rev02 12) Flash change (U14) 2020-03-30	
-03	1) All sch and pcb components were updated 2) R46 was changed to 330 Ohm 3) "TE0630.SchDoc" page was updated: System Overview was redesigned, Power Up Sequence was added, S/N1 Serialnumber was removed 4) U7 was changed from EN6347QI to MPM3860GQW-Z 5) U8 and U5 were changed from EN6338QI to MPM3834CGPA 6) Added pullups R84 and R85 for ST pin of U10 and U11 on page "FPGA_CFG_CLK.SchDoc" 7) TE logo was changed to UKCA Logo on page "TE0630.SchDoc" 8) "B2B_Connectors.SchDoc" page was updated: service information about IOs pins was added, colored signal groups were added 9) BR0 net was pulled to 1.5V on page "FPGA_DDR3.SchDoc" 10) U12 was changed from NT5CC64M16GP-DII to IS43TR16256BL-125KBLI 11) Assembly option. Pull down resistor R70 was added on page "FPGA_B0.SchDoc" 12) Assembly Variants table was changed on page "FPGA_DDR3.SchDoc": obsolete variants were deleted, new assembly variants were added 13) "Legal_Notices.SchDoc" page was added 14) Parameters of some capacitors were changed: C77 , C80 : 6.3V -> 10V 15) Fiducials PM1-PM6 were updated and moved for same positions on top and bottom layers 16) Removed testpoints TP2,TP3,TP7,TP10,TP13,TP14,TP15,TP17, TP19,TP20,TP21, TP27,TP28,TP30,TP31,TP32 17) Added testpoints TP27 and TP28 on page "USB.SchDoc" 18) Some net classes names were deleted: "MatchLendht150Mil", "MatchLendht300Mil", "Clear_10mil", "S50-33" 19) Net class "3Bank2Half" was renamed to "Bank3"	MT

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Title: TE0630 - Changes list		
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Filename: Revision_Changes.SchDoc		

U_Power
Power.SchDoc

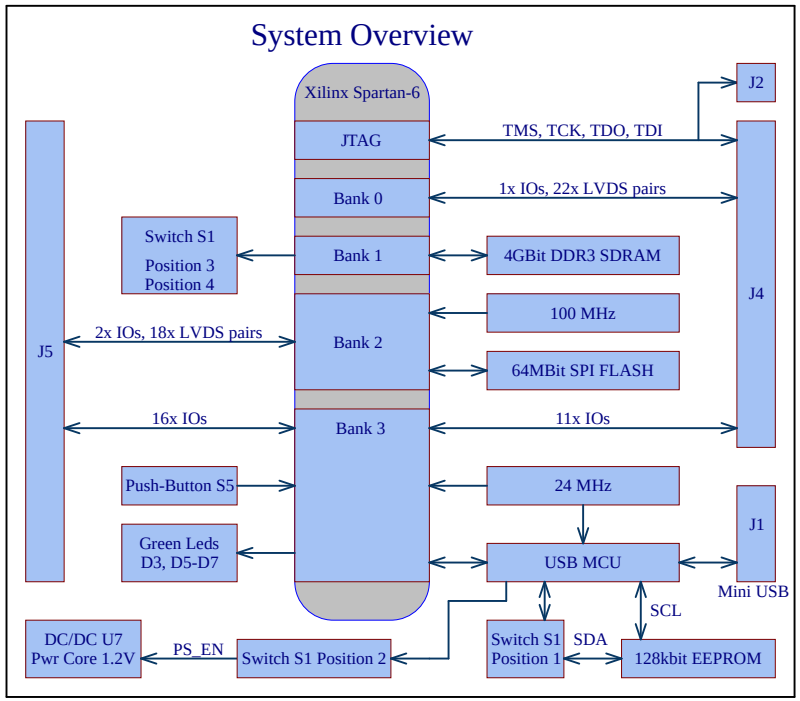
U_FPGA_PWR
FPGA_PWR.SchDoc

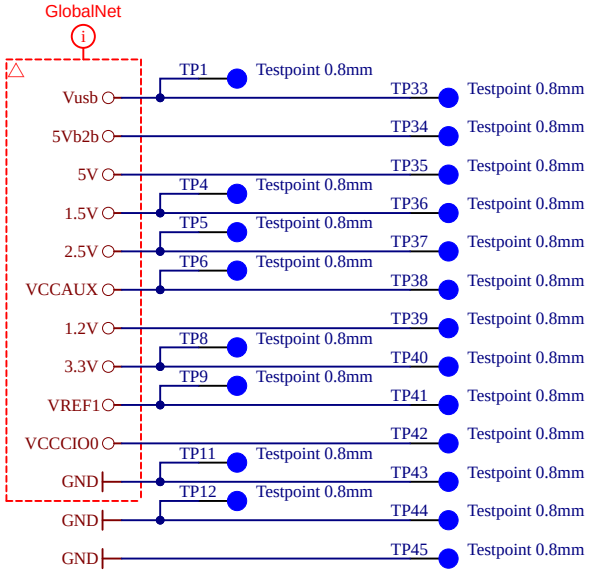
UKCA

UKCA Logo on Top Overlay

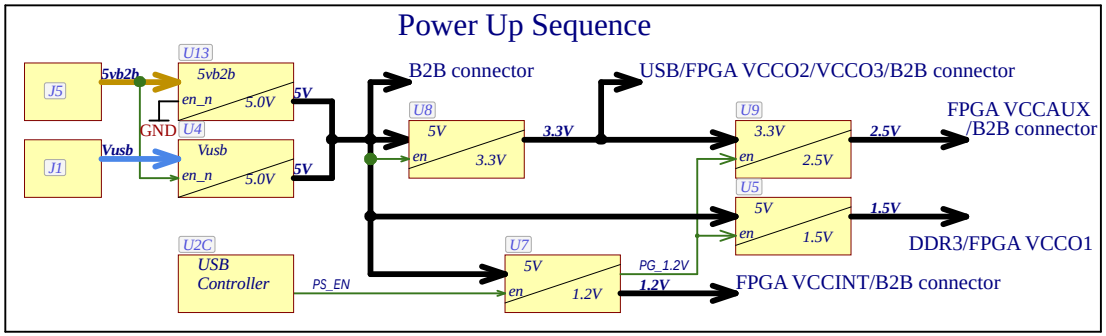
UKCA-TOPOVERLAY

Serial
Serial
Serialnumber 6,3 x 6.3mm



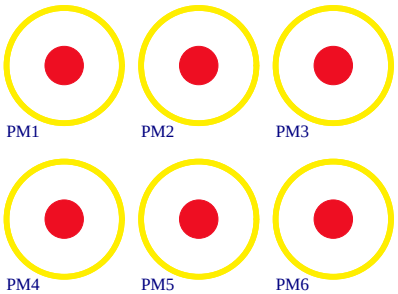


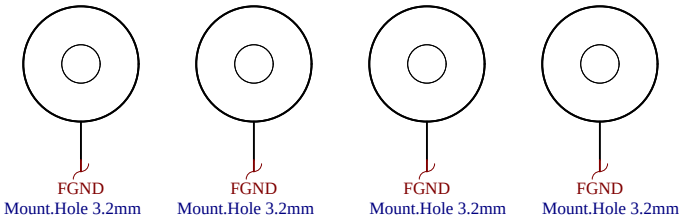
Special notes:




```
BR0 BR1 BR2 BR3  See BR nets on page "FPGA_DDR3.SchDoc"
-----------------------------------------
  0   0   0   0 | -00 Initial revision
  1   0   0   0 | -01
  0   1   0   0 | -02
  1   1   0   0 | -03
```

Assembly variant	63I12-A
Created by	MT
Modified by	MT
Modified at	2023-09-20





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Title: TE0630		
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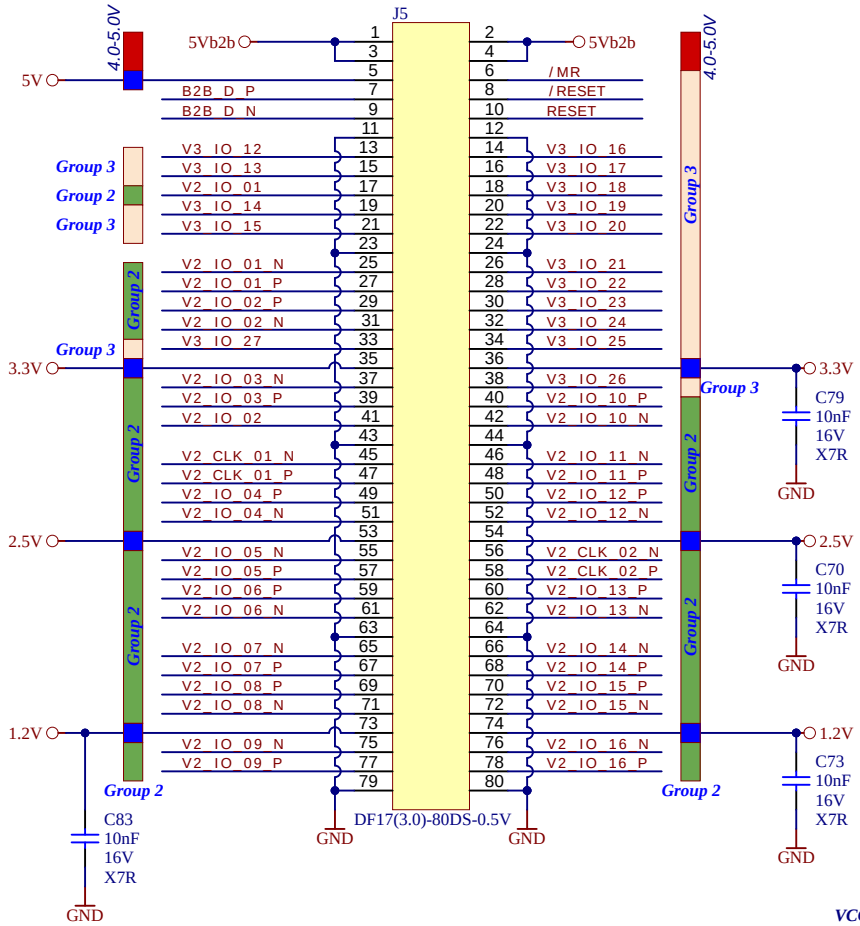
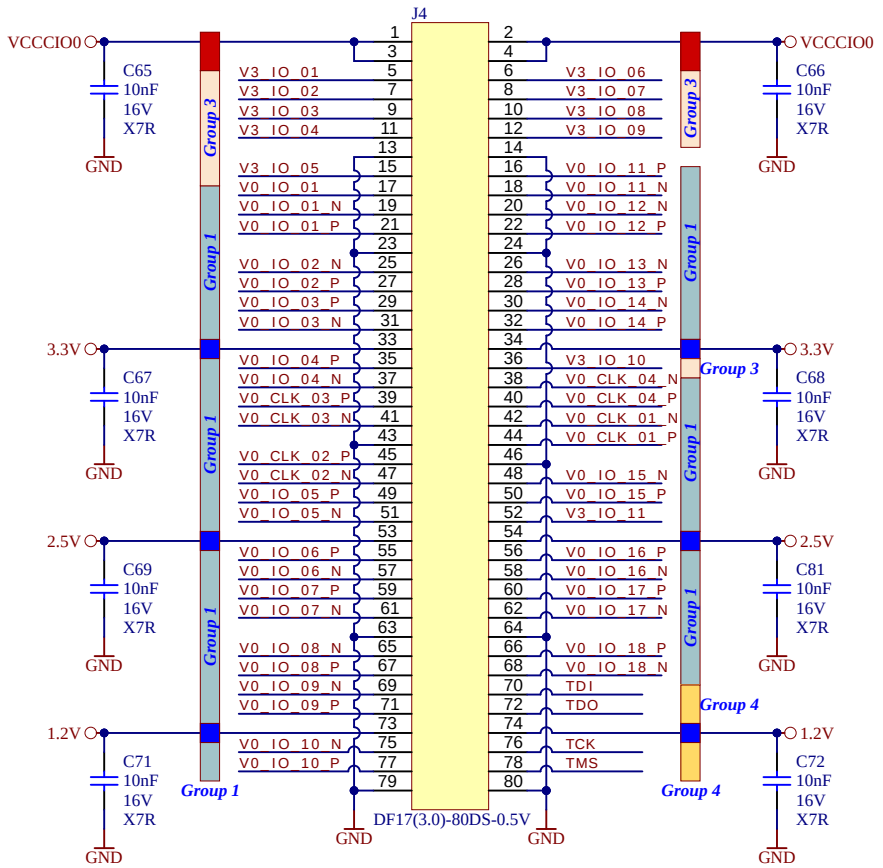
B2 38 IOs 3.3V, 18 LVDS Pairs
B3 16 IOs 3.3V



B0 45 IOs VCCIO0, 22 LVDS Pairs
B3 11 IOs 3.3V



R102 0R
R103 0R

VCCIO0	*1.1..3.45V*
VCCIO2	*3.3V*
VCCIO3	*3.3V*
VCCAUX	*2.5V*
Group 1	*0..VCCIO0*
Group 2	*0..VCCIO2*
Group 3	*0..VCCIO3*
Group 4	*0..VCCAUX*
	PWR in
	PWR out

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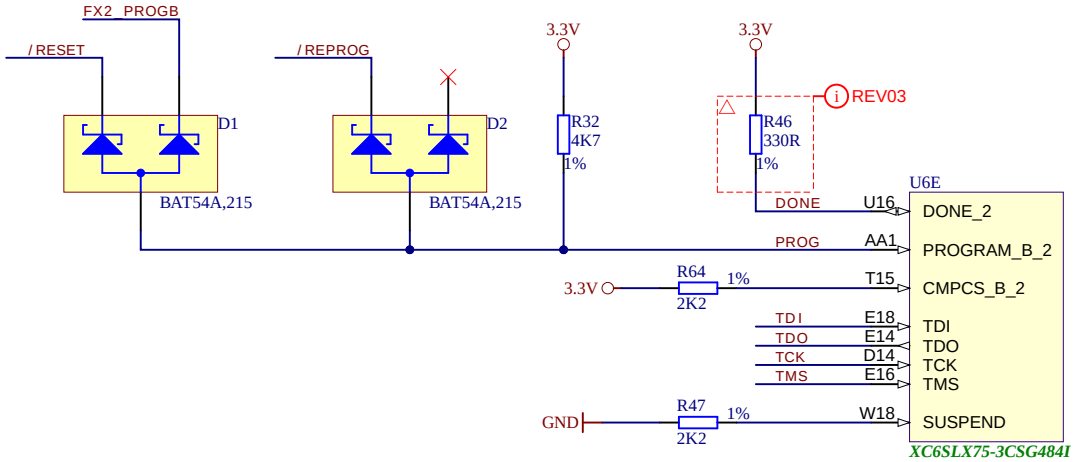
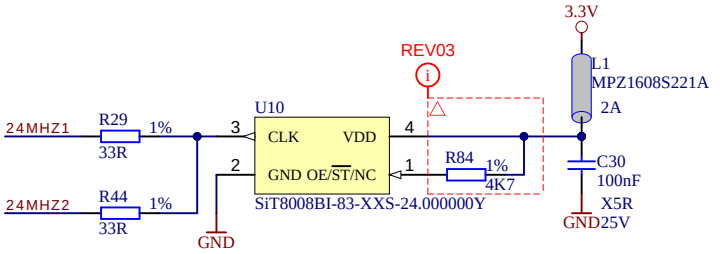
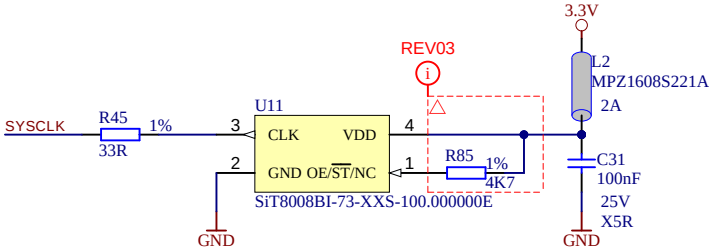
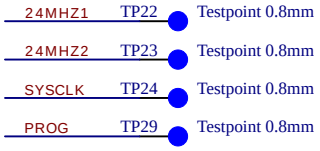
Title: TE0630 - B2B_Connectors

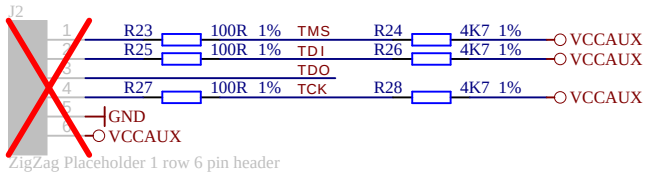
A4	Number: TE0630 63I12-A	Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH	Page 4 of 13
Filename: B2B_Connectors.SchDoc		











trenz electronic	Title: TE0630 - FPGA_CFG_CLK		
A4	Number: TE0630 63I12-A		Rev. 03
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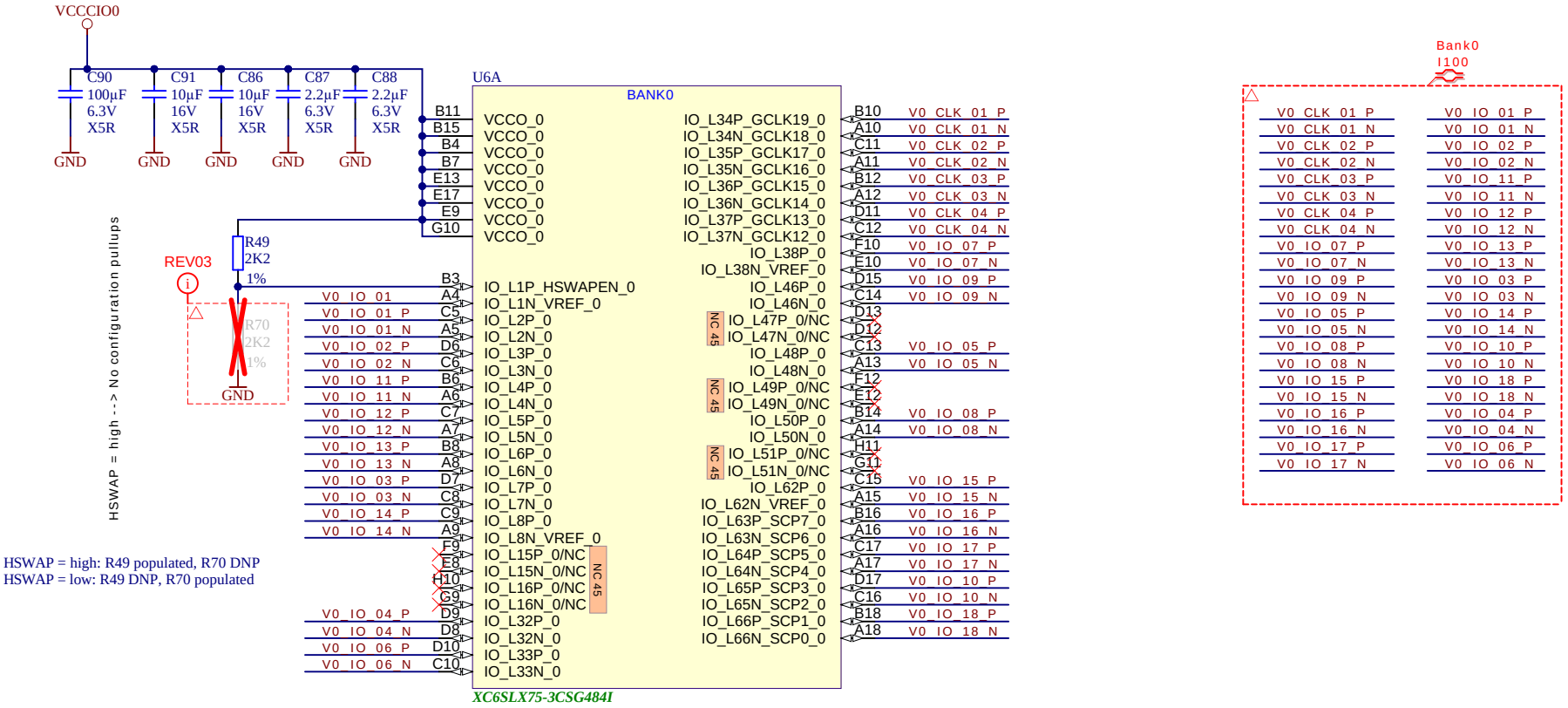
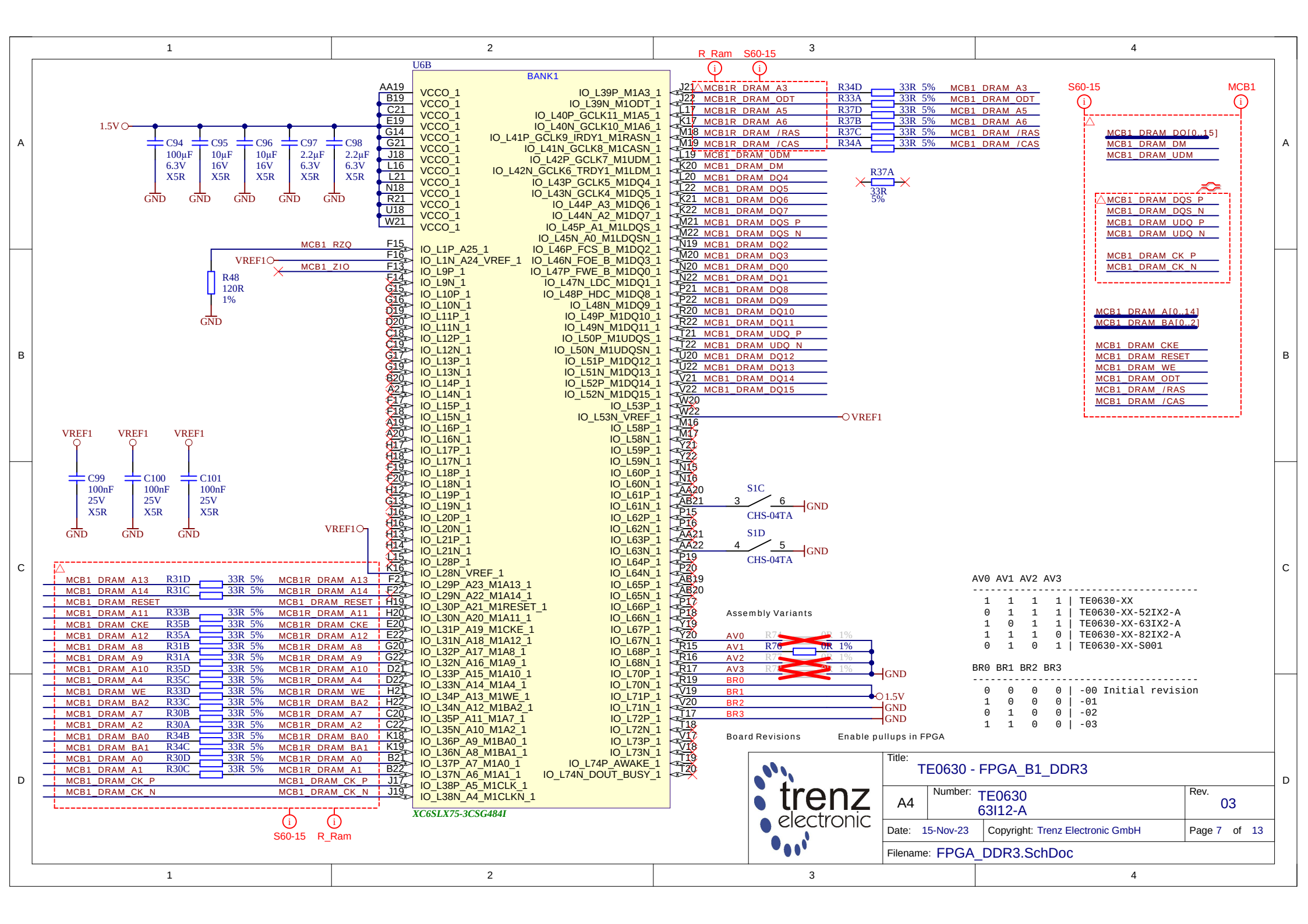
Filename: FPGA_CFG_CLK.SchDoc			



Title: TE0630 - FPGA_B0			
A4	Number: TE0630 63I12-A		Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH		Page 6 of 13
Filename: FPGA_B0.SchDoc			


U6B
BANK1
XC6SLX75-3CSG484I
1.5V
C94 100µF 6.3V X5R
C95 10µF 16V X5R
C96 10µF 16V X5R
C97 2.2µF 6.3V X5R
C98 2.2µF 6.3V X5R
GND
MCB1_RZQ
MCB1_ZIO
VREF1
R48 120R 1%
C99 100nF 25V X5R
C100 100nF 25V X5R
C101 100nF 25V X5R
R_Ram
S60-15
MCB1
R34D R33A R37D R37B R37C R34A 33R 5%
R37A 33R 5%
S1C S1D CHS-04TA
Assembly Variants
AV0 AV1 AV2 AV3
BR0 BR1 BR2 BR3
1.5V
Board Revisions
Enable pullups in FPGA
AV0 AV1 AV2 AV3
1 1 1 1 | TE0630-XX
0 1 1 1 | TE0630-XX-52IX2-A
1 0 1 1 | TE0630-XX-63IX2-A
1 1 1 0 | TE0630-XX-82IX2-A
0 1 0 1 | TE0630-XX-S001
BR0 BR1 BR2 BR3
0 0 0 0 | -00 Initial revision
1 0 0 0 | -01
0 1 0 0 | -02
1 1 0 0 | -03
trenz electronic
Title: TE0630 - FPGA_B1_DDR3
A4
Number: TE0630 63I12-A
Rev. 03
Date: 15-Nov-23
Copyright: Trenz Electronic GmbH
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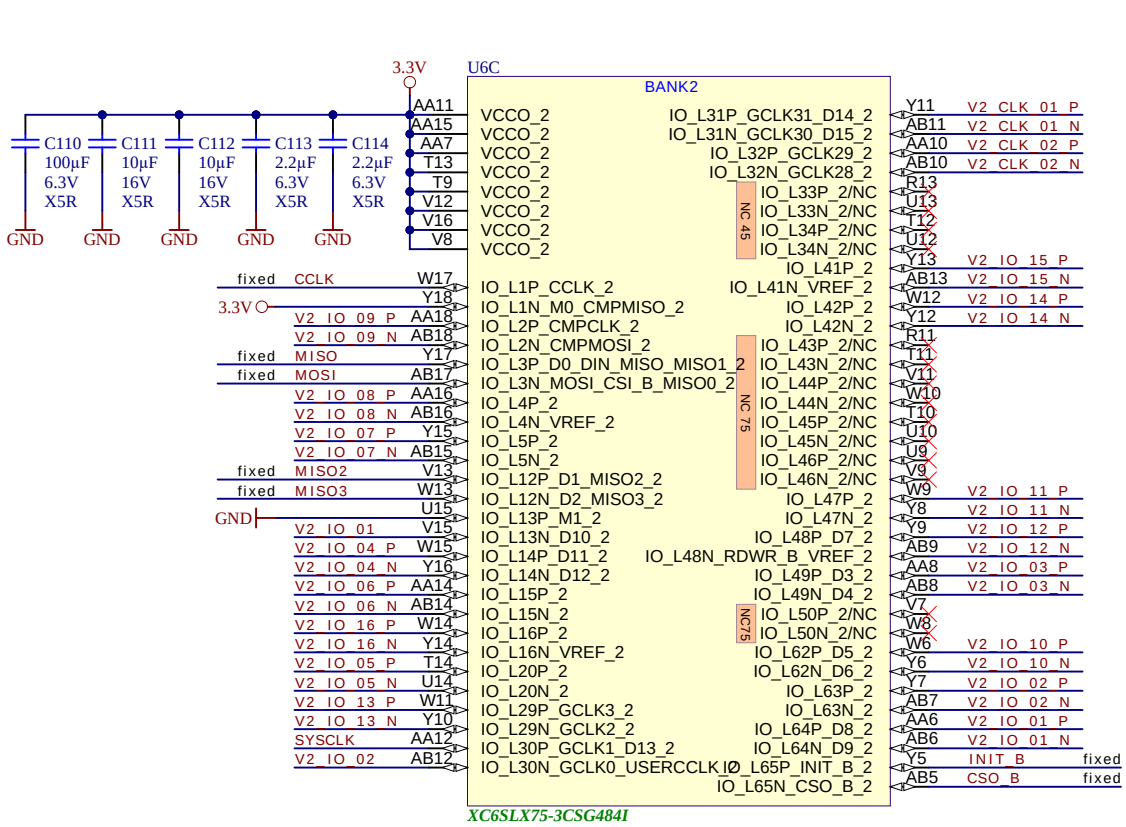
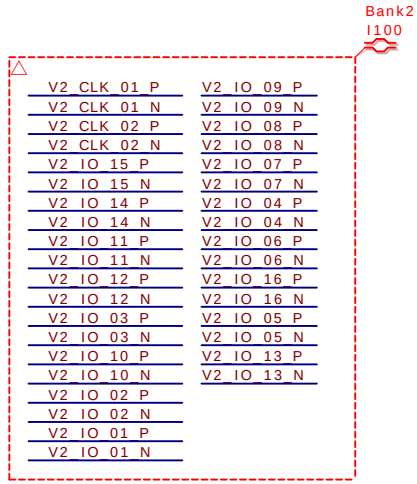
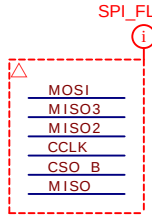
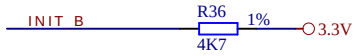
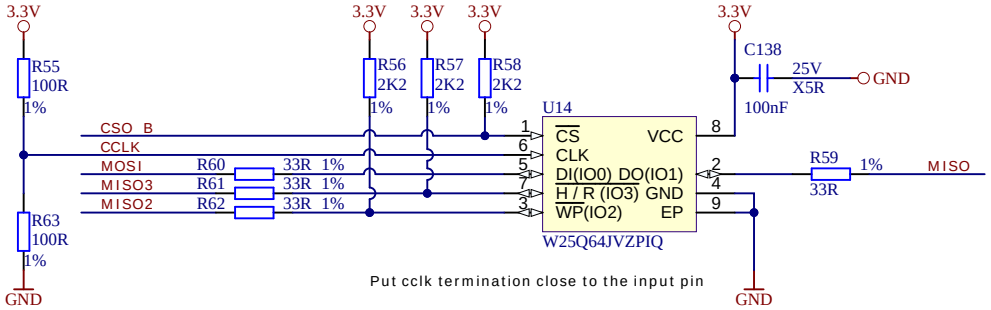
Filename: FPGA_DDR3.SchDoc

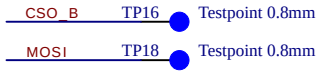












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Title: TE0630 - FPGA_B2		
A4	Number: TE0630 63I12-A	Rev. 03
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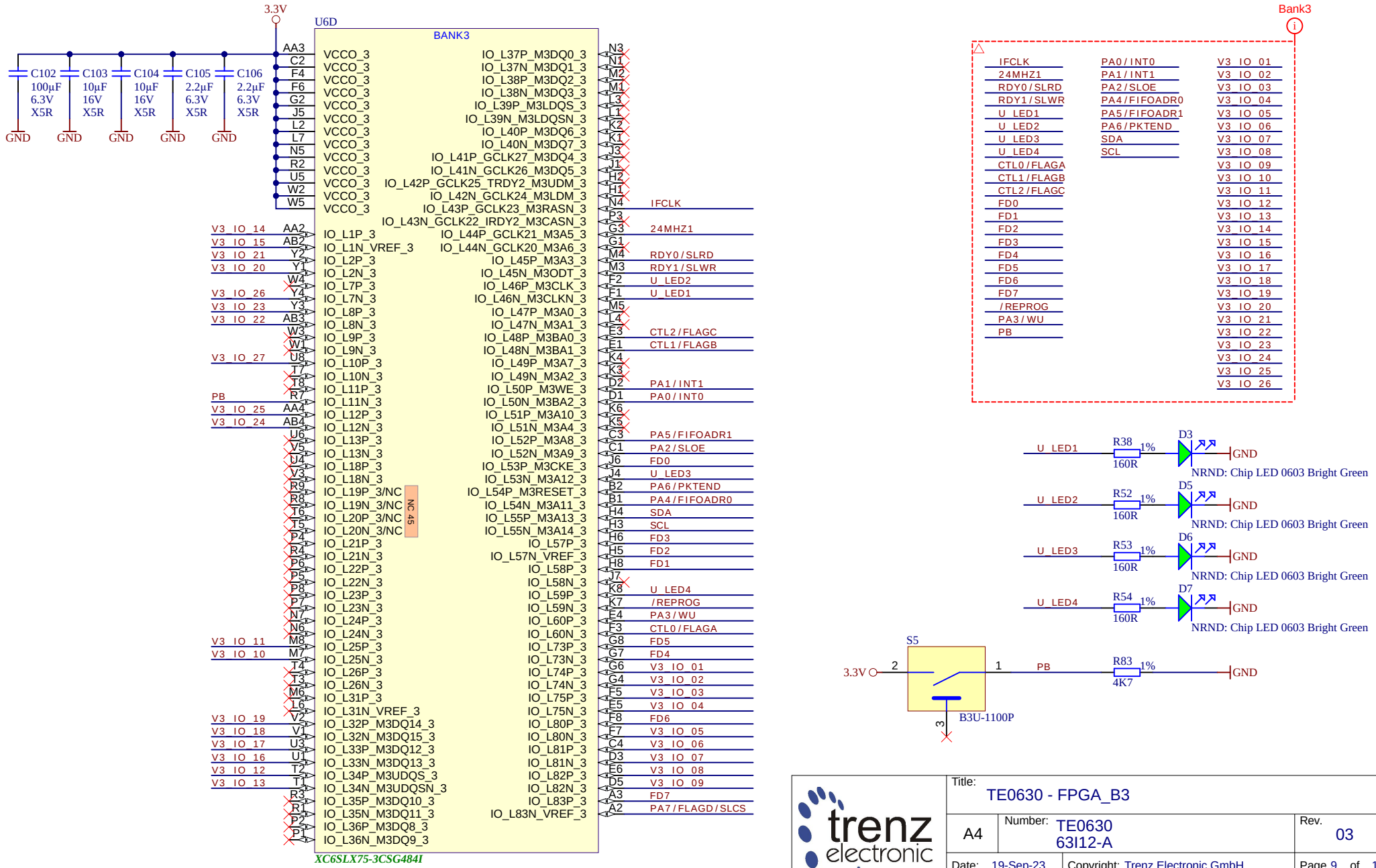
Filename: FPGA_B2.SchDoc		


3.3V
U6D
BANK3
C102 100µF 6.3V X5R
C103 10µF 16V X5R
C104 10µF 16V X5R
C105 2.2µF 6.3V X5R
C106 2.2µF 6.3V X5R
GND
VCCO_3
IO_L37P_M3DQ0_3
IO_L37N_M3DQ1_3
IO_L38P_M3DQ2_3
IO_L38N_M3DQ3_3
IO_L39P_M3LDQS_3
IO_L39N_M3LDQSN_3
IO_L40P_M3DQ6_3
IO_L40N_M3DQ7_3
IO_L41P_GCLK27_M3DQ4_3
IO_L41N_GCLK26_M3DQ5_3
IO_L42P_GCLK25_TRDY2_M3UDM_3
IO_L42N_GCLK24_M3LDM_3
IO_L43P_GCLK23_M3RASN_3
IO_L43N_GCLK22_IRDY2_M3CASN_3
IO_L1P_3
IO_L1N_VREF_3
IO_L44P_GCLK21_M3A5_3
IO_L44N_GCLK20_M3A6_3
IO_L2P_3
IO_L45P_M3A3_3
IO_L2N_3
IO_L45N_M3ODT_3
IO_L7P_3
IO_L46P_M3CLK_3
IO_L7N_3
IO_L46N_M3CLKN_3
IO_L8P_3
IO_L47P_M3A0_3
IO_L8N_3
IO_L47N_M3A1_3
IO_L9P_3
IO_L48P_M3BA0_3
IO_L9N_3
IO_L48N_M3BA1_3
IO_L10P_3
IO_L49P_M3A7_3
IO_L10N_3
IO_L49N_M3A2_3
IO_L11P_3
IO_L50P_M3WE_3
IO_L11N_3
IO_L50N_M3BA2_3
IO_L12P_3
IO_L51P_M3A10_3
IO_L12N_3
IO_L51N_M3A4_3
IO_L13P_3
IO_L52P_M3A8_3
IO_L13N_3
IO_L52N_M3A9_3
IO_L18P_3
IO_L53P_M3CKE_3
IO_L18N_3
IO_L53N_M3A12_3
IO_L19P_3/NC
IO_L54P_M3RESET_3
IO_L19N_3/NC
IO_L54N_M3A11_3
IO_L20P_3/NC
IO_L55P_M3A13_3
IO_L20N_3/NC
IO_L55N_M3A14_3
IO_L21P_3
IO_L57P_3
IO_L21N_3
IO_L57N_VREF_3
IO_L22P_3
IO_L58P_3
IO_L22N_3
IO_L58N_3
IO_L23P_3
IO_L59P_3
IO_L23N_3
IO_L59N_3
IO_L24P_3
IO_L60P_3
IO_L24N_3
IO_L60N_3
IO_L25P_3
IO_L73P_3
IO_L25N_3
IO_L73N_3
IO_L26P_3
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IO_L26N_3
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IO_L75P_3
IO_L31N_VREF_3
IO_L75N_3
IO_L32P_M3DQ14_3
IO_L80P_3
IO_L32N_M3DQ15_3
IO_L80N_3
IO_L33P_M3DQ12_3
IO_L81P_3
IO_L33N_M3DQ13_3
IO_L81N_3
IO_L34P_M3UDQS_3
IO_L82P_3
IO_L34N_M3UDQSN_3
IO_L82N_3
IO_L35P_M3DQ10_3
IO_L83P_3
IO_L35N_M3DQ11_3
IO_L83N_3
IO_L36P_M3DQ8_3
IO_L36N_M3DQ9_3
NC 45
XC6SLX75-3CSG484I
V3_IO_14
V3_IO_15
V3_IO_21
V3_IO_20
V3_IO_26
V3_IO_23
V3_IO_22
V3_IO_27
PB
V3_IO_25
V3_IO_24
V3_IO_11
V3_IO_10
V3_IO_19
V3_IO_18
V3_IO_17
V3_IO_16
V3_IO_12
V3_IO_13
IFCLK
24MHZ1
RDY0/SLRD
RDY1/SLWR
U_LED2
U_LED1
CTL2/FLAGC
CTL1/FLAGB
PA1/INT1
PA0/INT0
PA5/FIFOADR1
PA2/SLOE
FD0
U_LED3
PA6/PKTEND
PA4/FIFOADR0
SDA
SCL
FD3
FD2
FD1
U_LED4
/REPROG
PA3/WU
CTL0/FLAGA
FD5
FD4
V3_IO_01
V3_IO_02
V3_IO_03
V3_IO_04
FD6
V3_IO_05
V3_IO_06
V3_IO_07
V3_IO_08
V3_IO_09
FD7
PA7/FLAGD/SLCS
Bank3
IFCLK
24MHZ1
RDY0/SLRD
RDY1/SLWR
U_LED1
U_LED2
U_LED3
U_LED4
CTL0/FLAGA
CTL1/FLAGB
CTL2/FLAGC
FD0
FD1
FD2
FD3
FD4
FD5
FD6
FD7
/REPROG
PA3/WU
PB
PA0/INT0
PA1/INT1
PA2/SLOE
PA4/FIFOADR0
PA5/FIFOADR1
PA6/PKTEND
SDA
SCL
V3_IO_01
V3_IO_02
V3_IO_03
V3_IO_04
V3_IO_05
V3_IO_06
V3_IO_07
V3_IO_08
V3_IO_09
V3_IO_10
V3_IO_11
V3_IO_12
V3_IO_13
V3_IO_14
V3_IO_15
V3_IO_16
V3_IO_17
V3_IO_18
V3_IO_19
V3_IO_20
V3_IO_21
V3_IO_22
V3_IO_23
V3_IO_24
V3_IO_25
V3_IO_26
U_LED1
R38 160R 1%
D3
GND
NRND: Chip LED 0603 Bright Green
U_LED2
R52 160R 1%
D5
GND
NRND: Chip LED 0603 Bright Green
U_LED3
R53 160R 1%
D6
GND
NRND: Chip LED 0603 Bright Green
U_LED4
R54 160R 1%
D7
GND
NRND: Chip LED 0603 Bright Green
S5
3.3V
2
1
PB
R83 4K7 1%
GND
3
B3U-1100P
trenz electronic
Title: TE0630 - FPGA_B3
A4
Number: TE0630 63I12-A
Rev. 03
Date: 19-Sep-23
Copyright: Trenz Electronic GmbH
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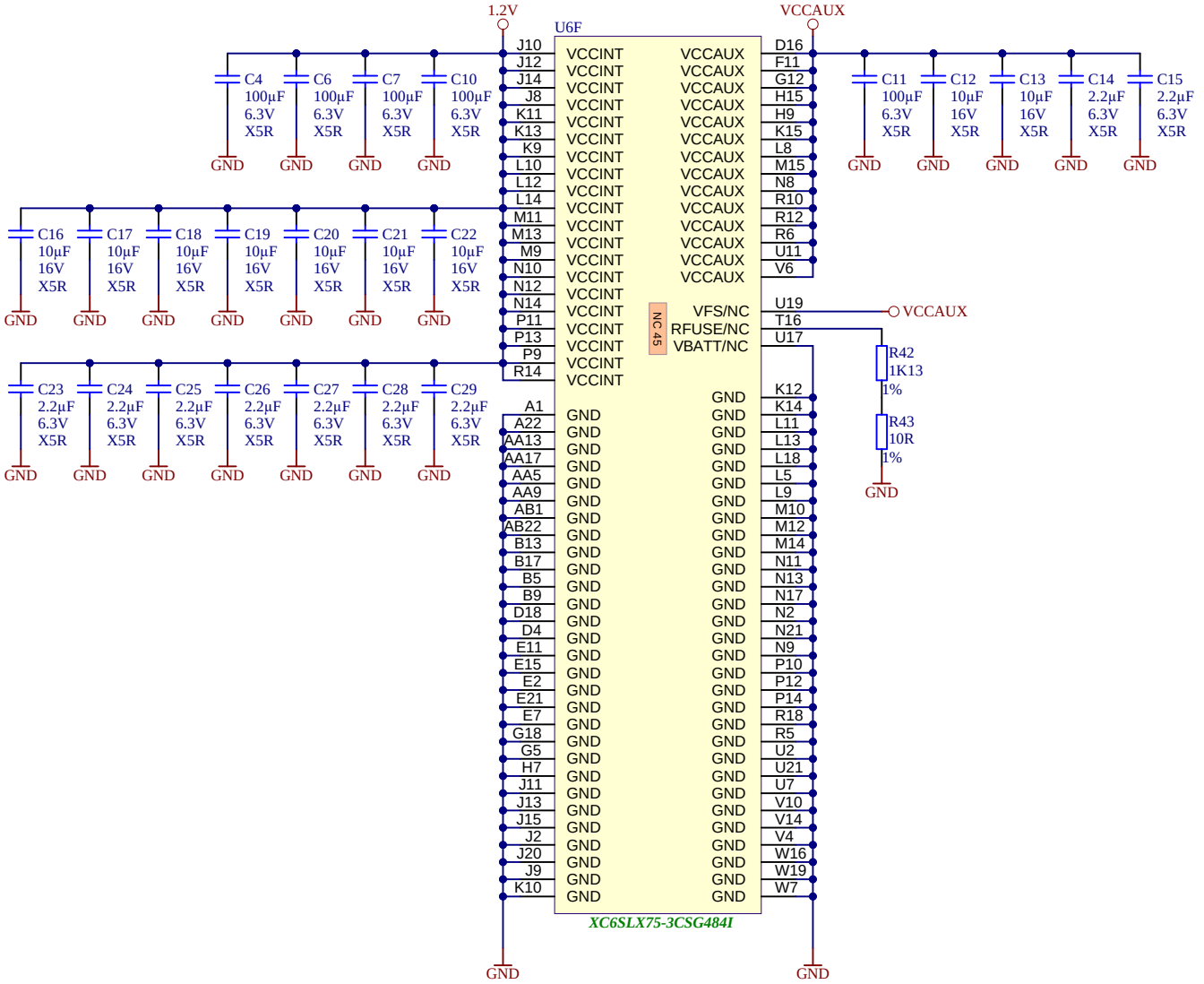
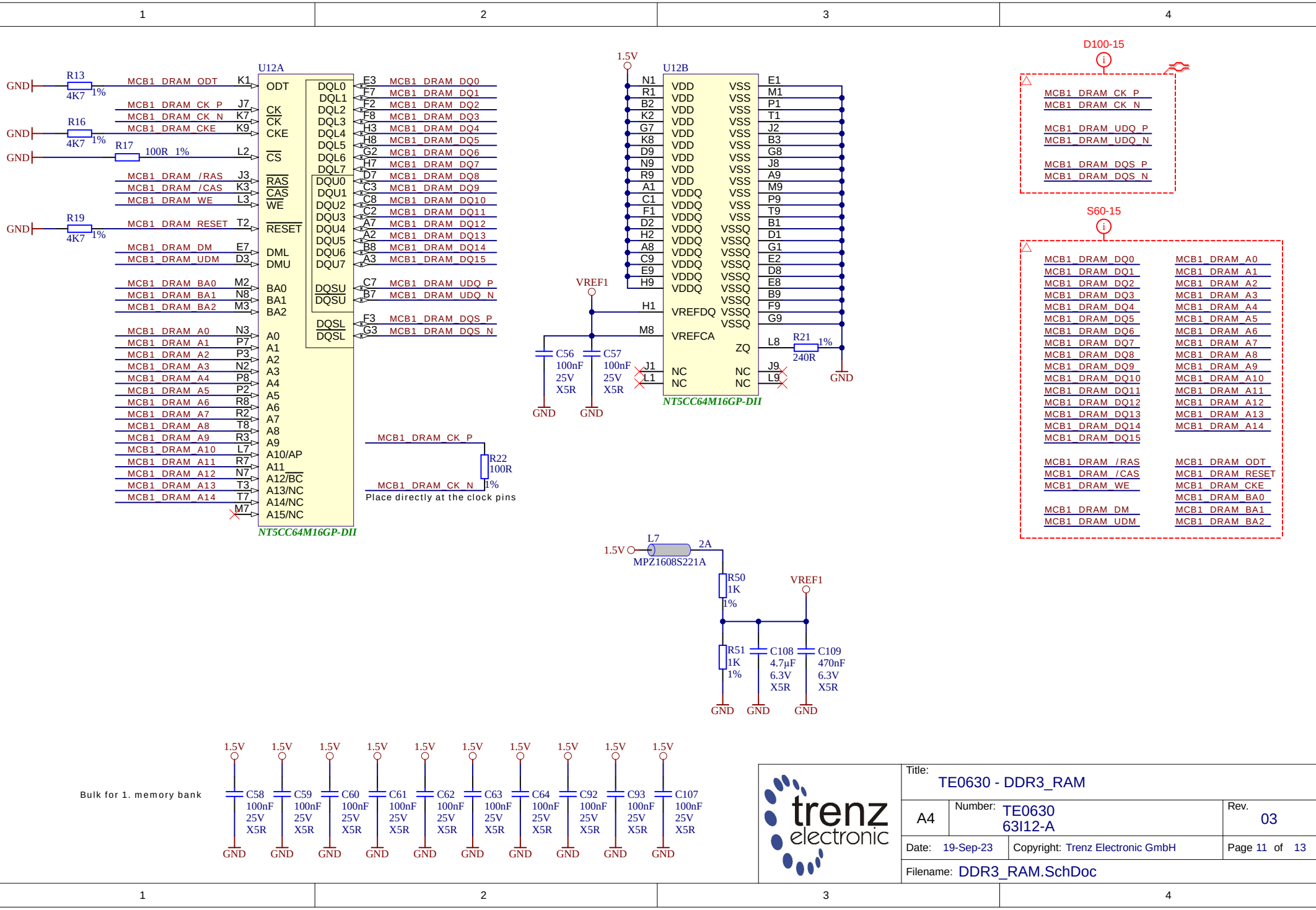
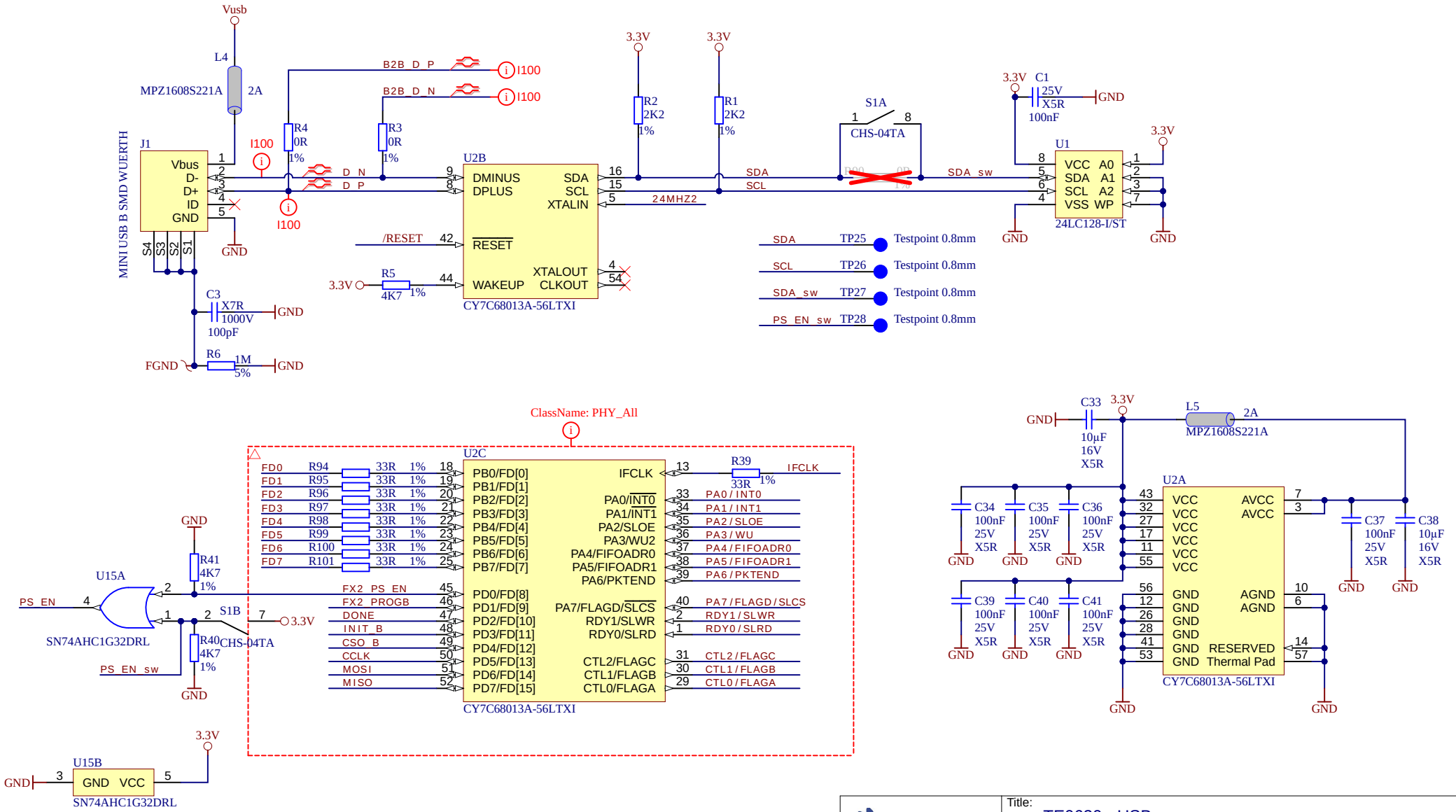
Filename: FPGA_B3.SchDoc



Title: TE0630 - FPGA_PWR		
A4	Number: TE0630 63I12-A	Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH	Page 10 of 13
Filename: FPGA_PWR.SchDoc		



Title: TE0630 - DDR3_RAM			
A4	Number: TE0630 63I12-A		Rev. 03
Date: 19-Sep-23	Copyright: Trenz Electronic GmbH		Page 11 of 13
Filename: DDR3_RAM.SchDoc			



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Title: TE0630 - USB			
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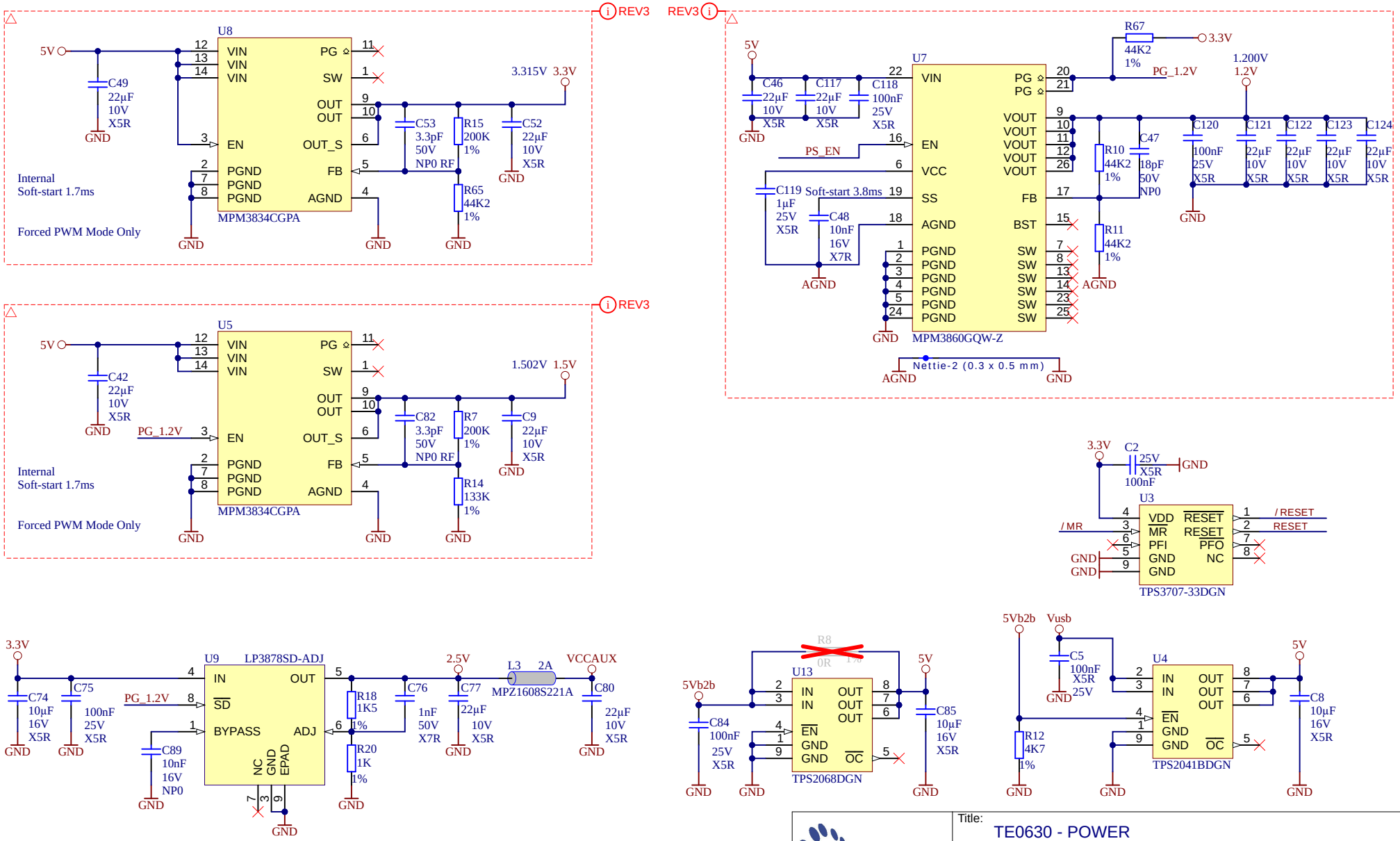
Filename: USB.SchDoc			



Title: TE0630 - POWER			
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Filename: Power.SchDoc			